800mA Single Resistor Rugged Linear Regulator with Monitors

FEATURES

- **Extended Safe Operating Area**
- **Maximum Output Current: 800mA**
- **Stable with or without Input/Output Capacitors**
- **Wide Input Voltage Range: 1.2V to 36V**
- **Single Resistor Sets Output Voltage**
- **Output Current Monitor: $I_{MON} = I_{OUT}/5000$**
- **Junction Temperature Monitor: 1µA/°C**
- **Output Adjustable to 0V**
- **50µA SET Pin Current: 1% Initial Accuracy**
- **Output Voltage Noise: 27µV_{RMS}**
- **Parallel Multiple Devices for Higher Current or Heat Spreading**
- **Programmable Current Limit**
- **Reverse-Battery and Reverse-Current Protection**
- <1mV Load Regulation Typical Independent of V_{OUT}
- <0.001%/V Line Regulation Typical
- Available in Thermally-Enhanced 12-Lead 4mm × 4mm DFN, 16-Lead TSSOP, and 7-Lead DD-Pak

APPLICATIONS

- All Surface Mount Power Supply
- Rugged Industrial Power Supply
- Post Regulator for Switching Supplies
- Low Output Voltage Supply
- Intrinsic Safety Applications

DESCRIPTION

The LT®3089 is an 800mA low dropout linear regulator designed for rugged industrial applications. Key features of the IC are the extended safe operating area (SOA), output current monitor, temperature monitor and programmable current limit. The LT3089 can be paralleled for higher output current or heat spreading. The device withstands reverse input and reverse output-to-input voltages without reverse current flow.

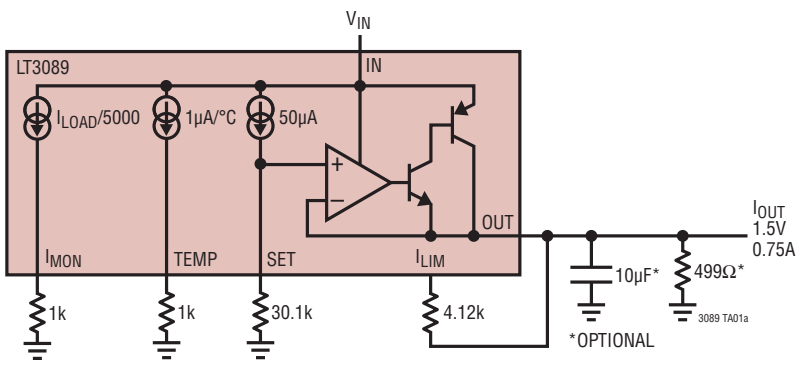
The LT3089's precision 50µA reference current source allows a single resistor to program output voltage to any level between zero and 34.5V. The current reference architecture enables load regulation to be independent of output voltage. The LT3089 is stable with or without input and output capacitors.

The output current monitor ($I_{OUT}/5000$) and die junction temperature output (1µA/°C) provide system monitoring and debug capability. In addition, a single resistor programs current limit.

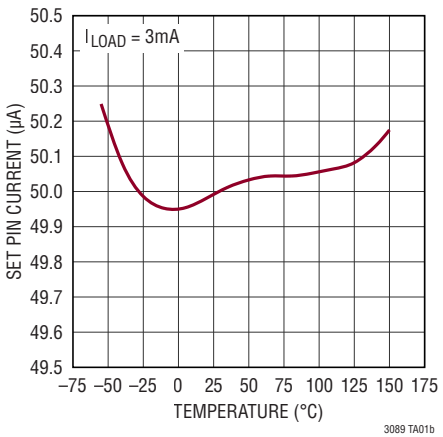
Internal protection circuitry includes reverse-battery and reverse-current protection, current limiting and thermal limiting. The LT3089 is offered in the 12-lead 4mm × 4mm DFN and 16-lead TSSOP (both with exposed pad for improved thermal performance), and 7-lead DD-Pak power package.

TYPICAL APPLICATION

Wide Safe Operating Area Supply



SET Pin Current

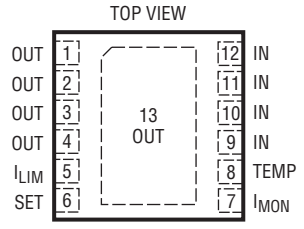


ABSOLUTE MAXIMUM RATINGS (Note 1) All voltages Relative to V_{OUT}.

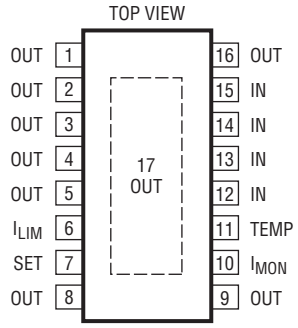
IN Pin to OUT Pin Differential Voltage ..... ±40V
SET Pin Current (Note 6) ..... ±25mA
SET Pin Voltage (Relative to OUT, Note 6) ..... ±10V
TEMP Pin Voltage (Relative to OUT) ..... 1V, –40V
I_{LIM} Pin Voltage (Relative to OUT) ..... ±0.2V
I_{MON} Pin Voltage (Relative to OUT) ..... 1V, –40V
Output Short-Circuit Duration ..... Indefinite

Operating Junction Temperature Range (Note 2)
E-, I-Grades ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)
FE, R Packages Only ..... 300°C

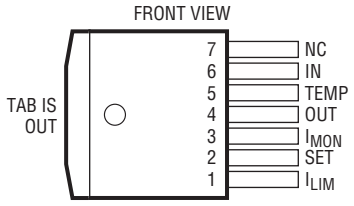
PIN CONFIGURATION



DF PACKAGE
12-LEAD (4mm × 4mm) PLASTIC DFN
T_{JMAX} = 125°C, θ_{JA} = 41°C/W, θ_{JC} = 1.6°C/W
EXPOSED PAD (PIN 13) IS OUT, MUST BE SOLDERED TO PCB



FE PACKAGE
16-LEAD PLASTIC TSSOP
T_{JMAX} = 125°C, θ_{JA} = 35°C/W, θ_{JC} = 2.3°C/W
EXPOSED PAD (PIN 17) IS OUT, MUST BE SOLDERED TO PCB



R PACKAGE
7-LEAD PLASTIC DD
T_{JMAX} = 125°C, θ_{JA} = 34°C/W, θ_{JC} = 3°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3089EDF#PBF	LT3089EDF#TRPBF	3089	12-Lead (4mm × 4mm) Plastic DFN	–40°C to 125°C
LT3089IDF#PBF	LT3089IDF#TRPBF	3089	12-Lead (4mm × 4mm) Plastic DFN	–40°C to 125°C
LT3089EFE#PBF	LT3089EFE#TRPBF	3089FE	16-Lead Plastic TSSOP	–40°C to 125°C
LT3089IFE#PBF	LT3089IFE#TRPBF	3089FE	16-Lead Plastic TSSOP	–40°C to 125°C
LT3089ER#PBF	LT3089ER#TRPBF	LT3089R	7-Lead Plastic DD-Pak	–40°C to 125°C
LT3089IR#PBF	LT3089IR#TRPBF	LT3089R	7-Lead Plastic DD-Pak	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_J = 25°C. (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SET Pin Current I_{SET}	V_{IN} = 2V, I_{LOAD} = 3mA 2V ≤ V_{IN} ≤ 36V, 3mA ≤ I_{LOAD} ≤ 800mA	 ●	49.5 48.75	50 50	50.5 51.25	µA µA
Offset Voltage (V_{OUT} – V_{SET}) V_{OS}	V_{IN} = 2V, I_{LOAD} = 3mA V_{IN} = 2V, I_{LOAD} = 3mA	 ●	–1.5 –3.5	0 0	1.5 3.5	mV mV
I_{SET} Load Regulation	ΔI_{LOAD} = 3mA to 800mA			–0.1		nA
V_{OS} Load Regulation (Note 7) ΔI_{LOAD} = 3mA to 800mA	DF, FE Packages	●		–0.5	–3	mV
	R Package	●		–1.5	–4	mV
Line Regulation ΔI_{SET} ΔV_{OS}	ΔV_{IN} = 2V to 36V, I_{LOAD} = 3mA ΔV_{IN} = 2V to 36V, I_{LOAD} = 3mA	 		1.5 0.001		nA/V mV/V
Minimum Load Current (Note 3)	2V ≤ V_{IN} ≤ 36V	●		1.1	3	mA
Dropout Voltage (Note 4)	I_{LOAD} = 100mA I_{LOAD} = 800mA	 ●		1.21 1.47	 1.65	V V
Internal Current Limit	V_{IN} = 5V, V_{SET} = 0V, V_{OUT} = –0.1V	●	0.8	1		A
I_{LIM} Programming Ratio		●	155	175	210	mA/kΩ
I_{LIM} Minimum Output Current Resistance				300		Ω
I_{MON} Full-Scale Output Current	I_{LOAD} = 800mA	●	130	160	190	µA
I_{MON} Scale Factor	100mA ≤ I_{LOAD} ≤ 800mA			200		µA/A
I_{MON} Operating Range		●	V_{OUT} – 40V		V_{OUT} + 0.4V	V
TEMP Output Current (Note 9)	T_J > 5°C			1		µA/°C
TEMP Output Current Absolute Error (Note 9)	0°C < T_J ≤ 125°C 125°C < T_J ≤ 150°C	 	–10 –15		10 15	µA µA
Reference Current RMS Output Noise (Note 5)	10Hz ≤ f ≤ 100kHz			5.7		nA_{RMS}
Error Amplifier RMS Output Noise (Note 5)	I_{LOAD} = 800mA, 10Hz ≤ f ≤ 100kHz, C_{OUT} =10µF, C_{SET} = 0.1µF			27		$µV_{RMS}$
Ripple Rejection V_{RIPPLE} = 0.5V_{P-P}, I_{LOAD} = 0.1A, C_{SET} = 0.1µF, C_{OUT}=10µF, V_{IN} = $V_{OUT(NOMINAL)}$ + 3V	f = 120Hz f = 10kHz f = 1MHz		75	90 75 20		dB dB dB
Thermal Regulation, I_{SET}	10ms Pulse			0.003		%/W

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Unless otherwise specified, all voltages are with respect to V_{OUT}. The LT3089 is tested and specified under pulse load conditions such that $T_J \approx T_A$. The LT3089E is tested at T_A = 25°C and performance is guaranteed from 0°C to 125°C. Performance of the LT3089E over the full –40°C and 125°C operating temperature range is assured by design, characterization, and correlation with statistical process controls. The LT3089I is guaranteed over the full –40°C to 125°C operating junction temperature range. High junction temperatures degrade operating lifetimes. Operating lifetime is degraded at junction temperatures greater than 125°C.

Note 3: Minimum load current is equivalent to the quiescent current of the part. Since all quiescent and drive current is delivered to the output of the part, the minimum load current is the minimum current required to maintain regulation.

Note 4: For the LT3089, dropout is specified as the minimum input-to-output voltage differential required supplying a given output current.

Note 5: Adding a small capacitor across the reference current resistor lowers output noise. Adding this capacitor bypasses the resistor shot noise and reference current noise; output noise is then equal to error amplifier noise (see Applications Information section).

Note 6: Diodes with series 400Ω resistors clamp the SET pin to the OUT pin. These diodes and resistors only carry current under transient overloads.

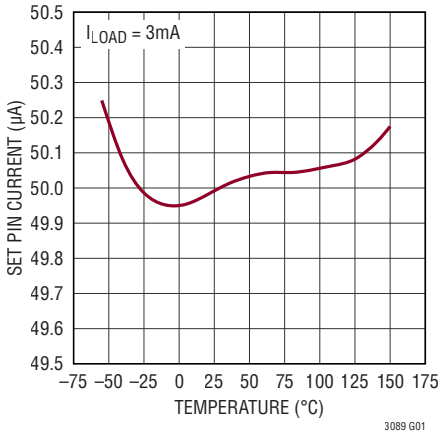
Note 7: Load regulation is Kelvin sensed at the package.

Note 8: This IC includes overtemperature protection that protects the device during momentary overload conditions. Junction temperature exceeds the maximum operating junction temperature when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

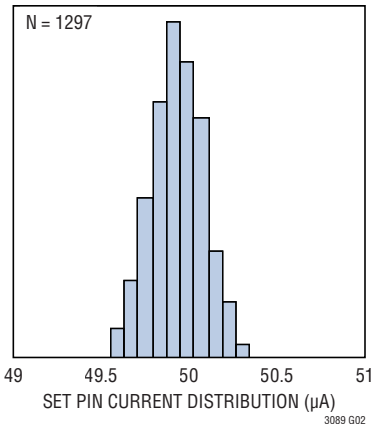
Note 9: The TEMP pin output current represents the average die junction temperature. Due to power dissipation and thermal gradients across the die, the TEMP pin output current measurement does not guarantee that absolute maximum junction temperature is not exceeded.

TYPICAL PERFORMANCE CHARACTERISTICS T_J = 25°C unless otherwise specified.

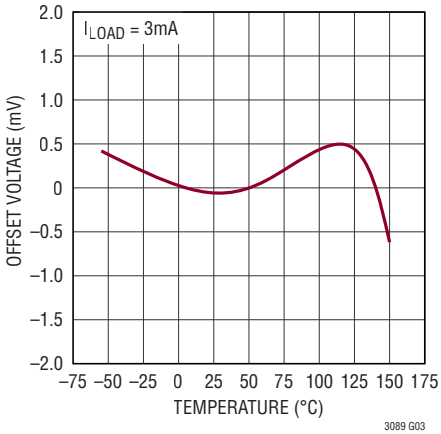
SET Pin Current



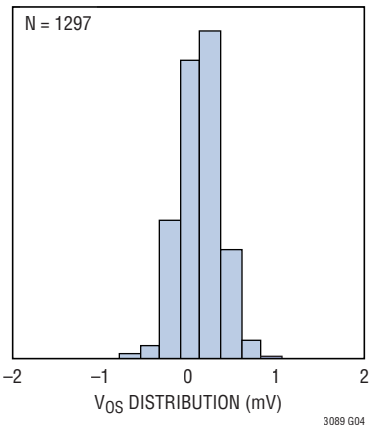
SET Pin Current



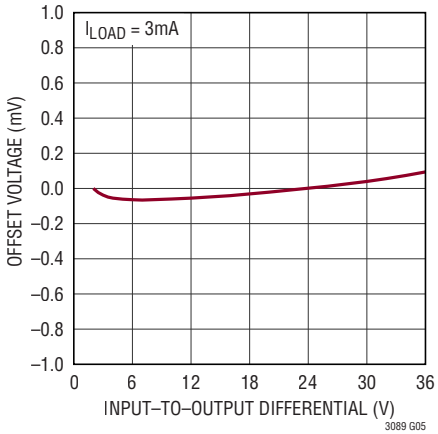
Offset Voltage (V_{OUT} – V_{SET})



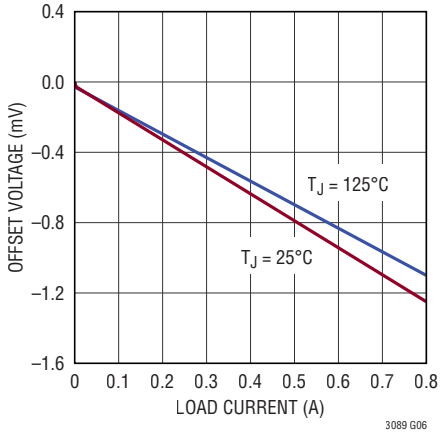
Offset Voltage



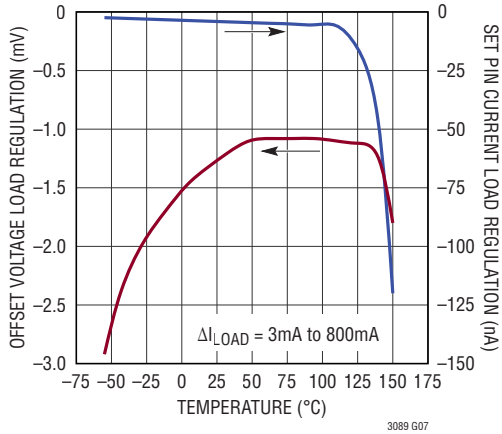
Offset Voltage (V_{OUT} – V_{SET})



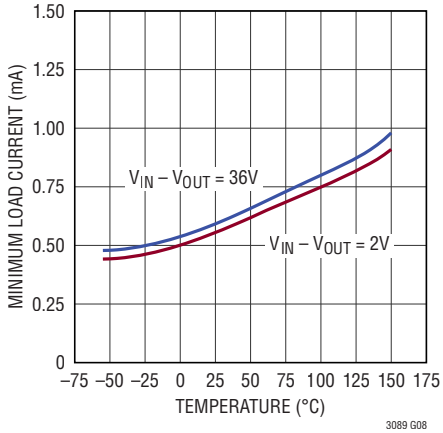
Offset Voltage (V_{OUT} – V_{SET})



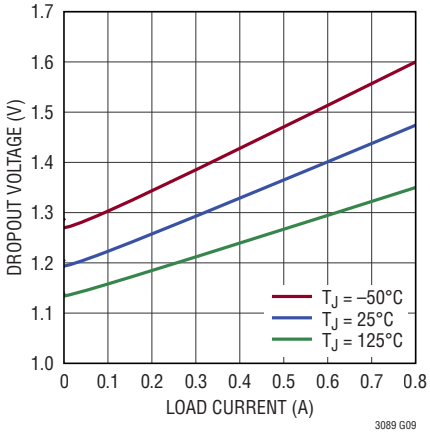
Load Regulation



Minimum Load Current



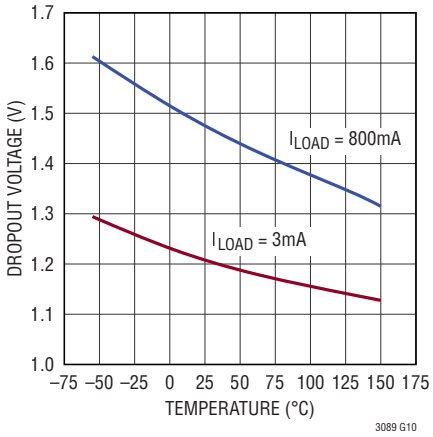
Dropout Voltage



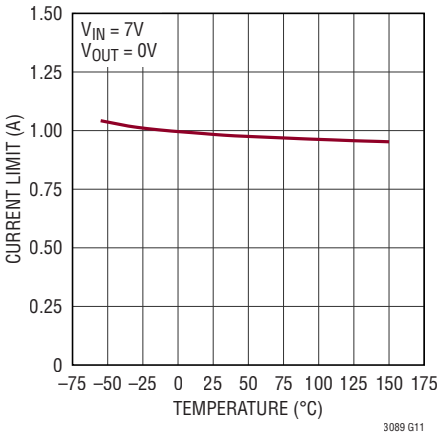
TYPICAL PERFORMANCE CHARACTERISTICS

T_J = 25°C unless otherwise specified.

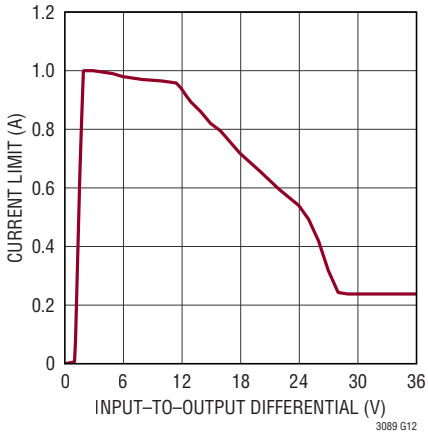
Dropout Voltage



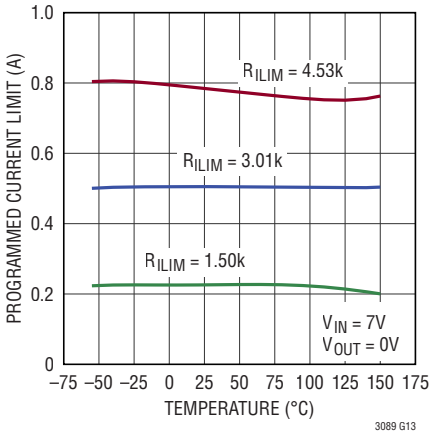
Internal Current Limit



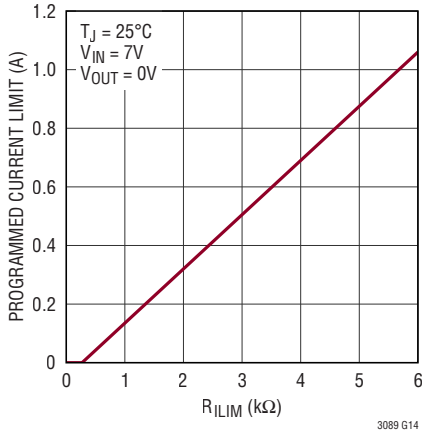
Internal Current Limit



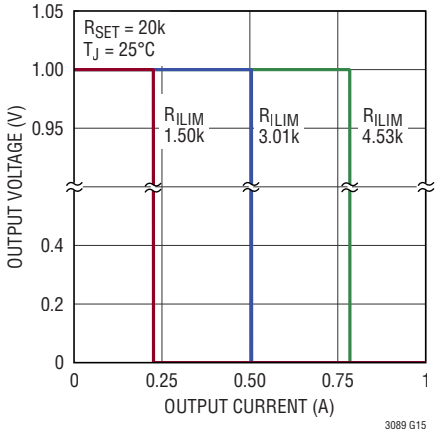
Programmable Current Limit



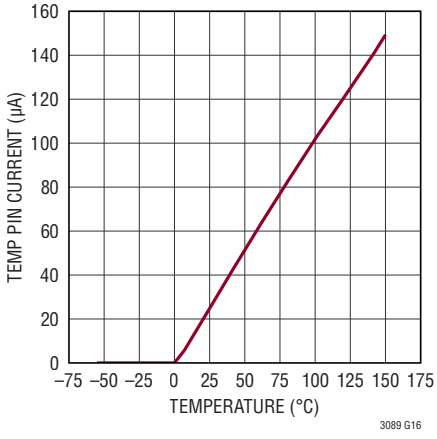
Programmable Current Limit



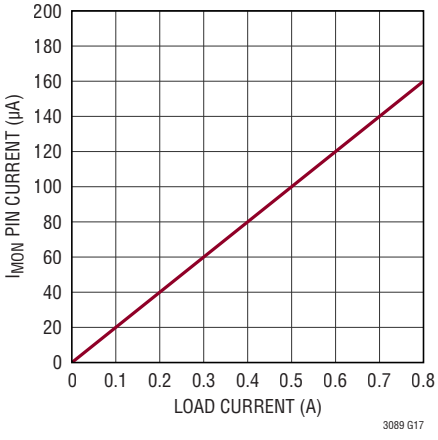
Programmable Current Limit



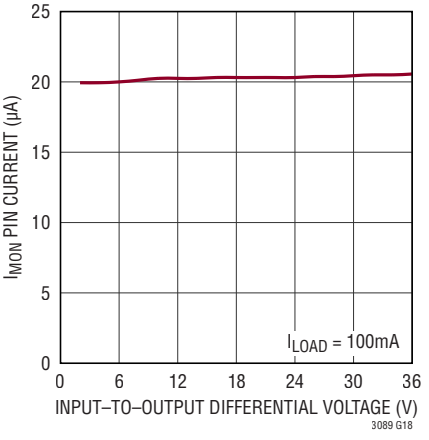
TEMP Pin Current



I_{MON} Pin Current



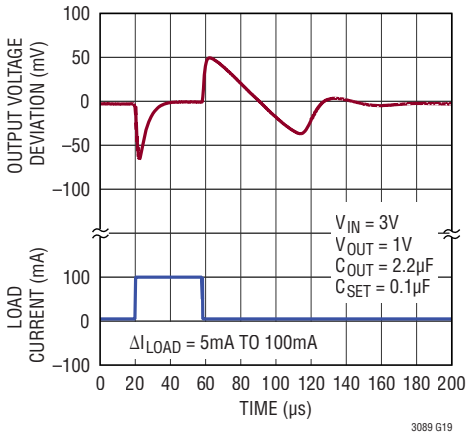
I_{MON} Pin Line Regulation



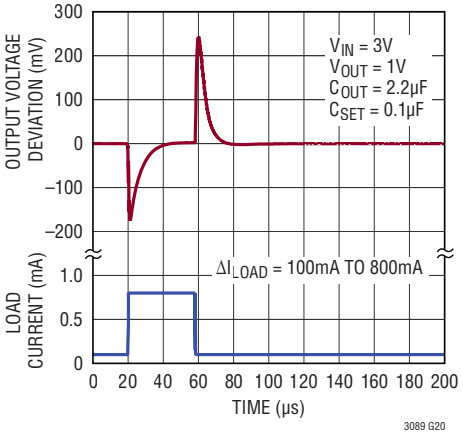
TYPICAL PERFORMANCE CHARACTERISTICS

T_J = 25°C unless otherwise specified.

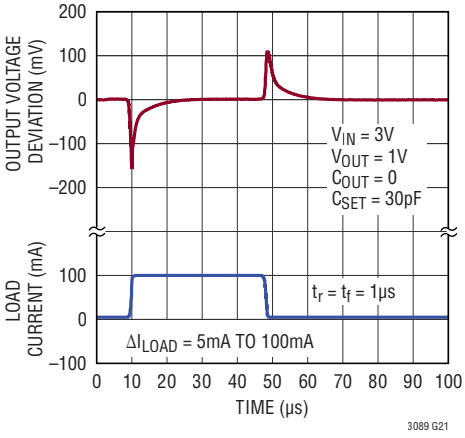
Linear Regulator Load Transient Response



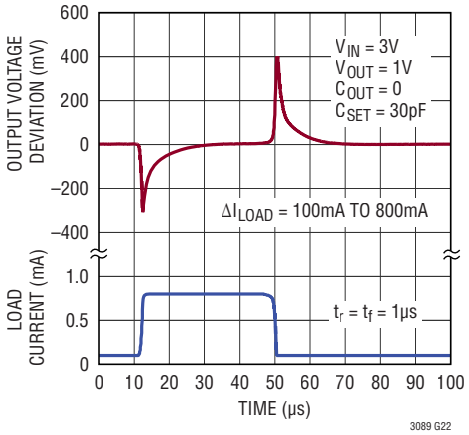
Linear Regulator Load Transient Response



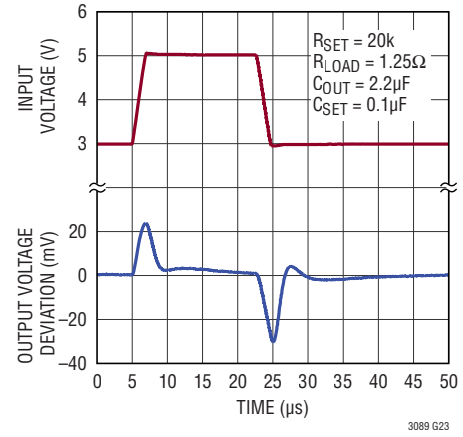
Linear Regulator Load Transient Response



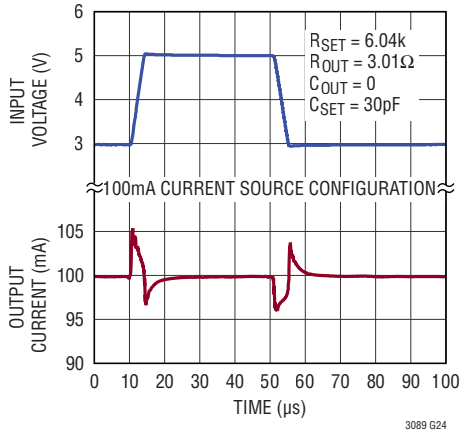
Linear Regulator Load Transient Response



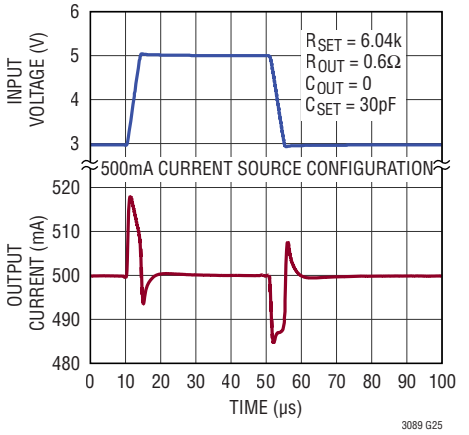
Linear Regulator Line Transient Response



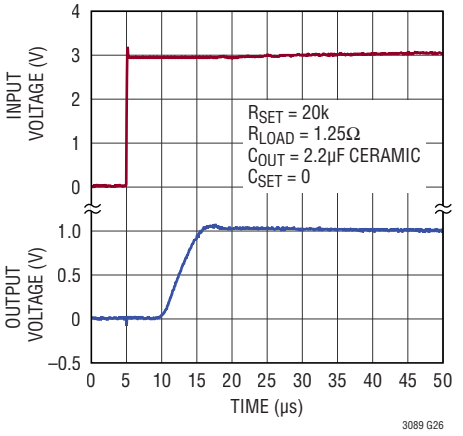
Current Source Line Transient Response



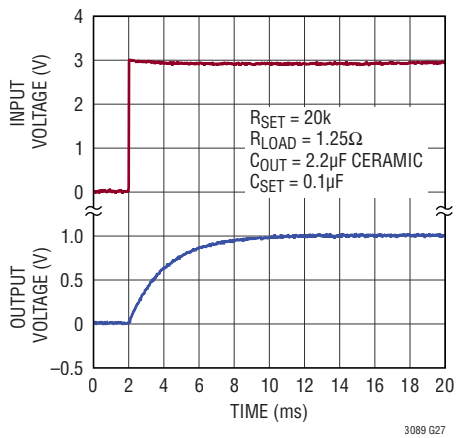
Current Source Line Transient Response



Linear Regulator Turn-On Response



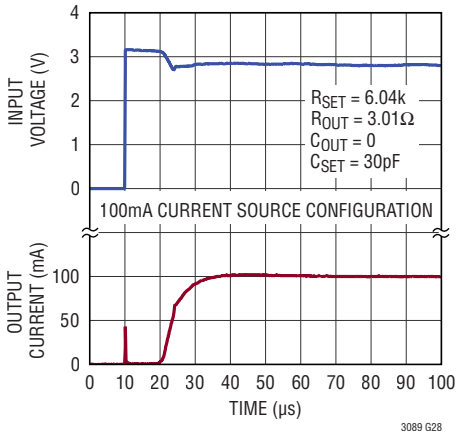
Linear Regulator Turn-On Response



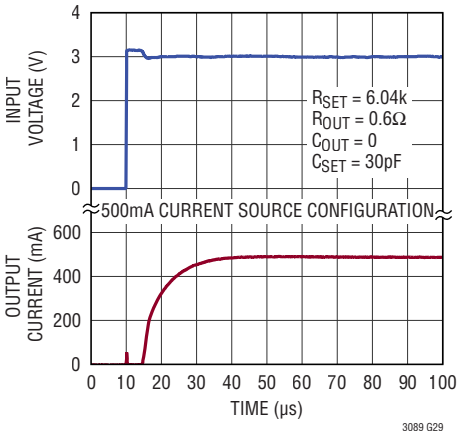
TYPICAL PERFORMANCE CHARACTERISTICS

T_J = 25°C unless otherwise specified.

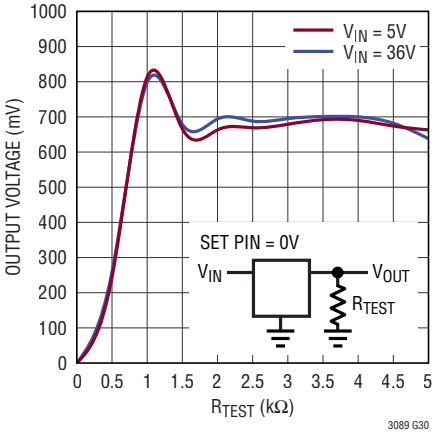
Current Source Turn-On Response



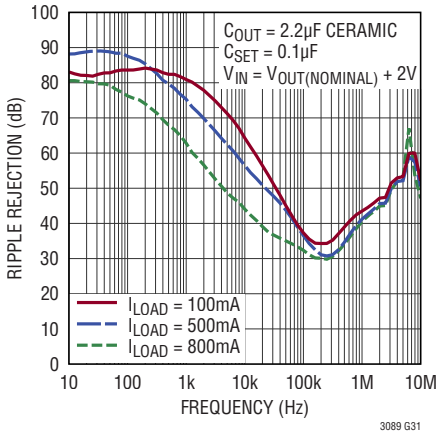
Current Source Turn-On Response



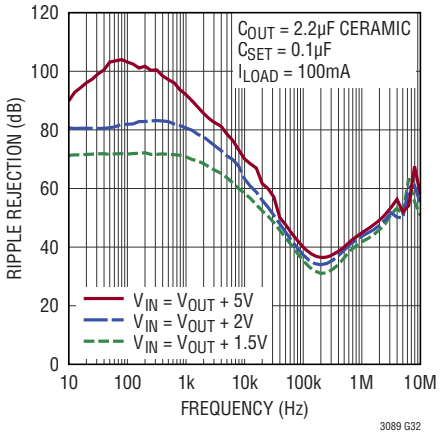
Residual Output Voltage with Less Than Minimum Load



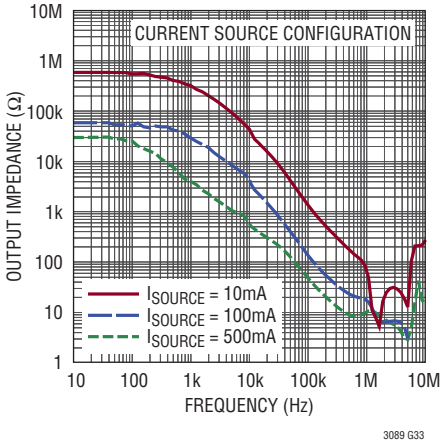
Ripple Rejection



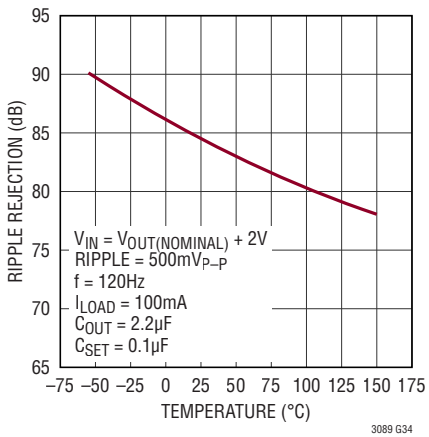
Ripple Rejection



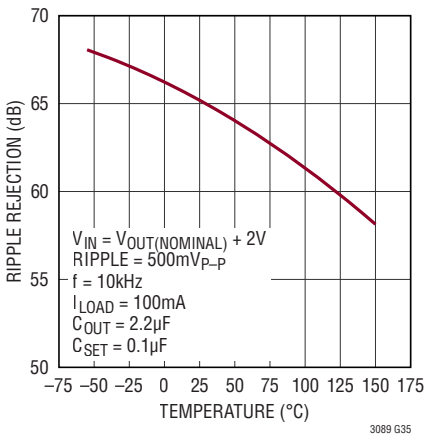
Output Impedance



Ripple Rejection (120Hz)

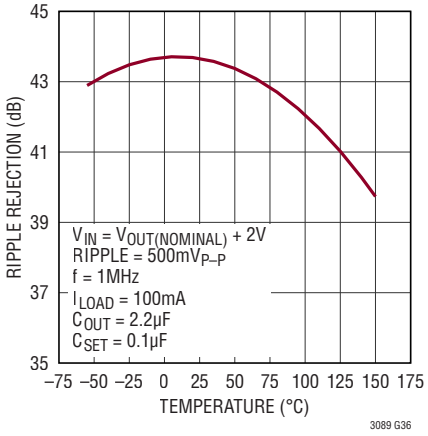


Ripple Rejection (10kHz)

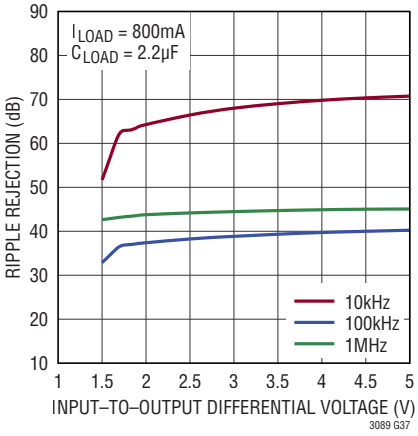


TYPICAL PERFORMANCE CHARACTERISTICS T_J = 25°C unless otherwise specified.

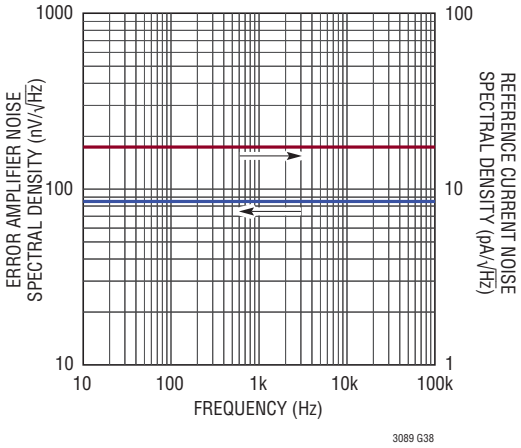
Ripple Rejection (1MHz)



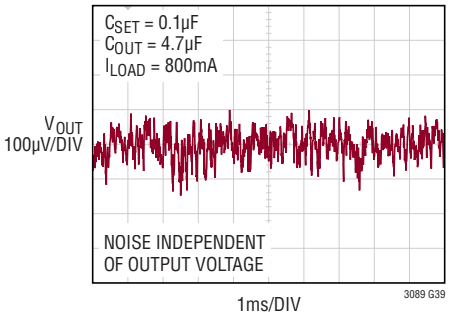
Ripple Rejection



Noise Spectral Density



10Hz to 100kHz Output Voltage Noise



PIN FUNCTIONS

IN: Input. This pin supplies power to regulate internal circuitry and supply output load current. For the device to operate properly and regulate, the voltage on this pin must be between the dropout voltage and 36V above the OUT pin (depending on output load current, see Dropout Voltage Specifications).

OUT: Output. This is the power output of the device. The LT3089 requires a 3mA minimum load current for proper output regulation.

TEMP: Temperature Output. This pin delivers a current proportional to the internal average junction temperature. Current output is 1µA/°C for temperatures above 5°C. The TEMP pin output current typically equals 25µA at 25°C. The output of the TEMP pin is valid for voltages from V_{OUT} + 0.4V to V_{OUT} – 40V. If unused, connect this pin to OUT.

I_{LIM}: Current Limit Program. A resistor between this pin and OUT programs output current limit to a level proportional to resistor value. Connect this resistor directly to OUT at the pins of the package. The typical ratio of current limit to resistor value is 175mA/kΩ with a 300Ω offset. If programmable current limit is not used, leave this pin open; the internal current limit of the LT3089 is still active, keeping the device inside safe operating limits. External voltage drops between the current limit resistor and V_{OUT} will affect the current limit. Keep drops below 1mV.

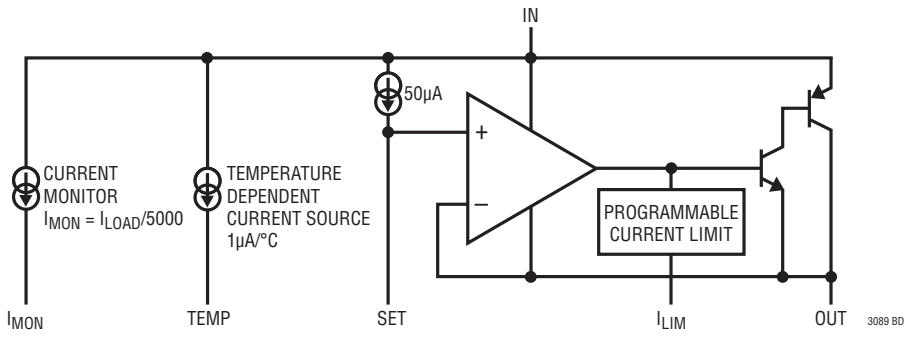
I_{MON}: Output Current Monitor. The I_{MON} pin sources a current typically equal to I_{LOAD}/5000 or 200µA per amp of output current. Terminating this pin with a resistor to GND produces a voltage proportional to I_{LOAD}. For example, at I_{LOAD} = 800mA, I_{MON} typically sources 160µA. With a 1k resistor to GND, this produces 160mV. The output of the I_{MON} pin is valid for voltages from V_{OUT} + 0.4V to V_{OUT} – 40V. If unused, connect this pin to OUT.

SET: Set. This pin is the error amplifier's noninverting input and also sets the operating bias point of the circuit. A fixed 50µA current source flows out of this pin. A single external resistor programs V_{OUT}. Output voltage range is 0V to 34.5V.

Exposed Pad/Tab: Output. The exposed pad of the DF and FE packages and the tab of the R package are tied internally to OUT. As such, tie them directly to OUT (Pins 1-4/Pins 1-5, 8, 9, 16/Pin 4) at the PCB. The amount of copper area and planes connected to OUT determine the effective thermal resistance of the packages.

NC: No Connection. No connect pins have no connection to internal circuitry and may be tied to IN, OUT, GND or floated.

BLOCK DIAGRAM



APPLICATIONS INFORMATION

Introduction

The LT3089 regulator is easy to use and has all the protection features expected in high performance regulators. Included are short-circuit protection, reverse-input protection and safe operating area protection, as well as thermal shutdown with hysteresis. Safe operating area (SOA) for the LT3089 is extended, allowing for use in harsh industrial and automotive environments where sudden spikes in input voltage lead to high power dissipation.

The LT3089 fits well in applications needing multiple rails. This new architecture adjusts down to zero with a single resistor, handling modern low voltage digital ICs as well as allowing easy parallel operation and thermal management without heat sinks. Adjusting to zero output allows shutting off the powered circuitry.

A precision "0" TC 50µA reference current source connects to the noninverting input of a power operational amplifier. The power operational amplifier provides a low impedance buffered output to the voltage on the noninverting input. A single resistor from the noninverting input to ground sets the output voltage. If this resistor is set to 0Ω, zero output voltage results. Therefore, any output voltage can be obtained between zero and the maximum defined by the input power supply is obtainable.

The benefit of using a true internal current source as the reference, as opposed to a bootstrapped reference in older regulators, is not so obvious in this architecture. A true reference current source allows the regulator to have gain and frequency response independent of the impedance on the positive input. On older adjustable regulators, such as the LT1086 loop gain changes with output voltage and bandwidth changes if the adjustment pin is bypassed to ground. For the LT3089, the loop gain is unchanged with output voltage changes or bypassing. Output regulation is not a fixed percentage of output voltage, but is a fixed fraction of millivolts. Use of a true current source allows all of the gain in the buffer amplifier to provide regulation, and none of that gain is needed to amplify up the reference to a higher output voltage.

The LT3089 has many additional features that facilitate monitoring and control. Current limit is externally programmable via a single resistor between the I_{LIM} pin and OUT. Shorting this resistor out disables all output current to the load, only bias currents remain.

The I_{MON} pin produces a current output proportional to load current. For every 100mA of load current, the I_{MON} pin sources 20µA of current. This can be sensed using an external resistor to monitor load requirements and detect potential faults. The I_{MON} pin can operate at voltages above OUT, so it operates even during a short-circuit condition.

One additional monitoring function is the TEMP pin, a current source that is proportional to average die temperature. For die temperatures above 0°C, the TEMP pin sources a current equal to 1µA/°C. This pin operates normally during output short-circuit conditions.

Programming Linear Regulator Output Voltage

The LT3089 generates a 50µA reference current that flows out of the SET pin. Connecting a resistor from SET to ground generates a voltage that becomes the reference point for the error amplifier (see Figure 1). The reference voltage equals 50µA multiplied by the value of the SET pin resistor. Any voltage can be generated and there is no minimum output voltage for the regulator.

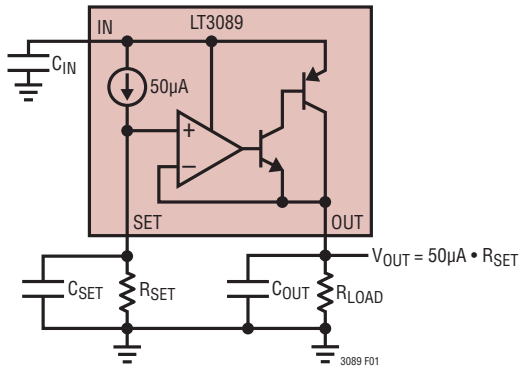


Figure 1. Basic Adjustable Regulator

APPLICATIONS INFORMATION

Table 1 lists many common output voltages and the closest standard 1% resistor values used to generate that output voltage.

Regulation of the output voltage requires a minimum load current of 3mA. For true zero voltage output operation, return this 3mA load current to a negative output voltage.

Table 1. 1% Resistors for Common Output Voltages

V_{OUT} (V)	R_{SET} (kΩ)
1	20
1.2	24.3
1.5	30.1
1.8	35.7
2.5	49.9
3.3	66.5
5	100

With the 50µA current source used to generate the reference voltage, leakage paths to or from the SET pin can create errors in the reference and output voltages. High quality insulation should be used (e.g., Teflon, Kel-F); cleaning of all insulating surfaces to remove fluxes and other residues is required. Surface coating may be necessary to provide a moisture barrier in high humidity environments.

Minimize board leakage by encircling the SET pin and circuitry with a guard ring operated at a potential close to itself. Tie the guard ring to the OUT pin. Guarding both sides of the circuit board is required. Bulk leakage reduction depends on the guard ring width. 50nA of leakage into or out of the SET pin and its associated circuitry creates a 0.1% reference voltage error. Leakages of this magnitude, coupled with other sources of leakage, can cause significant offset voltage and reference drift, especially over the possible operating temperature range. Figure 2 depicts an example guard ring layout.

If guard ring techniques are used, this bootstraps any stray capacitance at the SET pin. Since the SET pin is a high impedance node, unwanted signals may couple into the SET pin and cause erratic behavior. This will be most noticeable when operating with minimum output capacitors at full load current. The easiest way to remedy this is to bypass the SET pin with a small amount of capacitance from SET to ground, 10pF to 20pF is sufficient.

Configuring the LT3089 as a Current Source

Setting the LT3089 to operate as a 2-terminal current source is a simple matter. The 50µA reference current from the SET pin is used with one resistor to generate a small voltage, usually in the range of 100mV to 1V (200mV is a level that rejects offset voltage, line regulation, and other errors without being excessively large). This voltage is then applied across a second resistor that connect from OUT to the first resistor. Figure 3 shows connections and formulas to calculate a basic current source configuration.

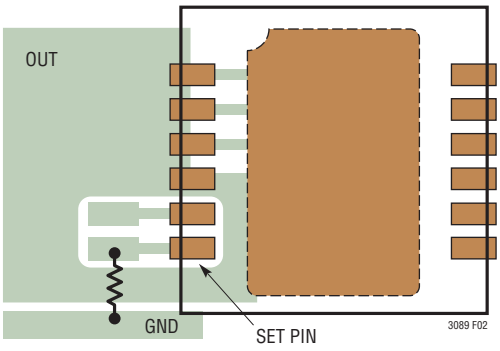
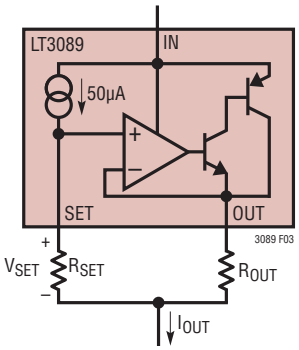


Figure 2. Guard Ring Layout Example of DF Package



$$I_{OUT} \geq 3mA$$

$$V_{SET} = 50\mu A \bullet R_{SET}$$

$$I_{OUT} = \frac{V_{SET}}{R_{OUT}} = \frac{50\mu A \bullet R_{SET}}{R_{OUT}}$$

Figure 3. Using the LT3089 as a Current Source

APPLICATIONS INFORMATION

Again, the lower current levels used in the LT3089 necessitate attention to board leakages as error sources (see the Programming Linear Regulator Output Voltage section).

In a current source configuration, programmable current limit and current monitoring functions are often unused. When not used, tie I_{MON} to OUT and leave I_{LIM} open. The TEMP pin is still available for use, if unused tie TEMP to OUT.

Selecting R_{SET} and R_{OUT} in Current Source Applications

In Figure 3, both resistors R_{SET} and R_{OUT} program the value of the output current. The question now arises: the ratio of these resistors is known, but what value should each resistor be?

The first resistor to select is R_{SET}. The value selected should generate enough voltage to minimize the error caused by the offset between the SET and OUT pins. A reasonable starting level is ~200mV of voltage across R_{SET} (R_{SET} equal to 4.02k). Resultant errors due to offset voltage are a few percent. The lower the voltage across R_{SET} becomes, the higher the error term due to the offset.

From this point, selecting R_{OUT} is easy, as it is a straightforward calculation from R_{SET}. Take note, however, resistor errors must be accounted for as well. While larger voltage drops across R_{SET} minimize the error due to offset, they also increase the required operating headroom.

Obtaining the best temperature coefficient does not require the use of expensive resistors with low ppm temperature coefficients. Instead, since the output current of the LT3089 is determined by the ratio of R_{SET} to R_{OUT}, those resistors should have matching temperature characteristics. Less expensive resistors made from the same material provide matching temperature coefficients. See resistor manufacturers' data sheets for more details.

Higher output currents necessitate the use of higher wattage resistors for R_{OUT}. There may be a difference between the resistors used for R_{OUT} and R_{SET}. A better method to maintain consistency in resistors is to use multiple resistors in parallel to create R_{OUT}, allowing the same wattage and type of resistor as R_{SET}.

Programming Current Limit Externally

A resistor placed between I_{LIM} and OUT on the LT3089 externally sets current limit to a level lower than the internal current limit. Connect this resistor directly at the OUT pins for best accuracy. The value of this resistor calculates as:

$$R_{ILIM} = I_{LIMIT}/175mA/k\Omega + 300\Omega$$

The resistor for a 0.5A current limit is: $R_{ILIM} = 0.5A/175mA/k\Omega + 300\Omega = 3.16k$. Tolerance over temperature is ±15%, so current limit is normally set 20% above maximum load current. The 300Ω offset resistance built in to the programmable current limit allows for lowering the maximum output current to only bias currents (see curve of Minimum Load Current in Typical Performance Characteristics) using external switches.

The LT3089's internal current limit overrides the programmed current limit if the input-to-output voltage differential in the power transistor is excessive. The internal current limit is ≈1A with a foldback characteristic dependent on input-to-output differential voltage, not output voltage *per se* (see Typical Performance Characteristics).

Stability and Input Capacitance

The LT3089 does not require an input capacitor to maintain stability. Input capacitors are recommended in linear regulator configurations to provide a low impedance input source to the LT3089. If using an input capacitor, low ESR, ceramic input bypass capacitors are acceptable for applications without long input leads. However, applications connecting a power supply to an LT3089 circuit's IN and GND pins with long input wires combined with low ESR, ceramic input capacitors are prone to voltage spikes, reliability concerns and application-specific board oscillations. The input wire inductance found in many battery-powered applications, combined with the low ESR ceramic input capacitor, forms a high Q LC resonant tank circuit. In some instances this resonant frequency beats against the output current dependent LDO bandwidth and interferes with proper operation. Simple circuit modifications/solutions are then required. This behavior is not indicative of LT3089 instability, but is a common ceramic input bypass capacitor application issue.

APPLICATIONS INFORMATION

The self-inductance, or isolated inductance, of a wire is directly proportional to its length. Wire diameter is not a major factor on its self-inductance. For example, the self-inductance of a 2-AWG isolated wire (diameter = 0.26") is about half the self-inductance of a 30-AWG wire (diameter = 0.01"). One foot of 30-AWG wire has about 465nH of self inductance.

One of two ways reduces a wire's self-inductance. One method divides the current flowing towards the LT3089 between two parallel conductors. In this case, the farther apart the wires are from each other, the more the self-inductance is reduced; up to a 50% reduction when placed a few inches apart. Splitting the wires basically connects two equal inductors in parallel, but placing them in close proximity gives the wires mutual inductance adding to the self-inductance. The second and most effective way to reduce overall inductance is to place both forward and return current conductors (the input and GND wires) in very close proximity. Two 30-AWG wires separated by only 0.02", used as forward and return current conductors, reduce the overall self-inductance to approximately one-fifth that of a single isolated wire.

If wiring modifications are not permissible for the applications, including series resistance between the power supply and the input of the LT3089 also stabilizes the application. As little as 0.1Ω to 0.5Ω, often less, is effective in damping the LC resonance. If the added impedance between the power supply and the input is unacceptable, adding ESR to the input capacitor also provides the necessary damping of the LC resonance. However, the required ESR is generally higher than the series impedance required.

Stability and Frequency Compensation for Linear Regulator Configurations

The LT3089 does not require an output capacitor for stability. LTC recommends an output capacitor of 10µF with an ESR of 0.5Ω or less to provide good transient performance in linear regulator configurations. Larger values of output capacitance decrease peak deviations and provide improved transient response for larger load current changes. Bypass capacitors, used to decouple individual components powered by the LT3089, increase the effective output capacitor value. For improvement in transient performance, place a capacitor across the voltage setting resistor. Capacitors up to 1µF can be used. This bypass capacitor reduces system noise as well, but start-up time is proportional to the time constant of the voltage setting resistor (R_{SET} in Figure 1) and SET pin bypass capacitor.

Stability and Frequency Compensation for Current Source Configurations

The LT3089 does not require input or output capacitors for stability in many current-source applications. Clean, tight PCB layouts provide a low reactance, well controlled operating environment for the LT3089 without requiring capacitors to frequency compensate the circuit. Figure 3 highlights the simplicity of using the LT3089 as a current source.

Some current source applications use a capacitor connected in parallel with the SET pin resistor to lower the current source's noise. This capacitor also provides a soft-start function for the current source. See Quieting the Noise section for further details. When operating without output capacitors, the high impedance nature of the SET pin as the input of the error amplifier allows signal from the output to couple in, showing as high frequency ringing during transients. Bypassing the SET resistor with a capacitor in the range of 20pF to 30pF dampens the ringing.

Depending on the pole introduced by a capacitor or other complex impedances presented to the LT3089, external compensation may be required for stability. Techniques are discussed to achieve this in the following paragraphs. Linear Technology strongly recommends testing stability in situ with final components before beginning production.

Although the LT3089's design strives to be stable without capacitors over a wide variety of operating conditions, it is not possible to test for all possible combinations of input and output impedances that the LT3089 will encounter. These impedances may include resistive, capacitive, and inductive components and may be complex distributed networks. In addition, the current source's value will differ between applications and its connection may be GND referenced, power supply referenced, or floating in a signal line path. Linear Technology strongly recommends that stability be tested in situ for any LT3089 application.

APPLICATIONS INFORMATION

In LT3089 applications with long wires or PCB traces, the inductive reactance may cause instability. In some cases, adding series resistance to the input and output lines (as shown in Figure 4) may sufficiently dampen these possible high-Q lines and provide stability. The user must evaluate the required resistor values against the design's headroom constraints. In general, operation at low output current levels (<20mA) automatically requires higher values of programming resistors and may provide the necessary damping without additional series impedance.

If the line impedances in series with the LT3089 are complex enough such that series damping resistors are not sufficient, a frequency compensation network may be necessary. Several options may be considered.

Figure 5 depicts the simplest frequency compensation networks as a single capacitor across the two terminals of the current source. Some applications may use the capacitance to stand off DC voltage but allow the transfer of data down a signal line.

For some applications, pure capacitance may be unacceptable or present a design constraint. One circuit example typifying this is an "intrinsically-safe" circuit in which an overload or fault condition potentially allows the capacitor's stored energy to create a spark or arc. For applications where a single capacitor is unacceptable, Figure 5 alternately shows a series RC network connected across the two terminals of the current source. This network has the added benefit of limiting the discharge current of the capacitor under a fault condition, preventing sparks or arcs. In many instances, a series RC network is the best solution for stabilizing the application circuit. Typical resistor values will range from 100Ω to 5k. Once again, Linear Technology strongly recommends testing stability in situ for any LT3089 application across all operating conditions, especially ones that present complex impedance networks at the input and output of the current source.

If an application refers the bottom of the LT3089 current source to GND, it may be necessary to bypass the top of the current source with a capacitor to GND. In some cases, this capacitor may already exist and no additional capacitance is required. For example, if the LT3089 was used as a variable current source on the output of a power supply, the output bypass capacitance would suffice to provide LT3089 stability. Other applications may require the addition of a bypass capacitor. A series RC network may also be used as necessary, and depends on the application requirements.

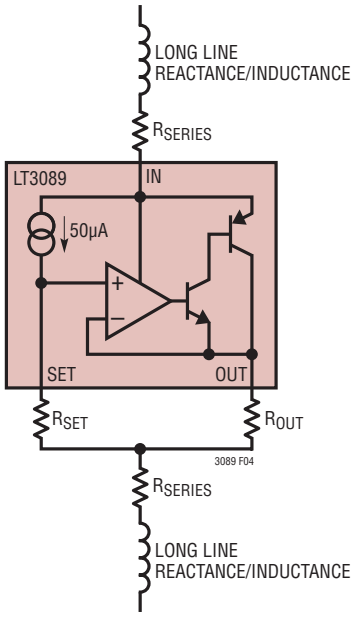


Figure 4. Adding Series Resistance Decouples and Dampens Long Line Reactances

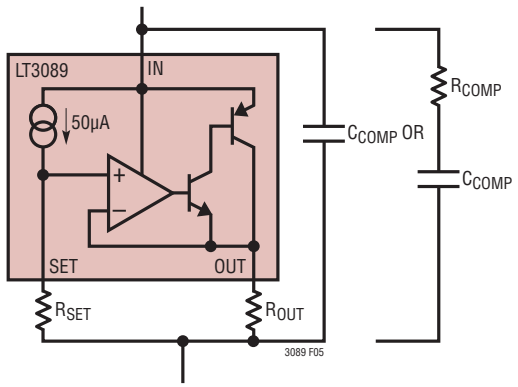


Figure 5. Compensation from Input to Output of Current Source Provides Stability

APPLICATIONS INFORMATION

In some extreme cases, capacitors or series RC networks may be required on both the LT3089's input and output to stabilize the circuit. Figure 6 depicts a general application using input and output capacitor networks rather than an input-to-output capacitor. As the input of the current source tends to be high impedance, placing a capacitor on the input does not have the same effect as placing a capacitor on the lower impedance output. Capacitors in the range of 0.1µF to 1µF usually provide sufficient bypassing on the input, and the value of input capacitance may be increased without limit. Pay careful attention to using low ESR input capacitors with long input lines (see the Stability and Input Capacitance section for more information).

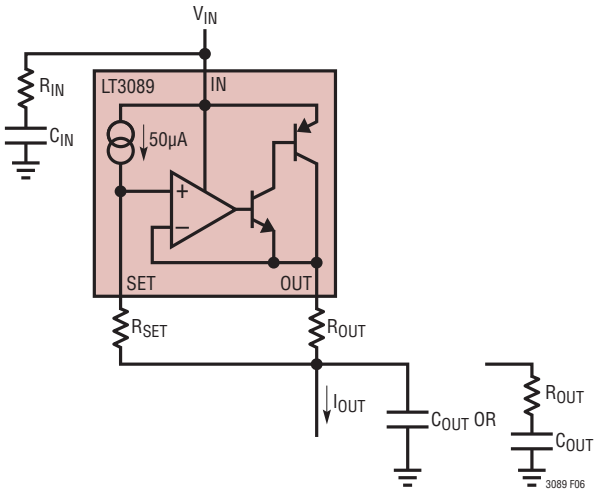


Figure 6. Input and/or Output Capacitors May Be Used for Compensation

Using Ceramic Capacitors

Give extra consideration to the use of ceramic capacitors. Ceramic capacitors are manufactured with a variety of dielectrics, each with different behavior across temperature and applied voltage. The most common dielectrics used are specified with EIA temperature characteristic codes of Z5U, Y5V, X5R and X7R. The Z5U and Y5V dielectrics are good for providing high capacitances in a small package, but they tend to have strong voltage and temperature coefficients as shown in Figures 7 and 8. When used with a 5V regulator, a 16V 10µF Y5V capacitor can exhibit an effective value as low as 1µF to 2µF for the DC bias voltage applied and over the operating temperature range. The X5R and X7R dielectrics result in more stable characteristics and are more suitable for use as the output capacitor. The X7R type has better stability across temperature, while the X5R is less expensive and is available in higher values. Care still must be exercised when using X5R and X7R capacitors. The X5R and X7R codes only specify operating temperature range and maximum capacitance change over temperature. Capacitance change due to DC bias with X5R and X7R capacitors is better than Y5V and Z5U capacitors, but can still be significant enough to drop capacitor values below appropriate levels. Capacitor DC bias characteristics tend to improve as component case size increases, but expected capacitance at operating voltage should be verified.

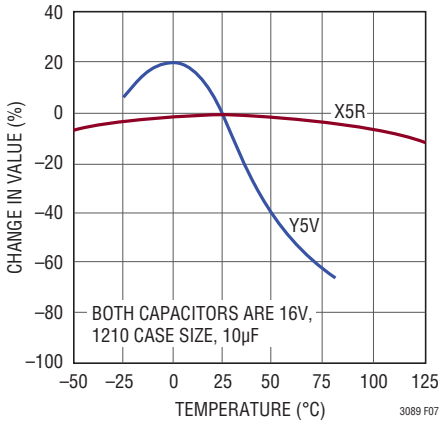


Figure 7. Ceramic Capacitor Temperature Characteristics

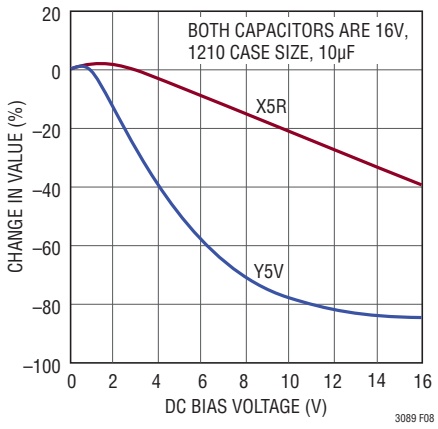


Figure 8. Ceramic Capacitor DC Bias Characteristics

APPLICATIONS INFORMATION

Voltage and temperature coefficients are not the only sources of problems. Some ceramic capacitors have a piezoelectric response. A piezoelectric device generates voltage across its terminals due to mechanical stress. In a ceramic capacitor, the stress can be induced by vibrations in the system or thermal transients.

Paralleling Devices

Higher output current is obtained by paralleling multiple LT3089s together. Tie the individual SET pins together and tie the individual IN pins together. Connect the outputs in common using small pieces of PC trace as ballast resistors to promote equal current sharing. PC trace resistance in milliohms/inch is shown in Table 2. Ballasting requires only a tiny area on the PCB.

Table 2. PC Board Trace Resistance

WEIGHT (oz)	10mil WIDTH	20mil WIDTH
1	54.3	27.1
2	27.1	13.6

Trace resistance is measured in mΩ/in.

The worst-case room temperature offset, only ±1.5mV between the SET pin and the OUT pin, allows the use of very small ballast resistors.

As shown in Figure 9, each LT3089 has a small 20mΩ ballast resistor, which at full output current gives better than 80% equalized sharing of the current. The external resistance of 20mΩ (10mΩ for the two devices in parallel) only adds about 16mV of output regulation drop at an output of 1.6A. Even with an output voltage as low as 1V, this only adds 1.6% to the regulation. Of course, paralleling more than two LT3089s yields even higher output current. Spreading the devices on the PC board also spreads the heat. Series input resistors can further spread the heat if the input-to-output difference is high.

If the increase in load regulation from the ballast resistors is unacceptable, the I_{MON} output can be used to compensate for these drops (see Using I_{MON} Cancels Ballast Resistor Drop in the Typical Applications section). Regulator paralleling without the use of ballast resistors is accomplished by comparing the I_{MON} outputs of regulators (see Load Current Sharing Without Ballasting in the Typical Applications section).

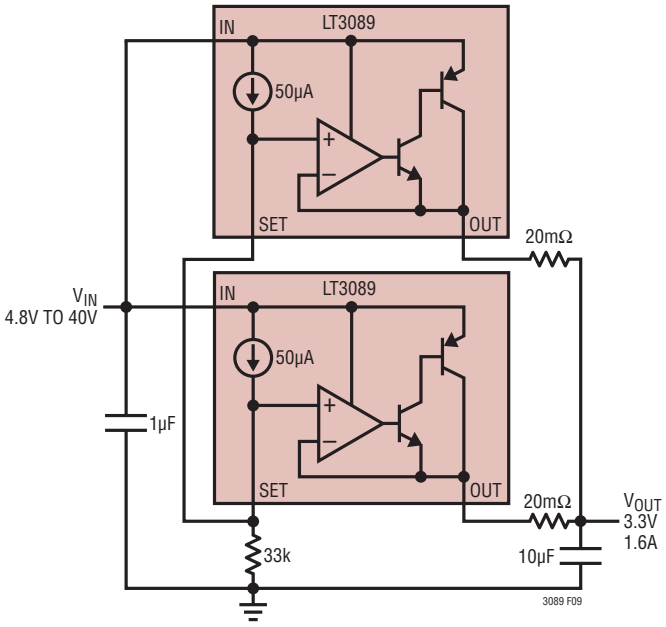


Figure 9. Parallel Devices

Quieting the Noise

The LT3089 offers numerous noise performance advantages. Every linear regulator has its sources of noise. In general, a linear regulator's critical noise source is the reference. In addition, consider the error amplifier's noise contribution along with the resistor divider's noise gain.

Many traditional low noise regulators bond out the voltage reference to an external pin (usually through a large value resistor) to allow for bypassing and noise reduction. The LT3089 does not use a traditional voltage reference like other linear regulators. Instead, it uses a 50µA reference current. The 50µA current source generates noise current levels of 18pA/$\sqrt{Hz}$ (5.7nA$_{RMS}$ over a 10Hz to 100kHz bandwidth). The equivalent voltage noise equals the RMS noise current multiplied by the resistor value.

The SET pin resistor generates spot noise equal to $\sqrt{4kTR}$ (k = Boltzmann's constant, $1.38 \cdot 10^{-23}$J/°K, and T is absolute temperature) which is RMS summed with the voltage noise. If the application requires lower noise performance, bypass the voltage setting resistor with a capacitor to GND. Note that this noise-reduction capacitor increases start-up time as a factor of the RC time constant.

APPLICATIONS INFORMATION

The LT3089 uses a unity-gain follower from the SET pin to the OUT pin. Therefore, multiple possibilities exist (besides a SET pin resistor) to set output voltage. For example, using a high accuracy voltage reference from SET to GND removes the errors in output voltage due to reference current tolerance and resistor tolerance. Active driving of the SET pin is acceptable.

The typical noise scenario for a linear regulator is that the output voltage setting resistor divider gains up the reference noise, especially if V_{OUT} is much greater than V_{REF}. The LT3089's noise advantage is that the unity-gain follower presents no noise gain whatsoever from the SET pin to the output. Thus, noise figures do not increase accordingly. Error amplifier noise is typical 85nV/$\sqrt{Hz}$(27μV_{RMS} over a 10Hz to 100kHz bandwidth). The error amplifier's noise is RMS summed with the other noise terms to give a final noise figure for the regulator.

Paralleling of regulators adds the benefit that output noise is reduced. For n regulators in parallel, the output noise drops by a factor of $\sqrt{n}$.

Curves in the Typical Performance Characteristics section show noise spectral density and peak-to-peak noise characteristics for both the reference current and error amplifier over a 10Hz to 100kHz bandwidth.

Load Voltage Regulation

The LT3089 is a floating device. No ground pin exists on the packages. Thus, the IC delivers all quiescent current and drive current to the load. Therefore, it is not possible to provide true remote load sensing. The connection resistance between the regulator and the load determines load regulation performance. The data sheet's load regulation specification is Kelvin sensed at the package's pins. Negative-side sensing is a true Kelvin connection by returning the bottom of the voltage setting resistor to the negative side of the load (see Figure 10).

Connected as shown, system load regulation is the sum of the LT3089's load regulation and the parasitic line resistance multiplied by the output current. To minimize load regulation, keep the positive connection between the regulator and load as short as possible. If possible, use large diameter wire or wide PC board traces.

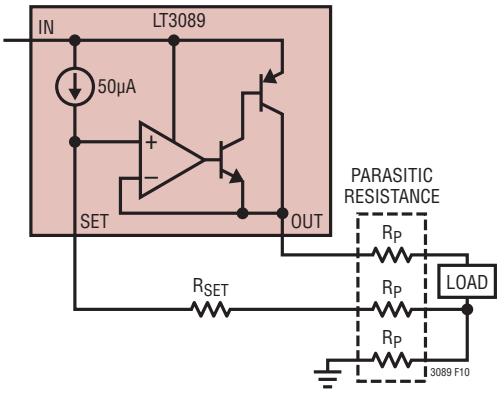


Figure 10. Connections for Best Load Regulation

TEMP Pin Operation (Die Temperature Monitor)

The TEMP pin of the LT3089 outputs a current proportional to average die temperature. At 25°C, the current from the TEMP pin is 25µA, with a slope of 1µA/°C. The current out of the TEMP pin is valid for junction temperatures above 0°C (absent initial offset considerations). Below 0°C, the TEMP pin will not sink current to indicate die temperature. The TEMP pin output current is valid for voltages up to 40V below and 0.4V above the OUT pin allowing operation even during short-circuit conditions.

Connecting a resistor from TEMP to ground converts the TEMP pin current into a voltage to allow for monitoring by an ADC. With a 1k resistor, 0mV to 150mV indicates 0°C to 150°C.

It should be noted that the TEMP pin current represents an average temperature and should not be used to guarantee that maximum junction temperature is not exceeded. Instantaneous power along with thermal gradients and time constants may cause portions of the die to exceed maximum ratings and thermal shutdown thresholds. Be sure to calculate die temperature rise for steady state (>1 minute) as well as impulse conditions.

I_{MON} Pin Operation (Current Monitor)

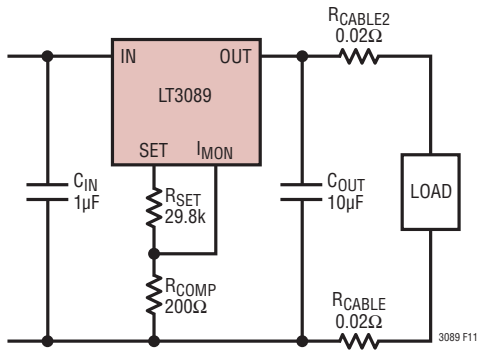
The LT3089's I_{MON} pin outputs a current proportional to the load current supplied at a ratio of 1:5000. The I_{MON} pin current is valid for voltages up to 40V below and 0.4V above the OUT pin, allowing operation even during short-circuit conditions.

APPLICATIONS INFORMATION

Connecting a resistor from I_{MON} to ground converts the I_{MON} pin current into a voltage to allow for monitoring by an ADC. With a 1k resistor, 0mV to 160mV indicates 0A to 800mA of load current.

Compensating for Cable Drops with I_{MON}

The I_{MON} pin can compensate for resistive drops in wires or cables between the LT3089 and the load. Breaking the SET resistor into two pieces adjusts the output voltage as a function of load current. The ratio of the output wire/cable impedance to the bottom resistor should be 1:5000. The sum total of the two SET resistor values determines the initial output voltage. Figure 11 shows a typical application and formulas for calculating resistor values.



$R_{COMP} = 5000 \bullet R_{CABLE(TOTAL)}$

$V_{OUT(LOAD)} = 50\mu A\ (R_{SET} + R_{COMP})$

Figure 11. Using I_{MON} to Compensate for Cable Drops

Thermal Considerations

The LT3089's internal power and thermal limiting circuitry protects itself under overload conditions. For continuous normal load conditions, do not exceed the 125°C (E- and I-grades) maximum junction temperature. Carefully consider all sources of thermal resistance from junction-to-ambient. This includes (but is not limited to) junction-to-case, case-to-heat sink interface, heat sink resistance or circuit board-to-ambient as the application dictates. Consider all additional, adjacent heat generating sources in proximity on the PCB.

Surface mount packages provide the necessary heat sinking by using the heat spreading capabilities of the PC board, copper traces and planes. Surface mount heat sinks, plated through-holes and solder-filled vias can also spread the heat generated by power devices.

Junction-to-case thermal resistance is specified from the IC junction to the bottom of the case directly, or the bottom of the pin most directly in the heat path. This is the lowest thermal resistance path for heat flow. Only proper device mounting ensures the best possible thermal flow from this area of the packages to the heat sinking material.

Note that the exposed pad of the DFN and TSSOP packages and the tab of the DD-Pak package are electrically connected to the output (V_{OUT}).

Tables 3 through 5 list thermal resistance as a function of copper areas on a fixed board size. All measurements were taken in still air on a 4-layer FR-4 board with 1oz solid internal planes and 2oz external trace planes with a total finished board thickness of 1.6mm.

Table 3. DF Package, 12-Lead DFN

COPPER AREA			
TOPSIDE*	BACKSIDE	BOARD AREA	THERMAL RESISTANCE (JUNCTION-TO-AMBIENT)
2500mm^2	2500mm^2	2500mm^2	21°C/W
1000mm^2	2500mm^2	2500mm^2	24°C/W
225mm^2	2500mm^2	2500mm^2	30°C/W
100mm^2	2500mm^2	2500mm^2	35°C/W

*Device is mounted on topside

Table 4. FE Package, 16-Lead TSSOP

COPPER AREA			
TOPSIDE*	BACKSIDE	BOARD AREA	THERMAL RESISTANCE (JUNCTION-TO-AMBIENT)
2500mm^2	2500mm^2	2500mm^2	18°C/W
1000mm^2	2500mm^2	2500mm^2	22°C/W
225mm^2	2500mm^2	2500mm^2	27°C/W
100mm^2	2500mm^2	2500mm^2	32°C/W

*Device is mounted on topside

Table 5. R Package, 7-Lead DD-Pak

COPPER AREA			
TOPSIDE*	BACKSIDE	BOARD AREA	THERMAL RESISTANCE (JUNCTION-TO-AMBIENT)
2500mm^2	2500mm^2	2500mm^2	13°C/W
1000mm^2	2500mm^2	2500mm^2	14°C/W
225mm^2	2500mm^2	2500mm^2	16°C/W

*Device is mounted on topside

APPLICATIONS INFORMATION

For further information on thermal resistance and using thermal information, refer to JEDEC standard JESD51, notably JESD51-12.

PCB layers, copper weight, board layout and thermal vias affect the resultant thermal resistance. Tables 3 through 5 provide thermal resistance numbers for best-case 4-layer boards with 1oz internal and 2oz external copper. Modern, multilayer PCBs may not be able to achieve quite the same level performance as found in these tables. Demo circuit 2318A's board layout using multiple inner V_{OUT} planes and multiple thermal vias achieves 17°C/W performance for the DF package.

Calculating Junction Temperature

Example: Given an output voltage of 0.9V, an IN voltage of 2.5V ±5%, output current range from 10mA to 0.8A and a maximum ambient temperature of 50°C, what is the maximum junction temperature for the DD-Pak on a 2500mm^2 board with topside copper of 1000mm^2?

The power in the circuit equals:

$$P_{TOTAL} = (V_{IN} - V_{OUT})(I_{OUT})$$

The current delivered to the SET pin is negligible and can be ignored.

$$V_{IN(MAX\_CONTINUOUS)} = 2.625V\ (2.5V + 5\%)$$

$$V_{OUT} = 0.9V,\ I_{OUT} = 0.8A,\ T_A = 50°C$$

Power dissipation under these conditions equals:

$$P_{TOTAL} = (V_{IN} - V_{OUT})(I_{OUT})$$

$$P_{TOTAL} = (2.625V - 0.9V)(0.8A) = 1.38W$$

Junction Temperature equals:

$$T_J = T_A + P_{TOTAL} \bullet \theta_{JA} \text{ (using tables)}$$

$$T_J = 50°C + 1.38W \bullet 14°C/W = 69.3°C$$

In this case, the junction temperature is below the maximum rating, ensuring reliable operation.

Reducing Power Dissipation

In some applications it may be necessary to reduce the power dissipation in the LT3089 package without sacrificing output current capability. Two techniques are available. The first technique, illustrated in Figure 12, employs a resistor in series with the regulator's input. The voltage drop across R_S decreases the LT3089's IN-to-OUT differential voltage and correspondingly decreases the LT3089's power dissipation.

As an example, assume: $V_{IN} = 7V$, $V_{OUT} = 3.3V$ and $I_{OUT(MAX)} = 0.8A$. Use the formulas from the Calculating Junction Temperature section previously discussed.

Without series resistor R_S, power dissipation in the LT3089 equals:

$$P_{TOTAL} = (7V - 3.3V) \bullet 0.8A = 2.96W$$

If the voltage differential (V_{DIFF}) across the LT3089 is chosen as 1.5V, then R_S equals:

$$R_S = \frac{7V - 3.3V - 1.5V}{0.8A} = 2.8\Omega$$

Power dissipation in the LT3089 now equals:

$$P_{TOTAL} = 1.5V \bullet 0.8A = 1.2W$$

The LT3089's power dissipation is now only 40% compared to no series resistor. R_S dissipates 1.8W of power. Choose appropriate wattage resistors or use multiple resistors in parallel to handle and dissipate the power properly.

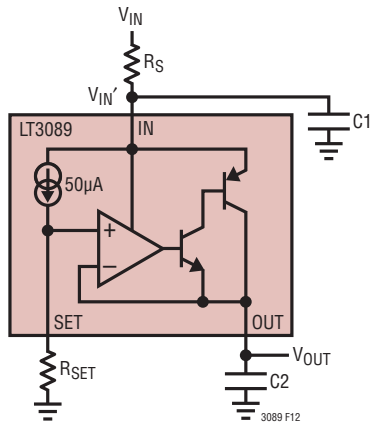


Figure 12. Reducing Power Dissipation Using a Series Resistor

APPLICATIONS INFORMATION

The second technique for reducing power dissipation, shown in Figure 13, uses a resistor in parallel with the LT3089. This resistor provides a parallel path for current flow, reducing the current flowing through the LT3089. This technique works well if input voltage is reasonably constant and output load current changes are small. This technique also increases the maximum available output current at the expense of minimum load requirements.

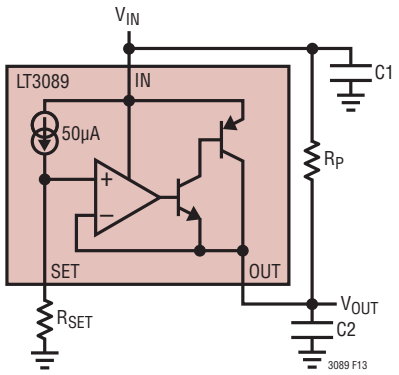


Figure 13. Reducing Power Dissipation Using a Parallel Resistor

As an example, assume: V_{IN} = 5V, $V_{IN(MAX)}$ = 5.5V, V_{OUT} = 3.3V, $V_{OUT(MIN)}$ = 3.2V, $I_{OUT(MAX)}$ = 0.8A and $I_{OUT(MIN)}$ = 0.4A. Also, assuming that R_P carries no more than 90% of $I_{OUT(MIN)}$ = 360mA.

Calculating R_P yields:

$$R_P = \frac{5.5V - 3.2V}{0.36A} = 6.39\Omega$$

(5% Standard value = 6.2Ω)

The maximum total power dissipation is:

(5.5V – 3.2V) • 0.8A = 1.84W

However, the LT3089 supplies only:

$$0.8A - \frac{5.5V - 3.2V}{6.2\Omega} = 0.43A$$

Therefore, the LT3089's power dissipation is only:

P_{DISS} = (5.5V – 3.2V) • 0.43A = 0.99W

R_P dissipates 0.85W of power. As with the first technique, choose appropriate wattage resistors to handle and dissipate the power properly. With this configuration, the LT3089 supplies only 0.43A. Therefore, load current can increase by 0.37A to a total output current of 1.17A while keeping the LT3089 in its normal operating range.

Protection Features

The LT3089 incorporates several protection features ideal for harsh industrial and automotive environments, among other applications. In addition to normal monolithic regulator protection features such as current limiting and thermal limiting, the LT3089 protects itself against reverse-input voltages, reverse-output voltages, and large OUT-to-SET pin voltages.

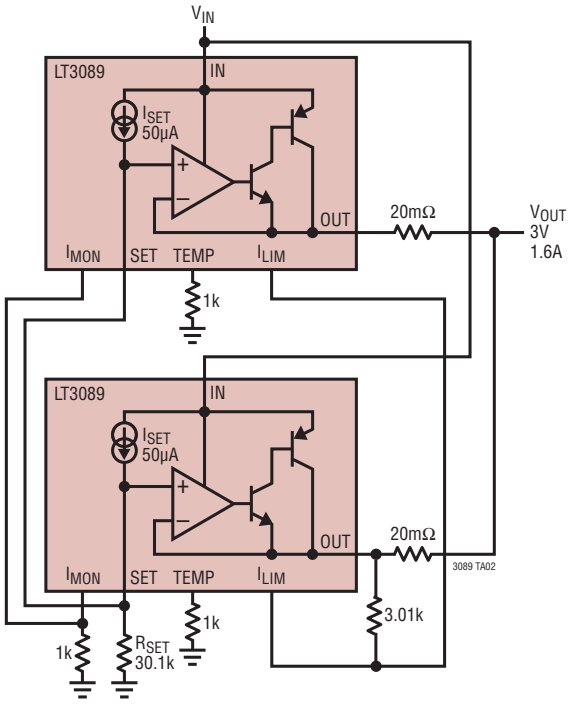
Current limit protection and thermal overload protection protect the IC against output current overload conditions. For normal operation, do not exceed the rated absolute maximum junction temperature. The thermal shutdown circuit's temperature threshold is typically 165°C and incorporates about 5°C of hysteresis.

The LT3089's IN pin withstands ±40V voltages with respect to the OUT and SET pins. Reverse current flow, if OUT is greater than IN, is less than 1mA (typically under 100µA), protecting the LT3089 and sensitive loads.

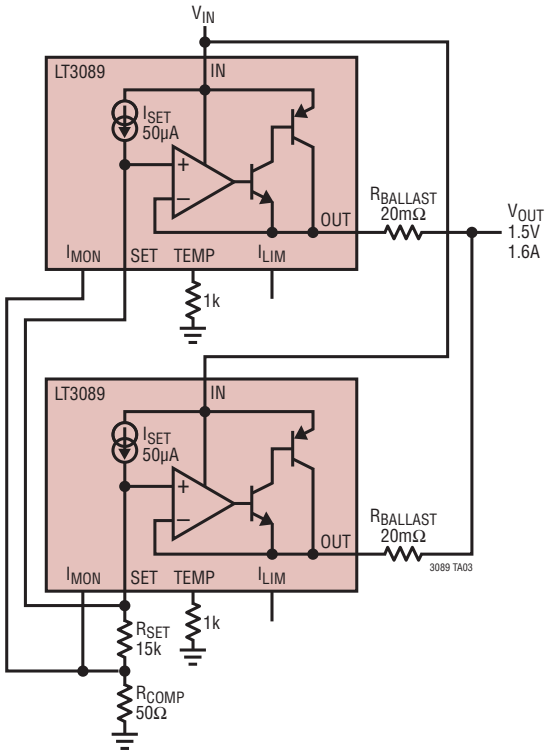
Clamping diodes and 400Ω limiting resistors protect the LT3089's SET pin relative to the OUT pin voltage. These protection components typically only carry current under transient overload conditions. These devices are sized to handle ±10V differential voltages and ±25mA crosspin current flow without concern. Relative to these application concerns, note the following two scenarios. The first scenario employs a noise-reducing SET pin bypass capacitor while OUT is instantaneously shorted to GND. The second scenario follows improper shutdown techniques in which the SET pin is reset to GND quickly while OUT is held up by a large output capacitance with light load.

TYPICAL APPLICATIONS

Paralleling Regulators

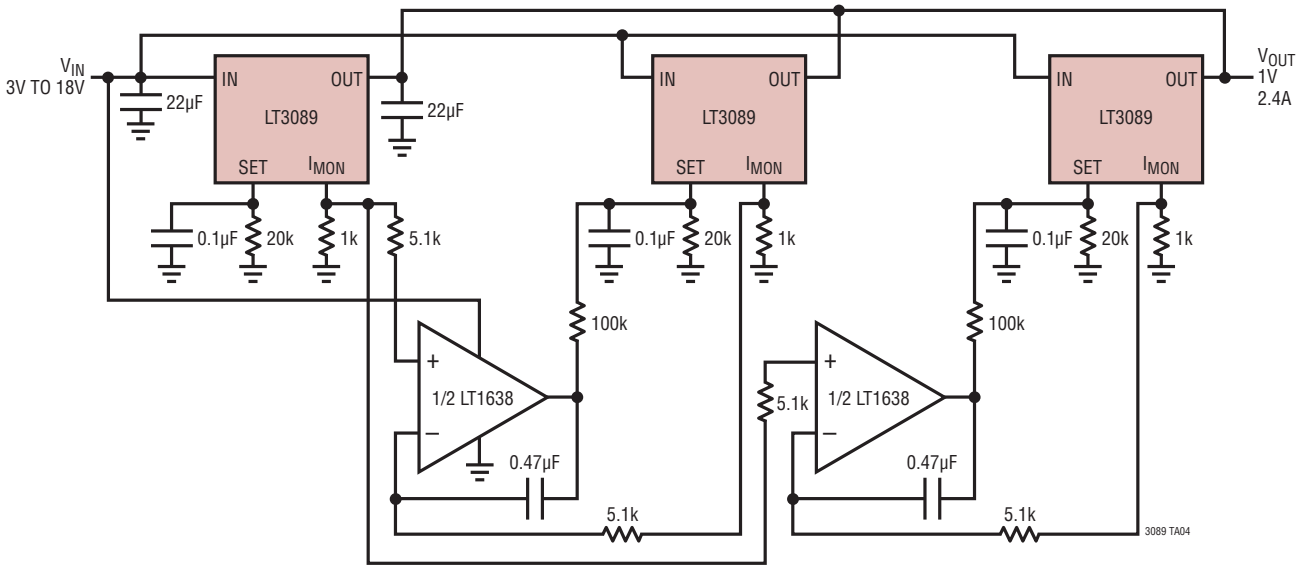


Using I_{MON} Cancels Ballast Resistor Drop

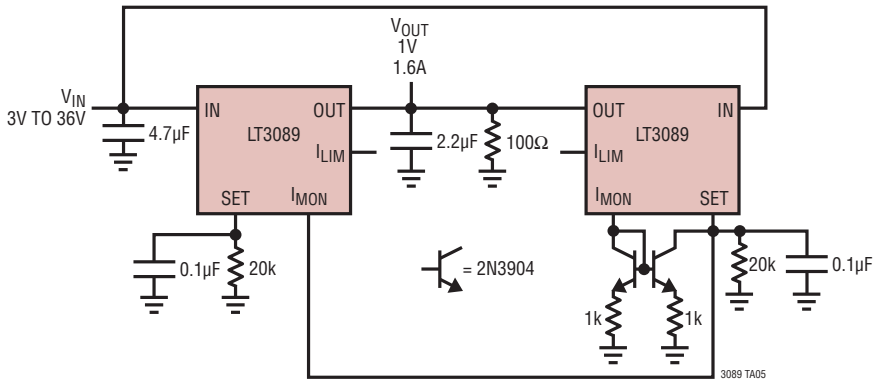


TYPICAL APPLICATIONS

Load Sharing Without Ballast Resistors

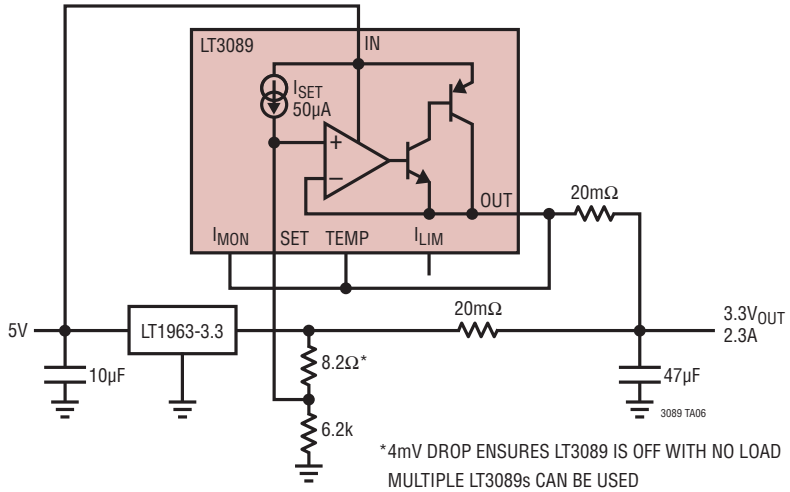


Load Current Sharing Without Ballasting

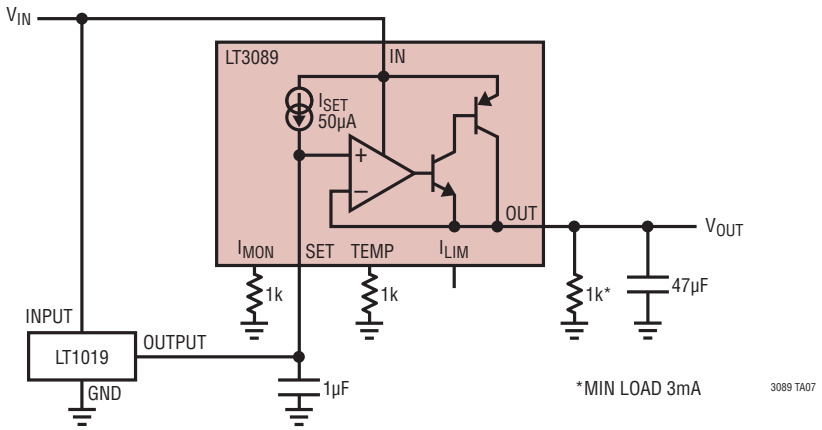


TYPICAL APPLICATIONS

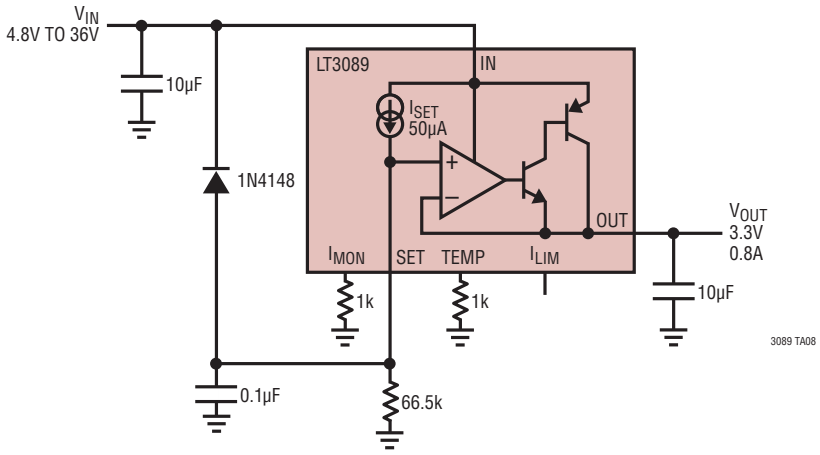
Boosting Fixed Output Regulators



Reference Buffer

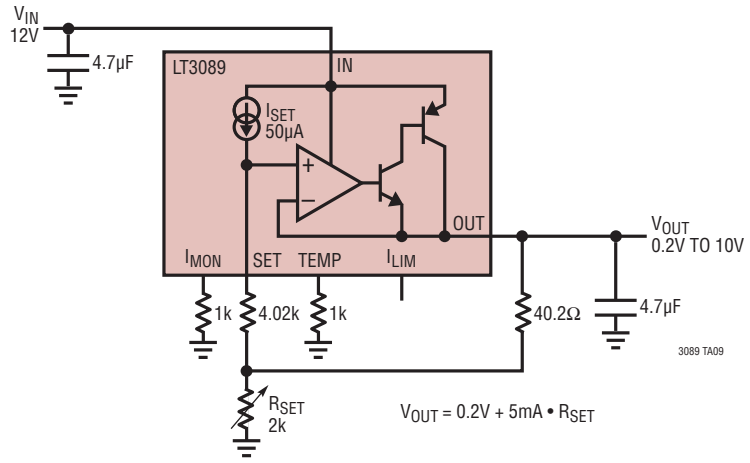


Adding Soft-Start

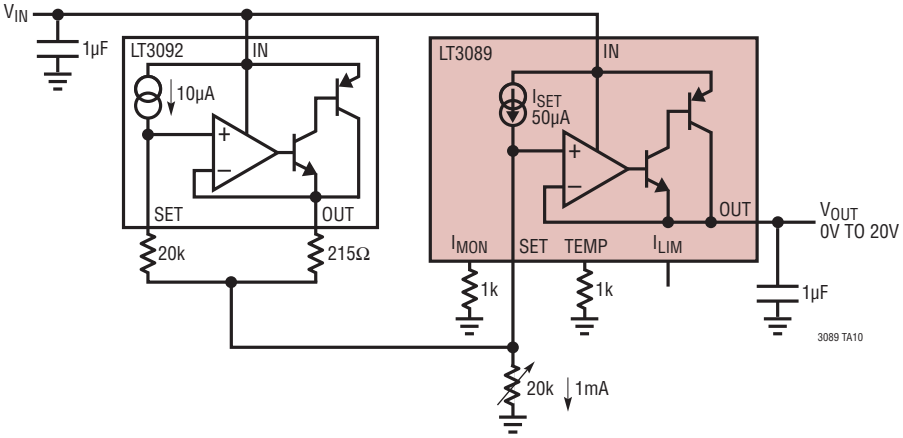


TYPICAL APPLICATIONS

Using a Lower Value Set Resistor



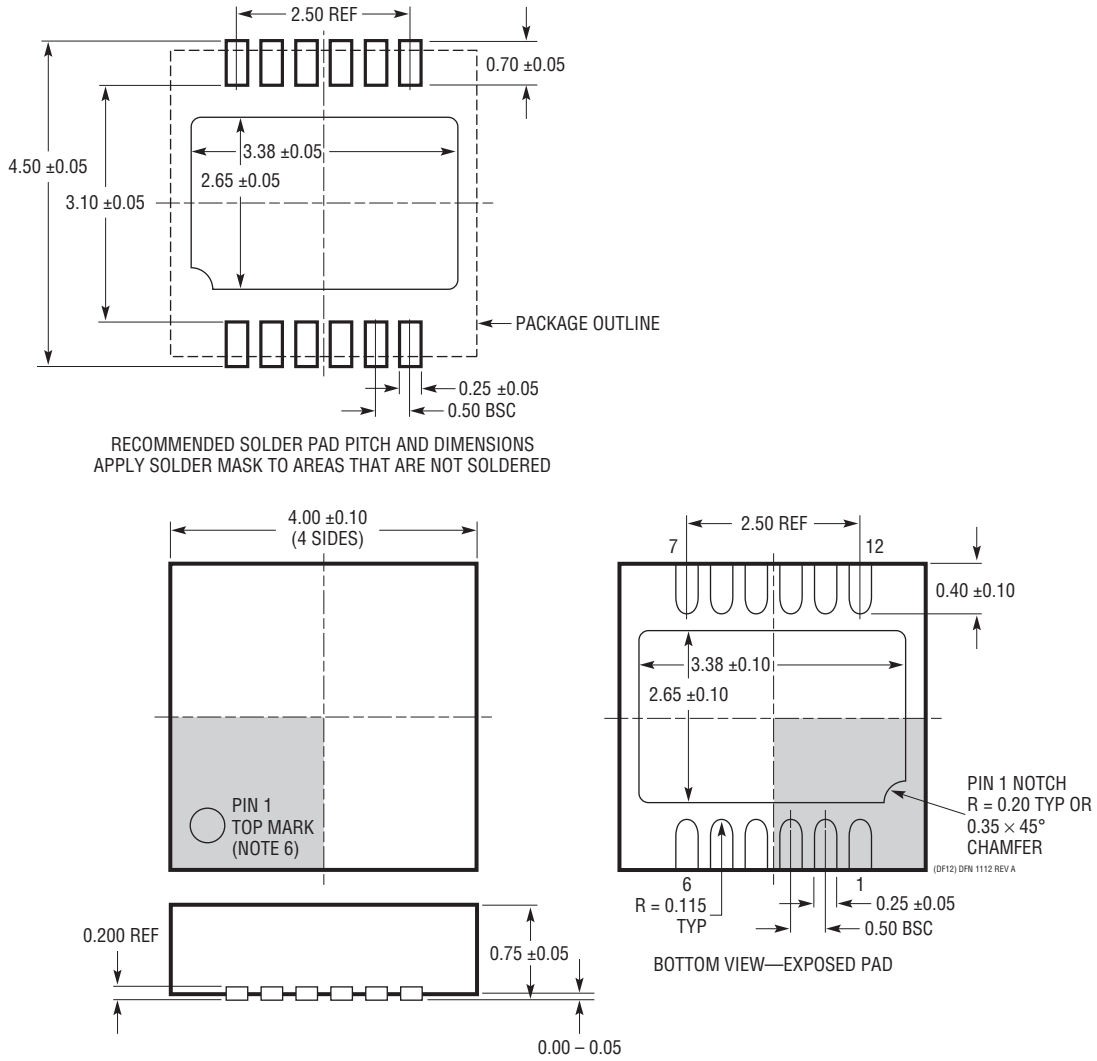
Using an External Reference Current



PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LT3089#packaging for the most recent package drawings.

DF Package
12-Lead Plastic DFN (4mm × 4mm)
(Reference LTC DWG # 05-08-1733 Rev A)

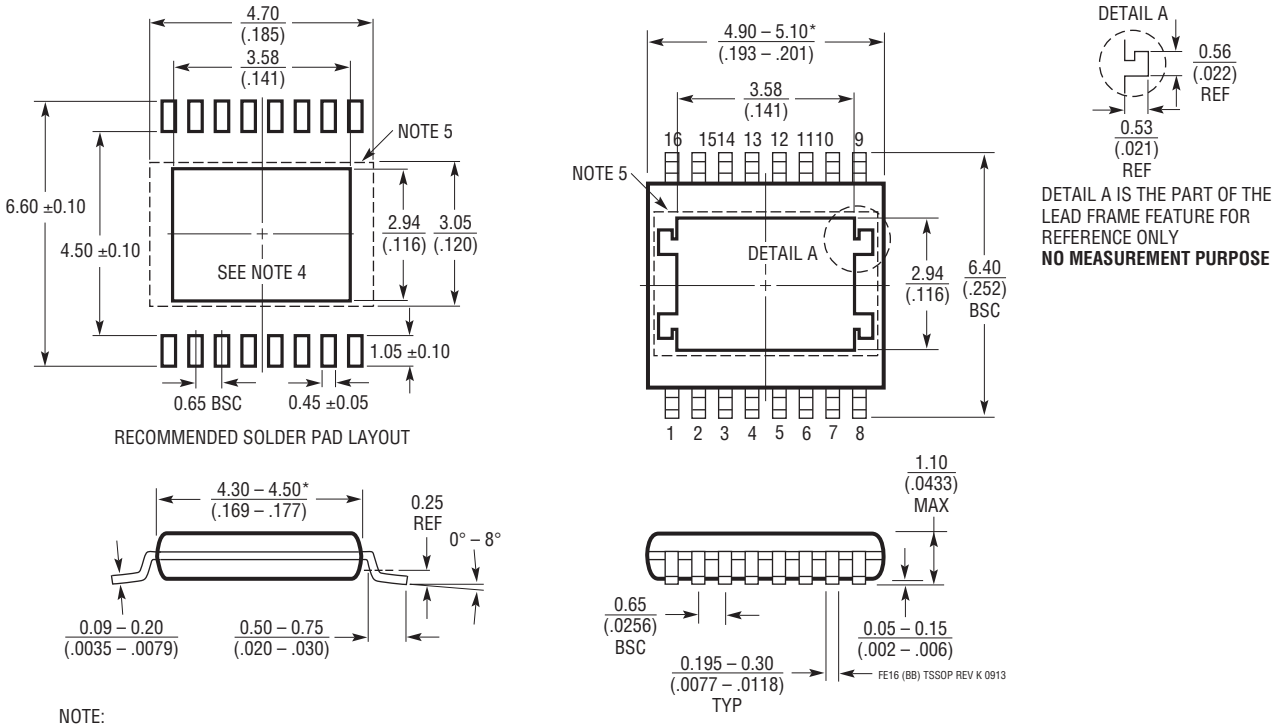


NOTE:
1. PACKAGE OUTLINE DOES NOT CONFORM TO JEDEC MO-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LT3089#packaging for the most recent package drawings.

FE Package
16-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1663 Rev K)
Exposed Pad Variation BB



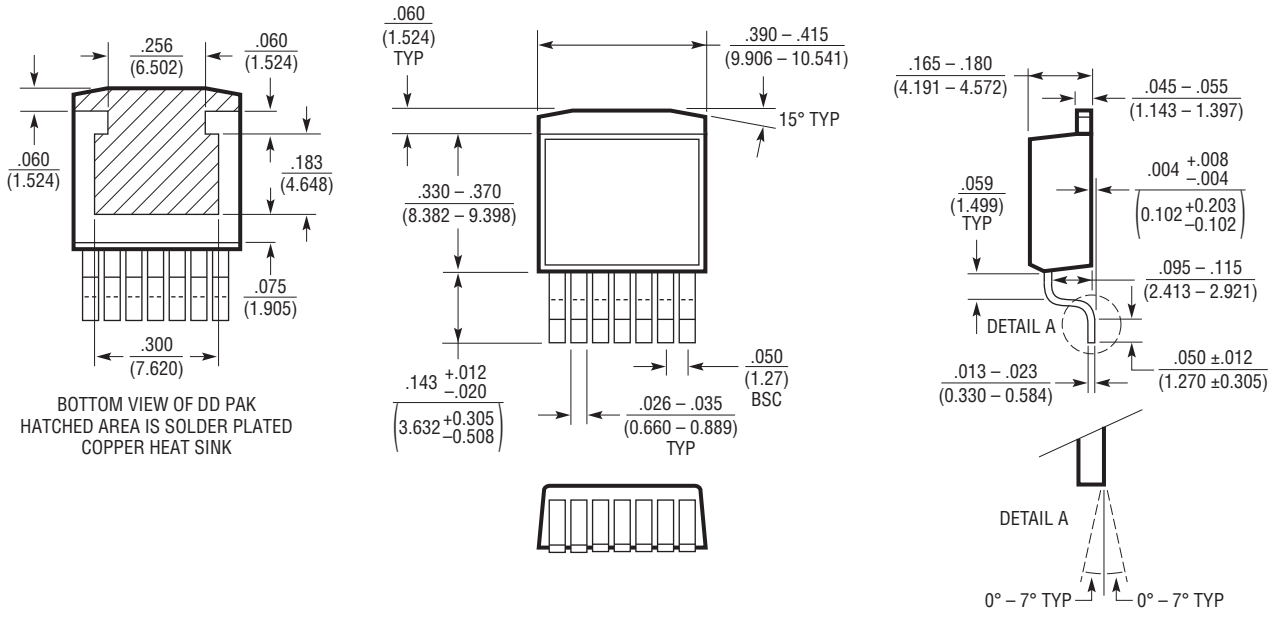
NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{\text{(INCHES)}}$
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT
5. BOTTOM EXPOSED PADDLE MAY HAVE METAL PROTRUSION IN THIS AREA. THIS REGION MUST BE FREE OF ANY EXPOSED TRACES OR VIAS ON PBC LAYOUT

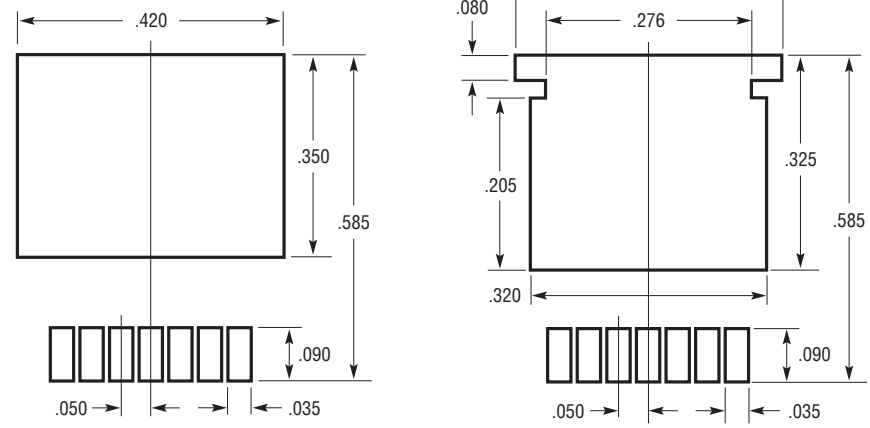
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LT3089#packaging for the most recent package drawings.

R Package
7-Lead Plastic DD Pak
(Reference LTC DWG # 05-08-1462 Rev F)





NOTE:
1. DIMENSIONS IN INCH/(MILLIMETER)
2. DRAWING NOT TO SCALE

R (DD7) 0212 REV F