Dual-Channel Low Noise Bias Generators

FEATURES

- **Generates Two Independent Low Noise Bias Supplies**
- **Boost Regulator:**
  - **Wide Input Voltage Range: 3V to 20V**
  - **Adjustable Switching Frequency: 450kHz to 2MHz**
  - **Synchronizable to External Clock**
  - **950mA Power Switches**
  - **Integrated Schottky Diodes**
  - **Internal Frequency Compensation**
- **Linear Regulator:**
  - **Wide Output Voltage Range: 1V to 20V**
  - **SET Pin Reference Current: 50µA**
  - **Low Noise: 4µV_{RMS} (10Hz to 100kHz)**
  - **High Frequency PSRR: 72dB at 1MHz**
- Independent Precision-Threshold Enable Pins
- Symmetric Pinout Simplifies PCB Layout
- Thermally Enhanced 3mm × 5mm 24-Lead QFN Package

APPLICATIONS

- Noise-Sensitive USB Powered Applications
- Data Conversion, Industrial Supplies, RF
- Instrumentation Amplifiers

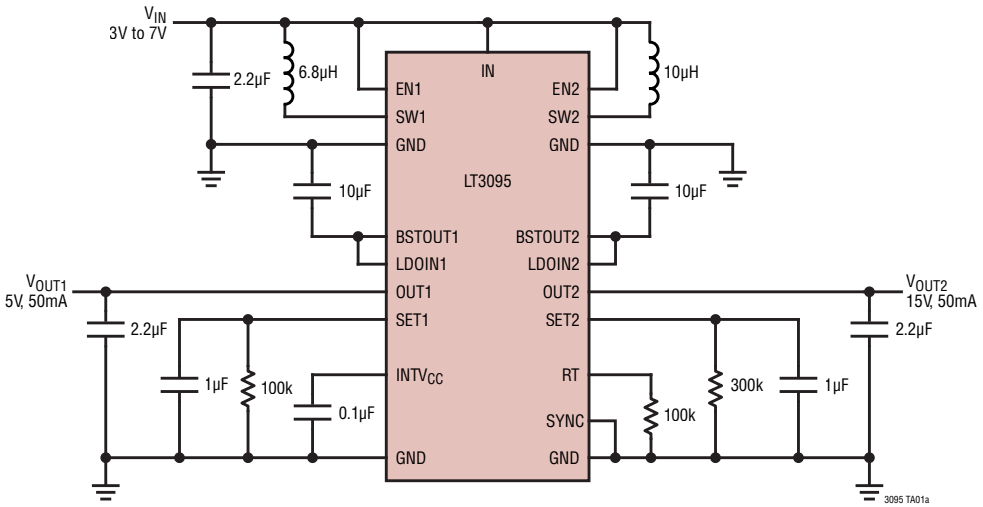
DESCRIPTION

The LT®3095 generates two low noise bias supplies from a common input voltage ranging from 3V to 20V. Each channel includes a fixed frequency, peak current-mode step-up switching regulator and a low noise, single-resistor-programmable 50mA linear regulator. The linear regulator's high power supply ripple rejection (PSRR) combined with its low noise performance results in less than 100µV_{P-P} output ripple and noise.

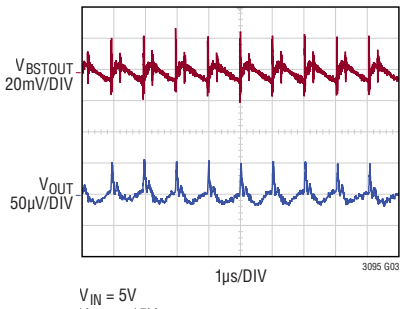
Each boost regulator adjusts its output voltage to 2V above the corresponding linear regulator's output voltage, optimizing power dissipation, PSRR and transient response. This tracking scheme, along with internal boost regulator frequency compensation and integrated Schottky diodes, minimizes external component count and simplifies system design. Each linear regulator includes internal current limit and thermal limit protection circuitry.

The LT3095 switching frequency is externally programmable with a single resistor from 450kHz to 2MHz. A SYNC pin allows synchronization to an external clock. The LT3095 is available in a thermally enhanced, low profile (0.75mm) 24-lead 3mm × 5mm QFN package.

TYPICAL APPLICATION



Output Ripple



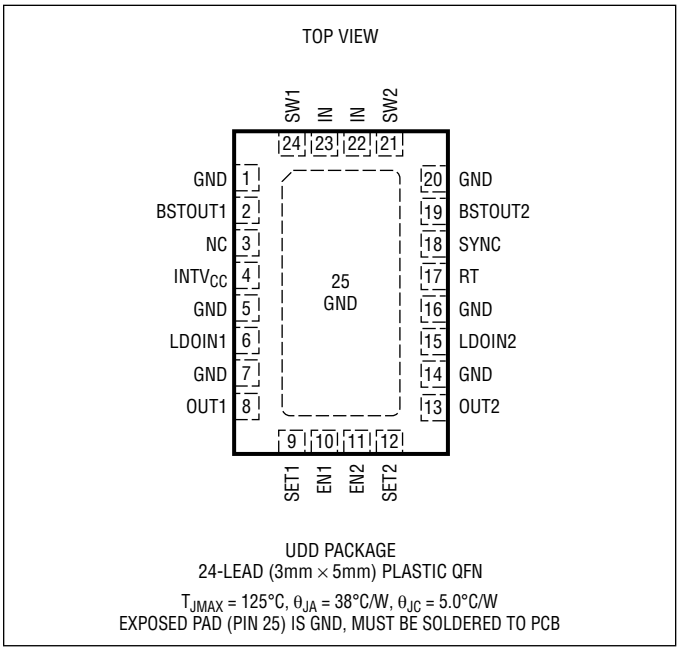
V_{IN} = 5V
V_{OUT} = 15V
I_{LOAD} = 50mA
f_{OSC} = 1MHz
20MHz BW

ABSOLUTE MAXIMUM RATINGS

(Note 1)

IN, SET1, SET2 .....24V
SW1, SW2,.....24V
OUT1, OUT2.....24V, –0.3V
EN1, EN2 .....24V, –0.3V
LDOIN1, LDOIN2, BSTOUT1, BSTOUT2.....24V
RT, SYNC 6V
Operating Junction Temperature (Note 2)
E-Grade, I-Grade.....–40°C to 125°C
MP-Grade .....–55°C to 125°C
Storage Temperature Range .....–65°C to 150°C

PIN CONFIGURATION



UDD PACKAGE
24-LEAD (3mm × 5mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JA} = 38°C/W, θ_{JC} = 5.0°C/W
EXPOSED PAD (PIN 25) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

(http://www.linear.com/product/LT3095#orderinfo)

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3095EUDD#PBF	LT3095EUDD#TRPBF	LGRQ	24-Lead (3mm x 5mm) Plastic QFN	–40°C to 125°C
LT3095IUDD#PBF	LT3095IUDD#TRPBF	LGRQ	24-Lead (3mm x 5mm) Plastic QFN	–40°C to 125°C
LT3095MPUDD#PBF	LT3095MPUDD#TRPBF	LGRQ	24-Lead (3mm x 5mm) Plastic QFN	–55°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, V_{IN} = 5V, SYNC = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Input Voltage Supply Range		●	3		20	V
I_{IN}	V_{IN} Pin Supply Current	V_{EN1} = V_{EN2} = 5.0V, V_{IN} = 5V (Not Switching)			3.25	5	mA
		V_{EN1} = V_{EN2} = 0.3V, V_{IN} = 20V (Shutdown)			1.6	5	µA
$V_{EN1,2}$	V_{TRIP} (off to on)	$V_{EN1,2}$ Rising	●	1.12	1.23	1.35	V
	Enable Threshold Hysteresis			110	125	135	mV
	Enable Pin Current	V_{EN} = 5V			1	5	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, V_{IN} = 5V, SYNC = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$INTV_{CC}$	$INTV_{CC}$ Voltage	$V_{EN1} = V_{EN2} = 5V$			2.7		V
	$INTV_{CC}$ Under Voltage Lockout	$V_{EN1} = V_{EN2} = 5V$, $INTV_{CC}$ Rising	●	2.25	2.4	2.55	V
	$INTV_{CC}$ Under Voltage Lockout Hysteresis	$V_{EN1} = V_{EN2} = 5V$			300		mV
Boost Regulator							
BOOST	($V_{LDOIN} – V_{OUT}$) Differential Regulation Voltage	$V_{EN1} = V_{EN2} = 5V$, $V_{OUT} = 10V$, $I_{LOAD} = 0mA$	●	1.85	2	2.15	V
	Boost Maximum Duty Cycle	f_{OSC} = 1MHz	●	90			%
	Switch Pin Leakage Current	Switch OFF, V_{SW} = 12V			0.01	1	µA
	Boost Switch Peak Current Limit	(Note 3)	●	0.8	0.95	1.1	A
	Switch V_{CESAT}	I_{SW} = 400mA			250		mV
OSC	Oscillator Frequency	RT = 210k, V_{IN} = 5V RT = 100k, V_{IN} = 5V RT = 44.5k, V_{IN} = 5V	● ● ●	0.47 0.95 1.85	0.5 1 2	0.53 1.05 2.15	MHz MHz MHz
	SYNC Duty Cycle Range	V_{SYNC} = 0V to 1.5V pulse		20		80	%
	SYNC Pin Input Current	V_{SYNC} = 5V			15	20	µA
	SYNC Threshold	f_{OSC} = 1MHz, 50% duty cycle	●	0.8	1.1	1.3	V
LDO Linear Regulator							
LDO	SET Pin Current	$V_{OUT} = 10V$, $I_{LOAD} = 0mA$		49.5	50	50.5	µA
		V_{OUT} = 1V to 20V, I_{LOAD} = 0mA to 50mA	●	49	50	51	µA
	Offset Voltage ($V_{OUT} – V_{SET}$)	$V_{OUT} = 10V$, $I_{LOAD} = 0mA$		–1	0.15	1	mV
	LDO Voltage Regulation: ΔI_{SET} LDO Voltage Regulation: ΔV_{OS} (Note 5)	V_{OUT} = 3V to 20V, $I_{LOAD} = 0mA$ V_{OUT} = 1V to 20V, $I_{LOAD} = 0mA$			–60 –50	–100	nA µV
	LDO Load Regulation: ΔI_{SET} LDO Load Regulation: ΔV_{OS} (Note 4)	$V_{OUT} = 10V$, I_{LOAD} = 0mA to 50mA $V_{OUT} = 10V$, I_{LOAD} = 0mA to 50mA			100 –6	150	nA mV
	LDOIN Supply Current	$I_{LOAD} = 0mA$			450		µA
	Ripple Rejection 3V < V_{OUT} < 20V, I_{LOAD} = 50mA	f_{RIPPLE} = 450kHz, C_{SET} = 0.1µF, C_{OUT} = 2.2µF, I_{LOAD} = 50mA f_{RIPPLE} = 1MHz, C_{SET} = 0.1µF, C_{OUT} = 2.2µF, I_{LOAD} = 50mA f_{RIPPLE} = 2MHz, C_{SET} = 0.1µF, C_{OUT} = 2.2µF, I_{LOAD} = 50mA			73 72 71		dB
	LDO Output Noise Voltage	$V_{OUT} = 5V$, I_{LOAD} = 50mA, C_{SET} = 0.47µF, C_{OUT} = 2.2µF, BW = 10Hz to 100KHz.			4		$µV_{RMS}$
	LDO Output Current Limit	V_{OUT} = 1V to 20V	●	55	70		mA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime. Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: The LT3095E is guaranteed to meet performance specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization, and correlation with statistical process controls. The LT3095I is guaranteed over the full –40°C to 125°C operating junction temperature range. The LT3095MP is 100% tested over the –55°C to 125°C operating junction temperature range.

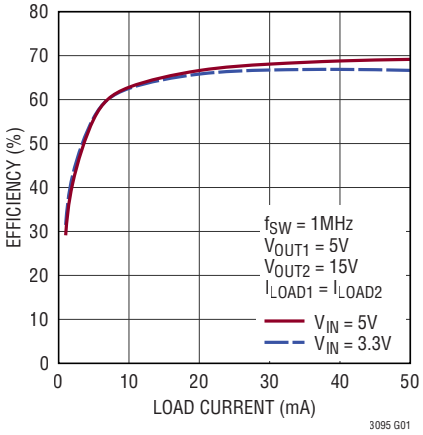
Note 3: The boost peak current limit is measured in a low frequency test mode. In operation at high frequencies, the inductor current may exceed this value due to delays in the control circuitry.

Note 4: Linear Technology® is unable to guarantee maximum load regulation due to production test limitations with Kelvin-sensing the package pins. Please consult the Typical Performance Characteristics for curves of output regulation as a function of load current.

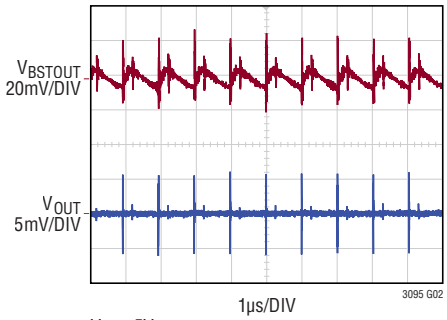
Note 5: For V_{OUT} < 1.25V, the LT3095 is tested with a 30µA external load. This load substitutes for an internal 30µA load which exists for V_{OUT} > 1.25V.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

Efficiency

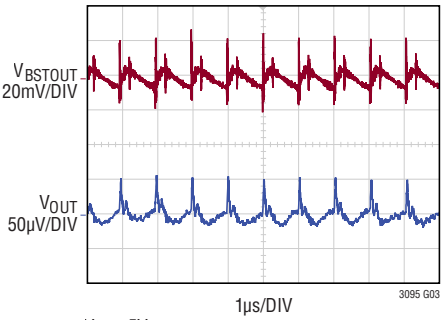


Transient Output Ripple



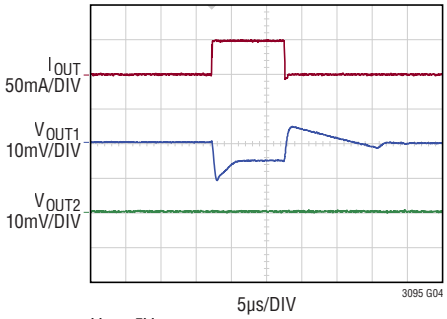
VIN = 5V
VOUT = 15V
ILOAD = 50mA
fOSC = 1MHz
350MHz BW

Transient Output Ripple



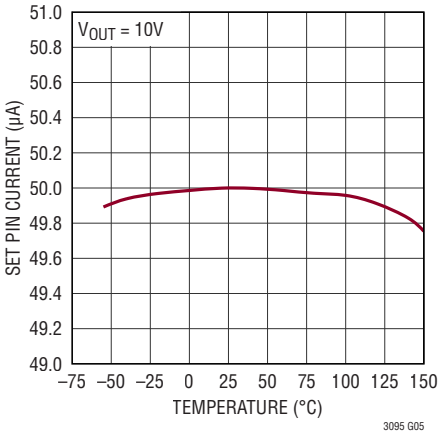
VIN = 5V
VOUT = 15V
ILOAD = 50mA
fOSC = 1MHz
20MHz BW

Linear Regulator Transient Response

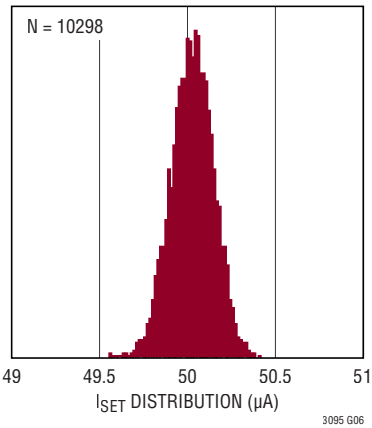


VIN = 5V
VOUT1 = 5V
VOUT2 = 15V
COUT = 2.2µF
CH1 LOAD STEP = 1mA to 50mA

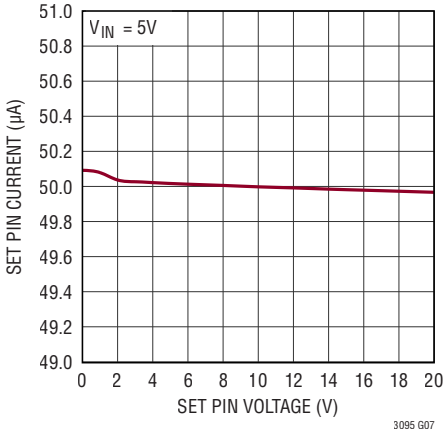
SET Pin Current



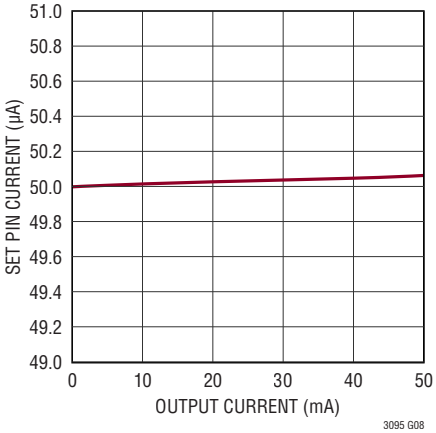
SET Pin Current Distribution



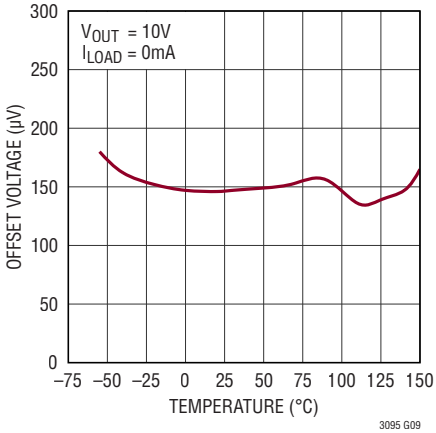
SET Pin Current



SET Pin Current

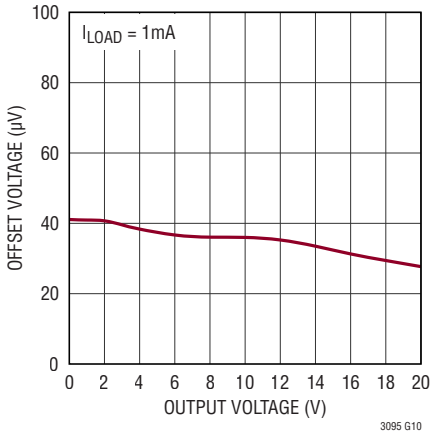


Offset Voltage (V_{OUT} – V_{SET})

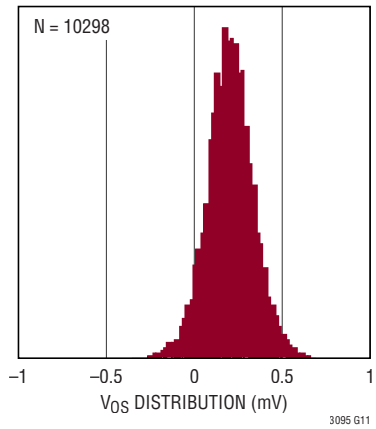


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

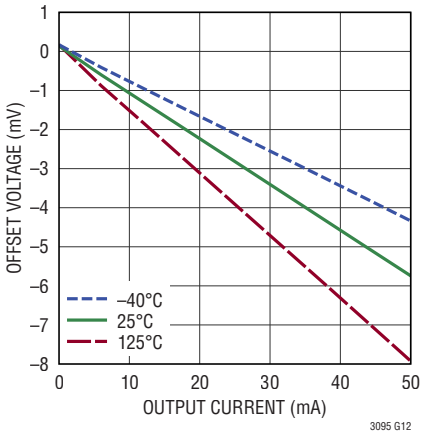
Offset Voltage (V_{OUT} – V_{SET})



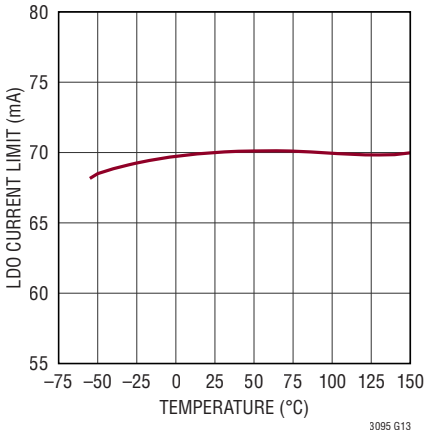
Offset Voltage Distribution



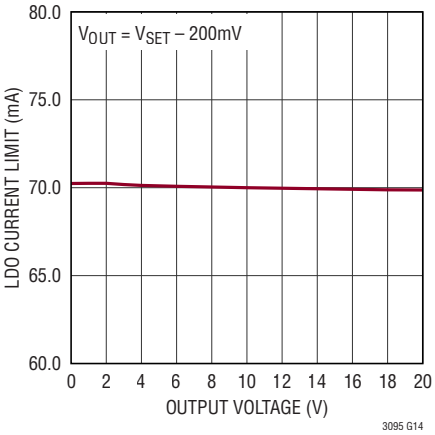
Offset Voltage (V_{OUT} – V_{SET})



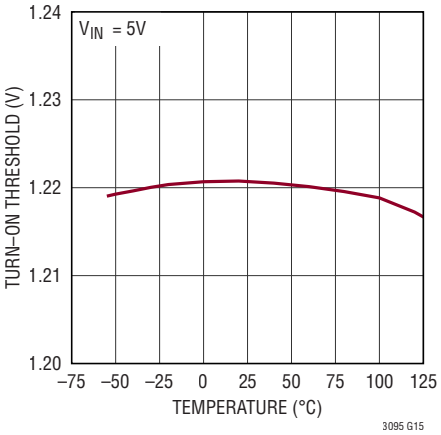
LDO Current Limit



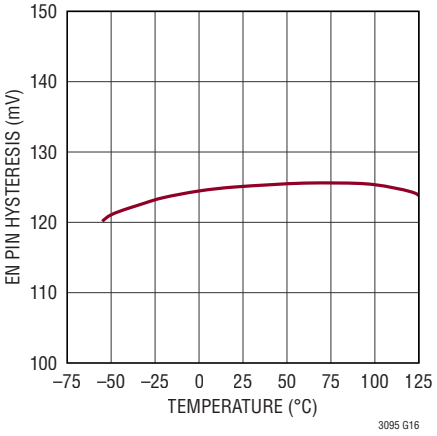
LDO Current Limit



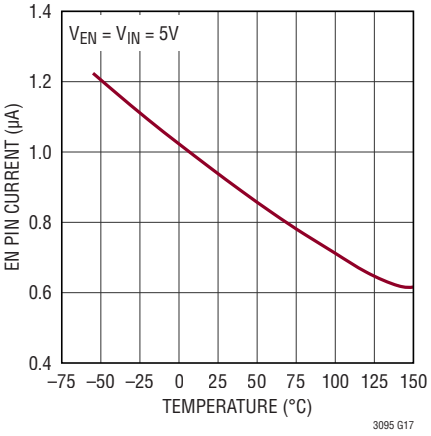
EN Turn-On Threshold



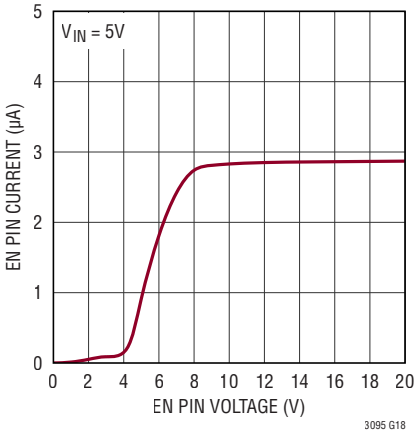
EN Pin Hysteresis



EN Pin Current

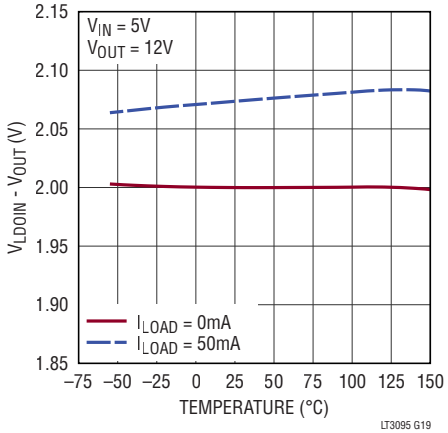


EN Pin Current

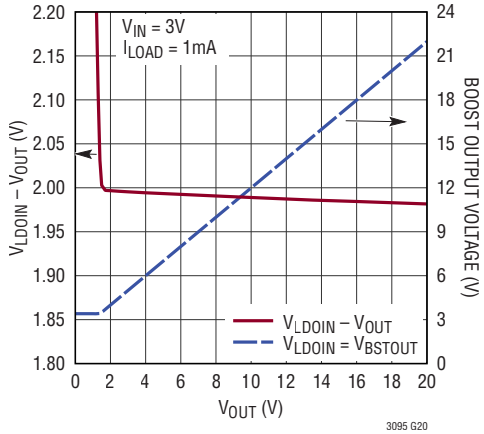


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

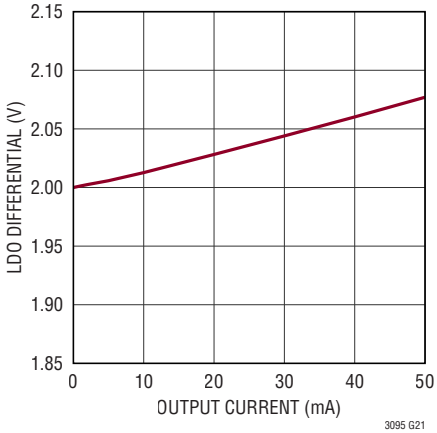
Differential Voltage ($V_{LDOIN} – V_{OUT}$)



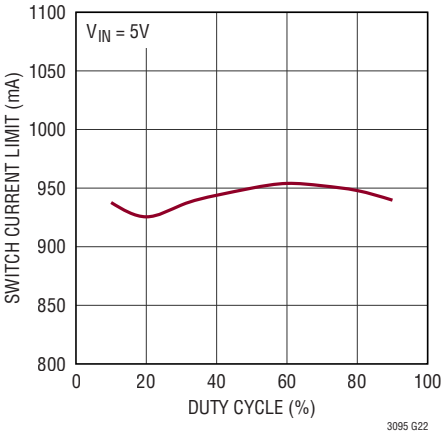
Boost Tracking



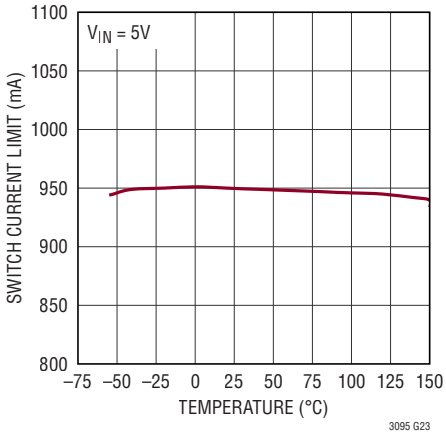
LDO Differential ($V_{LDOIN} – V_{OUT}$)



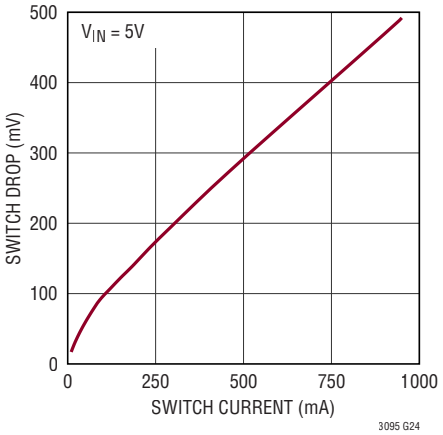
Boost Switch Peak Current Limit



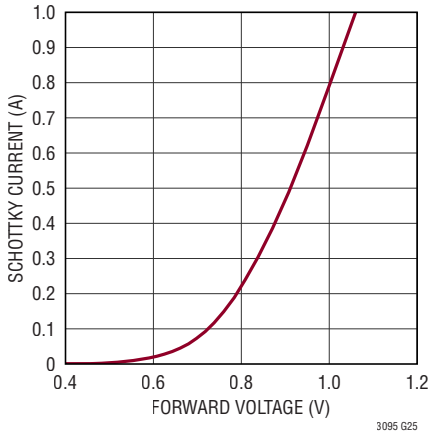
Boost Switch Peak Current Limit



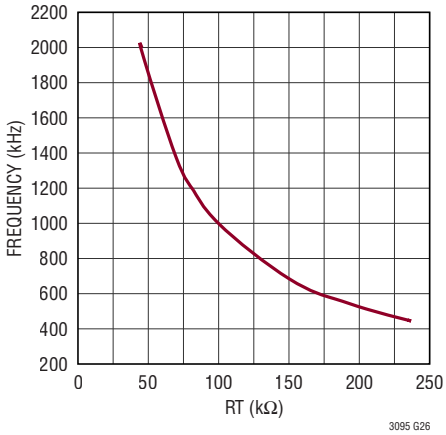
Switch Drop



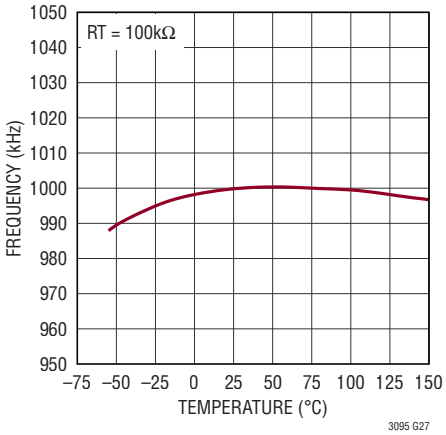
Power Schottky I-V Characteristic



Switching Frequency

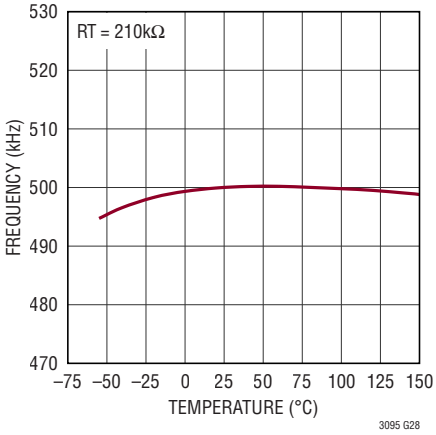


Switching Frequency

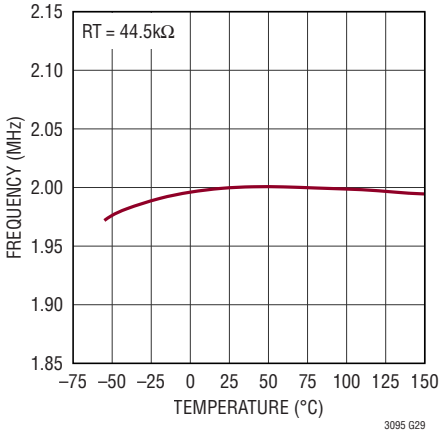


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

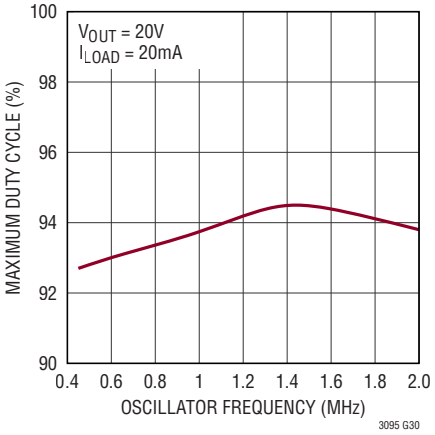
Switching Frequency



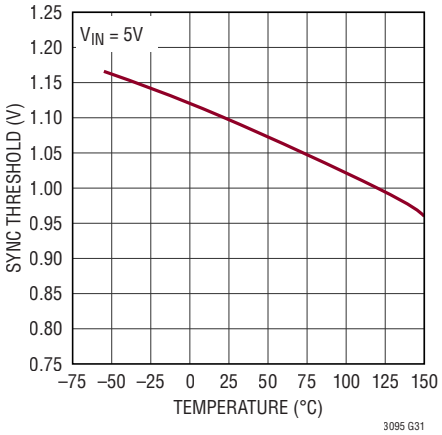
Switching Frequency



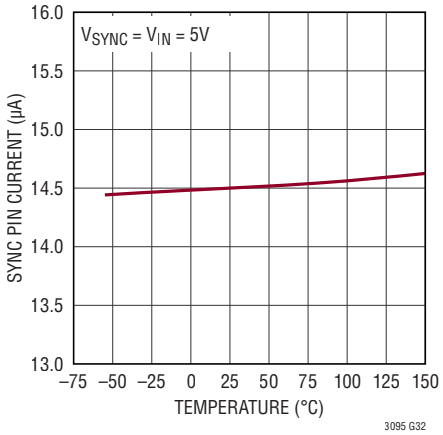
Maximum Duty Cycle



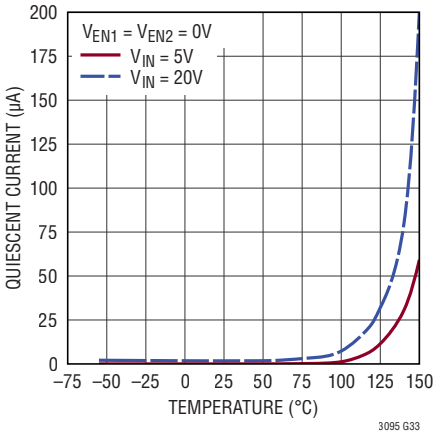
SYNC Threshold



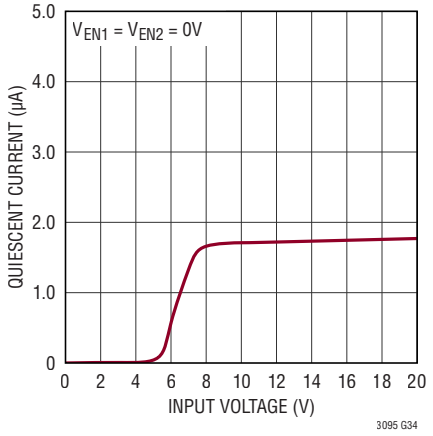
SYNC Pin Current



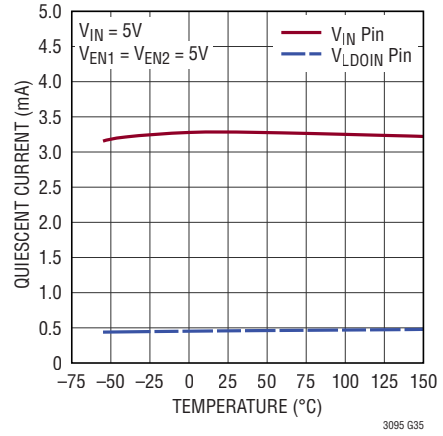
Quiescent Current in Shutdown (Both Channels, Boost + LDO)



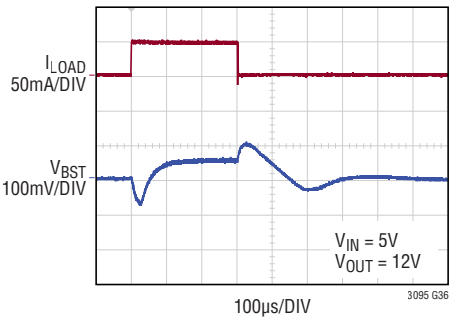
Quiescent Current in Shutdown (Both Channels, Boost + LDO)



Quiescent Current

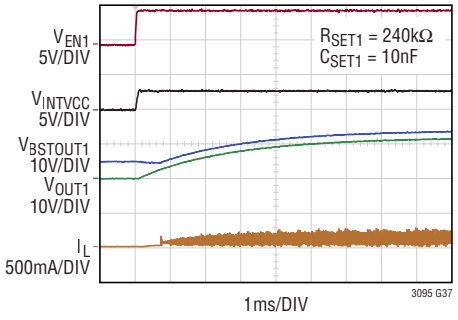


Boost Transient Response

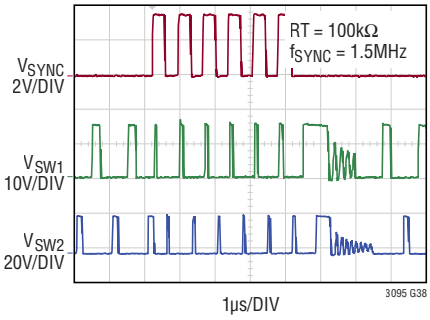


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

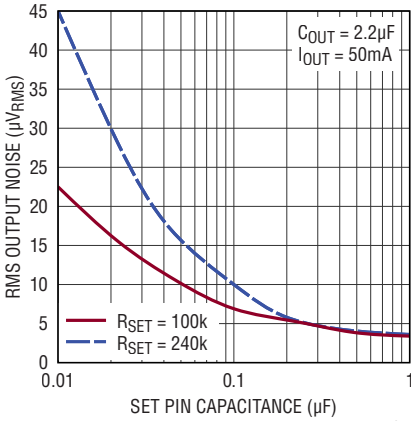
Start Up Response



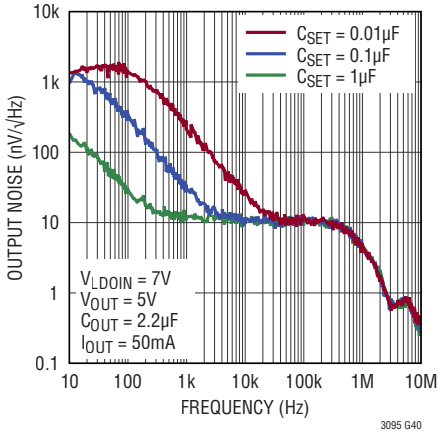
SYNC Acquisition



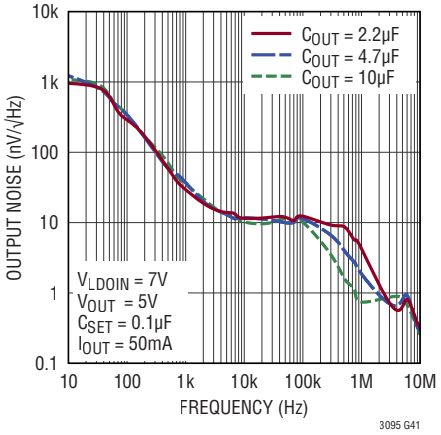
Integrated RMS Thermal Noise (10Hz – 100kHz)



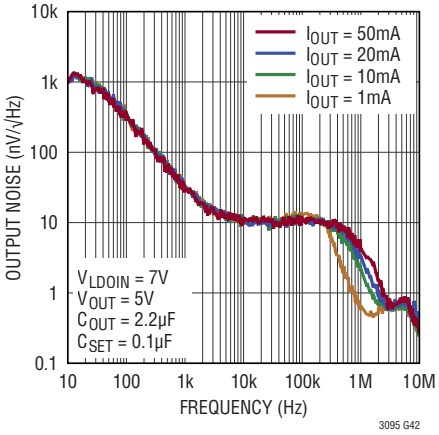
Noise Spectral Density



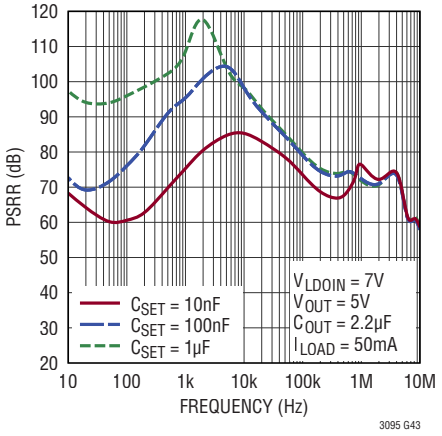
Noise Spectral Density



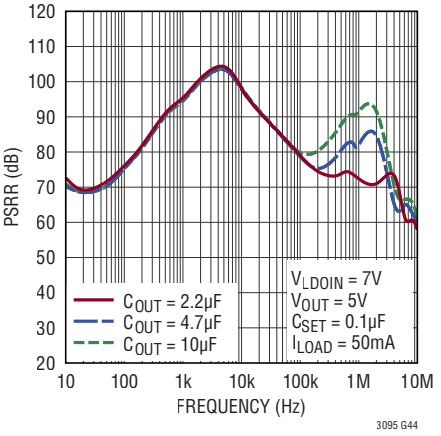
Noise Spectral Density



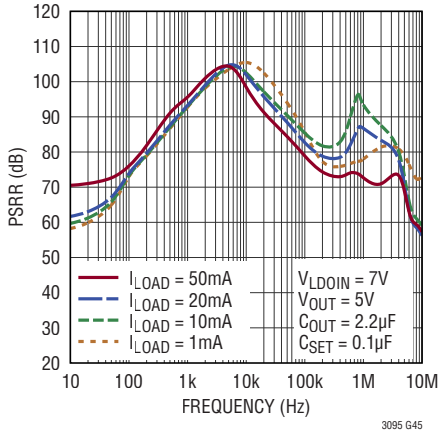
Linear Regulator Power Supply Rejection Ratio



Linear Regulator Power Supply Rejection Ratio



Linear Regulator Power Supply Rejection Ratio



PIN FUNCTIONS

GND (Pins 1, 5, 7, 14, 16, 20, Exposed Pad Pin 25): Ground. Tie the exposed pad Pin 25 directly to all other GND pins for optimum performance. The exposed pad provides enhanced thermal performance with its connection to the PCB ground.

BSTOUT1 (Pin 2): Channel 1 Step-Up Regulator Output. This pin is Channel 1's boost converter output. Connect BSTOUT1 directly to LDOIN1. Connect the boost output capacitor directly from BSTOUT1 to Pin 1's GND. An internal feedback loop regulates BSTOUT1's voltage typically to (OUT1 + 2V). This optimizes transient response and PSRR performance of the Linear Regulator.

NC (Pin 3): No Connect. Pin 3 has no internal electrical connection and may be floated or tied to GND.

$INTV_{CC}$ (Pin 4): Internal Regulator Output. $INTV_{CC}$ powers most of the internal circuitry for both channels. It nominally regulates to 2.7V. $INTV_{CC}$ is not designed to power any external load and should not be driven. Connect a minimum value 0.1µF or higher ceramic capacitor directly from $INTV_{CC}$ to Pin 5's GND.

LDOIN1 (Pin 6): Channel 1 Linear Regulator Input. This pin is Channel 1's linear regulator input supply pin. Connect Pin 6 directly to BSTOUT1 at Pin 2.

OUT1 (Pin 8): Channel 1 Linear Regulator Output. This pin supplies power to Channel 1's load. Use a minimum value 2.2µF ceramic capacitor with an ESR less than 0.1Ω to prevent oscillations. Large load transient applications require larger value output capacitors to limit peak voltage transients. See the applications information section for more information on output capacitance. Connect the output capacitor and the load directly to Pin 7's GND.

SET1 (Pin 9): Output Voltage Set. This pin is the noninverting input to Channel 1's LDO error amplifier and the regulation setpoint. A precision, trimmed 50µA flows out of SET1. Connecting a resistor from SET1 to GND programs Channel 1's output voltage (V_{OUT} = 50µA • R_{SET1}, Ohm's Law). Output voltage ranges from 1V to 20V. Connecting a capacitor from SET1 to Pin 7's GND improves transient response, PSRR, noise performance and soft starts the output. SET1 requires a minimum capacitor of 10nF. Larger value capacitors reduce output noise while correspondingly increasing startup time. For precision applications, an external reference or power supply may drive SET1 (see Applications Information section). This power supply must be current-limited to < 1mA or diode-clamped to exceed V_{LDOIN1} by no more than 1V.

EN1 (Pin 10): Channel 1's Enable. Pulling EN1 low disables Channel 1's boost converter and linear regulator, thus turning the output off. Its typical rising threshold is 1.23V with 125mV of hysteresis. Pulling both EN1 and EN2 low activates the micropower shutdown state in which internal circuit blocks shared by both channels are also disabled. EN1 can be used as a digital shutdown pin or, with the use of an external resistor divider, an external V_{IN} UVLO threshold can be programmed. If EN1 is unused, tie EN1 to V_{IN}. Do not float EN1.

EN2 (Pin 11): Channel 2's Enable. Pulling EN2 low turns off Channel 2's boost converter and linear regulator, thus turning the output off. Its typical rising threshold is 1.23V with 125mV of hysteresis. Pulling both EN1 and EN2 low activates the micropower shutdown state in which internal circuit blocks shared by both channels are also disabled. EN2 can be used as a shutdown pin or, with the use of an external resistor divider, an external V_{IN} UVLO threshold can be programmed. If EN2 is unused, tie EN2 to V_{IN}. Do not float EN2.

SET2 (Pin 12): Output Voltage Set. This pin is the noninverting input to Channel 2's LDO error amplifier and the regulation setpoint. A precision, trimmed 50µA flows out of SET2. Connecting a resistor from SET2 to GND programs Channel 2's output voltage (V_{OUT2} = 50µA • R_{SET2}, Ohm's Law). Output voltage ranges from 1V to 20V. Connecting a capacitor from SET2 to Pin 14's GND improves transient response, PSRR, noise performance and soft starts the output. SET2 requires a minimum capacitor of 10nF. Larger value capacitors reduce output noise while correspondingly increasing startup time. For precision applications, an external reference or power supply may drive SET2 (see Applications Information section). This power supply must be current-limited to < 1mA or diode-clamped to exceed V_{LDOIN2} by no more than 1V.

PIN FUNCTIONS

OUT2 (Pin 13): Channel 2 Linear Regulator Output. This pin supplies power to Channel 2's load. Use a minimum value 2.2µF ceramic capacitor with an ESR less than 0.1Ω to prevent oscillations. Large load transient applications require larger value output capacitors to limit peak voltage transients. See the applications information section for more information on output capacitance. Return the output capacitor and the load directly to Pin 14's GND.

LDOIN2 (Pin 15): Channel 2 Linear Regulator Input. This pin is Channel 2's linear regulator input supply pin. Connect Pin 15 directly to BSTOUT2 at Pin 19.

RT (Pin 17): Oscillator Frequency Target. A single resistor from RT to ground programs the internal oscillator from 450kHz to 2MHz. If synchronizing to an external clock, connect a resistor to program the oscillator to a frequency close to the SYNC clock frequency. Do not load the RT pin with a capacitor.

SYNC (Pin 18): External Clock Synchronization Input. Ground this pin to use the internal oscillator. Tie to a logic-level clock source for external synchronization. Do not leave floating.

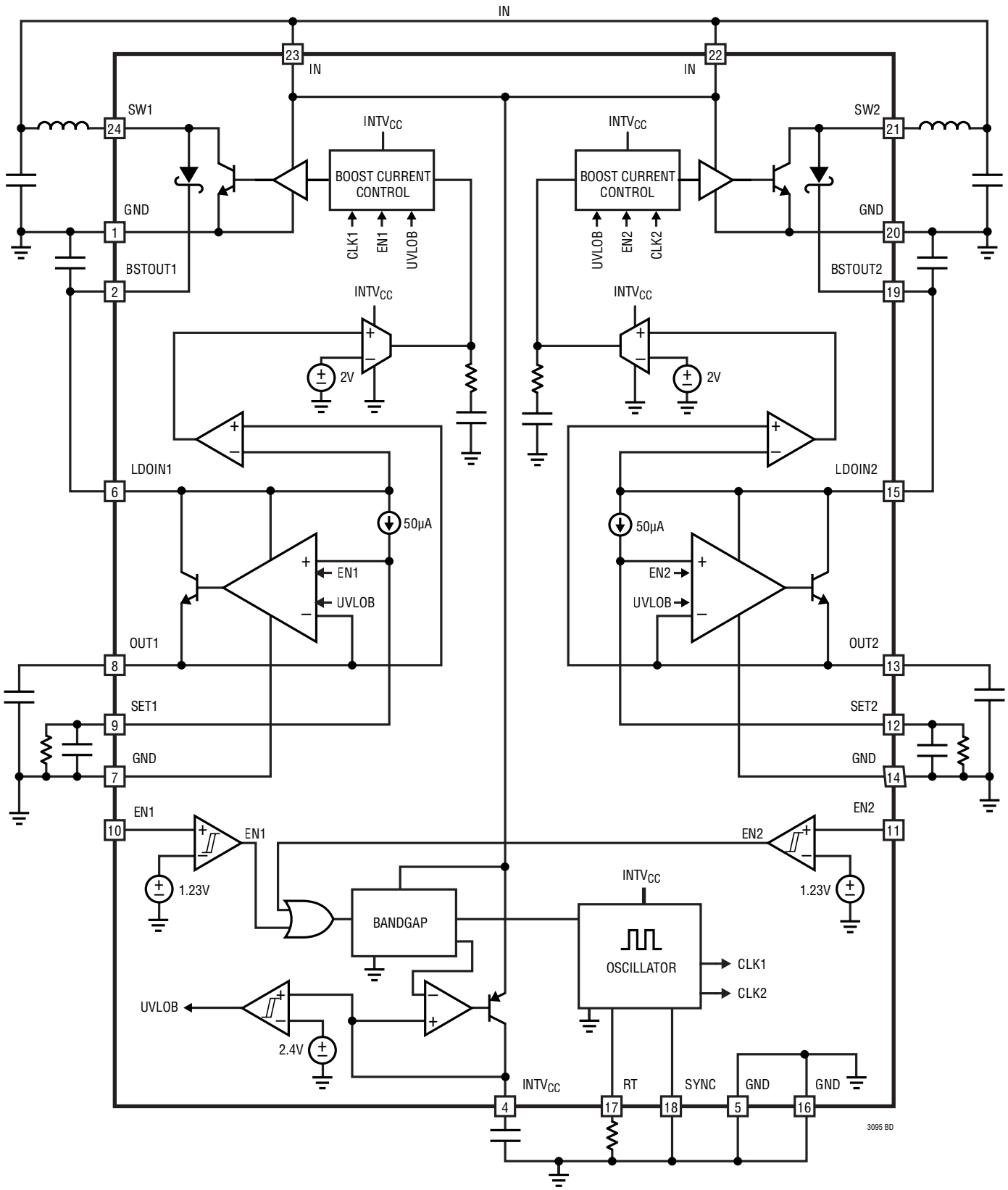
BSTOUT2 (Pin 19): Channel 2 Step-Up Regulator Output. This pin is Channel 2's boost converter output. Connect BSTOUT2 directly to LDOIN2. Connect the boost output capacitor directly from BSTOUT2 to Pin 20's GND. An internal feedback loop regulates BSTOUT2's voltage typically to (OUT2 + 2V). This optimizes transient response and PSRR performance of the Linear Regulator.

SW2 (21): Channel 2 Step-Up Regulator Switch Node. The SW pin is connected internally to the collector of the power switch and Schottky anode of the corresponding boost regulator. This is the path for boost input power of Channel 2.

IN (Pins 23, 22): Input Bias Supply. The IN pins supply current to the $INTV_{CC}$ regulator and switch drivers. These pins must be locally bypassed with a minimum of 2.2µF of low-ESR capacitance. Place the positive terminal of the capacitor as close as possible to IN pins and return near to Pin 1 & PIN 20's GND. Note that Pins 22 and 23 are internally connected.

SW1 (24): Channel 1 Step-Up Regulator Switch Node. The SW pin is connected internally to the collector of the power switch and Schottky anode of the corresponding boost regulator. This is the path for boost input power of Channel 1.

BLOCK DIAGRAM



APPLICATIONS INFORMATION

The LT3095 is an easy-to-use step-up bias generator with two independent channels supporting loads up to 50mA. Since the boost converters are monolithic and feature internal compensation, the LT3095 is easy to configure with a few external components. The output of each switcher is post-regulated by a linear regulator to filter output ripple and provide a precision DC voltage with very low noise for biasing sensitive circuits and sensors. The output of each channel is programmed with a single resistor and internal feedback automatically regulates the output of each boost converter to 2V above the corresponding linear regulator's output. The filtered outputs are protected by independent current limit and thermal shutdown.

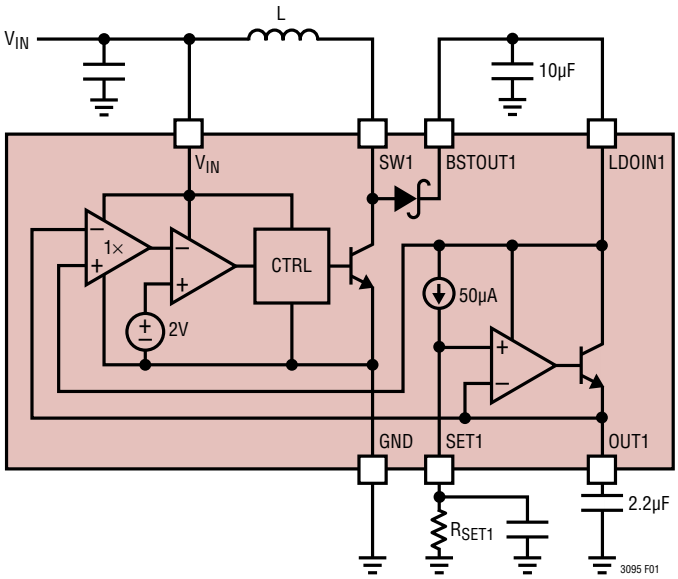


Figure 1. LT3095 Architecture (Single Channel)

Programming the Output Voltage

Figure 1 illustrates the architecture of the LT3095. The boost converter simply regulates the difference between LDOIN and OUT – no external feedback configuration is necessary. The linear regulators have a single-resistor-programmable reference architecture. An accurate, temperature-compensated 50µA current flows out of the SET pin and into an external resistor, R_{SET}, to establish the reference for the linear regulator output voltage. To program the output, simply choose the appropriate SET pin resistor according to Ohm's law:

$$R_{SET} = \frac{V_{OUT}}{50\mu A}$$

The SET pin voltage is buffered to the output, so the linear regulator always operates in unity gain configuration. This allows optimal loop gain and bandwidth regardless of output voltage. With this architecture, it is also possible to drive the set pin externally for a dynamic supply (see the Typical Applications section below).

The LT3095 step-up regulator tracks the output of the linear regulator and maintains 2V typically between LDOIN and OUT of each channel. This input-to-output voltage control obviates the need to externally program the boost output voltage and insures controlled power dissipation in the linear regulator pass device, even if the target output voltage is adjusted or programmed dynamically during operation.

Boost Output Capacitor/Linear Regulator Input Capacitor

The LT3095 step-up converters are internally compensated and require an output capacitor, which also serves as the input capacitor for the linear regulator. A value of 10µF is recommended. Consider capacitance degradation under bias and temperature conditions, as outlined below. The connection of the boost output capacitor on the PCB is crucial for ripple performance, as discussed in the Pin Functions section.

Linear Regulator Stability & Output Capacitor

The LT3095 linear regulators are stable with a minimum output capacitance of 2.2µF (ESR < 0.1Ω). Use low-ESR multilayer ceramic capacitors and give consideration to the actual capacitance under bias and temperature conditions. See the Effective Operating Capacitance section for more information.

The linear regulator feedback loop has very high bandwidth, allowing it to respond quickly to load steps and actively correct input ripple feed-through up to frequencies near the self-resonance of a typical multilayer ceramic capaci-

APPLICATIONS INFORMATION

tor. As an example, the loop bandwidth driving a 50mA load with C_{OUT} = 2.2µF is about 1MHz. With such a high bandwidth, the parasitic series resistance and inductance of the output capacitor can have a noticeable impact on the loop dynamics near the unity gain frequency. If the phase response of the loop is degraded, transient output ringing can result and supply ripple rejection may suffer. Avoid these problems by using ceramic capacitors with ESR less than 100mΩ; place the capacitor as close as possible to the OUT pin and return directly to the adjacent GND pin. See the discussion of board layout below for an example PCB design that meets these requirements.

If capacitor types with higher ESR (>100 mΩ) or lower self-resonant frequencies (< 500 kHz) must be used, it may be necessary to parallel several output capacitors. This lowers the effective ESR and ESL and can have beneficial effects on ripple rejection.

Using an output capacitor with a value greater than the minimum 2.2µF can improve ripple rejection under certain conditions, as shown in the Typical Performance plots. However, due to limitations in parasitic electromagnetic coupling, the advantages may not be dramatic in practice. A value of 2.2µF is recommended for most applications.

SET Pin (Reference Bypass) Capacitance

Within the bandwidth of the linear regulator, wideband thermal noise and injected ripple at the output of the LT3095's built-in reference (that is, the SET pin) are replicated at the output. Minimize this source of noise by using an external capacitor to bypass the SET pin. Table 1 shows the total RMS output noise in a 10Hz to 100kHz bandwidth and a 1kHz to 20MHz bandwidth for several different values of C_{SET} in a typical application. The lower-bandwidth measurement reflects thermal and shot noise only, while the higher-bandwidth measurement includes residual ripple components from the switching converter. Both are influenced by the value of C_{SET}. A minimum of 10nF is required, but noise is reduced substantially with $C_{SET} \geq$ 100nF.

Table 1. Output Noise for Different Values of C_{SET}

CSET	V_{OUT-AC} (μV_{RMS} 10Hz to 100kHz)	V_{OUT-AC} (μV_{RMS} 1kHz to 20MHz)
10nF	35	40
47nF	15	25
100nF	12	25
470nF	7	25
1µF	4	25

Single channel operation, V_{IN} = 5V, V_{OUT} = 18V, I_{LOAD} = 50mA, C_{OUT} = 2.2µF, C_{BSTOUT} = 10µF

A system level consideration that may limit the value of C_{SET} is start-up time: when the part is enabled from shutdown, the SET pin voltage rises with a time constant of $R_{SET} \bullet C_{SET}$. Since OUT tracks SET, this causes the linear regulator output to soft-start. If very fast startup is required and noise performance cannot be compromised, use an auxiliary circuit to speed up the start time or drive the SET pin externally (see Typical Applications).

Effective Operating Capacitance

The effective capacitance of a multilayer ceramic capacitor varies over temperature and DC bias conditions, and may be considerably lower than the manufacturer's nominal value. To ensure stable operation of the LT3095, make sure that the boost and linear regulator output capacitors meet the minimum requirement in their actual operating conditions, after accounting for temperature and DC bias.

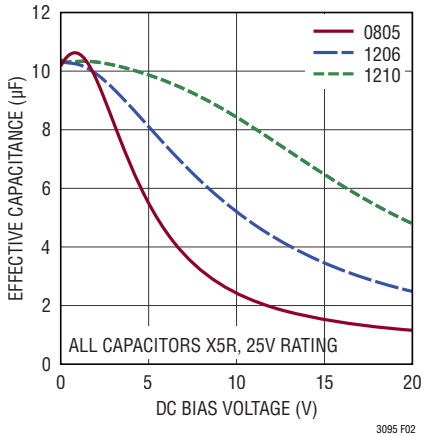


Figure 2. Capacitance Degradation with DC Bias Voltage

APPLICATIONS INFORMATION

Capacitance degradation under DC bias can be dramatic. In some cases, the effective value of a capacitor may be less than 20% of the nominal value, even at voltages well below the nominal voltage rating of the component. Different dielectric materials have different sensitivities to DC bias, with X5R and X7R offering good performance. Package size also has a large influence on the effective capacitance achieved at higher voltages. In general, capacitors in physically larger packages suffer less degradation under DC bias than capacitors of the same voltage rating in a smaller size. Figure 2 shows typical bias curves for three X5R capacitors with nominal values of 10µF, all rated for 25V, but in different package sizes.

The effective values of some ceramic capacitors can also degrade significantly with temperature, as Figure 3 demonstrates. Of the common dielectric types, X5R and X7R offer relatively stable capacitance over a wide temperature range. Both are widely available in a variety of sizes and values.

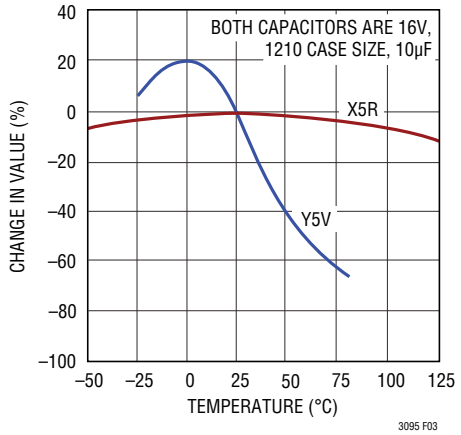


Figure 3. Capacitance De-Rating with Temperature

In the case of the linear regulator output capacitor, the regulator can show ringing or degraded ripple rejection if the effective capacitance is more than 20% below the recommended minimum of 2.2µF. The recommended minimum value for C_{BSTOUT} — the output capacitor for the boost converter — is 10µF; however, lower effective values may be tolerable in certain applications. At high duty cycles, for example, the linearized transconductance of the current control loop is reduced, and less output capacitance is required to achieve the same unity gain frequency. When using a boost output capacitor with effective capacitance below 8µF, verify the loop dynamics experimentally or with an AC model to ensure adequate loop stability in realistic operating conditions.

Programming the Switching Frequency

The LT3095's two switching regulator channels run out of phase to reduce input current ripple amplitude. An internal oscillator generates a precise clock that can be programmed from 450kHz to 2MHz by connecting an external resistor from the RT pin to ground. Table 2 lists the closest 1% resistor values for a few common frequencies. Refer to the Typical Performance section for a plot of clock frequency as a function of RT.

Table 2. SW Frequency vs RT Value

f_{OSC} (MHz)	RT (kΩ)
0.45	232
0.50	210
0.75	137
1.00	100
1.50	63.4
2.00	44.2

Alternatively, an external frequency source can be used to synchronize the switching edges to a system clock using the SYNC pin. The voltage and duty-cycle requirements for the logic level SYNC signal are listed in the Electrical Characteristics table. When using the SYNC pin to set the frequency, connect a resistor to the RT pin as if programming the oscillator to the SYNC frequency. Use a resistor with 1% tolerance to insure appropriate scaling of internal control signals. The LT3095 will sense a pulsed signal on the SYNC pin and override the oscillator to align the switch edges with the external clock.

When using the internal oscillator, each channel will run at the programmed switching frequency, f_{OSC}, and the power switches will turn on 180° out-of-phase. If SYNC functionality is used, each channel will run at the SYNC pulse frequency: one power switch will turn on at the rising edge of the SYNC input, and the other power switch at the falling edge.

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Inductor Selection & Boost Loop Stability

The choice of inductor for the boost converter affects the system efficiency, loop stability, and solution size. As a starting point, choose a value which results in ≤30% current ripple when the switcher is operating at its peak current of about 1A. The minimum inductor value that satisfies this requirement can be calculated from the input and output voltages and the switching frequency:

$$L_{MIN} = \frac{(V_{IN} - 0.5)(V_{OUT} + 3 - V_{IN})}{0.3(V_{OUT} + 3)f_{SW}}$$

…where V_{OUT} is the programmed voltage at the output of the linear regulator, and V_{IN} is the supply of the inductor current.

In some cases, it may be appealing to use a smaller inductor value because of solution size or other constrains. Before reducing the inductance, there are some considerations that must be taken into account. A smaller inductor will result in increased output ripple and additional conduction losses in the inductor and power switch. Higher peak currents will translate to increased EMI radiation during switching, which can easily couple frequency content onto the output of the linear regulators.

Furthermore, a small inductor may make the current-control loop unstable in continuous conduction mode, causing subharmonic oscillations in the inductor current. This can introduce unpredictable spectral content into the system. Subharmonic oscillation is only a concern for duty cycles greater than 50%, and can be avoided by making sure the inductor meets the following requirement:

$$L > \frac{V_{OUT} - V_{IN} + 3}{1.25V} \bullet 1\mu H \text{ for } D < 0.75$$

$$L > \frac{V_{OUT} - V_{IN} + 3}{2.50V} \bullet 1\mu H \text{ for } D > 0.75$$

where

$$D = 1 - \frac{V_{IN} - 0.5}{V_{OUT} + 3}$$

Finally, with a low inductance, the converter may operate at or near discontinuous conduction mode, even at large loads. While stability is guaranteed in discontinuous conduction mode, switch node ringing may introduce new frequency components into the system. In extreme cases (e.g. high boost ratio and heavy load), the step-up converter may not be able to deliver 50mA average output current, even when the inductor is energized to the switch peak current limit each clock cycle.

Use an inductor with a sufficient current rating to prevent core saturation, which can cause the effective inductance to drop dramatically and the current to jump very quickly. In case of runaway, an internal protection circuit senses very high currents in the internal catch diode and prevents the power switch from turning on until the inductor current falls. This safety mechanism protects the power switch, but damage to the power Schottky diode or overvoltage of the boost converter's output are still possible. For these reasons, avoid inductor core saturation during normal operation: choose an inductor rated for the peak current in your application, with appropriate margin for tolerances and transient overshoot. If in doubt, a rating of 1.5A will provide insurance against saturation in all normal operating conditions.

Regarding switching supply loop stability, it is well known that the control loop of a boost converter has an inherent right half-plane zero. Fundamentally, this is due to the fact that current is not delivered to the load while the inductor is being energized. Thus, when the loop commands more current, the output voltage temporarily drops. A linearized approximation of the zero frequency is:

$$f_{zero,RHP} = \frac{V_{BST}(1-D)^2}{2\pi L I_{LOAD}}$$

…where V_{BST} is the output of the boost converter (approximately V_{OUT} + 3V), D is the switch duty cycle, and L is the inductor value. When this zero falls near the loop unity gain frequency (typically around 50kHz), phase margin is degraded. For this reason, avoid inductor values much larger than suggested by the 30% ripple calculation given above.

APPLICATIONS INFORMATION

High Frequency Edges & Passive Filtering Techniques

Figure 4 shows the output of the LT3095 boost converter in a typical application with a 50mA load, before and after filtering by the linear regulator. The most noticeable residual switching feature is the short spike when the boost power switch turns off. This edge is generated by high dI/dt circulating through the boost output capacitor parasitic and the corresponding magnetic circuit on the PCB.

These edges can couple onto the output of the linear regulator indirectly through parasitic capacitance in the linear regulator or electromagnetically from one PCB trace to another. The spikes contain high frequency (>1MHz) content that the linear regulator control loop cannot actively filter out. Minimize the residual spike amplitude by following the PCB layout guidelines provided in the next section. In many applications, the energy associated with the residual spikes is at a sufficiently high frequency that it does not interfere with the load.

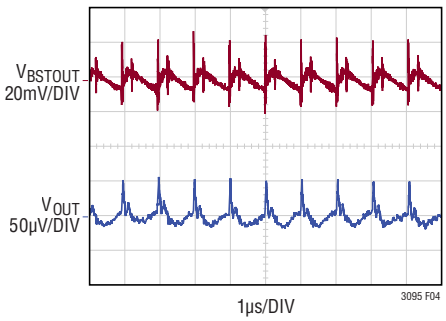


Figure 4. Output Transient Showing Spikes

In cases where extreme ripple rejection up to very high frequencies is required, a passive filter at the output of the LDO can be used. Form a pi-network by placing the output capacitor very close to the LT3095 and another capacitor directly at the load, as shown Figure 5. Make sure the additional capacitor is large enough to present low impedance to the load across the full frequency range. PCB trace inductance between the LT3095 and load will provide some high-frequency filtering, but passives with additional impedance can offer further improvement. One option is a small resistor — typically an Ohm or less to avoid introducing a large load regulation term to the voltage seen at the load. Another option is a low-ESR chip ferrite-bead or inductor. This solution offers the best rejection at very high frequencies (>10 MHz); however, a resonance is formed at a frequency of $1/\left(2\pi\sqrt{L_{FILTER}C_{LOAD}}\right)$ that can amplify noise and introduce a new ripple component at the load. The peaking, or Q, associated with the filter can be reduced by introducing a series damping resistor or reducing the ratio L_{FILTER}/C_{LOAD}.

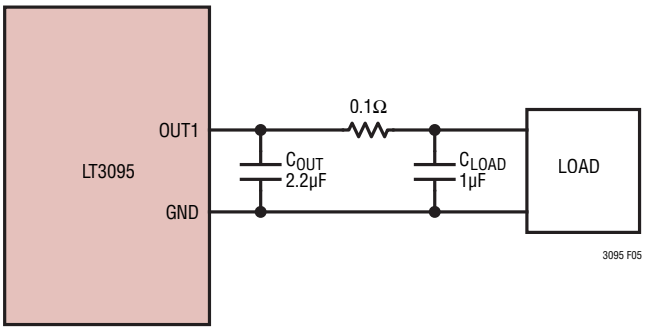


Figure 5. Pi Network Filter

Figure 6 shows the residual noise at the output of the LDO after it has been filtered with a 0.1Ω resistor and an additional 1µF capacitor at the load. The high frequency switch edges have been substantially reduced.

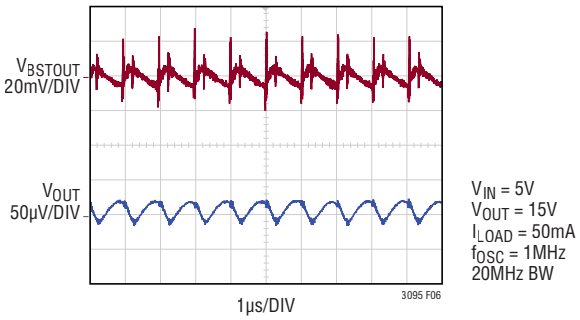


Figure 6. Residual Ripple with Passive Pi Filter

APPLICATIONS INFORMATION

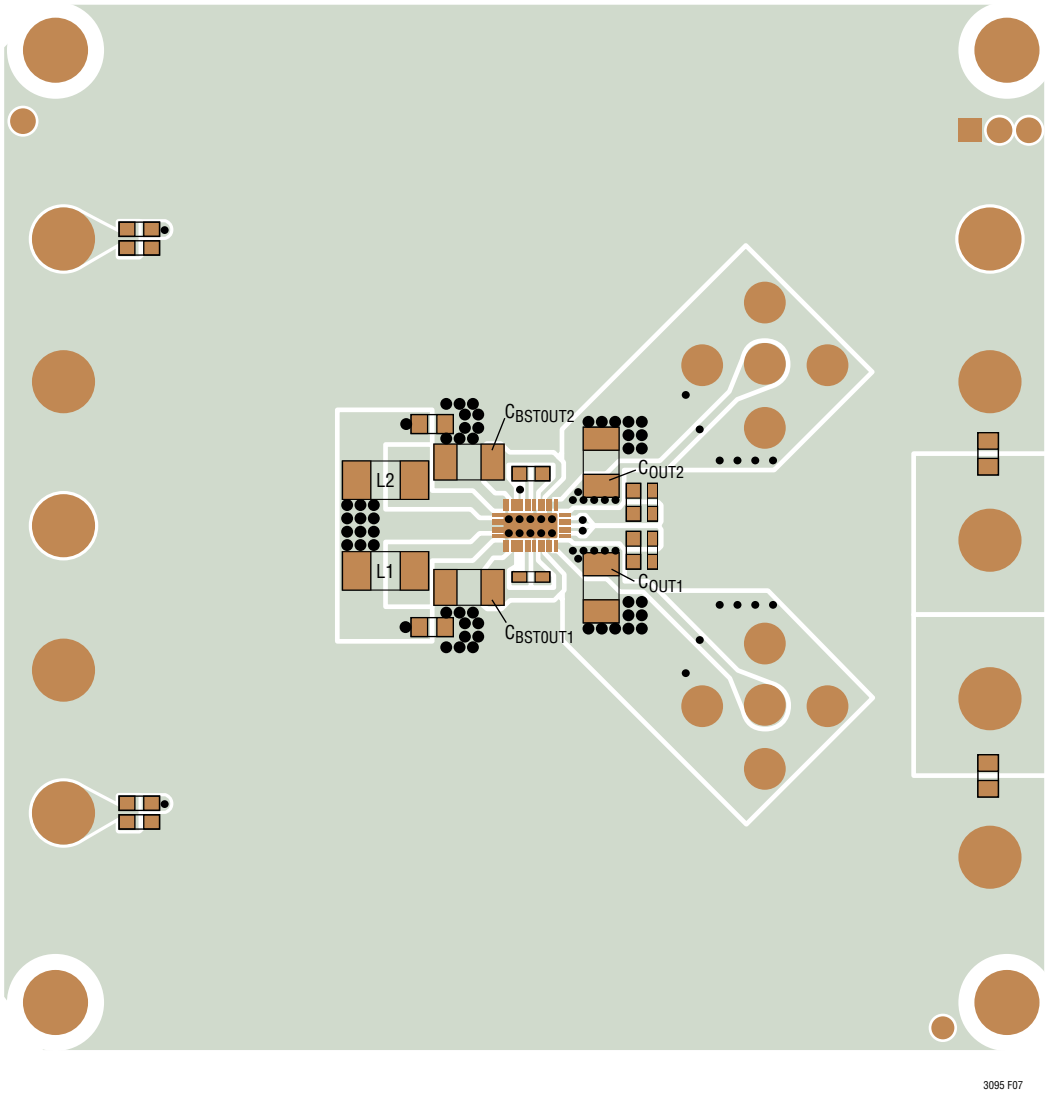


Figure 7. Example PCB Layout, Top Layer (Demo Board DC2270A)

Board Layout

Figure 7 shows a compact two-layer PCB layout designed to minimize the residual switching content at the output. Perhaps the most important component placement is the boost output capacitor, C_{BSTOUT}. A high frequency "hot" loop is formed by the internal power switch, the Schottky diode, and C_{BSTOUT}. The inductance of this loop generates spikes in the boost output and radiates high frequency electromagnetic energy that can feed through the parasitic capacitance of the linear regulator or couple directly to the post-regulator output. Minimize the size of the loop by placing the output capacitor as close as possible to the BSTOUT and adjacent GND pins. Do not force current to flow through vias while circulating around this loop. Furthermore, minimize the SW node trace area to prevent electrostatic coupling of the high dV/dt signal.

While the boost converter hot loop generates electromagnetic energy, the LDO output and reference traces act as antennas that can pick up and deliver it to the load. Reduce coupling onto the output by minimizing the unshielded output PCB trace area and returning C_{OUT} and C_{SET} as close as possible to the adjacent GND pin. Also take care

APPLICATIONS INFORMATION

to eliminate any ground loops between this return point and the reference ground of the regulator's load. In a multilayer board, shielding the output trace with ground conductors can also help prevent coupling.

The presence of a solid ground plane underneath the routing traces can significantly reduce electromagnetic radiation and coupling. The dielectric thickness separating the signal traces and ground plane determine how effective it is. For more information on this topic, and an extended discussion of PCB layout for high-frequency switching converters, read *Application Note 139 – Power Supply Layout and EMI.* The same principles that apply to EMI generation by stand-alone switching converters apply to LT3095 applications where residual ripple is of critical concern. In the end, electromagnetic coupling is likely to be responsible for most of the frequency content observed at the LT3095 output.

Thermal Considerations

The LT3095 has an internal thermal limiting circuit that will protect the device under overload conditions. For continuous normal load conditions, do not exceed the 125°C maximum junction temperature. Carefully consider all sources of thermal resistance from junction-to-ambient. This includes (but is not limited to) junction-to-case, case-to-heat sink interface, heat sink resistance or circuit board-to-ambient, as the application dictates. Consider all additional, adjacent heat generating sources in proximity on the PCB.

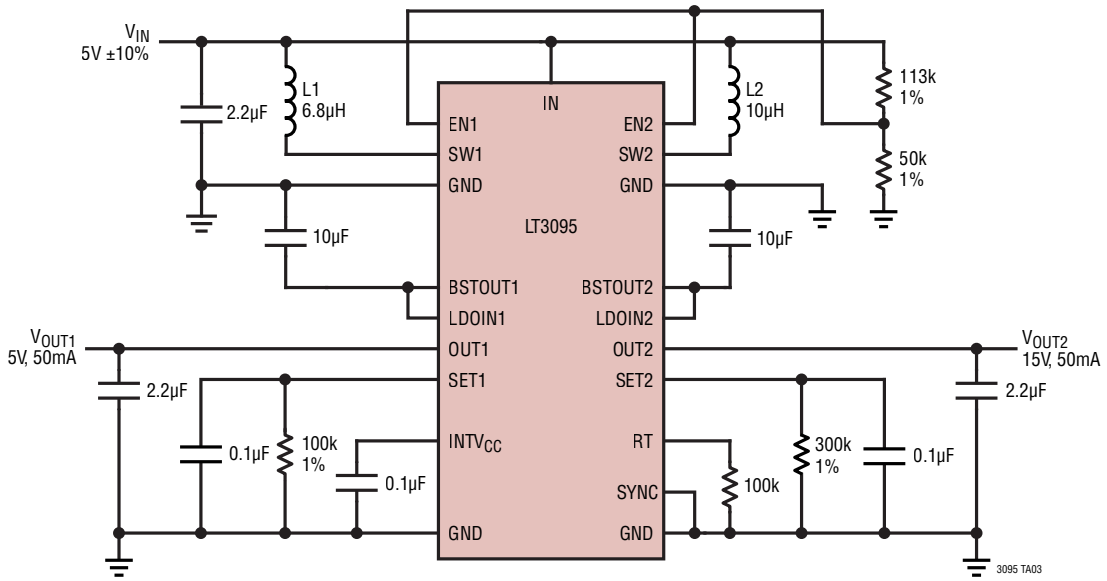
Surface mount packages provide the necessary heat sinking by using the heat spreading capabilities of the PC board, copper traces and planes. Surface mount heat sinks, plated through-holes and solder-filled vias can also spread the heat generated by power devices.

Junction-to-case thermal resistance is specified from the IC junction to the bottom of the case directly, or the bottom of the pin most directly in the heat path. This is the lowest thermal resistance path for heat flow. Only proper device mounting ensures the best possible thermal flow from this area of the packages to the heat sinking material. For further information on thermal resistance and using thermal information, refer to JEDEC standard JESD51, notably JESD51-12.

In typical applications, where V_{IN} is below the desired output voltage, the boost converter will maintain 2V across the linear regulator pass device. In this case, the power dissipation in the linear regulators will be limited to a few hundred milliwatts, even at full load. In applications where the input voltage may exceed one or both of the outputs, the linear regulator will dissipate approximately $(V_{IN} – V_{OUT}) • I_{LOAD}$. In this case, power dissipation may be substantial and extra care should be taken to ensure the maximum junction temperature is not exceeded.

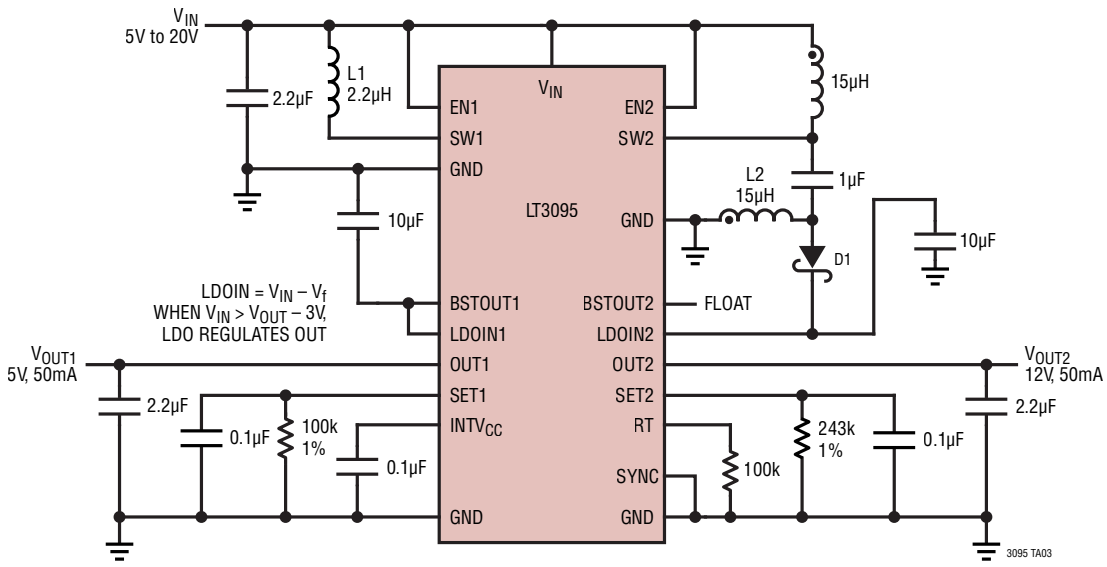
TYPICAL APPLICATIONS

5V V_{IN} with 5V and 15V Outputs and V_{IN} UVLO = 4V



L1: COILCRAFT LPS4012-682MRB
L2: COILCRAFT LPS4012-103MRB

5V to 20V V_{IN} with 5V and 12V Outputs and SEPIC on Channel 2 for Continuous Output Current

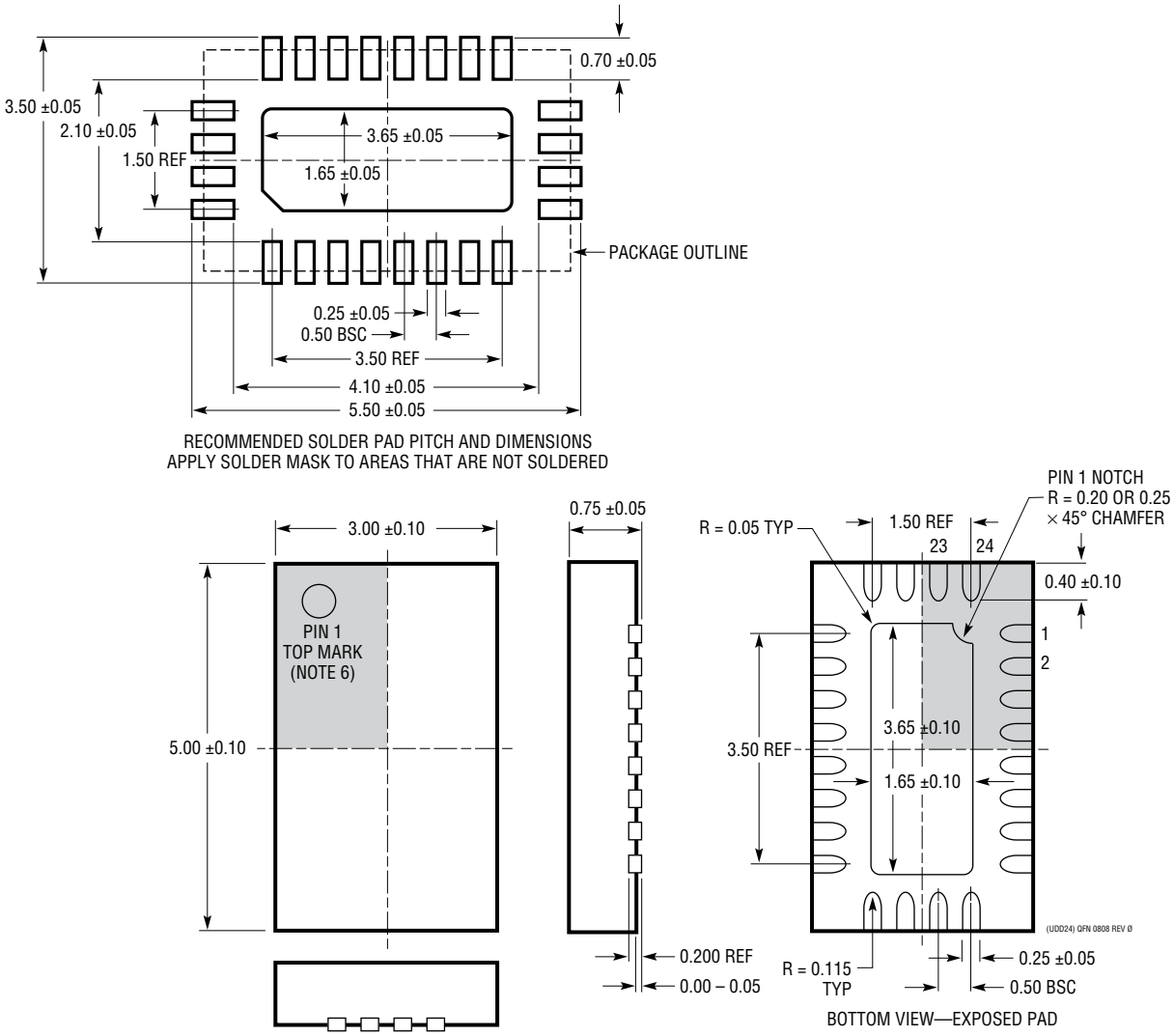


L1 = COILCRAFT LPS4012-222MR
L2 = WÜRTH 74489430150T
D1 = ON SEMI MBR130
V_f = INTERNAL BOOST REGULATOR SCHOTTKY FORWARD VOLTAGE

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC3095#packaging for the most recent package drawings.

UDD Package
24-Lead Plastic QFN (3mm × 5mm)
(Reference LTC DWG # 05-08-1833 Rev Ø)



NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	03/16	Changed Title of Graph	1
		Changed Bandwidth in SET Pin section	13
		Modified High Frequency Edges section	16