Full-Featured LED Driver with 1.5A Switch Current

FEATURES

- **5000:1 True Color PWM™ Dimming Ratio**
- **1.5A, 45V Internal Switch**
- **100mV High Side Current Sense**
- **Open LED Protection**
- **Adjustable Frequency: 250kHz to 2.5MHz**
- **Wide Input Voltage Range:**
  - **Operation from 3V to 30V**
  - **Transient Protection to 40V**
- **Operates in Boost, Buck Mode and Buck-Boost Mode**
- **Gate Driver for PMOS LED Disconnect**
- Constant-Current and Constant-Voltage Regulation
- CTRL Pin Provides 10:1 Analog Dimming
- Low Shutdown Current: <1µA
- Available in (4mm × 4mm) 16-Lead QFN and 16-Pin TSSOP Packages

APPLICATIONS

- Display Backlighting
- Automotive and Avionic Lighting
- Illumination
- Scanners

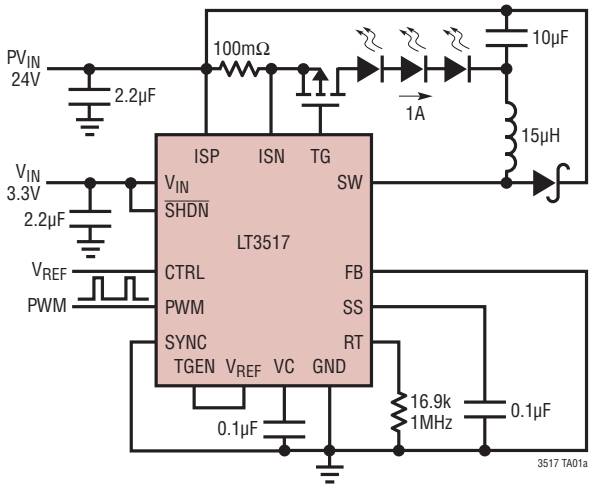
DESCRIPTION

The LT®3517 is a current mode DC/DC converter with an internal 1.5A, 45V switch specifically designed to drive LEDs. The LT3517 operates as a LED driver in boost, buck mode and buck-boost mode. It combines a traditional voltage loop and a unique current loop to operate as a constant-current source or constant-voltage source. Programmable switching frequency allows optimization of the external components for efficiency or component size. The switching frequency of LT3517 can be synchronized to an external clock signal. The LED current is externally programmable with a 100mV sense resistor. The external PWM input provides up to 5000:1 LED dimming. The CTRL pin provides further 10:1 dimming ratio.

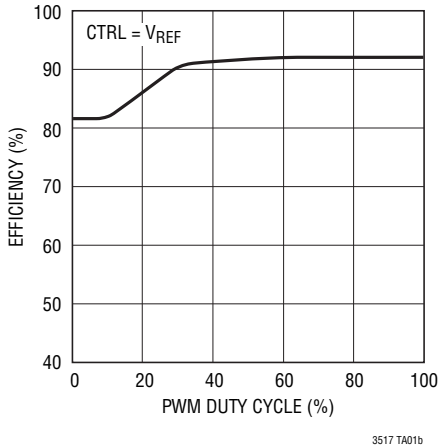
The LT3517 is available in the tiny footprint 16-lead QFN (4mm × 4mm) and the 16-pin TSSOP packages. The LT3517 provides a complete solution for both constant-voltage and constant-current applications.

TYPICAL APPLICATION

1A Buck Mode LED Driver



Efficiency

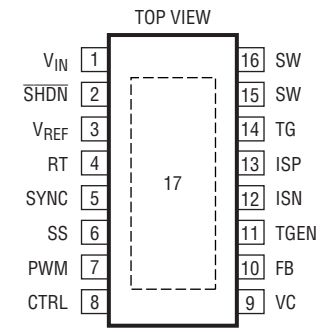


ABSOLUTE MAXIMUM RATINGS (Note 1)

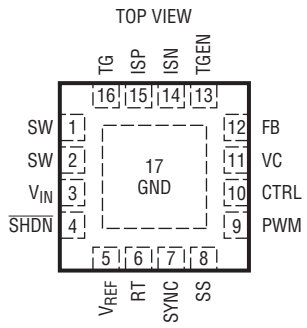
V_{IN}, $\overline{SHDN}$, PWM, TGEN (Note 3) 40V
SW, ISP, ISN, TG 45V
TG Pin Below ISP Pin 10V
FB, SYNC, SS, CTRL 6V
VC, RT, V_{REF} 3V
Operating Junction Temperature Range (Notes 2,4)
LT3517E .....–40°C to 125°C
LT3517I .....–40°C to 125°C
LT3517H .....–40°C to 150°C

Storage Temperature Range
QFN .....–65°C to 150°C
TSSOP .....–65°C to 150°C
Lead Temperature (Soldering, 10 sec)
TSSOP ..... 300°C

PIN CONFIGURATION



FE PACKAGE
16-LEAD PLASTIC TSSOP
T_{JMAX} = 150°C, θ_{JA} = 40°C/W, θ_{JC}(PAD) = 10°C/W



UF PACKAGE
16-LEAD (4mm × 4mm) PLASTIC QFN
T_{JMAX} = 150°C, θ_{JA} = 36°C/W
EXPOSED PAD (PIN 17) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION http://www.linear.com/product/LT3517#orderinfo

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3517EUF#PBF	LT3517EUF#TRPBF	3517	16-Lead (4mm × 4mm) Plastic QFN	–40°C to 125°C
LT3517IUF#PBF	LT3517IUF#TRPBF	3517	16-Lead (4mm × 4mm) Plastic QFN	–40°C to 125°C
LT3517HUF#PBF	LT3517HUF#TRPBF	3517	16-Lead (4mm × 4mm) Plastic QFN	–40°C to 150°C
LT3517EFE#PBF	LT3517EFE#TRPBF	3517FE	16-Lead Plastic TSSOP	–40°C to 125°C
LT3517IFE#PBF	LT3517IFE#TRPBF	3517FE	16-Lead Plastic TSSOP	–40°C to 125°C
LT3517HFE#PBF	LT3517HFE#TRPBF	3517FE	16-Lead Plastic TSSOP	–40°C to 150°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 2) V_{IN} = 5V, $\overline{SHDN}$ = 5V, PWM = 5V unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum V_{IN} Operating Voltage					3	V
Maximum V_{IN} Operating Voltage	Continuous Operation (Note 3)		30			V
Current Sense Voltage ($V_{ISP} – V_{ISN}$)	V_{CTRL} = 2V, V_{ISP} = 24V, VC = 1V V_{CTRL} = 2V, V_{ISP} = 0V, VC = 1V	●	96	100 100	103	mV mV
10% Scale Current Sense Voltage ($V_{ISP} – V_{ISN}$)	V_{CTRL} = 100mV, V_{ISP} = 24V, VC = 1V			9		mV
Current Sense Voltage Line Regulation	2V < V_{ISP} < 45V			0.03		%/V
V_{IN} Supply Current	PWM > 1.5V, VC = 0V PWM = 0V $\overline{SHDN}$ = 0V			6 4.5 0.1	10 1	mA mA µA
Switching Frequency	R_T = 16.7k R_T = 4.03k R_T = 91.5k	● 	0.85 2.25 220	1 2.5 250	1.15 2.7 270	MHz MHz kHz
RT Voltage				1		V
Soft-Start Pin Current	SS = 0.5V, Out of Pin		6	9	12	µA
SYNC Pull-Down Current (Into the Pin)	V_{SYNC} = 2V			60		µA
SYNC Input Low					0.4	V
SYNC Input High			1.5			V
Maximum Duty Cycle	R_T = 91.5k (250kHz) SYNC = 300kHz Clock Signal, R_T = 91.5k R_T = 16.7k (1MHz) R_T = 4.03k (2.5MHz)	 ● 	95 94 85 	97 96 90 74	 	% % % %
Switch Current Limit			1.5	1.9	2.3	A
Switch V_{CESAT}	I_{SW} = 1A			300		mV
Switch Leakage Current	V_{SW} = 45V, PWM = 0V				2	µA
CTRL Input Bias Current	Current Out of Pin, V_{CTRL} = 0.1V			20	100	nA
Error Amplifier Transconductance				550		µS
VC Output Impedance				1000		kΩ
VC Idle Input Bias Current	PWM = 0V, VC = 1V		–20	0	20	nA
FB Pin Input Bias Current	Current Out of Pin, V_{FB} = 0.5V			20	100	nA
FB Pin Threshold		●	0.98	1.01	1.04	V
ISP, ISN Idle Input Bias Current	PWM = 0V, ISP = ISN = 24V				300	nA
ISP, ISN Full-Scale Input Bias Current	ISP Tied to ISN, V_{ISP} = 24V, V_{CTRL} = 2V			20		µA
$\overline{SHDN}$ Voltage High		●	1.2			V
$\overline{SHDN}$ Voltage Low	–40°C ≤ T_J ≤ 125°C 125°C < T_J ≤ 150°C				0.45 0.40	V V
$\overline{SHDN}$ Pin Bias Current				60	100	µA
PWM Input High Voltage		●	1.2			V
PWM Input Low Voltage	–40°C ≤ T_J ≤ 125°C 125°C < T_J ≤ 150°C				0.45 0.40	V V
PWM Pin Bias Current				60	120	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 2) V_{IN} = 5V, $\overline{SHDN}$ = 5V, PWM = 5V unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
TGEN Input High Voltage			1.5			V
TGEN Input Low Voltage					0.4	V
TGEN Pin Bias Current	TGEN = 5V			100	200	µA
V_{REF} Pin Voltage	I_{REF} = –100µA	●	1.96	2	2.04	V
V_{REF} Pin Voltage Line Regulation	3V < V_{IN} < 40V				0.03	%/V
Gate Turn-On Delay	C_{LOAD} = 1nF Between ISP and TG			200		ns
Gate Turn-Off Delay	C_{LOAD} = 1nF Between ISP and TG			200		ns
Top Gate Drive V_{GS} (V_{ISP} – V_{TG})	V_{ISP} = 24V, TGEN = 5V PWM = 0V			7 0	 0.3	V V

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

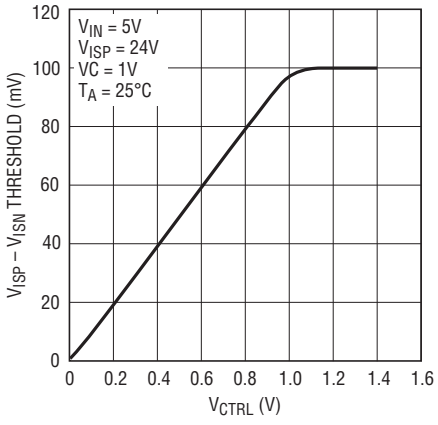
Note 2: The LT3517E is guaranteed to meet performance specifications from 0°C to 125°C operating junction temperature range. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT3517I is guaranteed over the full –40°C to 125°C operating junction temperature range. The LT3517H is guaranteed over the full –40°C to 150°C operating junction temperature range. Operating lifetime is derated at junction temperatures greater than 125°C.

Note 3: Absolute maximum voltage at V_{IN}, $\overline{SHDN}$, PWM and TGEN pins is 40V for nonrepetitive 1 second transients and 30V for continuous operation.

Note 4: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed the maximum operating junction temperature when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

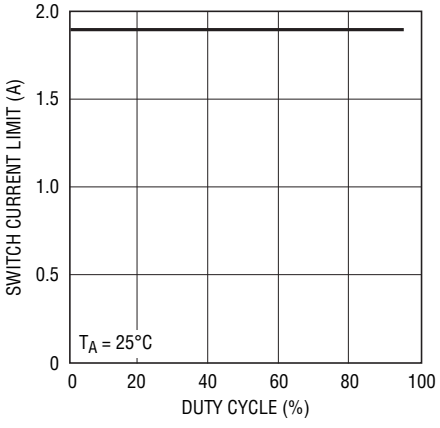
TYPICAL PERFORMANCE CHARACTERISTICS

V_{ISP} – V_{ISN} Threshold vs V_{CTRL}



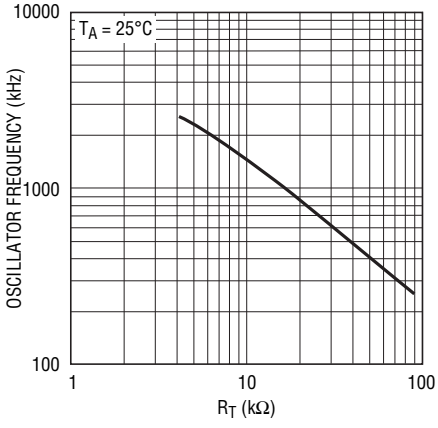
3518 G01

Switch Current Limit vs Duty Cycle



3517 G02

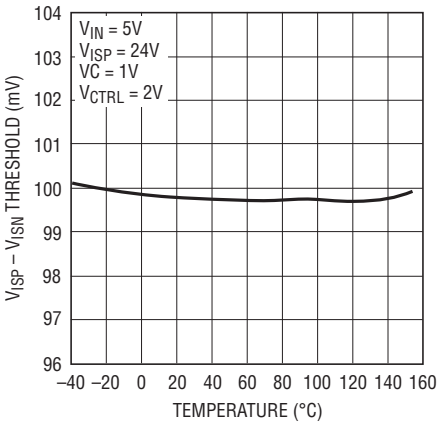
Oscillator Frequency vs R_T



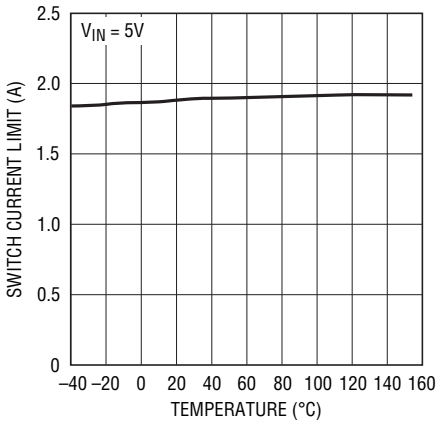
3518 G03

TYPICAL PERFORMANCE CHARACTERISTICS

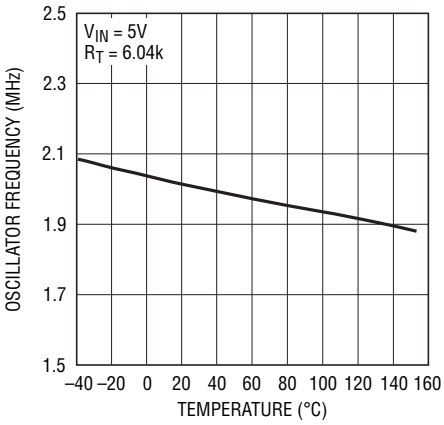
$V_{ISP} – V_{ISN}$ Threshold vs Temperature



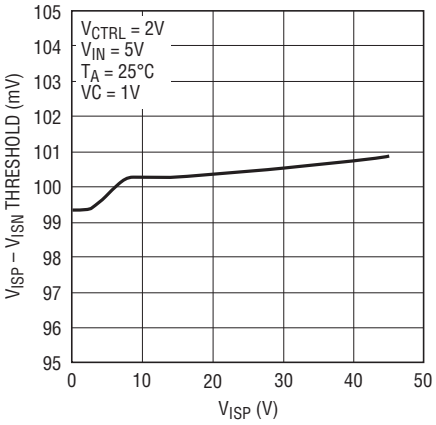
Switch Current Limit vs Temperature



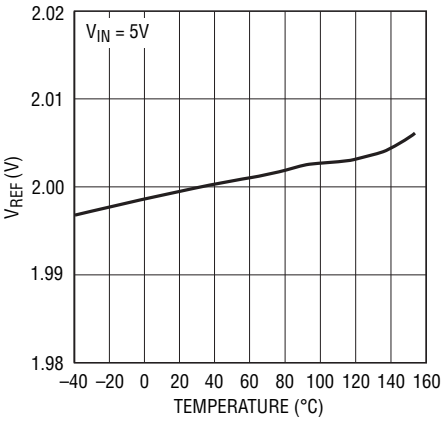
Oscillator Frequency vs Temperature



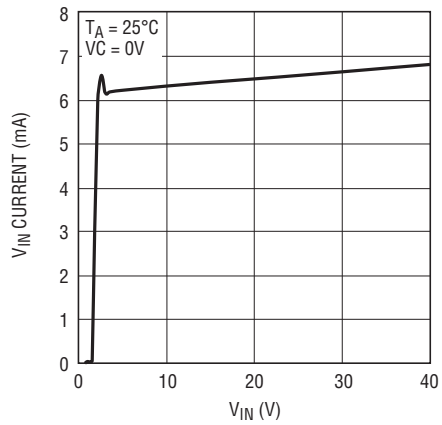
$V_{ISP} – V_{ISN}$ Threshold vs V_{ISP}



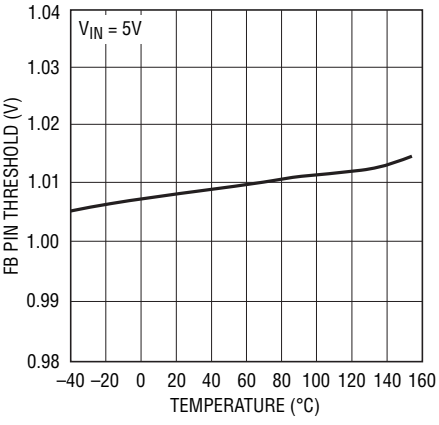
Reference Voltage vs Temperature



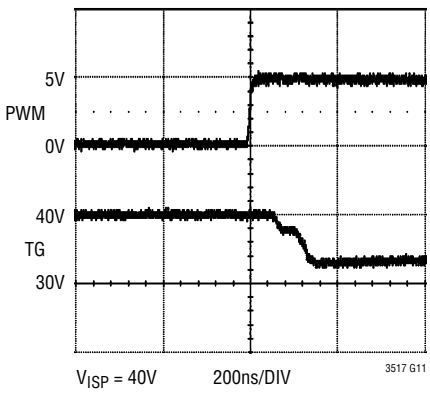
Quiescent Current vs V_{IN}



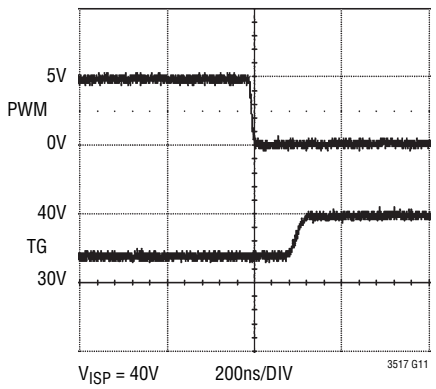
FB Pin Threshold vs Temperature



PMOS Turn-On



PMOS Turn-Off



PIN FUNCTIONS

SW: Switch Pin. Minimize trace at this pin to reduce EMI.

V_{IN}: Input Supply Pin. Must be locally bypassed.

$\overline{SHDN}$: Shutdown Pin. Tie to 1.5V or higher to enable device or 0.4V or less to disable device.

V_{REF}: Reference Output Pin. This pin can supply up to 100µA.

RT: Switching Frequency Adjustment Pin. Set switching frequency using a resistor to GND (see Typical Performance Characteristics for values). For SYNC function, choose the resistor to program a frequency 20% slower than the SYNC pulse frequency. Do not leave this pin open.

SYNC: Frequency Synchronization Pin. Tie an external clock signal here. R_T resistor should be chosen to program a switching frequency 20% slower than SYNC pulse frequency. Synchronization (power switch turn-on) occurs a fixed delay after the rising edge of SYNC. Tie the SYNC pin to ground if this feature is not used.

SS: Soft-Start Pin. Place a soft-start capacitor here. Leave the pin open if not in use.

PWM: Pulse Width Modulated Input Pin. Signal low turns off channel, disables the main switch and makes the TG pin high. Tie the PWM pin to V_{REF} pin or $\overline{SHDN}$ pin if not used. There is an equivalent 50k resistor from PWM pin to ground internally.

CTRL: LED Current Adjustment Pin. Sets voltage across sense resistor between ISP and ISN. Connect directly to V_{REF} for full-scale threshold of 100mV, or use signal values between GND and 1V to modulate LED current. Tie the CTRL pin to the V_{REF} pin if not used.

VC: g_m Error Amplifier Output Pin. Stabilize the loop with an RC network or compensating C.

FB: Voltage Loop Feedback Pin. Works as overvoltage protection for LED drivers. If FB is higher than 1V, the main switch is turned off.

TGEN: Top Gate Enable Input Pin. Tie to 1.5V or higher to enable the PMOS driver function. Tie the TGEN pin to ground if TG function is not used. There is an equivalent 40k resistor from TGEN pin to ground internally.

ISN: Current Sense (–) Pin. The inverting input to the current sense amplifier.

ISP: Current Sense (+) Pin. The noninverting input to the current sense amplifier. Also serves as positive rail for TG pin driver.

TG: Top Gate Driver Output. An inverted PWM signal drives series PMOS device between V_{ISP} and (V_{ISP} – 7V). An internal 7V clamp protects the PMOS gate. Leave TG unconnected if not used.

GND: Exposed Pad (QFN Package). Solder paddle directly to ground plane.

BLOCK DIAGRAM

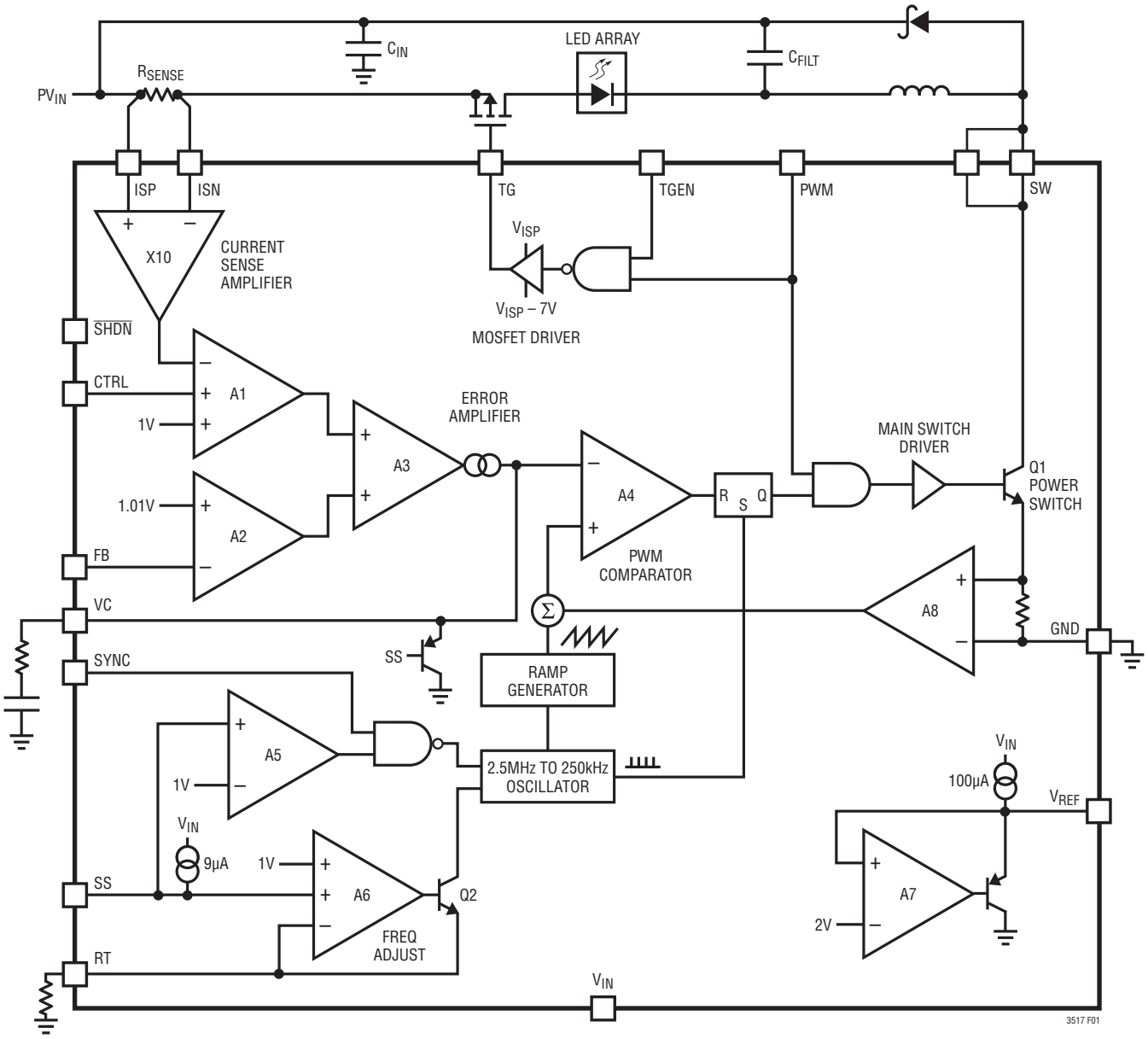


Figure 1. Buck Mode LED Driver

OPERATION

The LT3517 is a constant frequency, current mode regulator with an internal power switch. Operation can be best understood by referring to the Block Diagram in Figure 1. At the start of each oscillator cycle, the SR latch is set, which turns on the Q1 power switch. A voltage proportional to the switch current is added to a stabilizing ramp and the resulting sum is fed into the positive terminal of the PWM comparator, A4. When this voltage exceeds the level at the negative input of A4, the SR latch is reset, turning off the power switch. The level at the negative input of A4 is set by the error amplifier A3. A3 has two inputs, one from the voltage feedback loop and the other one from the current loop. Whichever feedback input is lower takes precedence, and forces the converter into either constant-current or constant-voltage mode. The LT3517 is designed to transition cleanly between these two modes of operation. The current sense amplifier senses the voltage across R_{SENSE} and provides a pre-gain to amplifier A1. The output of A1 is simply an amplified version of the difference between the voltage across R_{SENSE} and the lower of $V_{CTRL}/10$ or 100mV. In this manner, the error amplifier sets the correct peak switch current level to regulate the current through R_{SENSE}. If the error amplifier's output increases, more current is delivered to the output; if it decreases, less current is delivered. The current regulated in R_{SENSE} can be adjusted by changing the input voltage V_{CTRL}. The current sense amplifier provides rail-to-rail current sense operation. The FB voltage loop is implemented by the amplifier A2. When the voltage loop dominates, the error amplifier and the amplifier A2 regulate the FB pin to 1.01V (constant-voltage mode).

Dimming of the LED array is accomplished by pulsing the LED current using the PWM pin. When the PWM pin is low, switching is disabled and the error amplifier is turned off so that it does not drive the VC pin. Also, all internal loads on the VC pin are disabled so that the charge state of the VC pin will be saved on the external compensation capacitor. This feature reduces transient recovery time. When the PWM input again transitions high, the demand current for the switch returns to the value just before PWM last transitioned low. To further reduce transient recovery time, an external PMOS is used to disconnect the LED array current loop when PWM is low, stopping C_{FILT} from discharging.

APPLICATIONS INFORMATION

Dimming Control

There are two methods to control the current source for dimming using the LT3517. The first method uses the PWM pin to modulate the current source between zero and full current to achieve a precisely programmed average current. To make this method of current control more accurate, the switch demand current is stored on the VC node during the quiescent phase. This feature minimizes recovery time when the PWM signal goes high. To further improve the recovery time, a disconnect switch is used in the LED current path to prevent the output capacitor from discharging in the PWM signal low phase. The minimum PWM on or off time will depend on the choice of operating frequency through RT input pin or SYNC pin. When using the SYNC function, the SYNC and PWM signals must have the aligned rising edges to achieve the optimized high PWM dimming ratio. For best current accuracy, the minimum PWM low or high time should be at least four switching cycles (2µs for f_{SW} = 2MHz). Maximum PWM period is determined by the system and is unlikely to be longer than 12ms. The maximum PWM dimming ratio (PWM_{RATIO}) can be calculated from the maximum PWM period (t_{MAX}) and the minimum PWM pulse width (t_{MIN}) as follows:

$$PWM_{RATIO} = \frac{t_{MAX}}{t_{MIN}} \quad (1)$$

Example:

t_{MAX} = 10ms, t_{MIN} = 2µs (f_{SW} = 2MHz)

PWM_{RATIO} = 10ms/2µs = 5000:1

The second method of dimming control uses the CTRL pin to linearly adjust the current sense threshold during

APPLICATIONS INFORMATION

the PWM high state. When the CTRL pin voltage is less than 1V, the LED current is:

$$I_{LED} = \frac{V_{CTRL}}{10 \bullet R_{SENSE}} \quad (2)$$

When V_{CTRL} is higher than 1V, the LED current is clamped to be:

$$I_{LED} = \frac{100mV}{R_{SENSE}} \quad (3)$$

The LED current programming feature possibly increases total dimming range by a factor of ten.

The CTRL pin should not be left open (tie to V_{REF} if not used). The CTRL pin can also be used in conjunction with a PTC thermistor to provide overtemperature protection for the LED load.

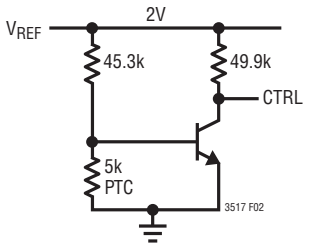


Figure 2

Setting Output Voltage

For a boost application, the output voltage can be set by selecting the values of R1 and R2 (see Figure 3) according to the following equation:

$$V_{OUT} = \left(\frac{R1}{R2} + 1\right) \bullet 1.01V \quad (4)$$

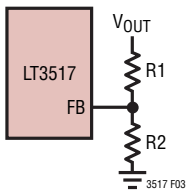


Figure 3

For a buck or a buck-boost configuration, the output voltage is typically level-shifted to a signal with respect to GND, as illustrated in the Figure 4. The output can be expressed as:

$$V_{OUT} = \frac{R1}{R2} \bullet 1.01V + V_{BE(Q1)} \quad (5)$$

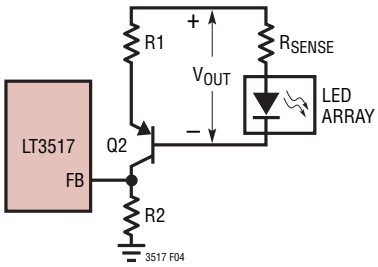


Figure 4

Inductor Selection

The inductor used with the LT3517 should have a saturation current rating of 2A or greater. For buck mode LED drivers, the inductor value should be chosen to give a ripple current "ΔI" of ~30% to 40% of the LED current. In the buck mode, the inductor value can be estimated using the formula:

$$L(\mu H) = \frac{D_{BUCK} \bullet t_{SW}(\mu s) \bullet (V_{IN} - V_{LED})}{\Delta I} \quad (6)$$

$$D_{BUCK} = \frac{V_{LED}}{V_{IN}}$$

V_{LED} is the voltage across the LED string, V_{IN} is the input voltage to the converter, and t_{SW} is the switching period. In the boost configuration, the inductor can be estimated using the formula:

$$L(\mu H) = \frac{D_{BOOST} \bullet t_{SW}(\mu s) \bullet V_{IN}}{\Delta I} \quad (7)$$

$$D_{BOOST} = \frac{V_{LED} - V_{IN}}{V_{LED}}$$

APPLICATIONS INFORMATION

Table 1 provides some recommended inductor vendors.

Table 1. Inductor Manufacturers

VENDOR	PHONE	WEB
Sumida	(408) 321-9660	www.sumida.com
Toko	(408) 432-8281	www.toko.com
Cooper	(561) 998-4100	www.cooperet.com
Vishay	(402) 563-6866	www.vishay.com

Input Capacitor Selection

For proper operation, it is necessary to place a bypass capacitor to GND close to the V_{IN} pin of the LT3517. A 1µF or greater capacitor with low ESR should be used. A ceramic capacitor is usually the best choice.

In the buck mode configuration, the capacitor at the input to the power converter has large pulsed currents due to the current returned though the Schottky diode when the switch is off. For best reliability, this capacitor should have low ESR and ESL and have an adequate ripple current rating. The RMS input current is:

$$I_{IN(RMS)} = I_{LED} \bullet \sqrt{(1-D) \bullet D} \quad (8)$$

where D is the switch duty cycle. A 2.2µF ceramic type capacitor is usually sufficient.

Output Capacitor Selection

The selection of output capacitor depends on the load and converter configuration, i.e., step-up or step-down. For LED applications, the equivalent resistance of the LED is typically low, and the output filter capacitor should be sized to attenuate the current ripple.

To achieve the same LED ripple current, the required filter capacitor value is larger in the boost and buck-boost mode applications than that in the buck mode applications. For LED buck mode applications, a 1µF ceramic capacitor is usually sufficient. For the LED boost and buck-boost mode applications, a 2.2µF ceramic capacitor is usually sufficient. Very high performance PWM dimming applications may require a larger capacitor value to support the LED voltage during PWM transitions.

Use only ceramic capacitors with X7R, X5R or better dielectric as they are best for temperature and DC bias stability of the capacitor value. All ceramic capacitors exhibit loss of capacitance value with increasing DC voltage bias, so it may be necessary to choose a higher value capacitor to get the required capacitance at the operation voltage. Always check that the voltage rating of the capacitor is sufficient. Table 2 shows some recommended capacitor vendors.

Table 2. Ceramic Capacitor Manufacturers

VENDOR	PHONE	WEB
Taiyo Yuden	(408) 573-4150	www.t-yuden.com
AVX	(843) 448-9411	www.avxcorp.com
Murata	(770) 436-1300	www.murata.com
TDK	(847) 803-6100	www.tdk.com

Loop Compensation

The LT3517 uses an internal transconductance error amplifier whose VC output compensates the control loop. The external inductor, output capacitor, and the compensation resistor and capacitor determine the loop stability. The inductor and output capacitor are chosen based on performance, size and cost. The compensation resistor and capacitor at VC are selected to optimize control loop stability. For typical LED applications, a 10nF compensation capacitor at VC is adequate and a series resistor is not required. A compensation resistor may be used to increase the slew rate on the VC pin to maintain tighter regulation of LED current during fast transients on V_{IN} or CTRL.

Diode Selection

The Schottky diode conducts current during the interval when the switch is turned off. Select a diode rated for the maximum SW voltage. If using the PWM feature for dimming, it is important to consider diode leakage, which increases with the temperature, from the output during the PWM low interval. Therefore, choose the Schottky diode with sufficiently low leakage current. Table 3 has some recommended component vendors.

APPLICATIONS INFORMATION

Table 3. Schottky Diodes

PART NUMBER	V_R (V)	I_{AVE} (A)
Diodes Inc.		
DFLS160	60	1
Zetex		
ZLLS1000TA	40	1
International Rectifier		
10MQ060N	60	1.5

Board Layout

The high speed operation of the LT3517 demands careful attention to board layout and component placement. The Exposed Pad of the package is the only GND terminal of the IC and is also important for thermal management of the IC. It is crucial to achieve a good electrical and thermal contact between the Exposed Pad and the ground plane of the board. To reduce electromagnetic interference (EMI), it is important to minimize the area of the SW node. Use a GND plane under SW and minimize the length of traces in the high frequency switching path between SW and GND through the diode and the capacitors. Since there is a small DC input bias current to the ISN and ISP inputs, resistance in series with these inputs should be minimized and matched, otherwise there will be an offset. Finally, the bypass capacitor on the V_{IN} supply to the LT3517 should be placed as close as possible to the V_{IN} terminal of the device.

Soft-Start

For many applications, it is necessary to minimize the inrush current at start-up. The built-in soft-start circuit significantly reduces the start-up current spike and output voltage overshoot. A typical value for the soft-start capacitor is 0.1µF.

Switching Frequency

There are two methods to set the switching frequency of LT3517. Both methods require a resistor connected at RT pin. Do not leave the RT pin open. Also, do not load this pin with a capacitor. A resistor must always be connected for proper operation. One way to set the frequency is simply connecting an external resistor between the RT pin and GND. See Table 4 below or see the Oscillator Frequency vs R_T graph in the Typical Performance Characteristics for resistor values and corresponding switching frequencies.

Table 4. Switching Frequency vs R_T

Switching Frequency (kHz)	R_T (kΩ)
250	90.9
500	39.2
1000	16.9
1500	9.53
2000	6.04
2500	4.02

The other way is to make the LT3517 synchronize with an external clock via SYNC pin. For proper operation, a resistor should be connected at the RT pin and be able to generate a switching frequency 20% lower than the external clock when external clock is absent.

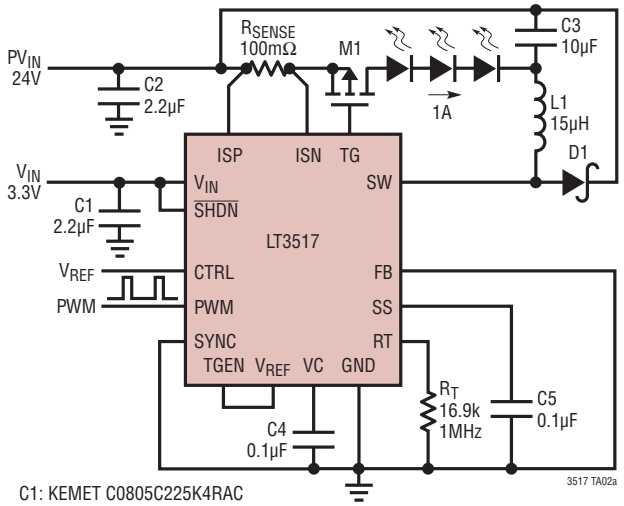
In general, a lower switching frequency should be used where either very high or very low switching duty cycle operation is required, or high efficiency is desired. Selection of a higher switching frequency will allow use of smaller value external components and yield a smaller solution size and profile.

Thermal Considerations

The LT3517 is rated to a maximum input voltage of 30V for continuous operation, and 40V for nonrepetitive one second transients. Careful attention must be paid to the internal power dissipation of the LT3517 at higher input voltages to ensure that the maximum junction temperature is not exceeded. This junction limit is especially important when operating at high ambient temperatures. The Exposed Pad on the bottom of the package must be soldered to a ground plane. This ground should then be connected to an internal copper ground plane with thermal vias placed directly under the package to spread out the heat dissipated by the LT3517.

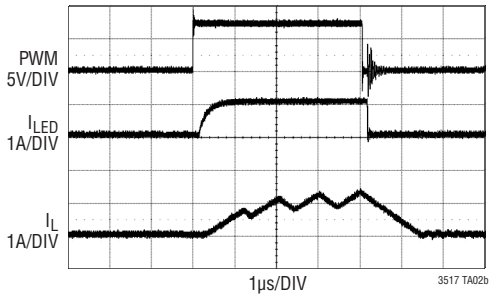
TYPICAL APPLICATIONS

Buck Mode 1A LED Driver



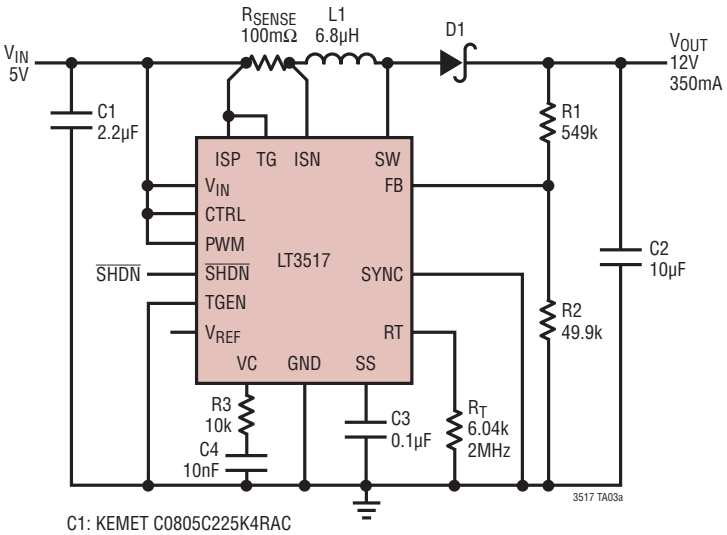
C1: KEMET C0805C225K4RAC
C2: MURATA GRM31MR71E225KA93
C3: MURATA GRM32DR71E106KA12B
C4, C5: MURATA GRM21BR71H104KA01B
D1: DIODES DFLS160
L1: TOKO B992AS-150M
LEDS: LUXEON K2 (WHITE)
M1: ZETEX ZXMP6A13FTA

2000:1 PWM Dimming at 120Hz



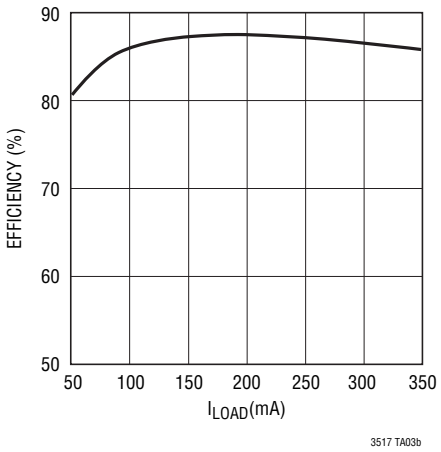
PV_{IN} = 24V
f_{OSC} = 1MHz
I_{LED} = 1A

350mA, 5V to 12V Boost Converter with Accurate Input Current Limit



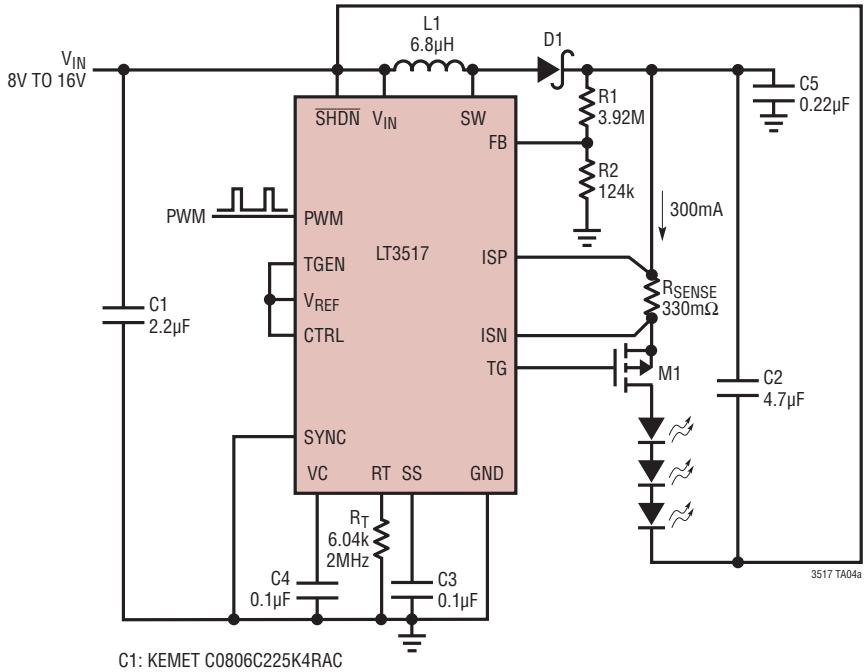
C1: KEMET C0805C225K4RAC
C2: KEMET C1206C106K4RAC
C3: MURATA GRM21BR71H104KA01B
C4: MURATA GCM033R71A103KA03
D1: ZETEX ZLLS1000TA
L1: TOKO B992AS-6R8N

Efficiency



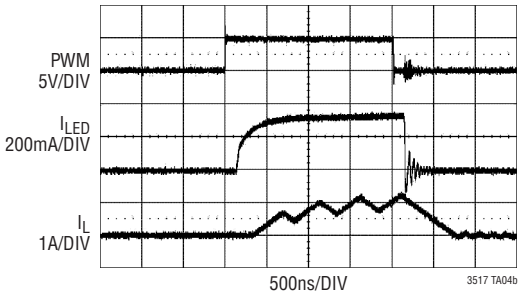
TYPICAL APPLICATIONS

Buck-Boost Mode LED Driver



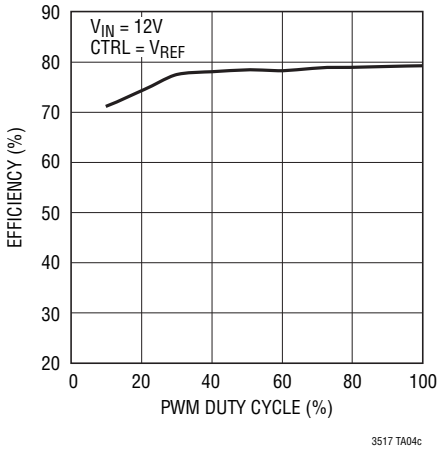
C1: KEMET C0806C225K4RAC
C2: KEMET C1206C475K3RAC
C3, C4: MURATA GRM21BR71H104KA01B
C5: MURATA GRM21BR71H224KA01B
D1: DIODE DFLS160
L1: TOKO B992AS-6R8N
LEDS: LUXEON I (WHITE)
M1: ZETEX ZXMP6A13FTA

5000:1 PWM Dimming at 100Hz



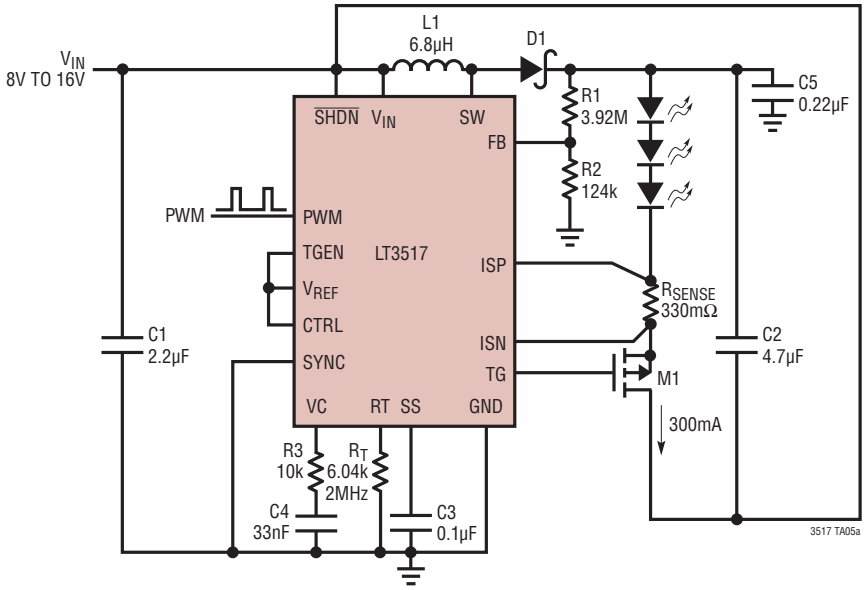
VIN = 12V
fOSC = 2MHz
ILED = 300mA

Efficiency



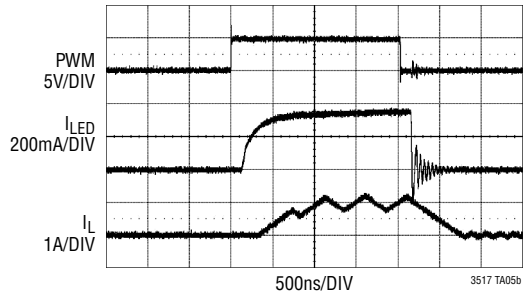
TYPICAL APPLICATIONS

Low Side Current Sensing Load Dump Protected Buck-Boost Mode LED Driver



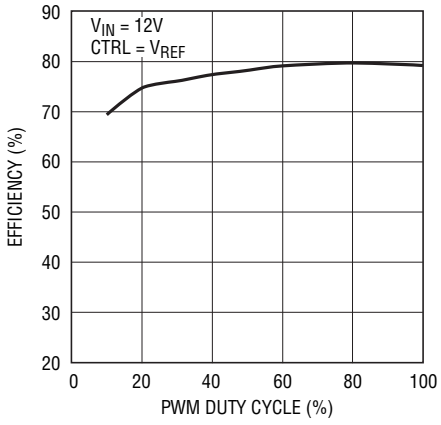
D1: DIODES DFLS160
L1: TOKO B992AS-6R8N
C1: KEMET C0806C225K4RAC
C2: KEMET C1206C475K3RAC
C3: MURATA GRM21BR71H104KA01B
C4: MURATA GRM219R71H333KAQ01B
C5: MURATA GRM21BR71H224KA01B
M1: ZETEX ZXMP6A13FTA
LEDs: LUXEON I (WHITE)

5000:1 PWM Dimming at 100Hz

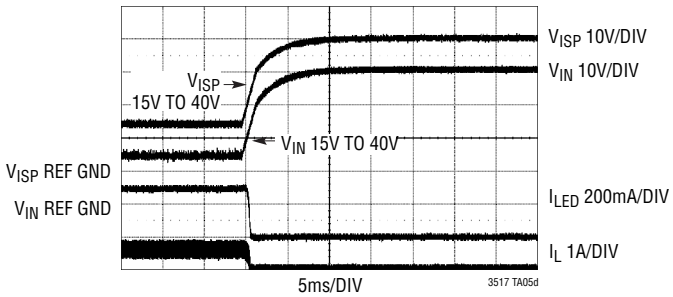


VIN = 12V
fOSC = 2MHz
ILED = 300mA

Efficiency



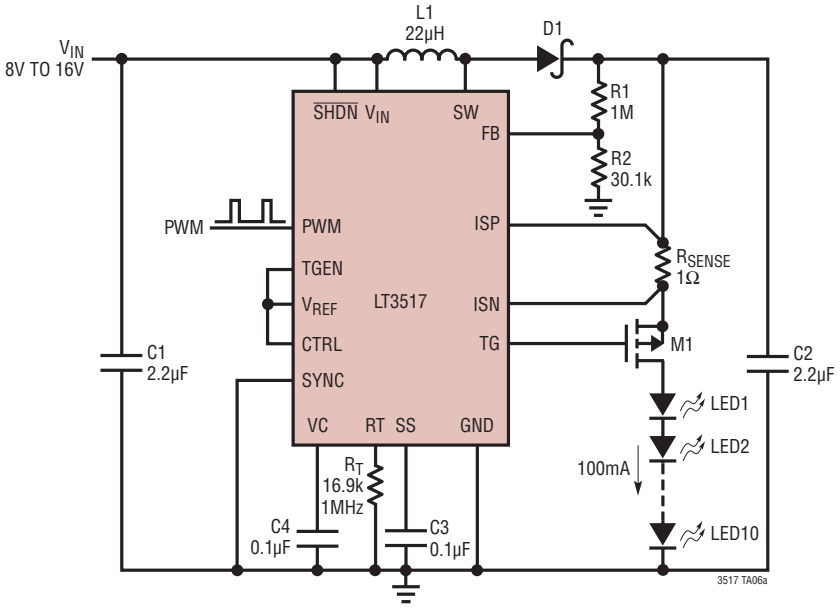
Load Dump Response



VIN Raises From 15V to 40V in 5ms.

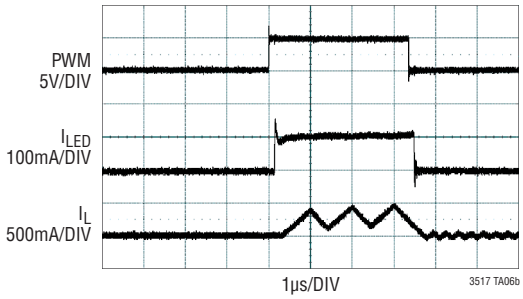
TYPICAL APPLICATIONS

Boost 100mA LED Driver with LED Open Protection



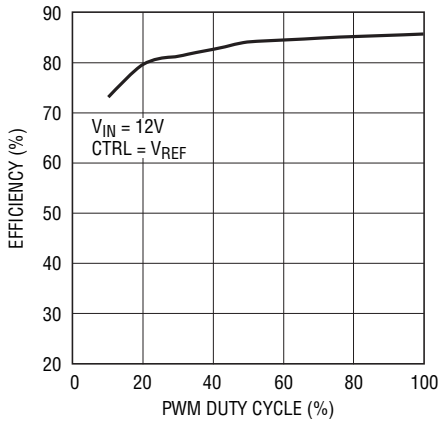
C1, C2: KEMET C1206C225K2RAC
C3, C4: MURATA GRM21BR71H104KA01B
D1: DIODES DFLS160
L1: COILCRAFT DS3316P-223
LEDS: CREE XLAMP 7090
M1: ZETEX ZXMP6A13FTA

3000:1 PWM Dimming at 100Hz



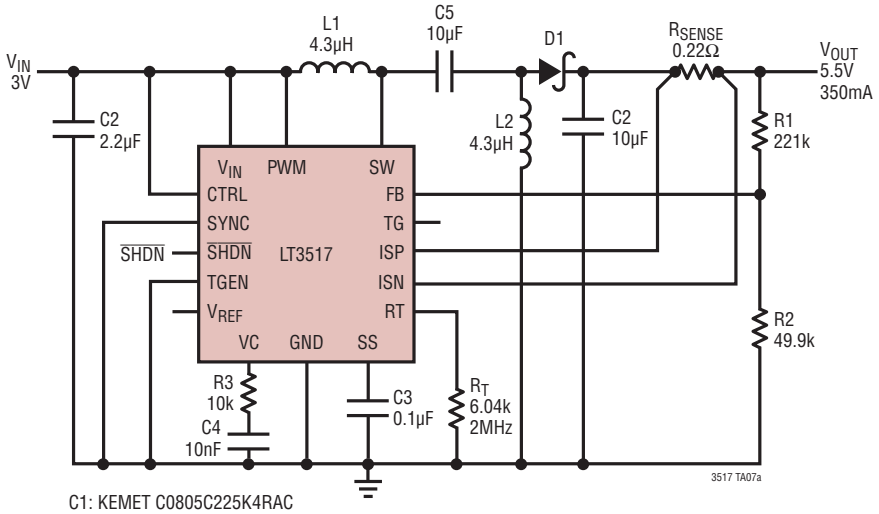
VIN = 12V
fOSC = 1MHz
ILED = 100mA

Efficiency



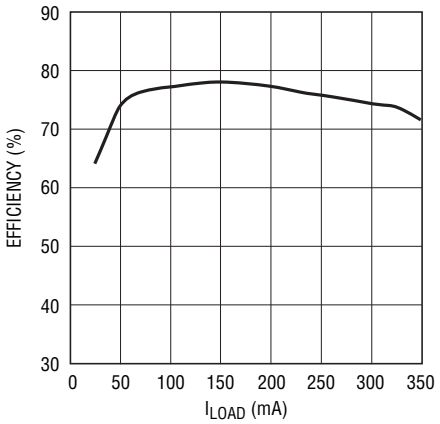
TYPICAL APPLICATION

5.5V SEPIC Converter with Short-Circuit Protection



C1: KEMET C0805C225K4RAC
C2, C5: KEMET C1206C106K4RAC
C3: MURATA GRM21BR71H104KA01B
C4: MURATA GCM033R71A103KA03
D1: ZETEX ZLLS1000TA
L1, L2: TOKO B992AS-4R3N

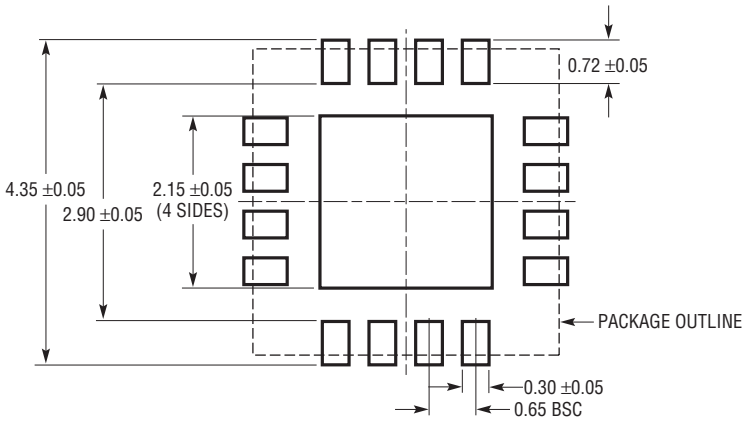
Efficiency



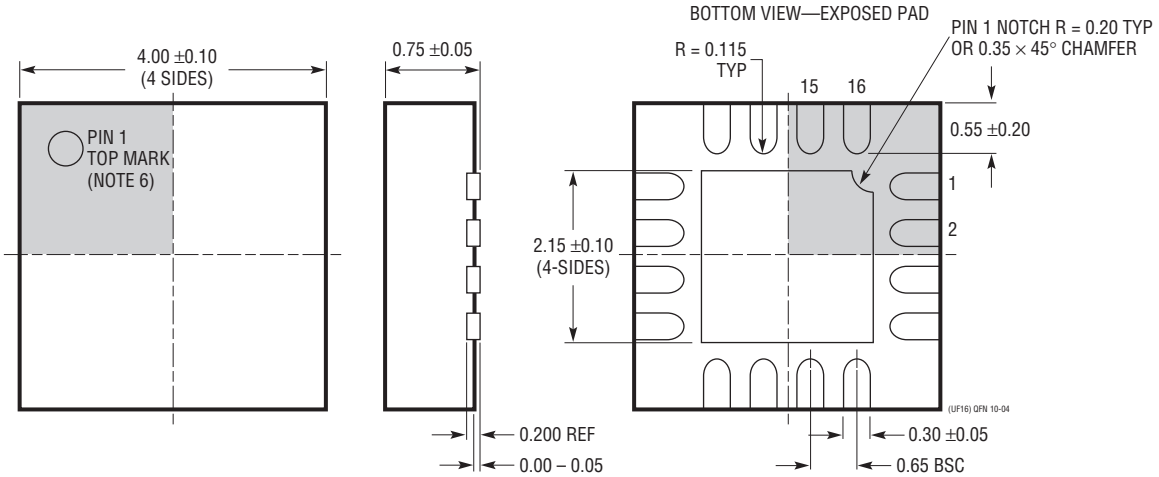
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LT3517#packaging for the most recent package drawings.

UF Package
16-Lead Plastic QFN (4mm × 4mm)
(Reference LTC DWG # 05-08-1692 Rev Ø)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

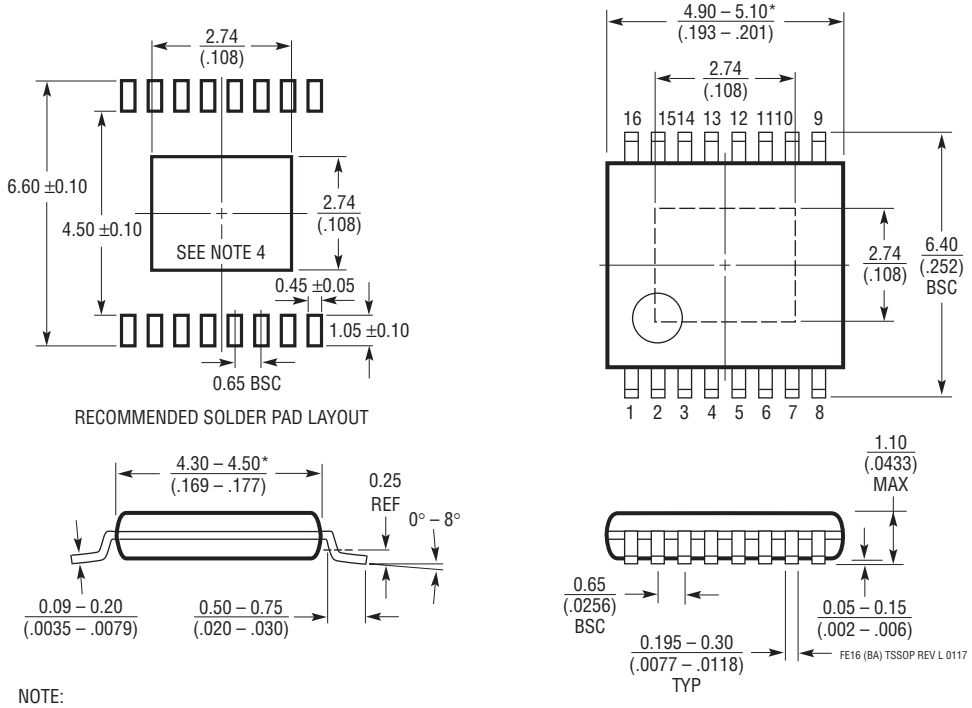


NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGGC)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LT3517#packaging for the most recent package drawings.

FE Package
16-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1663 Rev L)
Exposed Pad Variation BA



NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{\text{(INCHES)}}$
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT

*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

REVISION HISTORY (Revision history begins at Rev C)

REV	DATE	DESCRIPTION	PAGE NUMBER
C	4/10	Added H-grade to Order Information Section	2
D	7/10	Added conditions to ISP, ISN Idle Input Bias Current parameters	3
		Changed V_{IN} current sense to 9µA in Figure 1	7
E	01/11	Updated Electrical Characteristics	3
F	04/12	Subscript added to V_C Pin Label	1
		R_T changed to RT in ABS Max Table, QFM Max Temp changed to 150°C	2
		Added Operating in Note 2	4
		Clarified Application Schematics	15, 16
		Package Diagram Updated	18
G	04/13	Clarified Application schematic	15
H	03/17	Clarified $T_{J(MAX)}$	2