IO-Link Transceiver with Integrated Step-Down Regulator and LDO

FEATURES

- **IO-Link® PHY Compatible (COM1/COM2/COM3)**
- **Cable Interface Protected to ±60V**
- **Operation from 7.5V to 40V**
- **Integrated Step-Down Switching Regulator**
  - Max Load Current: 100mA (LT3669)/ 300mA (LT3669-2)
  - Synchronizable and Adjustable Switching Frequency: 250kHz to 2.2MHz
  - Output Voltage: 0.8V to 16V
- **Integrated 150mA LDO Linear Regulator**
- **Rugged Line Drivers with Adjustable Slew Rate and Current Limit**
- **Adaptive Line Driver Pulsing Scheme to Switch Heavy Loads Safely**
- **Drivers Configurable as Push-Pull, Pull-Up or Pull-Down**
- Adjustable Power-On Reset Timer
- Small 28-Pin Thermally Enhanced 4mm × 5mm QFN Package

APPLICATIONS

- Industrial Sensors and Actuators

DESCRIPTION

The LT®3669 is an industrial transceiver that includes a step-down switching regulator and a low dropout linear regulator. Wake-up detect functionality, as well as a programmable power-on reset timer are also included. The current limit and slew rate of the transmitters are externally adjustable for optimum EMC performance.

The line drivers can source/sink up to 250mA of current each or 500mA when connected together, with a minimal residual voltage of less than 2.1V. An internal adaptive pulsing scheme allows the drivers to safely switch heavy capacitive loads and incandescent bulbs. Thermal shutdown provides additional protection. Line protection of ±60V in the line interface pins allows the use of standard TVS diodes with L+ operating voltages up to 40V.

The switching regulator integrates the catch diode in LT3669 (up to 100mA load current) and requires an external catch diode in LT3669-2 (up to 300mA load current).

The LT3669 implements an IO-Link device PHY. For IO-Link master designs, see the LTC2874.

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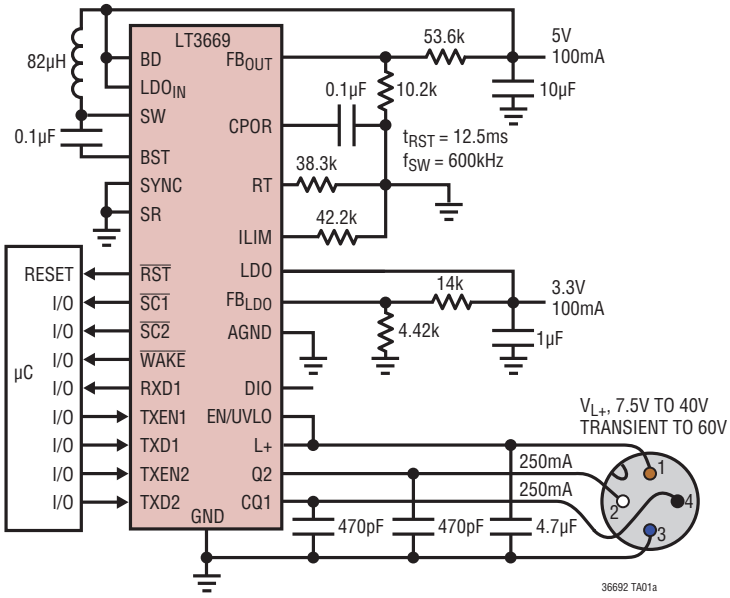
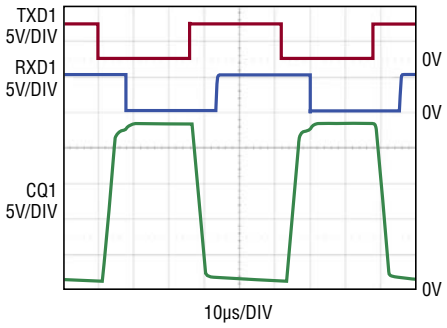
TYPICAL APPLICATION



36692 TA01a

Operating Waveforms



(RXD1 PULL-UP RESISTOR = 10k)

36692 TA01b

ABSOLUTE MAXIMUM RATINGS (Notes 1 and 2)

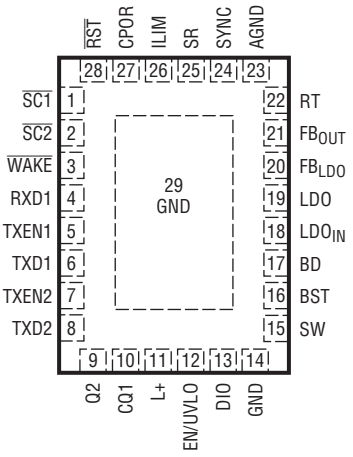
L+, EN/UVLO Voltage (Note 3) ..... –60V to 60V
CQ1, Q2 Voltage ..... –60V to 60V
(L+ to CQ1), (L+ to Q2) Voltage ..... –60V to 60V
DIO, LDO_{IN} Voltage (Note 3) ..... –0.3V to 60V
DIO Above L+ Voltage 90V
BST Voltage 50V
BST Above SW Voltage 30V
BD Voltage 30V
LDO Voltage 8V
LDO Above LDO_{IN} Voltage 0.3V

FB_{OUT}, FB_{LDO}, SYNC Voltage 6V
CPOR, RT, ILIM Voltage 3V
SR, TXEN1, TXD1, TXEN2, TXD2 Voltage 30V
$\overline{SC1}$, $\overline{SC2}$, $\overline{WAKE}$, $\overline{RST}$, RXD1 Voltage 30V
Operating Junction Temperature Range (Notes 4 and 5)
LT3669E ..... –40°C to 125°C
LT3669I ..... –40°C to 125°C
LT3669H ..... –40°C to 150°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION

LT3669

TOP VIEW

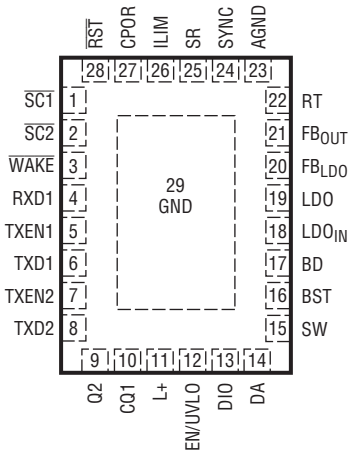


UFD PACKAGE
28-LEAD (4mm × 5mm) PLASTIC QFN

θ_{JA} = 44°C/W, θ_{JC} = 8°C/W
EXPOSED PAD (PIN 29) IS GND, MUST BE SOLDERED TO PCB

LT3669-2

TOP VIEW



UFD PACKAGE
28-LEAD (4mm × 5mm) PLASTIC QFN

θ_{JA} = 44°C/W, θ_{JC} = 8°C/W
EXPOSED PAD (PIN 29) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3669EUFD#PBF	LT3669EUFD#TRPBF	3669	28-Lead (4mm × 5mm) Plastic QFN	–40°C to 125°C
LT3669IUFD#PBF	LT3669IUFD#TRPBF	3669	28-Lead (4mm × 5mm) Plastic QFN	–40°C to 125°C
LT3669HUFD#PBF	LT3669HUFD#TRPBF	3669	28-Lead (4mm × 5mm) Plastic QFN	–40°C to 150°C
LT3669EUFD-2#PBF	LT3669EUFD-2#TRPBF	36692	28-Lead (4mm × 5mm) Plastic QFN	–40°C to 125°C
LT3669IUFD-2#PBF	LT3669IUFD-2#TRPBF	36692	28-Lead (4mm × 5mm) Plastic QFN	–40°C to 125°C
LT3669HUFD-2#PBF	LT3669HUFD-2#TRPBF	36692	28-Lead (4mm × 5mm) Plastic QFN	–40°C to 150°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, V_{L+} = 24V. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supply							
	L+ Undervoltage Lockout Threshold	V_{L+} Rising	●		6.4	7.5	V
V_{OVTH}	L+ Overvoltage Lockout Threshold	V_{L+} Rising	●	40.5	43	45	V
	Shutdown Current from L+	$V_{EN/UVLO}$ = 0.4V			1.15	1.65	mA
	Quiescent Current from L+	Not Switching			4	6	mA
Switching Regulator							
V_{FBOUT}	Switching Regulator Feedback Voltage		●	777	794	811	mV
	FB_{OUT} Pin Bias Current	FB_{OUT} Pin Voltage = 800mV	●		–15	–100	nA
	FB_{OUT} Voltage Line Regulation	7.5V < V_{L+} < 40V			0.005		%/V
	Switching Frequency	R_T = 5.36k R_T = 19.1k R_T = 107k		1.94 0.88 219	2.28 1.04 258	2.62 1.20 297	MHz MHz kHz
	Minimum Switch Off-Time	R_T = 19.1k	●		130	210	ns
	Foldback Frequency	R_T = 19.1k, FB_{OUT} = 0V			115		kHz
	Switch Current Limit (Note 6)	LT3669 LT3669-2	● ●	240 480	325 650	410 820	mA mA
	Switch V_{CESAT} (V_{DIO} – V_{SW})	I_{SW} = –100mA (LT3669) I_{SW} = –300mA (LT3669-2)			330 550		mV mV
	Switch Leakage Current				0.01	2	µA
	Catch Schottky Diode Forward Voltage Drop	I_{SW} = –100mA (LT3669)			720		mV
	Catch Schottky Diode Current Limit to Stop Internal Oscillator	LT3669 LT3669-2		140 330	200 450	260 570	mA mA
	Reverse Protection Diode Forward Voltage Drop	I_{DIO} = –100mA (LT3669) I_{DIO} = –300mA (LT3669-2)			720 840		mV mV
	Reverse Protection Diode Reverse Leakage	V_{L+} = 0V, V_{DIO} = 24V			0.01	2	µA
	Boost Schottky Diode Forward Voltage Drop	I_{BST} = –6mA (LT3669) I_{BST} = –15mA (LT3669-2)			700 750		mV mV
	Boost Schottky Diode Reverse Leakage	V_{BST} – V_{BD} = 24V			0.01	2	µA
	Minimum BST Voltage (Note 7)				1.4	1.8	V

ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	BST Pin Current	I_{SW} = –100mA (LT3669) I_{SW} = –300mA (LT3669-2)			5.25 10.5	7.5 15	mA mA
	SYNC Threshold Voltage			0.5	0.9	1.5	V
	SYNC Input Frequency			0.3		2.2	MHz
	EN/UVLO Threshold Voltage	$V_{EN/UVLO}$ Rising	●	1.44	1.5	1.56	V
	EN/UVLO Pin Hysteresis		●	50	75	100	mV
LDO Linear Regulator							
V_{FBLDO}	LDO Feedback Voltage		●	777	794	811	mV
	FB_{LDO} Pin Bias Current	FB_{LDO} Pin Voltage = 800mV	●		–20	–100	nA
	FB_{LDO} Voltage Line Regulation	7.5V < V_{L+} < 40V, V_{L+} – V_{LDO} > 4V			0.005		%/V
	LDO Current Limit		●	151	180	235	mA
	LDO Current Limit Foldback	V_{LDOIN} = 40V, V_{LDO} = 0V	●	15	35	55	mA
	LDO Dropout Voltage	LDO Load Current = 25mA LDO Load Current = 150mA	●		60 340	90	mV mV
	LDO Minimum Load Current		●		150	175	µA
Power-On Reset							
V_{RSTTH}	Reset Threshold as % of V_{FBOUT} (V_{FBLDO})	FB_{OUT} (FB_{LDO}) Pin Voltage Falling (Figure 6)	●	90.4	92.7	95	%
t_{RST}	Reset Timeout Period	C_{POR} = 100nF, $\overline{RST}$ R_{PU} = 100k (Figure 6)	●	10	12.5	15	ms
t_{UV}	UV Detect to $\overline{RST}$ Asserted	Step V_{FBOUT} (V_{FBLDO}) from 0.9V to 0.5V, $\overline{RST}$ R_{PU} = 100k (Figure 6)	●	11	24	37	µs
Line Driver Thermal Shutdown							
	Thermal Shutdown Threshold (Note 8)	Junction Temperature T_J Increasing		125	140	155	°C
	Thermal Shutdown Threshold (Note 8)	Junction Temperature T_J Decreasing		111	128	135	°C
	Thermal Shutdown Hysteresis (Note 8)			10	12	14	°C
Line Drivers							
I_{QH}	DC Driver Current P-Switching Output (ON State)	V_{ILIM} ≤ 0.3V, 7.5V < V_{L+} < 40V R_{ILIM} = 42.2k, 7.5V < V_{L+} < 40V	● ●	105 280	140 330	190 420	mA mA
I_{QL}	DC Driver Current N-Switching Output (ON State)	V_{ILIM} ≤ 0.3V, 7.5V < V_{L+} < 40V R_{ILIM} = 42.2k, 7.5V < V_{L+} < 40V	● ●	105 280	140 330	190 420	mA mA
V_{RQH}	Residual Voltage High (V_{L+} to $V_{CQ1,Q2}$)	$I_{CQ1,Q2}$ = –100mA $I_{CQ1,Q2}$ = –250mA	● ●		1.15 1.5	1.65 2.1	V V
V_{RQL}	Residual Voltage Low ($V_{CQ1,Q2}$)	$I_{CQ1,Q2}$ = 100mA $I_{CQ1,Q2}$ = 250mA	● ●		1.15 1.5	1.65 2.1	V V
	V_{RQH} (V_{RQL}) Pulsing Threshold	V_{RQH} (V_{RQL}) Increasing		2.7	2.95	3.2	V
	V_{RQH} (V_{RQL}) Pulsing Threshold Hysteresis			20	50	80	mV
	CQ1, Q2 Pin Leakage Current	–40°C to 125°C, V_{TXENn} < 0.4V –40°C to 150°C, V_{TXENn} < 0.4V	● ●		±1.2 ±1.2	±3 ±8	µA µA
Receiver							
V_{THH}	Input Threshold “H”	V_{L+} > 18V (Figure 14)	●	10.5	11.8	13	V
V_{THL}	Input Threshold “L”	V_{L+} > 18V (Figure 14)	●	8.0	9.6	11.2	V
V_{HYS}	Input Hysteresis	V_{L+} > 18V (Figure 14)	●	1.8	2.2	2.6	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, V_{L+} = 24V. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Digital IO							
	$\overline{WAKE}$, RXD1, $\overline{SCn}$ Pull-Down Output Current if Asserted	$V_{\overline{SCn}} = V_{\overline{WAKE}} = V_{RXD1}$ = 0.3V	●	0.7	1.05		mA
	$\overline{RST}$ Pull-Down Output Current if Asserted	$V_{\overline{RST}}$ = 0.3V	●	0.2	0.3		mA
V_{IH}	TXDn, TXENn, SR Input High Voltage		●	0.9			V
V_{IL}	TXDn, TXENn, SR Input Low Voltage		●			0.4	V
I_{LK}	TXDn, TXENn, SR Pin Input Leakage Current				0.1	1	µA
C_{IN}	TXDn, TXENn, SR Pin Input Capacitance				2.5		pF

SWITCHING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, V_{L+} = 24V. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Driver and Receiver							
f_{DTR}	Maximum Data Transfer Rate	$C_{CQ1,Q2} \le$ 4nF $V_{SR} \le$ 0.4V (for COM1/COM2) $V_{SR} \ge$ 0.9V (for COM3)	 ● ●	 38.4 230.4			 kb/s kb/s
t_{BIT}	Bit Time	$V_{SR} \le$ 0.4V (for COM2) $V_{SR} \ge$ 0.9V (for COM3)			26.04 4.34		µs µs
Driver							
t_{DR}	Rise Time	$C_{CQ1,Q2} \le$ 4nF (Figure 1) $V_{SR} \le$ 0.4V (for COM1/COM2) $V_{SR} \ge$ 0.9V (for COM3)	 ● ●		 1.6 0.26	 5.2 0.869	 µs µs
t_{DF}	Fall Time	$C_{CQ1,Q2} \le$ 4nF (Figure 1) $V_{SR} \le$ 0.4V (for COM1/COM2) $V_{SR} \ge$ 0.9V (for COM3)	 ● ●		 2.1 0.34	 5.2 0.869	 µs µs
t_{PHLD}, t_{PLHD}	Propagation Delay	$C_{CQ1,Q2} \le$ 4nF (Figure 2) $V_{SR} \le$ 0.4V (for COM1/COM2) $V_{SR} \ge$ 0.9V (for COM3)	 ● ●		 3.3 0.72	 6 1.3	 µs µs
t_{SKEWD}	Skew	$t_{SKEWD} = \lvert t_{PHLD} - t_{PLHD} \rvert$, $C_{CQ1,Q2} \le$ 4nF (Figure 2) $V_{SR} \le$ 0.4V (for COM1/COM2) $V_{SR} \ge$ 0.9V (for COM3)	 ● ●		 0.25 140	 1.5 400	 µs ns
t_{ZHD}, t_{ZLD}	Enable Time	$C_{CQ1,Q2}$ = 100pF, $R_{PU} = R_{PD}$ = 10k (Figure 3) $V_{SR} \le$ 0.4V (for COM1/COM2) $V_{SR} \ge$ 0.9V (for COM3)	 ● ●		 3.4 0.8	 6.1 1.4	 µs µs
t_{HZD}, t_{LZD}	Disable Time	$C_{CQ1,Q2}$ = 100pF, $R_{PU} = R_{PD}$ = 10k (Figure 3) $V_{SR} \le$ 0.4V (for COM1/COM2) $V_{SR} \ge$ 0.9V (for COM3)	 ● ●		 4 4	 6 6	 µs µs
t_{DWU}	Minimum Wake-Up Pulse Duration to Be Acknowledged	$R_{PU} = R_{PD}$ = 10k (Figure 7) $\overline{WAKE}$ Pull-Up Resistor = 5k	●		55	75	µs
t_{LZW}	Delay From Handshake Sequence Finished to $\overline{WAKE}$ High (Note 9)	$\overline{WAKE}$ Pull-Up Resistor = 5k			0.3	1	µs
	Pulsing On-Time	V_{RQH} (V_{RQL}) = 24V, Only CQ1 or Q2 Pulsing			320		µs
	Pulsing Off-Time				2.2		ms

SWITCHING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, V_{L+} = 24V. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Receiver							
	Noise Suppression Time	$V_{SR} \le 0.4V$ (for COM1/COM2) (Figure 5) $V_{SR} \ge 0.9V$ (for COM3) (Figure 5)	● ●	1/16 1/16		3.5/16 5/16	T_{BIT} T_{BIT}
t_{PHLR}, t_{PLHR}	Propagation Delay	RXD1 Pull-Up Resistor = 5k (Figure 4) $V_{SR} \le 0.4V$ (for COM1/COM2) $V_{SR} \ge 0.9V$ (for COM3)	 ● ●		 4.6 1.45	 6.5 2.1	 µs µs
t_{SKEWR}	Receiver Skew	$t_{SKEWR} = \lvert t_{PHLR} - t_{PLHR} \rvert$, RXD1 R_{PU} = 5k (Figure 4) $V_{SR} \le 0.4V$ (for COM1/COM2) $V_{SR} \ge 0.9V$ (for COM3)	 ● ●		 0.5 100	 1.5 400	 µs ns
C_{CQI}	CQ1 Pin Input Capacitance				20		pF

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltages are with respect to GND. All currents into device pins are positive; all currents out of device pins are negative.

Note 3: Absolute maximum voltage at L+, EN/UVLO, DIO and LDO_{IN} pins is 60V for non-repetitive one second transients, and 40V for continuous operation.

Note 4: The LT3669E is guaranteed to meet performance specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT3669I is guaranteed over the full –40°C to 125°C operating junction temperature range. The LT3669H is guaranteed over the full –40°C to 150°C operating junction temperature range. Specifications for the line driver do not apply above the thermal shutdown temperature.

Note 5: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions and will shut the line drivers off for typical junction temperatures higher than 140°C. The LDO and switching regulator will shut off for typical junction temperatures higher than 168°C. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 6: Current limit guaranteed by design and/or correlation to static test. Slope compensation reduces current limit at higher duty cycles.

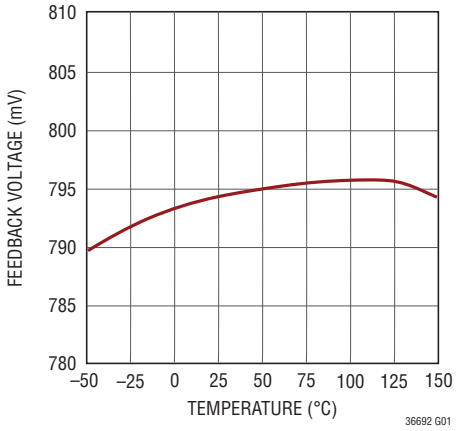
Note 7: This is the minimum voltage across the boost capacitor needed to guarantee full saturation of the NPN power switch.

Note 8: Thermal shutdown guaranteed by design and/or correlation to static test.

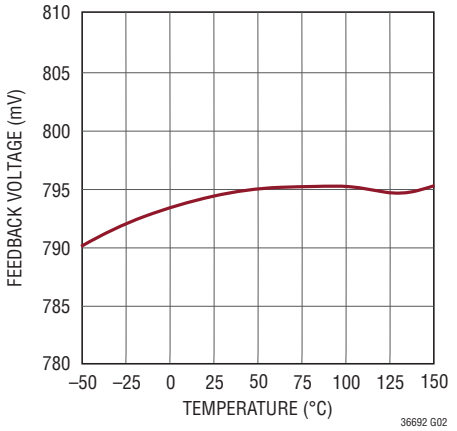
Note 9: Handshake sequence: set TXEN1 low and then toggle TXD1.

TYPICAL PERFORMANCE CHARACTERISTICS

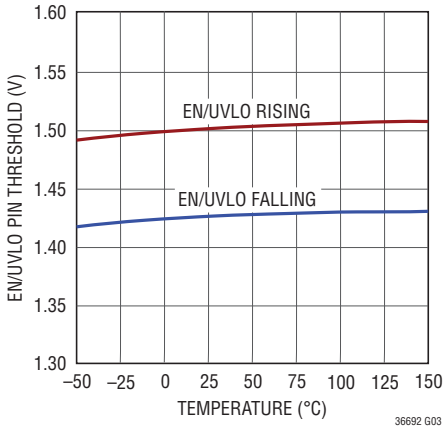
FB_{OUT} Feedback Voltage



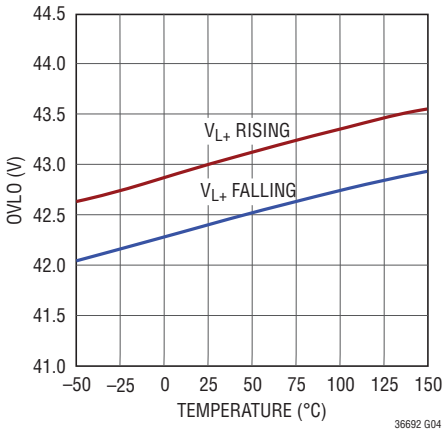
FB_{LDO} Feedback Voltage



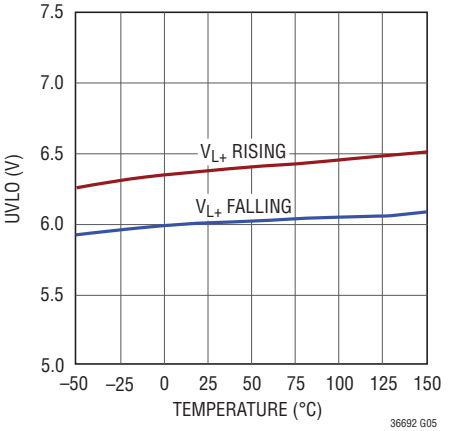
EN/UVLO Pin Threshold



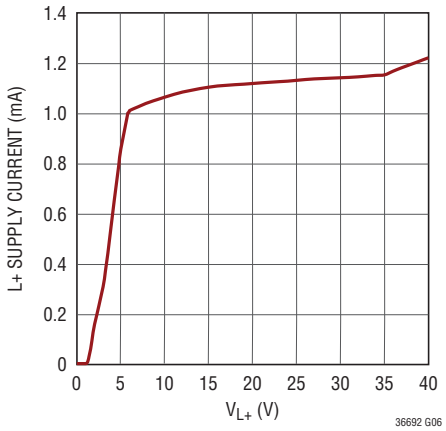
L+ Overvoltage Lockout



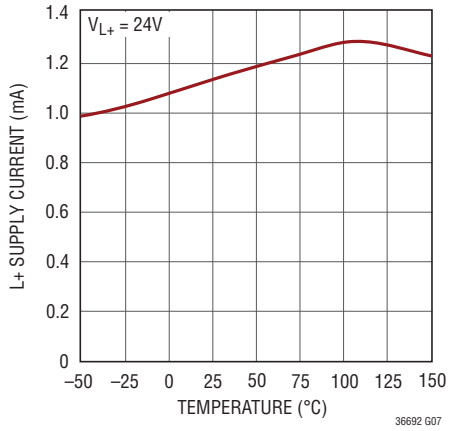
L+ Undervoltage Lockout



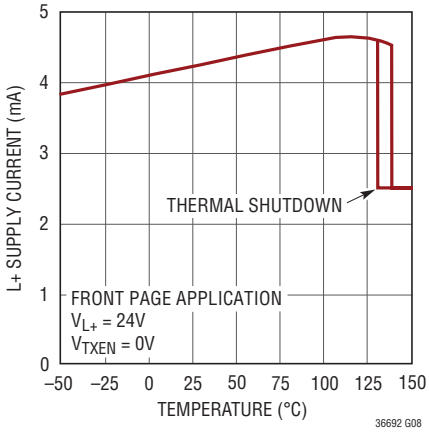
L+ Supply Current, $V_{EN/UVLO}$ < 0.4V



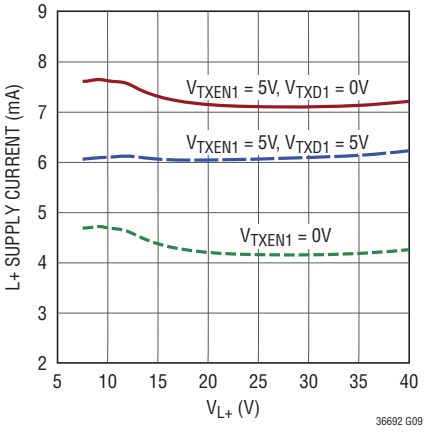
L+ Supply Current, $V_{EN/UVLO}$ < 0.4V



No-Load L+ Supply Current, $V_{EN/UVLO} = V_{L+}$

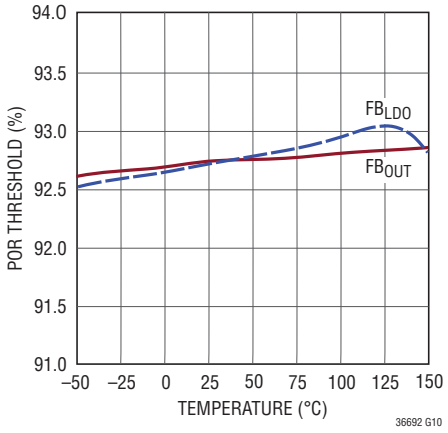


No-Load L+ Supply Current, $V_{EN/UVLO} = V_{L+}$, V_{TXEN2} = 0V

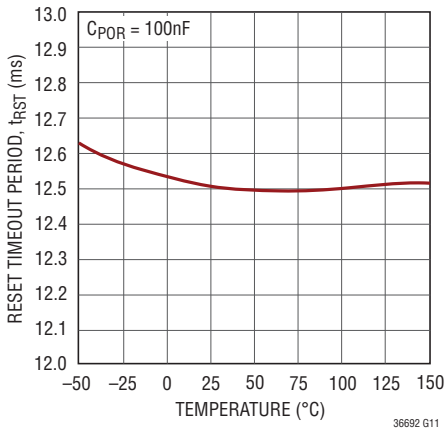


TYPICAL PERFORMANCE CHARACTERISTICS

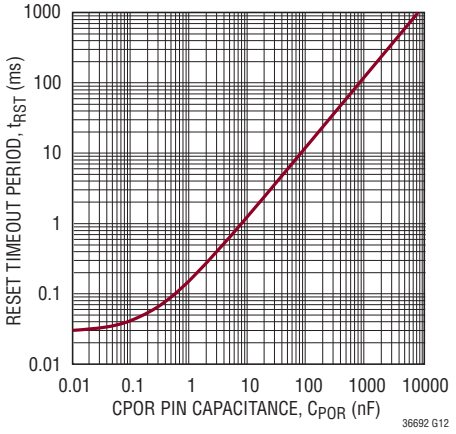
Power-On Reset Threshold



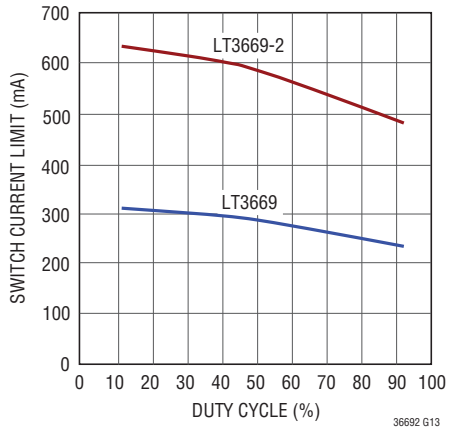
Reset Timeout Period



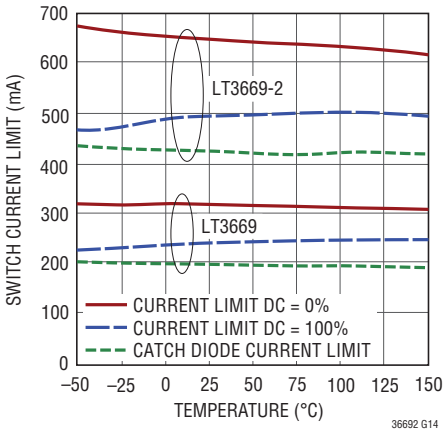
Reset Timeout Period



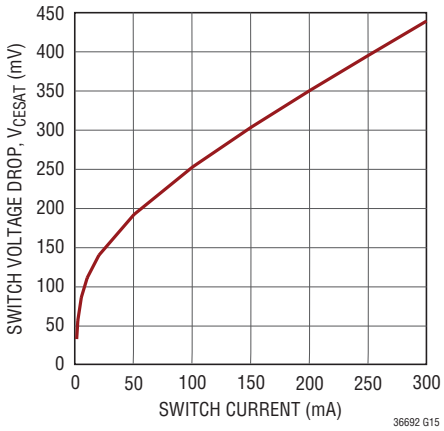
Switch Current Limit



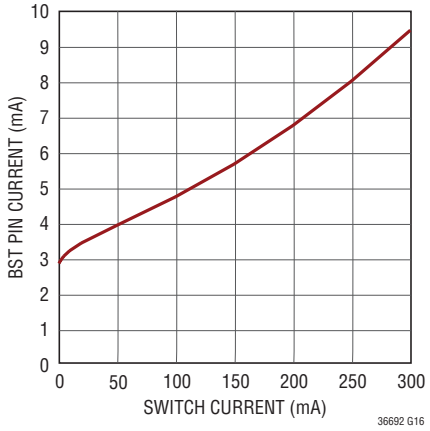
Switch Current Limits



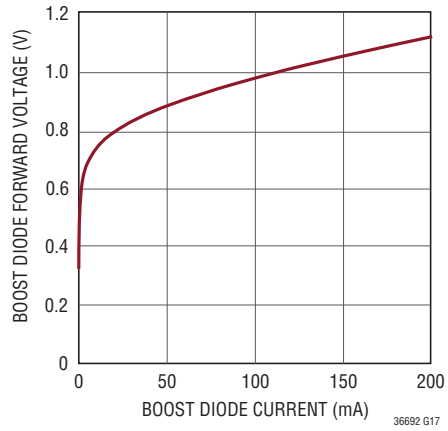
Switch Voltage Drop



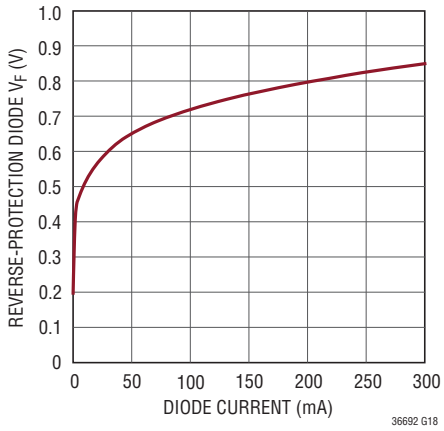
BST Pin Current



Boost Diode Forward Voltage

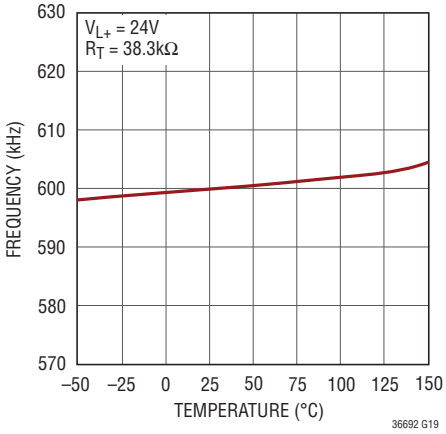


Reverse-Protection Diode Forward Voltage

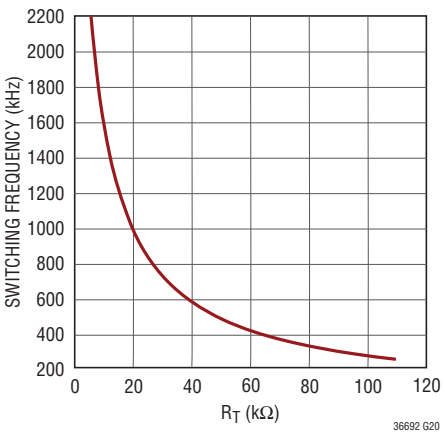


TYPICAL PERFORMANCE CHARACTERISTICS

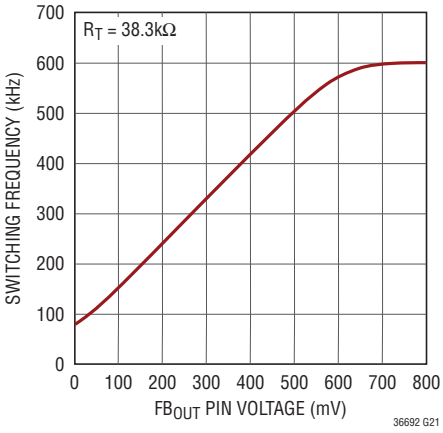
Switching Frequency



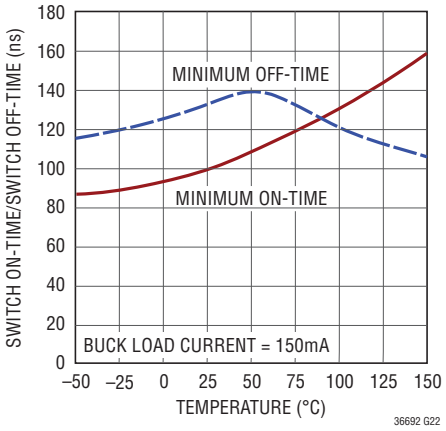
Switching Frequency



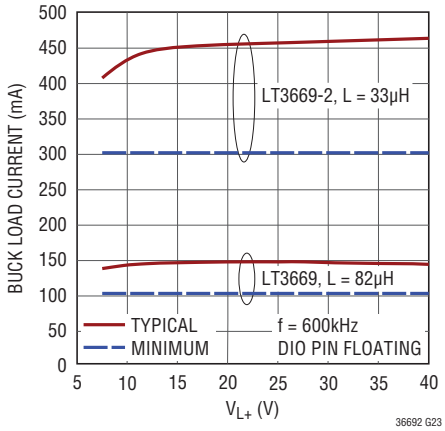
Frequency Foldback



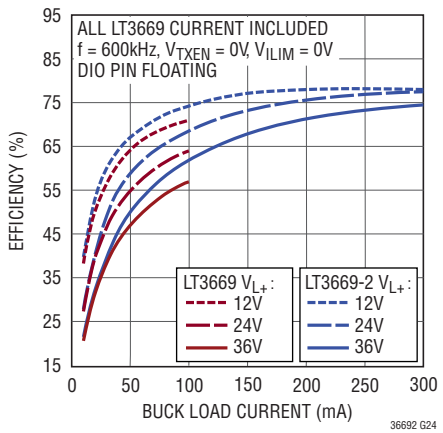
Minimum Switch-On Time/ Switch Off-Time



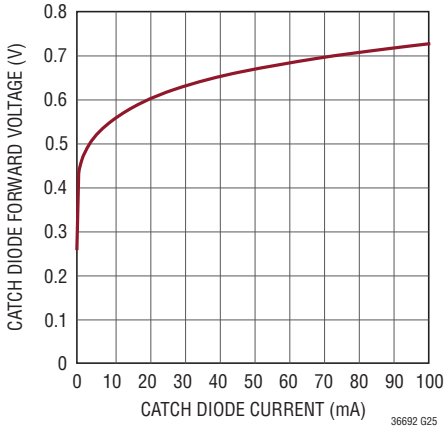
Maximum Buck Output Current, V_{OUT} = 5V



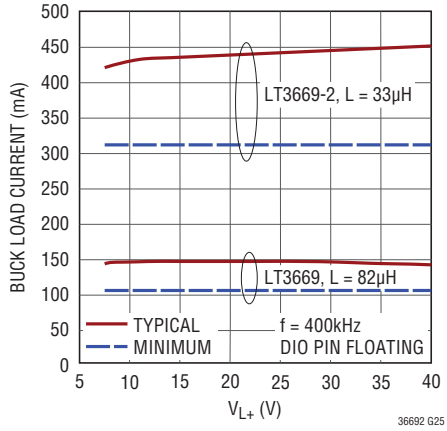
Efficiency, V_{OUT} = 5V



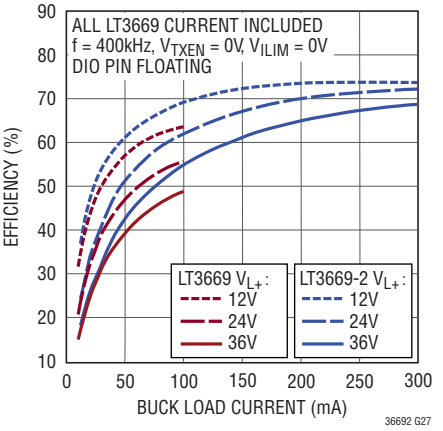
Catch Diode Forward Voltage (LT3669 Only)



Maximum Buck Output Current, V_{OUT} = 3.3V

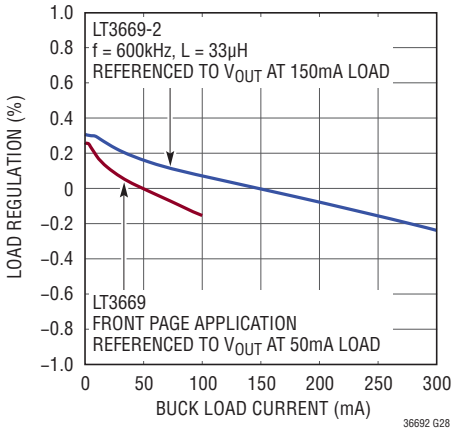


Efficiency, V_{OUT} = 3.3V

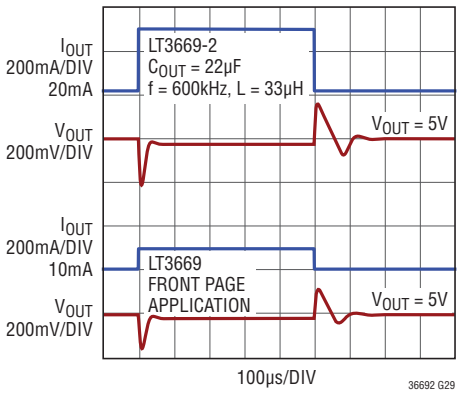


TYPICAL PERFORMANCE CHARACTERISTICS

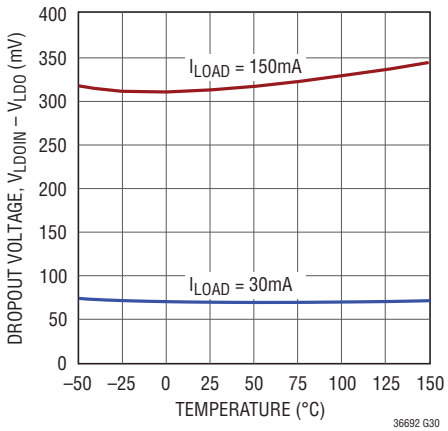
Buck Load Regulation



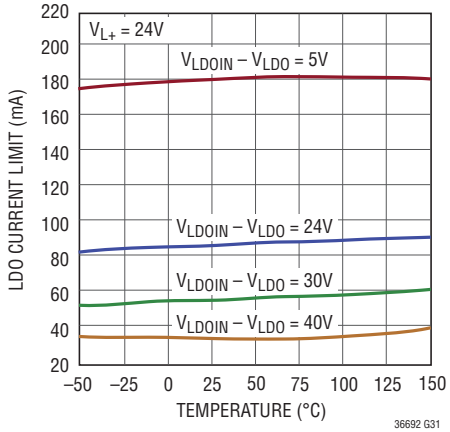
Buck Load Transient Response



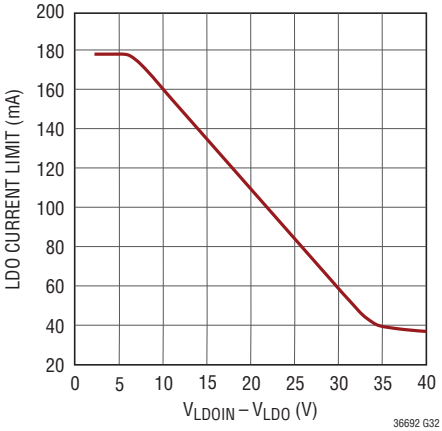
LDO Dropout Voltage



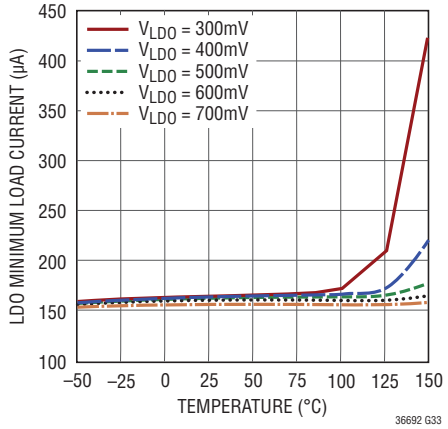
LDO Current Limit



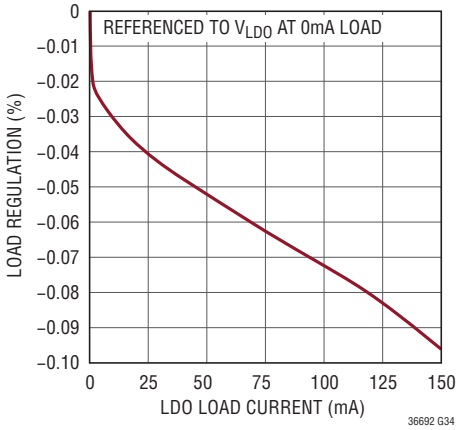
LDO Current Limit Foldback



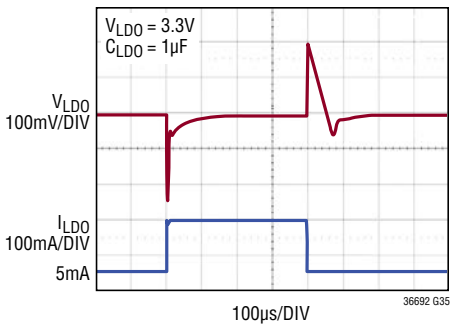
LDO Minimum Load Current



LDO Load Regulation

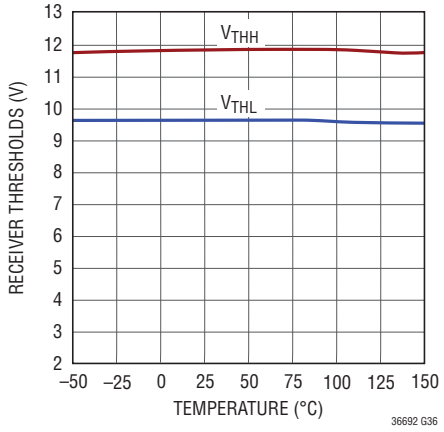


LDO Load Transient Response

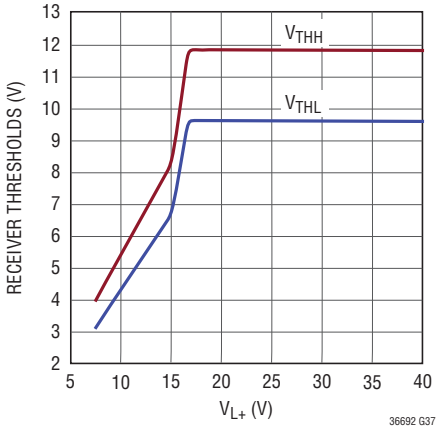


TYPICAL PERFORMANCE CHARACTERISTICS

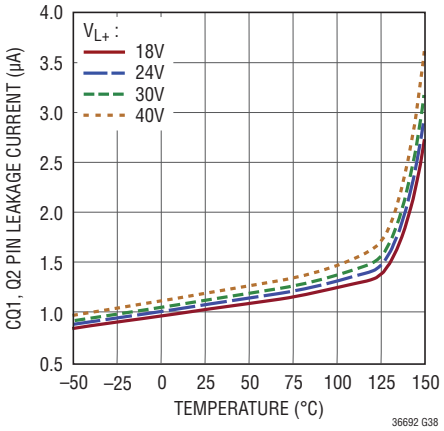
Receiver Thresholds



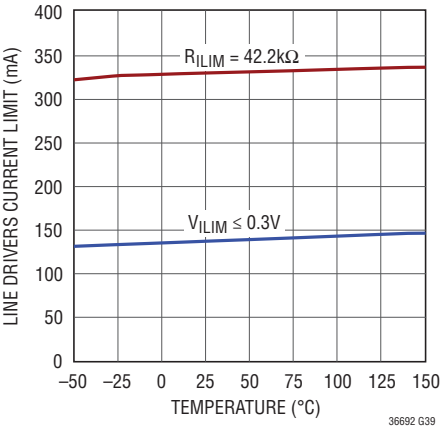
Receiver Thresholds



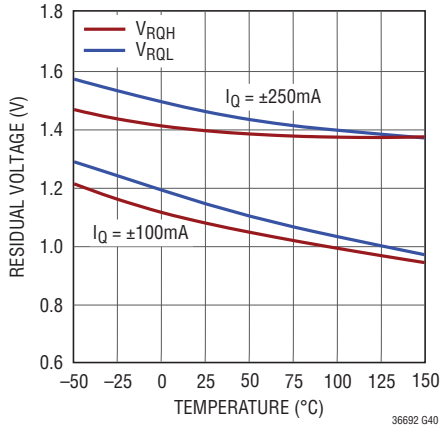
CQ1, Q2 Pin Leakage Current V_{TXEN} < 0.4V



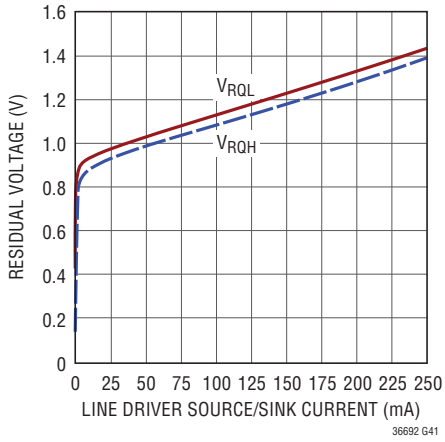
Line Driver Current Limit



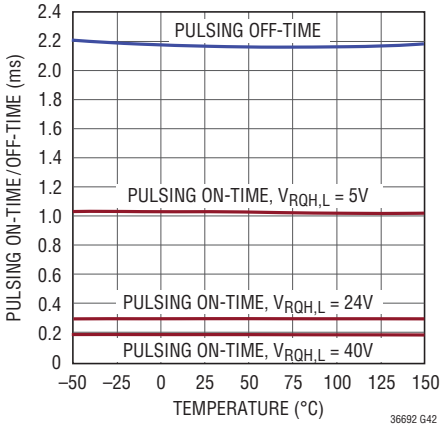
Line Driver Residual Voltage



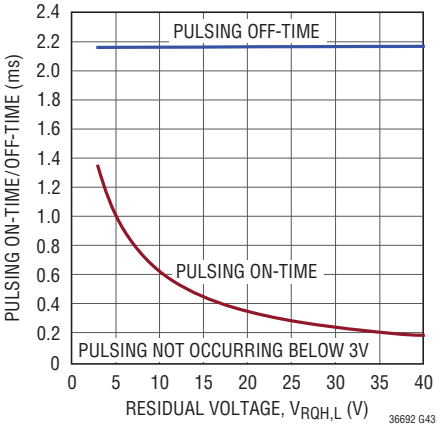
Line Driver Residual Voltage



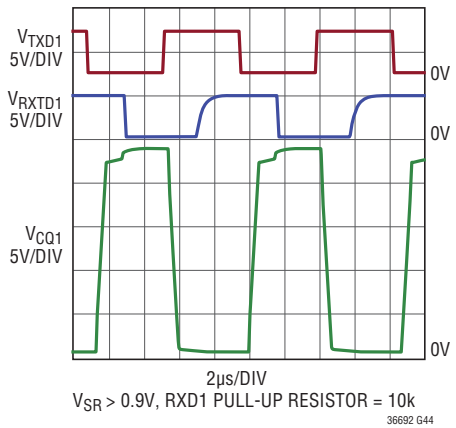
Line Driver Pulsing On-Time/ Off-Time



Line Driver Pulsing On-Time/ Off-Time



Line Driver Output Waveforms



PIN FUNCTIONS

$\overline{SC1}$ (Pin 1): CQ1 Short-Circuit Detect Open-Collector Output. $\overline{SC1}$ pulls low when a short-circuit is detected on the CQ1 driver output or after a thermal shutdown event. Use a 100k pull-up resistor to the µC's supply. Lowpass filter this signal before further processing. See the Applications Information section.

$\overline{SC2}$ (Pin 2): Q2 Short-Circuit Detect Open-Collector Output. $\overline{SC2}$ pulls low when a short-circuit is detected on the Q2 driver output or after a thermal shutdown event. Use a 100k pull-up resistor to the µC's supply. Lowpass filter this signal before further processing. See the Applications Information section.

$\overline{WAKE}$ (Pin 3): Wake-up Detect Open-Collector Output. $\overline{WAKE}$ pulls low when driver 1 detects a wake-up pulse longer than 75µs at the CQ1 pin (indicating that a data transmission is beginning). $\overline{WAKE}$ returns to high impedance after the handshaking sequence of setting TXEN1 low and then toggling TXD1 or after an internal reset event. Use a 10k pull-up resistor to the µC's supply.

RXD1 (Pin 4): CQ1 Receiver Output, Open Collector. Use a pull-up resistor of 10k or less for improved data performance in COM3. RXD1 polarity is inverted with respect to the line data CQ1.

TXEN1 (Pin 5): CQ1 Driver Enable. The TXEN1 pin enables the line data CQ1 driver in push-pull mode when pulled high. To use the driver in open-collector mode, tie TXD1 high (for pull-down mode) or low (for pull-up mode) and drive the data signal into the TXEN1 pin.

TXD1 (Pin 6): CQ1 Driver Input. The polarity of the driver output is inverted with respect to TXD1.

TXEN2 (Pin 7): Q2 Driver Enable. The TXEN2 pin enables the line data Q2 driver in push-pull mode when pulled high. To use the driver in open-collector mode, tie TXD2 high (for pull-down mode) or low (for pull-up mode) and drive the data signal into the TXEN2 pin.

TXD2 (Pin 8): Q2 Driver Input. The polarity of the driver output is inverted with respect to TXD2.

Q2 (Pin 9): Q2 Driver Output. The driver output polarity is inverted with respect to the driver input TXD2. Connect a capacitor (typically 470pF) from Q2 to ground for improved performance.

CQ1 (Pin 10): CQ1 Driver Output and Receiver Input. The driver output polarity is inverted with respect to the driver input TXD1. Tie directly to the industrial line data terminal. Connect a capacitor (typically 470pF) from CQ1 to ground for improved performance.

L+ (Pin 11): Power Supply Input and Anode of Internal Reverse Polarity Protection Diode. Connect to the industrial line supply terminal. The L+ pin supplies current to the LT3669's internal circuitry and must be locally bypassed with at least 4.7µF.

EN/UVLO (Pin 12): The EN/UVLO pin puts the LT3669 in shutdown mode. Pull the pin below 0.4V to shut down the LT3669. The 1.5V threshold functions as an accurate undervoltage lockout (UVLO), preventing the regulators and transceiver from operating until the input voltage has reached the programmed level.

DIO (Pin 13): Cathode of Internal Reverse Polarity Protection Diode. Do not use a bypass capacitor at DIO. An external diode from L+ to DIO can be used to improve efficiency. In this case only, a bypass capacitor is allowed at DIO. The external diode must be chosen with a reverse-breakdown voltage higher than the expected reverse-polarity condition, and it must be robust enough to withstand the inrush current of hot plugging.

GND (Pin 14, LT3669): Ground in LT3669. Leave this pin floating or tie the pin directly to the ground plane and the industrial line ground terminal L–.

DA (Pin 14, LT3669-2): Diode Anode in LT3669-2. Connect the anode of the external catch diode (D1 in LT3669-2's Block Diagram) to this pin. Internal circuitry senses the current through the catch diode providing frequency foldback in extreme situations.

SW (Pin 15): Output of the Internal NPN Power Switch. Connect this pin to the inductor and boost capacitor.

BST (Pin 16): The BST pin provides drive voltage higher than the input voltage to the internal NPN power switch. Connect a capacitor (typically 0.22µF) between BST and SW.

BD (Pin 17): An integrated Schottky diode is connected from BD to BST, providing the charging path for the boost capacitor. Connect to the output of the switching regulator.

PIN FUNCTIONS

LDO_{IN} (Pin 18): LDO Power Supply Input. This is the collector of the LDO power NPN. Tie to the output of the switching regulator for maximum efficiency, or to DIO. To preserve reverse-polarity protection, do not connect to L+.

LDO (Pin 19): Low Dropout Linear Regulator Output. Bypass to GND with at least 1µF of capacitance.

FB_{LDO} (Pin 20): The LT3669 regulates this pin to 0.794V. Connect a feedback resistor divider tap to this pin to set the output voltage of the LDO.

FB_{OUT} (Pin 21): The LT3669 regulates this pin to 0.794V. Connect a feedback resistor divider tap to this pin to set the output voltage of the switching regulator.

RT (Pin 22): Sets the Internal Oscillator Frequency. Tie a resistor from RT to AGND to program the frequency. See Table 2 for resistor values.

AGND (Pin 23): Analog Ground Used for Bandgap Voltage References. Connect to the ground node of the passive components connected to RT, FB_{OUT}, FB_{LDO}, ILIM and CPOR, and to the system ground in a star connection manner.

SYNC (Pin 24): External Clock Synchronization Input. Ground this pin to run the part using the internal oscillator. For external synchronization, drive the SYNC pin with a logic-level signal with positive and negative pulse widths of at least 80ns. Choose the RT resistor to set the LT3669 switching frequency at least 20% below the lowest synchronization input. For example, if the synchronization signal is 350kHz, the RT pin should be set for 280kHz.

SR (Pin 25): Slew Rate Control Pin. Setting SR low adjusts both CQ1 and Q2 drivers' rising and falling times for reduced EMI in COM1/COM2 speed mode. Set SR high for edge times suitable for COM3.

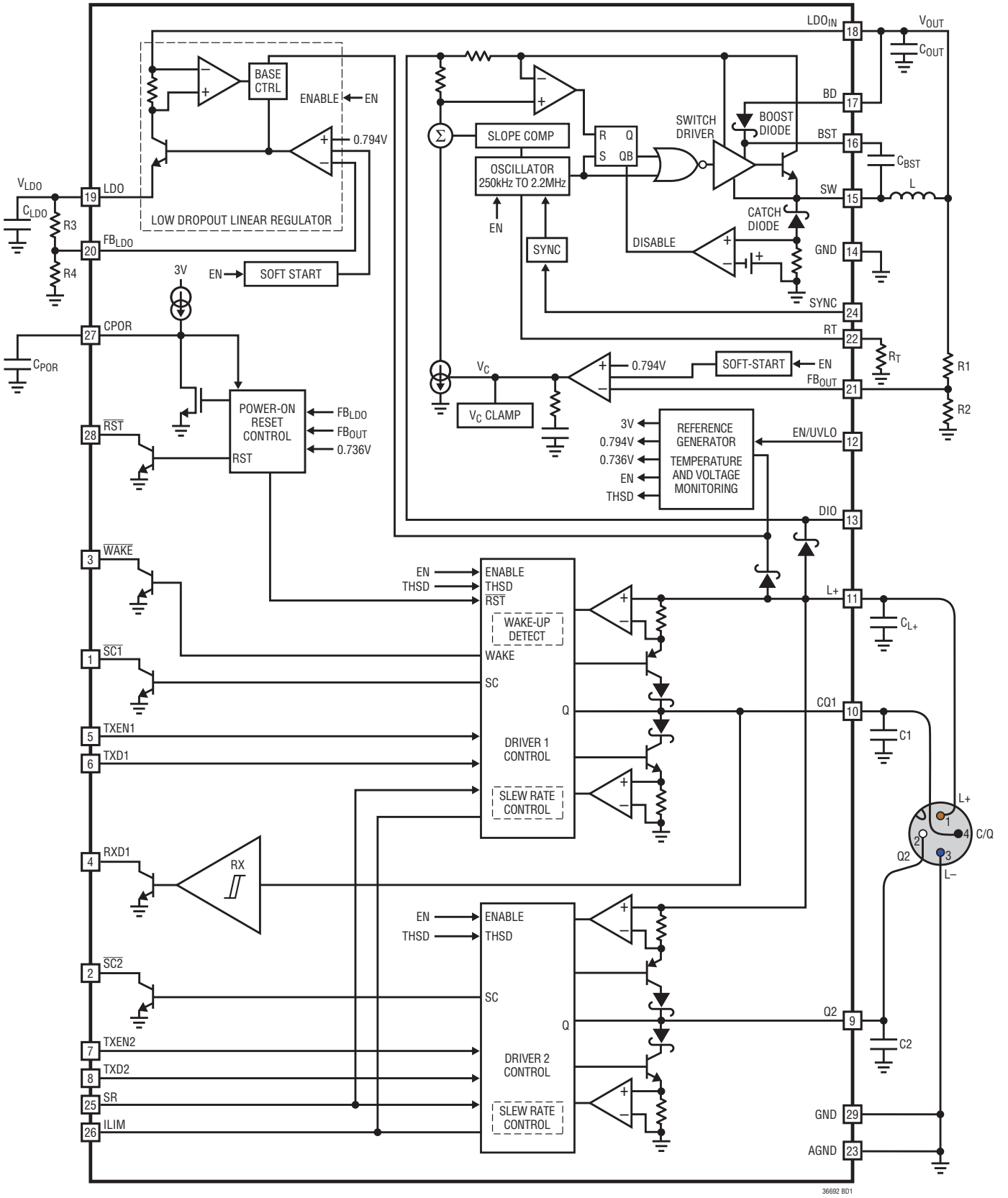
ILIM (Pin 26): Line Driver Current Limit Programming Pin. Source and sink current limits for both line drivers are programmed using this pin. Tie a resistor from ILIM to AGND to set the drivers output current limit. Tie ILIM to AGND for a 140mA current limit.

CPOR (Pin 27): Reset Delay Timer Programming Pin. Connect an external capacitor (C_{POR}) to AGND to program a reset delay time of 0.125ms/nF.

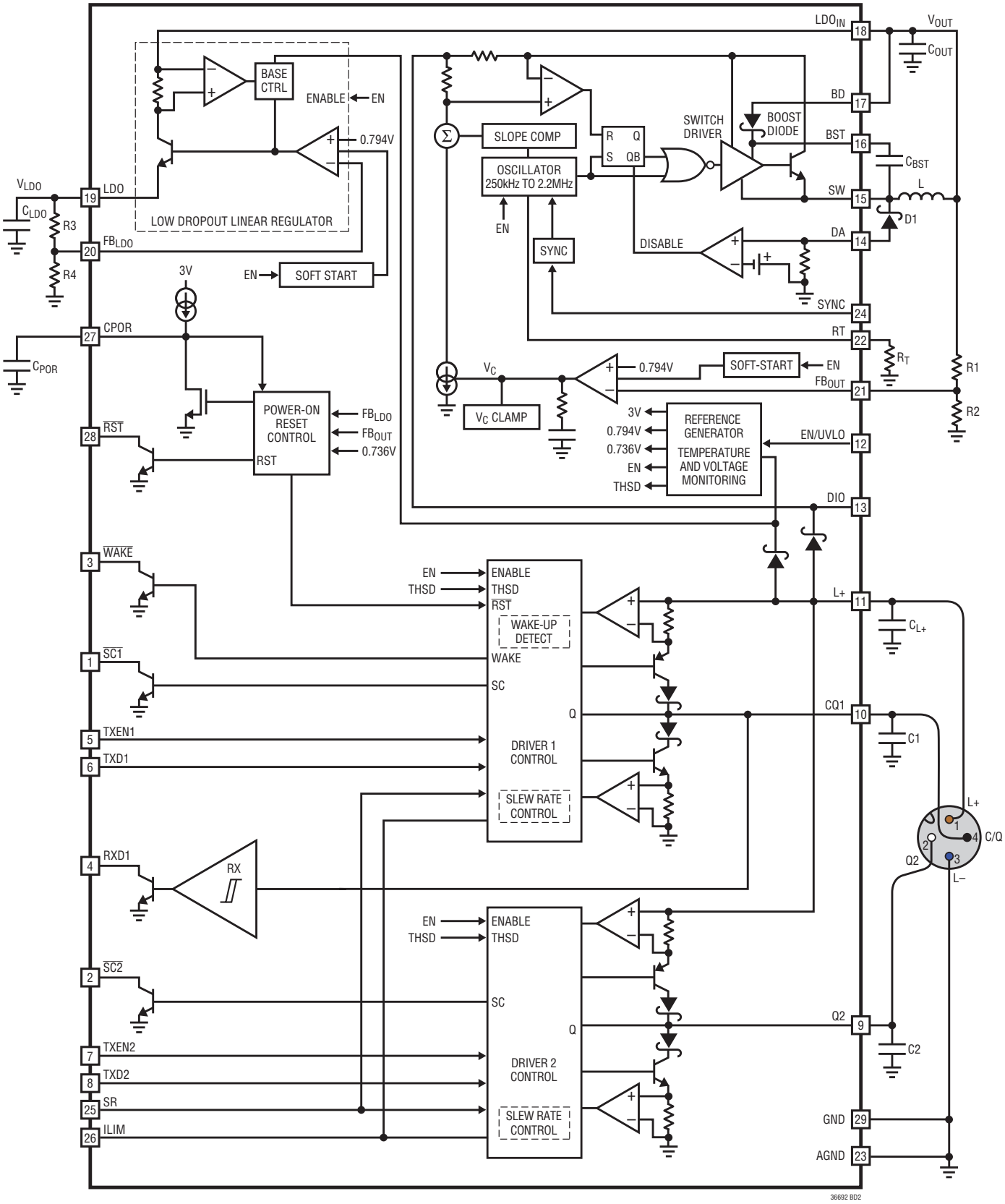
$\overline{RST}$ (Pin 28): Active Low, Open-collector Logic Output. After V_{OUT} and V_{LDO} rises above 92.7% of its programmed value, the reset remains asserted for the period set by the capacitor on the CPOR pin. $\overline{RST}$ will also pull low if V_{L+} is below the internal undervoltage threshold and V_{OUT} or V_{LDO} are above 1.5V for an $\overline{RST}$ pull-up resistor of 100k. If using the POR function, connect a 10pF capacitor between the CPOR and $\overline{RST}$ pins.

GND (Pin 29 Exposed Pad): Ground. Tie the exposed pad directly to the ground plane and the industrial line ground terminal. The exposed pad metal of the package provides both electrical contact to ground and good thermal contact to the circuit printed board. It must be soldered to the circuit board for proper operation.

BLOCK DIAGRAM LT3669



BLOCK DIAGRAM LT3669-2



TIMING DIAGRAMS

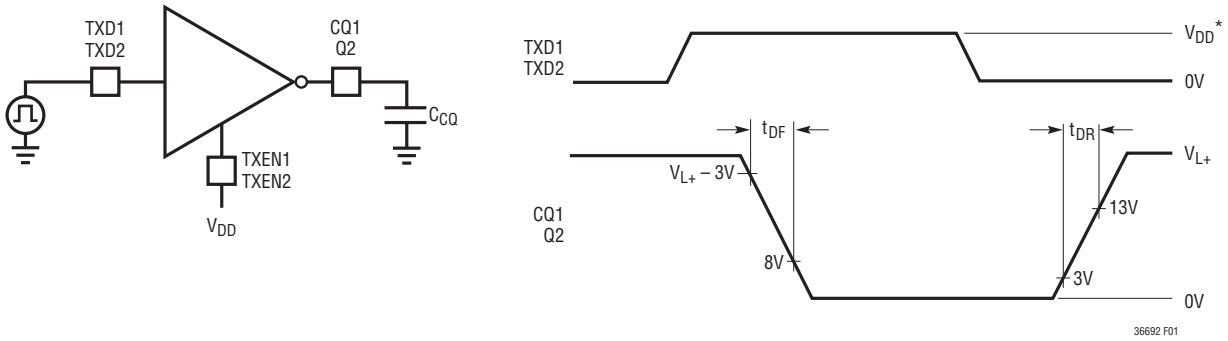


Figure 1. Driver Rising and Falling Times

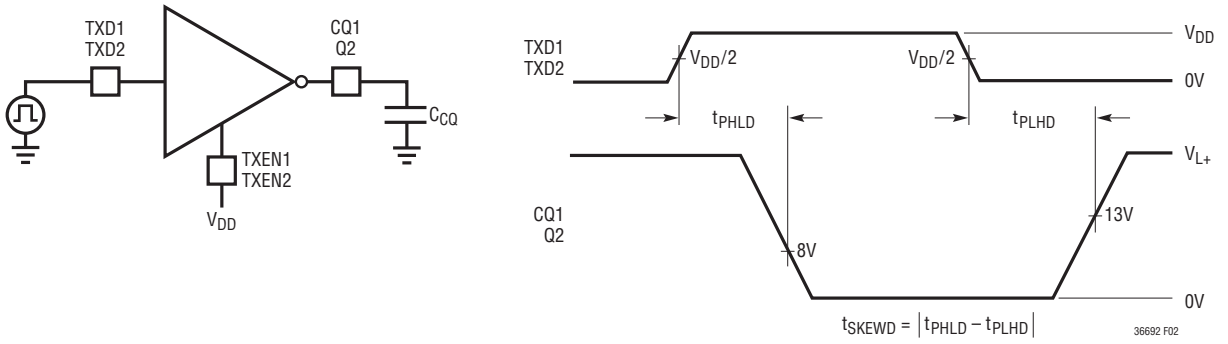


Figure 2. Driver Propagation Delays

* V_{DD} is the external µC's supply voltage which can be taken either from the switching regulator's or LDO's output (V_{OUT} or V_{LDO})

TIMING DIAGRAMS

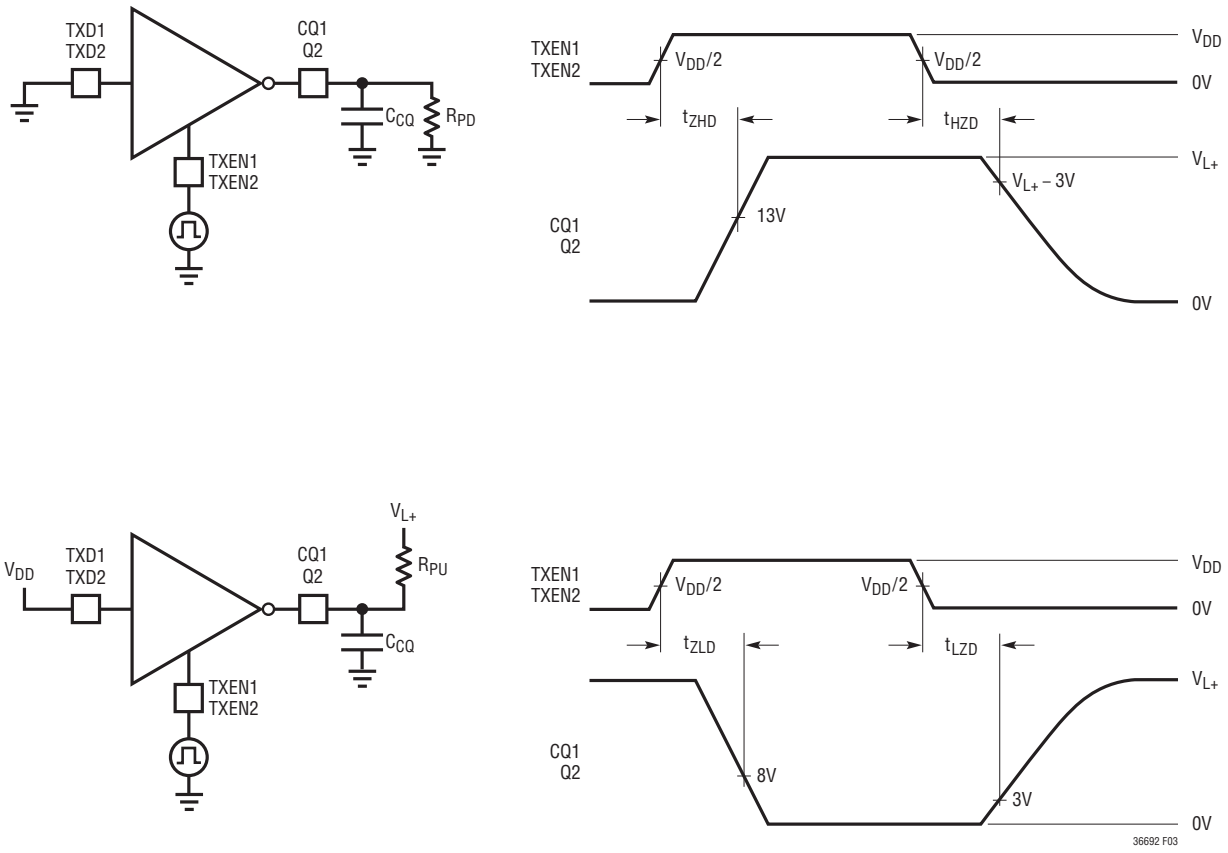


Figure 3. Driver Enable and Disable Times

TIMING DIAGRAMS

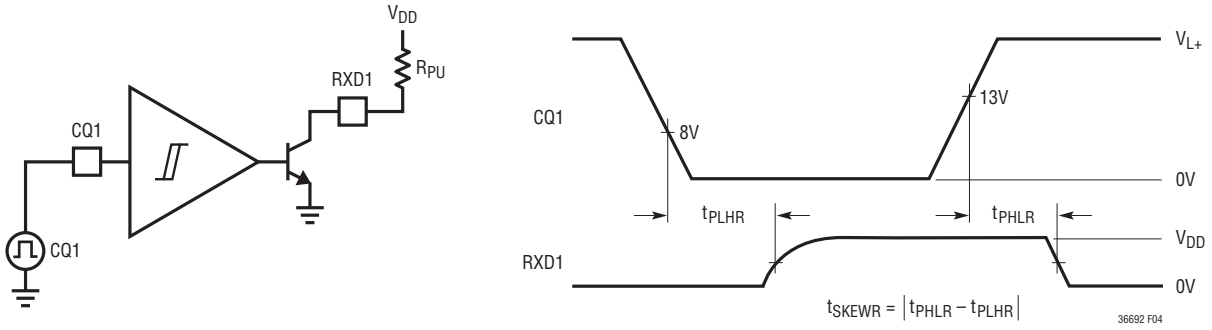


Figure 4. Receiver Propagation Delays

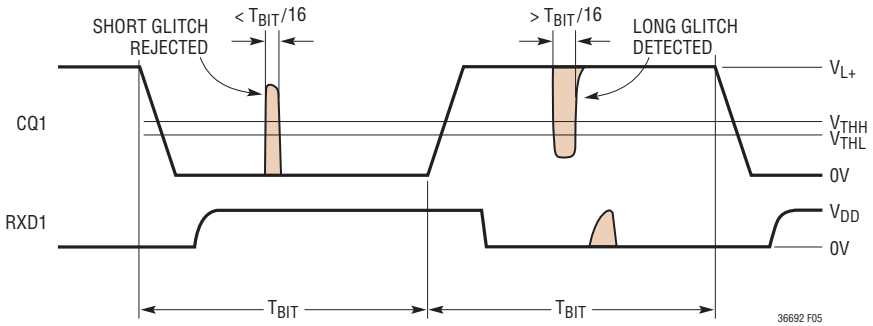


Figure 5. Receiver Detection and Noise Filter

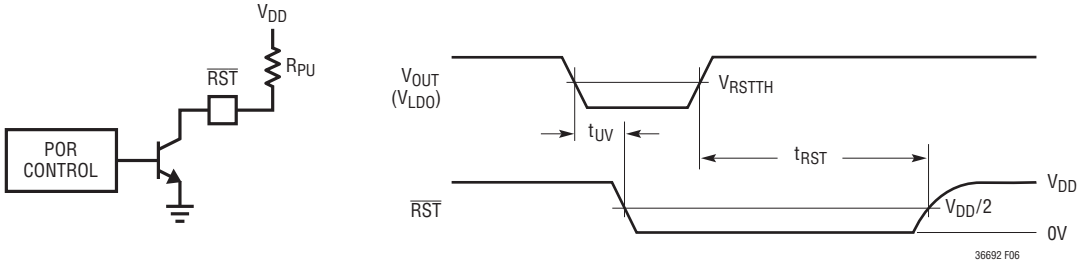
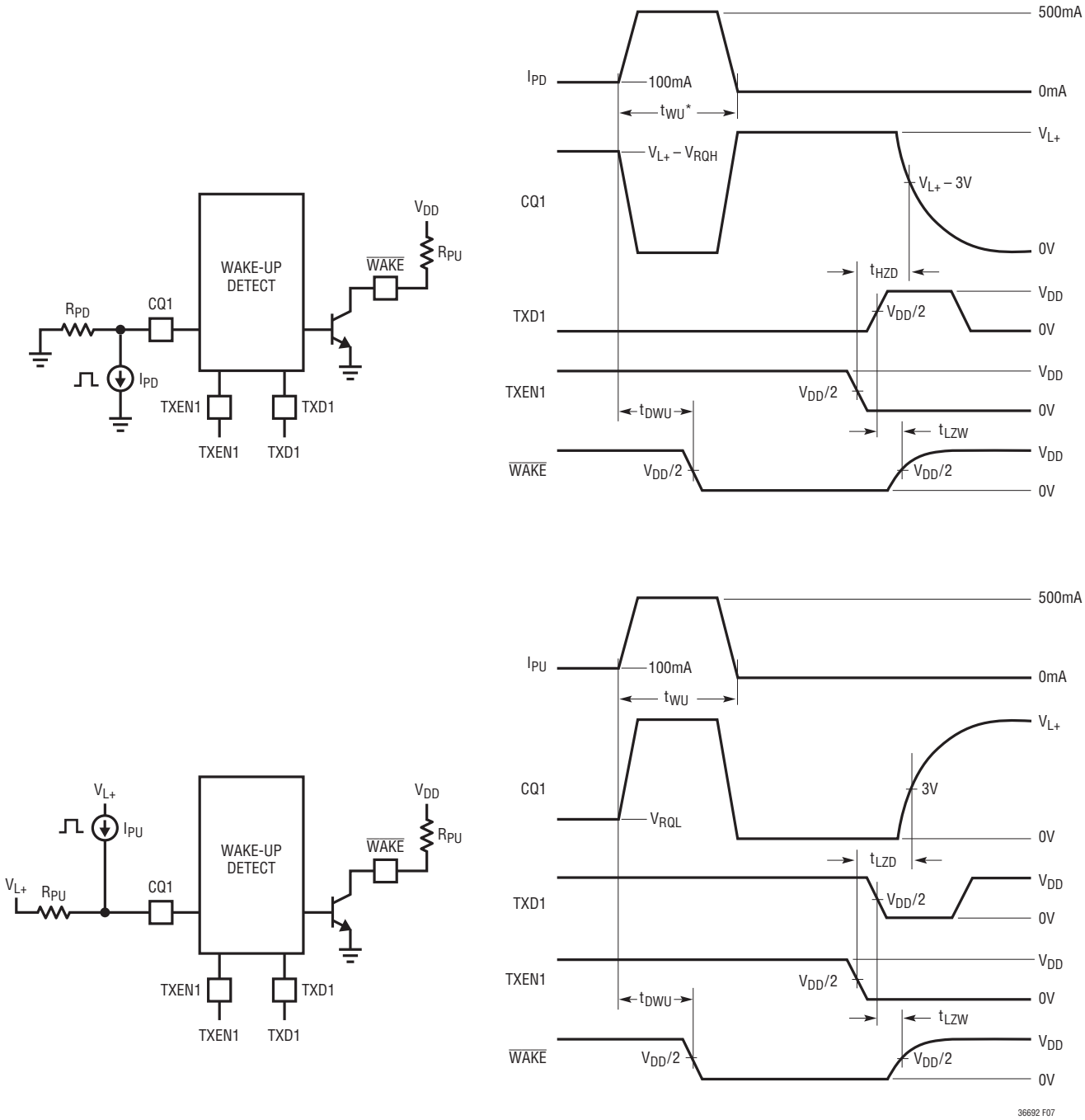


Figure 6. Power-On Reset Waveforms

TIMING DIAGRAMS



* t_{WU} is the width of the applied wake-up pulse >t_{DWU}

Figure 7. Wake-Up Waveforms

OPERATION

The LT3669/LT3669-2 is a complete industrial slave interface, including a switching voltage regulator, an LDO, a data transceiver with wake-up detect, a second driver and a power-on reset circuit. This set of features allows a typical industrial slave device to be built with just a sensor or actuator, the LT3669 and a microcontroller to provide the digital conversion and signal processing.

The line transceiver circuitry includes a receiver that monitors the CQ1 line for data and sets the output RXD1 accordingly, and a driver that drives the CQ1 line controlled by inputs TXEN1 and TXD1. Additionally, a second driver controlled by inputs TXEN2 and TXD2 drives the Q2 line. Both drivers share a common user-adjustable sink/source current limit (up to ±330mA, typical) by connecting a resistor to AGND at the ILIM pin. The drivers feature four modes of operation: push-pull, pull-up only, pull-down only, as well as a high impedance mode.

The CQ1 driver also includes a built-in wake-up pulse detect circuitry that senses when the output CQ1 is forced opposite of its driven value for a minimum of 75µs. When this wake-up signal is detected, the $\overline{\text{WAKE}}$ output pulls low to alert the host system that a data transmission is expected. The $\overline{\text{WAKE}}$ output returns to high impedance again when the host acknowledges the wake-up request by executing the handshake sequence of setting the TXEN1 input low (receive mode) and toggling the TXD1 input, or under an internal reset event. Both drivers support COM1 (4.8kb/s), COM2 (38.4kb/s) and COM3 (230.4kb/s) communication modes. The receiver supports logic swings on the CQ1 pin in accordance with the IO-Link communication standard. Tying CQ1 and Q2 pins together, as well as pins TXD1 and TXD2 and TXEN1 and TXEN2, increases the overall current capability.

The drivers are equipped with a pulsing scheme that allows them to safely drive heavy capacitive loads and incandescent bulbs. Outputs $\overline{\text{SC1}}$ and $\overline{\text{SC2}}$ will flag if CQ1 or Q2 outputs are forced within 2.95V of the opposite rail they are trying to reach. A blanking time prevents false alarms during normal output transitions.

The switching regulator of the LT3669 integrates the catch diode and provides a typical conversion efficiency greater than 60% at its maximum load current of 100mA with a standard industrial supply voltage of 24V at the L+ pin and 5V output. The LT3669-2 requires an external catch diode and provides a typical efficiency greater than 75% at its maximum load current of 300mA. Compared to a linear regulator, this drastically minimizes power dissipation in the slave device, and minimizes current draw on the industrial 24V line. The regulator features an on-chip power switch and built-in compensation, soft-start, current limit, and other support circuits required to maintain a robust, well regulated output voltage. The switching frequency is adjustable with a resistor to AGND at the RT pin to allow the circuit to be optimized either for space or efficiency, and the frequency can be synchronized to an external clock to minimize interference with signal processing circuits. A precision UVLO circuit allows the system to shut down at a user-selectable voltage.

An on-chip LDO linear regulator provides a second output voltage at up to 150mA. The LDO has current limit with foldback for robust performance in fault conditions.

The reset output ($\overline{\text{RST}}$) goes low at start-up and remains low until each regulated output is within 7.3% of its final value and the user-adjustable reset timer has expired. This ensures that the supply voltages are in regulation and stable before the signal processing circuitry is allowed to start. The reset timer is programmed with an external capacitor to AGND at the CPOR pin.

The LT3669 tolerates transient swings to +60V from GND and –60V from L+ on the CQ1 and Q2 pins without damage.

Logic inputs TXD1, TXD2, TXEN1, TXEN2 and SR feature 900mV thresholds and logic input SYNC a 1.5V threshold to interface easily with low voltage logic. All logic outputs (RXD1, $\overline{\text{RST}}$, $\overline{\text{SC1}}$, $\overline{\text{SC2}}$ and $\overline{\text{WAKE}}$) are open collector.

APPLICATIONS INFORMATION

LINE DRIVERS

Setting the Current Limit

The LT3669 line drivers have an accurate current limit that is programmed by a resistor tied from the ILIM pin to ground. Table 1 lists the necessary R_{ILIM} values for desired current limits. Tying the ILIM pin to ground sets the default current limit of 140mA.

Table 1. Current Limit vs R_{ILIM} Value

CURRENT LIMIT (mA)	R_{ILIM} VALUE (kΩ)
70	221
90	169
130	113
170	84.5
210	68.1
250	56.2
290	48.7
330	42.2

The accurate current-limit circuit loop has a time constant of approximately 10µs. Additionally, high speed current-limit clamps protect the part in case of heavy loads or short-circuits. Figure 8 depicts the high and low side driver's output current waveforms in a short-circuit condition.

Slew Rate Control

The LT3669 line drivers feature a controlled programmable slew rate for optimum EMC performance. CQ1 and Q2 rising and falling times can be programmed using the SR input pin and are independent of the L+ supply voltage. Forcing SR below 0.4V sets the rising/falling times to a typical value of 1.6µs/2.1µs. Forcing SR above 0.9V sets these times to a typical value of 260ns/340ns.

The LT3669 output drivers achieve a well controlled slew rate for a wide variety of output loads while offering a low residual voltage (<2.1V) for output load currents of up to 250mA. In order to do so, the output drivers switch to a low residual voltage mode after a defined time once the TXD signal has toggled. This time is dependent on the SR pin input level. For SR low, the drivers will enter this mode after 8.5µs; for SR high, after 1.8µs. This gives enough time for the controlled slew rate mechanism to bring the outputs to within 2.95V from the supply rails, therefore minimizing EMI during the main part of the level transition. Once the timer is expired the outputs will further approach the supply rails to within 2.1V. Figure 9 depicts the output waveforms during transitions.

Driving Heavy Loads

The LT3669 is equipped with a pulsing mechanism to drive heavy output loads like big capacitors and incandescent bulbs, and also protect it against output short-circuit conditions.

Under heavy load or output short-circuit conditions, the power dissipated in the switches may increase its local junction temperature to excessive levels if the loads were driven continuously. In order to maintain robust operation, the LT3669 output drivers use pulses of variable on-time and fixed off-time (2.2ms typical) to cool the drivers down

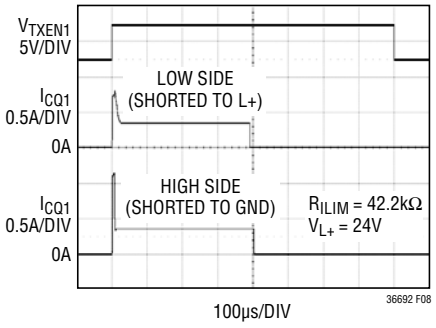


Figure 8. Current Limit Waveform in Short-Circuit

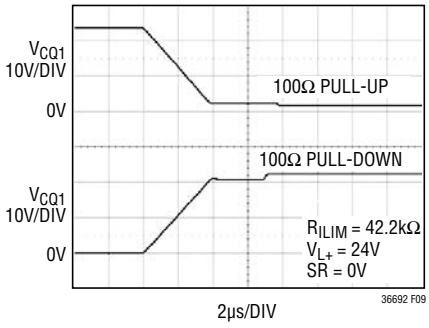


Figure 9. Output Waveforms During a Transition

APPLICATIONS INFORMATION

until the residual voltages approach within 2.95V of the intended power rail, in which case the loads are driven continuously. The on-time depends on the sum of the residual voltages for the active switches (provided that the residual voltage is higher than 2.95V) and since their current limit is fixed, it is inversely proportional to their power dissipation. The lower the power dissipated by the switches, the longer the on-time, thus optimizing the time to drive these heavy loads fully. In order to account for the case of normal load slew rate, the internal on-time timer only increases after a blanking period dependent on the SR setting. A thermal shutdown circuit with a trigger temperature of 140°C (typical) provides additional protection.

Short-Circuit and Thermal Shutdown Flags $\overline{SC1}$ and $\overline{SC2}$

A short-circuit is defined as the condition where the driver's output is within 2.95V from the opposite targeted rail, for instance if the CQ1 output is programmed to be high level (close to V_{L+}) but stays within 2.95V from GND. If either CQ1 or Q2 is short-circuited, the internal pulsing mechanism and thermal shutdown circuitry will protect the drivers. Open-collector outputs $\overline{SC1}$ and $\overline{SC2}$ will pull low during short-circuit events on CQ1 an Q2, respectively.

A heavy output load can be interpreted as a short-circuit condition during the first pulses, and $\overline{SC1}$ and $\overline{SC2}$ outputs will flag it accordingly. This information can be used by an external microcontroller to decide whether there is a real short-circuit or a heavy load is attached to the outputs. A heavy load requires a minimum amount of time to bring the driver's output outside of the short-circuit range. By setting timers using $\overline{SC1}$ and $\overline{SC2}$, a short-circuit condition can be found and the microcontroller will react accordingly (by disabling the affected driver, for example).

Figures 10, 11 and 12 show the behavior of the pulsing scheme when driving a light bulb, a 470µF capacitor and a short-circuit.

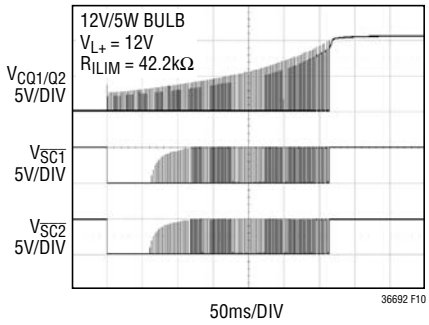


Figure 10. $\overline{SC1}$ and $\overline{SC2}$ Outputs While Driving a Light Bulb

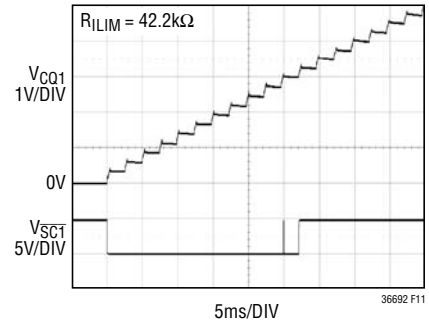


Figure 11. $\overline{SC1}$ Output While Driving 470µF

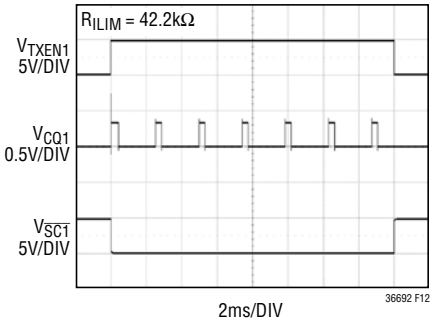


Figure 12. $\overline{SC1}$ Output While Driving a Short-Circuit

APPLICATIONS INFORMATION

If the junction temperature exceeds 140°C (typical), internal circuitry will shut the line drivers off. During the thermal shutdown event, $\overline{SC1}$ and $\overline{SC2}$ pull low simultaneously regardless of the level of the enable inputs TXEN1 and TXEN2 (see Figure 13). This behavior can be used to distinguish between short-circuit and thermal shutdown events. In case of short-circuit events without thermal shutdown being triggered, setting TXEN1 and TXEN2 low sets outputs $\overline{SC1}$ and $\overline{SC2}$ to high impedance, respectively.

While in short-circuit, the line drivers will pulse following the pulsing scheme described earlier. Depending on the cable length and nature of the heavy load, outputs $\overline{SC1}$ and $\overline{SC2}$ may report false information as the voltage across the line drivers exceeds the short-circuit range for a short time due to reflections in the cable at the beginning of each pulse. $\overline{SC1}$ and $\overline{SC2}$ should then be filtered digitally or by an RC filter before further processing. The analog filter should have a time constant of at least 80µs, for example, using pull-up resistors of 100k for $\overline{SC1}$ and $\overline{SC2}$ with 1nF to ground.

Driving Heavy Loads on Q2 During CQ1 Communication

The line drivers enter the protecting pulsing mechanism independently from each other. Only the driver under heavy load conditions will shut off after the defined pulsing on-time. While this driver is under overload conditions data can be sent reliably on the other driver in COM2 (SR < 0.4V) provided that it is enabled a minimum of 3ms before the data is actually applied on its TXD input. For IO-Link communication using the CQ1 transceiver in either COM2 (SR < 0.4V) or COM3 (SR > 0.9V), ensure the Q2 driver is not in a heavy load or short-circuit condition after a wake-up request is acknowledged and during the IO-Link start-up phase. Master and device can thus exchange initial data without disruption and establish communication successfully. Thereafter, a message sent by the master must be answered by the device after a short delay. However, the device might need additional time to perform operations before it can receive upcoming messages from the master. To support that, IO-Link defines the cycle time, the time between master messages, configured at the master side to meet the device timing requirements. If the device fails to answer a message sent by the master, as a consequence of the Q2 driver still pulsing the heavy load (disrupting CQ1 communication), the master repeats the message up to two additional times (waiting the cycle time between repetitions) before re-initiating communication by sending a new wake-up request. This master's retry property can be used to set an optimum cycle time for driving heavy loads on Q2 (by request of the IO-Link master) without breaking communication. For instance, a cycle time set to 100ms gives the Q2 driver 300ms to switch the heavy load on fully before the device has its last chance to answer (after 2 message failures) the repeated message from the master successfully.

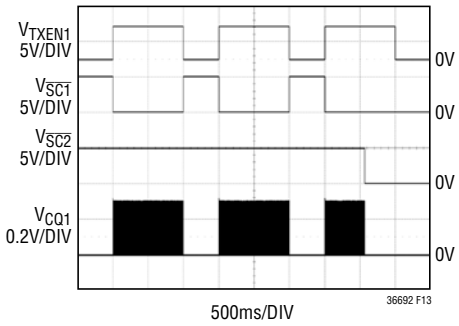


Figure 13. $\overline{SC1}$ and $\overline{SC2}$ Waveforms in Thermal Shutdown (CQ1 in Short-Circuit, TXEN2 Low)

APPLICATIONS INFORMATION

Receiver

The LT3669 line receiver input is connected to pin CQ1 and its output to pin RXD1. The receiver's thresholds are a nonlinear function of the voltage applied to L+, as shown in Figure 14.

The receiver has a noise filter that rejects pulses on the CQ1 line shorter than 1/16 of the bit time, i.e., 1.63µs for SR low (COM2) and 271ns for SR high (COM3). Pulses longer than 3.5/16 for COM2 and 5/16 for COM3 of the bit time will be detected. Pulses with duration between the mentioned time frame might be detected or rejected. Figure 15 illustrates the rejection and detection bands for a positive noise glitch.

Wake-Up

The LT3669's $\overline{\text{WAKE}}$ output can be used to flag current events on CQ1 when this line is overdriven by an external device. It works in the following way:

a) if TXEN1 is high, $\overline{\text{WAKE}}$ will pull low if CQ1 is forced opposite to its programmed level for more than 75µs. Thus, if TXD1 is high, the CQ1 programmed level is low (less than 2.1V from GND) and if an external device forces CQ1 to a voltage higher than 2.95V from GND for more than 75µs, $\overline{\text{WAKE}}$ will pull low. Similarly, if TXD1 is low, the CQ1 programmed level is high (higher than $V_{L+} - 2.1V$) and if an external device forces CQ1 to a voltage lower than $V_{L+} - 2.95V$ for more than 75µs, $\overline{\text{WAKE}}$ will pull low.

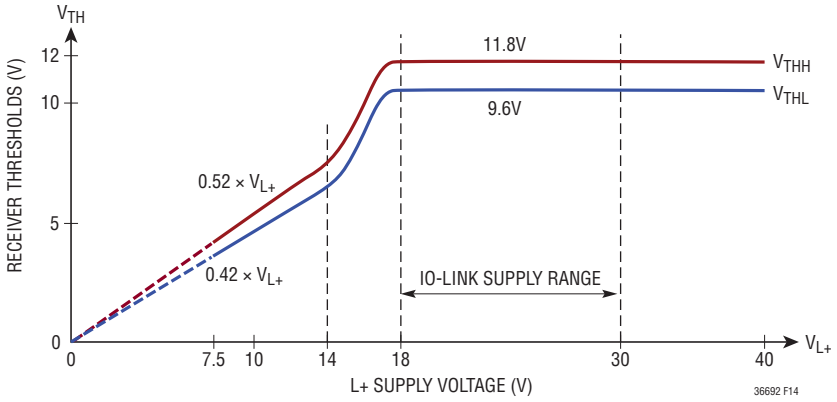


Figure 14. Receiver Thresholds vs L+ Supply Voltage

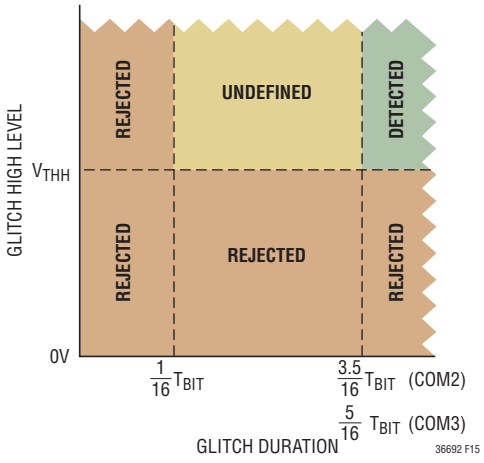


Figure 15. Receiver Noise Rejection and Detection Behavior for CQ1 Positive Glitch

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b) if TXEN1 is low, $\overline{WAKE}$ will pull low if CQ1 is forced to a voltage higher than V_{L+} – 2.95V for more than 75µs regardless of the TXD1 level. This relies on the fact that the external device has a current sink or pull-down resistor, meaning that the default level for CQ1 when TXEN1 is low will also be low.

Once $\overline{WAKE}$ pulls low, it will stay low until a defined handshaking sequence is applied to pin TXD1 and TXEN1. This sequence is as follows: TXEN1 must be set low and TXD1 toggled at least once. Figures 16a and 16b show the handshaking mechanism after $\overline{WAKE}$ pulls low for TXEN1 high and low, respectively. The $\overline{WAKE}$ output returns to high impedance also after an internal reset event.

Note that driving heavy loads or placing an external pull-up load to L+ (in case CQ1 is configured in pull-down mode) may cause $\overline{WAKE}$ to pull low as well, even if there is no external device driving the outputs. This could lead to false wake-up events which need to be handled by the microcontroller. Real wake-up events are normally followed by an exchange of information between the slave and the external device driving the outputs (master). A microcontroller can be programmed to react to a limited number of wake-up events. If no successful communication is established, then most likely there is no external driving device, but a heavy load or a pull-up load attached to the CQ1 output and the microcontroller's reaction to wake up events may be adjusted accordingly. For example, driving a 10µF capacitive load high (TXD1 set low) will force the CQ1 output below V_{L+} – 2.95V for more than 75µs (as shown in Figure 17), thus generating a false wake-up event. Similarly, configuring CQ1 in pull-down mode (TXD1 high) with an external 1k pull-up resistor to L+ will generate a false wake-up event as soon as TXEN1 is set low and the CQ1 output is pulled high by the external pull-up resistor for more than 75µs.

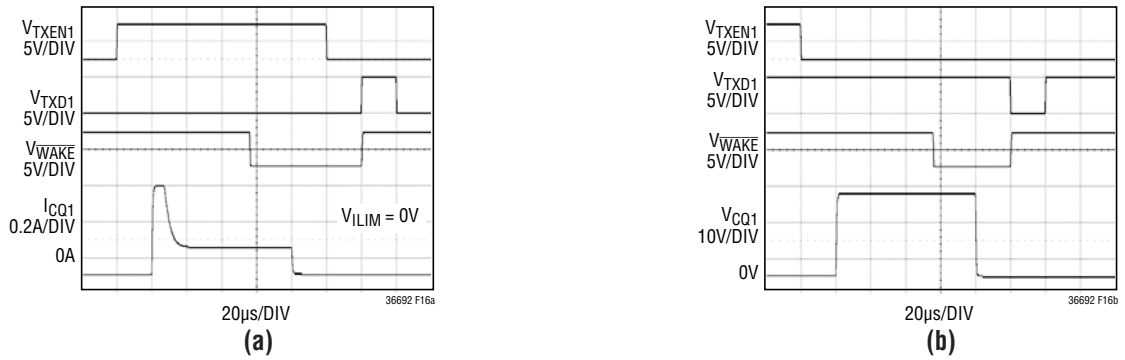

Figure 16. $\overline{WAKE}$ Handshaking Sequence When TXEN1 Is (a) High and (b) Low for V_{L+} = 24V

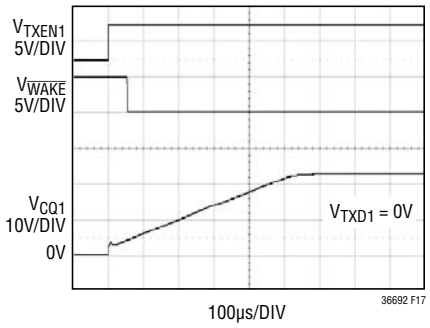

Figure 17. False Wake-Up Event When Driving a 10µF Capacitor

APPLICATIONS INFORMATION

LOW DROPOUT VOLTAGE REGULATOR (LDO)

FB_{LDO} Resistor Network

The LDO output voltage is programmed with a resistor divider between its output and the FB_{LDO} pin. Choose the resistor values according to:

$$R3 = R4 \left(\frac{V_{LDO}}{0.794V} - 1 \right)$$

Reference designators refer to the Block Diagram. Use 1% resistors to maintain output voltage accuracy.

Stability and Output Capacitance

The LT3669 LDO requires an output capacitor for stability. It is designed to be stable with most low ESR capacitors (typically ceramic, tantalum or low ESR electrolytic). Use a minimum output capacitor of 1µF with an ESR of 0.5Ω or less to prevent oscillations. Larger values of output capacitance decrease peak deviations and provide improved transient response for larger load current changes. Bypass capacitors, used to decouple individual components powered by the LT3669, increase the effective output capacitor value. If using ceramic capacitors, use X5R or X7R types.

LDO Input Considerations

For optimum efficiency and highest output current capability, connect the LDO input to the lowest possible available supply that guarantees a regulated output voltage, taking into account the maximum LDO dropout voltage of 750mV. If the programmed output of the switching regulator satisfies this condition, that supply could be a good choice. Otherwise, if no other low supply is available, then it can be connected to the DIO pin. If a bypass capacitor between LDO_{IN} and GND is needed in this configuration, connect an external diode between L+ and DIO to prevent damage on the internal reverse-polarity diode due to surge currents during hot plugging. To guarantee full reverse-polarity protection, do not connect LDO_{IN} directly to L+.

LDO Current-Limit Foldback

The LT3669 LDO has a current-limit foldback circuit that limits the maximum power dissipated by the LDO pass transistor to increase its robustness. Figure 18 shows the transfer function between current limit and voltage across the pass transistor.

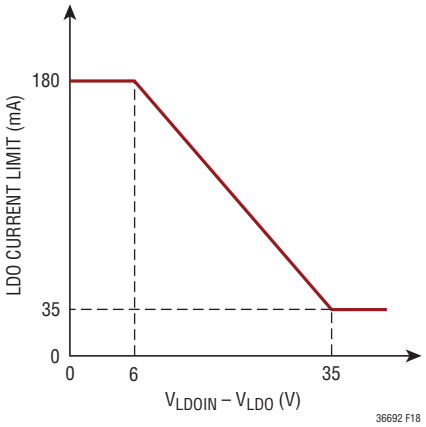

Figure 18. LDO Current Limit Foldback

Minimum LDO Load Current

The LT3669 LDO requires a minimum of 175µA load current to prevent its output from rising above the programmed voltage. It is recommended to choose the feedback resistors to meet this requirement (for example, R4 and R3 of 4.42kΩ and 14kΩ, respectively, for a 3.3V output voltage).

LDO Minimum L+ Voltage

The LDO's error amplifier is supplied from the L+ pin. A minimum L+ to LDO voltage difference of 4V is required to guarantee a regulated LDO output. For instance, for an LDO programmed output voltage of 3.3V, a minimum of 7.3V at the L+ pin would meet the requirement.

APPLICATIONS INFORMATION

SWITCHING REGULATOR

FB_{OUT} Resistor Network

The switching regulator output voltage is programmed with a resistor divider between its output and the FB_{OUT} pin. Choose the resistor values according to:

$$R1 = R2 \left(\frac{V_{OUT}}{0.794V} - 1 \right)$$

Reference designators refer to the Block Diagram. Use 1% resistors to maintain output voltage accuracy.

Setting the Switching Frequency

The LT3669 switching regulator uses a constant-frequency PWM architecture that can be programmed to switch from 250kHz to 2.2MHz by using a resistor tied from the RT pin to ground. Table 2 lists the required R_T values for various switching frequencies.

Table 2. Switching Frequency vs R_T Value

SWITCHING FREQUENCY (MHz)	R_T VALUE (kΩ)
0.25	110
0.3	88.7
0.4	63.4
0.5	47.5
0.6	38.3
0.7	31.6
0.8	26.7
0.9	22.6
1.0	19.6
1.2	15.4
1.4	12.1
1.6	10.0
1.8	8.06
2.0	6.65
2.2	5.49

Operating Frequency Trade-Offs

Selection of the operating frequency is a trade-off between efficiency, component size, minimum dropout voltage and maximum input voltage. The advantage of high frequency operation is that smaller inductor and capacitor values may be used. The disadvantages are lower efficiency, lower maximum input voltage and higher dropout voltage. The highest acceptable switching frequency ($f_{SW(MAX)}$) for a given application can be calculated as follows:

$$f_{SW(MAX)} = \frac{V_{OUT} + V_D}{t_{ON(MIN)} \bullet (V_{L+} - V_{SW} + V_D)}$$

where V_{L+} is the typical input voltage, V_{OUT} is the output voltage, V_D is the catch diode drop (~0.72V in LT3669) and V_{SW} is the internal drop from L+ to SW pins (~1.0V in LT3669 and ~1.4V in LT3669-2 at maximum load). This equation shows that a slower switching frequency is necessary to safely accommodate a high V_{L+}/V_{OUT} ratio. Lower frequency allows lower dropout voltage. The input voltage range depends on the switching frequency because the LT3669 switch has finite minimum on- and off-times. The switch can turn off for a minimum of ~210ns, but the minimum on-time is a strong function of temperature. Use the minimum switch on-time curve (see Typical Performance Characteristics) to design for an application's maximum temperature, while adding about 30% for LT3669 part-to-part variation. The minimum and maximum duty cycles that can be achieved, taking minimum on- and off-times into account are:

$$DC_{MIN} = f_{SW} \bullet t_{ON(MIN)}$$

$$DC_{MAX} = 1 - f_{SW} \bullet t_{OFF(MIN)}$$

where f_{SW} is the switching frequency, $t_{ON(MIN)}$ is the minimum switch-on time, and $t_{OFF(MIN)}$ is the minimum switch-off time. These equations show that the duty cycle range increases when the switching frequency is decreased.

A good choice of switching frequency allows adequate input voltage range (see the Input Voltage Range section) and keeps the inductor and capacitor values small.

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Input Voltage Range

The minimum input voltage is determined by either the LT3669's minimum operating voltage of 7.5V or by its maximum duty cycle (see equation in the Operating Frequency Trade-Offs section). The minimum input voltage due to duty cycle is:

$$V_{L+(MIN)} = \frac{V_{OUT} + V_D}{1 - f_{SW} \bullet t_{OFF(MIN)}} - V_D + V_{SW}$$

where $V_{L+(MIN)}$ is the minimum input voltage, and $t_{OFF(MIN)}$ is the minimum switch-off time. Note that higher switching frequency will increase the minimum input voltage. If a lower dropout voltage is desired, a lower switching frequency should be used.

The maximum input voltage for LT3669 applications depends on switching frequency, the absolute maximum ratings of the L+ and BST pins, and the operating mode. The LT3669 can operate continuously from input voltages up to 40V. Input voltage transients of up to 60V are also safely withstood. However, note that if V_{L+} exceeds V_{OVLO} (43V typical), the LT3669 will stop switching, allowing the output to fall out of regulation.

For a given application in which the switching frequency and the output voltage are already fixed, the maximum input voltage that guarantees optimum output voltage ripple for that application can be found by applying the following expression:

$$V_{L+(MAX)} = \frac{V_{OUT} + V_D}{f_{SW} \bullet t_{ON(MIN)}} - V_D + V_{SW}$$

where $V_{L+(MAX)}$ is the maximum operating input voltage, V_{OUT} is the output voltage, V_D is the catch diode drop (~0.72V in LT3669) and V_{SW} is the internal drop from L+ to SW pins (~1.0V in LT3669 and ~1.4V in LT3669-2 at maximum load), f_{SW} is the switching frequency (set by R_T), and $t_{ON(MIN)}$ is the minimum switch-on time. Note that a higher switching frequency will reduce the maximum operating input voltage. Conversely, a lower switching frequency is necessary to achieve optimum operation at high input voltages.

Special attention must be paid when the output is in start-up, short-circuit, or other overload conditions. In these cases, the LT3669 tries to bring the output in regulation by driving lots of current into the output load. During these events, the inductor peak current might easily reach and even exceed the maximum current limit of the LT3669, especially in those cases where the switch already operates at minimum on-time. The circuitry monitoring the current through the catch diode prevents the switch from turning on again if the inductor valley current is above 0.2A and 0.45A nominal values for LT3669 and LT3669-2, respectively. In these cases, the inductor peak current is therefore the maximum current limit of the LT3669 plus the additional current overshoot during the turn-off delay due to minimum on-time:

$$I_{L(PEAK)} = I_{SW(LIM)} + \frac{V_{L+(MAX)} - V_{OUTOL}}{L} \bullet t_{ON(MIN)}$$

where $I_{L(PEAK)}$ is the peak inductor current, $I_{SW(LIM)}$ is the switch current limit (0.325A in LT3669 and 0.65A in LT3669-2), $V_{L+(MAX)}$ is the maximum expected input voltage, L is the inductor value, $t_{ON(MIN)}$ is the minimum on-time and V_{OUTOL} is the output voltage under the overload condition. The part is robust enough to survive prolonged operation under these conditions as long as the peak inductor current does not exceed 0.6A in LT3669 and 1.3A in LT3669-2. Inductor current saturation and excessive junction temperature may further limit performance.

Inductor Selection and Maximum Output Current

A good first choice for the inductor value is:

$$L = (V_{OUT} + V_D) \bullet \frac{k}{f_{SW}}$$

(k = 9 in LT3669, k = 3.6 in LT3669-2)

where f_{SW} is the switching frequency in MHz, V_{OUT} is the output voltage, V_D is the catch diode drop (~0.72V in LT3669) and L is the inductor value in µH.

The inductor's RMS current rating must be greater than the maximum load current and its saturation current should be about 30% higher. To keep the efficiency high, the series resistance (DCR) should be less than 0.1Ω, and the core material should be intended for high frequency applications. Table 3 lists several vendors of inductors.

APPLICATIONS INFORMATION

Table 3. Inductor Vendors

VENDOR	URL
Murata	www.murata.com
TDK	www.componenttdk.com
Toko	www.toko.com
Coilcraft	www.coilcraft.com
Sumida	www.sumida.com
Würth Elektronik	www.we-online.com
Coiltronics	www.cooperet.com

For robust operation in fault conditions (start-up or short-circuit) and high input voltage (>30V), choose the saturation current high enough to ensure that the inductor peak current does not exceed 0.6A and 1.3A for LT3669 and LT3669-2, respectively. For example, an LT3669-2 application running from an input voltage of 36V using a 33µH inductor with a saturation current of 0.8A will tolerate the mentioned fault conditions.

The optimum inductor for a given application may differ from the one indicated by this simple design guide. A larger value inductor provides a higher maximum load current and reduces the output voltage ripple. If your load is lower than the maximum load current, then you can relax the value of the inductor and operate with higher ripple current. This allows the use of a physically smaller inductor, or one with a lower DCR resulting in higher efficiency. Be aware that if the inductance differs from the simple rule, then the maximum load current will depend on input voltage. In addition, low inductance may result in discontinuous mode operation, which further reduces maximum load current. For details of maximum output current and discontinuous mode operation, see Linear Technology's Application Note 44. Finally, for duty cycles greater than 50% ($V_{OUT}/V_{L+} > 0.5$), a minimum inductance is required to avoid subharmonic oscillations:

$$L_{MIN} = (V_{OUT} + V_D) \bullet \frac{k}{f_{SW}}$$

(k = 6.5 in LT3669; k = 2.6 in LT3669-2)

The current in the inductor is a triangle wave with an average value equal to the load current. The peak inductor and switch current is:

$$I_{SW(PEAK)} = I_{L(PEAK)} = I_{OUT(MAX)} + \frac{\Delta I_L}{2}$$

where $I_{L(PEAK)}$ is the peak inductor current, $I_{OUT(MAX)}$ is the maximum output load current, and ΔI_L is the inductor ripple current. The LT3669 limits its switch current in order to protect itself and the system from overload faults. Therefore, the maximum output current that the LT3669 will deliver depends on the switch current limit, the inductor value and the input and output voltages.

When the switch is off, the voltage across the inductor is the output voltage plus the catch diode drop. This gives the peak-to-peak ripple current in the inductor:

$$\Delta I_L = \frac{(1-DC) \bullet (V_{OUT} + V_D)}{L \bullet f_{SW}}$$

where f_{SW} is the switching frequency of the LT3669, DC is the duty cycle and L is the value of the inductor.

To maintain output regulation, the inductor peak current must be less than the switch current limit I_{LIM} which is 0.325A (LT3669) and 0.65A (LT3669-2) at low duty cycles and decreases to 0.24A (LT3669) and 0.48A (LT3669-2). The maximum output current is also a function of the chosen inductor value and can be approximated by the following expression:

$$I_{OUT(MAX)} = I_{LIM} - \frac{\Delta I_L}{2} =$$

$$I_{LIM(DC = 0)} \bullet (1 - 0.26 \bullet DC) - \frac{\Delta I_L}{2}$$

($I_{LIM(DC = 0)}$ = 0.325A in LT3669;

$I_{LIM(DC = 0)}$ = 0.65A in LT3669-2)

Choosing an inductor value so that the ripple current is small will allow a maximum output current near the switch current limit.

One approach to choosing the inductor is to start with the simple rule—look at the available inductors, and choose one to meet cost or space goals. Then use these equations

APPLICATIONS INFORMATION

to check that the LT3669 will be able to deliver the required output current. Note again that these equations assume that the inductor current is continuous. Discontinuous operation occurs when I_{OUT} is less than $\Delta I_L/2$.

Input Capacitor

Bypass the input of the LT3669 circuit with a ceramic capacitor of X7R or X5R type. Do not use Y5V types, which have poor performance over temperature and applied voltage. A 4.7µF ceramic capacitor is adequate to bypass the LT3669 and will easily handle the ripple current. Note that larger input capacitance is required when a lower switching frequency is used. If the input power source has high impedance, or there is significant inductance due to long wires or cables, additional bulk capacitance may be necessary. This can be provided with a lower performance electrolytic capacitor.

Step-down regulators draw current from the input supply in pulses with very fast rise and fall times. The input capacitor is required to reduce the resulting voltage ripple at the LT3669 and to force this very high frequency switching current into a tight local loop, minimizing EMI. A 4.7µF capacitor is capable of this task, but only if it is placed close to the LT3669 (see the PCB Layout section for more information). A second precaution regarding the ceramic input capacitor concerns the maximum input voltage rating of the LT3669. A ceramic input capacitor combined with trace or cable inductance forms a high-Q (underdamped) tank circuit. If the LT3669 circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the LT3669's voltage rating. For guidance see Application Note 88.

Output Capacitor and Output Ripple

The output capacitor has two essential functions. Along with the inductor, it filters the square wave generated by the LT3669 to produce the DC output. In this role, it determines the output ripple. Additionally, low impedance at the switching frequency is important. The second function is to store energy needed to satisfy transient loads and stabilize the LT3669's control loop. Ceramic capacitors have very low equivalent series resistance (ESR) and provide the best ripple performance. A good starting value is:

$$C_{OUT} = \frac{k}{V_{OUT} \bullet f_{SW}}$$

(k = 17 in LT3669; k = 43 in LT3669-2)

where f_{SW} is in MHz, and C_{OUT} is the recommended output capacitance in µF. Use X5R or X7R types. This choice will provide low output ripple and good transient response. Transient performance can be improved with a higher value capacitor if combined with a phase lead capacitor (typically 22pF) between the output and the feedback pin (FB_{OUT}). A lower value of output capacitor can be used to save space and cost but transient performance will suffer.

When choosing a capacitor, look carefully through the data sheet to find out what the actual capacitance is under operating conditions (applied voltage and temperature). A physically larger capacitor, or one with a higher voltage rating, may be required. High performance tantalum or electrolytic capacitors can be used for the output capacitor. Low ESR is important, so choose one that is intended for use in switching regulators. The ESR should be 0.05Ω or less. Such a capacitor will be larger than a ceramic capacitor and will have a larger capacitance, because the capacitor must be large to achieve low ESR.

LT3669-2 Diode Selection

The catch diode (D1 from the LT3669-2 Block Diagram) conducts current only during the switch-off time. Average forward current in normal operation is

$$I_{D(AVG)} = I_{OUT} \bullet (1–DC)$$

where DC is the duty cycle. However, a diode with 1A current rating is required for overload conditions. For inputs up to the maximum operating voltage of 40V, use a diode with a reverse-voltage rating greater than the input voltage. If transients at the input of up to 60V are expected, use a diode with a reverse-voltage rating only higher than the maximum OVLO of 45V. If operating at high ambient temperatures, consider using a Schottky with low reverse leakage. For example, Diodes, Inc. SBR1U40LP or DFLS160, ON Semiconductor MBRM140, and Central Semiconductor CMMSH1-60 are good choices for the catch diode.

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BST and BD Pin Considerations

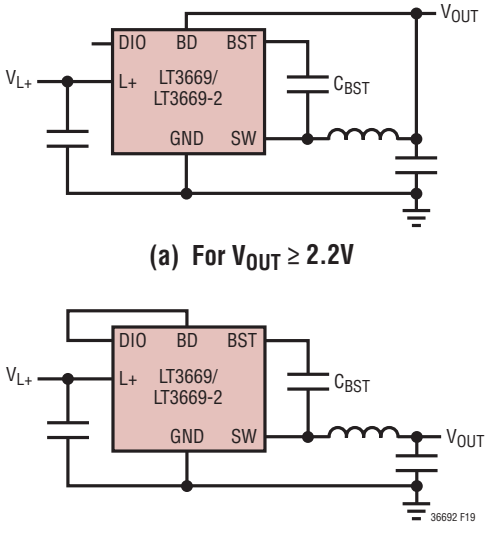
Capacitor C_{BST} and the internal boost Schottky diode (see the Block Diagram) are used to generate a boost voltage that is higher than the input voltage. In most cases a 0.1µF (LT3669) and 0.22µF (LT3669-2) capacitor will work well. Figure 19 shows two ways to arrange the boost circuit. The BST pin must be more than 1.9V above the SW pin for best efficiency. For outputs of 2.2V and above, the standard circuit (Figure 19a) is best. For outputs between 2.2V and 2.5V, use a 0.22µF (LT3669) and 0.47µF (LT3669-2) boost capacitor. For output voltages below 2.2V the boost diode can be tied to the input through pin DIO to preserve reverse-polarity protection (Figure 19b), or to another external supply greater than 2.2V. However the circuit in Figure 19a is more efficient because the BST pin current comes from a lower voltage source. Be sure that the maximum voltage ratings of the BST and BD pins are not exceeded.

The minimum operating voltage of an LT3669 application is limited by the minimum input voltage and by the maximum duty cycle as outlined previously. For proper start-up, the minimum input voltage is also limited by the boost circuit. If the input voltage is ramped slowly, or the LT3669 is turned on with its EN/UVLO pin (when the output is already in regulation), then the boost capacitor may not be fully charged. Because the boost capacitor is charged with the energy stored in the inductor, the circuit will rely on some minimum load current to get the boost circuit running properly. This minimum load will depend on input and output voltages, and on the arrangement of the boost circuit. The minimum load generally goes to zero once the circuit has started. In many cases the discharged output capacitor will present a load to the switcher, which will allow it to start. For a given programmed output voltage V_{OUT}, the minimum input voltage that guarantees a proper start-up regardless of load current is V_{OUT} + 2V.

Synchronization

Synchronizing the LT3669 oscillator to an external frequency can be done by connecting a square wave (with 20% to 80% duty cycle) to the SYNC pin. The square wave amplitude should have valleys that are below 0.5V and peaks that are above 1.5V (up to 6V).

The LT3669 may be synchronized over a 300kHz to 2.2MHz range. Choose the R_T resistor to set the LT3669 switching frequency 20% below the lowest synchronization input. For example, if the synchronization signal will be 360kHz, choose R_T for 300kHz. To assure a reliable



(a) For $V_{OUT} \geq 2.2V$

(b) For $V_{OUT} < 2.2V$; $V_{L+} < 25V$

Figure 19. Two Circuits for Generating the Boost Voltage

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and safe operation, the LT3669 will only synchronize when the output voltage is near regulation. Therefore, it is necessary to choose a large enough inductor value to supply the required output current at the frequency set by the R_T resistor. See the Inductor Selection section for more information. It is also important to note that slope compensation is set by the R_T value. To avoid subharmonics, calculate the minimum inductor value using the frequency determined by R_T.

PCB Layout

For proper operation and minimum EMI, care must be taken during printed circuit board layout. Figure 20 shows the recommended component placement with trace, ground plane and via locations. Note that large, switched currents flow in the LT3669's L+, SW and GND pins, the external catch diode (LT3669-2) and the input capacitor (C_{L+}). Place these components, along with the inductor and output capacitor (C_{OUT}), on the same side of the circuit board, and connect them on that layer, keeping the loop they form as small as possible.

All connections to GND should be made at a common star ground point or directly to a local, unbroken ground plane underneath. The SW and BST nodes should be laid out carefully to avoid interference. If the part is synchronized externally using the SYNC pin, arrange this signal to avoid interference with sensitive nodes, especially FB_{LDO}, FB_{OUT}, CPOR, ILIM and RT. Finally, keep the FB_{LDO}, FB_{OUT}, CPOR, ILIM and RT nodes small so that the ground traces will shield them from the SW and BST nodes. The exposed pad, Pin 29, on the bottom of the package acts as a heat sink and must be soldered to the ground node. To keep thermal resistance low, extend the ground plane as much as possible and add thermal vias under and near the LT3669 to any additional ground planes within the circuit board and on the bottom side.

High Temperature Considerations

Power dissipation within the LT3669 can be estimated by adding the power dissipated by the switching regulator, LDO and line drivers. The switching regulator's power dissipation can be obtained from an efficiency measurement. The LDO's power dissipation can be extracted simply by calculating the product between load current and voltage drop across the LDO pass device. The line drivers' contribution can be calculated in a similar manner taking the product of residual voltage and load current for each driver.

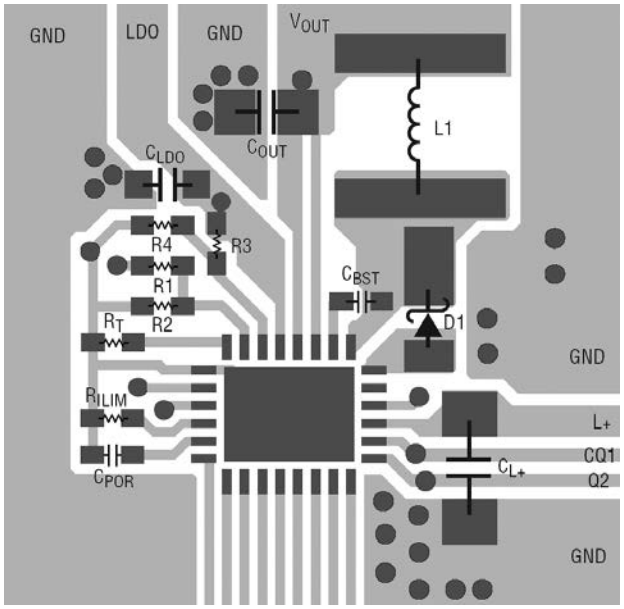

Figure 20. A Good PCB Layout Ensures Proper, Low EMI Operation

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The last parameter to take into account is the quiescent current required to keep all circuits working properly which is about 6mA. As an example, assume an L+ voltage of 24V, a programmed V_{OUT} and V_{LDO} voltages of 5V and 3.3V respectively and load currents for both line drivers of 250mA. The LDO input is connected to the switching regulator output and both switching regulator and LDO outputs are driving full load (300mA and 150mA, respectively). The total power dissipation can be estimated as:

$$P_D = 24V \bullet 0.006A + (5V - 3.3V) \bullet 0.15A +$$
$$5V \bullet 0.3A \bullet 25\% + 2 \bullet 1.5V \bullet 0.25A = 1.524W$$

With a θ_{JA} of 44°C/W, the increase in junction temperature compared to ambient will be 67°C.

The LT3669 protects itself against internal overheating with the help of two independent thermal shutdown circuits. One of them, with a hysteresis of 12°C, shuts only the line drivers off if the junction temperature exceeds 140°C, and pulls both $\overline{SC1}$ and $\overline{SC2}$ outputs low during the thermal shutdown event. The LDO and switching regulator outputs keep in regulation, allowing a µC to process the event. This thermal shutdown circuit keeps the junction temperature under control in those cases where only the line drivers are under heavy load or short-circuit conditions. In case of fault conditions on the LDO or switching regulator outputs, a second thermal shutdown circuit shuts them off if the junction temperature exceeds 168°C. Figure 21 depicts waveforms during a thermal shutdown event.

Reverse-Polarity Protection

The LT3669 is designed to withstand ±60V between any combination of the line driver ports (L+, CQ1, Q2 and GND).

The switching regulator's power devices are powered from L+ through an integrated reverse-polarity protection diode whose cathode is also wired to the DIO pin. In order to avoid damaging this diode due to surge currents during hot plugging, do not place any bypass capacitors at the DIO pin (leave it unconnected) unless an external diode is connected to bolster the integrated one.

Surge and ESD Protection Considerations

The LT3669 contains internal protection against ESD pulses (HBM 100pF/1.5kΩ) of ±4kV for the interface ports (L+, CQ1, Q2 and GND) and ±2kV for all other pins.

In order to protect the LT3669 interface ports against surge and contact/air discharge events based on the IEC 61000-4-5 and IEC 61000-4-2 standards, additional external protection is required. TVS diodes with breakdown voltages above the maximum operating voltage of the application and clamp voltages below 60V (for the maximum expected short-circuit current during the surge/ESD event) are required.

SM6T39A or equivalent TVS clamps are recommended for IO-Link and most other applications with L+ operating voltages as high as 36V and will protect the part against

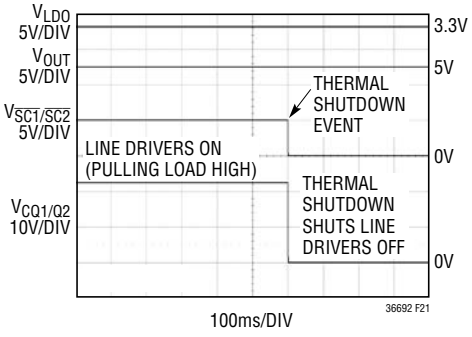


Figure 21. Thermal Shutdown Waveforms

APPLICATIONS INFORMATION

±2kV (Level 2) surge and ±6kV (Level 3) contact/air discharge events provided that there are bypass capacitors (>470pF) attached to pins CQ1 and Q2 and L+. For IO-Link L+ operation up to 30V, use SM6T36A or equivalent TVS clamps to further increase surge and ESD protection. Use SMCJ36A or equivalent TVS clamps for L+ operation above 36V. Figure 22 shows the placement of the TVS diodes to protect the LT3669 against surge events applied between any combination of the line driver ports.

UNDERVOLTAGE LOCKOUT

The LT3669 undervoltage lockout circuitry monitors the input supply L+ as well as the input pin EN/UVLO and disables the internal circuitry if various conditions are not met.

The LT3669 EN/UVLO pin voltage is internally compared to a precise 1.5V reference and can be used as an adjustable undervoltage lockout (see Figure 23). Setting this pin below the 1.5V threshold disables the switcher, LDO and line drivers. Typically, UVLO is used in situations in which the input supply is current limited, or has a relatively high source resistance. A switching regulator draws constant power from the source, so source current increases as source voltage drops. This looks like a negative resistance load to the source and can cause the source to current limit or latch low under low source voltage conditions. EN/UVLO prevents the LT3669 from operating at source voltages where the problems might occur.

Additional circuitry monitors the L+ voltage, too, and disables the line drivers if it falls below 6.5V. The switching regulator and LDO are disabled for V_{L+} below 6.0V. Current is drawn from L+ as soon as it is above 0.65V. Setting EN/UVLO low reduces the quiescent current to 1.15mA.

Keep the connections from the resistors to the EN/UVLO pin short and ensure the interplane or surface capacitance to switching nodes is minimized. If high resistor values are used, bypass the EN/UVLO pin with a 1nF capacitor to prevent coupling problems from the switch node.

OUTPUT VOLTAGE MONITORING

The LT3669 provides power supply monitoring for microprocessor-based systems including a power-on reset (POR).

A precise internal voltage reference and precision POR comparator circuit monitor the LT3669 LDO and switching regulator output voltages. These output voltages must be above 92.7% of the programmed value for $\overline{RST}$ not to be asserted (refer to the Timing Diagrams section). The LT3669 will assert $\overline{RST}$ during power-up, power-down and brownout conditions. Once the output voltage rises above the $\overline{RST}$ threshold, the adjustable reset timer is started and $\overline{RST}$ is released after the reset timeout period

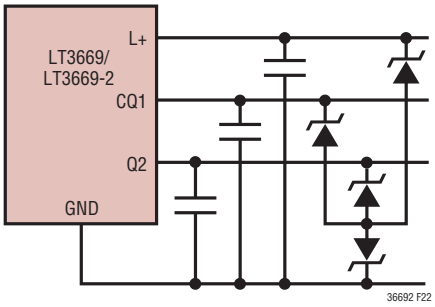


Figure 22. Placement of TVS Diodes

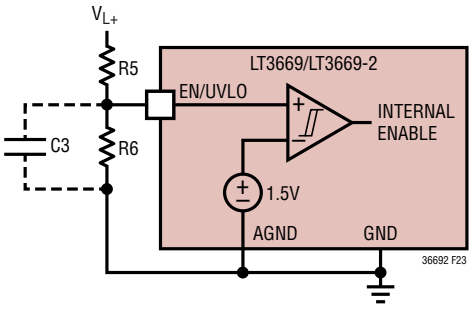


Figure 23. Undervoltage Lockout

APPLICATIONS INFORMATION

(see Figure 24). On power-down, once the output voltage drops below $\overline{RST}$ threshold, $\overline{RST}$ is held at a logic low. The reset timer is adjustable using an external capacitor. The POR comparator is designed to be robust against FB_{OUT} and FB_{LDO} pin noise, which could potentially false-trigger the $\overline{RST}$ pin. The POR comparator lowpass filters the first stage of the comparator. This filter integrates the output of the comparator before asserting the $\overline{RST}$. The benefit of adding this filter is that any transients at the buck regulator's output must be of sufficient magnitude and duration before it triggers a logic change in the output. This prevents spurious resets caused by output voltage transients, such as load steps or short brownout conditions, without sacrificing the DC reset threshold accuracy.

The $\overline{RST}$ signal also resets the internal wake-up latch. A wake-up event can then only be flagged when the $\overline{RST}$ signal goes high.

Selecting the Reset Timing Capacitor

The reset timeout period is adjustable in order to accommodate a variety of microprocessor applications. Set the reset timeout period, (t_{RST}), by connecting a capacitor, C_{POR}, between the CPOR pin and ground, with value determined by:

$$C_{POR} = t_{RST} \bullet 8000 \frac{pF}{ms}$$

This equation is accurate for reset timeout periods of 1.0ms, or greater. To program faster timeout periods, see the Reset Timeout Period vs Capacitance graph in the Typical Performance Characteristics section. Leaving the CPOR pin unconnected will generate a minimum reset timeout of approximately 22µs. Maximum reset timeout is limited by the largest available low leakage capacitor. The accuracy of the timeout period will be affected by capacitor leakage (the nominal charging current is 10µA) and capacitor tolerance. A low leakage ceramic capacitor is recommended.

To prevent noise from false tripping the comparator on the CPOR pin, place a 10pF capacitor between the $\overline{RST}$ and CPOR pins. The rising edge of $\overline{RST}$ coupled into the CPOR pin ensures generating a clean reset signal.

IO-Link Disclaimer

Linear Technology attempts to maintain compatibility with the IO-Link interface and system specifications. LTC is not a member of the IO-Link Consortium as set forth by PROFIBUS Nutzerorganisation (PNO) e.V.

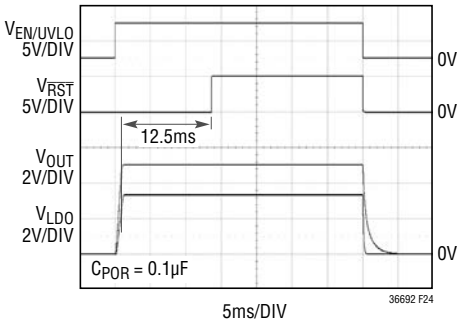
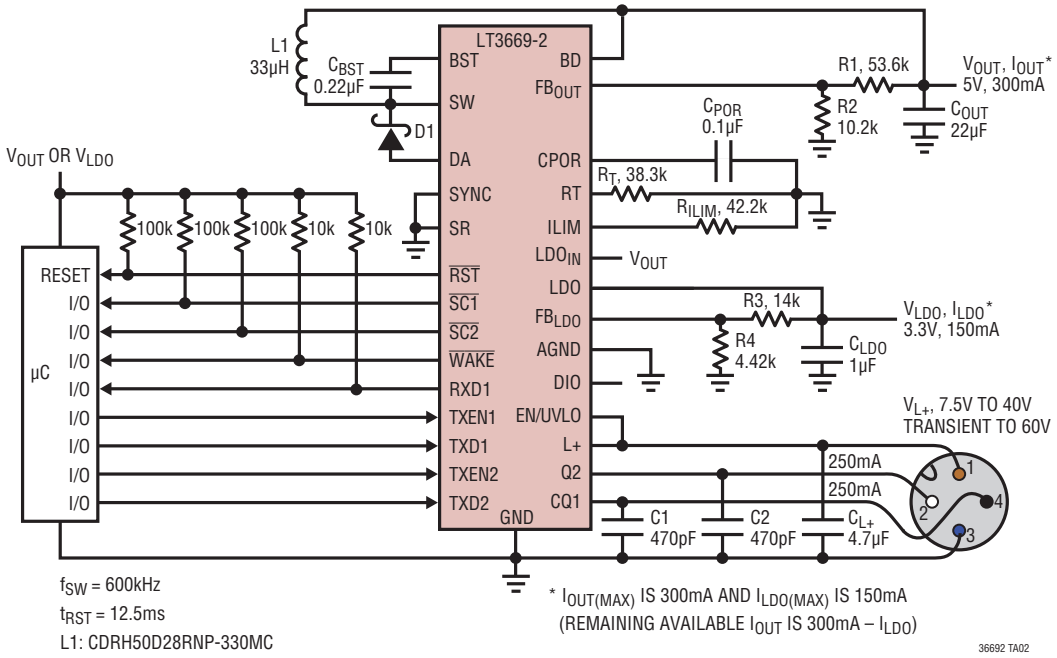


Figure 24. Reset Timer Waveforms

TYPICAL APPLICATIONS

5V Buck, 3.3V LDO, COM2, 250mA Line Drivers

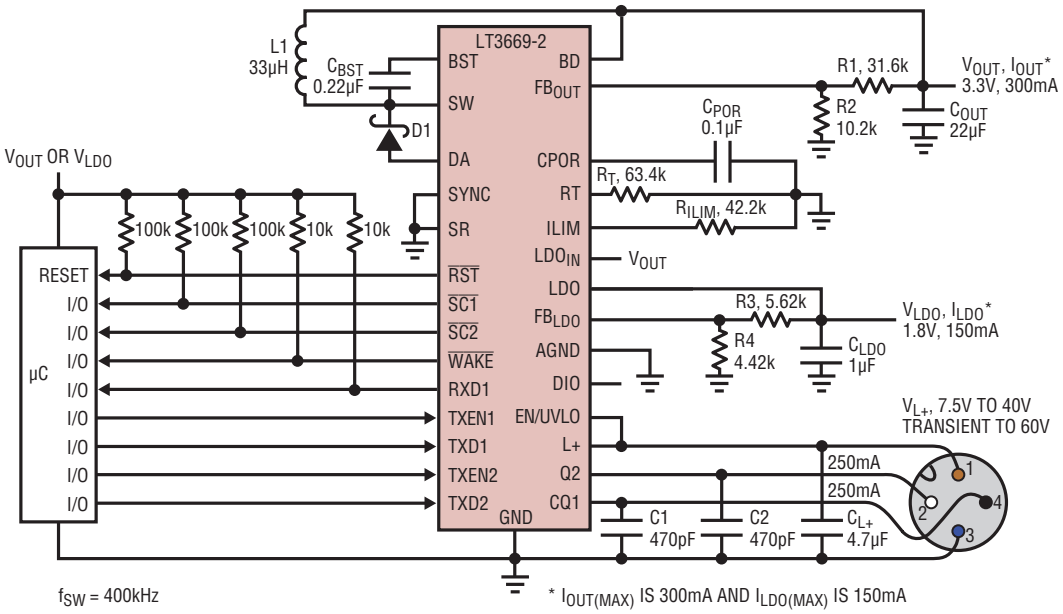


f_{SW} = 600kHz
t_{RST} = 12.5ms
L1: CDRH50D28RNP-330MC

* $I_{OUT(MAX)}$ IS 300mA AND $I_{LDO(MAX)}$ IS 150mA
(REMAINING AVAILABLE I_{OUT} IS 300mA – I_{LDO})

36692 TA02

3.3V Buck, 1.8V LDO, COM2, 250mA Line Drivers



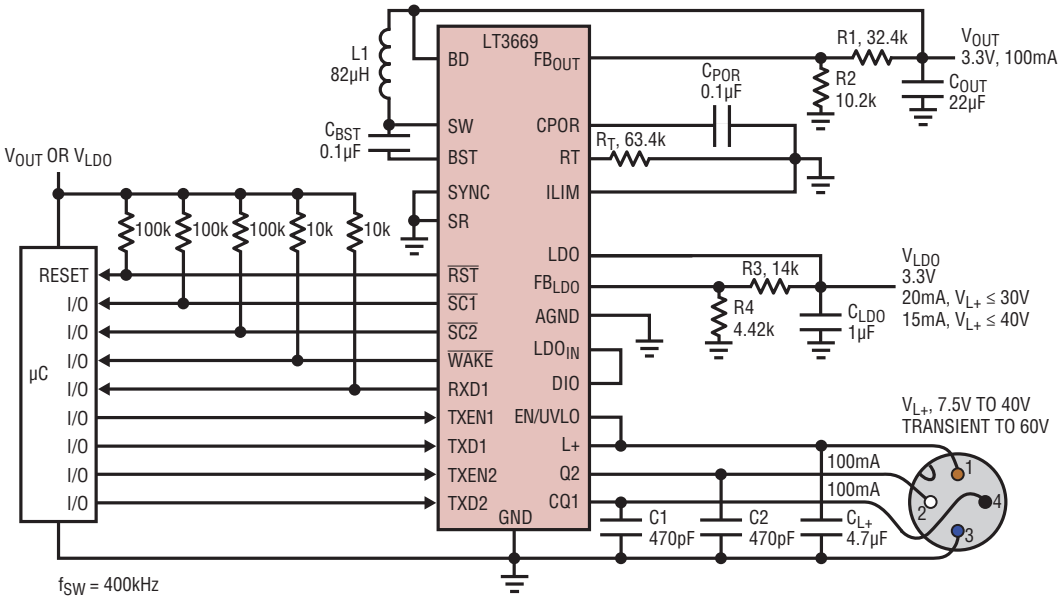
f_{SW} = 400kHz
t_{RST} = 12.5ms
L1: CDRH50D28RNP-330MC

* $I_{OUT(MAX)}$ IS 300mA AND $I_{LDO(MAX)}$ IS 150mA
(REMAINING AVAILABLE I_{OUT} IS 300mA – I_{LDO})

36692 TA03

TYPICAL APPLICATIONS

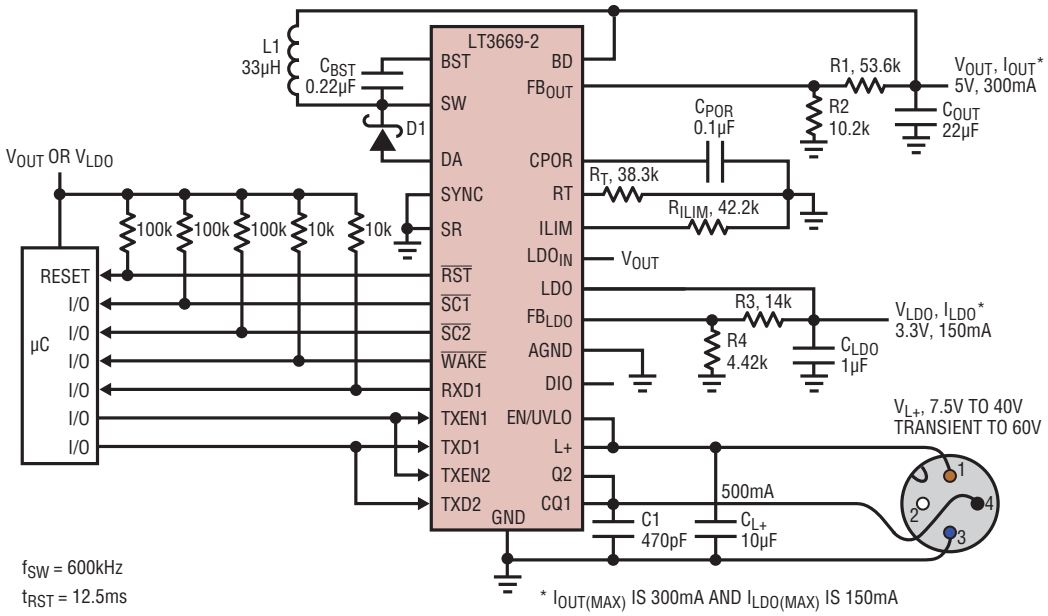
3.3V Buck, 3.3V LDO, COM2, 100mA Line Drivers



f_{SW} = 400kHz
t_{RST} = 12.5ms
L1: CDRH4D22HPNP-820MC

36692 TA04

5V Buck, 3.3V LDO, COM2, 500mA Line Driver (Non IO-Link)



f_{SW} = 600kHz
t_{RST} = 12.5ms
L1: CDRH50D28RNP-330MC

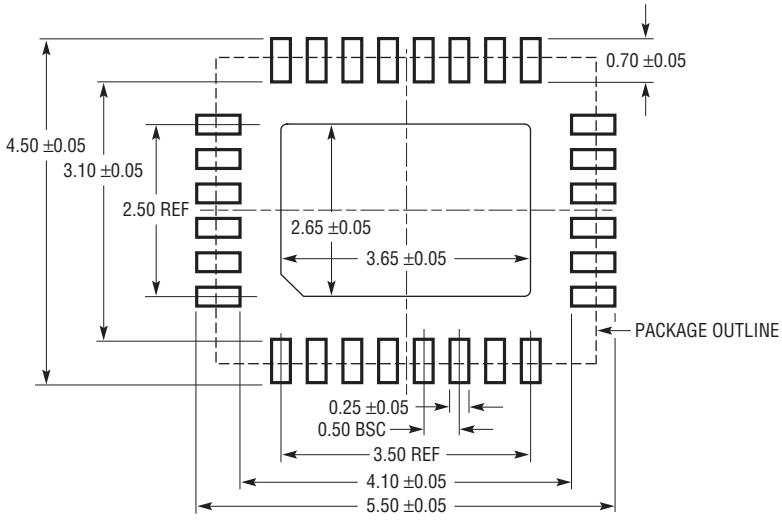
* $I_{OUT(MAX)}$ IS 300mA AND $I_{LDO(MAX)}$ IS 150mA
(REMAINING AVAILABLE I_{OUT} IS 300mA – I_{LDO})

36692 TA05

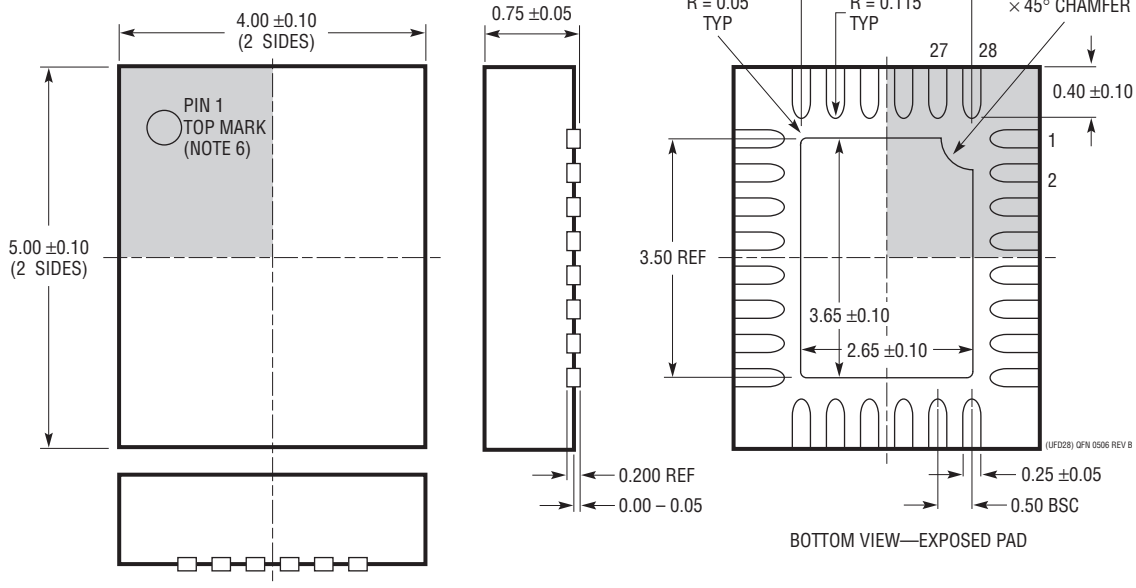
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

UFD Package
28-Lead Plastic QFN (4mm × 5mm)
(Reference LTC DWG # 05-08-1712 Rev B)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WXXX-X).
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	2/15	Clarified conditions in Electrical Characteristics.	3, 4, 5, 6
		Added Driving Heavy Loads on Q2 During CQ1 Communications section.	23
		Clarified $I_{OUT(MAX)}$ equations.	29
		Clarified power dissipation equation.	33
		Clarified Surge and ESD Protection Considerations.	33, 34

LINEAR TECHNOLOGY

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