High Current Synchronous Step-Down LED Driver with Three-State Control

FEATURES

- **PWM Dimming Provides Up to 3000:1 Dimming Ratio**
- **CTRL_SEL Dimming Provides Up to 3000:1 Dimming Ratio Between Any Current**
- **Three-State Current Control for Color Mixing**
- **±6% Current Regulation Accuracy**
- 6V to 36V Input Voltage Range
- Average Current Mode Control
- 2µs Maximum Recovery Time Between Any Current Regulation State
- <1µA Shutdown Current
- Output Voltage Regulation and Open-LED Protection
- Thermally Enhanced 4mm × 5mm QFN and 28-Pin FE Package

APPLICATIONS

- DLP Projectors
- High Power Architectural Lighting
- Laser Diodes

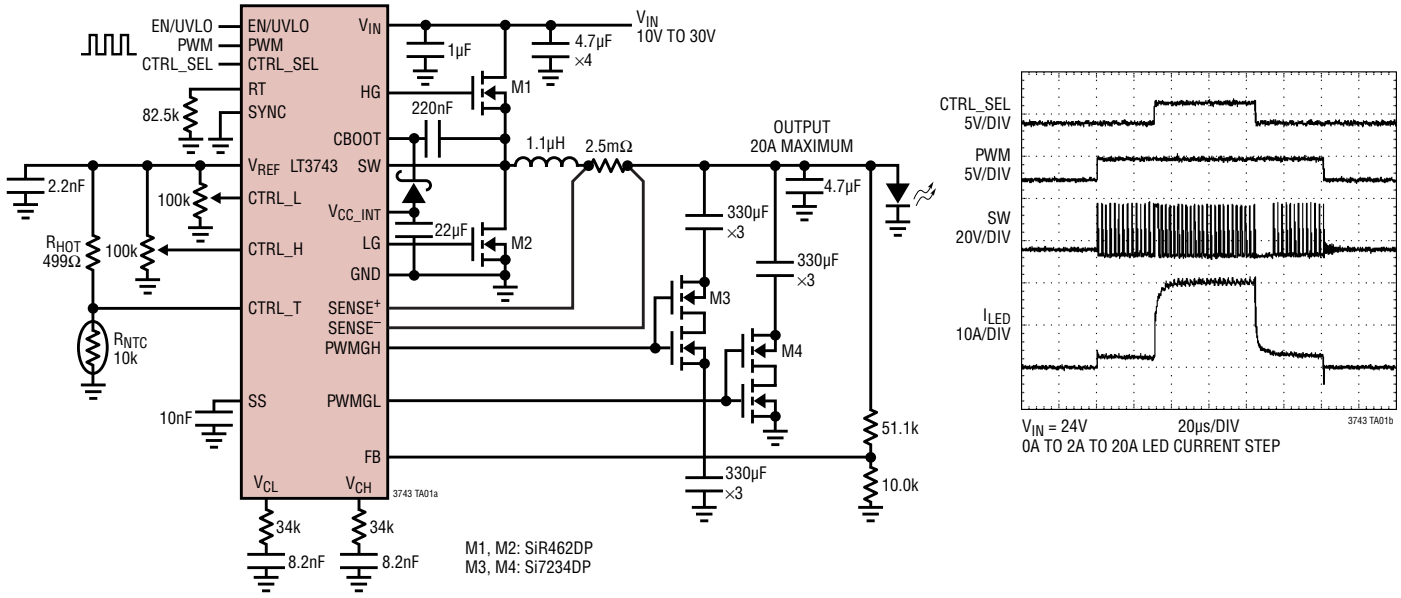
DESCRIPTION

The LT®3743 is a fixed frequency synchronous step-down DC/DC controller designed to drive high current LEDs. The average current mode controller will maintain inductor current regulation over a wide output voltage range of 0V to (V_{IN} – 2V). LED dimming is achieved through analog dimming on the CTRL_L, CTRL_H and CTRL_T pins and with PWM dimming on the PWM and CTRL_SEL pins. Through the use of externally switched load capacitors, the LT3743 is capable of changing regulated LED current levels within several µs, providing accurate, high speed PWM dimming between two current levels. The switching frequency is programmable from 200kHz to 1MHz through an external resistor on the RT pin.

Additional features include voltage regulation and overvoltage protection set with a voltage divider from the output to the FB pin. Overcurrent protection is provided and set by the CTRL_H pin.

TYPICAL APPLICATION

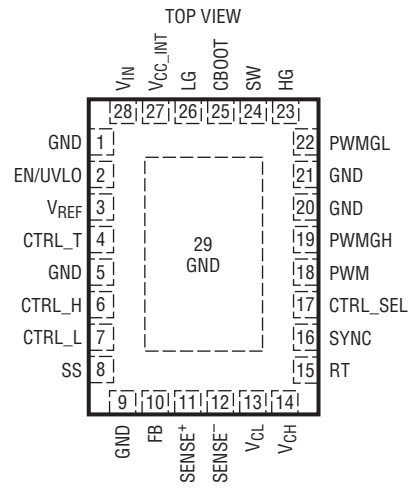
92% Efficient 20A LED Driver



ABSOLUTE MAXIMUM RATINGS (Note 1)

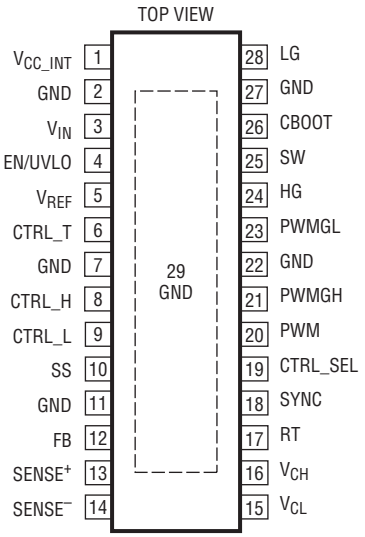
V_{IN} Voltage 40V
EN/UVLO Voltage 6V
V_{REF} Voltage 3V
CTRL_L, CTRL_H, CTRL_T Voltage 3V
PWM, CTRL_SEL Voltage 6V
$SENSE^+$ Voltage 40V
$SENSE^-$ Voltage 40V
V_{CH}, V_{CL} Voltage 3V
SW Voltage 40V
CBOOT 46V
RT Voltage 3V
FB Voltage 3V
SS Voltage 6V
SYNC Voltage 6V
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)
TSSOP ..... 300°C

PIN CONFIGURATION



UFD PACKAGE
28-LEAD (4mm × 5mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JA} = 37°C/W
EXPOSED PAD (PIN 29) IS GND, MUST BE SOLDERED TO PCB



FE PACKAGE
28-LEAD PLASTIC TSSOP

T_{JMAX} = 125°C, θ_{JA} = 30°C/W
EXPOSED PAD (PIN 29) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION (Note 2)

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3743EUFD#PBF	LT3743EUFD#TRPBF	3743	28-Lead (4mm × 5mm) Plastic QFN	–40°C to 125°C
LT3743IUFD#PBF	LT3743IUFD#TRPBF	3743	28-Lead (4mm × 5mm) Plastic QFN	–40°C to 125°C
LT3743EFE#PBF	LT3743EFE#TRPBF	LT3743FE	28-Lead Plastic TSSOP	–40°C to 125°C
LT3743IFE#PBF	LT3743IFE#TRPBF	LT3743FE	28-Lead Plastic TSSOP	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, $V_{EN/UVLO}$ = 5V, V_{SYNC} = 0V, V_{CTRL_SEL} = 0V, V_{PWM} = 2V, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range			6		36	V
V_{IN} Pin Quiescent Current (Note 3) Non-Switching Operation Shutdown Mode	 V_{PWM} = V_{CTRL_SEL} = 0V, Not Switching, R_T = 40k $V_{EN/UVLO}$ = 0V	 ●		 1.8 0.1	 2.5 1	 mA µA
EN/UVLO Pin Falling Threshold			1.49	1.55	1.61	V
EN/UVLO Hysteresis				130		mV
EN/UVLO Pin Current	V_{IN} = 6V, EN/UVLO = 1.45V			5.5		µA
PWM Pin Threshold				1.0		V
CTRL_SEL Threshold				1.0		V
SYNC Pin Threshold				1.0		V
CTRL_H and CTRL_L Pin Control Range			0		1.5	V
CTRL_H and CTRL_L Pin Current				100		nA
Reference						
Reference Voltage (V_{REF} Pin)		●	1.96	2	2.04	V
Inductor Current Sensing						
Full Range SENSE+ to SENSE–	V_{CTRL_H} = 1.5V, V_{SENSE}^- = 6V	●	48	51	54	mV
SENSE+ Pin Current	V_{SENSE}^+ = V_{SENSE}^- = 6V			50		nA
SENSE– Pin Current	V_{SENSE}^+ = V_{SENSE}^- = 6V			10		µA
Internal V_{CC} Regulator (V_{CC_INT} Pin)						
Regulation Voltage		●	4.7	5	5.2	V
NMOS FET Driver (Note 2)						
Non-Overlap time HG to LG				100		ns
Non-Overlap time LG to HG				60		ns
Minimum On-Time LG	(Note 3)			50		ns
Minimum On-Time HG	(Note 3)			80		ns
Minimum Off-Time LG	(Note 3)			60		ns
High Side Driver Switch On-Resistance Gate Pull Up Gate Pull Down	V_{CBOOT} – V_{SW} = 5V			 2.3 1.3		 Ω Ω
Low Side Driver Switch On-Resistance Gate Pull Up Gate Pull Down	V_{CC_INT} = 5V			 2.5 1.3		 Ω Ω
Switching Frequency						
f_{SW}	R_T = 40kΩ R_T = 200kΩ	●	900 190	1000 200	1070 233	kHz kHz
Soft-Start						
Charging Current				5.5		µA
Voltage Regulation Amplifier						
Input Bias Current				1		nA
g_m				200		µA/V
Feedback Regulation Voltage	V_{CTRL_H} = 0V, V_{CTRL_L} = 2V, V_{SENSE}^+ = 2V	●	0.945	1	1.025	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, $V_{EN/UVLO}$ = 5V, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
PWMG Control Signals						
CTRL_SEL High to PWMGL Low Delay				10	40	ns
CTRL_SEL High to PWMGH High Delay				150	200	ns
CTRL_SEL Low to PWMGH Low Delay				30	60	ns
CTRL_SEL Low to PWMGL High Delay				170	220	ns
PWMGH and PWMGL Pull-up Impedance				3.2		Ω
PWMGH and PWMGL Pull-Down Impedance				1.75		Ω
Current Control Loop g_m Amp						
Offset Voltage	V_{SENSE}^+ = 4V, V_{SENSE}^- = 4V	●	–3	0	3	mV
Input Common Mode Range $V_{CM(LOW)}$ $V_{CM(HIGH)}$	 $V_{CM(HIGH)}$ Measured from V_{IN} to V_{CM}			 0 2		 V V
Output Impedance				3.5		MΩ
g_m			375	475	625	µA/V
Differential Gain				1.7		V/mV

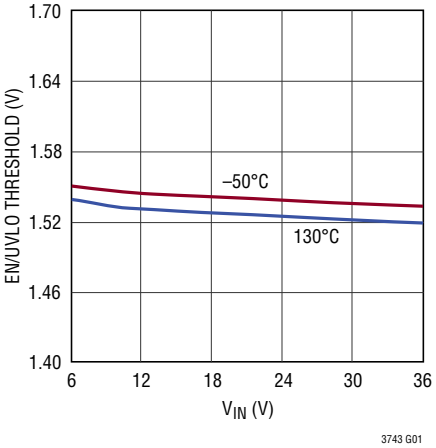
Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LT3743E is guaranteed to meet performance specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT3743I is guaranteed to meet performance specifications over the –40°C to 125°C operating junction temperature range.

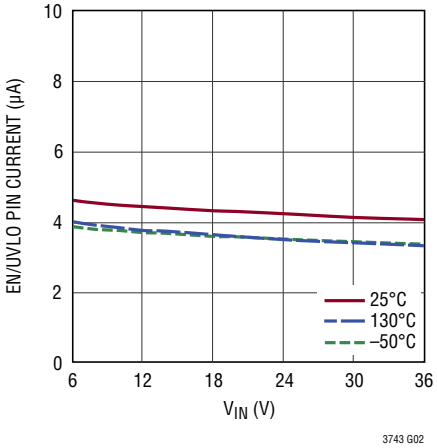
Note 3: The minimum on and off times are guaranteed by design and are not tested.

TYPICAL PERFORMANCE CHARACTERISTICS

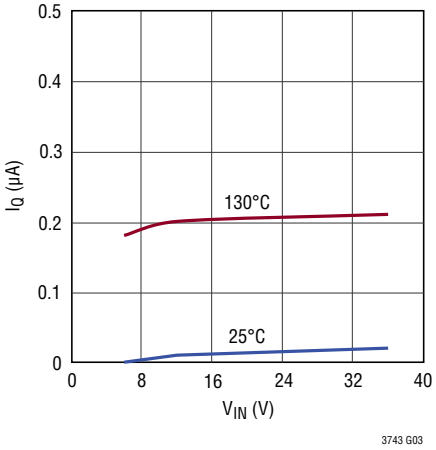
EN/UVLO Threshold (Falling)



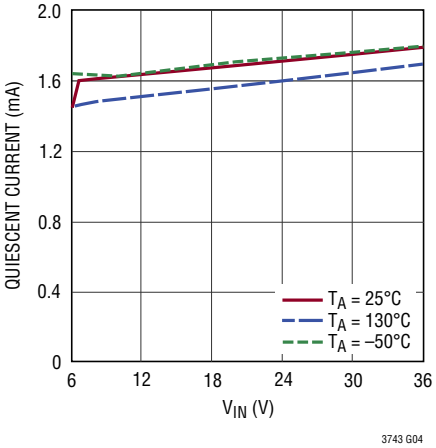
EN/UVLO Pin Current



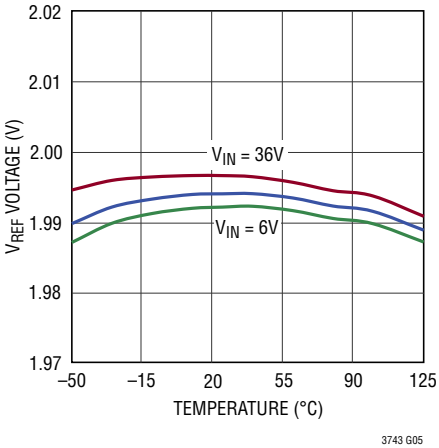
I_Q in Shutdown



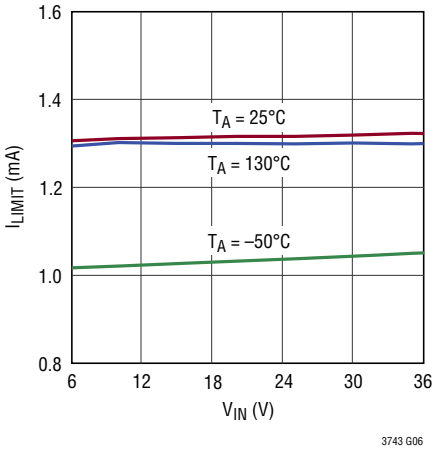
Quiescent Current (Non-Switching)



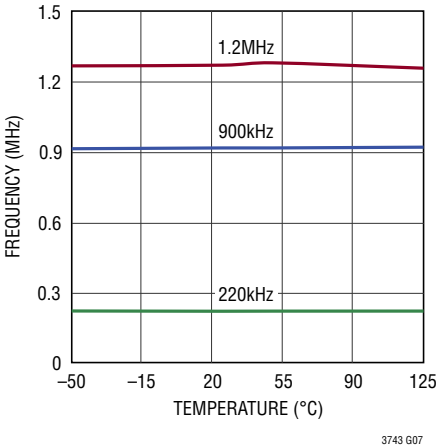
V_{REF} Pin Voltage



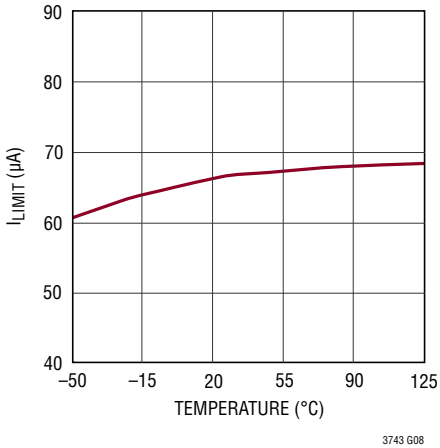
V_{REF} Current Limit



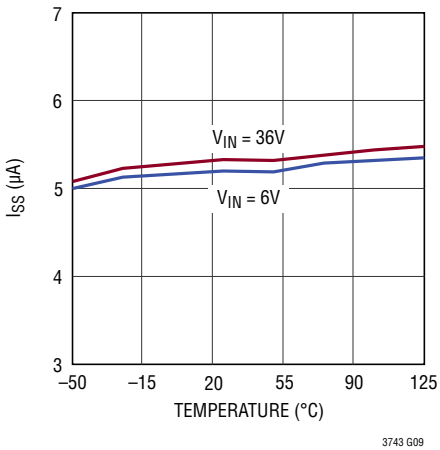
Oscillator Frequency



RT Pin Current Limit

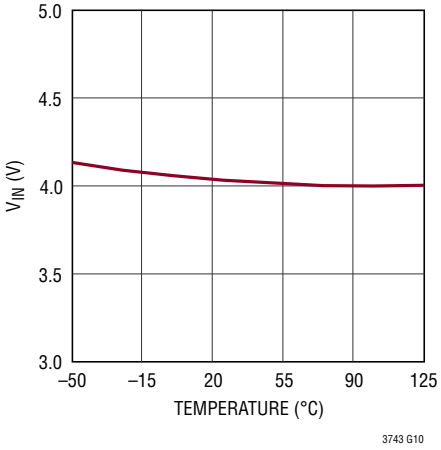


Soft-Start Pin Current

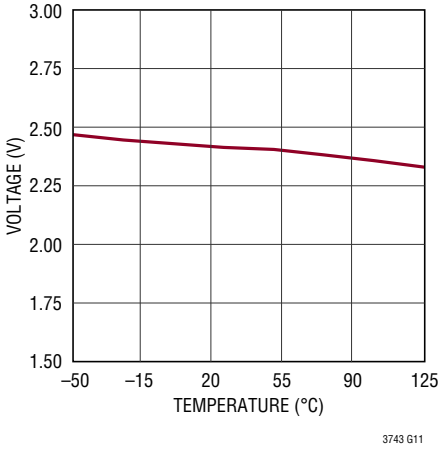


TYPICAL PERFORMANCE CHARACTERISTICS

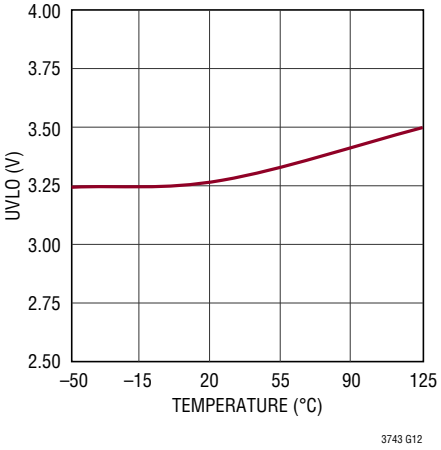
Internal UVLO



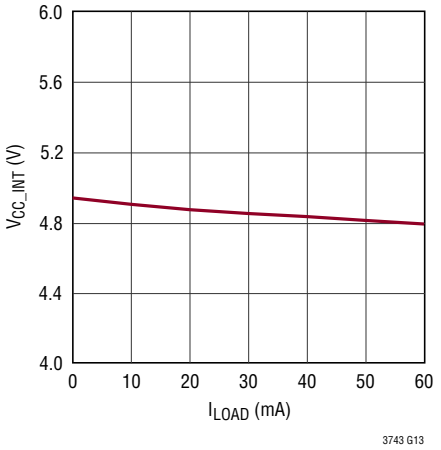
CBOOT-SW UVLO Voltage



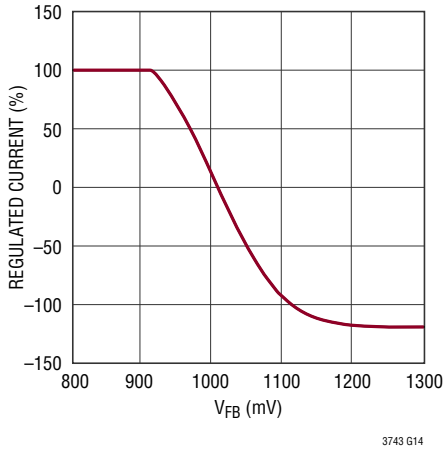
V_{CC_INT} UVLO



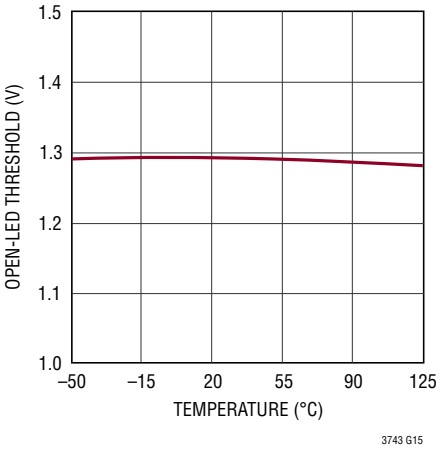
V_{CC_INT} Load Reg at 12V



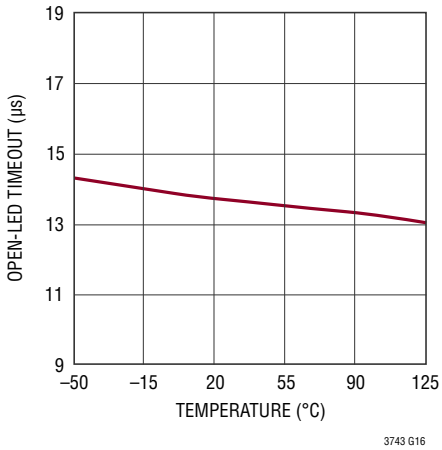
Regulated Current vs V_{FB}



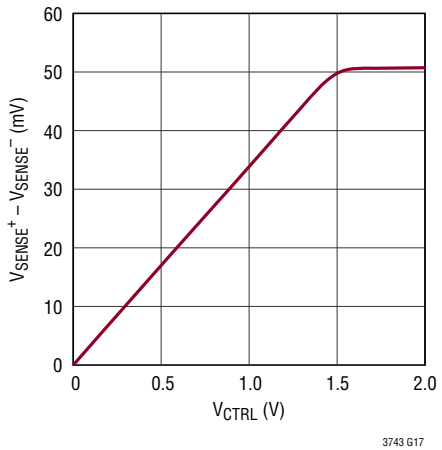
Open-LED Threshold



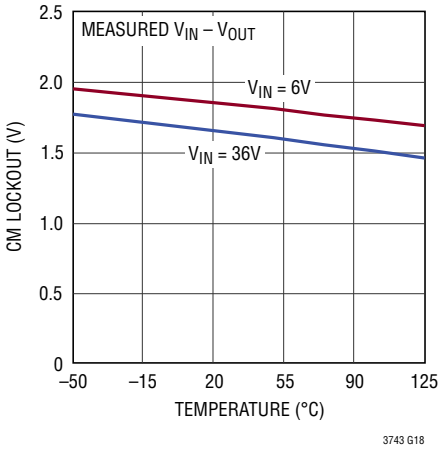
Open-LED Timeout



Regulated Sense Voltage

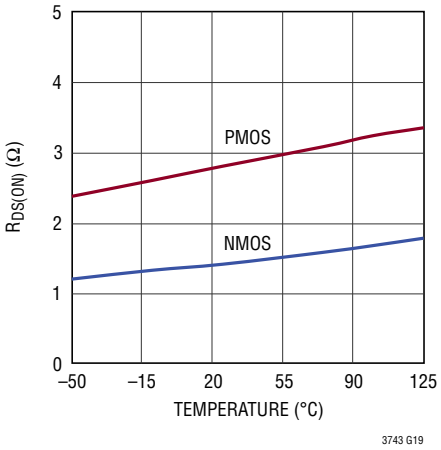


Common Mode Lockout

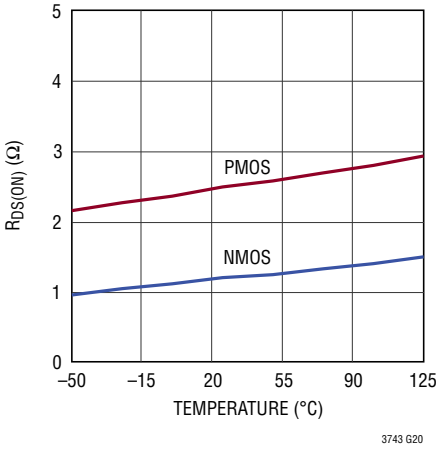


TYPICAL PERFORMANCE CHARACTERISTICS

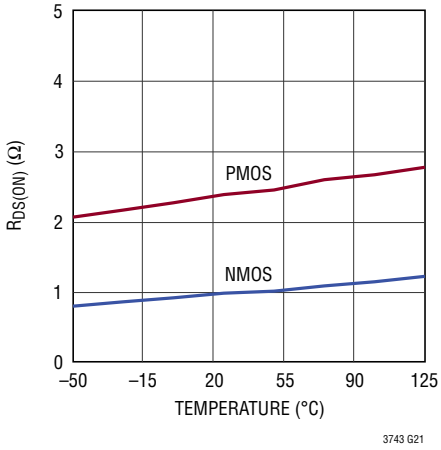
PWM Driver $R_{DS(ON)}$



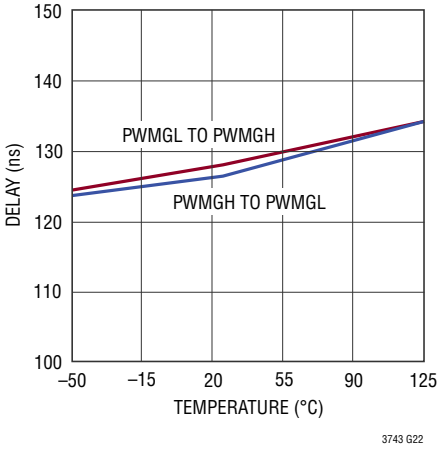
HG Driver $R_{DS(ON)}$



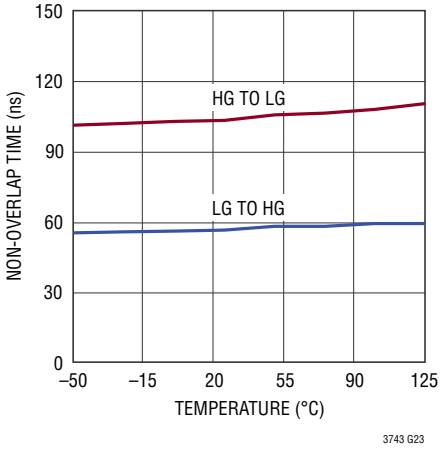
LG Driver $R_{DS(ON)}$



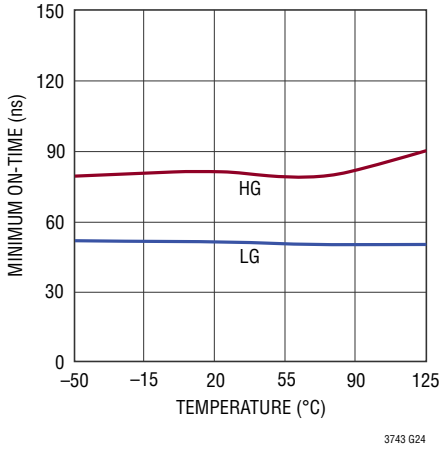
Non-Overlap PWM Signal Delay



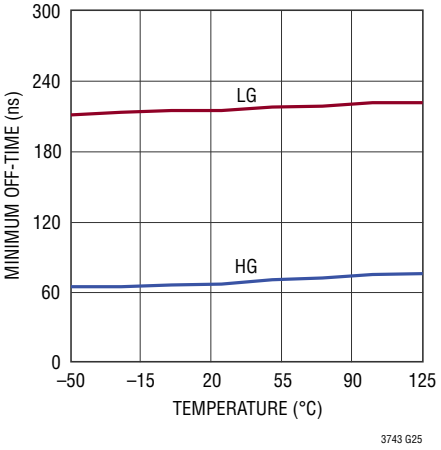
Non-Overlap Time



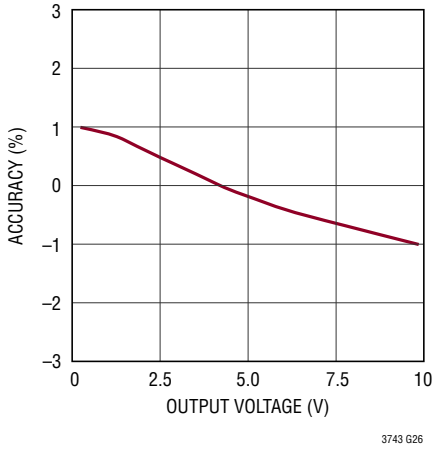
Minimum On-Time



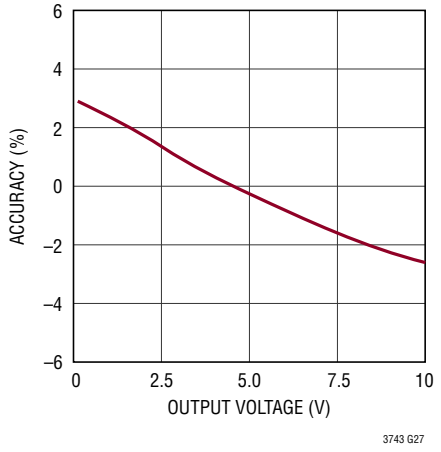
Minimum Off-Time



Regulation Accuracy
CTRL_H = 1.5V, V_{IN} = 12V

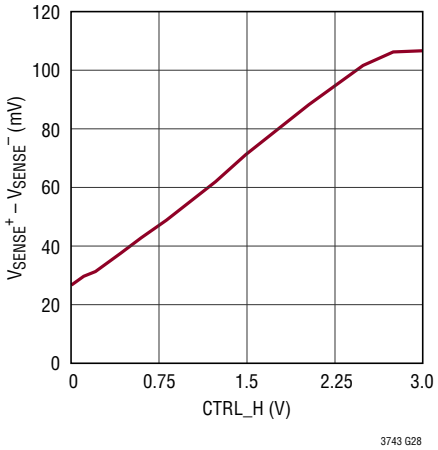


Regulation Accuracy
CTRL_H = 0.75V, V_{IN} = 12V

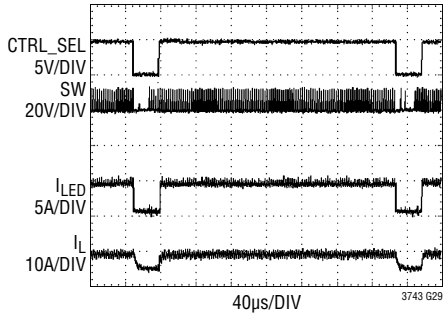


TYPICAL PERFORMANCE CHARACTERISTICS

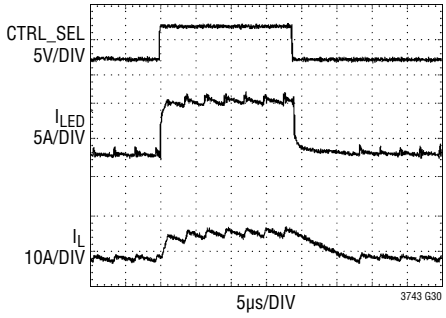
Overcurrent Threshold



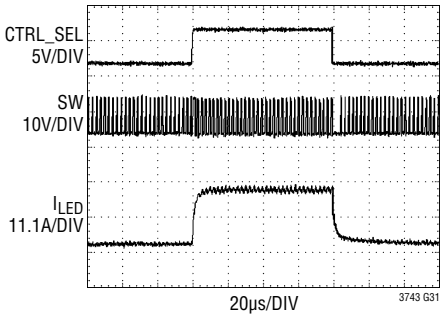
LED Current Waveforms (90% PWM) 0.5A to 5A



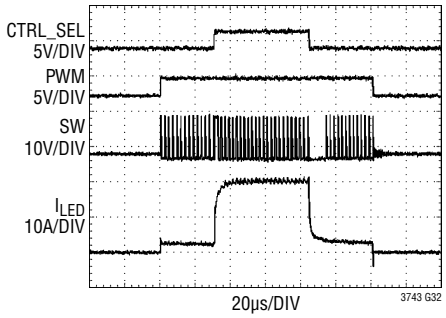
LED Current Waveforms (2000:1) 3A to 10A



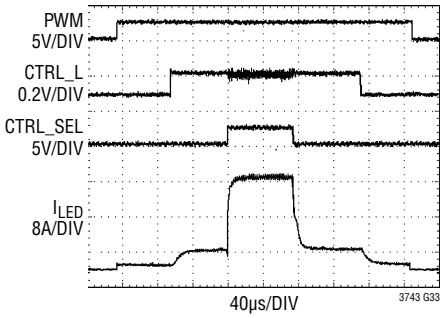
LED Current Waveforms (3000:1) 2A to 20A



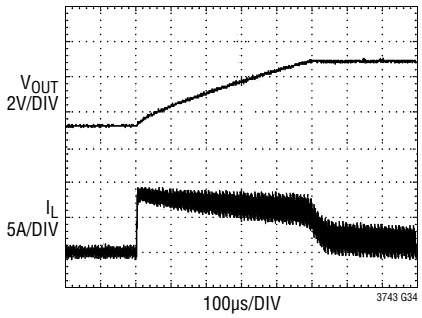
LED Current Waveforms (3000:1) 0A to 2A to 20A



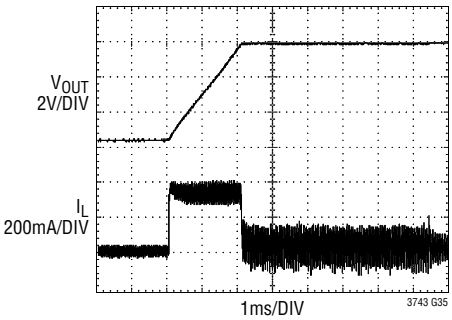
LED Current Waveforms (3000:1) Analog Dimming on CTRL_L $C_{OUT(LOW)}$ = 22µF, $C_{OUT(HIGH)}$ = 1mF



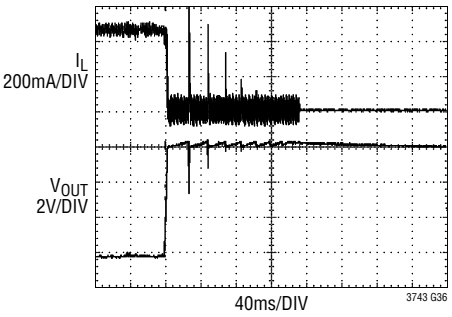
Voltage Regulation with 10A Regulated Inductor Current



Common Mode Lockout (V_{IN} = 7V)



Overvoltage Lockout Operation With Open-Load Condition



PIN FUNCTIONS (QFN/TSSOP)

GND (Pins 1, 5, 9, 20, 21, Exposed Pad Pin 29/Pins 2, 7, 11, 22, 27, Exposed Pad Pin 29): Ground. The exposed pad must be soldered to the PCB.

EN/UVLO (Pin 2/Pin 4): Enable Pin. The EN/UVLO pin acts as an enable pin and turns on the internal current bias core and subregulators at 1.55V. The pin does not have any pull-up or pull-down, requiring a voltage bias for normal part operation. Full shutdown occurs at approximately 0.5V.

V_{REF} (Pin 3/Pin 5): Buffered 2V Reference Capable of 0.5mA Drive.

CTRL_T (Pin 4/Pin 6): The thermal control input to reduce the regulated current level for both current levels (CTRL_L and CTRL_H).

CTRL_H (Pin 6/Pin 8): The CTRL_H pin sets the high level regulated output current and overcurrent. The maximum input voltage is internally clamped to 1.5V. The overcurrent set point is equal to the high level regulated current level set by the CTRL_H pin with an additional 23mV offset between the $SENSE^+$ and $SENSE^-$ pins.

CTRL_L (Pin 7/Pin 9): The CTRL_L pin sets the low level regulated output current. It is not recommended that the CTRL_L voltage be higher than the CTRL_H voltage.

SS (Pin 8/Pin 10): Soft-Start Pin. Place an external capacitor to ground to limit the regulated current during start-up conditions. The SS pin has a 5.5µA charging current. This pin controls both of the regulated inputs determined by CTRL_L and CTRL_H.

FB (Pin 10/Pin 12): Feedback Pin for Overvoltage Protection. The feedback voltage is 1V. Overvoltage/Open LED is sensed through the FB pin. When the feedback voltage exceeds 1.3V, the overvoltage lockout prevents switching and connects both output capacitors to discharge the inductor current.

$SENSE^+$ (Pin 11/Pin 13): $SENSE^+$ is the inverting input of the average current mode loop error amplifier. This pin is connected to the external current sense resistor, R_S. The voltage drop between $SENSE^+$ and $SENSE^-$ referenced to the voltage drop across an internal resistor produces the input voltages to the current regulation loop.

$SENSE^-$ (Pin 12/Pin 14): $SENSE^-$ is the noninverting input of the average current mode loop error amplifier. The reference current, based on CTRL_L or CTRL_H flows out of the pin to the output (LED) side of the sense resistor, R_S.

V_{CL} (Pin 13/Pin 15): V_{CL} provides the necessary compensation for the average current loop stability during low level current regulation. Typical compensation values are 15k to 80k for the resistor and 2nF to 10nF for the capacitor.

V_{CH} (Pin 14/Pin 16): V_{CH} provides the necessary compensation for the average current loop stability during high level current regulation. Typical compensation values are 15k to 80k for the resistor and 2nF to 10nF for the capacitor.

RT (Pin 15/Pin 17): A resistor to ground sets the switching frequency between 200kHz and 1MHz. When using the SYNC function, set the frequency to be 20% lower than the SYNC pulse frequency. This pin is current limited to 60µA. Do not leave this pin open.

SYNC (Pin 16/Pin 18): Frequency Synchronization Pin. This pin allows the switching frequency to be synchronized to an external clock. The R_T resistor should be chosen to operate the internal clock at 20% slower than the SYNC pulse frequency. The synchronization range is 240kHz to 1.2MHz. This pin should be grounded when not in use.

CTRL_SEL (Pin 17/Pin 19): The CTRL_SEL pin selects between the high current control, CTRL_H and the low current control, CTRL_L. When high, the V_{CH} pin is connected to the error amp output and the PWMGH gate signal is high. When low, the V_{CL} pin is connected to the error amp output and the PWMGL gate signal is high. This pin is used for current level dimming of the LED. This pin should be grounded when not in use.

PWM (Pin 18/Pin 20): The input pin for PWM dimming of the LED. When low, all switching is terminated and the output caps are disconnected. This pin should be pulled to V_{CC_INT} when not in use.

PWMGH (Pin 19/Pin 21): The PWMGH output pin drives the gate of an external FET to connect one of the switching regulator output capacitors to the load. The driver pull-up impedance is 3.2Ω and pull-down impedance is 1.75Ω.

PIN FUNCTIONS (QFN/TSSOP)

PWMGL (Pin 22/Pin 23): The PWMGL output pin drives the gate of an external FET to connect one of the switching regulator output capacitors to the load. The driver pull-up impedance is 3.2Ω and pull-down impedance is 1.75Ω.

HG (Pin 23/Pin 24): HG is the top FET gate drive signal that controls the state of the high side external power FET. The driver pull-up impedance is 2.3Ω and pull-down impedance is 1.3Ω.

SW (Pin 24/Pin 25): The SW pin is used internally as the lower rail for the floating high side driver. Externally, this node connects the two power FETs and the inductor.

CBOOT (Pin 25/Pin 26): The CBOOT pin provides a floating 5V regulated supply for the high side FET driver. An external Schottky diode is required from the V_{CC_INT} pin to the CBOOT pin to charge the C_{BOOT} capacitor when the switch pin is near ground.

LG (Pin 26/Pin 28): LG is the bottom FET gate drive signal that controls the state of the low side external power FET. The driver pull-up impedance is 2.5Ω and pull-down impedance is 1.3Ω.

V_{CC_INT} (Pin 27/Pin 1): A regulated 5V output for charging the C_{BOOT} capacitor. V_{CC_INT} also provides the power for the digital and switching subcircuits. Below 6V V_{IN}, tie this pin to the rail. V_{CC_INT} is current limited to ≈50mA. Shutdown operation disables the output voltage drive.

V_{IN} (Pin 28/Pin 3): Input Supply Pin. Must be locally bypassed with a 1µF low ESR capacitor to ground.

BLOCK DIAGRAM (QFN Package)

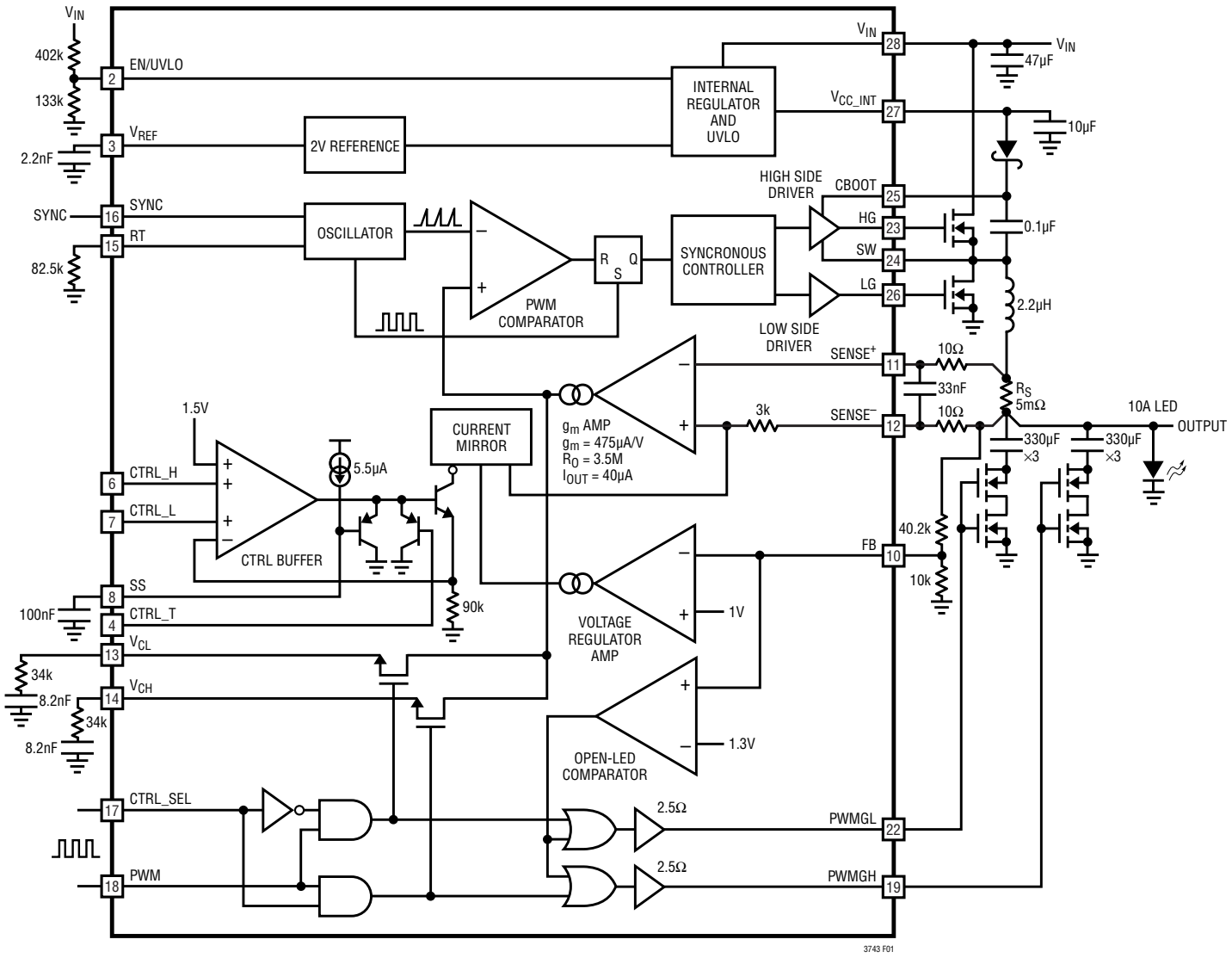


Figure 1. Block Diagram

OPERATION

The LT3743 utilizes fixed frequency, average current mode control to accurately regulate the inductor current, independently from the output voltage. This is an ideal solution for applications requiring a regulated current source including driving high current LEDs where the forward junction voltage can range from 2V to 6V with a dynamic resistance of 20mΩ to 40mΩ. The control loop will regulate the current in the inductor at an accuracy of 6%. For additional operation information, refer to the Block Diagram in Figure 1.

The control loop has two independent reference inputs, determined by the analog control pins, CTRL_H and CTRL_L. When the CTRL_SEL pin is low, the control loop uses the reference determined by the CTRL_L pin and when high, the loop uses the reference determined by the CTRL_H pin. The analog voltage at the CTRL_L and CTRL_H pins is buffered and produces a reference voltage across an internal resistor. The internal buffers have a 1.5V clamp on the output, limiting the analog control range of the CTRL_L and CTRL_H pins from 0V to 1.5V. The average current mode control loop uses the internal reference voltage to regulate the inductor current, as a voltage drop across the external sense resistor, R_S.

In many applications, a rapid transition between the two regulated current states is desirable to provide background LED color mixing for pure colors in an RGB projector or display. For this purpose, pulse width modulation dimming can be achieved with both the PWM and CTRL_SEL pins. When the PWM pin is low, the regulated current in the inductor is zero and both output capacitors are disconnected. When the PWM pin is high, and the CTRL_SEL pin is low, the regulated current in the inductor is determined by the analog voltage at the CTRL_L pin. When the PWM and CTRL_SEL pins are both high, the regulated current in the inductor is determined by the analog voltage at the CTRL_H pin.

The LT3743 uses a unique switched output capacitor topology and two independent compensation networks to transition between the two regulated current states in less than 2µs. When the CTRL_SEL pin is low and the PWM pin is high, the PWMGL output pin is high, switching in the output capacitor for the CTRL_L current level. The CTRL_L output capacitor stores the LED forward voltage drop when the control loop regulates the low current level. When the CTRL_SEL pin changes to the high state, a 150ns delay ensures that the output capacitors are not connected at the same time. After this delay, the output capacitor for the CTRL_H level is switched in when PWMGH goes high and immediately delivers current to the LED. The CTRL_H output capacitor has the voltage drop of the LED with the regulated current determined by the analog voltage at the CTRL_H pin. To achieve minimum transition delay, the inductor is precharged to 70% of the regulation current level just after the PWMGH pin goes high. Conversely, when the PWM pin goes low, the inductor is discharged to 70% of the low current level before normal switching at the low current level commences. The error amplifier for the average current mode control loop also has a common mode lockout that regulates the inductor current so that the error amplifier is never operated out of the common mode range. The common mode range is with an output voltage from 0V to 2V below the V_{IN} supply rail.

The overcurrent set point is equal to the high level regulated current level set by the CTRL_H pin with an additional 23mV offset between the $SENSE^+$ and $SENSE^-$ pins. The overcurrent is limited on a cycle-by-cycle basis; shutting switching down once the overcurrent level is reached. Overcurrent is not soft started.

The output voltage may be limited with a resistor divider from the output back to the FB pin. The reference at the FB pin is 1.0V. If the output voltage level is high enough to engage the voltage loop, the regulated inductor current will be reduced so that the output voltage is limited. If the voltage at the FB pin reaches 1.3V (30% higher than the regulation level), an internal open-LED flag is set, shutting down switching for 13µs and switching in both output capacitors to fully drain the inductor's current.

During start-up, the SS pin is held low until the first time the PWM pin goes high. Once the PWM signal goes high, the capacitor at the SS pin is charged with a 5.5µA current source. The internal buffers for the CTRL_L and CTRL_H signals are limited by the voltage at the SS pin, slowly ramping the regulated inductor current to the current determined by the voltage at the CTRL_H or CTRL_L pins.

APPLICATIONS INFORMATION

Programming Inductor Current

The analog voltage at the CTRL_L and CTRL_H pins is buffered and produces a reference voltage, V_{CTRL}, across an internal resistor. The regulated average inductor current is determined by:

$$I_O = \frac{V_{CTRL}}{30 \bullet R_S}$$

where R_S is the external sense resistor and I_O is the average inductor current, which is equal to the LED current. Figure 2 shows the LED current vs R_S. The maximum power dissipation in the resistor will be:

$$P_{RS} = \frac{(0.05V)^2}{R_S}$$

Table 1 contains several resistors values, the corresponding maximum current and power dissipation in the sense resistor. Figure 3 shows the power dissipation in R_S.

Table 1. Sense Resistor Values

MAXIMUM LED CURRENT (A)	RESISTOR, R_S (mΩ)	POWER DISSIPATION (W)
1	50	0.05
5	10	0.25
10	5	0.5
25	2	1.25

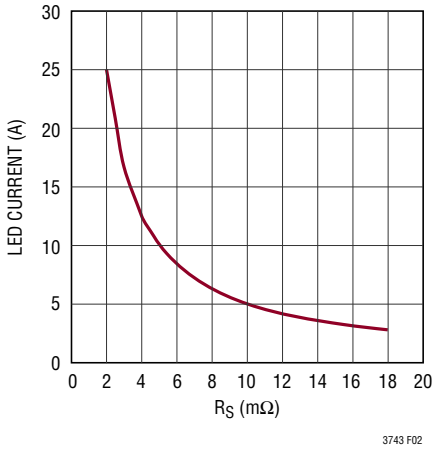


Figure 2. R_S Value Selection for LED Current

Inductor Selection

The recovery time between regulated states is critical to maintaining accurate control of the LED current. For this reason, sizing the inductor to have no less than 30% peak-to-peak ripple will provide excellent recovery time with reasonable ripple. The overcurrent set point is equal to the high level regulated current level set by the CTRL_H pin with an additional 23mV offset between the $SENSE^+$ and $SENSE^-$ pins. The saturation current for the inductor should be at least 20% higher than the maximum regulated current. The following equation sizes the inductor to achieve a reasonable recovery time while minimizing the inductor ripple:

$$L = \left(\frac{V_{IN} \bullet (V_F) - (V_F)^2}{0.2 \bullet f_S \bullet I_O \bullet V_{IN}} \right)$$

where V_F is the LED forward voltage drop, I_O is the maximum regulated current in the inductor and f_S is the switching frequency. Using this equation, the inductor will have approximately 10% ripple at maximum regulated current.

Table 2. Recommended Inductor Manufacturers

VENDOR	WEBSITE
Coilcraft	www.coilcraft.com
Sumida	www.sumida.com
Vishay	www.vishay.com
Wurth Electronics	www.we-online.com
NEC-Tokin	www.nec-tokin.com

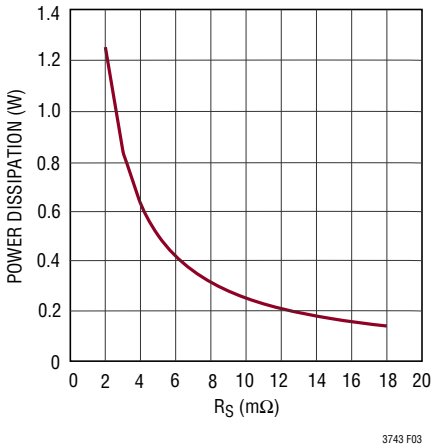


Figure 3. Power Dissipation in R_S

APPLICATIONS INFORMATION

Switching MOSFET Selection

When selecting switching MOSFETs, the following parameters are critical in determining the best devices for a given application: total gate charge (Q_G), on-resistance ($R_{DS(ON)}$), gate to drain charge (Q_{GD}), gate-to-source charge (Q_{GS}), gate resistance (R_G), breakdown voltages (maximum V_{GS} and V_{DS}) and drain current (maximum I_D). The following guidelines provide information to make the selection process easier.

Both of the switching MOSFETs need to have their maximum rated drain currents greater than the maximum inductor current. The following equation calculates the peak inductor current:

$$I_{MAX} = I_O + \left(\frac{V_{IN} \bullet \left(V_F + R_D I_O\right) - \left(V_F + R_D I_O\right)^2}{2 \bullet f_S \bullet L \bullet V_{IN}} \right)$$

where V_{IN} is the input voltage, L is the inductance value, V_F is the LED forward voltage drop, R_D is the dynamic series resistance of the LED, I_O is the regulated output current and f_S is the switching frequency. During MOSFET selection, notice that the maximum drain current is temperature dependant. Most data sheets include a table or graph of the maximum rated drain current vs temperature.

The maximum V_{DS} should be selected to be higher than the maximum input supply voltage (including transient) for both MOSFETs. The signals driving the gates of the switching MOSFETs have a maximum voltage of 5V with respect to the source. During start-up and recovery conditions, the gate drive signals may be as low as 3V. To ensure that the LT3743 recovers properly, the maximum threshold should be less than 2V. For a robust design, select the maximum V_{GS} greater than 7V.

Power losses in the switching MOSFETs are related to the on-resistance, $R_{DS(ON)}$; the transitional loss related to the gate resistance, R_G; gate-to-drain capacitance, Q_{GD} and gate-to-source capacitance, Q_{GS}. Power loss to the on-resistance is an Ohmic loss, $I^2 R_{DS(ON)}$, and usually dominates for input voltages less than ~15V. Power losses to the gate capacitance dominate for voltages greater than ~12V. When operating at higher input voltages, efficiency can be optimized by selecting a high side MOSFET with higher $R_{DS(ON)}$ and lower C_{GD}. The power loss in the high side MOSFET can be approximated by:

P_{LOSS} = (ohmic loss) + (transition loss)

$$P_{LOSS} \approx \left(\frac{\left(V_F + R_D I_O\right)}{V_{IN}} \bullet I_O^2 R_{DS(ON)} \bullet \rho_T \right) +$$

$$\left(\left(\frac{V_{IN} \bullet I_{OUT}}{5V} \right) \bullet \left(\left(Q_{GD} + Q_{GS}\right) \bullet \left(2 \bullet R_G + R_{PU} + R_{PD}\right) \right) \bullet f_S \right)$$

where ρ_T is a temperature-dependant term of the MOSFET's on-resistance. Using 70°C as the maximum ambient operating temperature, ρ_T is roughly equal to 1.3. R_{PD} and R_{PU} are the LT3743 high side gate driver output impedance, 1.3Ω and 2.3Ω respectively.

A good approach to MOSFET sizing is to select a high side MOSFET, then select the low side MOSFET. The trade-off between $R_{DS(ON)}$, Q_G, Q_{GD} and Q_{GS} for the high side MOSFET is shown in the following example. V_O is equal to 4V. Comparing two N-channel MOSFETs, with a rated V_{DS} of 40V and in the same package, but with 8× different $R_{DS(ON)}$ and 4.5× different Q_G and Q_{GD}:

M1: $R_{DS(ON)}$ = 2.3mΩ, Q_G = 45.5nC,
Q_{GS} = 13.8nC, Q_{GD} = 14.4nC, R_G = 1Ω

M2: $R_{DS(ON)}$ = 18mΩ, Q_G = 10nC,
Q_{GS} = 4.5nC, Q_{GD} = 3.1nC, R_G = 3.5Ω

Power loss for both MOSFETs is shown in Figure 4. Observe that while the $R_{DS(ON)}$ of M1 is eight times lower, the power loss at low input voltages is equal, but four times higher at high input voltages than the power loss for M2.

Another power loss related to switching MOSFET selection is the power lost to driving the gates. The total gate charge, Q_G, must be charged and discharged each switching cycle. The power is lost to the internal LDO within the LT3743. The power lost to the charging of the gates is:

$$P_{LOSS\_LDO} \approx (V_{IN} - 5V) \bullet (Q_{GLG} + Q_{GHG}) \bullet f_S$$

where Q_{GLG} is the low side gate charge and Q_{GHG} is the high side gate charge.

APPLICATIONS INFORMATION

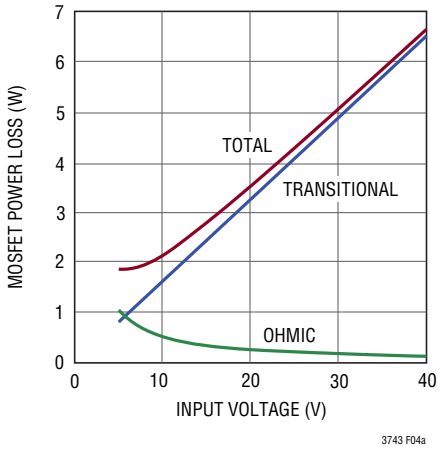


Figure 4a. Power Loss Example for M1

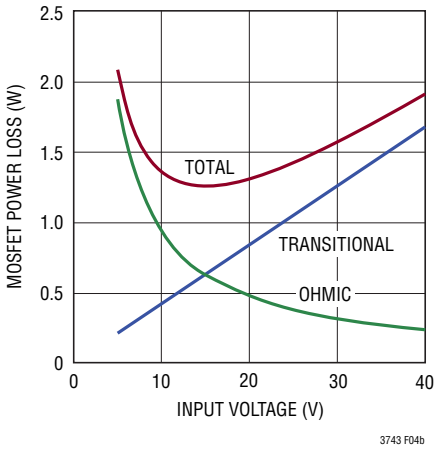


Figure 4b. Power Loss Example for M2

Figure 4

Whenever possible, utilize a switching MOSFET that minimizes the total gate charge to limit the internal power dissipation of the LT3743.

Table 3. Recommended Switching FETs

V_{IN} (V)	V_{OUT} (V)	I_D (A)	TOP FET	BOTTOM FET	MANUFACTURER
8	4	5-10	RJK0365DPA	RJK0330DPB	Renesas www.renesas.com
24	4	5	RJK0368DPA	RJK0332DPB	
24	2-4	20	RJK0365DPA	RJK0346DPA	
12	2-4	10	FDMS8680	FDMS8672AS	Fairchild www.fairchildsemi.com
36	4	20	Si7884BDP	SiR470DP	Vishay www.vishay.com
24	4	40	PSMN4R0-30YL	RJK0346DPA	NXP/Philips www.nxp.com

Input Capacitor Selection

The input capacitor should be sized at 4µF for every 1A of output current and placed very close to the high side MOSFET. A small 1µF ceramic capacitor should be placed near the V_{IN} and ground pins of the LT3743 for optimal noise immunity. The input capacitor should have a ripple current rating equal to half of the maximum output current.

It is recommended that several low ESR ceramic capacitors be used as the input capacitance. Use only type X5R or X7R capacitors as they maintain their capacitance over a wide range of operating voltages and temperatures.

Output Capacitor Selection

The output capacitors need to have very low ESR (equivalent series resistance) to allow the LED current to ramp quickly. A minimum of 50µF/A of load current should be used in most designs. The capacitors also need to be surge rated to the maximum output current. To achieve the lowest possible ESR, several low ESR capacitors should be used in parallel. Many applications benefit from the use of high density POSCAP capacitors, which are easily destroyed when exposed to overvoltage conditions. To prevent this, select POSCAP capacitors that have a voltage rating that is at least 50% higher than the regulated voltage

C_{BOOT} Capacitor Selection

The C_{BOOT} capacitor must be sized less than 220nF and more than 50nF to ensure proper operation of the LT3743. Use 220nF for high current switching MOSFETs with high gate charge.

APPLICATIONS INFORMATION

V_{CC_INT} Capacitor Selection

The bypass capacitor for the V_{CC_INT} pin should be larger than 5µF for stability and has no ESR requirement. It is recommended that the ESR be lower than 50mΩ to reduce noise within the LT3743. For driving MOSFETs with gate charges larger than 10nC, use 0.5µF/nC of total gate charge.

LED Current Dimming

The LT3743 provides the capability of traditional zero to full current PWM dimming as well as PWM dimming between two regulated LED current states. When the PWM signal is low, no switching occurs and the output capacitors are disconnected from ground. When PWM is high and CTRL_SEL is low, the inductor current is regulated to the low current state. In this state, the PWMGL signal is high, connecting the output capacitor for the low regulated current state. When PWM and CTRL_SEL are both high, the inductor current is regulated to the high current state. In this state, the PWMGH signal is high, connecting the output capacitor for the high regulated current state. The transition time between each of the regulated inductor currents is determined by the inductor size, V_{IN} and V_O. Due to the use of the switched output capacitors, the LED current will begin to flow within 130ns of the transition on the CTRL_SEL pin. Figure 8 shows the LED and inductor current waveforms with the various states of the control signals.

To adjust the regulated LED current for the two control states, an analog voltage is applied to the CTRL_L and CTRL_H pins. Figure 6 shows the regulated voltage across the sense resistor for control voltages up to 2V. Figure 7 shows the CTRL_L voltage created by a voltage divider from V_{REF} to ground. When sizing the resistor divider, please be aware that the V_{REF} pin is current limited to 500µA. Above 1.5V, the control voltage has no effect on the regulated LED current.

For the widest dimming range, use the highest switching frequency possible and lowest PWM frequency. For configuration with the maximum PWM range, please contact factory for optimized component selection.

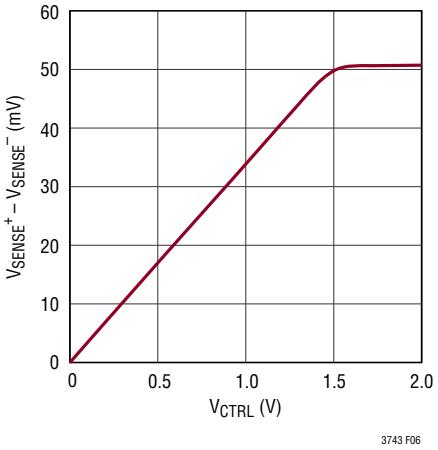


Figure 6. LED Current vs CTRL Voltage

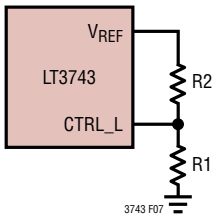


Figure 7. Analog Control of LED Current

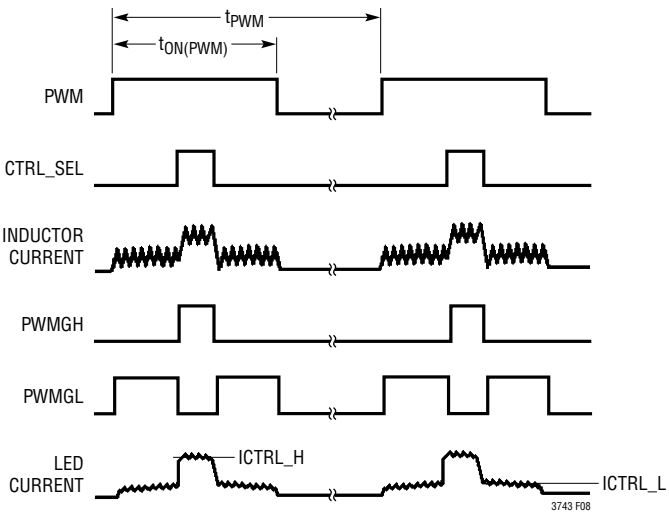


Figure 8. LED Current vs CTRL Voltage

APPLICATIONS INFORMATION

MOSFET Selection for the Switched Output Capacitors

The MOSFETs used for the switched-output capacitor need to also handle the maximum regulated current while the capacitor is charged. The output drivers on the PWMGH and PWMGL pins have a pull-up impedance of 3.2Ω and a pull-down impedance of 1.75Ω. This provides adequate gate drive for the PWM MOSFETs without the need for an additional gate driver. If the LED forward resistance and the difference between the two regulated currents is large enough, then two MOSFETs are required to prevent the body diode of the MOSFET from conducting and discharging the capacitor for the high current state. Figure 9 shows the output capacitor for the high current regulation state discharged with the body diode when a single MOSFET is used. Figure 10 shows the application circuit with a drain-to-drain configuration for the high current output capacitor. In this configuration, the body diode of the upper MOSFET blocks conduction and prevents discharge of the high current output capacitor.

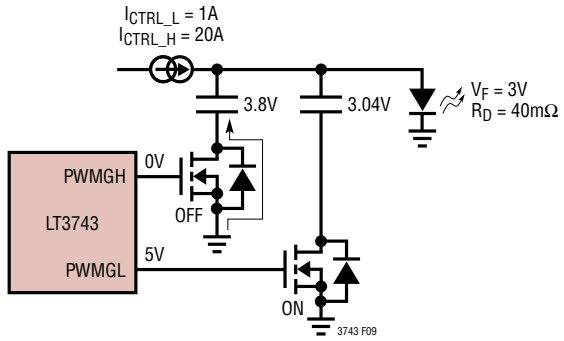


Figure 9. Body Diode of High Current FET Discharges the Output Capacitor

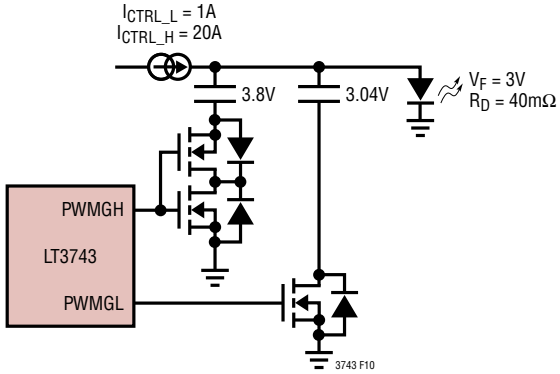


Figure 10. With a Drain-to-Drain Configuration, the Body Diode of the Top FET Blocks the Current Path That Would Discharge the High Current Output Capacitor

If the voltage between the low state and the high state is very large (greater than the threshold of the MOSFET) then the capacitor may once again be discharged. To account for this, choose a MOSFET that has a threshold greater than the voltage difference. If the voltage difference exceeds 1.5V, use the circuit shown in Figure 11. The circuit shown will keep the capacitor from discharging to a voltage difference of approximately 2V + V_{TH}.

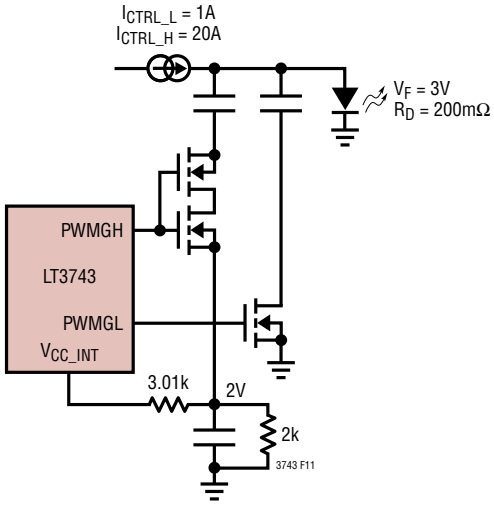


Figure 11. Application for Large Differences in Regulated Currents

Board and Interconnect Inductance

The board and interconnect inductance from the output capacitors to the load also determine the rate of change in load (LED) current. The rate of change in load current will be:

$$\frac{dI_L}{dt} = \frac{V_{HIGH} - V_{LOW}}{L_{BOARD}}$$

where dI_L/dt is the rate of change in the load current, V_{HIGH} is the output voltage when the inductor is regulated at the high level, and V_{LOW} is the output voltage when the inductor is regulated at the low state. When measuring the LED current do not use a current probe. The core material used in most probes adds inductance and slows the rise time of the LED current. Instead, when measuring the current, use a sense resistor.

APPLICATIONS INFORMATION

Voltage Regulation and Overvoltage Protection

The LT3743 uses the FB pin to regulate the output to a maximum voltage and to provide a high speed overvoltage lockout to avoid high voltage conditions that may damage expensive high current LEDs. The regulated output voltage is programmed using a resistor divider from the output and ground (Figure 12). When the output voltage exceeds 130% of the regulated voltage level (1.3V at the FB pin), the internal open-LED flag is set, terminating switching and forcing both PWMGL and PWMGH signals high. The regulated output voltage must be greater than 2V and is set by the equation:

$$V_{OUT} = 1V\left(1+\frac{R2}{R1}\right)$$

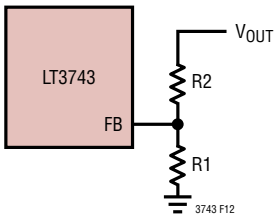


Figure 12. Output Voltage Regulation and Overvoltage Protection Feedback Connections

Soft-Start

Unlike conventional voltage regulators, the LT3743 utilizes the soft-start function to control the regulated inductor current. The charging current is 5.5µA and reduces the regulated current for both the high and low regulated current states. The SS pin is latched in a discharge state until the first PWM pulse and is reset by UVLO and thermal shutdown.

Programming Switching Frequency

The LT3743 has an operational switching frequency range between 200kHz and 1MHz. This frequency is programmed with an external resistor from the RT pin to ground. Do not leave this pin open under any condition. The RT pin is also current limited to 60µA. See Table 4 and Figure 13 for resistor values and the corresponding switching frequencies.

The internal power consumption of the LT3743 is determined by the switching frequency, V_{IN}, and the gate charge, Q_G of the external switching MOSFETs selected. The 4mm × 5mm QFN package has a θ_{JA} of 35°C/W. The following equation calculates the maximum switching frequency to avoid current limit and thermal shutdown at a given ambient operating temperature, T_A:

$$f_S \le \frac{(163°C - T_A)}{(35°C/W)\bullet(V_{IN} - 5V)\bullet(Q_{GHG} + Q_{GLG})}$$

$$f_S \le \frac{60mA}{(Q_{GLG} + Q_{GHG})}$$

Since the regulated output current flowing into the LED may be very large, the switching frequency needs to be carefully considered. Higher switching frequencies will reduce the large size of high saturation current inductors, while reducing efficiency and increasing power loss within the LT3743.

Table 4. Switching Frequency

SWITCHING FREQUENCY (MHz)	R_T (kΩ)
1	40.2
0.750	53.6
0.5	82.5
0.3	143
0.2	221

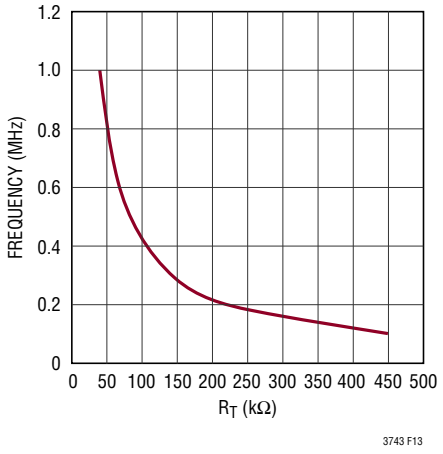


Figure 13. Frequency vs R_T Resistance

APPLICATIONS INFORMATION

Thermal Shutdown

The internal thermal shutdown within the LT3743 engages at 163°C and terminates switching, resets soft-start and shuts down the PWMGL and PWMGH drivers. When the part has cooled to 155°C, the internal reset is cleared and soft-start is allowed to charge once the PWM signal is asserted.

Switching Frequency Synchronization

The nominal switching frequency of the LT3743 is determined by the resistor from the RT pin to ground and may be set from 200kHz to 1MHz. The internal oscillator may also be synchronized to an external clock through the SYNC pin. The external clock applied to the SYNC pin must have a logic low below 0.3V and a logic high higher than 1.25V. The input frequency must be 20% higher than the frequency determined by the resistor at the RT pin. Input signals outside of these specified parameters will cause erratic switching behavior and subharmonic oscillations. The synchronization range is 240kHz to 1.2MHz. Synchronization is tested at 500kHz with a 200k R_T resistor. Operation under other conditions is guaranteed by design. When synchronizing to an external clock, please be aware that there will be a fixed delay from the input clock edge to the edge of switch. The SYNC pin must be grounded if the synchronization to an external clock is not required. When SYNC is grounded, the switching frequency is determined by the resistor at the RT pin.

Shutdown and UVLO

The LT3743 has an internal UVLO that terminates switching, resets all synchronous logic, and discharges the soft-start capacitor for input voltages below 4.2V. The LT3743 also has a precision shutdown at 1.55V on the EN/UVLO pin. Partial shutdown occurs at 1.55V and full shutdown is guaranteed below 0.5V with <1µA I_Q in the full shutdown state. Below 1.55V, an internal current source provides 5.5µA of pull-down current to allow for programmable UVLO hysteresis. The following equations determine the voltage divider resistors for programming the UVLO voltage and hysteresis as configured in Figure 14.

$$R2 = \frac{V_{HYST}}{5.5\mu A} - \frac{V_{UVLO}}{66\mu A}$$

$$R1 = \left(\frac{1.55V \bullet R2}{V_{UVLO} - 1.55V} \right)$$

The EN/UVLO pin as an absolute maximum voltage of 6V. To accommodate the largest range of applications, there is an internal Zener diode that clamps this pin. For applications where the supply range is greater than 4:1, size R2 greater than 375k.

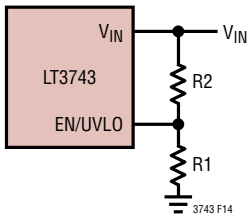


Figure 14. UVLO Configuration

LED Current Derating Using the CTRL_T Pin

The LT3743 is designed specifically for driving high current LEDs. Most high current LEDs require derating the maximum current based on operating temperature to prevent damage to the LED. In addition, many applications have thermal limitations that will require the regulated current to be reduced based on LED and/or board temperature. To achieve this, the LT3743 uses the CTRL_T pin to reduce the effective regulated current in the LED for both the high and low control currents. While CTRL_H and CTRL_L program the regulated current in the LED, CTRL_T can be configured to reduce this regulated current based on the analog voltage at the CTRL_T pin. The LED/board temperature derating is programmed using a resistor divider with a temperature dependant resistance (Figure 15). When the board/LED temperature rises, the CTRL_T voltage will decrease. To reduce the regulated current, the CTRL_T voltage must be lower than voltage at the CTRL_L and CTRL_H pins.

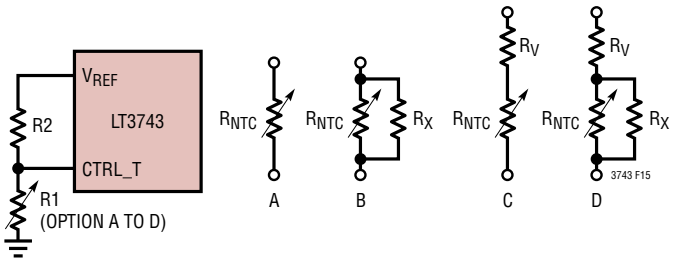


Figure 15. LED Current Derating vs Temperature Using NTC Resistor

APPLICATIONS INFORMATION

Average Current Mode Control Compensation

The use of average current mode control allows for precise regulation of the inductor and LED currents. Figure 16 shows the average current mode control loop used in the LT3743, where the regulation current is programmed by a current source and a 3k resistor.

To design the compensation network, the maximum compensation resistor needs to be calculated. In current mode controllers, the ratio of the sensed inductor current ramp to the slope compensation ramp determines the stability of the current regulation loop above 50% duty cycle. In the same way, average current mode controllers require the slope of the error voltage to not exceed the PWM ramp slope during the switch off-time.

Since the closed-loop gain at the switching frequency produces the error signal slope, the output impedance of the error amplifier will be the compensation resistor, R_C.

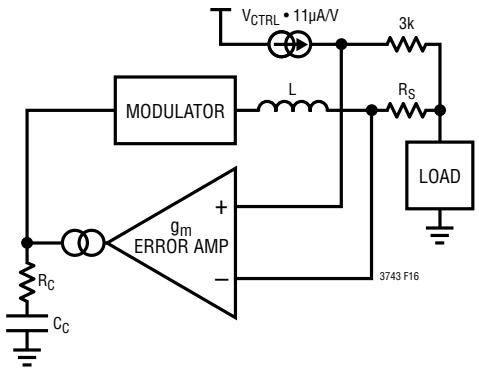


Figure 16. LT3743 Average Current Mode Control Scheme

Use the following equations as a good starting point for compensation component sizing:

$$R_C = \frac{f_S \bullet L \bullet 1000V}{V_O \bullet R_S}\ [\Omega],\ C_C = \frac{0.002}{f_S}[F]$$

where f_S is the switching frequency, L is the inductance value, V_{IN} is the input voltage and R_S is the sense resistor. For most LED applications, a 4.7nF compensation capacitor is adequate and provides excellent phase margin with optimized bandwidth. Please refer to Table 6 for recommended compensation values.

For applications where the load is not an LED, please call the factory for additional compensation assistance.

Board Layout Considerations

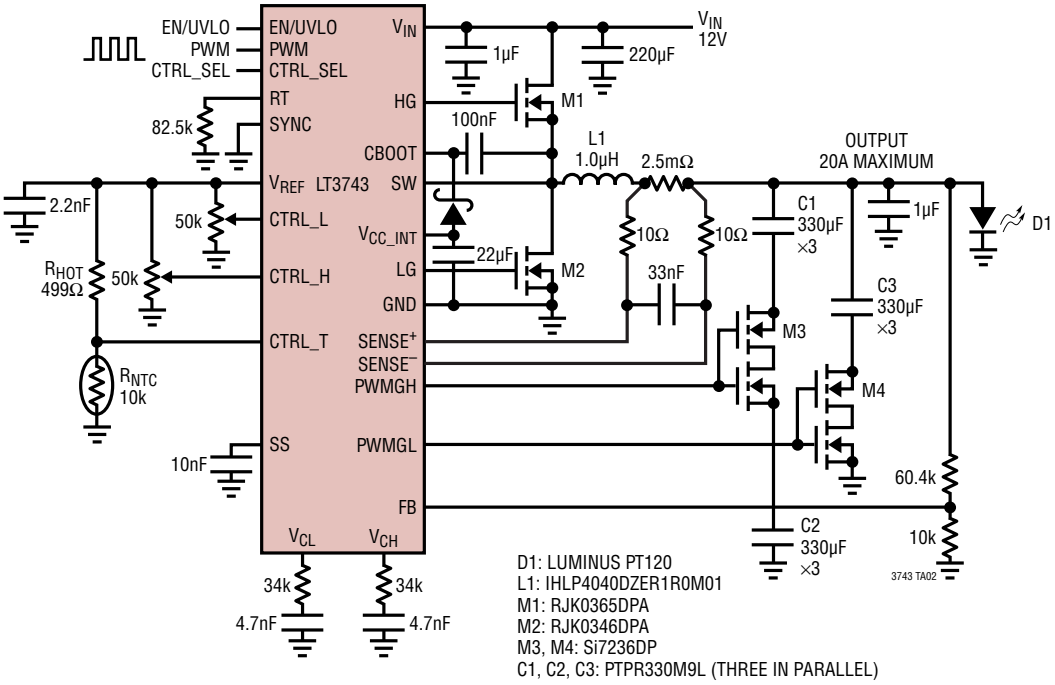
Average current mode control is relatively immune to the switching noise associated with other types of control schemes. Placing the sense resistor as close as possible to the SENSE$^+$ and SENSE$^-$ pins avoids noise issues and ensures the fastest LED current transition time. For currents exceeding 5A, use 10Ω resistors in-series with SENSE$^+$ and SENSE$^-$, with a 33nF capacitor placed as close as possible to the SENSE$^+$ and SENSE$^-$ pins. Utilizing a good ground plane underneath the switching components will minimize interplane noise coupling. To dissipate the heat from the switching components, increase the area of the switching node as much as possible without negatively affecting the radiated noise. The interconnect inductance and resistance between the output capacitors and the LED load directly impacts the rise time of the load current. To reduce the inductance and resistance, make the traces as wide as physically possible and minimize the trace length.

Table 6. Recommended Compensation Values

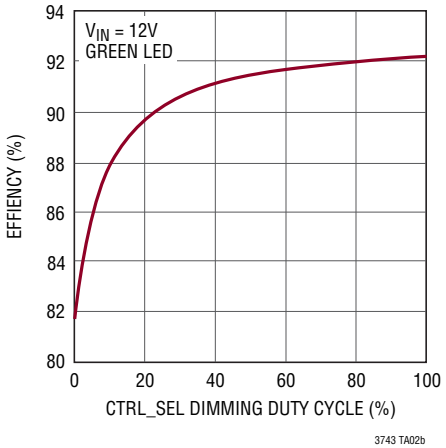
V_{IN} (V)	V_O (V)	I_L (A)	f_{SW} (MHz)	L (µH)	R_S (mΩ)	R_C (kΩ)	C_C (nF)
12	4	5	0.5	1.5	5	47.5	4.7
12	4	10	0.5	1.5	5	47.5	4.7
12	5	20	0.25	1.8	2.5	38.3	8.2
24	4	2	0.5	1.0	2.5	52.3	4.7
24	4	20	0.5	1.0	2.5	52.3	4.7

TYPICAL APPLICATIONS

12V, 20A LED Driver

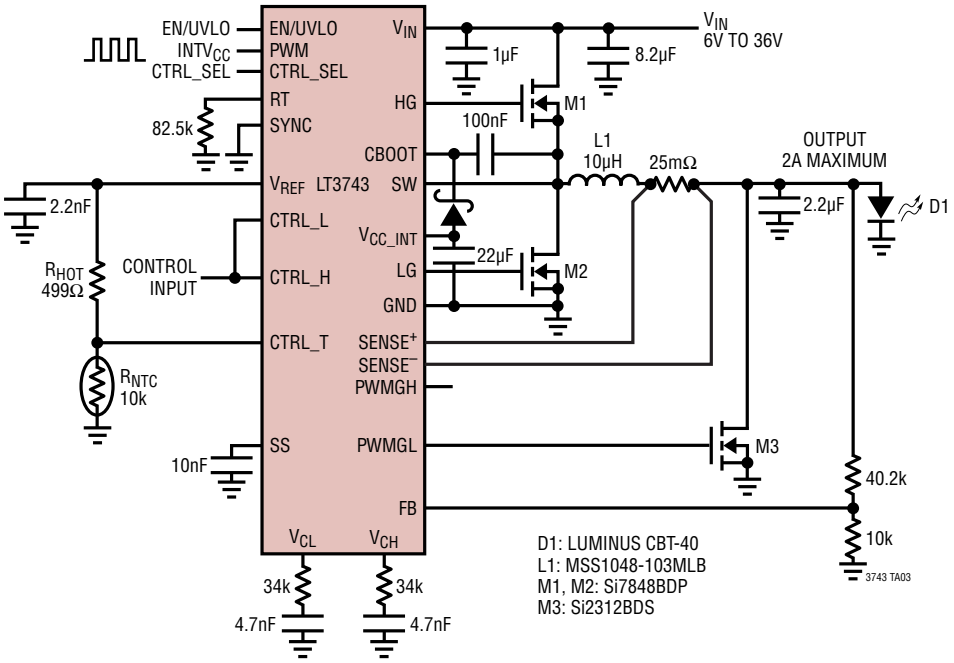


Efficiency (Stepping from 2A to 20A)

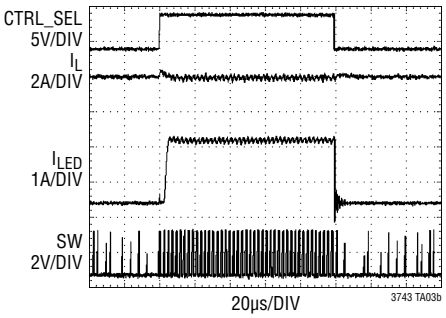


TYPICAL APPLICATIONS

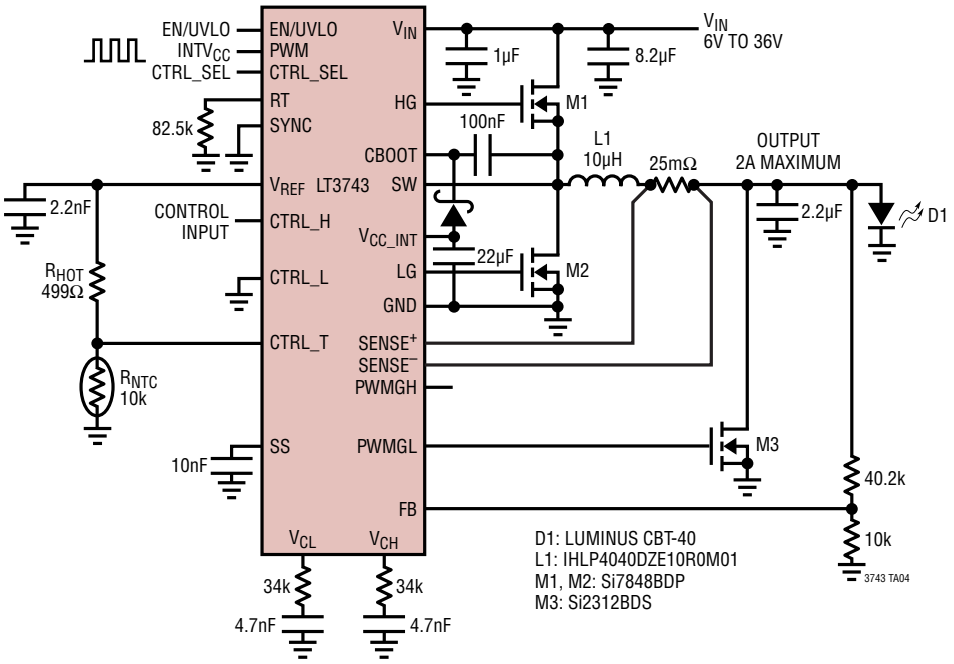
6V to 36V, 2A LED Driver With Shunted Output



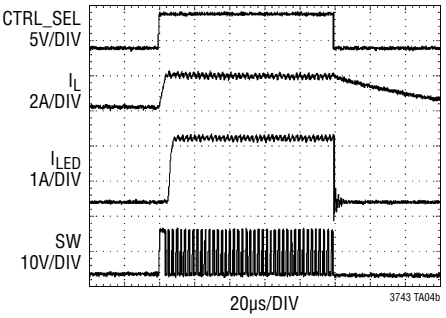
Shunted Output with CTRL_H Equal to CTRL_L



6V to 36V, 2A LED Driver With Current Limited Shunted Output

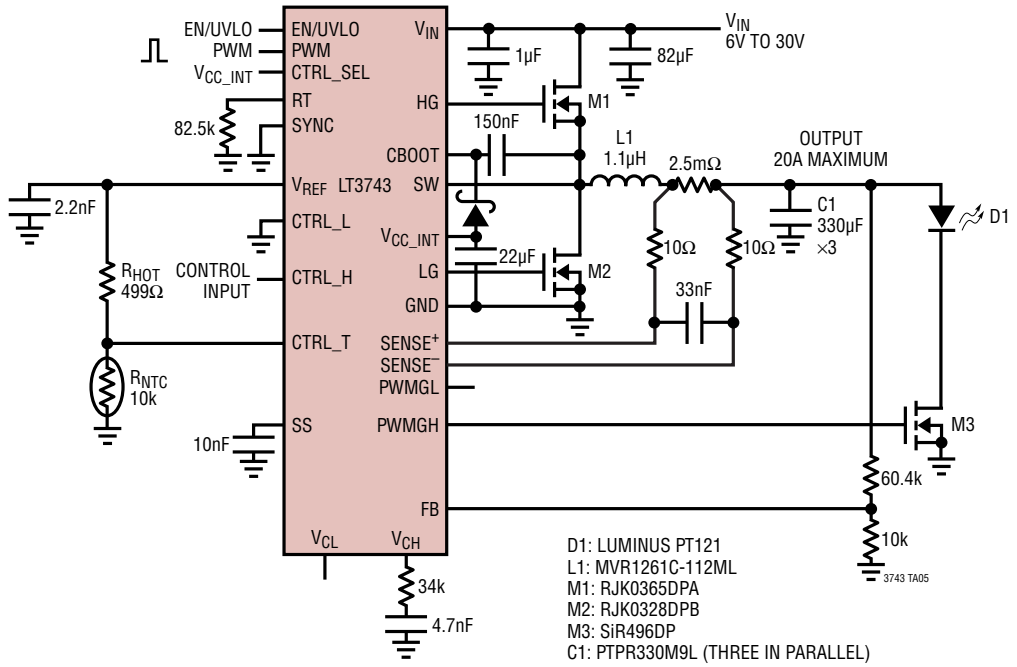


Shunted Output with CTRL_L at GND

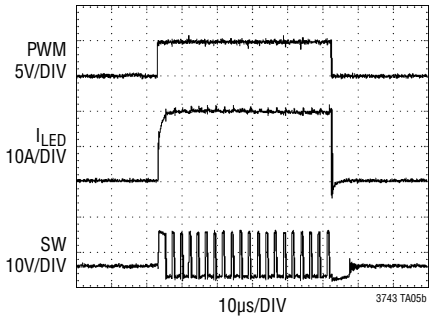


TYPICAL APPLICATIONS

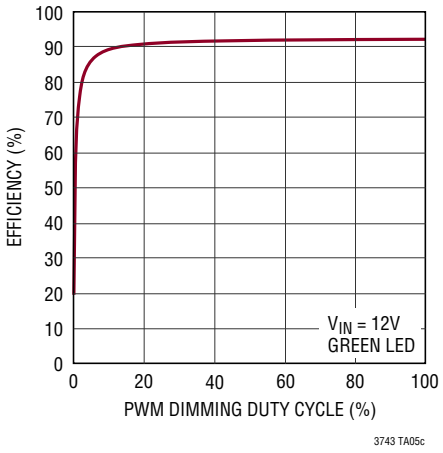
6V to 30V, 20A LED Driver with Switched Cathode



Switched Cathode PWM Dimming (100:1) 0A to 20A

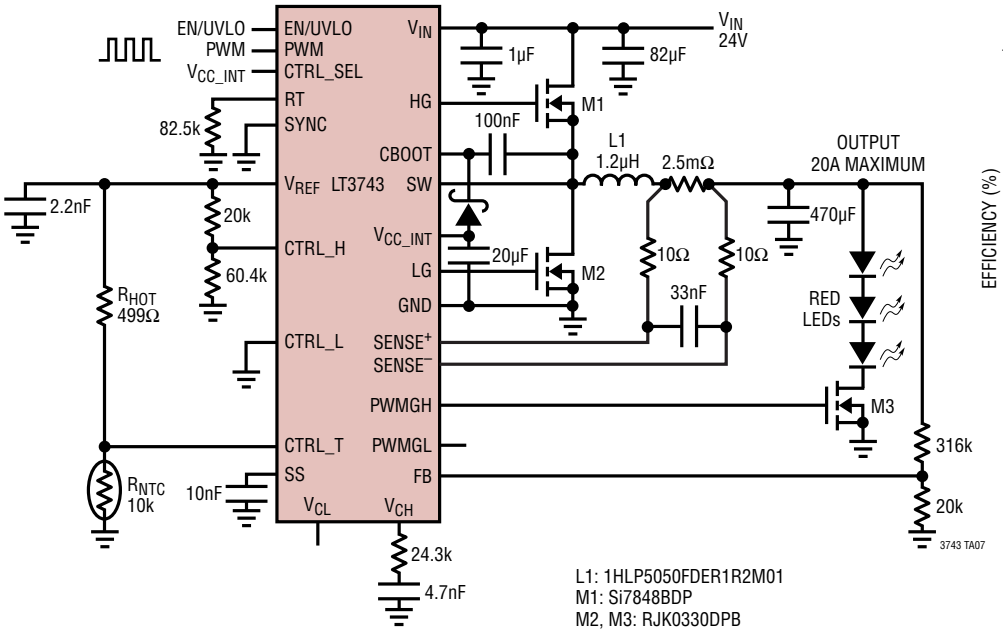


0A to 20A Efficiency



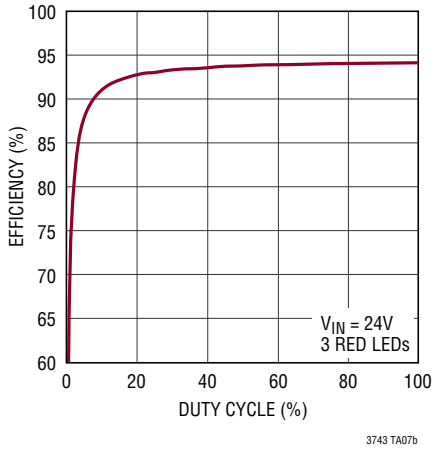
TYPICAL APPLICATIONS

24V, 20A 3-LED Driver



L1: 1HLP5050FDER1R2M01
M1: Si7848BDP
M2, M3: RJK0330DPB

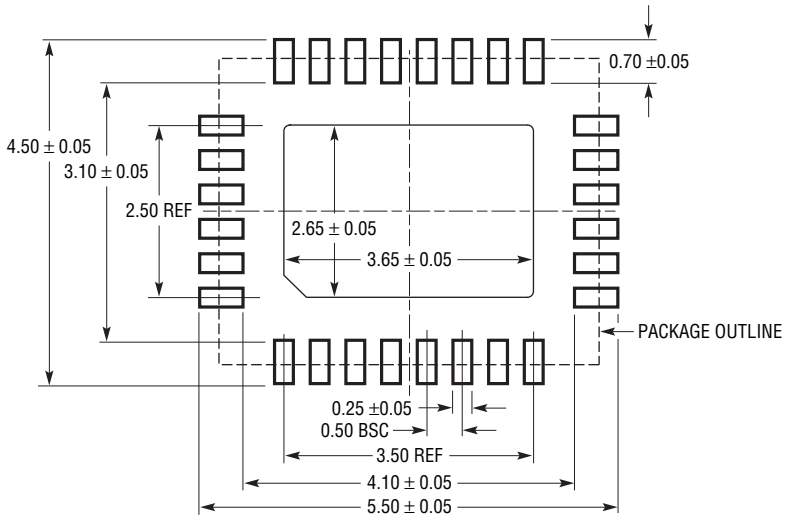
Efficiency



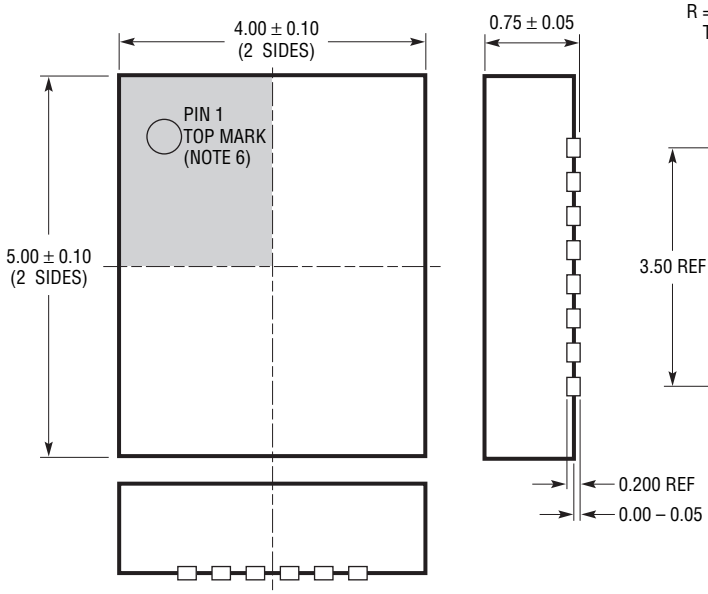
PACKAGE DESCRIPTION

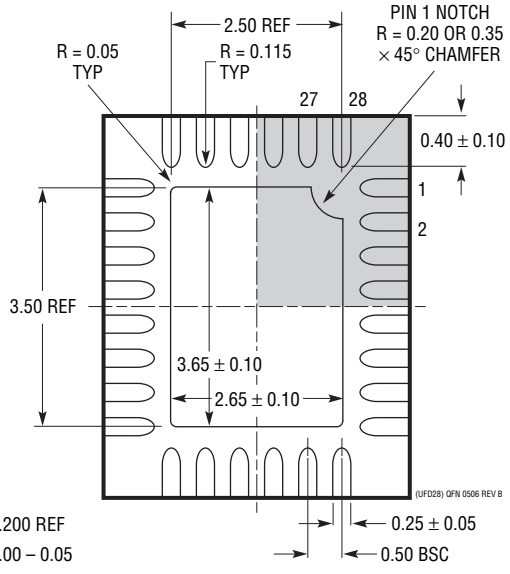
Please refer to http://www.linear.com/product/LT3743#packaging for the most recent package drawings.

UFD Package
28-Lead Plastic QFN (4mm × 5mm)
(Reference LTC DWG # 05-08-1712 Rev B)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED





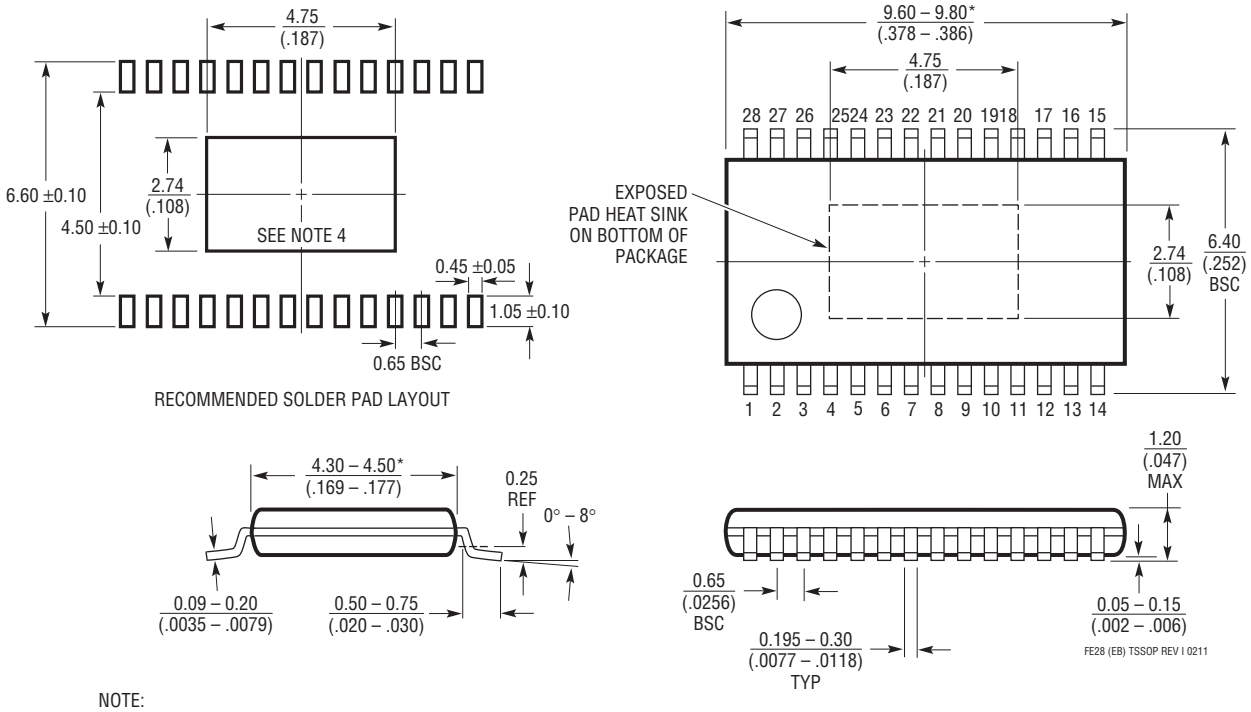
BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WXXX-X).
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LT3743#packaging for the most recent package drawings.

FE Package
28-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1663 Rev I)
Exposed Pad Variation EB



NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN MILLIMETERS (INCHES)
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	2/10	Revised Features and Typical Application	1
		Updated Electrical Characteristics values	3, 4
		Revised values on curves G32 and G33 in the Typical Performance Characteristics section	8
		Revised the Block Diagram	11
		Changed value in equation and made minor text edit in the Inductor Selection section	13
		Revised Table 4 values	18
		Added text to Average Current Mode Control Compensation and Board Layout Considerations sections in the Applications Information section	20
		Revised all Typical Applications drawings	21 to 25, 28
B	8/10	Updated Electrical Characteristics values and conditions	3, 4
		Revised Pin Functions	9, 10
		Revised Block Diagram	11
		Changed soft-start current in Operation section	12
		Revised units for M1 and M2 equations	14
		Removed 0.1MHz switching frequency from Table 4	18
		Added text to Switching Frequency Synchronization, Shutdown and UVLO sections in the Applications Information section	19
		Corrected M2 and M3 part numbers on Typical Applications drawings	24, 28
C	9/11	Revised Feedback Regulation Voltage listing in Electrical Characteristics section	3
D	11/12	Clarified V_{CL} and V_{CH} pins	1, 2, 9, 11, 21-24
		Clarified Regulated Current vs V_{FB} graph	6
		Clarified Minimum Off-Time graph	7
E	10/15	Added patent number	1
		Revised UVLO Hysteresis Equation	19
		Corrected typo in Block Diagram	11