High Current Synchronous Step-Down LED Driver

FEATURES

- **Ideal for Driving Up to 40A LEDs**
- **Up to 3000:1 PWM Dimming**
- **20:1 Analog Dimming**
- **±3% Current Regulation Accuracy**
- **±3% Voltage Regulation Accuracy**
- Unique Inverting Buck-Boost Topology Allows Grounded Heat Sink to Be Used for RGB LEDs
- 3.3V to 36V Input Voltage Range
- Peak Current Mode with DC LED Current Sensing
- Open and Shorted LED Protection and Fault Reporting
- Floating LED Driver Allows Single Power Solution to Drive Multicolor LEDs or Single LED with Three Different Regulated Currents
- Thermally Enhanced 5mm × 6mm QFN 36-Lead Package

APPLICATIONS

- LED Driver for DLP Projectors
- Heads-Up Displays
- High Power LED

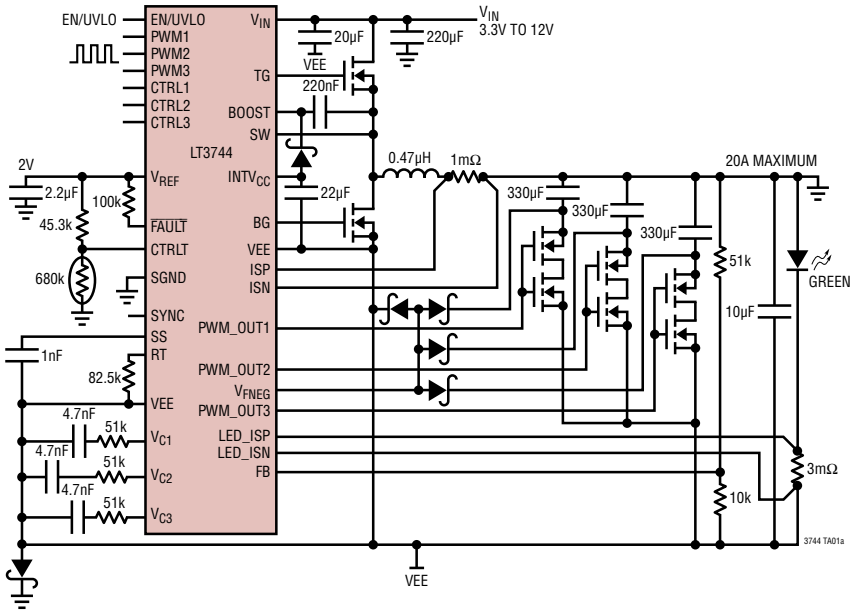
DESCRIPTION

The LT®3744 is a fixed frequency synchronous step-down DC/DC controller designed to drive a LED load at up to 20A continuous or 40A pulsed. The peak current mode controller will maintain ±3% LED current regulation over a wide output voltage range, from VEE to V_{IN}. By allowing VEE to float to negative voltages, several LEDs in series can be driven from a single Li-Ion battery with a simple, single step-down output stage. PWM dimming is achieved with the PWM pins. The regulated LED current is set with analog voltages at the CTRL pins. Regulated voltage and overvoltage protection are set with a voltage divider from the output to the FB pin. The switching frequency is programmable from 100kHz to 1MHz through an external resistor on the RT pin.

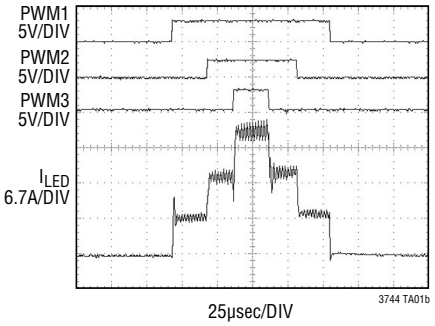
Additional features include an accurate external reference voltage, a control input for thermally derating regulation current, an accurate EN/UVLO pin, an open-drain output fault flag, OVLO, frequency synchronization, and thermal shutdown.

TYPICAL APPLICATION

LED Driver for DLP Projectors



LED Current Waveforms (2000:1) 0A to 6.7A to 13.3A to 20A



ABSOLUTE MAXIMUM RATINGS (Note 1)

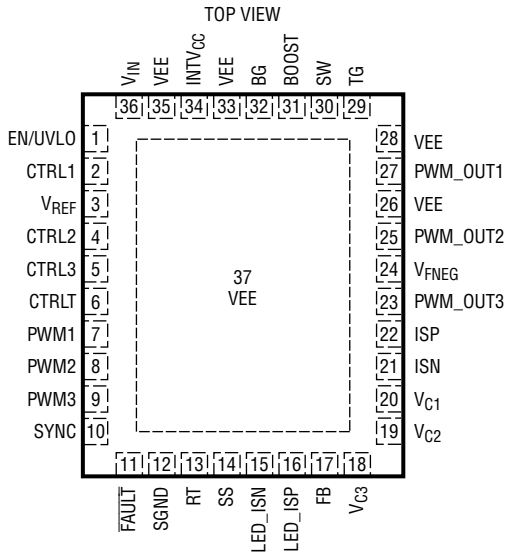
Relative to VEE (Tested with VEE = 0V and SGND = 20V):

V_{IN} 36V
EN/UVLO 36V
CTRL1, CTRL2, CTRL3 ..... 23V
CTRLT 23V
ISP, ISN 36V
LED_ISP, LED_ISN 3V
V_{C1}, V_{C2}, V_{C3} 3V
V_{FNEG} ..... –15V to 3V
BOOST 41V
$\overline{FAULT}$, SYNC 23V
PWM1, PWM2, PWM3 ..... 25V
FB 3V
SW 36V
$INTV_{CC}$, RT, BG, TG, PWM_OUT1, PWM_OUT2, PWM_OUT3, V_{REF}, SS ..... Note 4

Relative to SGND (Tested with VEE = 0V and SGND = 0V):

V_{IN} 36V
EN/UVLO 36V
CTRL1, CTRL2, CTRL3 ..... 3V
CTRLT 3V
ISP, ISN 36V
LED_ISP, LED_ISN 3V
V_{C1}, V_{C2}, V_{C3} 3V
V_{FNEG} ..... –15V to 3V
BOOST 41V
$\overline{FAULT}$, SYNC 3V
PWM1, PWM2, PWM3 ..... 5V
FB 3V
SW 36V
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



UHE PACKAGE
36-LEAD (5mm × 6mm) PLASTIC QFN

θ_{JA} = 34°C/W, θ_{JC} = 3°C/W
EXPOSED PAD (PIN 37) IS VEE, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3744EUHE#PBF	LT3744EUHE#TRPBF	3744	36-Lead (5mm × 6mm) Plastic QFN	–40°C to 125°C
LT3744IUHE#PBF	LT3744IUHE#TRPBF	3744	36-Lead (5mm × 6mm) Plastic QFN	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Consult LTC Marketing for information on nonstandard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, $V_{EN/UVLO}$ = 2V, SGND = VEE = 0V unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range	(Note 2)		3.3		36	V
V_{IN} Pin Quiescent Current (Note 3) Non-Switching Operation Shutdown Mode	 $V_{EN/UVLO}$ = 2V, Not Switching $V_{EN/UVLO}$ = 0V	 ●		 2.2	 2.6 1	 mA µA
EN/UVLO Pin Threshold (Rising)			1.225	1.3	1.375	V
EN/UVLO Hysteresis				–65		mV
EN/UVLO Pin Current	EN/UVLO = 1.0V			4.8		µA
PWM1, PWM2, PWM3 Input High	Referenced to SGND		2.0			V
PWM1, PWM2, PWM3 Input Low	Referenced to SGND				0.8	V
PWM1, PWM2, PWM3 Pin Currents	PWM1, PWM2, PWM3 = 2.0V			100		nA
CTRL1, CTRL2, CTRL3 Control Range	Referenced to SGND		0		1.5	V
CTRL1, CTRL2, CTRL3, Pin Currents	CTRL1, CTRL2, CTRL3, = 1.5V			100		nA
CTRLT Pin Current	CTRLT = 1.5V			100		nA
Reference						
Reference Voltage (V_{REF} Pin)	Referenced to SGND	●	1.96	2	2.04	V
LED and Inductor Current Sensing						
Full Range LED_ISP to LED_ISN	CTRL1 = 1.5V, PWM1 = 2V, PWM2 and PWM3 = 0V	●	58.2	60.0	61.8	mV
Current Regulation Accuracy, Full Range		●	–3.0		3.0	%
1/20 Range LED_ISP to LED_ISN	CTRL1 = 0.075V, PWM1 = 2V, PWM2 and PWM3 = 0V	●	2	3	4	mV
LED_ISP and LED_ISN Pin Current	CTRL1 = 1.5V, PWM1 = 2V, PWM2, PWM3, LED_ISP and LED_ISN = 0V			65		µA
ISN and ISP Pin Current at 0V	ISN = ISP = 0V, PWM1 = 2V, PWM2 and PWM3 = 0V			390		µA
ISN and ISP Pin Current at 0V, Dimming	ISN = ISP = 0V, PWM1 = 0V, PWM2 and PWM3 = 0V			1		µA
ISN and ISP Pin Current at 5V	ISN = ISP = 5V, PWM1 = 2V, PWM2 and PWM3 = 0V			10		µA
ISN and ISP Pin Current at 5V, Dimming	ISN = ISP = 5V, PWM1 = 0V, PWM2 and PWM3 = 0V			1		µA
OC Inductor Threshold, Rising (ISP-ISN)	ISN = 3V			110		mV
OC Inductor Threshold, Falling (ISP-ISN)	ISN = 3V			75		mV
Internal V_{CC} Regulator ($INTV_{CC}$ Pin)						
Regulation Voltage			4.75	5	5.25	V
Current Limit ($INTV_{CC}$ Short)	$INTV_{CC}$ = 0V			50		mA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, $V_{EN/UVLO}$ = 2V, SGND = VEE = 0V unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
NMOS FET Drivers						
Non-Overlap Time TG to BG				50		ns
Non-Overlap Time BG to TG				50		ns
Minimum On-Time BG	(Note 3)			50		ns
Minimum On-Time TG	(Note 3)			160		ns
Top Gate Driver Switch R_{ON} Gate Pull Up Gate Pull Down	$V_{BOOST} - V_{SW}$ = 5V			 3 1.5		 Ω Ω
Bottom Gate Driver Switch R_{ON} Gate Pull Up Gate Pull Down	V_{INTVCC} = 5V			 2.5 1.5		 Ω Ω
PWM Out Drivers						
PWM_OUT Switch R_{ON} Gate Pull Up Gate Pull Down	V_{INTVCC} = 5V, V_{FNEG} = –15V			 5 1.65		 Ω Ω
PWMX High To PWM_OUTX High Delay PWMX Low To PWM_OUTX Low Delay				175 80		ns ns
Oscillator						
Switching Frequency Range			100		1000	kHz
RT Pin Current Limit				66		µA
SYNC Input High	Referenced to SGND		2.0			V
SYNC Input Low	Referenced to SGND				0.8	V
SYNC Pin Current	SYNC = 2.0V			25		nA
SYNC Range	Tested at 190kHz and 1.1MHz with R_T = 422kΩ		90		900	kHz
Switching Frequency						
f_{SW}	R_T = 40.2kΩ R_T = 422kΩ	● 	950 95	1000 104	1050 120	kHz kHz
Soft-Start						
Charge Current	PWM1 = 2V, SS, PWM2 and PWM3 = 0V	●	4.8	5	5.2	µA
Fault						
Lower Fault Falling V_{FB} Threshold		●	240	250	260	mV
Lower Fault Rising V_{FB} Hysteresis				30		mV
Upper Fault Rising V_{FB} Threshold		●	1.06	1.100	1.14	V
Upper Fault Falling V_{FB} Hysteresis				–30		mV
Fault Voltage Low	I_{FAULT} = 2mA			0.1		V
Fault Leakage Current				50		nA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, $V_{EN/UVLO}$ = 2V, SGND = VEE = 0V unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Voltage Regulation Amplifier						
FB Pin Current	V_{FB} = 1.2V			1.2		µA
g_m				600		µA/V
Feedback Regulation Voltage		●	1.169	1.205	1.241	V
LED Current Control Loop g_m Amplifier						
Input Bias Current (LED_ISP and LED_ISN)	CTRL1 = 1.5V, PWM1 = 2V, PWM2, PWM3, LED_ISP and LED_ISN = 0V			65		µA
Output Impedance				25		MΩ
g_m				200		µA/V
Differential Gain				5		kV/V
C/10 Comparator						
Falling Threshold	LED_ISN = 0V, Threshold = LED_ISP-LED_ISN, CTRL1 = CTRL2 = CTRL3 = 2V		4.0	6	8.0	mV
Rising Hysteresis	LED_ISN = 0V, Threshold = LED_ISP-LED_ISN, CTRL1 = CTRL2 = CTRL3 = 2V			3.0		mV

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for an extended periods may affect device reliability and lifetime.

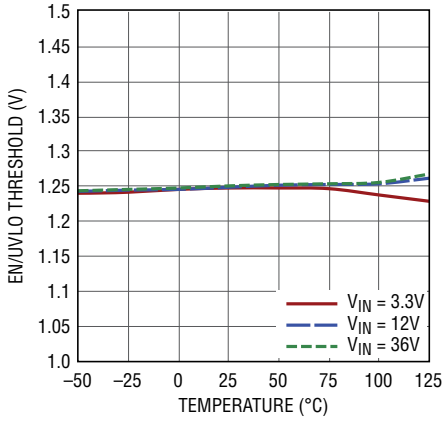
Note 2: The LT3744E is guaranteed to meet performance specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT3744I is guaranteed to meet performance specifications over the –40°C to 125°C operating junction temperature range.

Note 3: The minimum on and off times are guaranteed by design and are not tested.

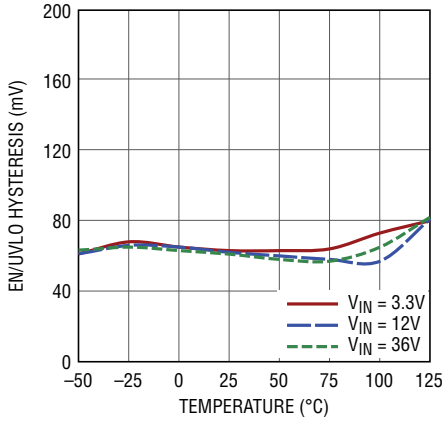
Note 4: Do not apply a positive or negative voltage to $INTV_{CC}$, RT, V_{REF}, SS, TG, BG, PWM_OUT1, PWM_OUT2, or PWM_OUT3 pins, otherwise permanent damage may occur.

TYPICAL PERFORMANCE CHARACTERISTICS

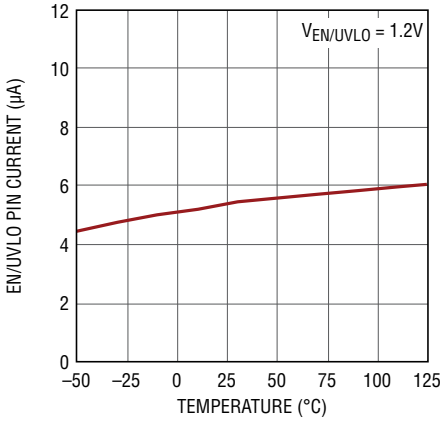
EN/UVLO Threshold (Falling)



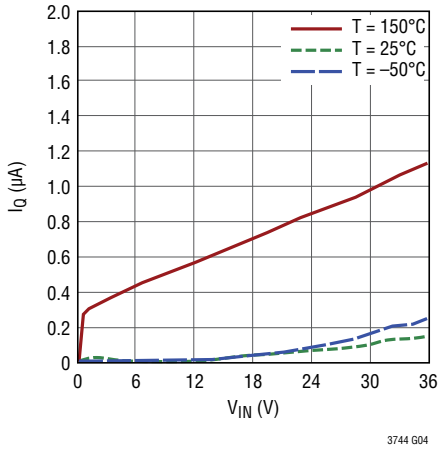
EN/UVLO Hysteresis



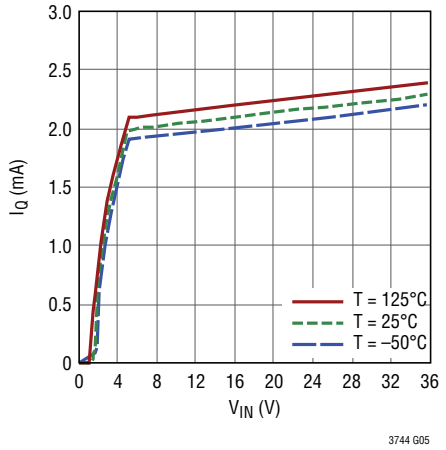
EN/UVLO Pin Current



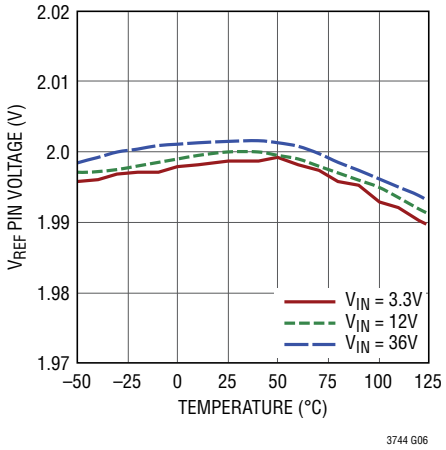
I_Q in Shutdown



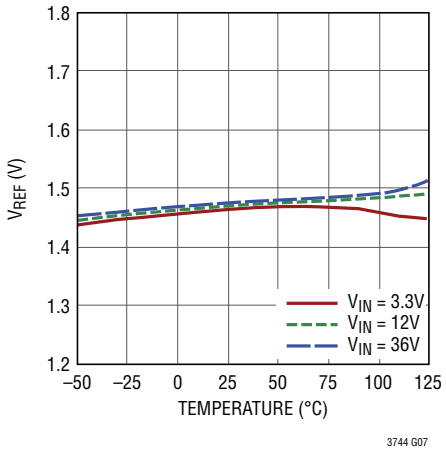
Quiescent Current (Non-Switching)



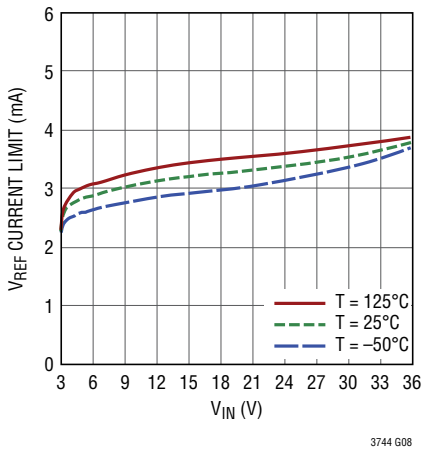
V_{REF}



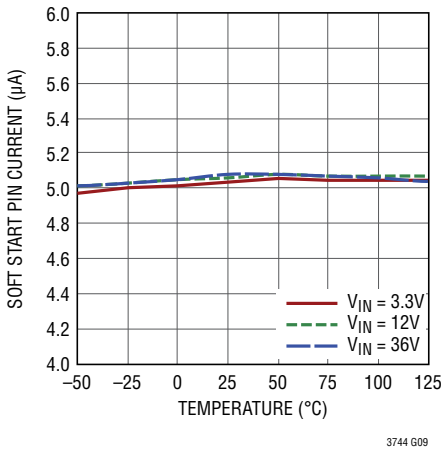
V_{REF} UVLO



V_{REF} Current Limit

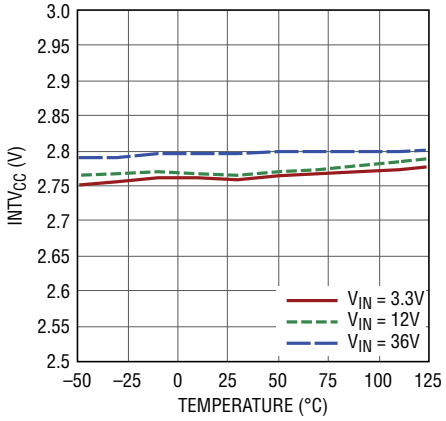


Soft-Start Pin Current

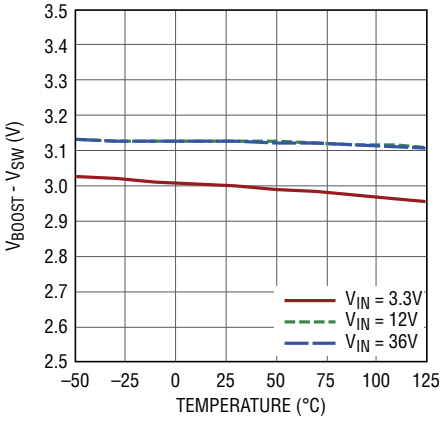


TYPICAL PERFORMANCE CHARACTERISTICS

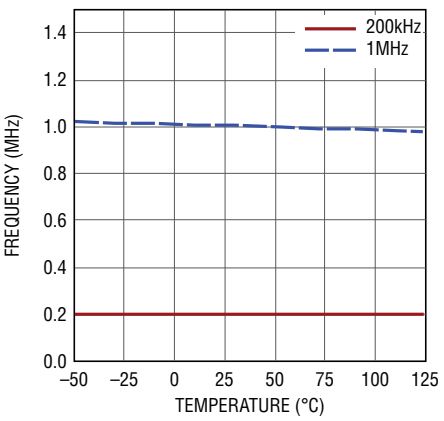
$INTV_{CC}$ UVLO (Falling Threshold)



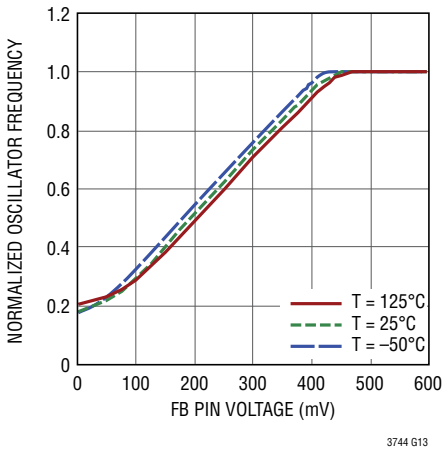
V_{BOOST} - V_{SW} UVLO (Falling Threshold)



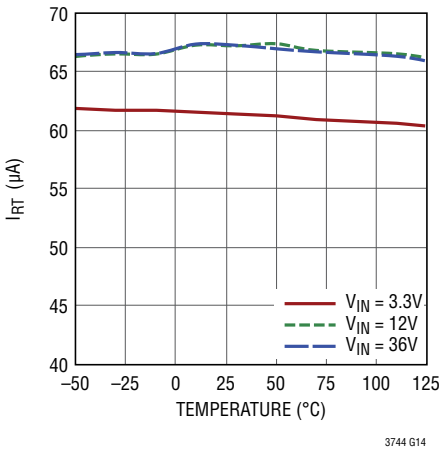
Oscillator Frequency



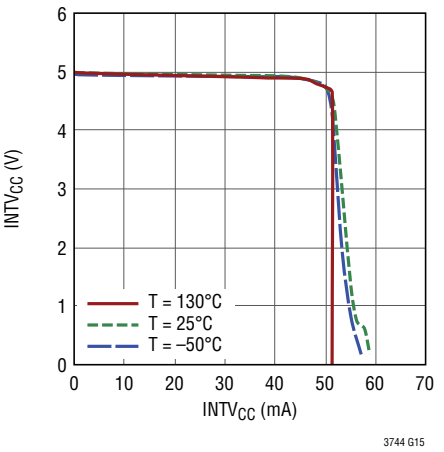
Frequency Foldback



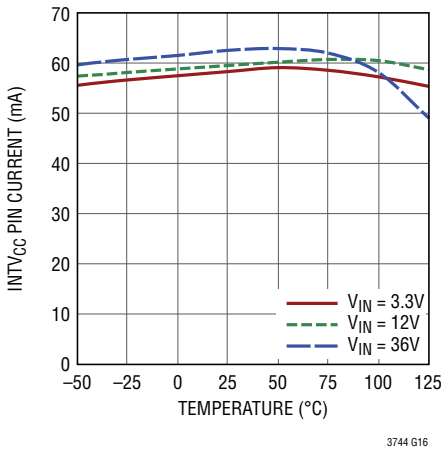
RT Pin Current Limit



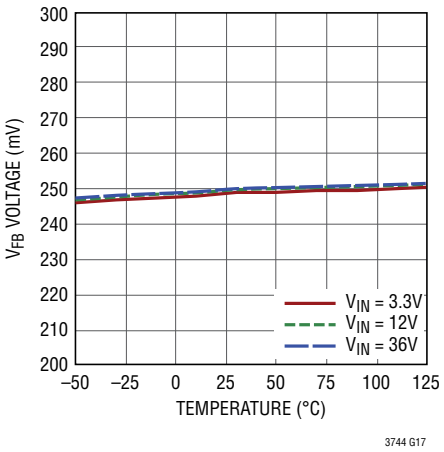
$INTV_{CC}$ Load Regulation



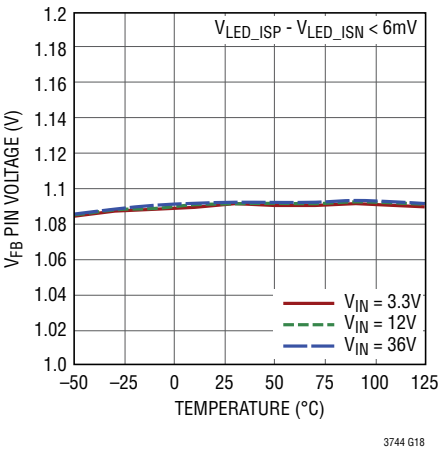
$INTV_{CC}$ Current Limit



Lower $\overline{FAULT}$ Threshold (Falling)

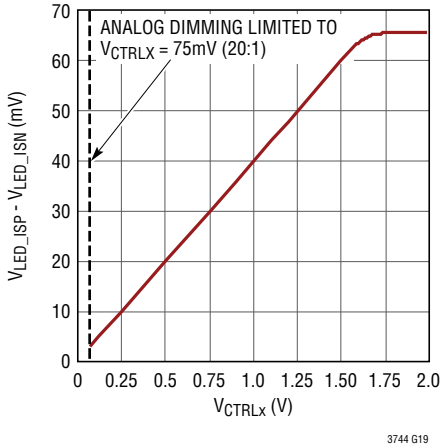


Upper $\overline{FAULT}$ Threshold (Rising)



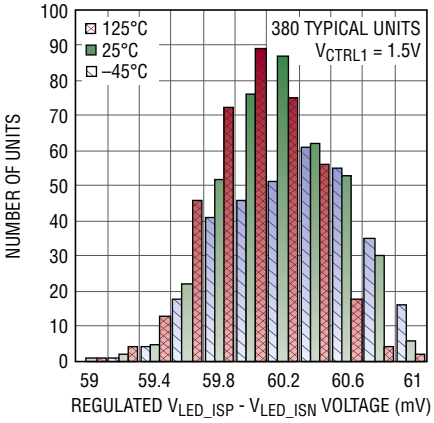
TYPICAL PERFORMANCE CHARACTERISTICS

Regulated Sense Voltage



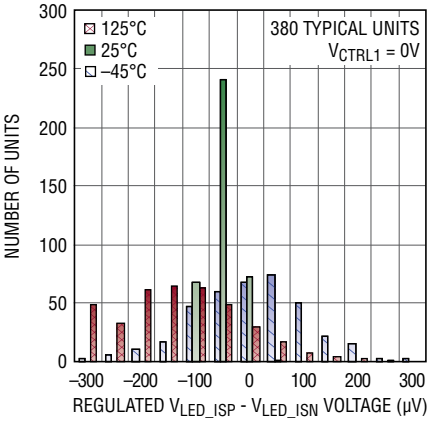
3744 G19

LED Current Regulation Accuracy



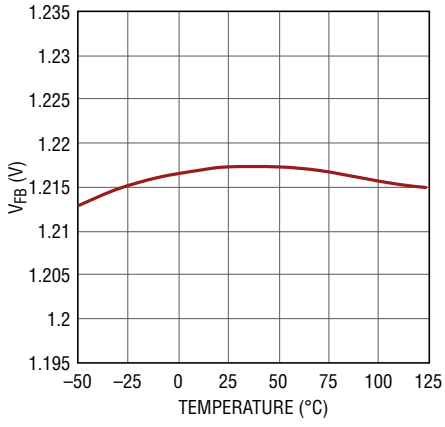
3744 G20

LED Current Regulation Accuracy



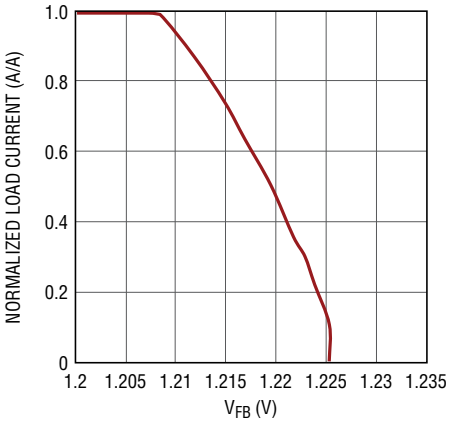
3744 G21

Feedback Voltage



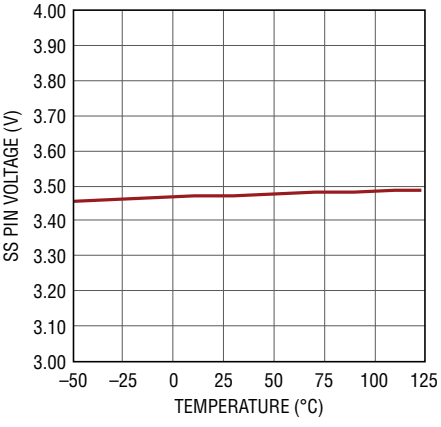
3744 G22

V_{FB} Load Regulation



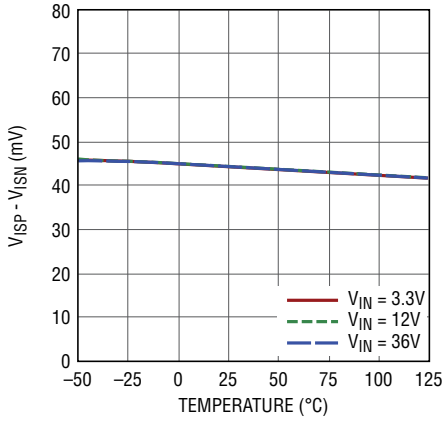
3744 G23

SS "Finished" Threshold



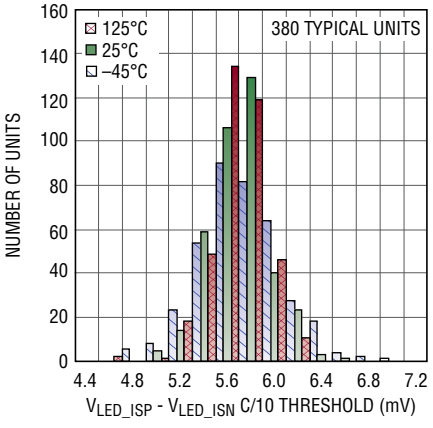
3744 G23a

Average Current Regulation During Start-Up



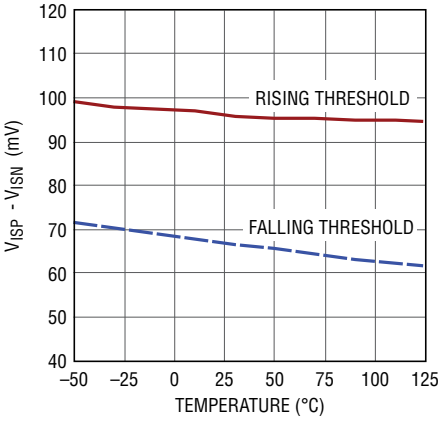
3744 G24

Falling C/10 Threshold



3744 G25

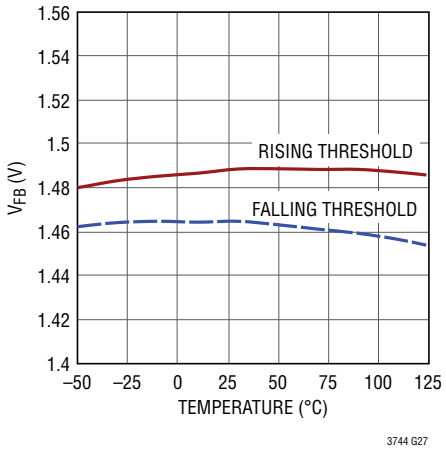
Overcurrent Threshold



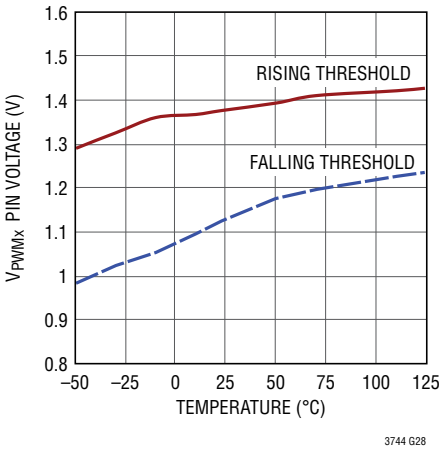
3744 G26

TYPICAL PERFORMANCE CHARACTERISTICS

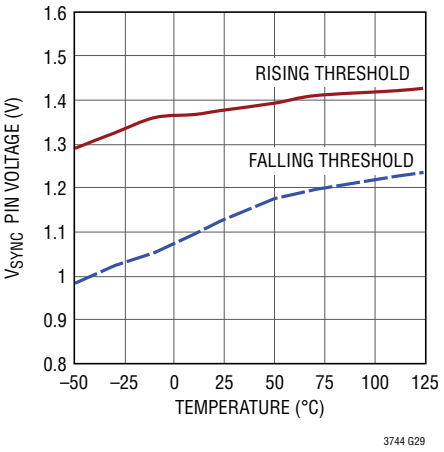
OVLO Threshold



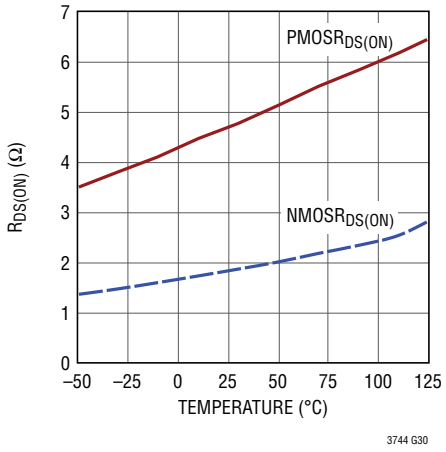
PWM1, PWM2, PWM3 Threshold



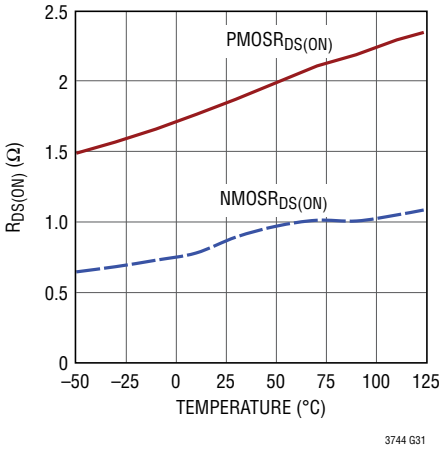
SYNC Threshold



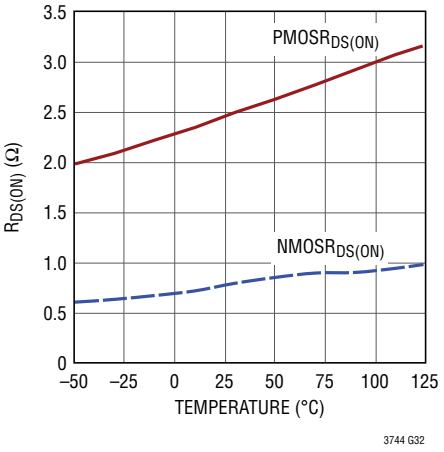
PWM Driver $R_{DS(ON)}$



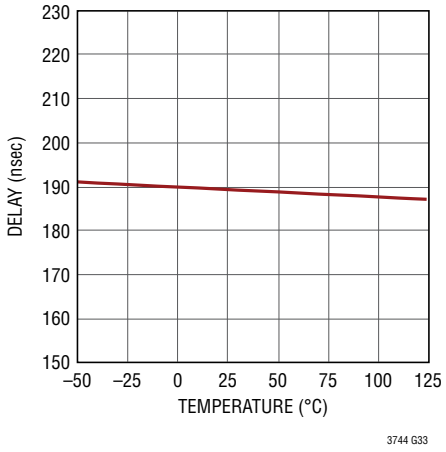
Bottom Gate Driver $R_{DS(ON)}$



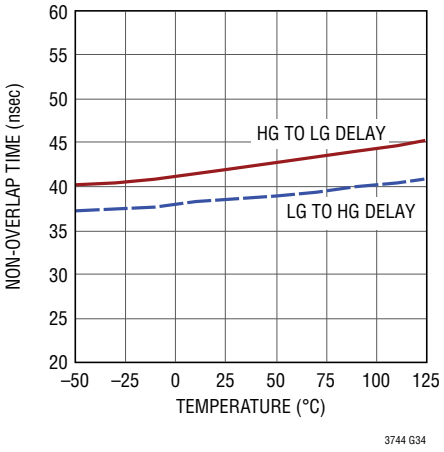
Top Gate Driver $R_{DS(ON)}$



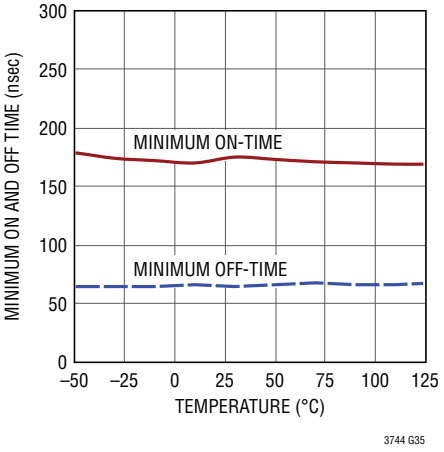
Non-Overlap PWM Signal Delay



BG and TG Non-Overlap Time

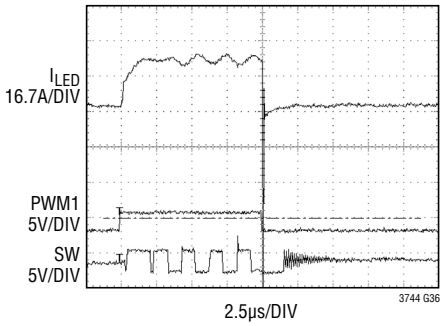


TG Minimum On-Time

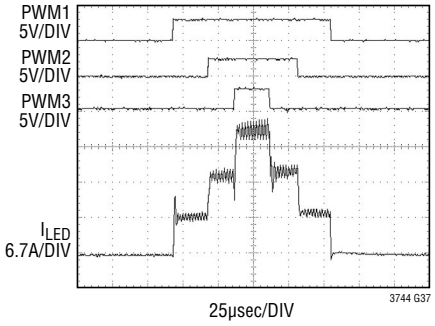


TYPICAL PERFORMANCE CHARACTERISTICS

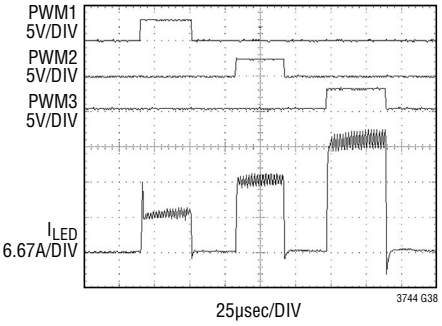
LED Current Waveforms (0A to 20A) 2000:1



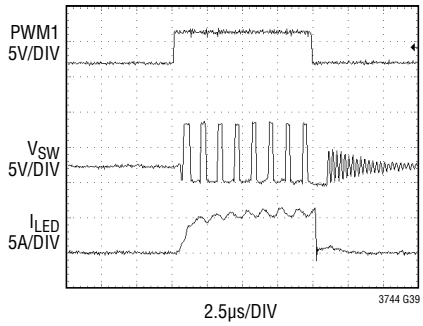
LED Current Waveforms (0A to 6.7A to 13.3A to 20A) 2000:1



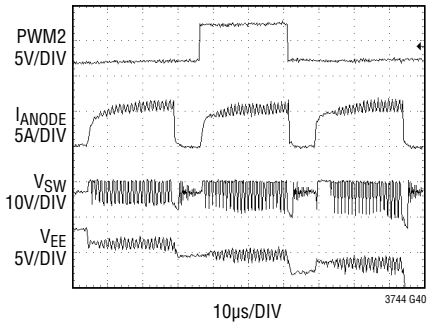
LED Current Waveforms (0A to 6.7A to 13.3A to 20A) 5000:1



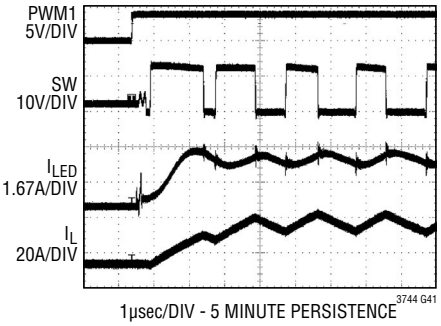
LED Current Waveforms (0A to 5A) 2000:1 Inverting Buck-Boost Regulator



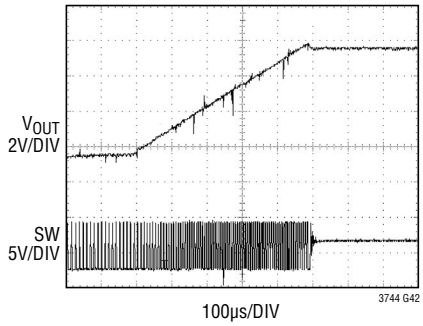
LED Current Waveforms (0A to 10A) 1000:1 Inverting Regulator



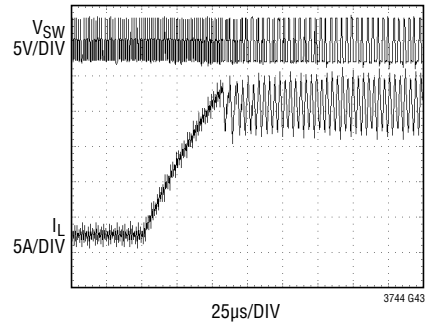
LED Current Waveforms (5000:1) 0A TO 20A Flicker-Free Performance



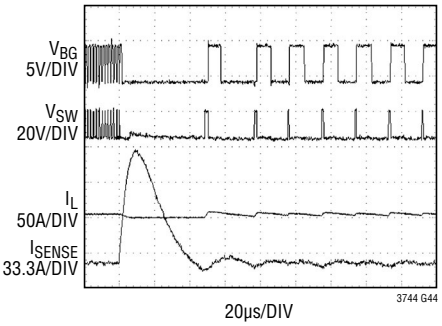
Voltage Regulation



Overcurrent



LED_ISP – LED_ISN Overvoltage Protection



PIN FUNCTIONS

EN/UVLO (Pin 1): The EN/UVLO pin acts as a precision enable and turns on the internal current bias core and subregulators with a rising threshold of 1.30V and a falling threshold of 1.235V. The pin has a 4.8µA pull-down current when below 1.235V. For normal operation, this pin requires a voltage bias. Full shutdown occurs at approximately 0.5V and low I_Q operations is guaranteed below 0.3V. This pin is referenced to SGND.

CTRL1, CTRL2, CTRL3 (Pin 2, 4, 5): The voltage at the CTRL pins set the regulated LED current. When PWM1 is high and PWM2 and PWM3 are low, CTRL1 is used. When PWM2 is high and PWM3 is low, CTRL2 is used. Whenever PWM3 is high, CTRL3 is used. The maximum analog control is 1.5V providing 60mV regulated voltage across the LED_ISP and LED_ISN sense resistor. The analog dimming range using the CTRL pins is 20:1. This means the lowest CTRL input for guaranteed operation is 75mV. At this V_{CTRL}, the voltage between the LED_ISP and LED_ISN pins will be regulated at 3mV ±500µV (±17%). All CTRL pins are referenced to SGND.

V_{REF} (Pin 3): V_{REF} is a buffered 2.0V reference capable of 0.5mA drive. This pin is referenced to SGND. A minimum capacitance of 2.2µF to SGND is required on this pin.

CTRLT (Pin 6): The voltage at the CTRLT pin limits the regulated LED current whenever CTRLT is lower than CTRL1, CTRL2 or CTRL3. This pin may be used for thermally limiting the LED current using an NTC resistor. The CTRLT pin is referenced to SGND.

PWM1, PWM2, PWM3 (Pins 7, 8, 9): Pins PWM1, PWM2 and PWM3 are digital input pins that determine which of the CTRL voltages are used to regulate the LED current and which LEDs and/or capacitors are connected to the output. All PWM input pins are referenced to SGND.

SYNC (Pin 10): Frequency Synchronization Pin. This pin allows the switching frequency to be synchronized to an external clock. The R_T resistor should be chosen to operate the internal clock at 10% slower than the SYNC pulse frequency. This pin should be grounded when not in use. The SYNC pin is referenced to SGND.

$\overline{\text{FAULT}}$ (Pin 11): The $\overline{\text{FAULT}}$ pin indicates either an overvoltage or shorted output. At FB voltages less than 250mV and greater than 1.1V (with V_{LED_ISP} - V_{LED_ISN} less than 6mV), the $\overline{\text{FAULT}}$ pin is pulled low to SGND. The pull-down impedance is 50Ω. The $\overline{\text{FAULT}}$ pin is referenced to SGND.

SGND (Pin 12): System/Board Ground. All input pins are referenced to SGND. V_{SGND}-VEE may have a potential difference of up to 20V. The voltage at the VEE pin should never be higher than the voltage at the SGND pin. For proper operation when configured as an inverting buck-boost regulator, use a low V_F Schottky diode between VEE and SGND.

RT (Pin 13): A resistor to ground sets the switching frequency between 100kHz and 1.0MHz. This pin is current limited to 66µA. Connect this pin through a resistor to VEE only. Do not connect to SGND and do not leave this pin open.

SS (Pin 14): Soft-Start Pin. Place a capacitor from this pin to VEE to limit the start-up voltage ramp. The SS pin has a 5µA charging current and is referenced to VEE.

LED_ISN (Pin 15): LED_ISN is the noninverting input of the LED current sensing error amplifier. Connect this pin to the lower terminal of an external current sense resistor in series with the LED cathode or the source of the LED disconnect FET (LED_ISN must be connected to VEE). The voltage drop between LED_ISP and LED_ISN is regulated to the current determined by the voltage of the CTRL1, CTRL2 and CTRL3 pins. The LED_ISN pin is referenced to VEE.

LED_ISP (Pin 16): LED_ISP is the inverting input of the LED current sensing error amplifier. Connect this pin to the upper terminal of the sense resistor in series with the LED cathode. The voltage drop between LED_ISP and LED_ISN is regulated to the current determined by the voltage at the CTRL pins. The LED_ISP pin is referenced to VEE.

PIN FUNCTIONS

FB (Pin 17): Feedback Pin. The feedback regulation voltage is 1.205V. The LT3744 will go into frequency foldback at feedback voltages less than 0.4V and foldback to a minimum of 10% of the normal switching frequency. If the voltage between LED_ISP and LED_ISN is less than 6mV while the voltage on FB is greater than 1.1V, $\overline{FAULT}$ is pulled low to SGND. Also, if the voltage on the FB pin is less than 250mV, the $\overline{FAULT}$ pin is again pulled low to SGND. If the FB voltage is less than 100mV, the BG signal is disabled during overcurrent events. The FB pin is referenced to VEE.

V_{C3}, V_{C2}, V_{C1} (Pins 18, 19, 20): V_{C3}, V_{C2} and V_{C1} provide the necessary compensation for the peak current loop stability. Typical compensation values are 20kΩ to 40kΩ for the resistor and 2.2nF to 10nF for the capacitor. The VC pins are referenced to VEE.

ISN (Pin 21): ISN is the inverting input of the inductor current sense g_m amplifier. This pin is connected to an external current sense resistor in series with the inductor. The inductor current sense amplifier provides inductor current information to the LT3744. The amplifier senses inductor current with a common mode range of 0V to a maximum of 36V. ISN and ISP are independent of V_{IN} and may go to a higher voltage than the supply of the LT3744.

ISP (Pin 22): ISP is the noninverting input of the inductor current sense g_m amplifier. This pin is connected to an external current sense resistor in series with the inductor. Inductor overcurrent is set at 110mV between the ISP and ISN pins and has –35mV of hysteresis.

PWM_OUT3, PWM_OUT2, PWM_OUT1 (Pins 23, 25, 27): The PWM_OUT pins drive the gates of a external NMOS FETs connected in series with output capacitors or LED cathodes.

V_{FNEG} (Pin 24): V_{FNEG} is the negative supply voltage to the PWM_OUT drivers. It is used with diodes to control the gate of the PWM dimming FETs when the FETs are off. The voltage at this pin may go to –15V below VEE.

VEE (Pins 26, 28, 33, 35, Exposed Pad Pin 37): VEE is the LT3744 internal ground. All internal and driver output signals are referenced to VEE. VEE and SGND may have a voltage difference of up to –20V. The voltage at the VEE pin should never be higher than the voltage at the SGND pin. For step-down applications, connect VEE to SGND. For inverting buck-boost applications, do not connect SGND and VEE.The VEE exposed pad must be soldered to the PCB. If VEE and SGND are isolated, the exposed pad must not be on the same ground plane as SGND.

TG (Pin 29): TG is the top FET gate drive signal that controls the state of the high side external power FET. The driver pull-up impedance is 3Ω and pull-down impedance is 1.5Ω.

SW (Pin 30): The SW pin is used internally as the lower supply rail for the floating high side driver. Externally, this node connects the two power FETs and the inductor.

BOOST (Pin 31): The BOOST pin provides a floating 5V regulated supply for the high side FET driver. An external Schottky diode is required from the $INTV_{CC}$ pin to the BOOST pin to charge the BOOST capacitor when the switch pin is near ground.

BG (Pin 32): BG is the bottom FET gate drive signal that controls the state of the low side external power FET. The driver pull-up impedance is 2.5Ω and pull-down impedance is 1.5Ω.

$INTV_{CC}$ (Pin 34): A regulated 5V output (referenced to VEE) for charging the BOOST capacitor. $INTV_{CC}$ also provides the power for the digital and switching sub-circuits. $INTV_{CC}$ is current limited to 50mA. Shutdown operation disables the output voltage drive. Use a minimum of 10µF to bypass this pin to VEE.

V_{IN} (Pin 36): Input Supply Pin. Must be locally bypassed with at least a 1µF low ESR capacitor to ground.

BLOCK DIAGRAM

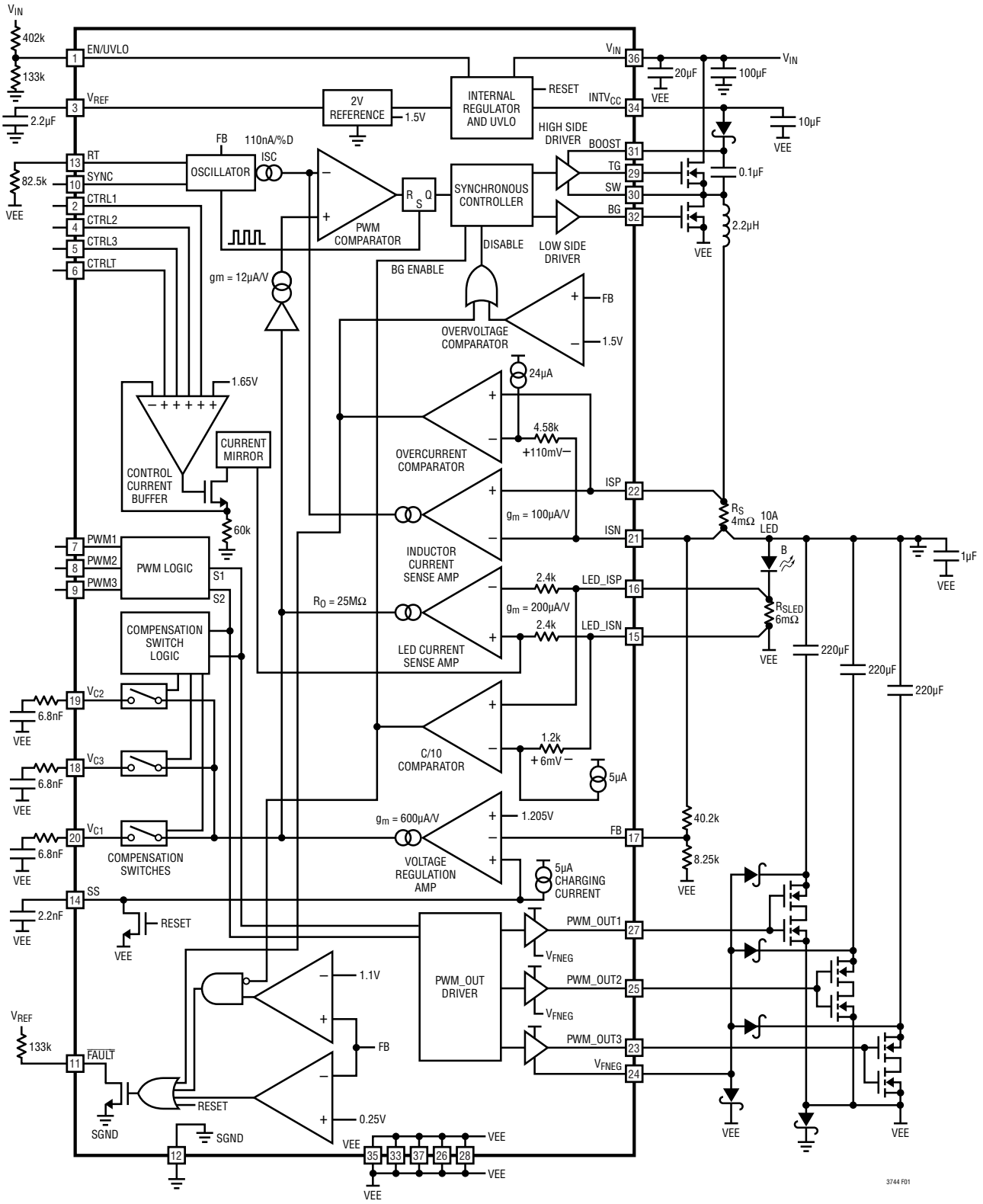


Figure 1. Block Diagram

OPERATION

The LT3744 utilizes fixed frequency, peak inductor current mode control to accurately regulate the current in a single externally switched LED, multiple parallel LEDs, or a string of LEDs. The current control loop will regulate the LED current at an accuracy of ±3% at 60mV when the CTRL input is at 1.5V. If the output voltage reaches the regulation voltage determined by the resistor divider from the output to the FB pin and VEE, the peak inductor current will be reduced by the voltage regulation loop. In voltage regulation, the output voltage has an accuracy of ±3%. For additional operation information, refer to the Block Diagram in Figure 1.

To provide maximum flexibility, the LT3744 may be used to regulate negative output voltages in an inverting buck-boost topology. This allows the use of a single lithium-ion battery to drive a multi-LED string without the need to use complex buck-boost or multiple converter topologies. VEE is the internal ground of the LT3744 and SGND is the system/board ground. All digital and analog input signals are referenced to SGND. All digital, analog, and gate drive output signals are referenced to VEE. SGND and VEE may have a potential difference of up to 20V. The voltage at the VEE pin should never be higher than the voltage at the SGND pin.

The LED current control loop uses the reference current determined by the voltage at the analog control pins: CTRL1, CTRL2 and CTRL3. The analog dimming range using the CTRL pins is 20:1. At 1.5V, the voltage between the LED_ISP and LED_ISN pins will be regulated at 60mV. The lowest CTRL input for guaranteed operation is 75mV. At this V_{CTRL}, the voltage between the LED_ISP and LED_ISN pins will be regulated at 3mV ±500µV (±17%). Control voltages above 1.65V have no effect on the regulated LED current. The regulated LED current corresponds to the state of the PWM1, PWM2 and PWM3 pins. When PWM1 is high, and PWM2 and PWM3 are low, CTRL1 pin is used as the current regulation reference, and PWM_OUT1 is high. When PWM2 is high and PWM3 is low, CTRL2 pin is used as the current regulation reference, and PWM_OUT2 is high. Whenever PWM3 is high, CTRL3 pin is used as the current regulation reference, and PWM_OUT3 is high.

The LT3744 is designed to drive LEDs with fast rising and falling edges. This includes transitioning between multiple current states for color mixing, or between LEDs with different forward voltages. By using three states, the LT3744 may be used as a standalone driver for RGB systems, or in high performance LED projectors where color blending creates more pure colors. The rapid transition between the three states is achieved with a switched-capacitor topology, where each output capacitor stores the forward voltage of each state so that returning to this state is achieved quickly. Each of these capacitors must be switched individually with drain-to-drain FETs. To prevent the capacitor from discharging through the FET switches, the bottom rail for the PWM_OUT drivers is provided on the V_{FNEG} pin. Schottky diodes connected from the negative terminal of the switched capacitors to the V_{FNEG} pin, allows the output capacitors to have up to 15V difference between them. This allows the use of multiple LEDs in one of the strings and single LEDs in the others.

A 2.0V external reference voltage is provided on the V_{REF} pin to allow the use of a resistor voltage divider to the CTRL1, CTRL2, CTRL3 and CTRLT pins. Although the current limit for V_{REF} is set at 3mA, for accuracy, the load current on the V_{REF} pin should be limited to 0.5mA.

$INTV_{CC}$ provides a regulated 5V for internal circuitry and for the gate driver. For stability, this pin should be bypassed with at least a 10µF capacitor to VEE. The $INTV_{CC}$ pin is current limited to 50mA. Please be aware that the current limit on this pin is thermally derated for temperatures above 120°C. Do not use this pin to drive any external load. The internal UVLO on the $INTV_{CC}$ pin prevents switching until the voltage is higher than 2.9V.

The inductor overcurrent is set at 110mV between the ISP and ISN pins and has –35mV hysteresis. The overcurrent is limited on a cycle-by-cycle basis; shutting down the high side gate once the overcurrent level is reached. If the feedback voltage is less than 100mV during an overcurrent event, the bottom gate is disabled, otherwise the bottom FET will conduct current until the lower overcurrent limit threshold is reached. The $\overline{FAULT}$ pin is asserted whenever an overcurrent event occurs.

OPERATION

The regulated output voltage is set with a resistor divider from the output back to the FB pin. The voltage reference at the FB pin is 1.205V. If the output voltage level is high enough to engage the voltage loop, the peak inductor current will be reduced to support the load at the output. Whenever the voltage on the FB pin is less than 250mV, the $\overline{FAULT}$ flag is asserted.

Whenever the FB pin is greater than 1.1V and the voltage across the LED_ISP and LED_ISN pins less than 6mV, the $\overline{FAULT}$ flag is asserted. If there is any internal fault condition to the LT3744 (such as thermal shutdown or UVLO), the $\overline{FAULT}$ flag is asserted.

For maximum efficiency, the BG driver is disabled whenever the voltage across the LED_ISP and LED_ISN pins is less than 6mV. For overvoltage protection, if V_{FB} exceeds 1.5V, the PWM_OUT drivers are turned off and switching stops.

The EN/UVLO pin functions as a precision shutdown pin, with a 1.3V rising threshold and a 1.235V falling threshold. Full shutdown is guaranteed below 0.3V with a quiescent current of less than 1µA. In addition, when the voltage at the EN/UVLO pin is less than 1.235V, a 4.8µA pull-down current source is internally connected to this pin. This current allows the amount of hysteresis to be programmed with a series resistor to the EN/UVLO pin or resistor divider from V_{IN}.

During start-up (or after a reset event), the TG, BG and PWM_OUT drivers are disabled until the first rising edge of any of the PWM pins inputs. After this, all PWM_OUT drivers are turned on to allow multiple capacitor topologies to charge all of the capacitors at once. Soft-start is also allowed to charge with a 5µA current source and switching commences. During this start-up time, the average inductor current is regulated to 48mV between the ISP and ISN pins. Once the current in the LED/load (sensed by the voltage across the LED_ISP and LED_ISN pins) reaches 15% of maximum (9mV), the PWM_OUT drivers connect the correct LED to the output, corresponding to the state of the PWM input pins. This avoids potentially long start-up times and overshoot of the VC pin, causing potentially damaging currents to flow into the LED. This start-up scheme also avoids undesirably bright “start-up flash” that is observed in many other high current LED drivers. If the voltage between LED_ISP and LED_ISN does not exceed 9mV before the SS (soft-start) pin voltage reaches roughly 3.5V, then the startup sequence is terminated, the correct LED is connected to the output, and normal operation begins. This is required so that regulated LED_ISP and LED_ISN voltages below 9mV are dimmed correctly after soft-start has timed out. Soft-start ramps the internal feedback voltage used in the voltage regulation loop. If the output voltage is prebiased, the BG driver is disabled until the voltage at the soft-start pin exceeds the voltage at the feedback pin. This prevents high negative currents from flowing in the bottom FET during a start-up recovery.

The thermal shutdown is guaranteed to be higher than the operational temperature of the part. During thermal shutdown, all switching is terminated, all PWM_OUT signals are forced low, and the part is in reset (forcing the SS pin low).

The switching frequency is determined by a resistor from the RT pin to VEE. The RT pin is current limited to 66µA, limiting the switching frequency to 2.4MHz when the RT pin is shorted to VEE. The LT3744 may also be synchronized to an external clock through the use of the SYNC pin. The SYNC pin is referenced to SGND. When the voltage on the FB pin decreases below 400mV, the switching frequency is reduced linearly to a minimum of 10%.

APPLICATIONS INFORMATION

Programming LED Current

The analog voltage at the CTRL pins are buffered and produce a reference voltage, V_{CTRL}, across an internal resistor. The regulated LED current is determined by:

$$I_{LED} = \frac{V_{CTRL}}{25 \bullet R_{SLED}}$$

where R_{SLED} is the external sense resistor in series with the LED cathode and I_{LED} is the LED current. Figure 2 shows the maximum LED current vs R_{SLED}.

Table 1 lists several resistance values and the corresponding maximum LED current and sense resistor power dissipation. The accuracy of the LED sense resistor is very important. Susumu, Panasonic and Vishay offer accurate sense resistors. The accuracy of the inductor current sense resistor is not as critical and lower accuracy resistors may be used.

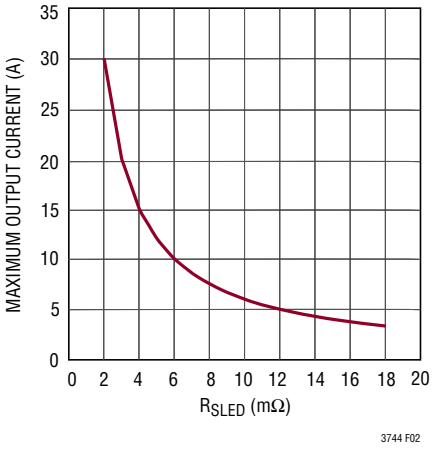


Figure 2. R_{SLED} Value Selection for Regulated Output Current

Table 1. Sense Resistor Values

MAXIMUM LED CURRENT (A)	RESISTOR, R_{SLED} (mΩ)	POWER DISSIPATION (W)
1	60	0.06
5	12	0.3
10	6	0.6
20	3	1.2

LED Current Regulation

The regulation voltage across the LED_ISP and LED_ISN pins is 60mV when there is 1.5V at the corresponding control pin. When PWM1 is high with a low on PWM2 and PWM3, the voltage at the CTRL1 pin is used as the reference for the regulated LED current. When PWM2 is high with a low on PWM3, the voltage at the CTRL2 pin is used as the reference for the regulated LED current. Whenever PWM3 is high, the voltage at the CTRL3 pin is used. During start-up, or a recovery from a fault condition, the inductor current is regulated at 80% of maximum current (48mV between ISP and ISN) until the voltage between LED_ISP and LED_ISN is greater than 9mV or the voltage at the soft-start pin has reached 3.5V. This will prevent excessive current overshoot in the LED when it begins conducting. Also, whenever the voltage between LED_ISP and LED_ISN is lower than 6mV, the bottom gate (BG) is disabled, improving low current efficiency.

The analog voltage at the CTRL pins adjusts the regulated LED current, Figure 3 shows the regulated voltage across the sense resistor for control voltages up to 2V. The LT3744 utilizes a highly accurate regulation scheme to achieve ±1.8mV regulation accuracy across the LED sense resistor at 60mV and ±500µV at 3mV. This high accuracy allows up to 20:1 analog dimming ratios. A resistor divider from V_{REF} to the CTRL pins may be used. When sizing the resistor divider, please be aware that the V_{REF} pin is current limited to 0.5mA, and that above 1.65V, the control voltage has no effect on the regulated LED current.

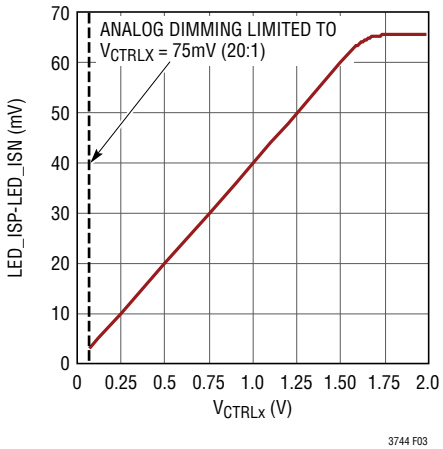


Figure 3. Sense Voltage vs CTRL Voltage

APPLICATIONS INFORMATION

Inductor Selection

Inductor sizing depends on circuit topology. The LT3744 may be used in a step-down configuration, producing positive voltages, or in an inverting buck-boost configuration, producing negative voltages with respect to supply ground. For step-down applications, size the inductor so that the peak-to-peak ripple current is approximately 30% of the output current. The following equation sizes the inductor for best performance in a step-down application:

$$L_{STEP-DOWN} = \left(\frac{V_{IN} \bullet V_{LED} - V_{LED}^2}{0.3 \bullet f_{SW} \bullet I_{LED} \bullet V_{IN}} \right)$$

where V_{LED} is the LED forward voltage, V_{IN} is the input voltage, I_O is the maximum regulated current in the inductor and f_{SW} is the switching frequency. The peak current in a step-down application is:

$$I_{L(PEAK\_STEP-DOWN)} = \left(\frac{V_{IN} \bullet V_{LED} - V_{LED}^2}{2 \bullet f_{SW} \bullet L \bullet V_{IN}} \right) + I_{LED}$$

The inductor saturation current should be equal or higher than the peak current. For inverting buck-boost applications, use the following equation to size the inductor for best performance:

$$L_{INVERTING} = \left(\frac{V_{IN} \bullet V_{LED}}{0.3 \bullet f_{SW} \bullet I_O \bullet (V_{IN} + V_{LED})} \right)$$

The peak current for inverting buck-boost applications will be:

$$I_{L(PEAK\_INVERTING)} = \left(\frac{V_{IN} \bullet V_{LED}}{2 \bullet f_{SW} \bullet L \bullet (V_{IN} + V_{LED})} \right) + \left(\frac{V_{IN} + V_{LED}}{V_{IN}} \right) \bullet 1.2 \bullet I_{LED}$$

The overcurrent comparator terminates switching when the voltage between the ISP and ISN pins exceeds 110mV. If this occurs, and the FB pin voltage is higher than 100mV, BG will be high, allowing the inductor current to decrease. Once the voltage across the ISP and ISN sense pins has decreased below 75mV, normal switching will resume. During overcurrent, if the FB pin voltage is lower than 100mV, BG is turned off, allowing the inductor current to discharge through the body diode of the bottom FET.

Recommended inductor manufacturers are listed in Table 2.

Table 2. Recommended Inductor Manufacturers

VENDOR	WEBSITE
Coilcraft	www.coilcraft.com
Sumida	www.sumida.com
Vishay	www.vishay.com
Würth Electronics	www.we-online.com
NEC-Tokin	www.nec-tokin.com

Switching MOSFET Selection

The following parameters are critical in determining the best switching MOSFETs for a given application: total gate charge (Q_G), on-resistance ($R_{DS(ON)}$), gate-to-drain charge (Q_{GD}), gate-to-source charge (Q_{GS}), gate resistance (R_G), breakdown voltages (maximum V_{GS} and V_{DS}) and drain current (maximum I_D). The following guidelines provide information to make the selection process easier, and Table 3 lists some recommended parts and manufacturers.

For both switching MOSFETs the rated drain current should be greater than the maximum inductor current, either $I_{L(PEAK\_STEP-DOWN)}$ or $I_{L(PEAK\_INVERTING)}$ (see Inductor Selection section).

The rated drain current is temperature dependent and most MOSFET data sheets include a table or graph of the rated drain current vs temperature. Use this information to properly derate the delivered current using the CTRLT pin (see Load Current Derating Using the CTRLT Pin section).

The rated V_{DS} should be higher than the maximum input voltage (including transients) for both MOSFETs. The signals driving the gates of the switching MOSFETs have a maximum voltage of 5V with respect to the source. However, during start-up and recovery conditions, the gate-drive signals may be as low as 3V. Therefore, to ensure that the LT3744 recovers properly, the maximum threshold voltage should be less than 2V, and for a robust design, ensure that the rated V_{GS} is greater than 7V.

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Power losses in the switching MOSFETs are related to the on-resistance, $R_{DS(ON)}$; gate resistance, R_G; gate-to-drain charge, Q_{GD} and gate-to-source charge, Q_{GS}. Power lost to the on-resistance is an ohmic loss, $I^2R_{DS(ON)}$, and usually dominates for input voltages less than 15V. Power lost while charging the gate capacitance dominates for input voltages greater than 15V. When operating at higher input voltages, efficiency can be optimized by selecting a high side MOSFET with higher $R_{DS(ON)}$ and lower Q_G. The total power loss in the high side MOSFET can be approximated by:

$$P_{LOSS} = (\text{Ohmic Loss}) + (\text{Transition Loss})$$

$$P_{LOSS} \approx \left(\frac{V_O}{V_{IN}} \bullet I_O^2 \bullet R_{DS(ON)} \bullet \rho_T\right) + \left(\left(\frac{V_{IN} \bullet I_{OUT}}{5V}\right) \bullet ((Q_{GD} + Q_{GS}) \bullet (2 \bullet R_G + R_{PU} + R_{PD})) \bullet f_{SW}\right)$$

where ρ_T is a dimensionless temperature-dependent factor in the MOSFET's on-resistance. Using 70°C as the maximum ambient operating temperature, ρ_T is roughly equal to 1.3. R_{PD} and R_{PU} are the LT3744 high side gate-driver output impedance: 1.5Ω and 3Ω, respectively.

A good approach to MOSFET sizing is to select a high side MOSFET, then select the low side MOSFET. The trade-off between $R_{DS(ON)}$, Q_G, and Q_{GS} for the high side MOSFET is evident in the following example. V_O is equal to 4V, I_O is equal to 10A, and the switching frequency is 500kHz. The following N-channel MOSFETs are rated for a V_{DS} of 40V and have the same package, but with 8× different $R_{DS(ON)}$ and 4.5× different Q_G and Q_{GD}:

M1: $R_{DS(ON)}$ = 2.3mΩ, Q_G = 45.5nC, Q_{GS} = 13.8nC, Q_{GD} = 14.4nC, R_G = 1Ω

M2: $R_{DS(ON)}$ = 18mΩ, Q_G = 10nC, Q_{GS} = 4.5nC, Q_{GD} = 3.1nC, R_G = 3.5Ω

Power loss for M1 is shown in Figure 4a where nearly all of the losses are transitional. Power loss for M2 is shown in Figure 4b. For M2, the ohmic losses dominate at low V_{IN}, and transitional loss dominant at higher V_{IN}.

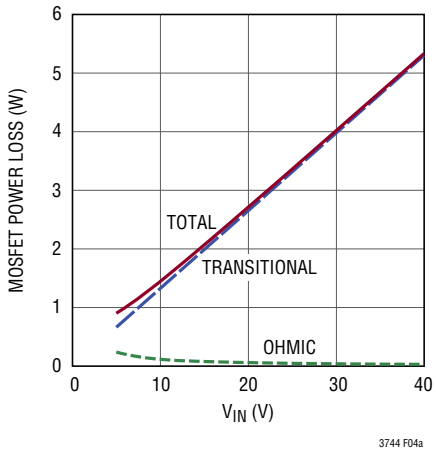

Figure 4a. Power Loss Example for M1

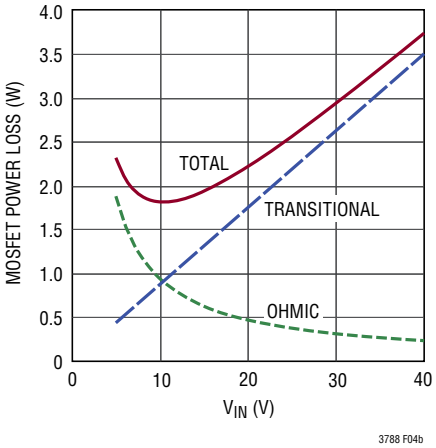

Figure 4b. Power Loss Example for M2

Power loss within the low side MOSFET is entirely from the $R_{DS(ON)}$ of the FET. Select the low side FET with the lowest $R_{DS(ON)}$ while keeping the total gate charge, Q_G to 30nC or less.

Table 3. Recommended Switching FETs

V_{IN} (V)	V_{LED} (V)	I_{LED} (A)	TOP FET	BOTTOM FET	MANUFACTURER
8	4	10	BSC010NE2LSI	BSC018N04LS	Infineon www.infineon.com
12	2-4	10	FDMS8680	FDMS8672AS	Fairchild www.fairchildsemi.com
26	4	20	Si7884BDP	SiR470DP	Vishay www.vishay.com

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PWM Dimming

The LT3744 has versatile dimming that accommodates many different PWM dimmed LED applications. This includes traditional PWM dimming with a single LED and a single-current level (Figure 5), shunt dimming (Figure 6), PWM dimming between three different currents with a single LED (Figure 7), or PWM dimming with three individual LEDs all at different regulated currents (Figures 8 and 9). When all three PWM input signals are low, no switching occurs and all three PWM_OUT signals are held low (to V_{FNEG}). After startup or a recovery from a fault condition (UVLO, Thermal Shutdown, etc.), on the first rising edge of any PWM input signal, switching begins, the Soft-Start capacitor is allowed to charge, and all PWM_OUT signals are held high. During this recovery time, the PWM input signals are ignored and the inductor current is regulated at 80% of the maximum output current (48mV between ISP and ISN). This allows the output capacitors to rapidly charge. The startup cycle is terminated when the voltage across the LED_ISP and LED_ISN input reaches 9mV or when the Soft-Start voltage reaches approximately 3.5V.

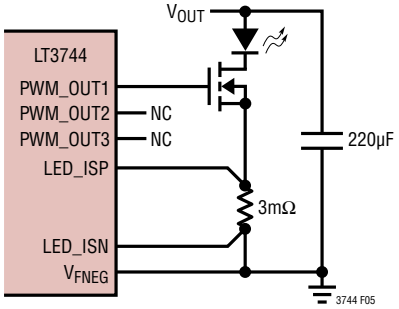

Figure 5. Driving a Single LED

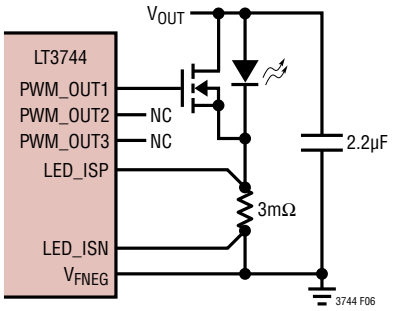

Figure 6. Shunt Dimming

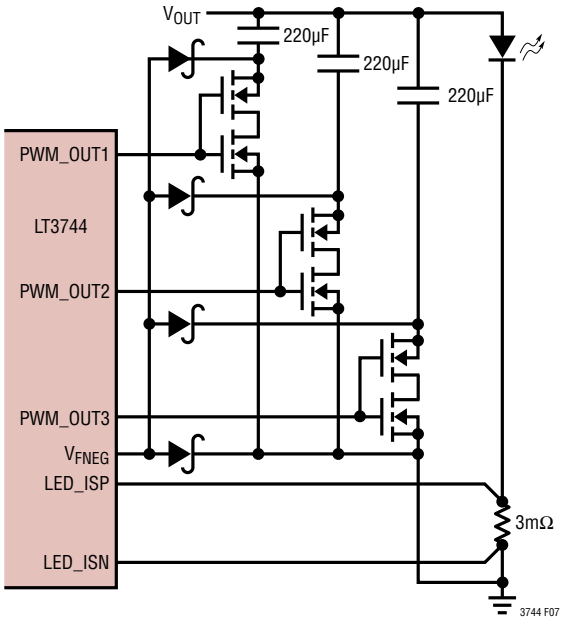

Figure 7. Driving a Single LED with Multiple Different Current Levels

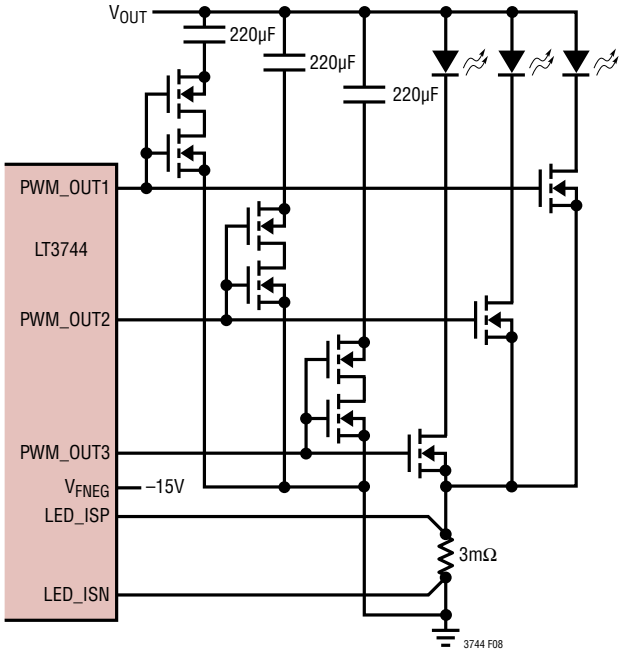

Figure 8. Driving Multiple LEDs from the Same Output Using a –15V Supply on V_{FNEG}

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Table 4 shows the PWM_OUT driver logic.

Table 4. PWM_OUT Driver Logic Truth Table

PWM3	PWM2	PWM1	PWM_OUT3	PWM_OUT2	PWM_OUT1
0	0	0	Low	Low	Low
0	0	1	Low	Low	High
0	1	0	Low	High	Low
0	1	1	Low	High	Low
1	0	0	High	Low	Low
1	0	1	High	Low	Low
1	1	0	High	Low	Low
1	1	1	High	Low	Low

The V_{FNEG} pin is the negative rail for the PWM_OUT drivers. When dimming with multiple current levels, or with multiple different LEDs, the use of Schottky diodes or an additional negative supply is required to allow the negative drive voltage to go below the power ground. This is needed to eliminate a leakage path for the output capacitors and allow the fastest LED current recovery time.

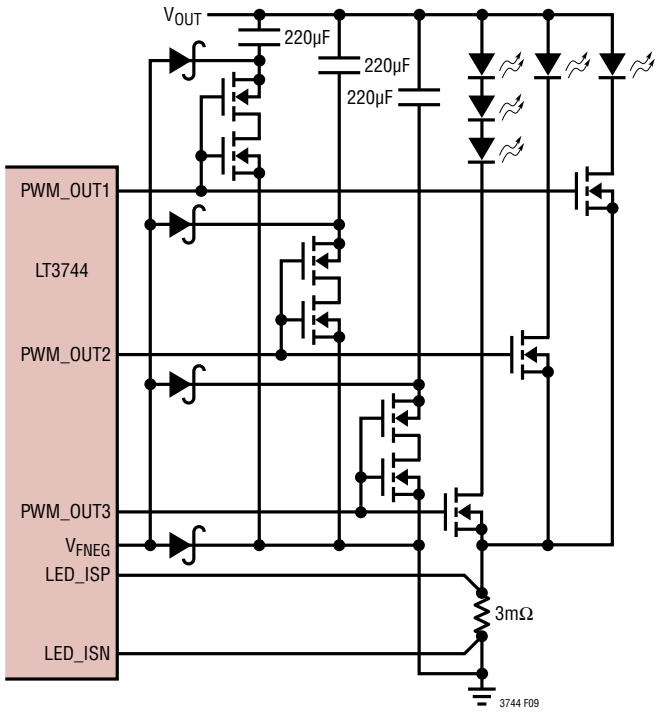

Figure 9. Driving Multiple LEDs from the Same Output Using Schottky Diodes For V_{FNEG}

Switched Capacitor and PWM Dimming MOSFET Selection

The rated V_{DS} for the switched capacitor and PWM dimming MOSFETs should be higher than the maximum output voltage. Although this permits a MOSFET choice with a smaller Q_G specification than that of the switching MOSFETs, it will have little affect on efficiency because the PWM switching frequency will be much lower than the driver switching frequency. Power lost charging the gate of these MOSFETs will be much lower than the power lost charging the switching MOSFETs. $R_{DS(ON)}$ conduction losses in these MOSFETs will also be much smaller if the duty cycle of the PWM signal is very low. When the LT3744 is configured to produce negative voltages, additional on-resistance will produce large amounts of ripple current in the LED. For configurations producing negative voltages, choose MOSFETs with the lowest available $R_{DS(ON)}$.

The switched capacitor and PWM dimming MOSFETs are driven with a maximum positive gate voltage of 5V, limited by the $INTV_{CC}$ pin. This requires that the threshold of the MOSFETs is lower than 2V. The maximum negative gate drive voltage is limited by the voltage at the V_{FNEG} pin. When the LT3744 is configured to drive LED loads with large differences in output voltages, the gate of these MOSFETs must be able to handle a maximum negative voltage equal in magnitude to the maximum output voltage without damage. As an example, if the maximum LED load voltage is 10V, the MOSFETs must survive –10V from gate to source/body. Please be aware that many MOSFETs have maximum V_{DS} ratings that are higher than the maximum V_{GS} rating. This means that the maximum V_{GS} rating should be used as the limiting voltage when selecting switched capacitor and PWM dimming MOSFETs.

Table 5. Recommended PWM MOSFETs

MAXIMUM V_{LED} (V)	I_{LED} (A)	PWM MOSFET (DUAL PACKAGE)	COMMENTS	MANUFACTURER
12	6	FDMB2307NZ	Common Drain	Fairchild www.fairchildsemi.com
12	8	Si7900AEDN	Common Drain	Vishay www.vishay.com
12	6	PHKD6N02LT	Dual Package SO8	NXP/Philips www.nxp.com

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Programming Switching Frequency

The LT3744 has a switching frequency range between 100kHz and 1MHz. This frequency is programmed with an external resistor from the RT pin to VEE. Do not leave this pin open under any condition. The RT pin is also current limited to 66µA. See Table 6 and Figure 10 for resistor values and the corresponding switching frequencies.

Table 6. Switching Frequency

SWITCHING FREQUENCY (MHz)	R_T (kΩ) - 1%
1.00	40.2
0.75	53.6
0.50	82.5
0.30	143
0.10	453

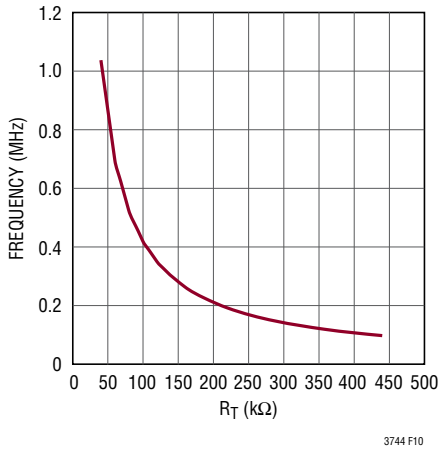

Figure 10. Frequency vs R_T Resistance

Switching Frequency Synchronization

The internal oscillator may be synchronized to an external clock through the SYNC pin. The external clock applied to the SYNC pin must have a logic low below 0.8V and a logic high above 2.0V. The input frequency must be 10% higher than the frequency that would otherwise be determined by the resistor at the RT pin. Input signals outside of these specified parameters will cause erratic switching behavior and subharmonic oscillations. Synchronization is tested at 190kHz and 1.1MHz with a 422k R_T resistor. Operation under other conditions is guaranteed by design. When synchronizing to an external clock, please be aware that there will be a fixed delay from the input clock edge to the edge of the signal at the SW pin. The SYNC pin must be grounded if the synchronization to an external clock is not required. When SYNC is grounded, the switching frequency is determined by the resistor R_T.

Frequency Foldback

To minimize erratic switching for low output voltages, the switching frequency is linearly decreased from 100% to a minimum of 10%, when the FB pin voltage is linearly decreased from 400mV to 0V as shown in Figure 11. This will provide a minimum of 50kHz when the desired switching frequency is 500kHz.

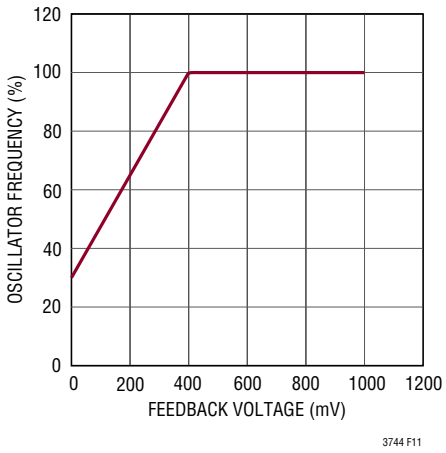

Figure 11. Frequency Foldback

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Input Capacitor Selection

The input capacitor should be sized at 10µF for every 1A of output current and placed between V_{IN} and SGND very close to the high side MOSFET. It should have a ripple-current rating equal to half of the maximum output current. Additionally, a small 1µF ceramic capacitor should be placed between V_{IN} and VEE as close as possible to the V_{IN} pin and the exposed pad of the package for optimal noise immunity.

It is recommended that several low ESR (equivalent series resistance) ceramic capacitors be used as the input capacitance. Use only X5R or X7R capacitors as they maintain their capacitance over a wide range of operating voltages and temperatures.

C_{BOOT} Capacitor Selection

The C_{BOOT} capacitor must be sized less than or equal to 220nF and more than 50nF to ensure proper operation of the LT3744. Use 220nF for high current switching MOSFETs with high gate charge.

Output Capacitor Selection

The output capacitors need to have very low ESR to reduce output ripple. The minimum size of the output capacitor should use the following equation:

$$C_{OUT\_MIN} = \left(I_{OUT} \bullet 8\mu F/A\right) \bullet \left(\frac{1MHz}{f_{SW}}\right)$$

In this equation, I_{OUT} is the maximum load current, and f_{SW} is the switching frequency. The capacitors also need to be surge-rated to the maximum output current. To achieve the lowest possible ESR, several low ESR capacitors should be used in parallel. Many applications benefit from the use of high density POSCAP capacitors, which are easily destroyed when exposed to overvoltage conditions. To prevent this, select POSCAP capacitors that have a voltage rating that is at least 50% higher than the regulated voltage. When using switched output capacitors, an additional small capacitor connected from the LED Anode to VEE is required. Size this capacitor at a maximum of 1/100th of the switched capacitor size.

$INTV_{CC}$ Capacitor Selection

The bypass capacitor for the $INTV_{CC}$ pin should be larger than 10µF to ensure stability, and it should be connected as close as possible to the exposed pad (VEE) underneath the package. It is recommended that the ESR be lower than 50mΩ to reduce noise within the LT3744. For driving MOSFETs with gate charges larger than 10nC, use 1µF/nC of total gate charge.

Soft-Start

The LT3744 utilizes the soft-start function to control the regulated output voltage. The charging current is 5µA and reduces the output voltage as long as the SS pin voltage is lower than the reference voltage of 1.205V. In a fault condition, (including thermal shutdown, or UVLO from either V_{IN}, $INTV_{CC}$ or V_{REF}) the soft-start pin is discharged to VEE. When the fault condition no longer exists, the soft-start pin is allowed to charge. Whenever the voltage at the feedback pin is higher than the soft-start pin (a prebiased output) the BG driver is disabled, preventing large negative inductor currents on a recovery from a fault condition.

Common-Anode LED Applications

The unique drive stage used on the LT3744 allows the anodes of three LEDs to be connected together – where the forward voltages may be up to 15V away from each other (allowing multiple LEDs in a single string to be connected to the same common point as a single LED). This connection will work in both inverting buck-boost and noninverting step down regulators. Some of the advantages using the noninverting topology is that the efficiency will be higher - typically by 5% to 10% depending on step-down ratio and regulated current; the inductor current will be less (in the inverting buck-boost configuration, inductor current is only delivered to the load on the “off” cycle); the LED current recovery time is faster (since the inductor current is delivered to the load constantly in the noninverting configuration); and the control loop bandwidth could be 5-times faster than the inverting buck-boost topology. Some of the disadvantages of the noninverting topology are that the output voltage is limited to less than the supply,

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the common-anode voltage will change depending on the LED load (LED color, forward voltage, regulated current, number of LEDs, etc.) – where the heat sink for the LEDs must be electrically isolated from chassis ground. The differences between the configurations are summarized in table 7.

Table 7. Comparison Between Noninverting and Inverting Buck-Boost Common-Anode Configurations

	Noninverting	Inverting
Topology	Step-Down	Buck-Boost
Max. Efficiency	90-95%	80-85%
Inductor Current	I_{LED}	$I_{LED}/(1-D)$
Loop Bandwidth	$f_{SW}/5$	$f_{SW}/25$
I_{LED} Recovery Time	$2/f_{SW}$	$8/f_{SW}$
Max V_{OUT}	$<V_{IN}$	Down to –20V
Heat sink	Isolated	Chassis GND

Inverting Buck-Boost Applications

For inverting buck-boost applications where the anode of the LED must be connected to the chassis or share a single electrically-conductive heat sink, the output voltage may be connected to board ground with the power ground (VEE) floating. In this configuration, the LT3744 may drive a single LED or multiple LEDs with higher forward voltages than the supply and have the anode of the LED tied to board (or system) ground. When in this configuration, the control loop of the LT3744 is similar to a boost converter and the bandwidth should be limited to avoid the right-half-plane zero associated with this type of switching converter (please see Inverting Buck-Boost Control Loop Compensation section). To allow the LT3744 to start-up properly, a low V_F Schottky diode is required between VEE and SGND.

Shutdown and UVLO

The LT3744 has a precision enable at 1.3V on the EN/UVLO pin. Partial shutdown occurs at 1.235V and full shutdown is guaranteed below 0.3V with <1µA I_Q in the full shutdown state. Below 1.235V, an internal current source provides 4.8µA of pull-down current to allow for programmable UVLO hysteresis. The following equations determine the voltage-divider resistors for programming the UVLO rising and falling thresholds configured in Figure 12.

$$V_{IN(RISING)} = 1.3V \bullet \left(\frac{R_1 + R_2}{R_1}\right) + R_2 \bullet 4.8\mu A$$

$$V_{IN(FALLING)} = 1.235V \bullet \left(\frac{R_1 + R_2}{R_1}\right)$$

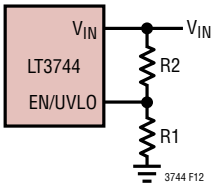

Figure 12. UVLO Configuration

LED Fault Detection

The LT3744 detects an open or shorted LED event and will indicate either condition by pulling the $\overline{FAULT}$ pin to SGND. These conditions are detected by monitoring the voltage at the FB pin. A shorted LED condition is detected as V_{FB} lower than 0.25V. A continuous output short to VEE will cause the current regulation loop to allow the inductor current to increase until the inductor current exceeds the maximum current limit at 110mV between the ISP and ISN pins. In an open-LED condition, the inductor current will charge the output capacitor and the voltage at FB will increase. When the FB pin is higher than 1.1V and the voltage between LED_ISP and LED_ISN is lower than 6mV, the open-LED condition will be indicated by pulling $\overline{FAULT}$ to SGND. The output voltage will continue to increase until the FB pin is regulated to 1.205V.

Voltage Regulation and Overvoltage Protection

The LT3744 uses the FB pin to regulate the output voltage, provide an overvoltage lockout, detect output fault conditions and foldback the switching frequency. The regulated output voltage is programmed using a resistor

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divider from the output and VEE (Figure 13). The regulated voltage is 1.205V at the FB pin. When the output voltage exceeds 125% of the regulated voltage level (1.5V at the FB pin), the internal overvoltage flag is set, terminating switching. The regulated output voltage must be greater than 1.205V and is set by the equation:

$$V_{OUT} = 1.205V\left(1+\frac{R2}{R1}\right)$$

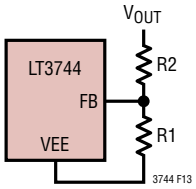

Figure 13. Output Voltage Regulation and Overvoltage Protection Feedback Connections

Load Current Derating Using the CTRLT Pin

The LT3744 is designed specifically for driving high power loads. In high current applications, derating the maximum current based on operating temperature prevents damage to the load. In addition, many applications have thermal limitations that will require the regulated current to be reduced based on load temperature and/or board temperature. To achieve this, the LT3744 uses the CTRLT pin to reduce the effective regulated current in the load, which is otherwise programmed by the analog voltages at the CTRL1, CTRL2 or CTRL3 pins. The load/board temperature derating is programmed using a resistor divider with a temperature dependant resistance (Figure 14).

Step-Down Control Loop Compensation

The peak current mode control in the LT3744 requires the external sense resistor, R_S to monitor the inductor current. To properly size R_S for the (noninverting) Step-Down Regulator, R_S must be equal to R_{SLED}. The LT3744 uses a high gain internal transconductance error amplifier to regulate the current in the load. The output of this amplifier is connected to one the three VC nodes (V_{C1}, V_{C2}, or V_{C3}). The LT3744's control loop is shown in Figure 15. For applications where positive voltages are generated with respect to board ground, use the following procedure for setting the compensation component values when driving LEDs:

1. Set the dominant pole at 0.5Hz with following equation:

$$C_{C1} = \frac{1}{2\pi \bullet R_{OEA} \bullet 0.5Hz} = 10nF$$

Since the dominant pole is based on the internal error amplifier output impedance, R_{OEA} (25MΩ), use of a 10nF capacitor is recommended for most applications.

2. Set the bandwidth with R_C. This is done to limit the bandwidth to 1/5 of the switching frequency. Starting with the load pole, f_{PLOAD}:

$$f_{PLOAD} = \frac{1}{2\pi \bullet C_{OUT} \bullet (R_{ESR} + R_{SLED})}$$

where R_{LOAD} is the resistive load of the LED, R_{ESR} is the equivalent series resistance of the output capacitor and R_{SLED} is the LED current sense resistor.

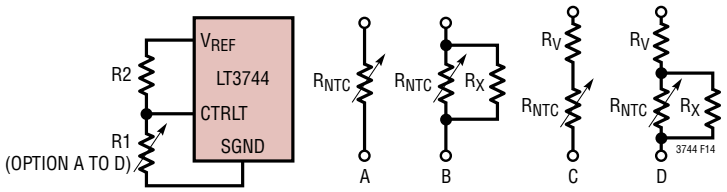

Figure 14. Load Current Derating vs Temperature Using NTC Resistor Divider from V_{REF}

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The following equation sets R_C:

$$R_C = \left(\frac{R_{OEA}}{AV_{LOOP}}\right) \bullet \left(\frac{f_{SW}}{5 \bullet f_{PLOAD}}\right)$$

In this equation, AV_{LOOP} is the loop gain, f_{PLOAD} is the load pole, and f_{SW} is the switching frequency. AV_{LOOP} is fixed and equal to 743V/V. R_C is typically 100kΩ to 600kΩ.

3. The output capacitor's ESR and capacitance form a load zero. To cancel this zero, use the following equation to set C_{C2}:

$$C_{C2} = \left(\frac{C_{OUT}}{R_C}\right) \bullet R_{ESR}$$

C_{C2} is typically between 5pF and 50pF. If the calculated value of this capacitor is less than 5pF, it may be removed.

Inverting Buck-Boost Control Loop Compensation

When the LT3744 is used to generate negative voltages, the compensation approach changes. To restore total system gain, the inductor current sense resistor should be sized to compensate for the loss in current gain due to the inverting buck-boost topology. Use the following equation to size the sense resistor, R_S:

$$R_S = \frac{V_{IN} \bullet R_{SLED}}{V_{IN} + V_{LED}}$$

Since the current is delivered to the load out-of-phase from the high side switch, a right-half-plane (RHP) zero exists that must be considered when sizing the compensation for the inverting topology. The RHP zero is at:

$$f_{RHPZ} = \frac{(R_{LOAD} + R_{SLED}) \bullet (1-D)^2}{2\pi \bullet L}$$

For proper sizing of the compensation capacitor, use the lowest supply voltage when computing D and the highest supply voltage when sizing the inductor (see Programming Inductor Current). In this case, since the total supply voltage for the synchronous switcher is equal to $V_{IN} + V_{LED}$, D is equal to:

$$D = \frac{V_{LED}}{V_{IN} + V_{LED}}$$

When the driving high current LEDs, the RHP zero can be at a very low frequency. To ensure stability, and allow for 10dB of gain margin, the crossover of the loop should be

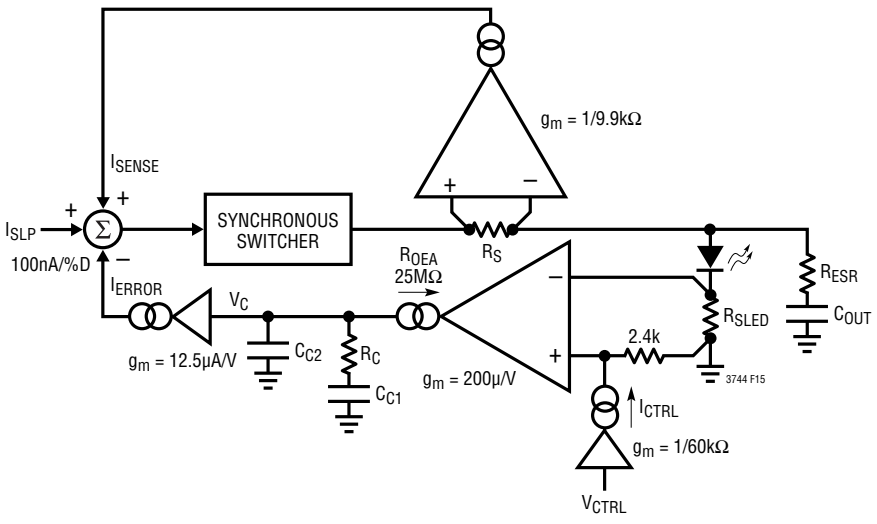

Figure 15. Step-Down LT3744 Control Loop

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set at 1/3 of the frequency of the RHP zero. The following equation properly sizes the compensation capacitor, C_C:

$$C_C = \frac{3 \bullet A_{VLOOP}}{2\pi \bullet R_{OEA} \bullet f_{RHPZ}}$$

where A_{VLOOP} is fixed and equal to 743V/V, R_{OEA} is also fixed and equal to 25MΩ. In most LED applications, C_C will range from 2.2nF to 20nF (if the application has a wide supply range, this capacitor could be as large as 82nF). Since the loop must have a very low frequency crossover, a single, large value compensation capacitor is all that is required for the inverting buck-boost topology.

PC Board Layout Checklist

- The PC board for a high current controller requires the use of a dedicated ground layer. To dissipate the heat from the switching components, use a large area for the switching node while keeping in mind that this negatively affects the radiated noise. To maximize efficiency and to avoid any potential noise issues, place both sense resistors as close as possible to the ISP, ISN, LED_ISP, and LED_ISN pins.
- The VEE power-ground layer should only connect to the bottom FET, $INTV_{CC}$ capacitor, output capacitor, and the LED (or load ground). It should not have any other traces. Analog signals referenced to VEE should be Kelvin connected to the exposed pad of the LT3744.
- Use vias directly under the exposed pad of the LT3744 and connect all VEE pins to the exposed pad metal through short lines.
- Place a large supply bypass capacitor close to the high side FET and another, lower value capacitor as close to the LT3744's V_{IN} pin as possible. For noninverting applications the ground terminal of input bypass capacitors should be tied to the power ground plane – where SGND and VEE are tied together. For inverting applications, the ground terminal of the input bypass capacitors should be tied to VEE only, not SGND.
- Use large planes for V_{IN} and V_{OUT}. Any additional trace length that is more than is necessary to connect to the LED will add inductance and reduce the effective current rise time in the LED.
- In an inverting configuration, output capacitor ESR will directly add to the LED current ripple, use the lowest ESR capacitor available. If the output capacitor is also switched, use the lowest $R_{DS(ON)}$ possible for the switched-capacitor FETs.

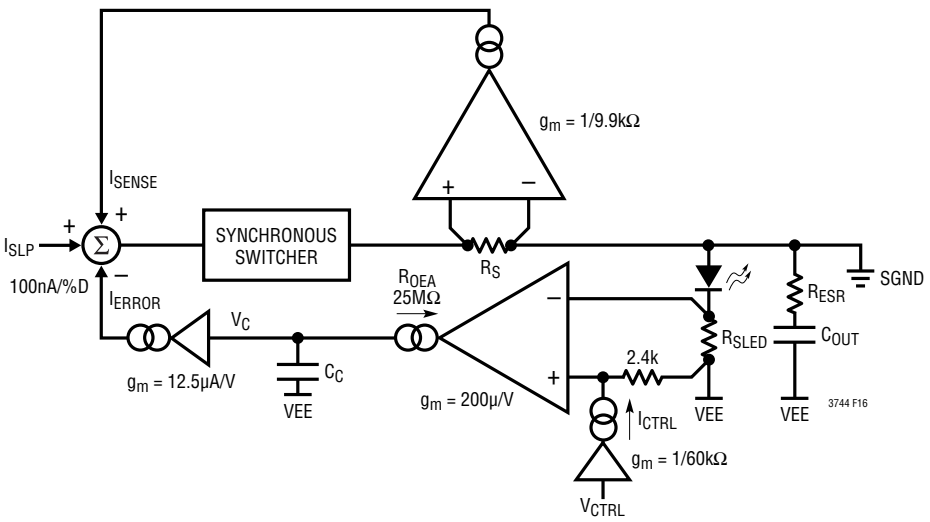


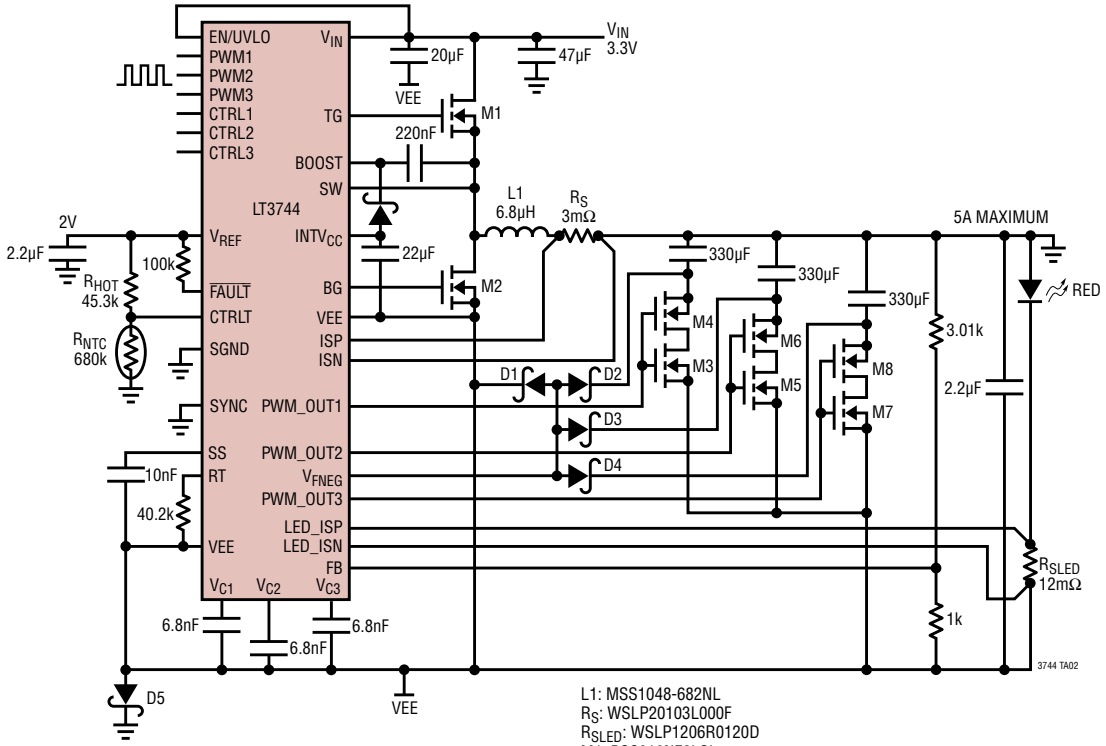
Figure 16. Inverting Buck-Boost LT3744 Control Loop

APPLICATIONS INFORMATION

- For noninverting applications, VEE and SGND should be Kelvin connected. For inverting applications, they should not be connected.
- Fill any unused area on any PCB layer with copper. This will add to the local heat sinking of the board and will increase efficiency by lowering the temperature rise of the power components. Connect these added copper areas to V_{IN}, SGND or VEE.
- Keep the pins that experience high dv/dt (SW, BOOST, TG and BG) away from any sensitive nodes. Nodes to be very careful about are: V_{C1}, V_{C2}, V_{C3}, FB, CTRL1, CTRL2, CTRL3, LED_ISP and LED_ISN.
- The compensation components should be placed as close as possible to the VC pins and the LT3744's exposed pad, and always connected to VEE.
- The sense lines from the R_{SLED} resistor should be routed together with minimal routing lengths to the LED_ISN and LED_ISP pins. For best accuracy, the LED_ISN and LED_ISP sense lines should connect to the R_{SLED} resistor with Kelvin connections.
- The sense lines from the R_S resistor should be routed together with minimal routing lengths to the ISN and ISP pins.
- The negative terminals of the input and output bypass capacitors should be placed as close as possible to each other and always tied to VEE (power ground).
- The $INTV_{CC}$ bypass capacitor should be placed close to the $INTV_{CC}$ pin and VEE (power ground). For stability and noise immunity, use at least a 10µF capacitor directly at the $INTV_{CC}$ pin.

TYPICAL APPLICATIONS

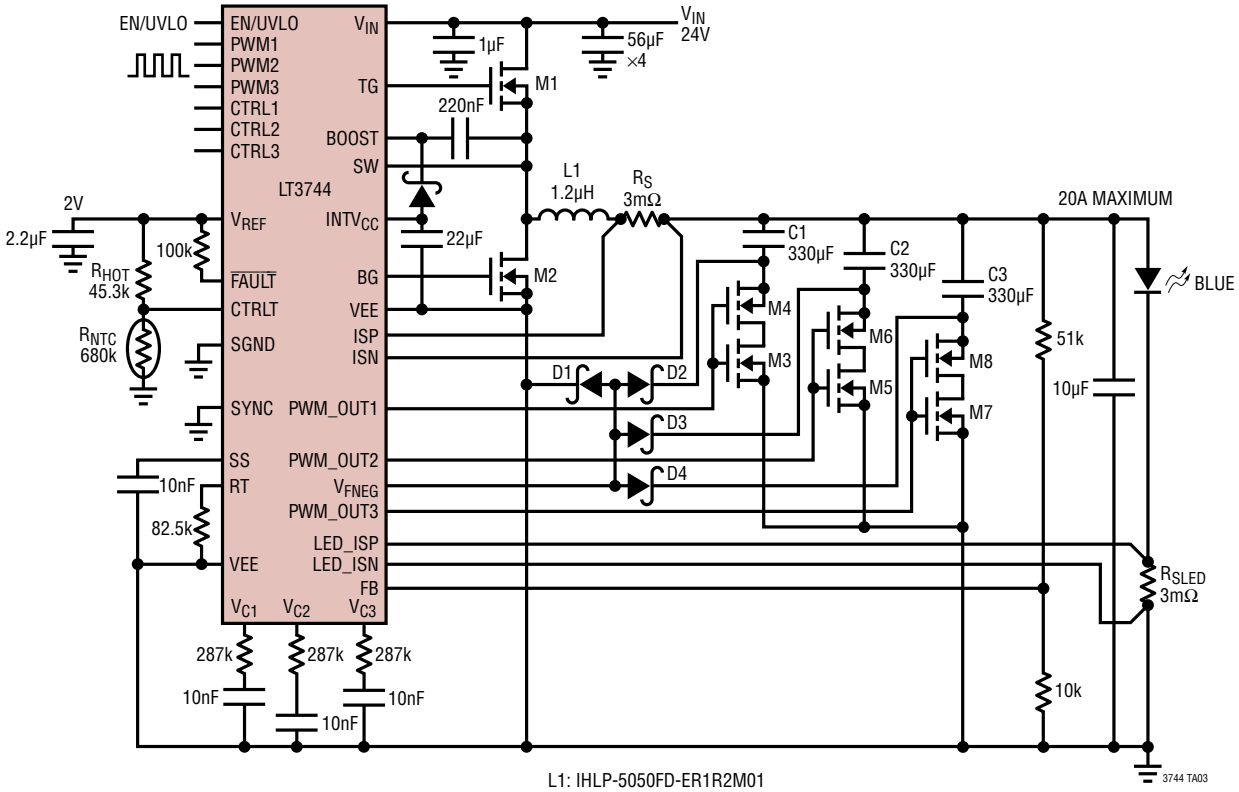
LED Driver for 3-Current-Level Single LED, Common Anode, Color Mixing Applications



L1: MSS1048-682NL
R_S: WSLP20103L000F
R_{SLED}: WSLP1206R0120D
M1: BSC010NE2LSI
M2: SiR438DP
M3, M4, M5, M6, M7, M8: Si7234DP
D1, D2. D3, D4: BAT54A
D5: PMEG4010

TYPICAL APPLICATIONS

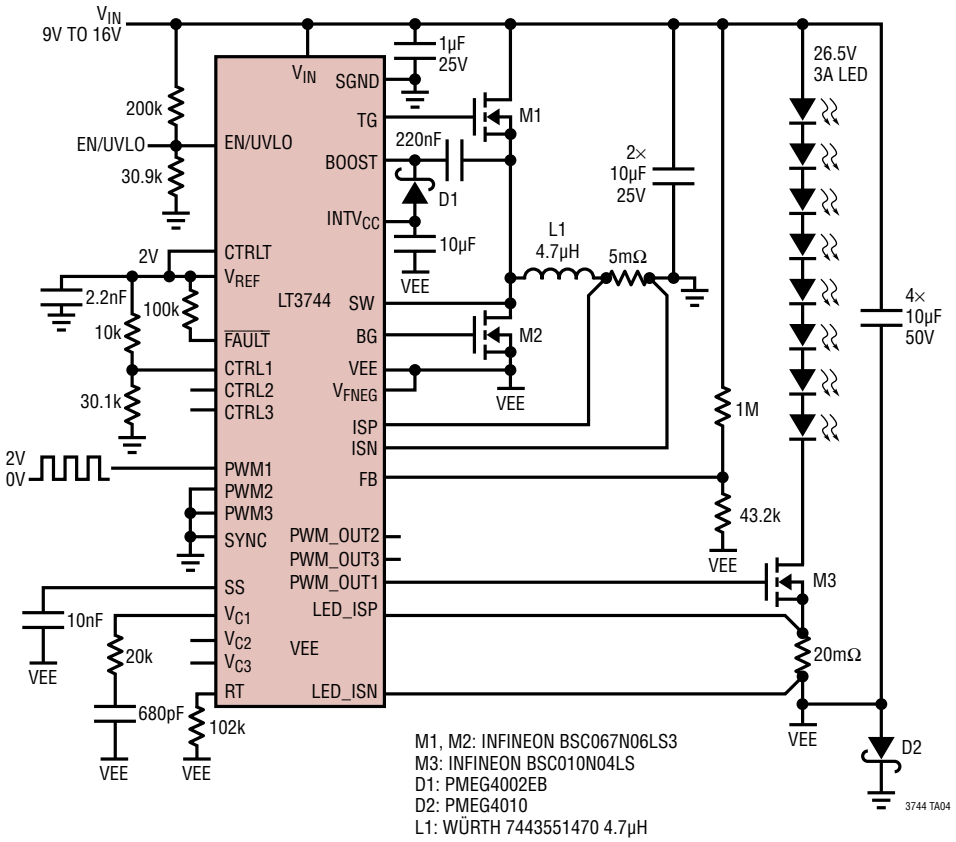
LED Driver for 3-Current-Level Single LED, Color Mixing Applications



L1: IHLP-5050FD-ER1R2M01
R_S: WSL28163L000D
R_{SLED}: WSL28163L000J
M1: BSC050NE2LS
M2: SiR438DP
M3, M4, M5, M6, M7, M8: Si7234DP
D1, D2. D3, D4: BAT54A
C1, C2, C3: 10T4B330M

TYPICAL APPLICATIONS

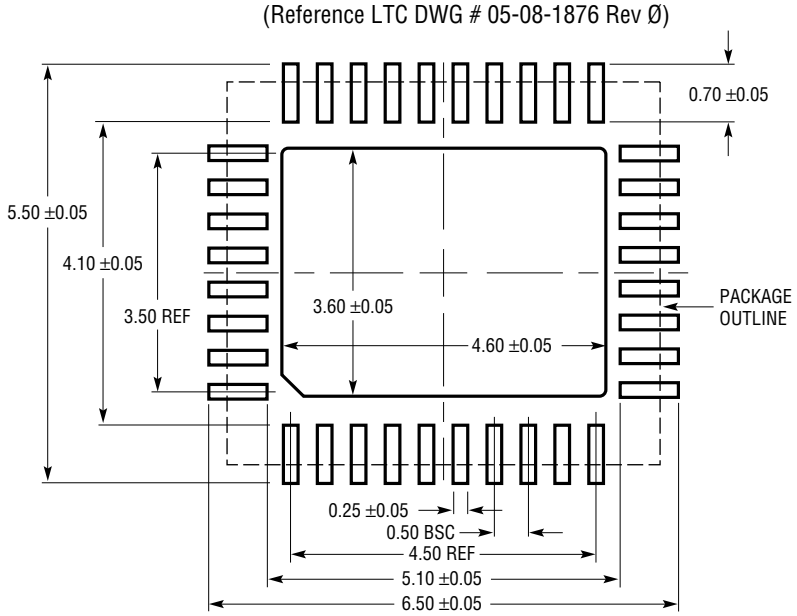
Boost Mode 3A LED Driver with 98% Efficiency



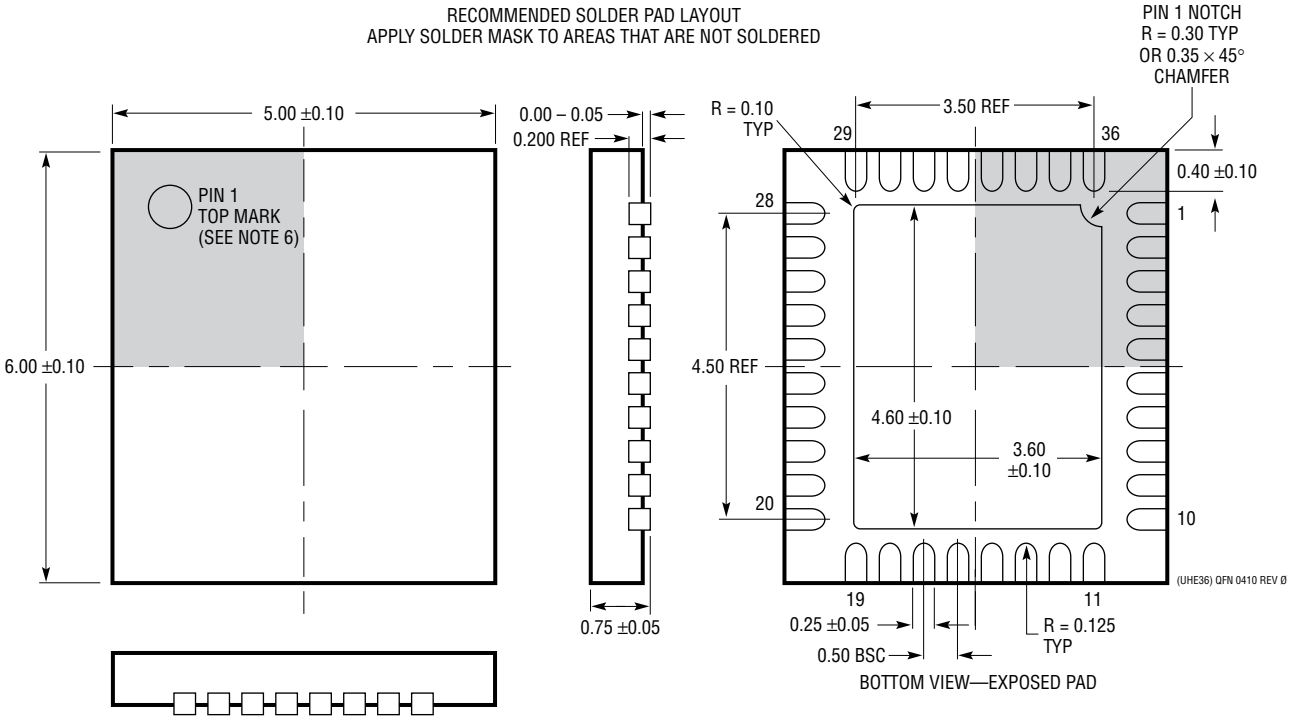
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

UHE Package
36-Lead Plastic QFN (5mm × 6mm)
(Reference LTC DWG # 05-08-1876 Rev Ø)



RECOMMENDED SOLDER PAD LAYOUT
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	9/15	Amended Absolute Maximum Ratings	2
		Corrected Figure 7 description	19
		Corrected Figure 9 description	20