60V Synchronous Boost LED Controller

FEATURES

- **3000:1 External PWM Dimming**
- **250:1 Internal PWM Dimming**
- **Wide V_{IN} Operating Range: 2.5V to 38.5V**
- **Synchronous Boost Output Voltage up to 60V**
- **Spread-Spectrum Frequency Modulation for Lower EMI**
- **PMOS Switch Driver for PWM and Output Disconnect**
- Constant Current (±3.5%) Regulation
- Constant Voltage (±2%) Regulation
- Rail-to-Rail LED Current Sense: 0V to 60V
- Programmable V_{IN} Undervoltage Lockout
- Analog Dimming via Two Control Pins
- 100kHz to 1MHz Operation
- Programmable Open LED Protection with $\overline{\text{OPENLED}}$ Flag
- Short-Circuit Protection and $\overline{\text{SHORTLED}}$ Flag
- Drives LEDs in Boost, SEPIC, Buck Mode, or Buck-Boost Mode Configurations
- 28 Lead TSSOP and QFN (4mm × 5mm) Exposed Pad Packages

APPLICATIONS

- Industrial and Automotive Lighting
- Accurate Current-Limited Voltage Regulators

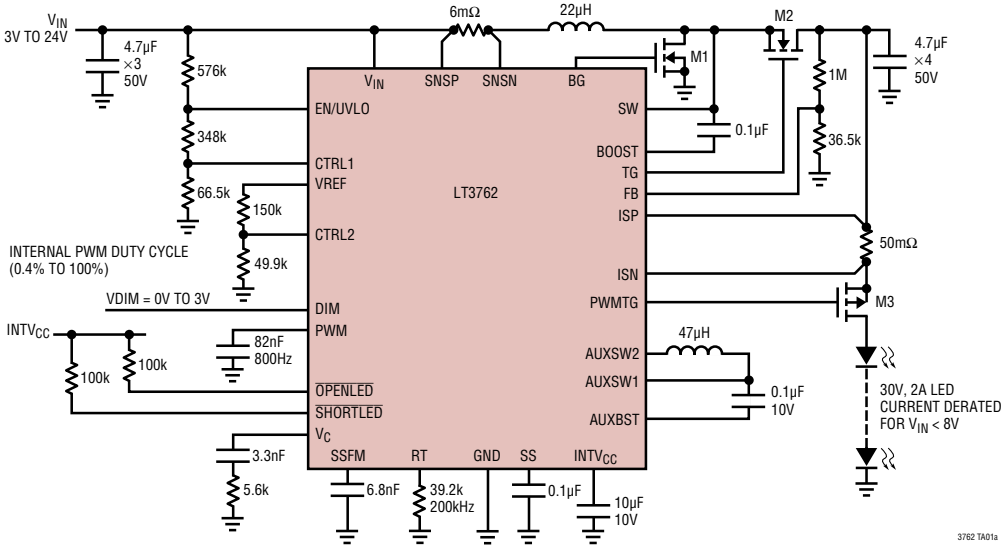
DESCRIPTION

The LT®3762 is a synchronous DC/DC controller designed to operate as a constant-current source and constant-voltage regulator. It features a programmable internal PWM dimming signal generator and a synchronous gate driver. The LT3762 is ideally suited for driving high current LEDs with high efficiency and reduced power loss. Rail-to-rail switch current sensing enables synchronous boost topologies and nonsynchronous topologies such as SEPIC. A voltage feedback pin serves as the input for several LED protection features and also allows the converter to operate as a constant-voltage source.

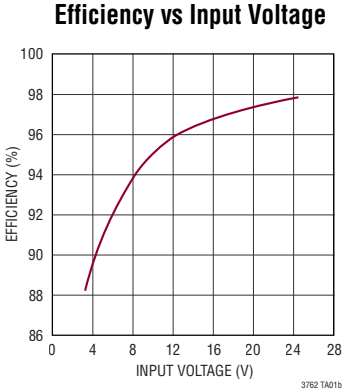
A frequency adjust pin allows the user to program the frequency from 100kHz to 1MHz to optimize efficiency, performance and external component size. Adding a capacitor at SSFM pin activates the Spread-Spectrum Modulation feature to reduce EMI. The LT3762 also includes an integrated DC/DC converter to efficiently produce a regulated 7.5V supply for the N-channel MOSFET gate drivers. The PWM pin controls PWMTG to drive the P-channel MOSFET, allowing a high PWM dimming range (3000:1) and providing LED overcurrent protection and short-circuit protected boost capability.

TYPICAL APPLICATION

98% Efficient 60W Synchronous Boost LED Driver with 3V Minimum Input Voltage



Efficiency vs Input Voltage



Rev 0

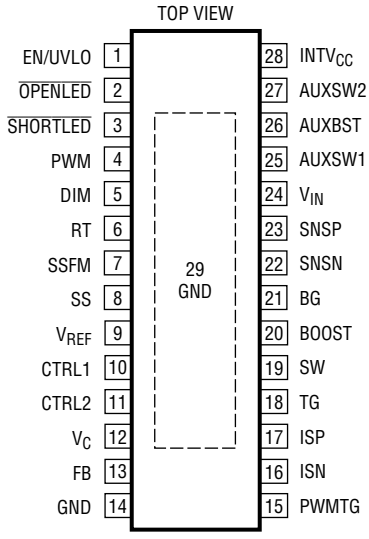
ABSOLUTE MAXIMUM RATINGS

(Note 1)

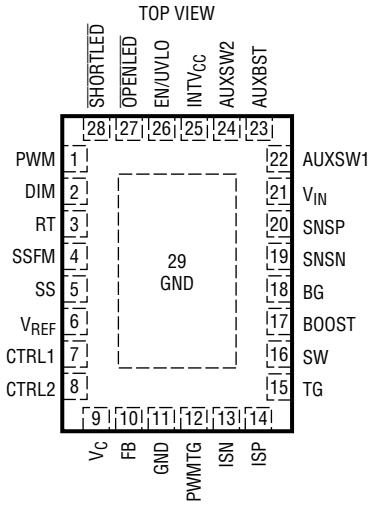
ISP, ISN 80V
V_{IN}, EN/UVLO, SNSP, SNSN, SW (Note 7) 60V
CTRL1, CTRL2, $\overline{OPENLED}$, $\overline{SHORTLED}$ 15V
FB, PWM, $INTV_{CC}$, DIM 8V
V_C, V_{REF}, SS, SSFM 3V

AUXSW1, AUXSW2, TG, BG, PWMTG
BOOST, AUXBST, RT ..... (Note2)
Operating Junction Temperature Range (Note 3, 4)
LT3762E/LT3762I ..... –40°C to 125°C
LT3762H ..... –40°C to 150°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



FE PACKAGE
28-LEAD PLASTIC TSSOP
θ_{JA} = 30°C/W, θ_{JC} = 10°C/W
EXPOSED PAD (PIN 29) IS GND, MUST BE SOLDERED TO PCB



UFD PACKAGE
28-LEAD (4mm × 5mm) PLASTIC QFN
θ_{JA} = 43°C/W, θ_{JC} = 3.4°C/W
EXPOSED PAD (PIN 29) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

http://www.linear.com/product/LT3762#orderinfo

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3762EFE#PBF	LT3762EFE#TRPBF	LT3762	28-Lead Plastic TSSOP	-40°C to 125°C
LT3762IFE#PBF	LT3762IFE#TRPBF	LT3762	28-Lead Plastic TSSOP	-40°C to 125°C
LT3762HFE#PBF	LT3762HFE#TRPBF	LT3762	28-Lead Plastic TSSOP	-40°C to 150°C
LT3762EUFD#PBF	LT3762EUFD#TRPBF	3762	28-Lead Plastic QFN	-40°C to 125°C
LT3762IUFD#PBF	LT3762IUFD#TRPBF	3762	28-Lead Plastic QFN	-40°C to 125°C
LT3762HUFD#PBF	LT3762HUFD#TRPBF	3762	28-Lead Plastic QFN	-40°C to 150°C

Consult ADI Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 24V; CTRL1, CTRL2, PWM = 2V; SW, SSFM = 0V; $INTV_{CC}$, BOOST, DIM = 8V unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN} Minimum Operation Voltage		●			2.5	V
V_{IN} Overvoltage Lockout	Rising V_{IN} Falling Hysteresis	●	38.5	41 1	43.5	V V
V_{IN} Shutdown I_Q	EN/UVLO = 0V EN/UVLO = 1.15V			0.1	1 13	µA µA
V_{IN} Operating I_Q (Not Switching)	R_T = 82.5k, FB = 1.5V, PWM = 0V				500	µA
$INTV_{CC}$ Operating I_Q (Not Switching)	PWM = 0V			3		mA
V_{REF} Voltage	0µA ≤ I_{VREF} ≤ 250µA	●	1.96	2	2.04	V
V_{REF} Line Regulation	2.5V ≤ V_{IN} ≤ 38.5V	●		0.006		%/V
Switch Current Sense Limit Threshold	SNSN = 0V, 24V	●	72	80	88	mV
Current Sense Zero Cross Detect Threshold, $V_{SNSP–SNSN}$	SNSN = 24V, Falling		3	7	10	mV
Current Sense Zero Cross Detect Threshold Hysteresis $V_{SNSP-SNSN}$	SNSN = 24V			2.5		mV
$V_{SNSP, SNSN}$ Synchronous Driver Enable	$V_{SNSP–SNSN}$ > 15mV				2	V
SNSP, SNSN Input Bias Current (Low-Side Sensing)	Combined Current Out of Pin, SNSP = SNSN = 0V			22		µA
SNSP, SNSN Input Bias Current (High-Side Sensing)	Combined Current into Pin, SNSP = SNSN = 24V			125		µA
SS Sourcing Current	SS = 0V			28		µA
SS Sinking Current	SS = 2V			2.8		µA
Error Amplifier						
Full-Scale LED Current Sense Threshold ($V_{ISP-ISN}$)	CTRL ≥ 1.2V, ISP = 48V	●	240	249	257	mV
Full-Scale LED Current Sense Threshold ($V_{ISP-ISN}$)	CTRL ≥ 1.2V, ISN = GND (Ground Sensing)	●	232	245	255	mV
1/10th LED Current Sense Threshold ($V_{ISP-ISN}$)	CTRL = 0.2V, ISP = 48V	●	18	22.5	27	mV
1/10th LED Current Sense Threshold ($V_{ISP-ISN}$)	CTRL = 0.2V, ISN = GND (Ground Sensing)	●	10	21	29	mV
½ LED Current Sense Threshold ($V_{ISP-ISN}$)	CTRL = 0.6V, ISP = 48V	●	118	122	126	mV
½ LED Current Sense Threshold ($V_{ISP-ISN}$)	CTRL = 0.6V, ISN = GND (Ground Sensing)	●	110	120	130	mV
ISP/ISN Overcurrent Threshold	ISP = 48V			600		mV
ISP/ISN Current Sense Amplifier Input Common Mode Range (V_{ISN})			0		60	V
ISP/ISN Input Bias Current (Combined)	PWM = 5V (Active), ISP = 48V PWM = 0V (Standby), ISP = 48V			850 0	 1	µA µA
ISP/ISN Current Sense Amplifier gm	$V_{ISP-ISN}$ = 250mV, ISP = 48V			120		µS
CTRL1,2 Input Bias Current	CTRL = 0V			30		nA
V_C Output Impedance	0.9V≤ V_C ≤ 1.5V			11		MΩ
V_C Standby Input Bias Current	PWM = 0V		–20		20	nA
FB Regulation Voltage (V_{FB})	ISP = ISN = 48V, 0V	●	1.225	1.25	1.275	V
FB Amplifier g_m	FB = V_{FB}, ISP = ISN = 48V			500		µS
FB Open LED Threshold Rising	$\overline{OPENLED}$ Falling, ISP Tied to ISN	●	V_{FB}^- 60mV	V_{FB}^- 50mV	V_{FB}^- 40mV	V
FB Shorted LED Threshold Falling	$\overline{SHORTLED}$ Falling	●		300	350	mV
FB Input Bias Current	FB = 1V			200		nA
C/10 Inhibit for $\overline{OPENLED}$ Assertion ($V_{ISP-ISN}$)	ISN = 0V, 48V		12	25	39	mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 24V; CTRL1, CTRL2, PWM = 2V; SW, SSFM = 0V; $INTV_{CC}$, BOOST, DIM = 8V unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
FB Overvoltage Threshold Rising	PWMTG rising	●	V_{FB}+ 55mV	V_{FB}+ 65mV	V_{FB}+ 75mV	V
V_C Current Mode Gain (ΔV_{VC} / $\Delta V_{SNSP-SNSN}$)				4		V/V
Oscillator						
Switching Frequency (f_{SWITCH})	R_T = 82.5kΩ R_T = 19.6kΩ R_T = 6.65kΩ	● ● ●	90 340 980	105 400 1080	125 460 1240	kHz
Switching Frequency Modulation	V_{SSFM} = 2V			–30		$\%f_{SWITCH}$
SSFM Input Disable Threshold					0.95	V
SSFM Pin Sink/Source Current	V_{SSFM} = 1V, 2V			12		µA
SSFM Peak-to-Peak Triangle Amplitude				1		V
MOSFET Gate Drivers						
BG Minimum On Time				230		ns
BG Minimum Off Time				150		ns
TG Minimum On Time (Note 5)				130		ns
BG Drive On Voltage			V_{INTVCC} –125mV	V_{INTVCC}		V
BG Drive Off Voltage					0.1	V
TG Drive On Voltage	SW = 0V		V_{BOOST} –125mV	V_{BOOST}		V
TG Drive Off Voltage	SW = 0V				0.1	V
TG, BG Drive Rise Time	C_{TG} = C_{BG} = 2.7nF			20		ns
TG, BG Drive Fall Time	C_{TG} = C_{BG} = 2,7nF			20		ns
PWMTG Driver Output Rise Time	CL = 300pF			50		ns
PWMTG Driver Output Fall Time	CL = 300pF			100		ns
PWMTG On Voltage (V_{ISP} – V_{PWMTG})	PWM = 2V			7	8	V
PWMTG Off Voltage (V_{ISP} – V_{PWMTG})	PWM = 0V			0	0.3	V
BOOST UVLO	V_{BOOST} – V_{SW}			4.2		V
Internal Power Supply						
INTVcc Regulation Voltage		●	7.3	7.5	7.7	V
INTVcc Undervoltage Lockout Threshold	Falling INTVcc Rising Hysteresis	●	5.1	5.3 0.4	5.5	V V
INTVcc Line Regulation (ΔV_{INTVCC} / ΔV_{IN})	2.5V < V_{IN} < 38.5V			0.002		%/V
Logic Inputs/Outputs						
EN/UVLO Threshold Voltage Falling		●	1.185	1.220	1.245	V
EN/UVLO Rising Hysteresis				6		mV
EN/UVLO Input Low Voltage	I_{VIN} Drops Below 1µA				0.4	V
EN/UVLO Pin Bias Current Low	EN/UVLO = 1.15V	●	1.4	2	2.3	µA
$\overline{OPENLED}$ Output Low	$I_{\overline{OPENLED}}$ = 500µA			200	300	mV
$\overline{SHORTLED}$ Output Low	$I_{\overline{SHORTLED}}$ = 500µA			200	300	mV
$\overline{OPENLED}$ Pin Bias Current High	$\overline{OPENLED}$ = 1.30V			10	100	nA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 24V; CTRL1, CTRL2, PWM = 2V; SW, SSFM = 0V; $INTV_{CC}$, BOOST, DIM = 8V unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$\overline{\text{SHORTLED}}$ Pin Bias Current High	$\overline{\text{SHORTLED}}$ = 1.30V			10	100	nA
EN/UVLO Pin Bias Current High	EN/UVLO = 1.30V			10	100	nA
PWM Pin Signal Generator						
PWM Falling Threshold	DIM = 4V	●	1.25	1.3	1.35	V
PWM Threshold Hysteresis (V_{PWMHYS})	DIM = 4V	●	0.35	0.43	0.6	V
PWM Pull-Up Current (I_{PWMUP})	DIM = 3.1V, PWM = 0V (100% Duty Cycle)			5		µA
DIM Input Current	DIM = 5V				1	µA
PWM Signal Generator Duty Ratio (Note 6)	DIM = 0V DIM = 1.19V DIM = 1.42V DIM = 1.76V DIM = 2.1V		0.22 3.7 7 17 37	0.32 5 10 25 50	0.4 6.8 13 33 58	% % % % %
DIM Input Internal PWM Disable Threshold	RisingDIM Falling hysteresis	●	2.9	3.0 25	3.1	V mV
PWM Signal Generator Frequency	PWM = 82nF to GND, DIM = 0.75V, 2.5V		570	800	1050	Hz

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Do not apply a positive or negative voltage or current source to these pins, otherwise, permanent damage may occur.

Note 3: The LT3762E is guaranteed to meet specified performance from 0ºC to 125ºC. Specifications over the –40ºC to 125ºC operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT3762I is guaranteed to meet performance specifications over the –40ºC to 125ºC operating junction temperature range. The LT3762H is guaranteed over the full –40ºC to 150ºC operating junction temperature range. High junction temperatures degrade operating lifetimes. Operating lifetime is derated at junction temperatures greater than 125ºC.

Note 4: The LT3762 includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed the maximum operating junction temperature when overtemperature protection is active. Continuous operation above the specified maximum junction temperature may impair device reliability.

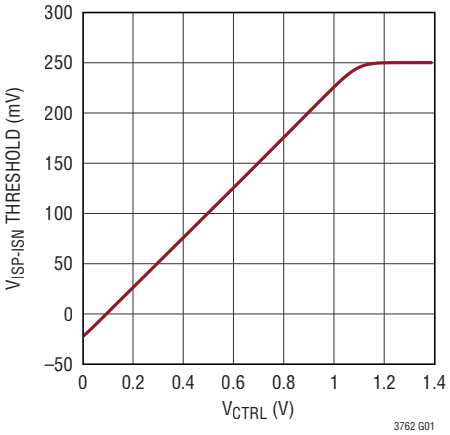
Note 5: Guaranteed by design. A TG pulse will be generated only if the BG off-time is greater than 310ns (typ). See TG Synchronous Driver under Duty Cycle Considerations in the Applications Information section.

Note 6: PWM Signal Generator Duty Ratio is calculated by:
Duty = I_{PWMUP} / (I_{PWMUP} + I_{PWMDN}).

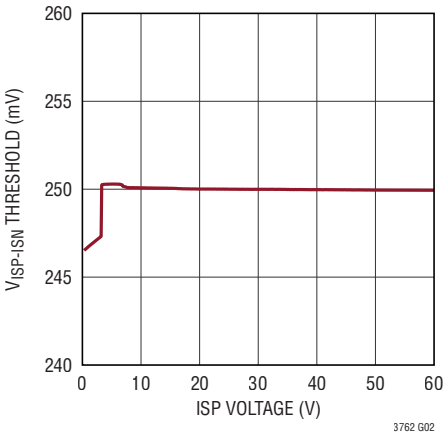
Note 7: For operation at T_j < 125°C, the absolute maximum voltage at V_{IN}, EN/UVLO, SNSP, SNSN, and SW pins is 38.5V for continuous operation and 60V for up to one second nonrepetitive transients. For operation at Tj > 125°C, the absolute maximum voltage at V_{IN}, EN/UVLO, SNSP, SNSN, and SW is 38.5V.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

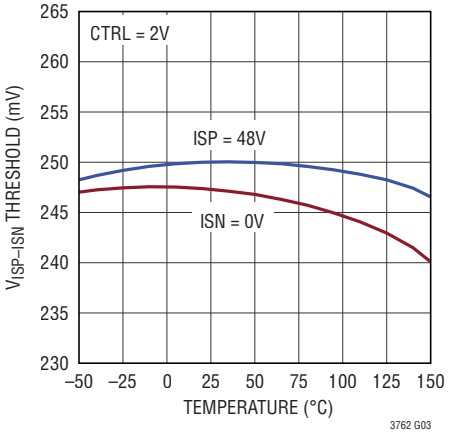
$V_{ISP-ISN}$ Threshold vs CTRL Voltage



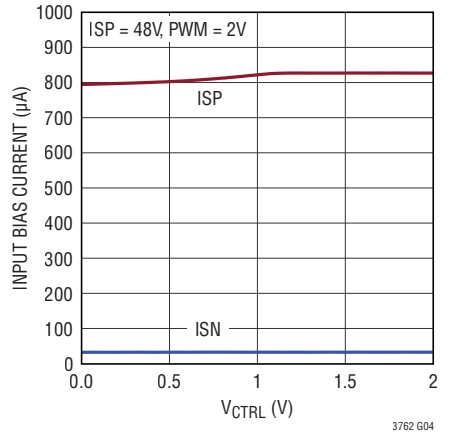
$V_{ISP-ISN}$ Threshold vs ISP Voltage



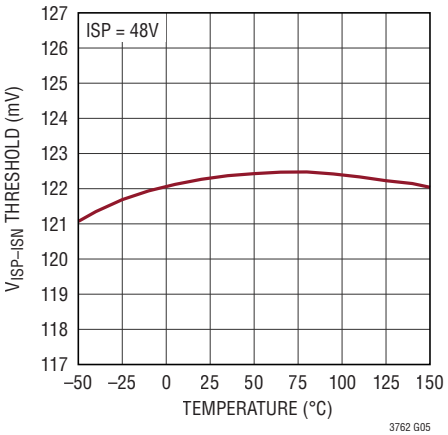
$V_{ISP-ISN}$ Threshold vs Temperature



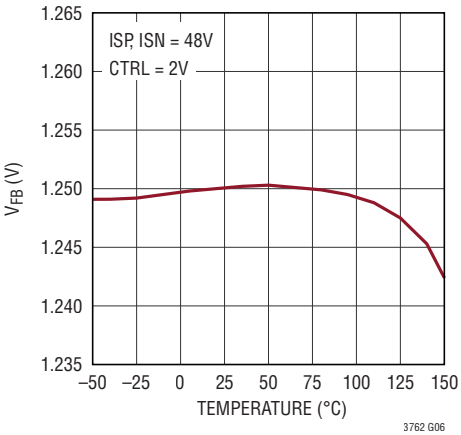
ISP/ISN Bias Current vs CTRL Voltage



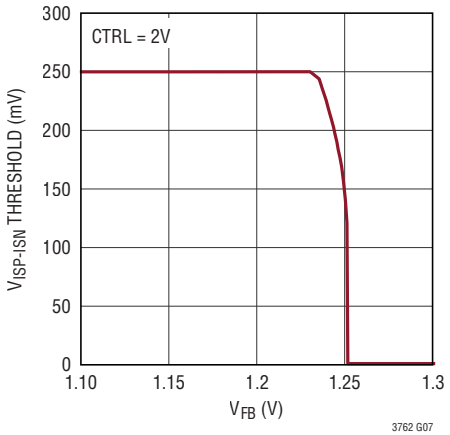
$V_{ISP-ISN}$ Threshold vs Temperature, CTRL = 0.6V



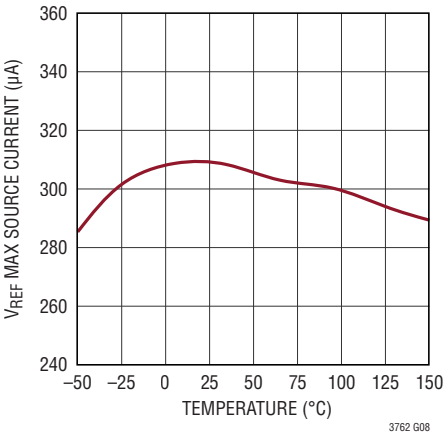
FB Regulation Voltage (V_{FB}) vs Temperature



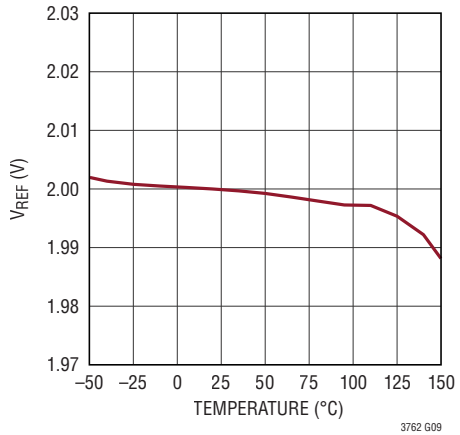
$V_{ISP-ISN}$ Threshold vs FB Voltage



V_{REF} Source Current vs Temperature

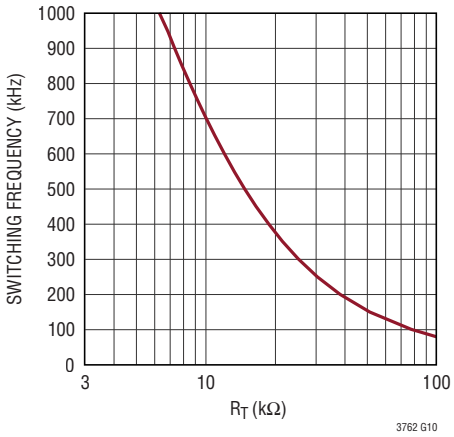


V_{REF} Voltage vs Temperature

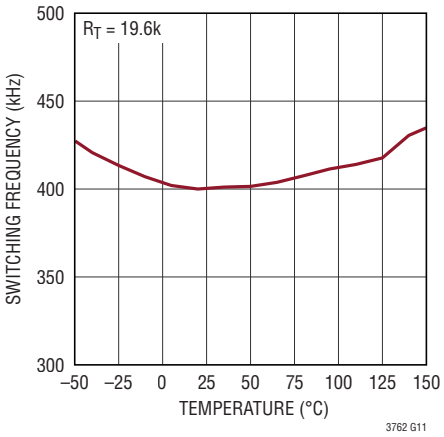


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

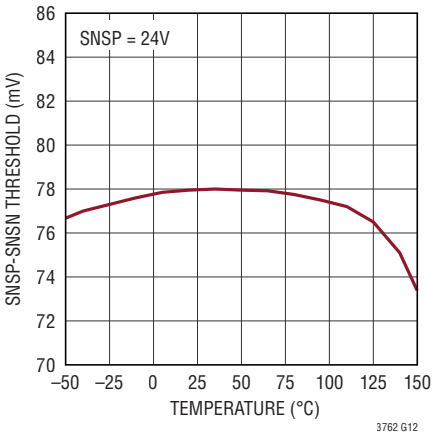
Switching Frequency vs R_T



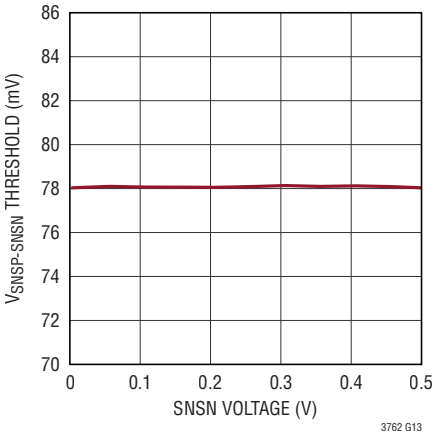
Switching Frequency vs Temperature



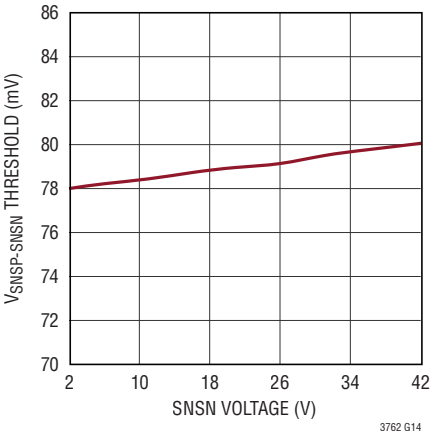
SNSP–SNSN Current Limit Threshold vs Temperature



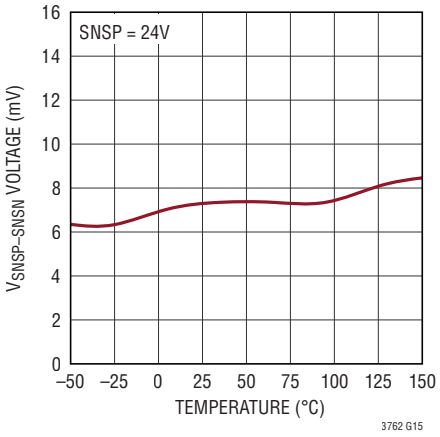
$V_{SNSP–SNSN}$ Current Limit Threshold vs SNSN Voltage, SNSN < 0.5V



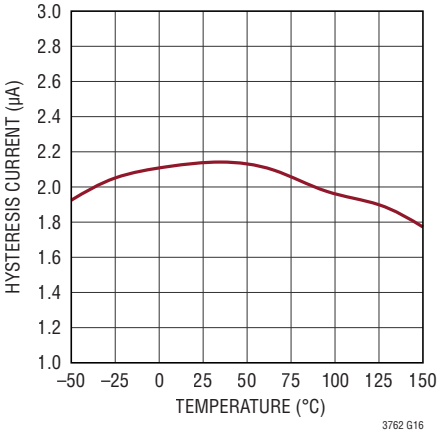
$V_{SNSP–SNSN}$ Current Limit Threshold vs SNSN Voltage, SNSN > 2V



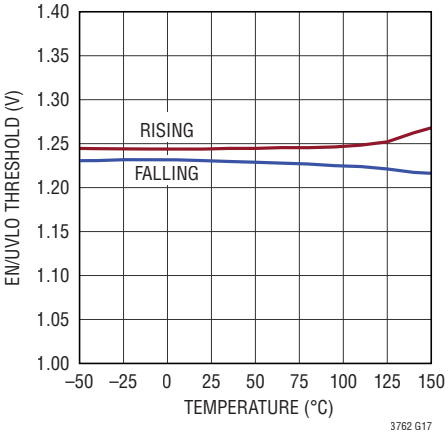
SNSP–SNSN Zero Cross Threshold vs Temperature



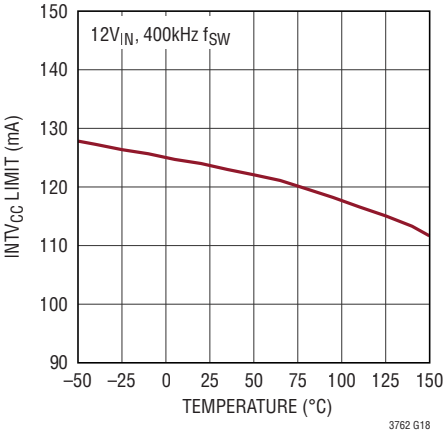
EN/UVLO Hysteresis Current vs Temperature



EN/UVLO Threshold vs Temperature

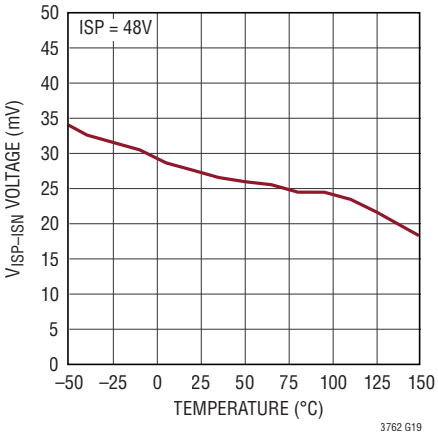


$INTV_{CC}$ Maximum Source Current vs Temperature

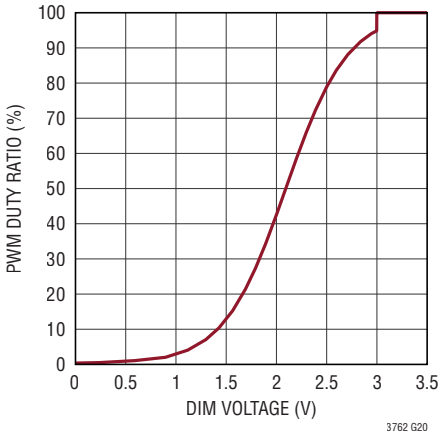


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

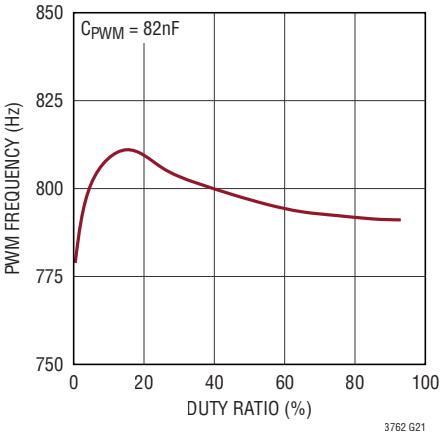
$V_{ISP-ISN}$ C/10 Threshold vs Temperature



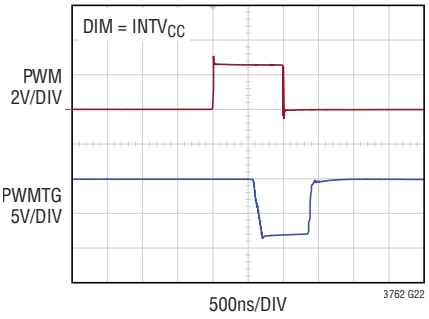
PWM Signal Generator Duty Ratio vs DIM Voltage



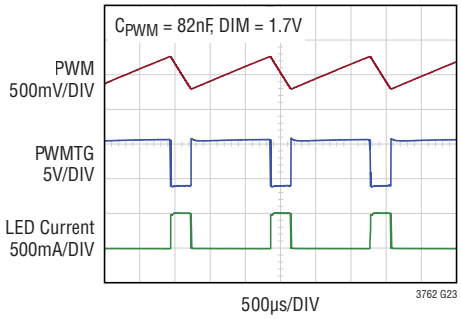
PWM Generator Frequency vs DIM Voltage



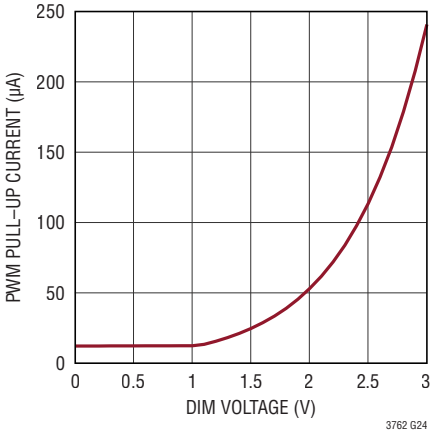
PWMTG When PWM Generator Disabled (External PWM Control)



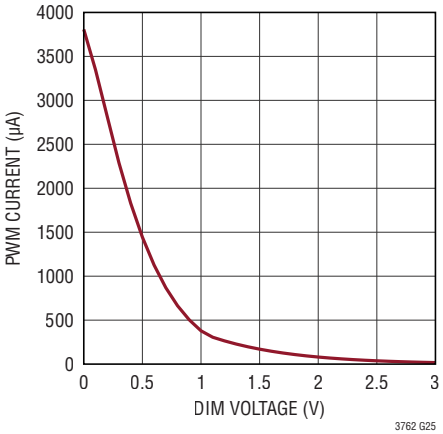
PWMTG When PWM Generator Enabled (Internal PWM Control)



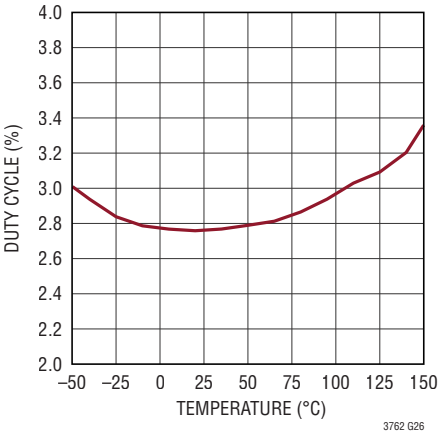
PWM Pull-Up Current vs DIM Voltage



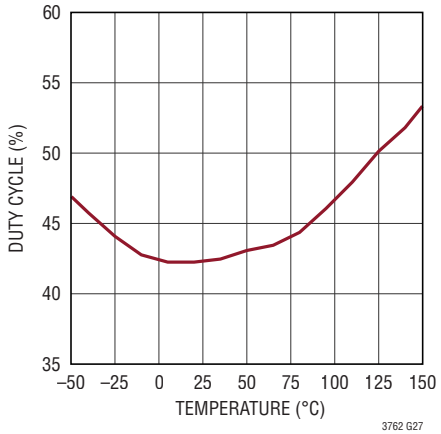
PWM Pull-Down Current vs DIM Voltage



PWMTG Duty Ratio vs Temperature, V_{DIM} = 1V

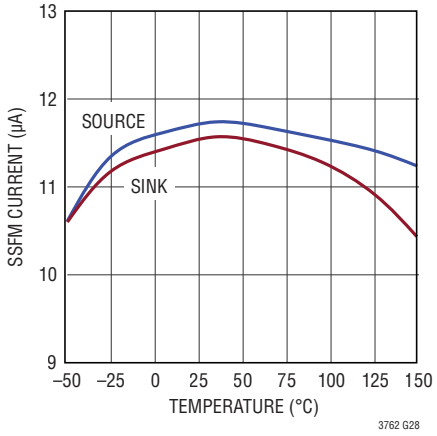


PWMTG Duty Ratio vs Temperature, V_{DIM} = 2V

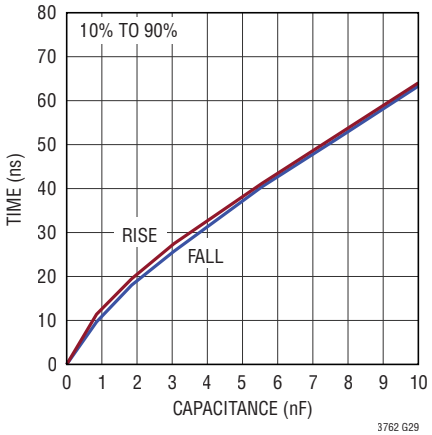


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

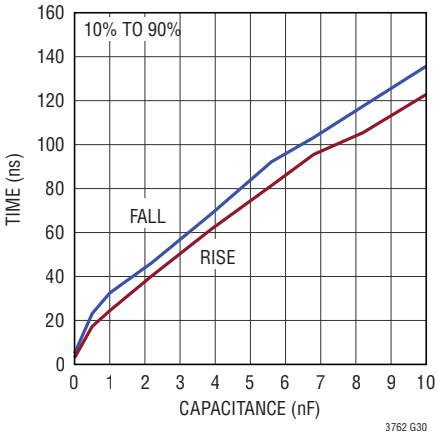
SSFM Current vs Temperature



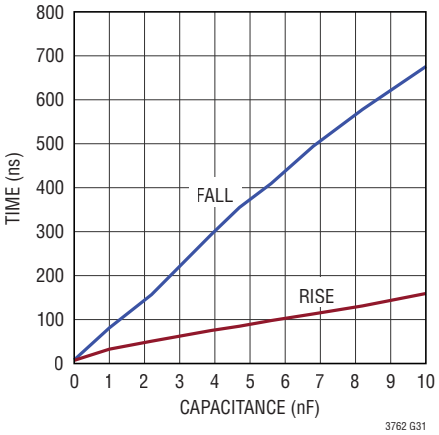
BG Rise/Fall Time vs Capacitance



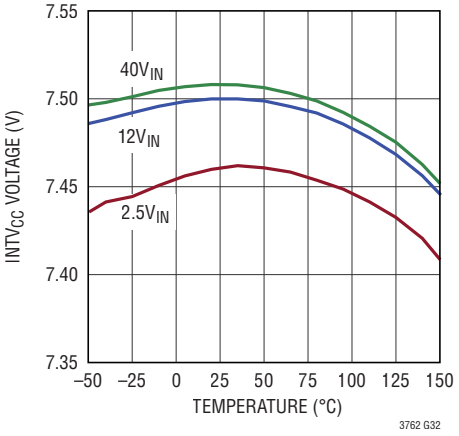
TG Rise/Fall Time vs Capacitance



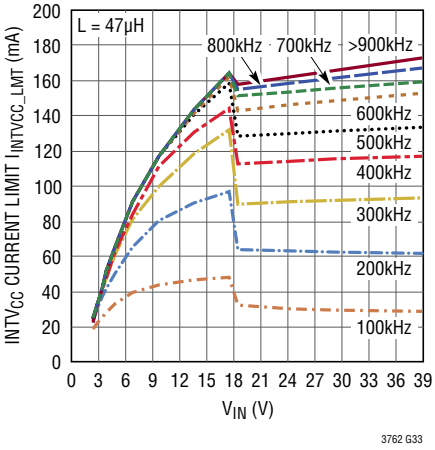
PWMTG Rise/Fall Time vs Capacitance



$INTV_{CC}$ vs Temperature, V_{IN}



$INTV_{CC}$ Maximum Current vs V_{IN}, f_{SW}



PIN FUNCTIONS

V_{IN}: Power Supply for Internal Loads and $INTV_{CC}$ Regulator. Must be locally bypassed with a 1µF (or larger) low ESR capacitor placed close to the pin.

EN/UVLO: Shutdown and Undervoltage Detect Pin. An accurate 1.22V (nominal) falling threshold with externally programmable hysteresis detects when power is okay to enable switching. Rising hysteresis is generated by the external resistor divider and an accurate internal 2µA pull-down current. Tie to 0.4V, or less, to disable the device and reduce V_{IN} quiescent current below 1µA.

$INTV_{CC}$: $INTV_{CC}$ is the internal power supply output voltage node that provides supply for control circuits and NMOS gate drivers. This pin must be bypassed with a 10µF ceramic capacitor placed close to the pin.

V_C: Transconductance Error Amplifier output pin used to stabilize the switching regulator control loop with an RC network. The V_C pin is high impedance when PWM is low. This feature allows the V_C pin to store the demand current state variable for the next PWM high transition. Connect a capacitor between this pin and GND; a resistor in series with the capacitor is recommended for fast transient response.

FB: Voltage Loop Feedback Pin. FB is intended for constant-voltage regulation or for LED protection and open LED detection. The internal transconductance amplifier with output V_C will regulate FB to 1.25V (nominal) through the DC/DC converter. If the FB input exceeds the regulation voltage, V_{FB}, minus 50mV (typical) and the voltage between ISP and ISN has dropped below the C/10 threshold of 25mV (typical), the $\overline{OPENLED}$ pull-down is asserted. This action may signal an open LED fault. If FB is driven above the FB overvoltage threshold, the TG and BG pins will be driven low and PWMTG driven high to protect the LEDs from an overcurrent event. If FB < 300mV (nominal) or $V_{ISP-ISN}$ > 600mV, $\overline{SHORTLED}$ pull-down is asserted. Do not leave the FB pin open.

RT: Switching Frequency Adjustment Pin. Set the frequency using a resistor to GND (for resistor values, see the Typical Performance curve or Table 2). Do not leave the RT pin open.

SS: Soft-Start Pin. This pin modulates oscillator frequency and compensation pin voltage (V_C) clamp. The soft-start interval is set with an external capacitor. The pin has a 28µA (typical) pull-up current source to an internal 2.5V rail. This pin can be used as a fault timer. Provided the SS pin has exceeded 1.7V, the pull-up current source is disabled and a 2.8µA pull-down current enabled when anyone of the following fault conditions happen:

1. LED overcurrent ($V_{ISP-ISN}$ > 600mV)
2. $INTV_{CC}$ undervoltage
3. Output short (FB < 0.3V)
4. Thermal limit

The SS pin must be discharged below 0.2V to reinitiate a soft-start cycle. Switching is disabled until SS begins to recharge. It is important to select a capacitor large enough that FB can exceed 0.4V under normal load conditions before SS exceeds 1.7V. Do not leave this pin open.

BG: The BG pin is the high current gate drive for the low-side N-channel MOSFET.

TG: The TG pin is the high current gate drive for the synchronous N-channel MOSFET.

SW: The SW pin is the high current return path of the synchronous MOSFET driver and is externally connected to the negative terminal of the BOOST capacitor. If not using the synchronous FET, tie this pin to ground.

SNSP: The Positive Current Sense Input for the Switch Control Loop. Kelvin connect the SNSP pin to the positive terminal of the switch current sense resistor. Connect to V_{IN} (after C_{VIN}) for synchronous applications where sense resistor is in series with the inductor at the supply side. Connect to the source of low-side FET for nonsynchronous applications such as SEPIC.

PIN FUNCTIONS

SNSN: The Negative Current Sense Input for the switch control loop. For synchronous applications, Kelvin connect the SNSN pin to the negative terminal of the switch current sense resistor in series with the inductor at the supply side. For non-synchronous applications such as SEPIC, Kelvin connect to the ground side of the sense resistor.

ISN: Connection Point for the Negative Terminal of the Current Feedback Resistor.

ISP: Connection Point for the Positive Terminal of the Current Feedback Resistor. Input bias current depends upon CTRL pin voltage. When it is greater than $INTV_{CC}$ it flows into the pin. Below $INTV_{CC}$, ISP bias current decreases until it flows out of the pin. If the difference between ISP and ISN exceeds 600mV (typical), then an overcurrent event is detected. In response to this event, the BG and TG pins are driven low and PWMTG is driven high to protect the switching regulator. Also during an overcurrent event, the $\overline{SHORTLED}$ flag is asserted.

PWM: A signal low turns off switcher, idles the oscillator and disconnects the V_C pin from all internal loads. $V_{PWMTG} = V_{ISP} - 7V$ when PWM is above its high threshold, except in fault conditions. The PWM pin can be driven with a digital signal to cause pulse width modulation (PWM) dimming of an LED load. During start-up when SS is below 0.8V, the first rising edge of PWM enables switching which continues until $V_{ISP-ISN} \geq 25mV$ or $SS \geq 0.8V$. Connecting a capacitor from PWM pin to GND invokes a self-driving oscillator where internal pull-up and pull-down currents set a duty ratio at PWMTG pin for dimming LEDs. The magnitude of the pull-up/down currents is set by the voltage at the DIM pin and is illustrated in the Typical Performance Characteristics section. The capacitor on PWM sets the frequency of the dimming signal. If not used, connect the PWM and DIM pins to $INTV_{CC}$.

AUXSW1: The AUXSW1 pin is a switching node of the auxiliary bias supply. Connect the pin to the auxiliary bias supply inductor and to the AUXBST pin with a 0.1µF or larger ceramic capacitor.

AUXSW2: The AUXSW2 node is a switching node of the $INTV_{CC}$ supply and is connected to the auxiliary bias supply inductor.

AUXBST: The AUXBST pin provides drive voltage to the $INTV_{CC}$ supply and is connected to the AUXSW1 pin through a 0.1µF or larger ceramic capacitor.

$\overline{OPENLED}$: An open-collector pull-down on this pin asserts if the FB input is greater than the FB regulation voltage (V_{FB}) minus 50mV (typical) AND the difference between current sense inputs ISP and ISN is less than 25mV. The pin requires an external pull-up resistor, usually to $INTV_{CC}$. When the PWM input is low and the DC/DC converter is idle, the $\overline{OPENLED}$ condition is latched to the last valid state when the PWM input was high. When PWM input goes high again, the $\overline{OPENLED}$ pin will be updated. This pin may be used to report transition from constant current regulation to constant voltage regulation modes, for instance in a charger or current limited voltage supply.

BOOST: The BOOST pin is the supply for the bootstrapped TG pin gate drive and is externally connected to a low ESR ceramic BOOST capacitor (0.1µF typ) referenced to the SW pin. An internal Schottky connects BOOST to $INTV_{CC}$ for charging this capacitor when SW is pulled to ground by the bottom FET. If not using a synchronous FET, tie this pin to $INTV_{CC}$.

V_{REF}: Reference Output Pin. Can supply up to 250µA. This pin can drive a resistor divider for the CTRL1, CTRL2 or DIM pins for dimming or for temperature limit/compensation of LED loads. The normal output voltage is 2V.

CTRL1, CTRL2: Current Sense Threshold Adjustment Pin. Constant current regulation point $V_{ISP-ISN}$ is one-fourth V_{CTRL} plus an offset for $0V \leq V_{CTRL} \leq 1V$. For $V_{CTRL} > 1.2V$ the $V_{ISP-ISN}$ current regulation point is constant at the full-scale value of 250mV. For $1V \leq V_{CTRL} \leq 1.2V$, the dependence of $V_{ISP-ISN}$ upon CTRL voltage transitions from a linear function to a constant value, reaching 98% of full-scale value by $V_{CTRL} = 1.1V$. Do not leave this pin open.

Exposed Pad and GND: Ground Connection. Solder pin and exposed pad to ground plane.

PIN FUNCTIONS

SSFM: Used for spread spectrum frequency modulation. If SSFM is enabled, a triangle ramp is generated at the SSFM pin. During each cycle of this SSFM ramp, the internal switching frequency is modulated between F_{SWITCH} and F_{SWITCH} – 30%. The SSFM ramp frequency is set by 12µA/(2 x 1V x C_{SSFM}). If used, tie C_{SSFM} from SSFM to GND to set the ramp frequency. If not used, tie this pin to GND. Do not float this pin.

PWMTG: PWM Top-Gate Driver Output. An inverted PWM signal drives the gate of a series PMOS device between V_{ISP} and (V_{ISP} – 7V) if V_{ISP} > 7V. An internal 7V clamp protects the PMOS gate by limiting V_{GS}. Leave PWMTG disconnected if not used.

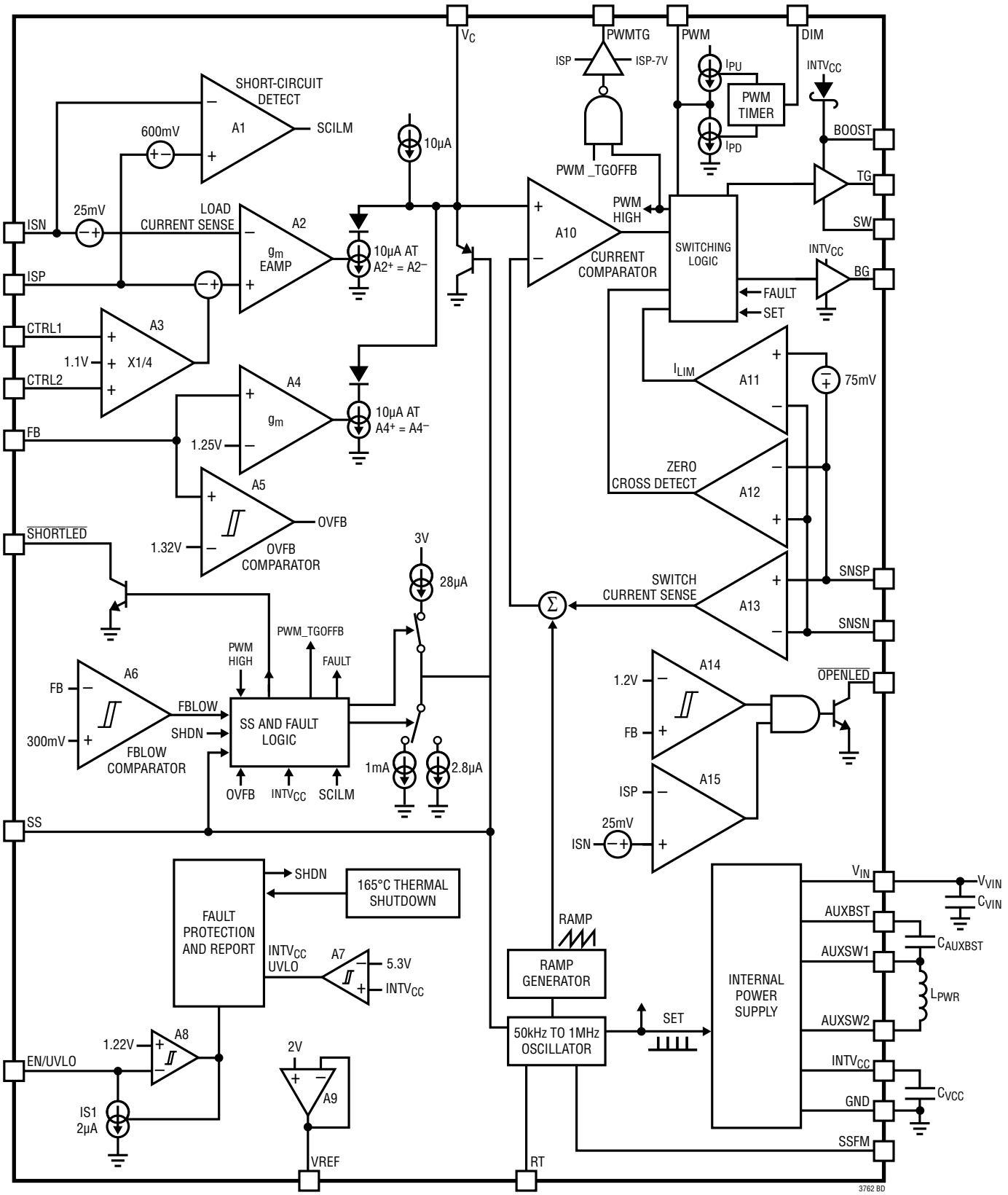
$\overline{\text{SHORTLED}}$: An open-collector pull-down on $\overline{\text{SHORTLED}}$ asserts when any of the following conditions happen:

1. FB < 0.3V after SS pin reaches 1.7V.
2. LED overcurrent ($V_{ISP-ISN}$ > 600mV).

This pin requires an external pull-up resistor. $\overline{\text{SHORTLED}}$ status is only updated during PWM high state and latched during PWM low state. After an LED overcurrent event, $\overline{\text{SHORTLED}}$ remains asserted until the SS pin is discharged below 0.2V.

DIM: Analog voltage control of PWM duty cycle from 0.4% to 97%(typ) when a capacitor is connected between PWM and ground. When DIM is pulled above 3V (typical), the PWM duty cycle timer is disabled and the PWM pin is pulled high with a 5µA current source. The duty cycle set by V_{DIM} follows a curve shown in Figure 9. A lowpass RC filter on DIM (10kΩ, 1µF) is recommended if driving DIM externally to control PWM duty cycle. Do not leave the DIM pin open. If not used, or if driving PWM externally connect to $INTV_{CC}$.

BLOCK DIAGRAM



OPERATION

The LT3762 is a constant-frequency, current mode controller with a low side NMOS gate driver and a high side NMOS synchronous gate driver. The operation of the LT3762 is best understood by referring to the Block Diagram. In this general description, the LT3762 is operating as a synchronous boost controller where the switch current is sensed at V_{IN} (sensing at V_{IN} enables TG driver function for synchronous operation). When power is first applied to the IC and the PWM pin is low, the BG pin is driven to GND, the TG pin is driven to SW, and the PWMTG pin is pulled high to ISP to turn off the PMOS disconnect switch which disconnects the load from the output of the switching regulator. The V_C pin becomes high impedance to store the previous switching state on the external compensation capacitor, and the ISP and ISN pin bias currents are reduced to leakage levels. When the PWM pin transitions high (either by setting externally or the PWM timer setting internally), the PWMTG pin transitions low after a short delay – connecting the load to the output. At the same time, the internal oscillator wakes up and generates a pulse to set a latch, turning on the external low side N-channel MOSFET switch (BG goes high). A voltage input proportional to the switch current, sensed by an external current sense resistor between the SNSP and SNSN pins, is added to a stabilizing slope compensation ramp and the resulting switch current sense signal is fed into the negative terminal of the current comparator. The current in the external inductor increases steadily during the time the switch is on. When the switch current sense voltage exceeds the output of the error amplifier, V_C, the latch in logic is reset and the low side switch is turned off. If configured as a synchronous boost controller, once BG goes low, the zero cross detect comparator determines if the inductor current is high enough to allow the synchronous NMOS switch to turn on – preventing the inductor current from crossing zero and discharging output capacitor. If the zero cross comparator output is low, TG goes high (in reference to SW) and turns on the top switch. During this phase, the inductor current decreases. TG goes low when either the oscillator terminates the switch cycle or the inductor current reaches near zero. If configured as a nonsynchronous boost controller, that is SNSN connected to GND and the sense resistor placed in the source of the BG switch, then TG will not switch high during this phase and a diode placed between SW and the output will conduct the inductor current until the end of the switch cycle. At the completion of each oscillator cycle, internal signals such as slope compensation return to their starting points and a new cycle begins with the set pulse from the oscillator. Through this repetitive action, the current mode control algorithm establishes a switch duty cycle to regulate the load current or voltage at the load. The V_C signal is integrated over many switching cycles and is an amplified version of the difference between the LED current sense voltage, measured between ISP and ISN, and the target difference voltage set by the CTRL pins. In this manner, the error amplifier sets the correct peak switch current level to keep the LED current in regulation. If the error amplifier output increases, more current is demanded in the switch; if it decreases, less current is demanded. The switch current is monitored during the on phase and the voltage between the SNSP and SNSN pins is not allowed to exceed the current limit threshold of 75mV (typical). If this current limit is reached, the latch is reset regardless of the output state of the current comparator and the TG switch will turn on until the end of the start of a new switching cycle or the inductor current reaches near zero. Under fault conditions, i.e. FB overvoltage (FB > 1.3V) , output short (FB < 0.3V after start-up), LED overcurrent, or $INTV_{CC}$ undervoltage ($INTV_{CC}$ < 5.3V), the BG and TG drivers turn off immediately.

In voltage feedback mode, the operation is similar to that described above, except the voltage at the V_C pin is set by

OPERATION

the amplified difference of the internal reference of 1.25V and the FB pin. If FB is lower than the reference voltage, the switch current increases; if FB is higher than the reference voltage, the switch demand current decreases. The LED current sense feedback interacts with the voltage feedback so that FB does not exceed the internal reference and the voltage between ISP and ISN does not exceed the threshold set by either of the CTRL pins. For accurate current or voltage regulation, it is necessary to be sure that under normal operating conditions, the appropriate loop is dominant. To deactivate the voltage loop entirely, FB can be set between 0.35V and 1.1V through a resistor network to V_{REF} pin. To deactivate the LED current loop entirely, the ISP and ISN pins should be tied together and CTRL1 and CTRL2 tied to V_{REF}.

Two LED specific functions featured on the LT3762 are controlled by the voltage feedback FB pin. First, when the FB pin exceeds a voltage 50mV (–4%) lower than the FB regulation voltage and $V_{(ISP-ISN)}$ is less than 25mV (typical), the pull-down driver on the $\overline{OPENLED}$ pin is activated. This function provides a status indicator that the load may be disconnected and the constant-voltage feedback loop is taking control of the switching regulator. When the FB pin drops below 0.3V after start-up, the $\overline{SHORTLED}$ pin is asserted by the FBLOW Comparator. During start-up, the FBLOW comparator output is blocked from when the EN/UVLO pin goes high to when the SS pin reaches 1.7V.

The LT3762 features a PMOS disconnect switch driver that serves two purposes — PWM control of LED load current and fault protection of LED load. When no fault condition exists, the PWMTG state depends on the state of the PWM pin. When PWM pin is high, the PWMTG is pulled below ISP to turn on the PMOS switch. When PWM pin is low, PWMTG is pulled to ISP to turn off the PMOS. Once a fault condition is detected, the PWMTG pin is pulled high to turn off the PMOS switch — independent of the PWM pin state. This action isolates the LED array from the power path, preventing excessive current from damaging the LEDs.

PWM control of LED load current is achieved by externally setting the PWM pin or by allowing the internal PWM Timer to set the PWM pin. If externally controlling the PWM pin, the DIM pin is set above 3V (e.g. tie to $INTV_{CC}$). If the internal PWM Timer is used, PWM pin is connected to an external capacitor (size of cap sets PWM frequency) and the voltage at DIM determines the duty cycle at PWMTG. The duty cycle range is 0.32% to 97% (typical). Setting DIM above 3V (typ) disables the timer and sets PWM to 100% duty cycle. The relationship between V_{DIM} and the generated duty cycle allows a linear change in V_{DIM} to be perceived by the human eye as a linear change in LED intensity.

The $INTV_{CC}$ rail is generated by an internal buck-boost regulator and requires external capacitors at $INTV_{CC}$ and AUXBST pins and a small external inductor at AUXSW1, AUXSW2 pins. This rail provides the gate drive potential for BG and TG and also provides bias to internal circuitry. $INTV_{CC}$ is also available to support other external circuitry using care to stay within its max supply current range.

APPLICATIONS INFORMATION

Programming the Turn-On and Turn-Off Thresholds with the EN/UVLO Pin

The power supply undervoltage lockout (UVLO) value can be accurately set by the resistor divider to the EN/UVLO pin. A small 2µA pull-down current is active when EN/UVLO is below the threshold. The purpose of this current is to allow the user to program the rising hysteresis. The following equations should be used to determine the values of the resistors:

$$V_{IN(FALLING)} = 1.22V \bullet \frac{R1+R2}{R2}$$

$$V_{IN(RISING)} = V_{IN(FALLING)} + 2\mu A \bullet R1$$

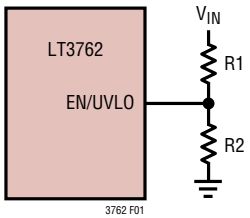


Figure 1.

Programming the LED Current

The LED current is programmed by placing an appropriate value current sense resistor, R_{LED}, in series with the LED string. The voltage drop across R_{LED} is (Kelvin) sensed by the ISP and ISN pins. A half watt resistor is usually a good choice. To give the best accuracy, sensing of the current should be done at the top of the LED string. For best fault protection and use of the PWM feature provided by the high side PMOS disconnect switch, sensing of the current should be done at the top of the LED string. If this option is not available, then the current may be sensed at the bottom of the string. However, if the string terminates to a voltage less than a PMOS threshold above GND, low side sensing will sacrifice the PMOS disconnect feature.

Both the CTRL pins should be tied to a voltage higher than 1.2V to get the full-scale 250mV (typical) threshold across the sense resistor. Either CTRL pin can be used to dim the LED current to zero current, although relative accuracy decreases with the decreasing voltage sense threshold. The lower of the two CTRL pins sets the LED current. When a CTRL pin voltage is less than 1V, the LED current is:

$$I_{LED} = \frac{V_{CTRL} - 100mV}{R_{LED} \bullet 4}$$

When the lower CTRL pin voltage is between 1V and 1.2V, the LED current varies with CTRL, but departs from the previous equation by an increasing amount as the CTRL voltage increases. Ultimately, the LED current no longer varies for CTRL ≥ 1.2V. At CTRL = 1.1V, the value of I_{LED} is ~98% of the equation's estimate. Some values are listed in Table 1.

Table 1. (ISP-ISN) Threshold vs CTRL

V_{CTRL} (V)	(ISP-ISN) THRESHOLD (mV)
1.0	225
1.05	236
1.1	244.5
1.15	248.5
1.2	250

When both CTRL pins are higher than 1.2V, the LED current is regulated to: $I_{LED} = 250mV/R_{LED}$

The CTRL pins should not be left floating (tie to V_{REF} if not used). Either CTRL pin can be used with a thermistor to provide overtemperature protection for the LED load, or with a resistor divider to V_{IN} to reduce the output power and switching current when V_{IN} is low. The presence of a time varying differential voltage signal (ripple) across ISP and ISN at the switching frequency is expected. The amplitude of this signal is increased by the high LED load current, low switching frequency and/or a smaller value output filter capacitor. For best accuracy, the amplitude of this ripple should be less than 25mV. If using a R_{LED} of 500mΩ or greater, a 10µF capacitor should be placed across R_{LED} to dampen the effect of transients across the error amp.

APPLICATIONS INFORMATION

Programming Output Voltage (Constant Voltage Regulation) and Output Voltage Open LED and Shorted LED Thresholds

The LT3762 has a voltage feedback pin FB that can be used to program a constant voltage output. In addition, FB programming determines the output voltage that will cause $\overline{\text{OPENLED}}$ and $\overline{\text{SHORTLED}}$ to assert. For a boost LED driver, the output voltage can be programmed by selecting the values of R3 and R4 (see Figure 2) according to the following equation:

$$V_{OUT} = 1.25V \bullet \frac{R3 + R4}{R4}$$

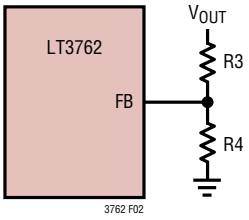


Figure 2.

For an LED driver of buck mode or buck-boost mode configuration, the FB voltage is typically level shifted to a signal with respect to GND as illustrated in Figure 3. In buck mode, R1 provides SNSP and SNSN with enough current to maintain regulation during an OPENLED event. Note that R1 will affect PWM performance by loading C_{OUT} when PWM is low. In buck-boost mode, when SNSP is tied to V_{IN} or another low impedance node, R1 can be omitted. The output can be expressed as:

Buck mode:

$$V_{OUT} = \left[1.25V \bullet \frac{R3}{R4} + V_{BE(Q1)}\right] \bullet 2$$

$$R1 = R2 = V_{OUT}/600\mu A$$

Buck-boost mode

$$V_{OUT} = 1.25V \bullet \frac{R3}{R4} + V_{BE(Q1)}$$

$$R2 = 100k, R1 = OPEN$$

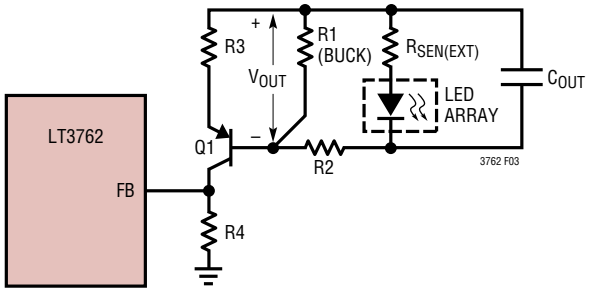


Figure 3. Feedback Resistor Connection for Buck Mode or Buck-Boost Mode LED Driver

If the open LED clamp voltage is programmed correctly using the resistor divider, then the FB pin should not exceed 1.2V when LEDs are connected.

To detect both open-circuit and short-circuit conditions at the output, the LT3762 monitors both output voltage and current. When FB exceeds V_{FB} – 50mV, $\overline{\text{OPENLED}}$ is asserted, if $V_{(ISP-ISN)}$ is less than 25mV. $\overline{\text{OPENLED}}$ is de-asserted when $V_{(ISP-ISN)}$ is higher than 50mV or FB drops below the OPENLED threshold.

The $\overline{\text{SHORTLED}}$ pin is asserted if $V_{(ISP-ISN)}$ > 600mV or the FB pin falls below 300mV after initial start-up and SS reaches 1.7V. The ratio between the FB $\overline{\text{OPENLED}}$ threshold of 1.2V and the $\overline{\text{SHORTLED}}$ threshold of 0.3V can limit the range of V_{OUT}. The range of V_{OUT} using the maximum $\overline{\text{SHORTLED}}$ threshold of 0.35V is 3.5:1. The range of V_{OUT} can be made wider using the circuits shown in Figures 4 and 5. For a V_{OUT} range that is greater than 8:1, consult factory applications.

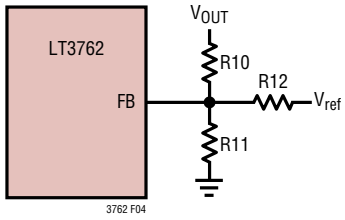


Figure 4. Feedback Resistor Connection for Wide Range Output in Boost and SEPIC Applications

APPLICATIONS INFORMATION

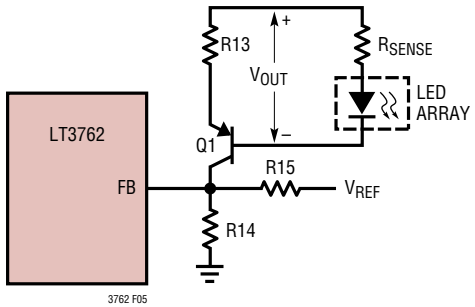


Figure 5. Feedback Resistor Connection for Wide Range Output in Buck Mode and Buck-Boost Mode Applications

The equations to widen the range of V_{OUT} are derived using a $\overline{SHORTLED}$ threshold of 0.35V, and $\overline{OPENLED}$ threshold of 1.2V and a reference voltage V_{REF} of 2V. The resistor values for R11 and R12 in Figure 4 can be calculated as shown below. See the example that follows for a suggested R10 value.

$$R11 = \frac{R10 \bullet 1.64V}{1.61 \bullet V^{H}_{OUT} - 0.79 \bullet V^{L}_{OUT} - 1.64V}$$

$$R12 = \frac{R10 \bullet 1.64V}{0.41 \bullet V^{H}_{OUT} - 1.41 \bullet V^{L}_{OUT}}$$

Example: Calculate the resistor values required to increase the V_{OUT} range of a boost LED driver to 5:1 and have $\overline{OPENLED}$ occur when V_{OUT} is 60V.

Step 1: Choose R10 = 1MΩ

Step 2: V^{L}_{OUT} = 60V/5 = 12V

Step 3:

$$R11 = \frac{1000k\Omega \bullet 1.64V}{1.61 \bullet 60V - 0.79 \bullet 12V - 1.64V} = 19.18k\Omega$$

Use R11 = 19.1kΩ

$$R12 = \frac{1000k\Omega \bullet 1.64V}{0.41 \bullet 60V - 1.41 \bullet 12V} = 213.54k\Omega$$

Use R12 = 215kΩ

The resistor values for R14 and R15 in Figure 5 can be calculated as shown below. See the example that follows for a suggested R13 value.

$$R14 = \frac{R13 \bullet 1.64V}{1.61 \bullet V^{H}_{OUT} - 0.79 \bullet V^{L}_{OUT} \bullet V_{BE}}$$

$$R15 = \frac{R13 \bullet 1.64V}{0.41 \bullet V^{H}_{OUT} - 1.41 \bullet V^{L}_{OUT} + 0.82 \bullet V_{BE}}$$

Example: Calculate the resistor values required to increase the V_{OUT} range of a buck-boost mode LED driver to 7.5:1 and have $\overline{OPENLED}$ occur when V_{OUT} is 43.5V. Use $V_{BE(Q1)}$ = 0.7V:

Step 1: Choose R13 = 357kΩ

Step 2: V^{L}_{OUT} = 43.5V/7.5 = 5.8V

Step 3:

$$R14 = \frac{357k\Omega \bullet 1.64V}{1.61 \bullet 43.5V - 0.79 \bullet 5.8V - 0.82 \bullet 0.7V} = 9.02k\Omega$$

Use R14 = 9.09kΩ

$$R15 = \frac{357k\Omega \bullet 1.64V}{0.41 \bullet 43.5V - 1.41 \bullet 5.8V + 0.82 \bullet 0.7V} = 56.5k\Omega$$

Use R15 = 56.2kΩ

LED Overcurrent Protection Feature

The ISP and ISN pins have a short-circuit protection feature independent of the LED current sense feature. This feature prevents the development of excessive switching currents and protects the power components. The short-circuit protection threshold (600mV, typical) is designed to be more than 140% higher than the default LED current sense threshold. Once the LED overcurrent is detected, the BG pin is driven to GND and the TG pin is pulled to SW to stop switching, PWMTG is pulled high to disconnect the LED array from the power path, SHORTLED is latched low, and fault protection is initiated via the SS pin. A typical LED short-circuit protection scheme for a boost or buck-boost mode converter is shown in Figure 6. The Schottky or ultrafast diode D2 should be put close to the drain of M2 on the board. It protects the LED^{+} node from

APPLICATIONS INFORMATION

swinging well below ground when being shorted to GND through a long cable. Usually, the internal protection loop takes about 600ns to respond. When a faster short-circuit response is required, a PNP helper can be added as shown in Figure 6. Note that the impedance of the short-circuit cable affects the peak current. Schottky or ultrafast recovery diodes D1 and D3 are recommended to protect against a short circuit for the buck mode circuit shown in Figure 7.

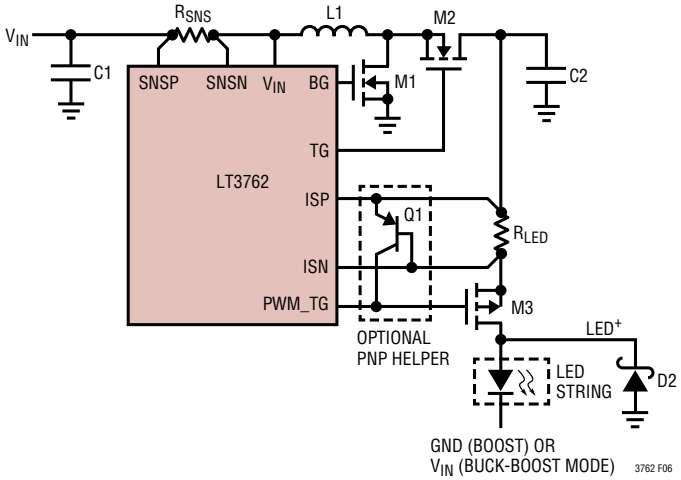


Figure 6. Simplified LED Short-Circuit Protection Schematic for Boost or Buck-Boost Mode Converter

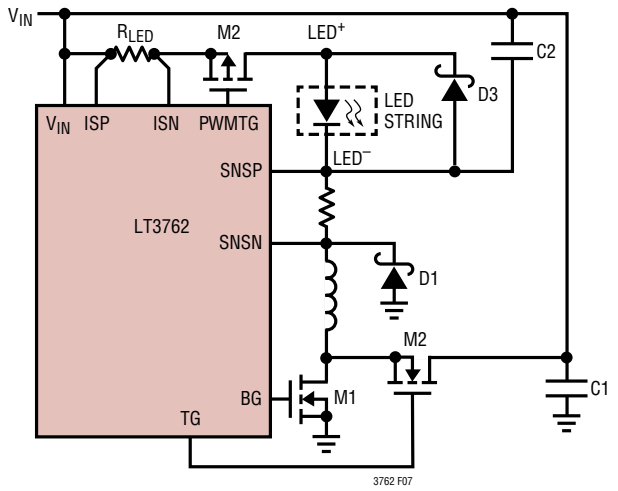


Figure 7. Simplified LED Short-Circuit Protection Schematic for Buck Mode Converter

PWM Dimming Control

There are two methods to control the current source for dimming using the LT3762. One method uses the CTRL pins to adjust the current regulated in the LEDs. A second method uses the PWM pin to modulate the current source between zero and full current to achieve a precisely programmed average current, without the possibility of color shift that occurs at low current in LEDs. To make PWM dimming more accurate, the switch demand current is stored on the V_C node during the quiescent phase when PWM is low. This feature minimizes recovery time when the PWM signal goes high. To further improve recovery time and allow for low PWM duty cycles, the PWMTG disconnect PMOS switch is used in the LED current path and prevents the output capacitor from discharging during the PWM signal low phase. The minimum PWM on or off time depends on the choice of operating frequency set by the RT input. For best current accuracy, the minimum PWM high time should be at least three switching cycles (3µs for f_{SW} = 1MHz)

A low duty cycle PWM signal can cause excessive start-up times if it were allowed to interrupt the soft-start sequence at start-up. Therefore, once start-up is initiated by PWM high, the LT3762 will ignore a PWM logic low and continue to soft-start with PWMTG enabled until either the voltage at SS reaches the 0.8V level or the output current reaches one-tenth of the full-scale current. At this point, the device will begin following the dimming control as designated by PWM. If at any time an output overcurrent is detected, BG, TG, and PWMTG will be disabled even as SS continues to charge.

PWM Dimming Signal Generator

The LT3762 features a PWM dimming signal generator with programmable duty cycle at PWMTG pin, controlling average current delivered to the LED load. The frequency of the square wave signal at PWMTG is set by a capacitor C_{PWM} from the PWM pin to GND according to the equation:

$$f_{PWM} = \frac{66kHz \bullet nF}{C_{PWM}}$$

APPLICATIONS INFORMATION

The duty cycle at PWMTG is set by a voltage applied at DIM pin. This duty cycle varies between 0.4% and 97% with an applied DIM voltage between 0V and 3V. Above 3V (typical), the internal PWM signal generator is disabled and the duty cycle goes to 100% unless the PWM pin is externally driven. To filter out any noise and smooth transitions between output levels, the DIM pin should be driven through a lowpass RC filter (10k resistor and 1µF capacitor is recommended) when used to control PWM duty cycle. Internally generated pull-up and pull-down currents on the PWM pin are used to charge and discharge its capacitor between high and low thresholds to generate the duty cycle signal. These current signals on the PWM pin are small enough that they can be overdriven by an external signal from a microcontroller. To synchronize the PWM generator with soft-start during power-on reset, a PNP can be connected as shown in Figure 8 to quickly discharge the PWM generator capacitor during a reset event.

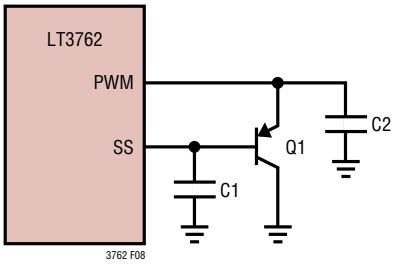


Figure 8. Syncing PWM During Reset

If controlling PWM pin externally, it is recommended to raise DIM above 3V (e.g. tie to $INTV_{CC}$) to disable PWM generator and conserve quiescent current.

The relationship between V_{DIM} and duty cycle at PWMTG is illustrated in Figure 9 and given by the following equations. This relationship allows a linear change in V_{DIM} to be perceived by the human eye as a linear change in LED intensity.

$$\text{Duty Cycle, } DC = \frac{1}{1+e^{6.812-V(DIM)\bullet 3.25}} \bullet \frac{1}{1V}$$

$$V_{DIM} = \frac{\left(6.812 - \ln\left(\frac{1-DC}{DC}\right)\right)\bullet 1V}{3.25}$$

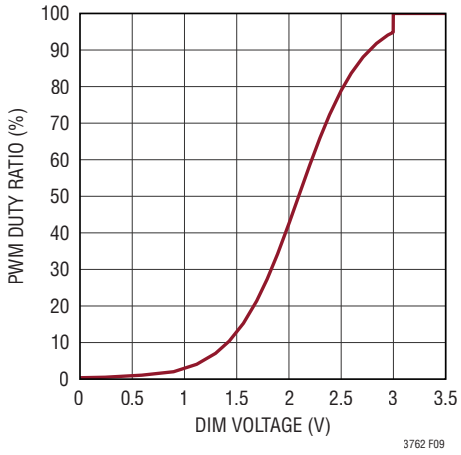


Figure 9. V_{DIM} vs Duty Cycle

Programming the Switching Frequency

The RT frequency adjust pin allows the user to program the switching frequency (f_{SW}) from 100kHz to 1MHz to optimize efficiency/performance or external component size. Higher frequency operation yields smaller component size but increases switching losses and gate driving current, and may not allow sufficiently high or low duty cycle operation. Lower frequency operation gives better performance at the cost of larger external component size. For an appropriate RT resistor value, see Table 2. An external resistor from the RT pin to GND is required – do not leave this pin open.

Table 2. Typical Switching Frequency vs R_T Value (1% Resistor)

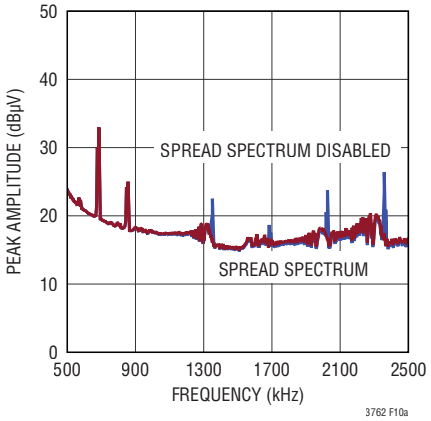
f_{OSC}(kHz)	R_T(kΩ)
1000	6.65
900	7.50
800	8.87
700	10.2
600	12.4
500	15.4
400	19.6
300	26.1
200	39.2
100	82.5

Spread Spectrum Frequency Modulation

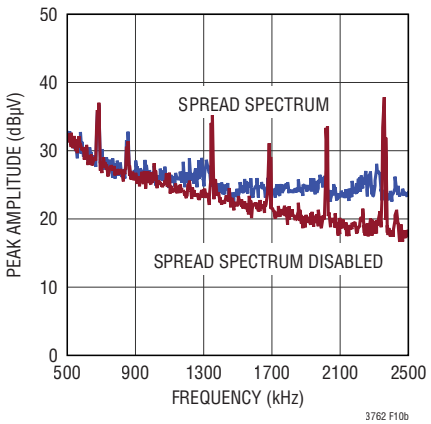
Switching regulators can be particularly troublesome for applications where electromagnetic interference (EMI) is a concern. To improve the EMI performance, the LT3762

APPLICATIONS INFORMATION

includes a spread spectrum frequency feature. If there is a capacitor (C_{SSFM}) at the SSFM pin, a triangle wave sweeping between 1V and 2V is generated. This signal is then fed into the internal oscillator to modulate the switching frequency between 70% of the base frequency and the base frequency, which is set by the RT resistor. The modulation frequency is set by 12µA / (2 • 1V • C_{SSFM}). Figure 10 shows the noise spectrum comparison between a conventional boost switching converter (with the LT3762 SSFM pin tied to GND) and a spread spectrum modulation enabled boost switching converter with 6.8nF at the SSFM pin. The results of EMI measurements are sensitive to the SSFM frequency selected with the capacitor. 1kHz is a good starting point to optimize peak measurements, but some fine tuning of this selection may be necessary to get the best overall EMI results in a particular system. Consult factory application for more detailed information about EMI reduction.



(10a) Conducted Average EMI Comparison



(10b) Conducted Peak EMI Comparison

Figure 10.

Duty Cycle Considerations

Switching duty cycle is a key variable in defining converter operation, therefore, its limits must be considered when programming the switching frequency for a particular application. The fixed BG minimum on-time and minimum off-time (see Figure 11) and the switching frequency define the minimum and maximum duty cycle of the switch, respectively. The following equations express the minimum/maximum duty cycle:

Min Duty Cycle = min on-time • switching frequency

Max Duty Cycle = 1 – min off-time • switching frequency

When calculating the operating limits, the typical values for on/off-time in the data sheet should be increased by at least 100ns to allow margin for PWM comparator and logic delays, TG & BG rise/fall times and SW node rise/fall times.

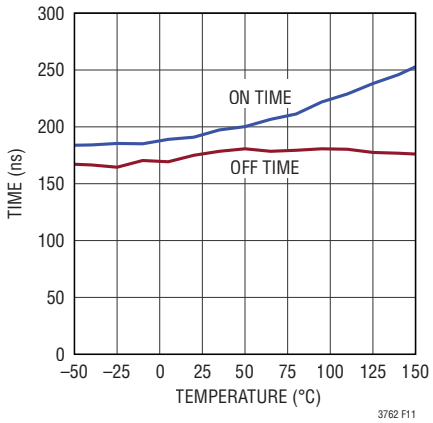


Figure 11. Typical Minimum On-Time and Off-Time vs Temperature

Synchronous vs Non-Synchronous Operation

The TG synchronous driver is designed to improve the efficiency of the power converter by replacing the conventional power diode with a power NMOS device. The synchronous driver feature is enabled when the following criteria are met:

1. The switch current sense resistor R_{SENSE} is placed in series with the inductor so that SNSP and SNSN can monitor the power switch currents in both phases of the switching cycle.

APPLICATIONS INFORMATION

2. The common mode voltage of SNSP and SNSN remains greater than 2V during both phases of the switching cycle.
3. A capacitor, C_{BOOST}, is tied between BOOST and SW pins, where SW pin switches to GND during the BG enabled phase allowing C_{BOOST} to charge via an internal diode to $INTV_{CC}$, and the SW pin is tied to the source of the TG driver NMOS device.

In addition to boost power converters, topologies such as buck mode and buck-boost mode (see applications diagrams) are capable of meeting these criteria and can take advantage of the synchronous feature.

The LT3762 can also operate as a non-synchronous power converter for applications such as SEPIC where R_{SENSE} cannot be used to sense the switch currents in both phases of the switching cycle. Nonsynchronous operation may also be chosen for high-voltage applications (e.g. ISP, ISN sensing LED current at string voltages up to 80V) where the efficiency savings of the synchronous feature are not significant.

TG Synchronous Driver

Once the synchronous top gate (TG) driver is enabled, it remains on until either the switching cycle is terminated by the oscillator or the inductor current reaches near zero to prevent the inductor current from reversing and discharging the output capacitor. To improve high duty cycle performance, a timer (TG disable timer) disables the TG driver at high BG duty cycles when the BG off-time is below 310ns (typical). During the non-overlap time between the BG driver and synchronous TG driver, the inductor current flows in the body diode of the synchronous NMOS device.

Integrated $INTV_{CC}$ Power Supply

The LT3762 includes an internal switch mode DC/DC converter to generate a regulated 7.5V $INTV_{CC}$ power supply to power the BG and TG NMOS gate drivers. (I_{DRIVE}). This $INTV_{CC}$ power supply has two major advantages over the traditional internal LDO regulators. It is able to generate 7.5V $INTV_{CC}$ voltage from a V_{IN} voltage as low as 2.5V, allowing the LT3762 to drive high threshold MOSFETs in low V_{IN} applications. It is also able to deliver large current from a V_{IN} voltage as high as 43V without overheating the package, due to its high efficiency (over 70% at full load). This integrated DC/DC converter requires three external components (C_{VCC}, C_{AUXBST} and L_{PWR}) for operation as shown in Figure 1. Select these three components based on the following guidelines:

- C_{VCC} is a 10µF/10V ceramic capacitor used to bypass $INTV_{CC}$ to GND as close to the pin as possible.
- C_{AUXBST} is a 0.1µF/10V ceramic capacitor connected between the AUXBST pin and the AUXSW1 pin.
- Select a 47µH inductor with the saturation current rating of 0.6A or greater and RMS current rating of 0.4A or greater for L_{PWR}.

The $INTV_{CC}$ power supply can also be used to drive external circuits (I_{EXT}). Any external circuit should be connected as shown in Figure 12. This will disconnect the external $INTV_{CC}$ load during an overtemperature event, preventing the generation of additional heat while the LT3762 returns to a safe operating temperature.

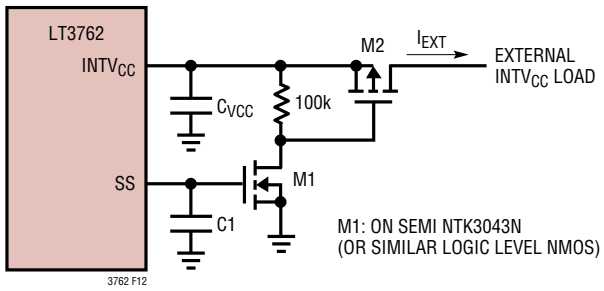


Figure 12. Powering External Circuits with $INTV_{CC}$

The $INTV_{CC}$ power supply has an output current limit function to protect itself from excessive electrical and thermal stress. Figure 13 shows the $INTV_{CC}$ output limit I_{INTVCC_LMT} vs V_{IN} and switching frequency. Make sure the sum of the I_{DRIVE} and I_{EXT} is always lower than the I_{INTVCC_LMT} across the whole V_{IN} range of the application:

$$I_{DRIVE} + I_{EXT} < I_{INTVCC\_LMT}$$

where:

$$I_{DRIVE} = (Q_{TG} + Q_{BG}) \bullet f_{SW}$$

APPLICATIONS INFORMATION

Q_{TG} and Q_{BG} is the total gate charge of the NMOS devices controlled by TG and BG at 0V to 7.5V.

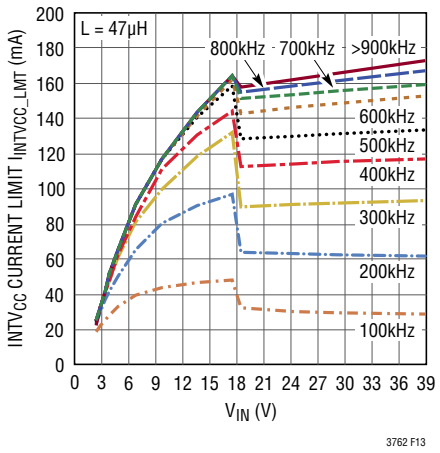


Figure 13. $INTV_{CC}$ Maximum Current vs V_{IN}, f_{SW}

Input Capacitor Selection

The input capacitor supplies the transient input current for the power inductor of the converter and must be placed and sized according to the transient current requirements. The switching frequency, output current and tolerable input voltage ripple are key inputs to estimating the capacitor value. An X7R type ceramic capacitor is usually the best choice since it has the least variation with temperature and DC bias. Typically, boost and SEPIC converters require a lower value capacitor than a buck mode converter. Assuming that a 100mV input voltage ripple is acceptable, the required capacitor value for a boost converter can be estimated as follows ($T_{SW} = 1/f_{OSC}$):

$$C_{IN}(\mu F) = I_{LED}(A) \bullet \frac{V_{LED}}{V_{IN}} \bullet T_{SW}(\mu s) \bullet \frac{1\mu F}{A \bullet \mu s \bullet 2.8}$$

Therefore, a 2.2µF capacitor is an appropriate selection for a 400kHz boost regulator with 12V input, 48V output and 500mA load.

With the same V_{IN} voltage ripple of less than 100mV, the input capacitor for a buck mode converter can be estimated as follows:

$$C_{IN}(\mu F) = I_{LED}(A) \bullet \frac{V_{LED} \bullet (V_{IN} - V_{LED})}{V_{IN}^2} \bullet T_{SW}(\mu s) \bullet \frac{10\mu F}{A \bullet \mu s}$$

A 10µF input capacitor is an appropriate selection for a 400kHz buck mode converter with 24V input, 12V output and 1A load.

In the buck mode configuration, the input capacitor has large pulsed currents due to the current returned through the Schottky diode when the switch is off. It is important to place the capacitor as close as possible to the Schottky diode and the GND return of the switch (i.e., the sense resistor). It is also important to consider the ripple current rating of the capacitor. For best reliability, this capacitor should have low ESR and ESL and have an adequate ripple current rating. The RMS input current for a buck mode LED driver is:

$$I_{IN(RMS)} = I_{LED} \bullet \sqrt{(1-D) \bullet D}$$

$$D = \frac{V_{LED}}{V_{IN}}$$

where D is the switch duty cycle.

Table 3. Recommended Ceramic Capacitor Manufacturers

MANUFACTURER	WEB
TDK	www.tdk.com
Kemet	www.kemet.com
Murata	www.murata.com
Taiyo Yuden	www.t-yuden.com
AVX	www.avx.com

Output Capacitor Selection

The selection of the output capacitor depends on the load and converter configuration, i.e., step-up or step-down and the operating frequency. For LED applications, the equivalent resistance of the LED is typically low and the output filter capacitor should be sized to attenuate the current ripple. Use of an X7R type ceramic capacitor is recommended.

To achieve the same LED ripple current, the required filter capacitor is larger in the boost, SEPIC, and buck-boost mode applications than that in the buck mode applications. Lower operating frequencies will require proportionately

APPLICATIONS INFORMATION

higher capacitor values. The component values shown in the data sheet applications are appropriate to drive the specified LED string. The product of the output capacitor and LED string impedance decides the second dominant pole in the LED current regulation loop. It is prudent to validate the power supply with the actual load (or loads).

Power MOSFET Selection

For applications operating at high input or output voltages, the power N-channel MOSFET switches are typically chosen for drain voltage V_{DS} rating and low gate charge Q_G. Consideration of switch on-resistance, $R_{DS(ON)}$, is usually secondary because switching losses dominate power loss. For driving LEDs, be careful to choose a switch with a V_{DS} rating that exceeds the threshold set by the FB pin in case of an open load fault. Several MOSFET vendors are listed in Table 4. The MOSFETs used in the application circuits in this data sheet have been found to work well with the LT3762. Consult factory applications for other recommended MOSFETs.

Table 4. MOSFET Manufacturers

VENDOR	WEB
Vishay Siliconix	www.vishay.com
Fairchild	www.fairchildsemi.com
International Rectifier	www.irf.com
Infineon	www.infineon.com
Nexperia	www.nexperia.com

High Side PMOS Disconnect Switch Selection

A high side PMOS disconnect switch with a minimum V_{TH} of –1V to –2V is recommended in most LT3762 applications to optimize or maximize the PWM dimming ratio and protect the LED string from excessive heating during fault conditions as well. The PMOS disconnect switch is typically selected for drain-source voltage V_{DS}, and continuous drain current I_D. For proper operations, V_{DS} rating must exceed the open LED regulation voltage set by the FB pin, and I_D rating should be above I_{LED}.

Schottky Rectifier Selection (Non-Synchronous Application)

When the synchronous MOSFET is not used (MOSFET controlled by TG driver), the SW pin should be grounded, BOOST pin tied to $INTV_{CC}$ and TG pin floated. A power Schottky diode is selected to conduct current during the interval when the BG controlled MOSFET is turned off. Select a diode rated for the maximum SW voltage. It is important to choose a Schottky diode with sufficiently low leakage current when using the PWM feature for dimming, because leakage increases with temperature and occurs from the output during the PWM low interval. Table 5 has some recommended component vendors.

Table 5. Schottky Rectifier Manufacturers

VENDOR	WEB
On Semiconductor	www.onsemi.com
Diodes, Inc	www.diodes.com
Central Semiconductor	www.centralsemi.com
Rohm Semiconductor	www.rohm.com

Sense Resistor Selection

The resistor, R_{SENSE}, that senses the BG controlled MOSFET current during the on cycle, should be selected to provide adequate switch current to drive the application without exceeding the 80mV (typical) current limit threshold on the SNSP-SNSN pins. For buck mode applications, select a resistor that gives a switch current at least 30% greater than the required LED current. For buck mode, select a resistor according to:

$$R_{SENSE(BUCK)} \leq \frac{0.05V}{I_{LED}}$$

For buck-boost mode, select a resistor according to:

$$R_{SENSE(BUCK–BOOST)} \leq \frac{V_{IN} \bullet 0.05V}{(V_{IN} + V_{LED}) \bullet I_{LED}}$$

APPLICATIONS INFORMATION

For boost, select a resistor according to:

$$R_{SENSE(BOOST)} \leq \frac{V_{IN} \bullet 0.05V}{V_{LED} \bullet I_{LED}}$$

The placement of R_{SENSE} should minimize the current path to the MOSFET controlled by the BG gate driver. The SNSP and SNSN inputs to the LT3762 should be a Kelvin connection to positive and negative terminals of R_{SENSE} respectively.

50mV is used in the equations above to give some margin below the 80mV (typical) sense current limit threshold.

Inductor Selection

The inductor used with the LT3762 should have a saturation current rating appropriate to the maximum switch current selected with the R_{SENSE} resistor. Choose an inductor value based on operating frequency and input and output voltage to provide a differential current mode signal on SNSP-SNSN of approximately 15mV magnitude. The following equations are useful to estimate the inductor value (TSW=1/fOSC):

$$L_{BUCK} = \frac{T_{SW} \bullet R_{SENSE} \bullet V_{LED}(V_{IN} - V_{LED})}{V_{IN} \bullet 0.015}$$

$$L_{BUCK-BOOST} = \frac{T_{SW} \bullet R_{SENSE} \bullet V_{LED} \bullet V_{IN}}{(V_{LED} + V_{IN}) \bullet 0.015}$$

$$L_{BOOST} = \frac{T_{SW} \bullet R_{SENSE} \bullet V_{IN}(V_{LED} - V_{IN})}{V_{LED} \bullet 0.015}$$

Table 6 provides some recommended inductor vendors.

Table 6. Inductor Manufacturers

VENDOR	WEB
Sumida	www.sumida.com
Wurth Elektronik	www.we-online.com
Coiltronics	www.cooperet.com
Vishay	www.vishay.com
Coilcraft	www.coilcraft.com

Loop Compensation

The LT3762 uses an internal transconductance error amplifier whose V_C output compensates the control loop. The external inductor, output capacitor and the compensation resistor and capacitor determine the loop stability. The inductor and output capacitor are chosen based on performance, size and cost. The compensation resistor and capacitor at V_C are selected to optimize control loop response and stability. For typical LED applications, a 10nF compensation capacitor at V_C is adequate, and a series resistor should always be used to increase the slew rate on the V_C pin to maintain tighter regulation of LED current during fast transients on the input supply to the converter.

Soft-Start Capacitor Selection

For many applications, it is important to minimize the inrush current at start-up. The built-in soft-start circuit significantly reduces the start-up current spike and output voltage overshoot. The soft-start interval is set by the soft-start capacitor selection according to the equation:

$$T_{SS} = C_{SS} \bullet \frac{2V}{28\mu A}$$

A typical value for the soft-start capacitor is 0.1µF. The soft-start pin reduces the oscillator frequency and the maximum current in the switch. Soft-start also operates as fault protection, which forces the converter to hiccup or latchoff mode. Detailed information is provided in the Fault Protection: Hiccup Mode and Latchoff Mode section.

Fault Protection: Hiccup Mode and Latchoff Mode

If an LED overcurrent condition, $INTV_{CC}$ undervoltage, output short (FB ≤ 0.3V), or thermal limit happens, the PWMTG pin is pulled high to disconnect the LED array from the power path, and the BG and TG pins are driven low. If the soft-start pin is charging and still below 1.7V, then it will continue to do so with a 28µA source. Once above 1.7V, the pull-up source is disabled and a 2.8µA pull-down

APPLICATIONS INFORMATION

is activated. While the SS pin is discharging, the BG and TG pin are forced low. When the SS pin is discharged below 0.2V, a new cycle is initiated. This is referred as hiccup mode operation. If the fault still exists when SS crosses below 0.2V, then a full SS charge/discharge cycle has to complete before switching is enable.

If a resistor is placed between the V_{REF} pin and SS pin to hold SS pin higher than 0.2V during a fault, then the LT3762 will enter latchoff mode with BG and TG pins low and PWMTG pin high. To exit latchoff mode, the EN/UVLO pin must be toggled low to high.

Board Layout

The high speed operation of the LT3762 demands careful attention to board layout and component placement. The exposed pad of the package is the GND terminal of the IC and is also important for thermal management of the IC. It is crucial to achieve a good electrical and thermal contact between the exposed pad and the ground plane of the board. To reduce electromagnetic interference (EMI), it is important to minimize the area of the high dV/dt switching nodes, especially at routes connected to the BOOST, SW, TG, AUXSW1 and AUXBST pins. Use a ground plane under the switching notes to eliminate interplane coupling to sensitive signals. The lengths of the high dI/dt traces should also be minimized:

1. from the BG switch to GND, and

2. from the TG switch to the output filter capacitor to GND.

The ground points of these two switching current traces should come to a common point and then connect to the ground plane under the LT3762. Likewise, the ground terminal of the bypass capacitor for the $INTV_{CC}$ regulator should be placed near the GND of the switching path. The ground for the compensation network and other DC control signals should be star connected to the underside of the IC. Do not extensively route high impedance signals such as FB, RT, PWM and V_C, as they may pick up switching noise. Since there is a small variable DC input bias current to the ISN and ISP inputs, resistance in series with these pins should be minimized to avoid creating an offset in the current sense threshold. Likewise, minimizing resistance in series with the SNSP and SNSN inputs will avoid changes to the switch current sense limit threshold. Figure 14 is a suggested two-sided layout for a boost converter. Note that a 4-layer layout is recommended for best performance. Please see the DC2342A demo circuit for a reference layout design.

APPLICATIONS INFORMATION

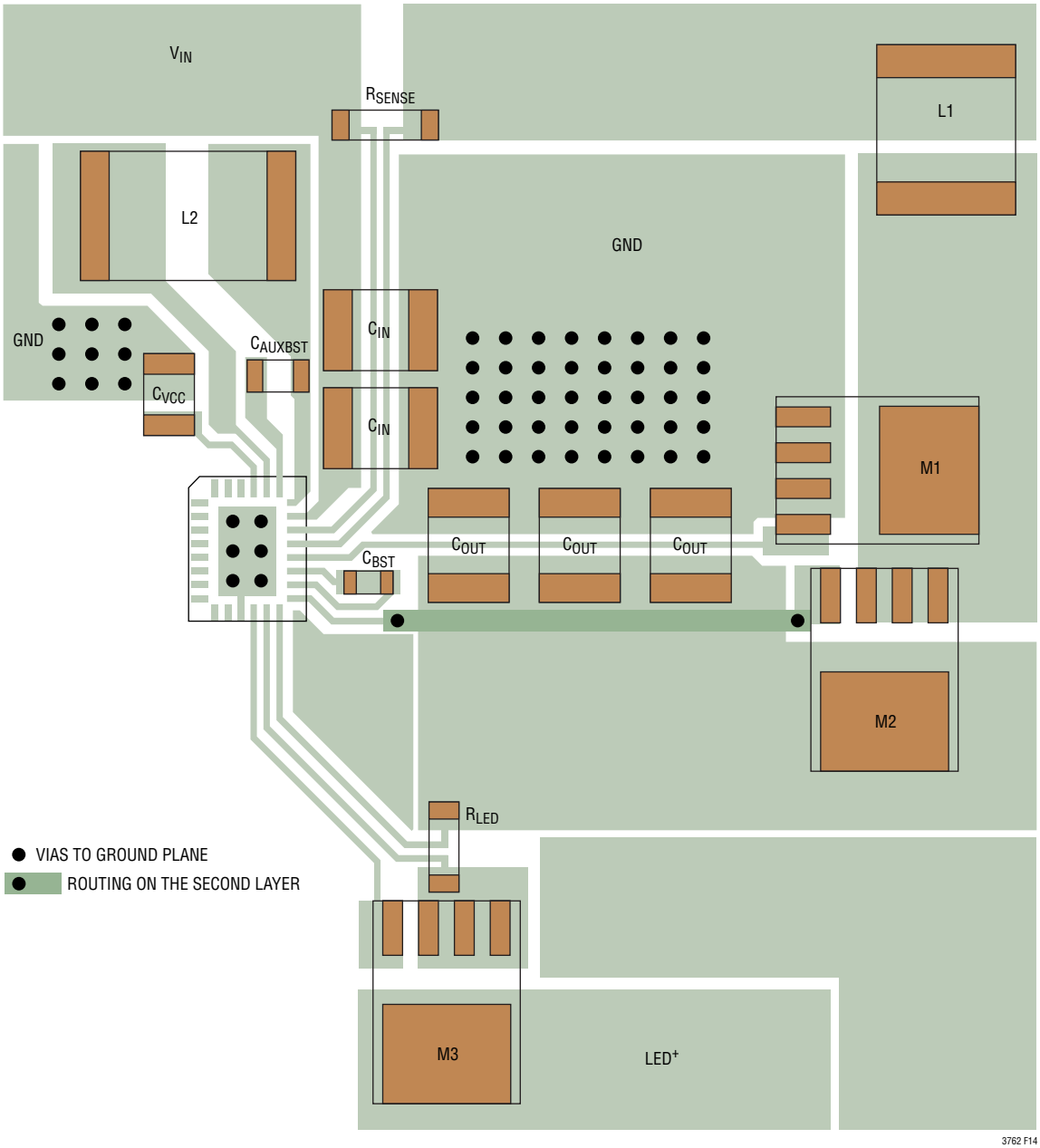
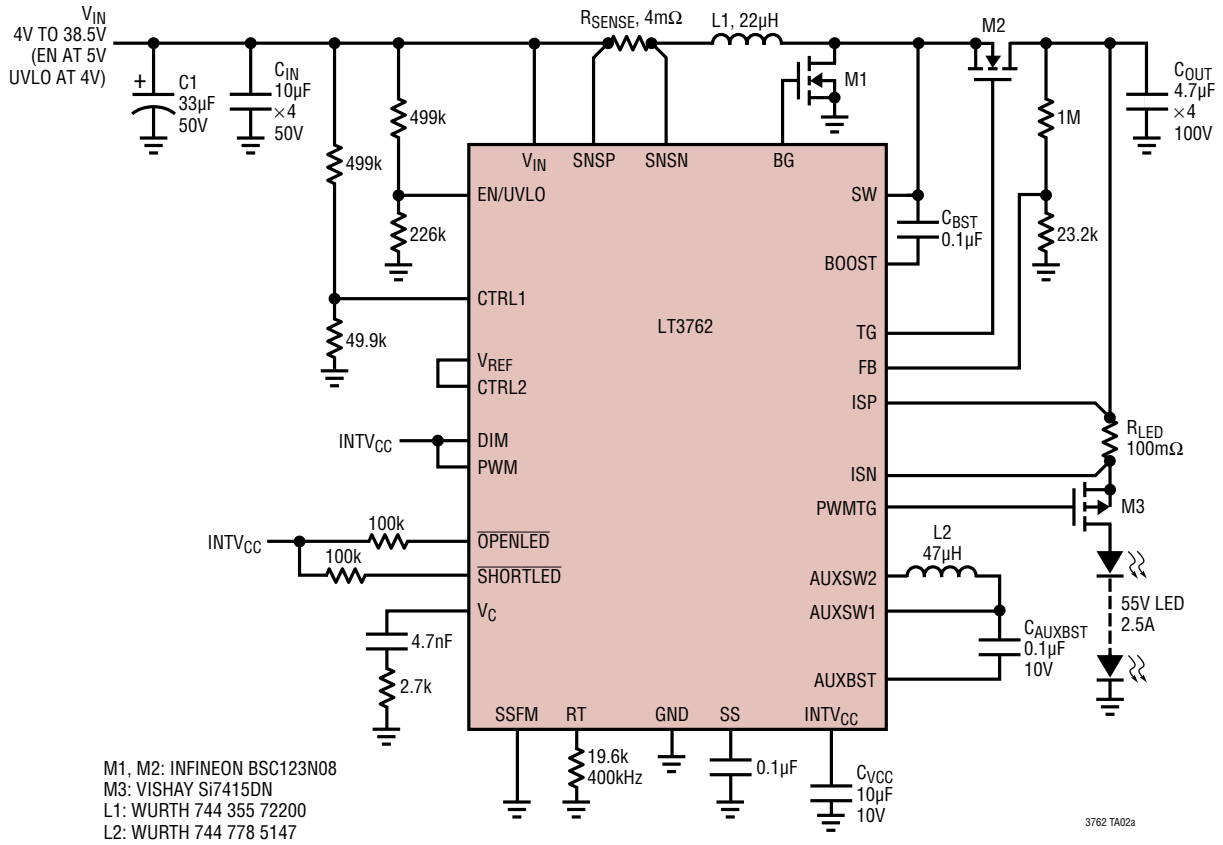


Figure 14. Simplified 2-Layer Board Layout for Boost Converter Power Stage (UFD Package)

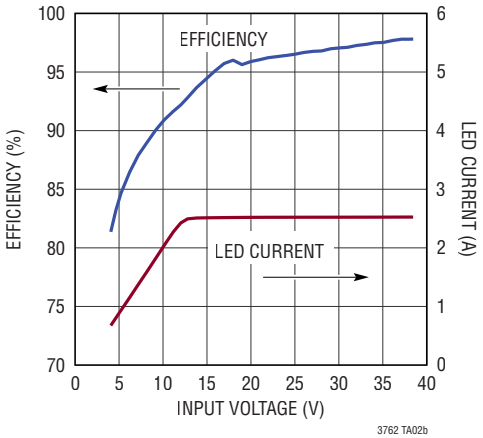
TYPICAL APPLICATIONS

140W Synchronous Boost LED Driver



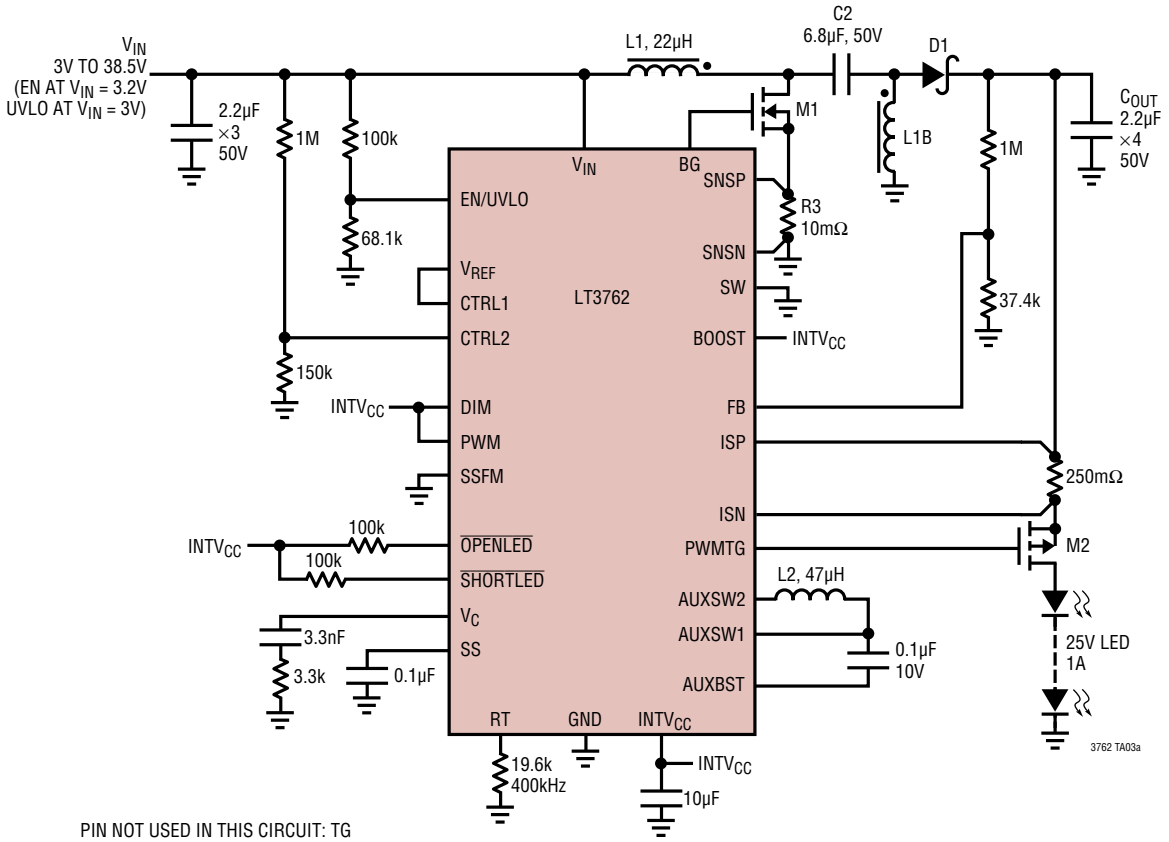
M1, M2: INFINEON BSC123N08
M3: VISHAY Si7415DN
L1: WURTH 744 355 72200
L2: WURTH 744 778 5147

Efficiency



TYPICAL APPLICATIONS

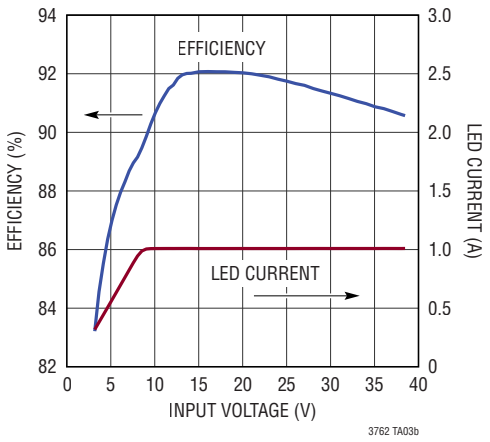
SEPIC LED Driver for Automotive DRL



PIN NOT USED IN THIS CIRCUIT: TG

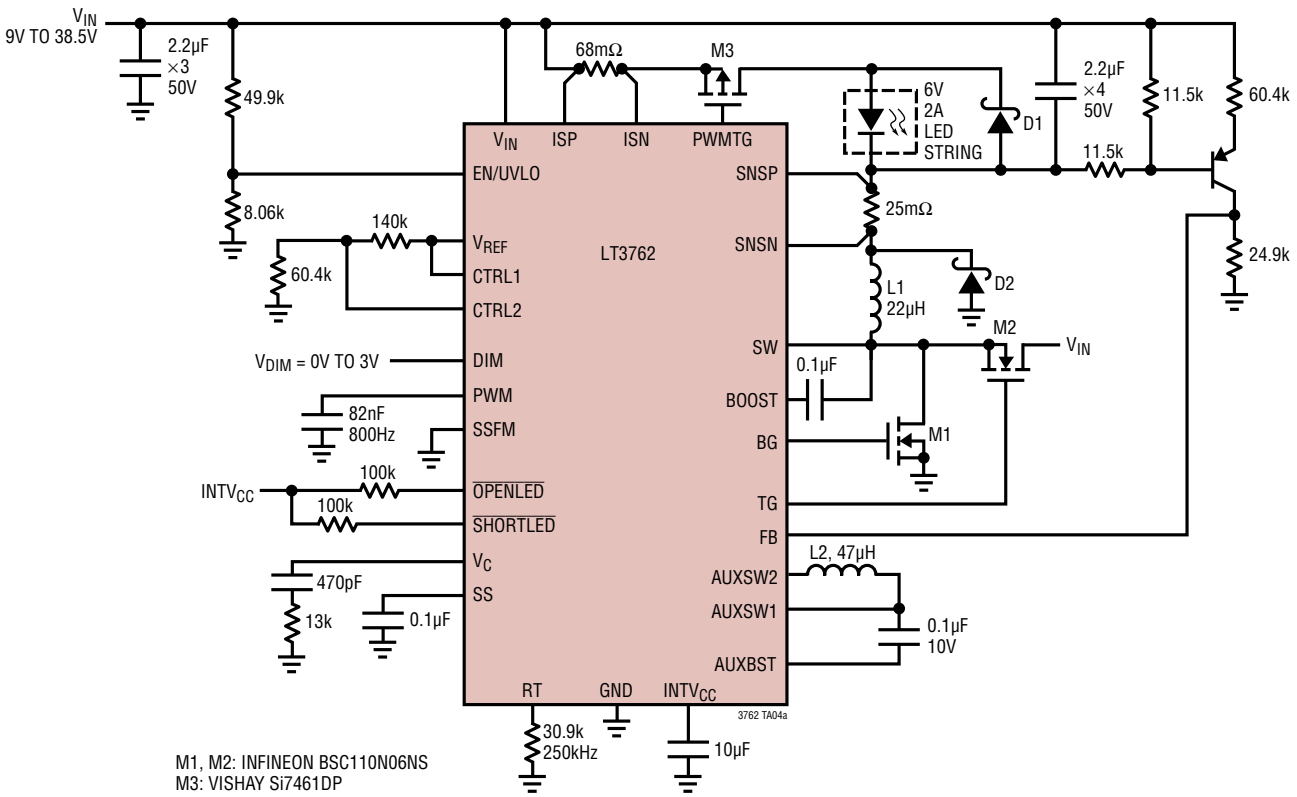
M1: INFINEON BSC123N08NS3
M2: VISHAY Si7415DN
D1: DIODES INC. PDS5100H
L1: WURTH 744 873 220
L2: WURTH 744 778 5147

Efficiency



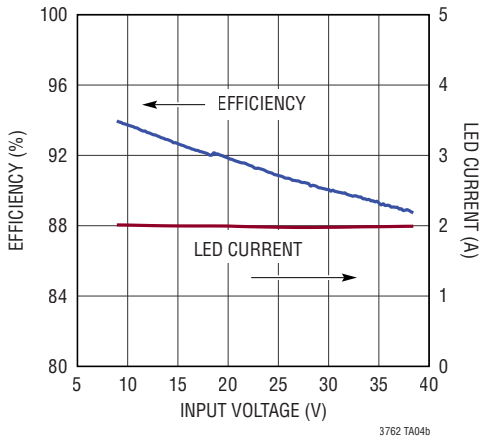
TYPICAL APPLICATIONS

Synchronous Buck Mode LED Driver

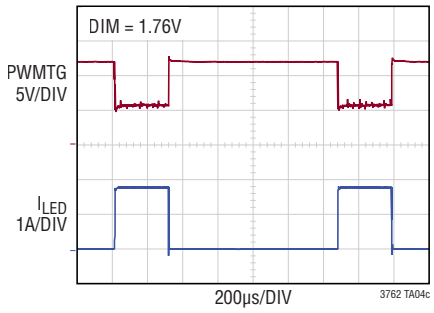


M1, M2: INFINEON BSC110N06NS
M3: VISHAY Si7461DP
L1: WURTH 744 355 72200
L2: WURTH 744 778 5147
D1, D2: CENTRAL SEMI CMSH2-20

Efficiency

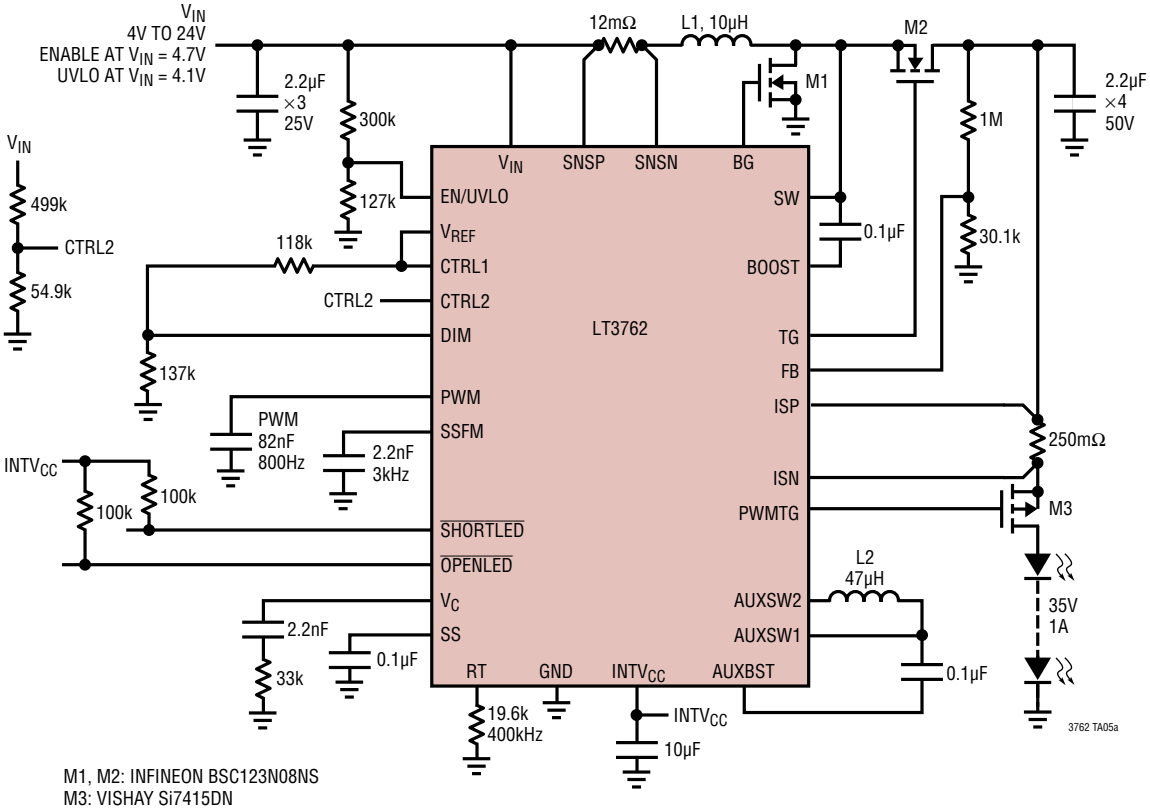


Internal PWM Dimming 25% Duty Cycle



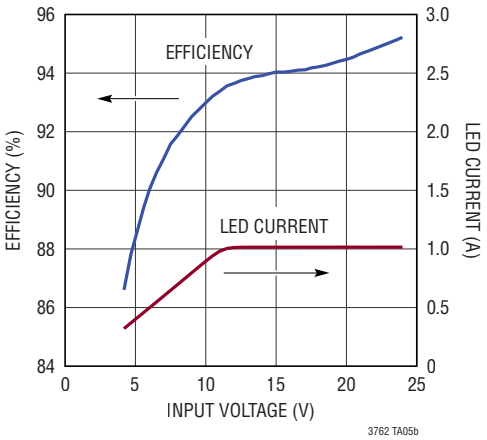
TYPICAL APPLICATIONS

Low V_{IN} Synchronous Boost LED Driver with Internal 3.5% PWM Dimming and Spread-Spectrum EMI Reduction

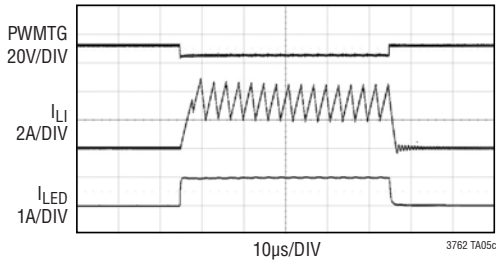


M1, M2: INFINEON BSC123N08NS
M3: VISHAY Si7415DN
L1: WURTH 744 355 1920
L2: WURTH 755 778 5147

Efficiency



Internal PWM Dimming with Spread Spectrum Frequency Modulation (Oscilloscope Set to Infinite Persistence)

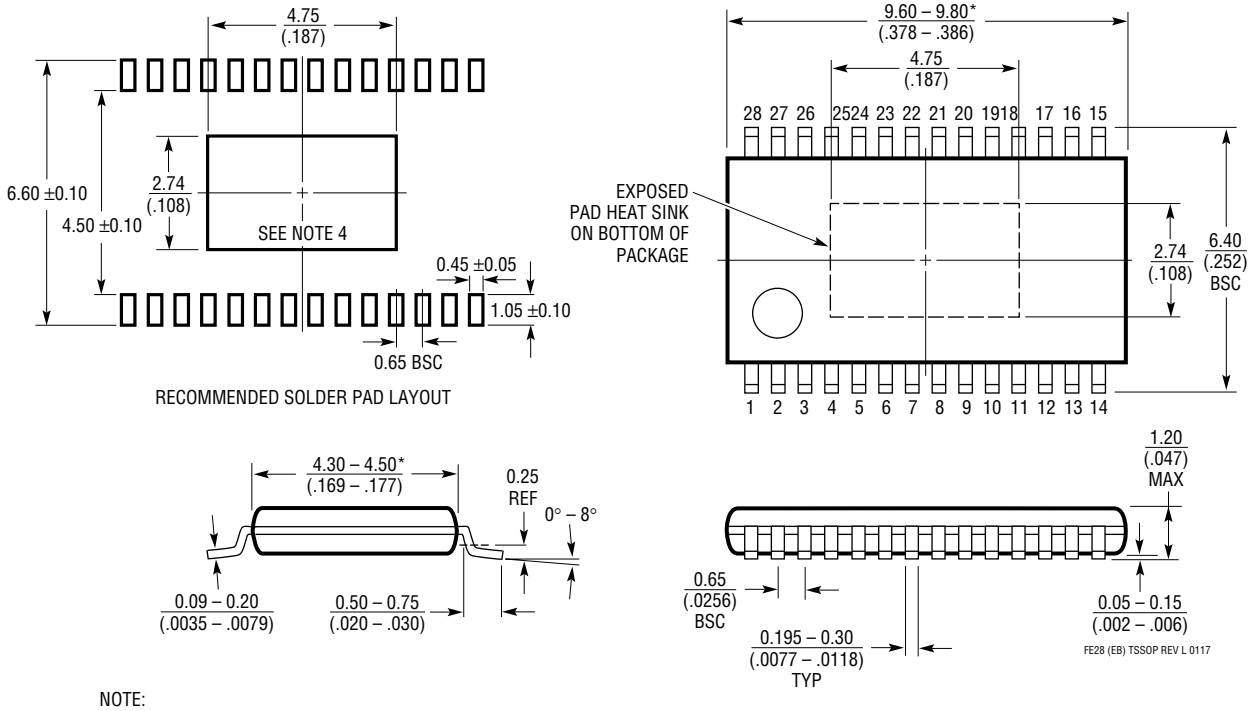


DIM = 1.19V (3.5% DUTY CYCLE AT 700Hz)

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LT3762#packaging for the most recent package drawings.

FE Package
28-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1663 Rev L)
Exposed Pad Variation EB

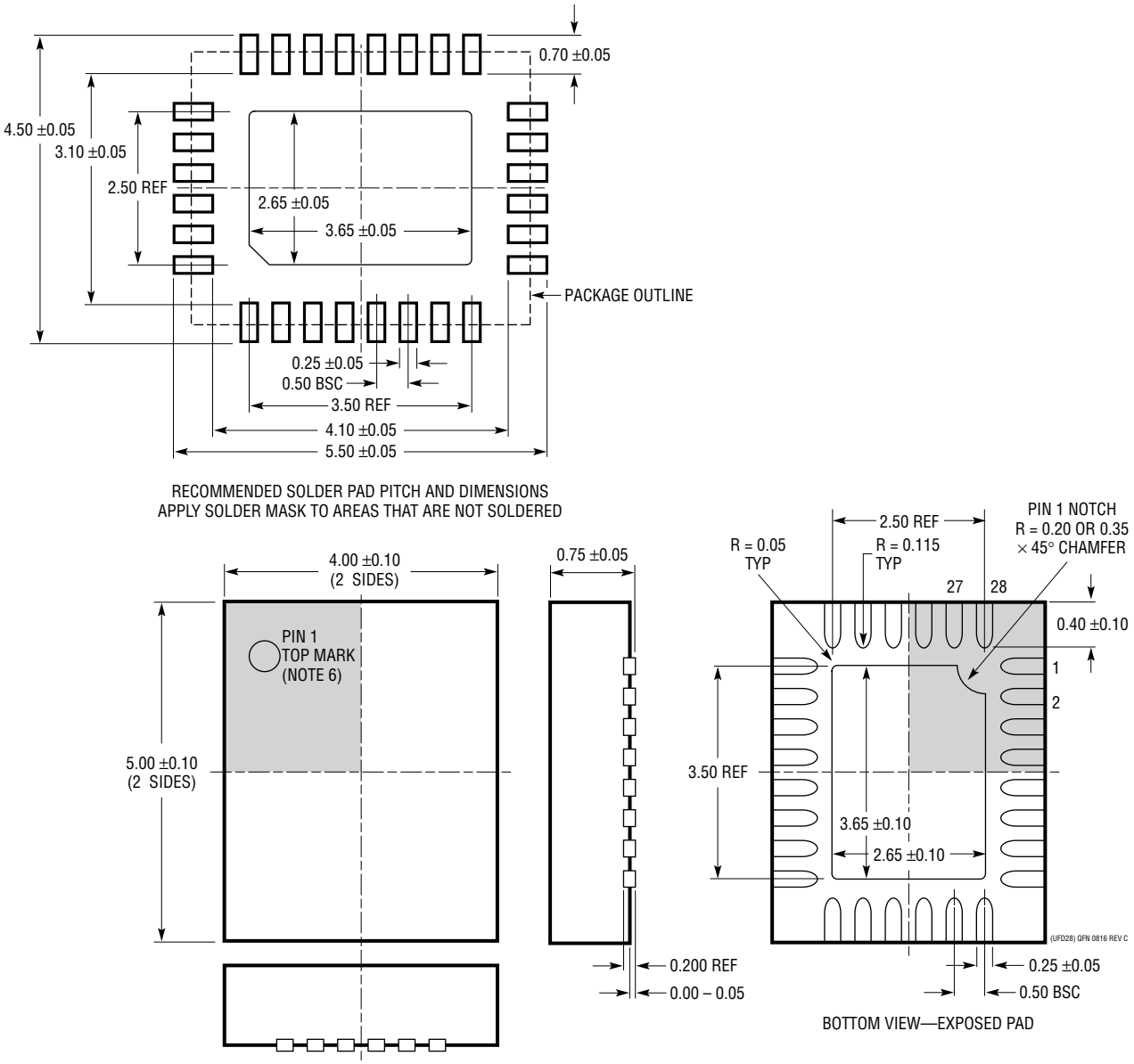


NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN MILLIMETERS (INCHES)
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LT3762#packaging for the most recent package drawings.

UFD Package
28-Lead Plastic QFN (4mm × 5mm)
(Reference LTC DWG # 05-08-1712 Rev C)



NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGHD-3).
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE