36V, 2A Synchronous Step-Up LED Driver

FEATURES

- **±2.5% LED Current Regulation**
- **±2% Output Voltage Regulation**
- **5000:1 PWM Dimming at 100Hz**
- **128:1 Internal PWM Dimming**
- **Spread Spectrum Frequency Modulation**
- **Silent Switcher® Architecture for Low EMI**
- **Operates in Boost, Buck Mode and Buck-Boost Mode**
- 2.8V to 36V Input Voltage Range
- Up to 34V LED String Voltage
- 2A, 40V Internal Switches
- 200kHz to 2MHz with SYNC Function
- Analog or Duty Cycle LED Current Control
- Open/Short LED Protection and Fault Indication
- Thermally Enhanced 28-Lead (4mm × 5mm) QFN

APPLICATIONS

- Automotive and Industrial Lighting
- Machine Vision

DESCRIPTION

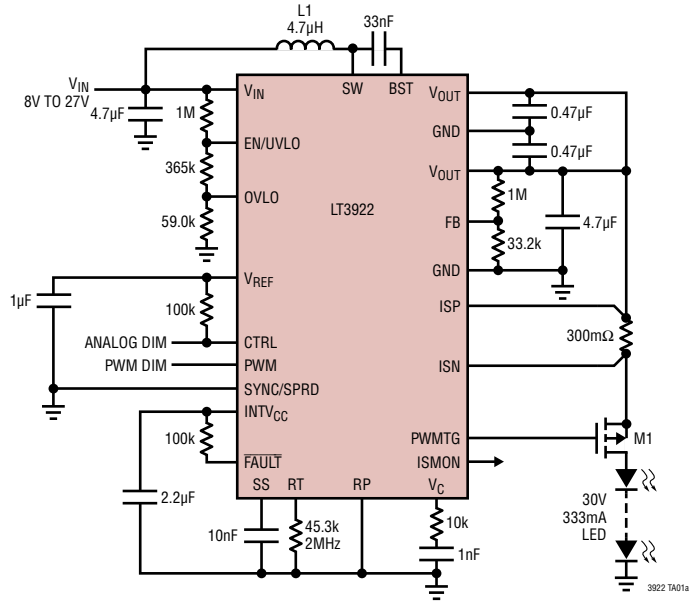
The LT®3922 is a monolithic, synchronous, step-up DC/DC converter that utilizes fixed-frequency, peak current control and provides PWM dimming for a string of LEDs. The LED current is programmed by an analog voltage or the duty cycle of pulses at the CTRL pin. The LT3922 will maintain ±2.5% current regulation through an external sense resistor over a wide range of output voltages.

The switching frequency is programmable from 200kHz to 2MHz by an external resistor at the RT pin or by an external clock applied at the SYNC/SPRD pin. With the optional spread spectrum frequency modulation enabled, the frequency varies from 100% to 125% to reduce EMI. The LT3922 also includes a driver for an external high side PMOS for PWM dimming and an internal PWM signal generator for analog control of PWM dimming when an external signal is not available.

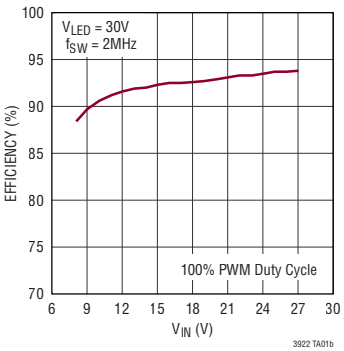
Additional features include an accurate external reference voltage for use with the CTRL and PWM pins, an LED current monitor, an accurate EN/UVLO pin threshold, open-drain fault reporting for open-circuit and short-circuit load conditions, and thermal shutdown.

TYPICAL APPLICATION

2MHz, 93% Efficient 10W (30V, 333mA) Boost LED Driver



Efficiency vs V_{IN}

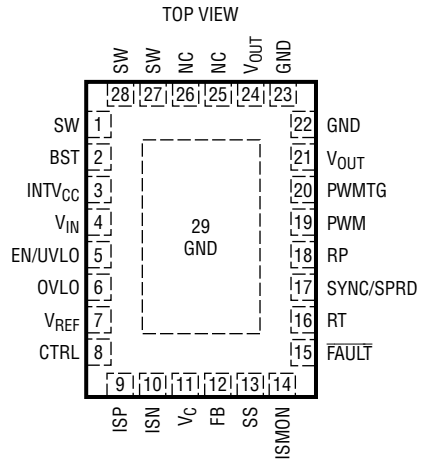


ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN} and EN/UVLO 40V
ISP, ISN, and V_{OUT} 40V
ISP – ISN 0.3V
CTRL and FB 3.3V
OVLO, PWM, SYNC/SPRD, and $\overline{FAULT}$ 6V
SS and V_C 3.3V
SW, BST, $INTV_{CC}$, V_{REF}, ISMON, PWMTG, RT, and RP ..... (Note 2)
Operating Junction Temperature Range (Notes 3, 4)
LT3922E/LT3922I ..... –40 to 125°C
LT3922H ..... –40 to 150°C
Storage Temperature Range ..... –60 to 150°C

PIN CONFIGURATION



UFD PACKAGE
28-LEAD (4mm × 5mm) PLASTIC QFN
θ_{JA} = 34°C/W
EXPOSED PAD (PIN 29) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3922EUFD#PBF	LT3922EUFD#TRPBF	3922	28-Lead (4mm × 5mm) Plastic QFN	–40°C to 125°C
LT3922IUFD#PBF	LT3922IUFD#TRPBF	3922	28-Lead (4mm × 5mm) Plastic QFN	–40°C to 125°C
LT3922HUFD#PBF	LT3922HUFD#TRPBF	3922	28-Lead (4mm × 5mm) Plastic QFN	–40°C to 150°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, V_{IN} = 12V, $V_{EN/UVLO}$ = 2V unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range			2.8		36	V
V_{IN} Pin Quiescent Current	$V_{EN/UVLO}$ = 1.5V, Not Switching $V_{EN/UVLO}$ = 0.1V, Shutdown			2.9	4 1	mA µA
EN/UVLO Threshold (Falling)			1.260	1.330	1.400	V
EN/UVLO Rising Hysteresis				25		mV
EN/UVLO Pin Current	$V_{EN/UVLO}$ = 1.2V			2		µA
Input OVLO Threshold (Rising)			1.145	1.205	1.265	V
Input OVLO Falling Hysteresis				50		mV
OVLO Pin Current	V_{OVLO} = 1.0V		–100		100	nA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, V_{IN} = 12V, $V_{EN/UVLO}$ = 2V unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Reference						
V_{REF} Voltage	I_{VREF} = 10µA I_{VREF} = 500µA	● ●	1.97 1.985	2 2	2.03 2.015	V V
V_{REF} Pin Current Limit	V_{REF} = 0V, Current Out of Pin			3.2		mA
LED Current Regulation						
CTRL-Off Threshold (Falling)		●	200	210	220	mV
CTRL-Off Rising Hysteresis				15		mV
CTRL Pin Current	V_{CTRL} = 2V		–100		100	nA
Sense Voltage (V_{ISP}–V_{ISN}) (Analog Input)	V_{CTRL} = 2V (100%), V_{ISP} = 24V V_{CTRL} = 0.75V (50%), V_{ISP} = 24V V_{CTRL} = 0.3V (5%), V_{ISP} = 24V	● ● ●	97.5 48 3.5	100 50 5	102.5 52 6.5	mV mV mV
ISP Pin Current	V_{ISP} = 24.1V, V_{ISN} = 24V, V_{CTRL} = 2V			75		µA
ISN Pin Current	V_{ISP} = 24.1V, V_{ISN} = 24V , V_{CTRL} = 2V			75		µA
Current Error Amplifier Transconductance	V_{ISP} = 24V			140		µA/V
Duty Cycle Control of LED Current						
Sense Voltage (V_{ISP}–V_{ISN}) (Duty Cycle Input)	CTRL Duty = 75% (100%), V_{ISP} = 24V CTRL Duty = 37.5% (50%), V_{ISP} = 24V CTRL Duty = 15% (5%), V_{ISP} = 24V		99 49 4	100 50 5	101 51 6	mV mV mV
CTRL Pulse Input High (V_{IH})			1.6			V
CTRL Pulse Input Low (V_{IL})					0.4	V
CTRL Pulse Input Frequency Range			10		200	kHz
Voltage Regulation						
FB Regulation Voltage	V_{CTRL} = 2V	●	1.175	1.200	1.225	V
FB Pin Current	FB in Regulation		–100		100	nA
Voltage Error Amplifier Transconductance				1000		µA/V
$INTV_{CC}$ Regulator						
$INTV_{CC}$ Voltage			2.7	3	3.3	V
$INTV_{CC}$ Pin Current Limit	V_{INTVCC} = 0V, Current Out of Pin			20		mA
Power Stage						
Peak Current Limit	V_{IN} = 3V		2.0	2.3	2.6	A
Bottom Switch Minimum Off-Time		●	15	25	35	ns
Bottom Switch On-Resistance				140		mΩ
Top Switch On-Resistance				155		mΩ
Oscillator						
Programmed Switching Frequency (f_{SW})	R_T = 45.3k, $V_{SYNC/SPRD}$ = 0V R_T = 499k, $V_{SYNC/SPRD}$ = 0V	● ●	1880 175	2000 200	2120 245	kHz kHz
Spread Spectrum Frequency Range	R_T = 45.3k, $V_{SYNC/SPRD}$ = 3V R_T = 499k, $V_{SYNC/SPRD}$ = 3V		1880 175		2650 306	kHz kHz
RT Pin Current Limit	V_{RT} = 0V, Current Out of Pin			75		µA
SYNC/SPRD Threshold (Rising)				1.4	1.5	V
SYNC/SPRD Falling Hysteresis				0.2		V
SYNC/SPRD Pin Current	$V_{SYNC/SPRD}$ = 5V		–100		100	nA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, V_{IN} = 12V, $V_{EN/UVLO}$ = 2V unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Soft-Start						
SS Pin Charging Current	V_{SS} = 1V			20		µA
SS Pin Discharging Current	V_{SS} = 2V			2		µA
SS Lower Threshold				0.2		V
SS Higher Threshold				1.7		V
Fault Detection						
Open-Circuit Threshold (FB Rising)	V_{ISP} = V_{ISN} = 20V	●	1.117	1.140	1.163	V
Open-Circuit Falling Hysteresis				50		mV
LED Short-Circuit Threshold (V_{ISP} – V_{ISN})	V_{ISP} = 20V			150		mV
$\overline{FAULT}$ Pull-Down Current	$V_{\overline{FAULT}}$ = 0.2V, V_{FB} = 1.25V		0.8			mA
$\overline{FAULT}$ Leakage Current	$V_{\overline{FAULT}}$ = 3V, V_{FB} = 0.7V		–100		100	nA
Overvoltage Protection						
FB Overvoltage Threshold (Rising)		●	1.240	1.266	1.292	V
FB Overvoltage Falling Hysteresis				22		mV
LED Current Monitor						
ISMON Voltage	V_{ISP} – V_{ISN} = 100mV (100%), V_{ISP} = 24V V_{ISP} – V_{ISN} = 10mV (10%), V_{ISP} = 24V		0.980 80	1.000 100	1.020 120	V mV
PWM Driver						
PWMTG Gate Drive (V_{OUT} – V_{PWMTG})	V_{OUT} = 20V, V_{PWM} = 1.5V			10	11	V
PWM Threshold (Rising)				1.4		V
PWM Falling Hysteresis				0.2		V
PWM Pin Current	V_{PWM} = 2V		–100		100	nA
PWM to PWMTG Propagation Delay Turn-On Turn-Off	C_{PWMTG} = 2.1nF (Connected from V_{OUT} to PWMTG) V_{OUT} = 20V			 110 140		 ns ns
Internal PWM Dimming						
PWM Voltage for 100% PWM Dimming	R_P = 28.7k, V_{REF} = 2V		2.00			V
PWM Voltage for 0% PWM Dimming	R_P = 28.7k, V_{REF} = 2V				0.99	V
PWM Dimming Accuracy	R_P = 28.7k, V_{REF} = 2V, V_{PWM} = 1.1V R_P = 28.7k, V_{REF} = 2V, V_{PWM} = 1.9V		7.5 89	10.5 92	13.5 95	% %
PWM Dimming Frequency	R_P = 28.7k, R_T = 45.3k, $V_{SYNC/SPRD}$ = 0V R_P = 332k, R_T = 45.3k, $V_{SYNC/SPRD}$ = 0V		7.34 115	7.81 122	8.28 129	kHz Hz
RP Pin Current Limit	V_{RP} = 0V, Current Out of Pin			65		µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Do not apply a positive or negative voltage source to these pins, otherwise permanent damage may occur.

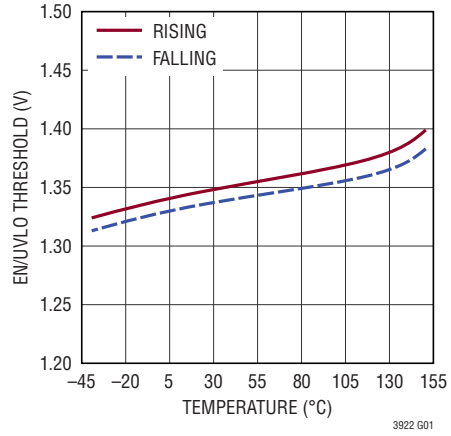
Note 3: The LT3922E is guaranteed to meet performance specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT3922I is guaranteed to meet performance specifications over the –40°C to 125°C operating junction temperature range. The LT3922H is guaranteed over the –40°C to 150°C operating junction temperature range. Operating lifetime is derated at junction temperatures greater than 125°C.

Note 4: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. The maximum rated junction temperature will be exceeded when this protection is active. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability or permanently damage the device.

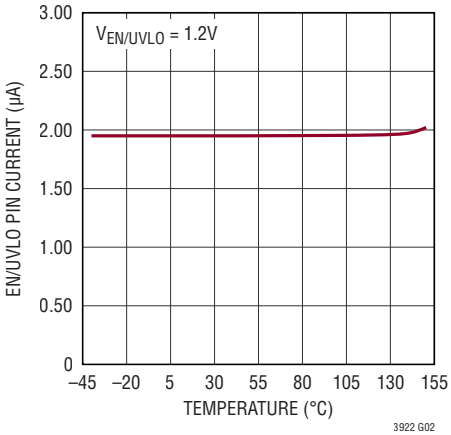
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, T_A = 25°C, unless otherwise noted.

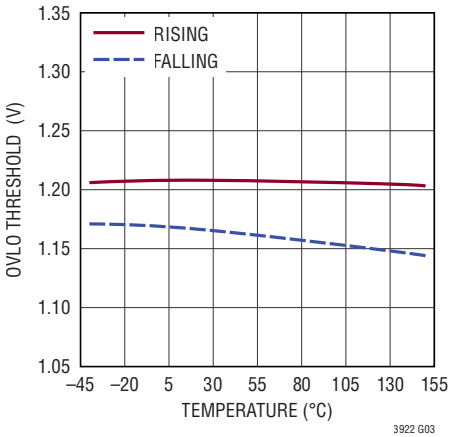
EN/UVLO Thresholds



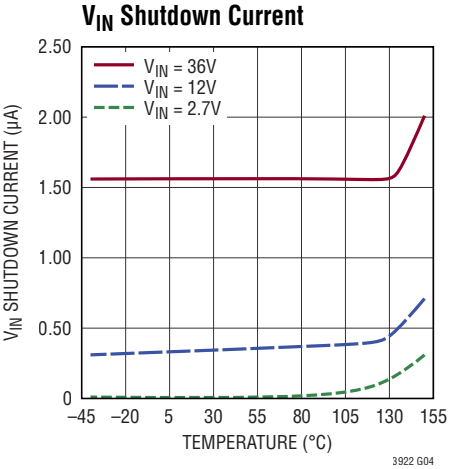
EN/UVLO Pin Current



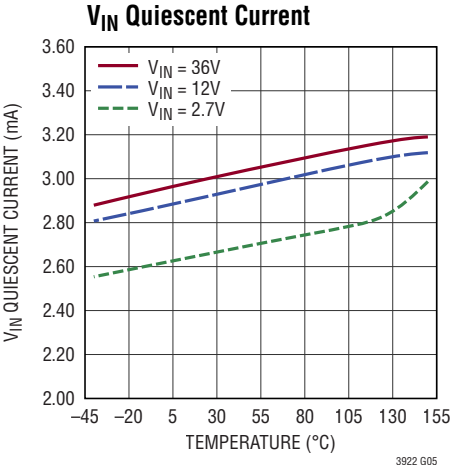
OVLO Threshold



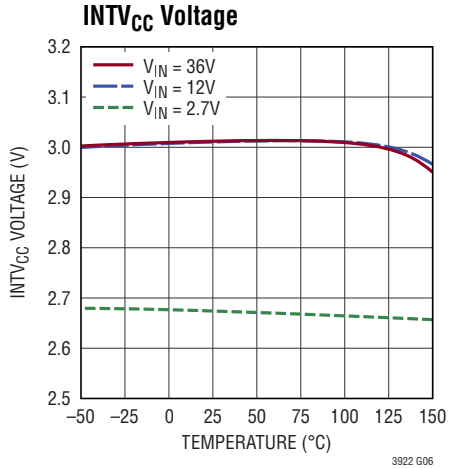
V_{IN} Shutdown Current



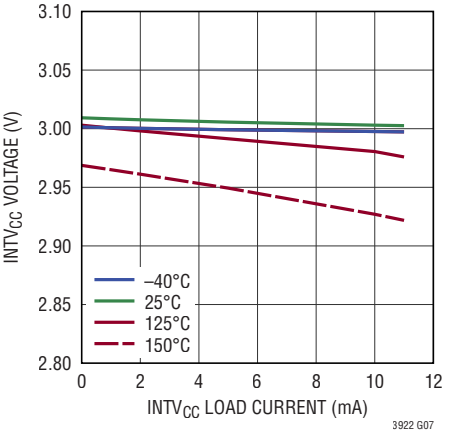
V_{IN} Quiescent Current



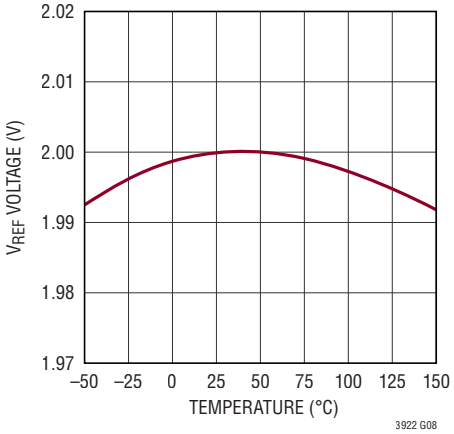
$INTV_{CC}$ Voltage



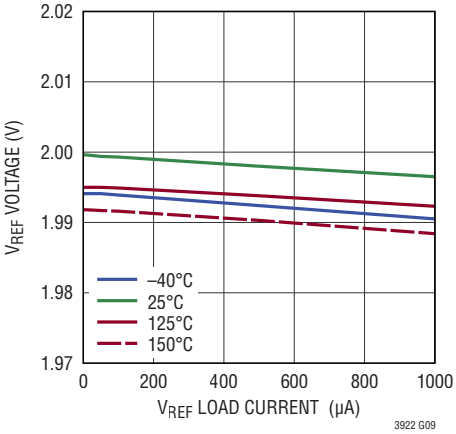
$INTV_{CC}$ Load Regulation



V_{REF} Voltage



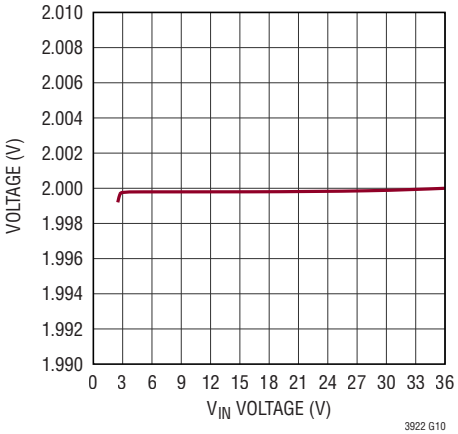
V_{REF} Load Regulation



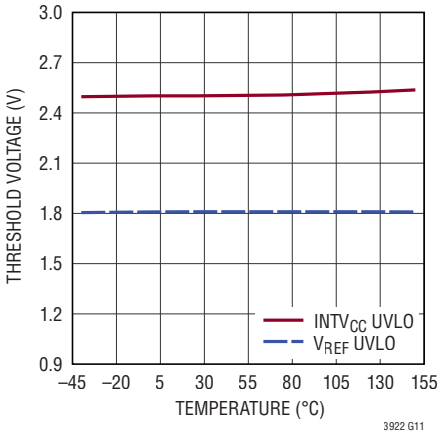
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, T_A = 25°C, unless otherwise noted.

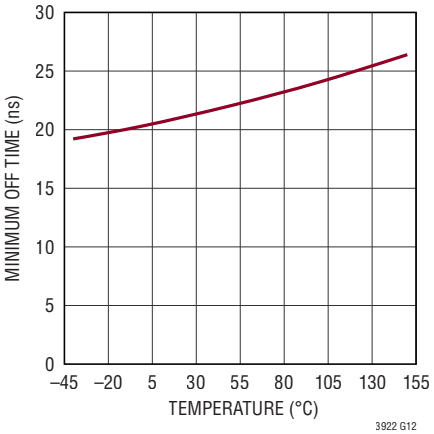
V_{REF} Line Regulation



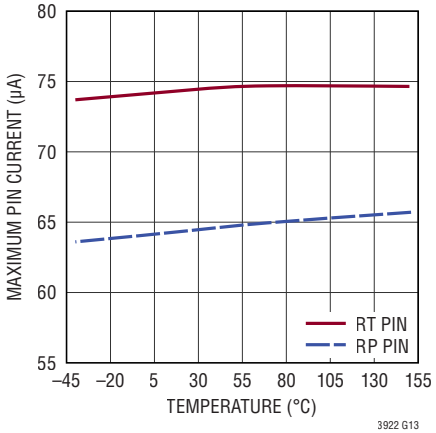
$INTV_{CC}$ and V_{REF} UVLO Falling Thresholds



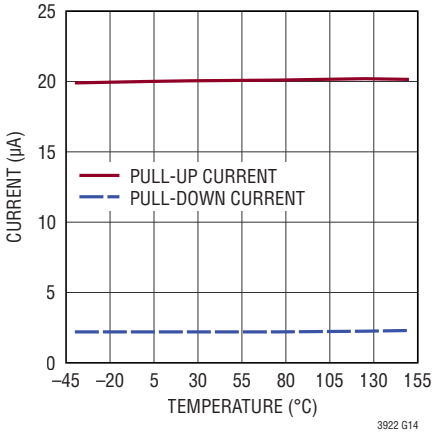
Minimum Off Time



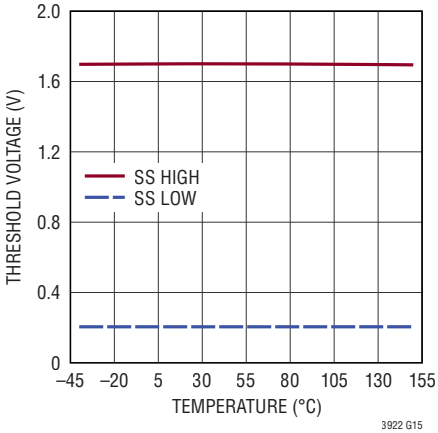
RT and RP Pin Current Limits



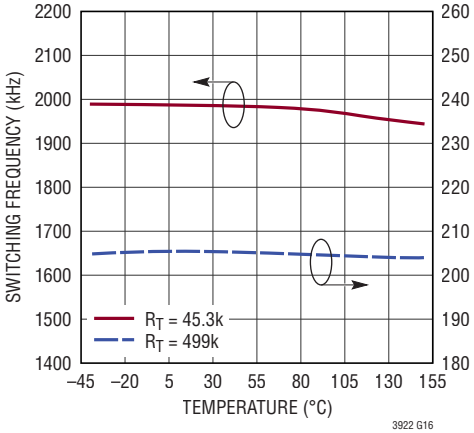
SS Currents



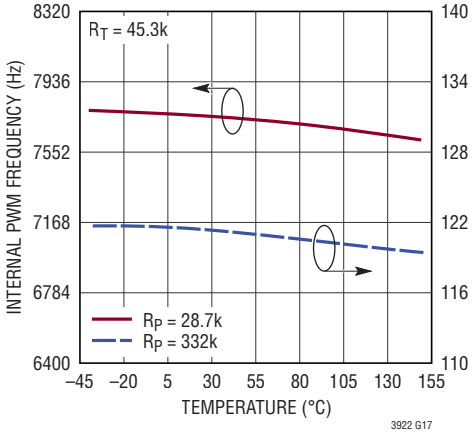
SS Thresholds



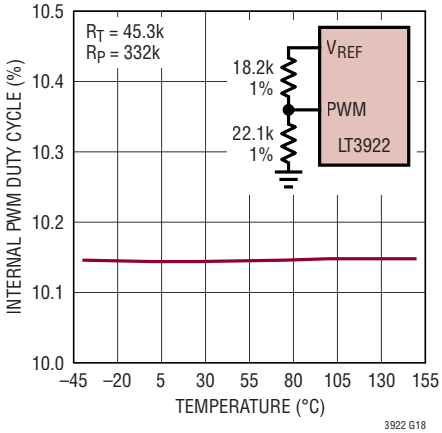
Switching Frequency



Internal PWM Frequency



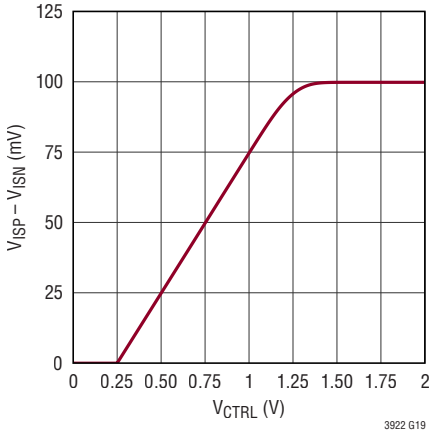
Internal PWM Duty Cycle



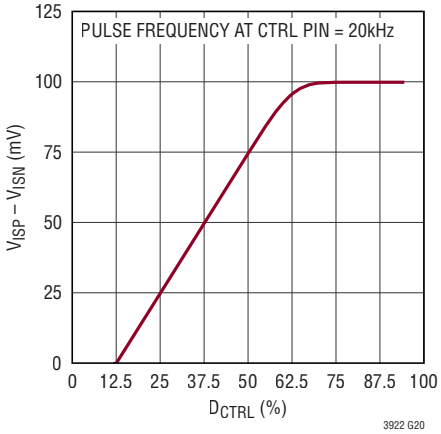
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, T_A = 25°C, unless otherwise noted.

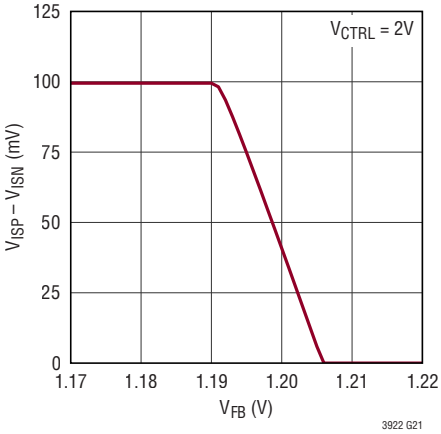
LED Current (Analog CTRL)



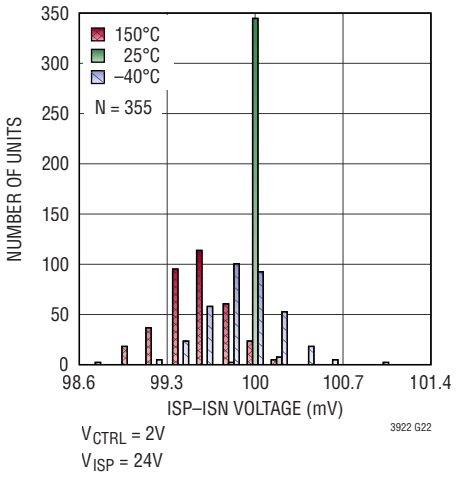
LED Current (Digital CTRL)



LED Voltage Limit

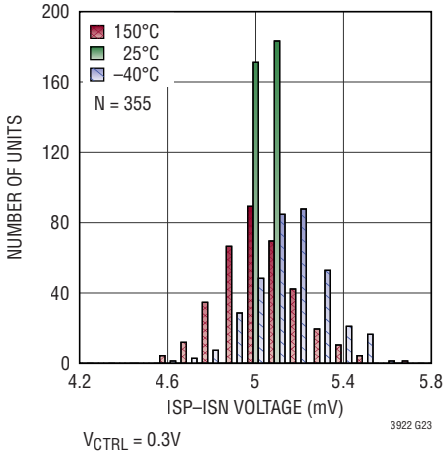


LED Current (100% Regulation)



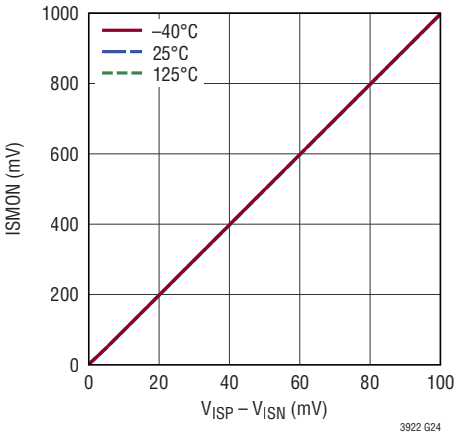
V_{CTRL} = 2V
V_{ISP} = 24V

LED Current (5% Regulation)

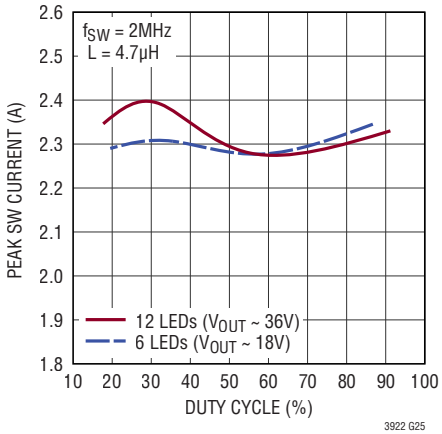


V_{CTRL} = 0.3V
V_{ISP} = 24V

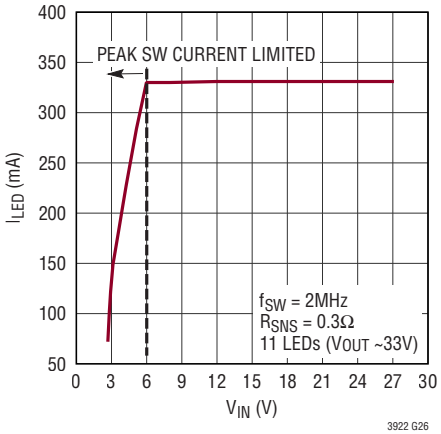
ISMON Voltage



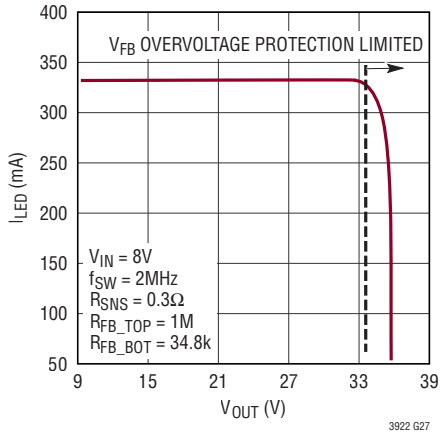
Peak SW Current Limit



LED Current Line Regulation



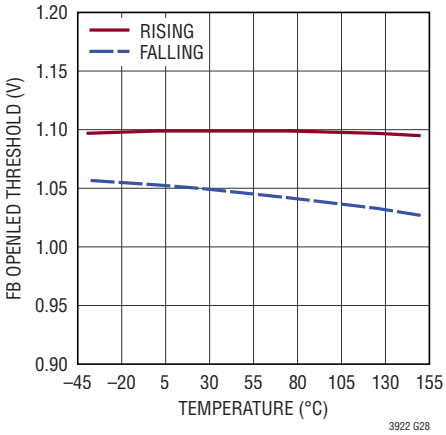
LED Current vs V_{OUT}



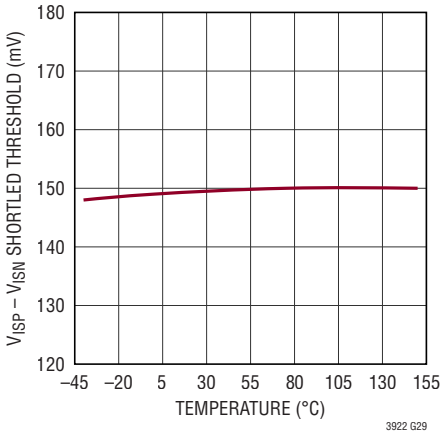
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, T_A = 25°C, unless otherwise noted.

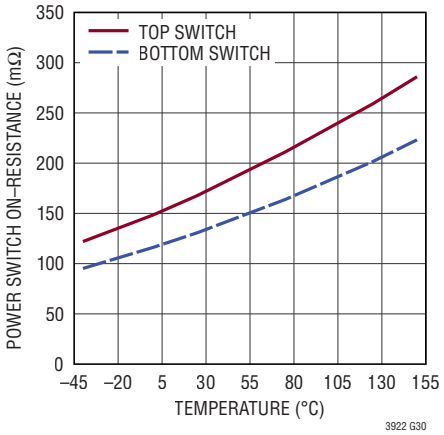
FB OPENLED Threshold



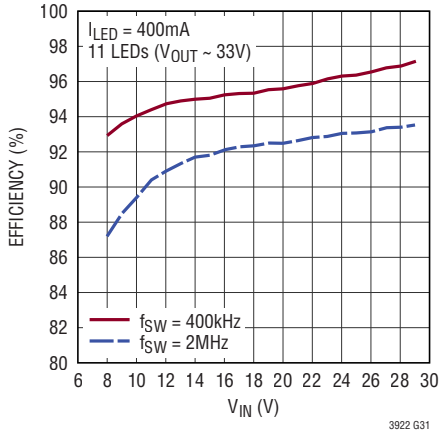
$V_{ISP} – V_{ISN}$ SHORTLED Threshold



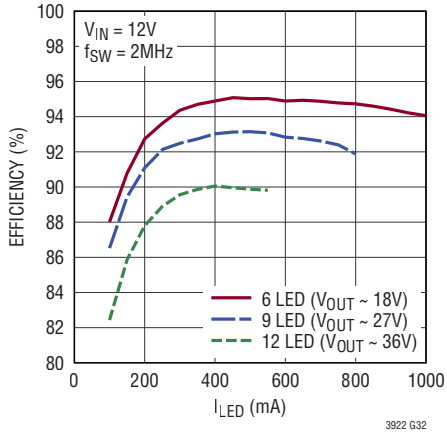
Power Switch On-Resistance



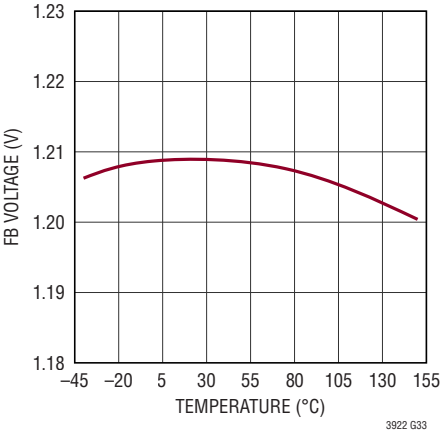
Efficiency vs V_{IN}



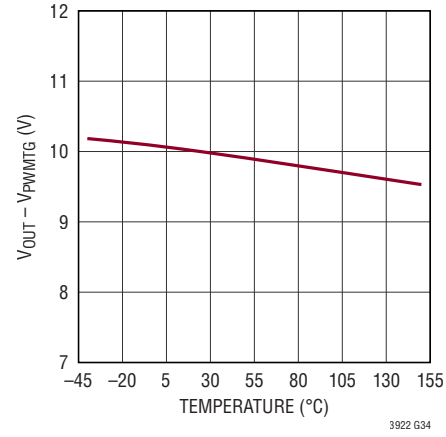
Efficiency vs I_{LED}



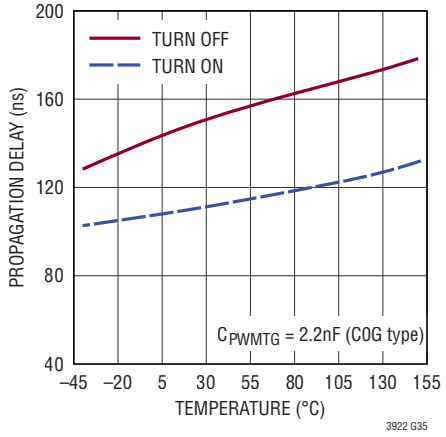
Regulated FB Voltage



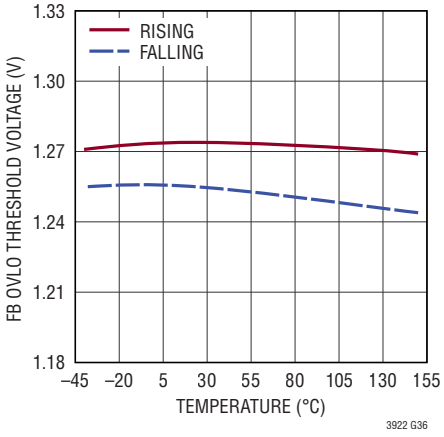
PWMTG ON Voltage



PWM Driver Propagation Delay

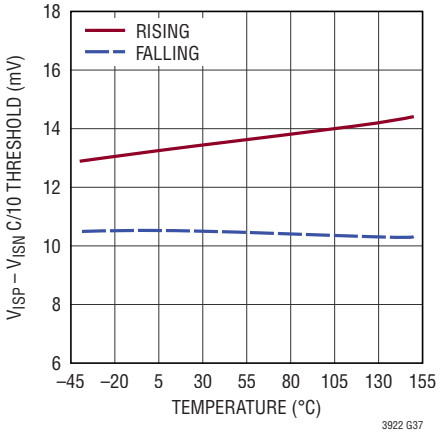


FB OVLO Threshold

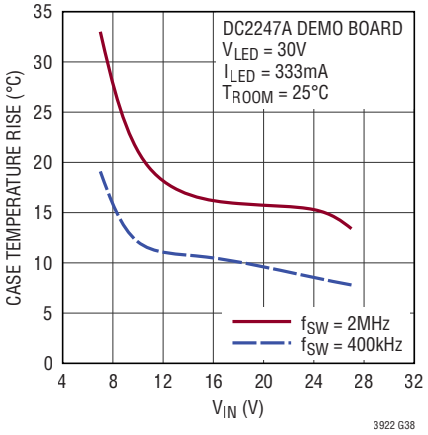


TYPICAL PERFORMANCE CHARACTERISTICS V_{IN} = 12V, T_A = 25°C, unless otherwise noted.

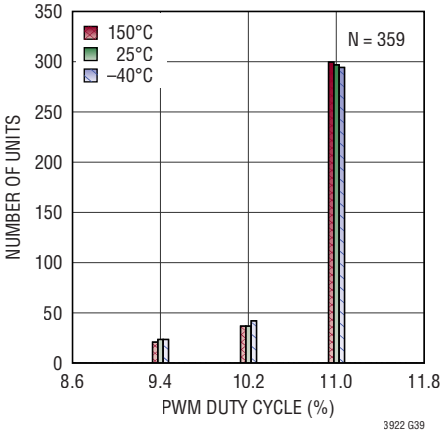
C/10 Threshold



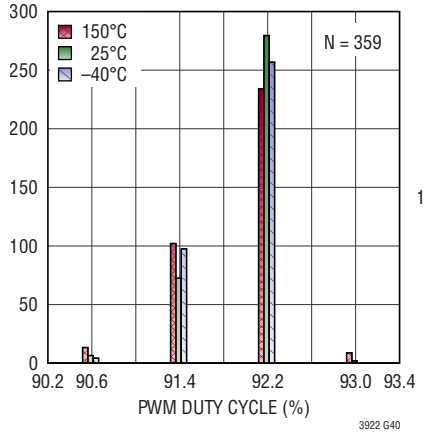
Case Temperature Rise



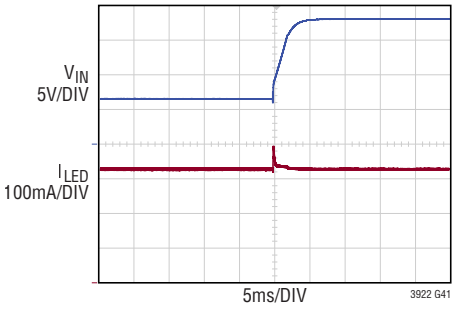
Internal PWM Duty Cycle (10%)



Internal PWM Duty Cycle (90%)

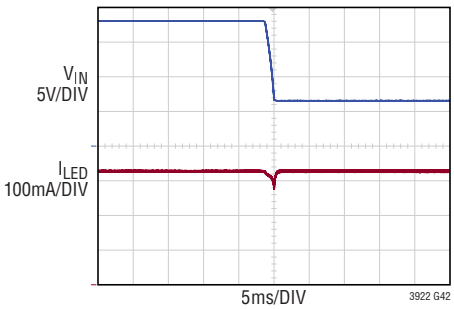


Input Voltage Transient Response



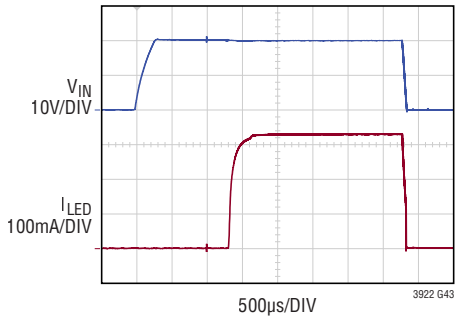
FRONT PAGE APPLICATION
6.5V to 18V INPUT VOLTAGE TRANSIENT
V_{LED} = 30V
I_{LED} = 333mA

Input Voltage Transient Response



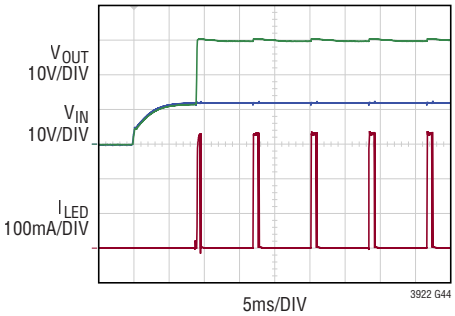
FRONT PAGE APPLICATION
18V to 6.5V INPUT VOLTAGE TRANSIENT
V_{LED} = 30V
I_{LED} = 333mA

Turn ON and OFF Performance



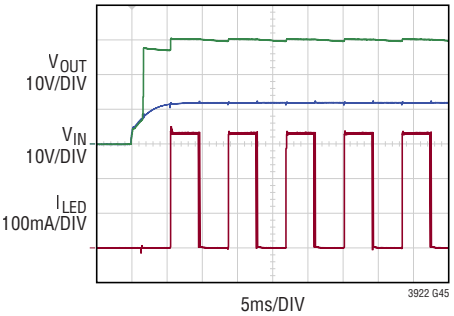
FRONT PAGE APPLICATION
V_{LED} = 30V
I_{LED} = 333mA

Start-Up with 10% Internal PWM



FRONT PAGE APPLICATION WITH PWM = 1.1V
RP = 332k TO GND
V_{LED} = 30V
I_{LED} = 333mA

Start-Up with 50% Internal PWM



FRONT PAGE APPLICATION WITH PWM = 1.5V
RP = 332k TO GND
V_{LED} = 30V
I_{LED} = 333mA

PIN FUNCTIONS

SW: Switch Pins. These pins are internally connected to the power devices and drivers. They should always be tied together. In normal operation, the voltage of these pins will switch between the output voltage and zero at the programmed frequency. Do not force any voltage on these pins.

BST: Boost Pin. This pin supplies the top power switch GATE driver. Connect a 33nF capacitor between this pin and SW close to the package. An internal diode from $INTV_{CC}$ to BST will charge the capacitor when the SW pin switches low.

$INTV_{CC}$: Internally Regulated, Low-Voltage Supply Pin. This pin provides the power for the converter switch GATE drivers. Do not force any voltage on this pin. Place a 2.2µF bypass capacitor to GND close to the package.

V_{IN}: Input Voltage Pin. This pin supplies power to the internal, high-performance analog circuitry. Connect a bypass capacitor between this pin and GND.

EN/UVLO: Enable and Undervoltage Lockout Pin. A voltage at this pin greater than 1.33V will enable switching, and a voltage less than 0.1V is guaranteed to shut down the internal current bias and sub-regulators. A resistor network between this pin and ground can be used to set the pin voltage and automatically lockout the part when V_{IN} is below a certain level. No internal components pull up or down on this pin, so it requires an external voltage bias for normal operation. This pin may be tied directly to V_{IN}.

OVLO: Input Overvoltage Lockout Pin. When the voltage at this pin rises above 1.205V, the system disables switching and resets the soft-start capacitor. Do not leave this pin open. Tie this pin to GND when the OVLO function is not used.

V_{REF}: Reference Voltage Pin. This pin provides a buffered 2V reference capable of 3mA drive. It can be used to supply resistor networks for setting the voltages at the CTRL and PWM pins. Bypass with a 1µF capacitor to GND.

CTRL: Control Pin. An analog voltage from 250mV to 1.25V at this pin programs the regulated voltage between ISP and ISN (and therefore, the regulated current supplied to the load). Alternatively, a digital pulse at this pin with duty cycle from 12.5% to 62.5% can be used to program the regulated voltage. Below 200mV or 10% duty cycle, the CTRL pin voltage disables switching. For more detail, see Typical Performance Characteristics and Applications Information sections.

ISP: Positive Current Sense Pin. This pin is one of the inputs to the internal current sense error amplifier. It should be connected to the positive side of the external sense resistor. Use Kelvin connection for accurate current sensing.

ISN: Negative Current Sense Pin. This pin is one of the inputs to the internal current sense error amplifier. It should be connected to the negative side of the external sense resistor. Use Kelvin connection for accurate current sensing.

V_C: Compensation Pin. A resistor and capacitor connected in series from this pin to GND stabilize the current and voltage regulation. Typical resistor and capacitor values are from 0k to 100k and from 0.1nF to 10nF, respectively.

FB: Feedback Pin. When the voltage at this pin is near 1.2V the regulated current is automatically reduced from the programmed value. A resistor network between this pin and V_{OUT} can be used to set a limit for the output voltage. If the voltage at the FB pin reaches 1.266V, a FB overvoltage lockout comparator disables switching.

SS: Soft-Start Pin. At startup and recovery from fault conditions, a 20µA current charges the capacitor and the FB voltage tracks the rising voltage at this pin until the load current reaches its programmed level. Typical values for the capacitor are 10nF to 100nF. Using a single resistor from SS to $INTV_{CC}$, the LT3922 can be set in two different fault modes for the shorted LED conditions: hiccup (no resistor) and latchoff (100k). Refer to the Application Information section for a detailed explanation.

ISMON: Output Current Monitoring Pin. This pin provides a buffered voltage output equal to 10mV for every 1mV between ISP and ISN.

PIN FUNCTIONS

$\overline{\text{FAULT}}$: Fault Pin. Connect to $INTV_{CC}$ through a resistance of 100k. An internal switch pulls this pin low when any of following conditions happen:

1. Open LED: $V_{FB} > 1.14V$ and $(V_{ISP} – V_{ISN}) < 10mV$
2. Shorted LED:
   $(V_{ISP} – V_{ISN}) > 150mV$ for more than 300us, or
   $(V_{ISP} – V_{ISN}) > 700mV$ (typical), or
   $V_{OUT} < (V_{IN} – 2V)$

RT: Timing Resistor Pin. A resistor from this pin to GND programs the switching frequency between 200kHz and 2MHz. Do not leave this pin open.

SYNC/SPRD: Synchronization Pin. To override the programmed switching frequency, drive this pin with an external clock having a frequency between 200kHz and 2MHz. Even when using the external clock, select an R_T resistor that corresponds to the desired switching frequency. Tie the pin to $INTV_{CC}$ to enable Spread Spectrum Frequency Modulation. This pin should be tied to GND when not in use.

RP: PWM Resistor Pin. Connect a resistor from this pin to GND to set the frequency of the internal PWM signal. Do not use a resistor larger than 1MΩ. If using an external PWM pulse for LED dimming, tie this pin to GND. Refer to the Application Information section for a detailed explanation.

PWM: PWM Input Pin. With the RP pin tied to GND, drive this pin with a digital pulse to control PWM dimming of the LEDs. Alternatively, when using a resistor on the RP pin to GND, set the voltage of this pin between 1V and 2V to generate an internal pulse with duty cycle between 0% and 100%. When using an analog signal, place a 1µF bypass capacitor between this pin and GND. Tie this pin high when PWM dimming is not required.

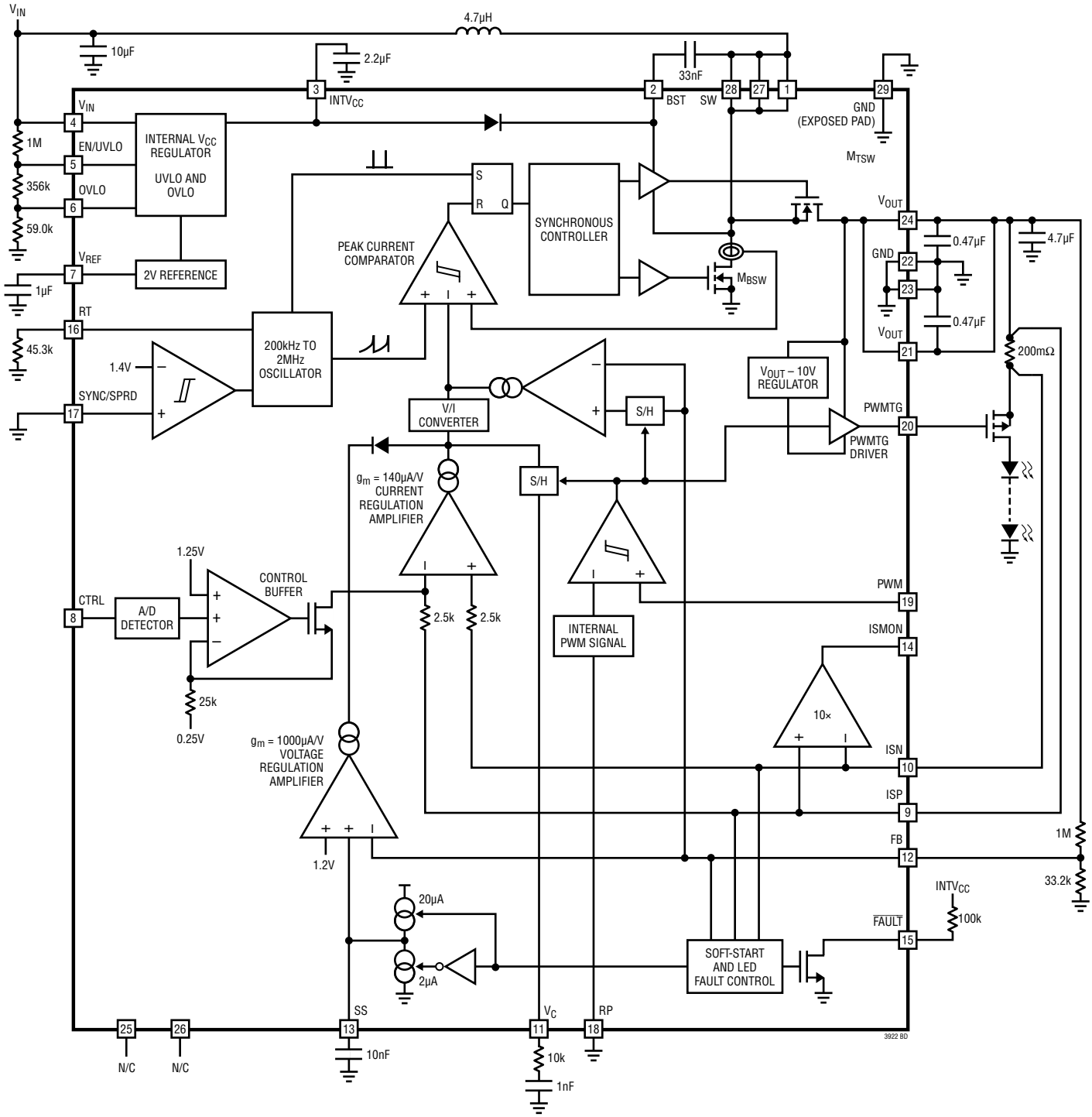
PWMTG: PWM Driver Output Pin. This pin can drive the gate of an external high-side PMOS device for PWM dimming of LEDs. Do not force any voltage on this pin.

V_{OUT}: Output Pins. Connect to the output and place output capacitors between these pins and GND as close as possible to the package. Refer to the Application Information section for the recommended capacitor placements.

GND (Pin 22, 23, Exposed Pad Pin 29): Ground Pins. All GND pins must be soldered to the board ground plane.

NC: No Connect Pins. These pins can be left open or connected to the ground.

BLOCK DIAGRAM



OPERATION

The LT3922 is a step-up LED driver that utilizes a fixed-frequency peak current control to accurately regulate the current through a string of LEDs. It includes two power switches, their drivers, and a diode for providing power to the top switch driver. The switches connect the external inductor terminal connected to the SW pin alternately to the ground and then to the output (V_{OUT}). The inductor current rises and falls accordingly and the peak current can be regulated by adjusting the duty ratio of the power switches through the combined effect of the other circuit blocks.

The synchronous controller ensures the power switches do not conduct at the same time, and a programmable oscillator turns on the bottom switch at the beginning of each switching cycle. The frequency of this oscillator is set by an external resistor at the RT pin and can be overridden by external pulses at the SYNC/SPRD pin. The SYNC/SPRD pin can also be used to command spread spectrum frequency modulation (SSFM), which reduces radiated and conducted electromagnetic interference (EMI).

The bottom switch is turned off by the peak current comparator which waits during the on-time for the increasing inductor current to exceed the target set by the voltage at the V_C pin. This target is modified by a signal from the oscillator which stabilizes the inductor current. A network of passive components at the V_C pin is necessary to stabilize this regulation loop.

The target for the inductor current is derived from the desired LED current programmed by the voltage at the CTRL pin. The analog-to-digital detector and the control buffer convert either a DC voltage or duty cycle of pulses at the CTRL pin into the input for the current regulation amplifier. The other input to this amplifier comes from the ISP and ISN pin voltages. An external current sense resistor between these pins should be placed in series with the string of LEDs such that the voltage across it provides the feedback to regulate the LED current. The current regulation amplifier then compares the actual LED current to the desired LED current and adjusts V_C as necessary.

The voltage regulation amplifier overrides the current regulation amplifier when the FB pin voltage is higher than an internal 1.2V reference. An external resistor network from the LED string to the FB pin provides an indication of the LED string voltage and allows the voltage amplifier to prevent overvoltage of the LED string.

The ISP, ISN, and FB pin voltages are also monitored to detect fault conditions like open and short circuits, which are then reported by pulling $\overline{FAULT}$ pin low. The response to a fault can be selected either to try hiccup restarts or to latchoff by the choice of an external resistor connected to the SS pin. Refer to the Applications Information section for a detailed explanation of fault responses.

Finally, pulse-width modulation (PWM) of the LED current is achieved by turning on and off an external PMOS switch between the V_{OUT} and the string of LEDs. An external pulse at the PWM pin controls the state of the PWM driver or a DC voltage at the PWM pin dictates the duty ratio of an internal PWM pulse, whose frequency is programmed with an external resistor at the RP pin. After each pulse, when the PMOS switch opens, the LT3922 preserves the voltages of the capacitors at V_C and V_{OUT} to ensure a rapid recovery for the next pulse.

APPLICATIONS INFORMATION

The following is a guide to selecting the external components and configuring the LT3922 according to the requirements of an application.

Programming LED Current with the CTRL Pin

The primary function of the LT3922 is to regulate the current in a string of LEDs. This current should pass through a series current sense resistor. The voltage across this resistor is sensed by the current regulation amplifier through the ISP and ISN pins and regulated to a level programmed by the CTRL pin. The maximum resistor voltage that can be programmed is 100mV which corresponds to 1A through the LED string when a 100mΩ current sense resistor is used.

To allow for this maximum current, the CTRL pin may be connected directly to the V_{REF} pin which provides

APPLICATIONS INFORMATION

an accurate 2V reference. Lower current levels can be programmed by DC CTRL voltages between 250mV and 1.25V as shown in Figure 1.

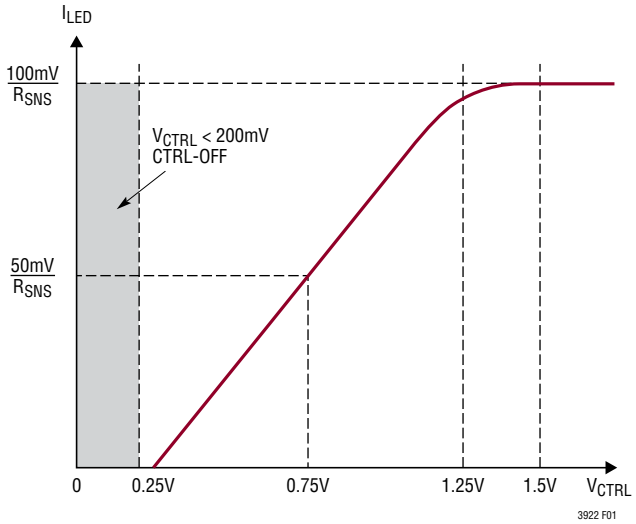


Figure 1. Analog CTRL Range

Below 250mV, the CTRL pin commands zero LED current, and above 1.25V, it commands the maximum. When an independent voltage source is not available, the intermediate CTRL voltages may be derived from the 2V reference at the V_{REF} pin using a resistor network or potentiometer as long as the total current drawn from the V_{REF} pin is less than 1mA.

Additionally, the LT3922 is capable of interpreting a digital pulse at the CTRL pin. The high level of the pulse must be greater than 1.6V. The low level must be less than 0.4V. The frequency must be greater than 10kHz and less than 200kHz. Then the regulated voltage between ISP and ISN will vary with the duty ratio of the pulse as shown in Figure 2.

In this case, the LED current is zero for duty cycles less than 12.5% and reaches its maximum above 62.5%. The LT3922 will cease switching if the duty cycle of the CTRL pin pulse is less than 10%, and also for DC CTRL pin voltages less than 200mV.

To reduce the LED current when the temperature of the LEDs rises, use resistors with negative temperature coefficient (NTC) in the network from V_{REF} to CTRL as shown in Figure 3.

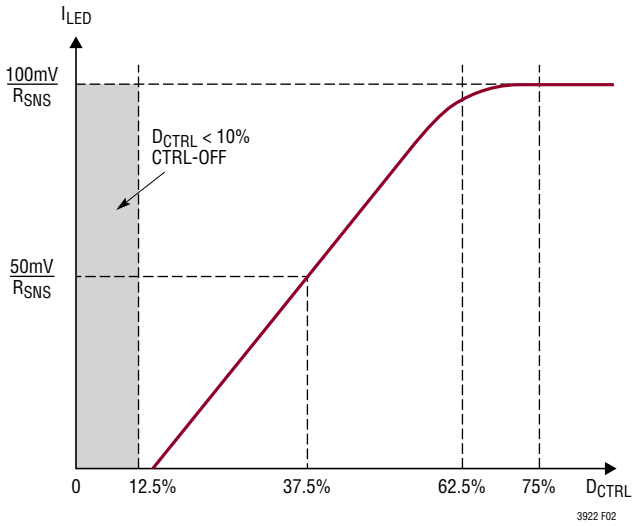


Figure 2. Duty Cycle CTRL Range

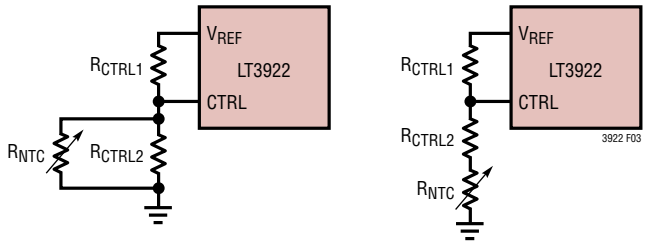


Figure 3. Setting CTRL with NTC Resistors

Setting Switching Frequency with the RT Pin

The switching frequency of the LT3922 is programmed by a resistor connected between the RT pin and GND. Values of the R_T resistor from 45.3k up to 499k program frequencies from 2MHz down to 200kHz as shown in Table 1. Higher frequencies allow for smaller external components but increase switching power losses and radiated EMI.

Table 1. R_T Resistance Range

SWITCHING FREQUENCY	R_T
2.0 MHz	45.3k
1.6 MHz	57.6k
1.2 MHz	78.7k
1.0 MHz	95.3k
400 kHz	249k
200 kHz	499k

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Synchronizing Switching Frequency

The switching frequency can also be synchronized to an external clock connected to the SYNC/SPRD pin. The high-level of the external clock must be at least 1.5V, and the frequency must be between 200kHz and 2MHz. The R_T resistor is still required in this case, and the resistance should correspond to the frequency of the external clock. If the external clock ever stops, the LT3922 will rely on the R_T resistor to set the frequency.

Enabling Spread Spectrum Frequency Modulation

Connecting SYNC/SPRD to $INTV_{CC}$ will enable spread spectrum frequency modulation (SSFM). The switching frequency will vary from the frequency set by the R_T resistor to 125% of that frequency. If neither synchronization nor SSFM is required, connect SYNC/SPRD to GND.

As shown in Figure 4, enabling SSFM can significantly attenuate the electromagnetic interference that the LT3922, like all switching regulators, emits at the switching frequency and its harmonics. This feature is designed to help devices that include the LT3922 perform better in the various standard industrial tests related to interference.

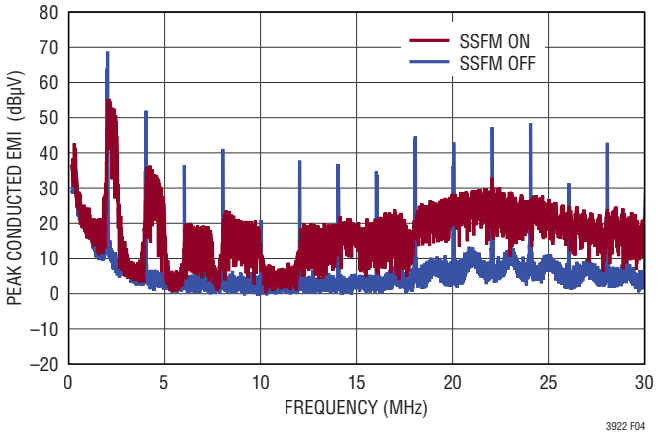

Figure 4. Typical Conducted Peak EMI of the LT3922 with 2MHz Switching Frequency

The attenuation varies depending on the chosen switching frequency, the range of frequencies in which interference is measured, and whether a test measures peak, quasi-peak, or average emissions. The results of several other emission measurements are with select typical application circuits.

Maximum Duty Cycle

The choice of switching frequency should be made knowing that the maximum V_{OUT} voltage of a boost converter is determined by the maximum duty cycle for a given V_{IN} voltage as shown in the following equation:

$$V_{OUT} = \frac{V_{IN}}{(1-D)} \quad (1)$$

where D is the duty cycle of the boost converter defined as the ratio of the on-time of the bottom power switch to the total switching period. The maximum duty cycle for a given switching frequency is determined by the minimum off-time of the bottom power switch. The longest minimum off-time of the LT3922 is 35ns, so the maximum duty cycle is 93% at 2MHz switching frequency. Therefore, if an application requires higher duty cycle, the switching frequency should be set lower to achieve the demanded duty cycle.

Selecting an Inductor

The LT3922 limits the inductor peak current to a minimum of 2A over the duty cycle without sub-harmonic oscillations. This current limit will override the CTRL input command if the programmed LED current demands higher inductor peak current than 2A. Therefore, it is important to select the inductor value to ensure the peak inductor current is below the limit over the desired input voltage range. The following is an example of inductor value decision process for the application where we want 300mA LED current at 30V output, while the input ranges from 8V to 25V and the switching frequency is 2MHz. The maximum peak inductor current can be derived by adding the half of the inductor current ripple amplitude to the average inductor current value, both values of which are determined by the input and output voltages, switching frequency, efficiency and the inductor values. Hence, the minimum inductor value L_{MIN} that ensures the peak inductor current below 2A is:

$$L_{MIN} = \frac{\left[\frac{V_{IN(MIN)} \bullet \left(V_{OUT} - V_{IN(MIN)}\right)}{2 \bullet V_{OUT} \bullet f_{SW}}\right]}{\left[2 - \frac{V_{OUT} \bullet I_{LED}}{V_{IN(MIN)} \bullet EFFICIENCY}\right]} \quad (2)$$

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Using this equation gives an inductance of about 2µH assuming 90% efficiency for the given conditions.

With this minimum inductor value guideline, choose an inductor with low core loss and low DC resistance. Inductor must be able to handle the peak inductor current without saturation. To minimize the radiated noise, use a shielded inductor. The manufacturers featured in Table 2 are recommended sources of inductors.

Table 2. Inductor Manufacturers

MANUFACTURER	WEBSITE
Wurth Electronics	www.we-online.com
Coilcraft	www.coilcraft.com
Vishay Intertechnology	www.vishay.com

Selecting an Input Capacitor

The input capacitor supplies the inductor ripple current and the transient current that occurs in PWM dimming operations. A 10µF ceramic capacitor should be sufficient to provide these non-steady state currents. Place the input capacitor close to the inductor. If possible, place an additional 1µF ceramic capacitor close to the V_{IN} pin for better noise immunity. Use X7R ceramic capacitors as they typically retain their capacitance better than other capacitor types over wide voltage and temperature ranges.

If the input power source has high impedance, or there is significant inductance due to long wires or cables, additional bulk electrolytic capacitance may be necessary. A low ESRlow ESR ceramic input capacitor combined with parasitic inductances in the current paths can form a high-Q LC tank circuit which can ring the capacitor voltage up to twice the input voltage. A higher ESR electrolytic capacitor, on the other hand, minimizes this ringing. Refer to the Linear Technology Application Note 88 for more information. Sources of quality ceramic and electrolytic capacitors are listed in Table 3.

Table 3. Capacitor Manufacturers

MANUFACTURER	WEBSITE
Murata Manufacturing	www.murata.com
Garrett Electronics	www.garrettelec.com
Panasonic	www.industrial.panasonic.com
Nippon Chemi-Con	www.chemi-con.co.jp

Stabilizing the Regulation Loop

The LT3922 uses internal error amplifiers to regulate the LED current and the output voltage to the user programmed values. The output impedance of the error amplifiers and the external compensation capacitor, C_C, connected to V_C pin create the dominant pole of the control loop. The compensation resistor, R_C, in series with C_C forms a left-half-plane (LHP) zero. This LHP zero allows better regulation of LED current and output voltage during transient operations. For most LED applications, 1nF and 10k would be good starting values for C_C and R_C, respectively. Refer to the Linear Technology Application Note 76 for more information.

Selecting and Placing Output Capacitors

The output capacitors need to have very low ESR to reduce the output ripple. Placing several low ESR ceramic capacitors in parallel is an effective way to reduce ESR. These output capacitors in a boost converter should have a ripple current rating greater than the half of the maximum SW pin current. Use X7R ceramic capacitors as they typically retain their capacitance better than other capacitor types over wide voltage and temperature ranges.

The LT3922 utilizes a proprietary architecture to reduce EMI noise generated by switching. To best utilize this feature, V_{OUT} should be bypassed with three capacitors. Figure 5 shows the V_{OUT} capacitor placements for the QFN package. C_{OUT1} and C_{OUT2} are 0402-0.47µF ceramic capacitors placed as close as possible to the LT3922's V_{OUT} and GND pins. C_{OUT3} should be larger in size and value. A 1206-4.7µF ceramic capacitor is recommended for typical applications.

APPLICATIONS INFORMATION

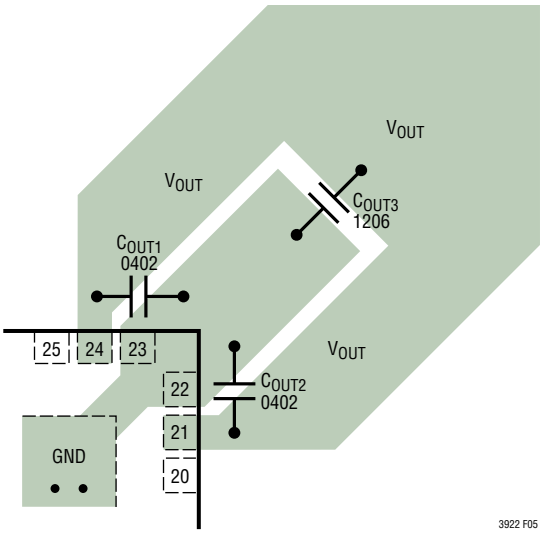

Figure 5. Placement of Output Capacitors

Selecting a MOSFET for PWM Dimming

Pulse-Width-Modulation (PWM) dimming of the LED current is an effective way to control the brightness of the light without varying its color. The brightness can also be adjusted with finer resolution this way than by varying the current level.

The LT3922 features a PWMTG driver that is intended for a high-voltage PMOS switch in position to effectively PWM dim a string of LEDs from the output capacitor and the current sense resistor. When the switch is open and the string is disconnected, the LED current will be zero. In contrast to a low-side NMOS driver, this feature eliminates the need for a dedicated return path for the LED current in automotive applications or other grounded chassis systems.

The gate driver for this PMOS is supplied through the V_{OUT} pin. When the PWM pin voltage is greater than 1.4V, the driver will pull the gate of the PMOS to a maximum of 10V below the V_{OUT} pin. If V_{OUT} is below 10V, the gate drive is necessarily reduced. For constant current applications, leave PWMTG open, connect the load directly after the current sense resistor, and connect PWM to $INTV_{CC}$. In these cases, analog dimming may be implemented with the CTRL pin.

The drain source voltage rating of the chosen PMOS should be greater than the maximum output voltage. Typically the output voltage is a little higher than the sum of the forward voltages of the LEDs in the string. However, when the string is broken, the output voltage will begin to increase due to the imbalance of inductor current and load current. As described in detail later, the LT3922 will not reduce the inductor current nor limit the output voltage until the FB pin voltage approaches 1.2V. Therefore, the maximum output voltage is ultimately determined by the resistor network between FB and V_{OUT}.

In most applications, the gate source voltage rating of the PMOS should be at least 10V. The only exceptions to this rule are applications for which the output voltage is always less than 10V. The PWMTG driver will try to pull the gate of the PMOS down to 10V below V_{OUT}, but it cannot pull the gate below GND. Therefore, when the maximum output voltage is less than 10V, the PMOS gate source voltage rating will be sufficient if it is merely equal to or greater than the output voltage.

Finally, the drain current rating of the PMOS must exceed the programmed LED current. Assuming this condition and the conditions above are met, the only electrical parameter to be considered is the on-resistance. Other parameters such as gate charge are less important because PWM dimming frequencies are typically too low for efficiency to be affected noticeably by gate charging loss or transition loss.

Table 4 lists recommended manufacturers of PMOS devices.

Table 4. PMOS Manufacturers

MANUFACTURER	WEBSITE
Infineon	www.infineon.com
Vishay Intertechnology	www.vishay.com
Fairchild Semiconductor Corp.	www.fairchildsemi.com
NXP Semiconductors	www.nxp.com

Selecting an RP Resistor for Internal PWM Dimming

If the RP pin is tied to GND, an external pulse-width modulated signal at the PWM pin will control PWM dimming of the LED load. The signal will enable the PWMTG driver and turn on the external PMOS device when it is higher than 1.4V.

APPLICATIONS INFORMATION

However, the LT3922 is capable of PWM dimming even when an external PWM signal is not available. In this case, an internal PWM signal with frequency set by a resistor at the RP pin and duty ratio set by a DC voltage at the PWM pin will control the PWMTG driver. The R_P resistor should be one of the seven values listed in Table 5. For each of these values, the PWM frequency is a unique ratio of the switching frequency.

Table 5. Internal PWM Dimming Frequencies

		SWITCHING FREQUENCY		
R_P	RATIO	2MHz	1MHz	200kHz
28.7k	2^8	7.81kHz	3.91kHz	781Hz
47.5k	2^9	3.91kHz	1.95kHz	391Hz
76.8k	2^{10}	1.95kHz	977Hz	195Hz
118k	2^{11}	977Hz	488Hz	97.7Hz
169k	2^{12}	488Hz	244Hz	48.8Hz
237k	2^{13}	244Hz	122Hz	24.4Hz
332k	2^{14}	122Hz	61Hz	12.2Hz

When using the internal PWM signal, set the voltage at the PWM pin between 1V and 2V. The PWMTG driver will stay off if PWM is below 1V, and it will stay on if PWM is above 2V. Between 1V and 2V there are 128 evenly spaced thresholds corresponding to 128 discrete PWM duty ratios from 0% to 100%. This range of 1V to 2V has been chosen so that the PWM voltage may be set using a potentiometer or a resistor network and the 2V reference available at the V_{REF} pin. Place a small 1µF ceramic capacitor near PWM pin to ground.

There are a couple of exceptions to the above rules for PWM dimming. First, once initiated, the PWM on-time will last at least four switching cycles regardless of the signal at the PWM pin and the resistor at the RP pin. This ensures that the current regulation loop has enough time to reach equilibrium but still allows for a 5000:1 dimming ratio when the external PWM frequency is 100Hz and the switching frequency is 2MHz. Second, to avoid excessive start-up times, after the first PWM pulse, PWMTG will stay on until the SS pin voltage reaches 1.7V or the LED current has reached approximately 10% of the full-scale current.

PWM Dimming with Very Long Off Times

To enhance PWM dimming, the V_{OUT} and V_C pins are driven when the PWM pulse (internal or external) is at a logic low to maintain the charge on the capacitors at those pins. Consequently, when PWM returns to a logic high state, the LED current can quickly reach the regulated level even if PWM was low for a very long time.

Monitoring LED Current

The ISMON pin provides an amplified and buffered monitor of the voltage between the ISP and ISN pins. The gain of the internal amplifier is ten, and the speed is fast enough to track the pulse-width modulated LED current. However, as shown in Figure 6, the ISMON voltage can be filtered with a resistor-capacitor network to monitor the average LED current instead.

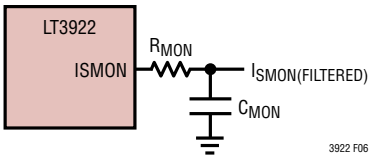

Figure 6. ISMON Filter Configuration

The resistor should be at least 10k. The capacitance can be as large or small as needed without affecting the stability of the internal amplifier. For example, when the PWM frequency is 200Hz, a 10µF capacitor combined with the 10k resistor would limit the ripple on ISMON to 1%.

Selecting the FB Resistors

Two resistors should be selected to form a network between the output voltage and the FB pin as shown in Figure 7.

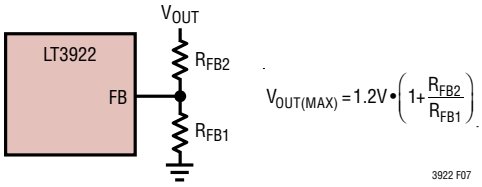

Figure 7. FB Resistor Configuration

APPLICATIONS INFORMATION

This network forms part of a voltage regulation loop when FB is near 1.2V. In this case, the LT3922 will override the programmed LED current and adjust the inductor current to lower the output voltage and limit FB to 1.2V. This resistor configuration therefore determines the maximum output voltage.

In this way, the LT3922 can also be configured as a voltage regulator instead of an LED driver. It will regulate the output voltage near the programmed maximum as long as the load current is less than the current programmed by CTRL.

Note that this voltage limit may be reached inadvertently if it is set too close to the typical output voltage and the output capacitor is too small. To avoid interference with the current regulation, the feedback resistors should be chosen such that FB is below 1.14V when the LEDs are conducting.

Understanding FB Overvoltage Lockout

Despite the voltage regulation loop, the FB voltage can temporarily exceed the 1.2V limit. If the output voltage is near the maximum when the LED string opens, it may take too long for the feedback loop to adjust the inductor current and avoid overcharging the output. To quickly respond to the overvoltage conditions, the LT3922 will immediately stop switching, disconnect the LED string by shutting the external PMOS off when the FB pin exceeds the 1.266V FB overvoltage lockout threshold.

The FB overvoltage lockout threshold may be routinely exceeded when the LT3922 is being operated as a voltage regulator if the load current decreases rapidly. In this case, the pause in switching limits the output overshoot and ensures that the voltage is back in regulation as quickly as possible. For safe operation, choose R_{FB1} and R_{FB2} values to ensure the output voltage is not greater than 40V when the FB voltage is 1.266V.

Open LED Fault Detection and Response

The resistor network formed by R_{FB1} and R_{FB2} also defines the criteria for the open-LED fault condition. An open-LED fault is detected when the FB pin voltage is greater than 1.14V and simultaneously the difference between ISP and ISN pins is less than 10mV. The latter condition ensures that the output current is low (as it should be in an open circuit) not just that output voltage is high as it may be when the LEDs are conducting a large current.

A fault is reported by an internal device pulling the voltage at the $\overline{FAULT}$ pin low. There is nothing internal that pulls this voltage high, so an external resistor between $INTV_{CC}$ and $\overline{FAULT}$ is necessary as shown in Figure 8. This configuration allows multiple $\overline{FAULT}$ pins and similar pins on other parts to be connected and share a single resistor.

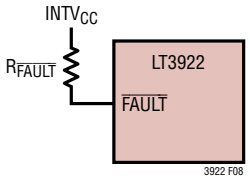

Figure 8. $\overline{FAULT}$ Resistor Configuration

Shorted LED Fault Detection and Responses

The LT3922 prevents excessive currents that could damage the LED and the driver by three detection schemes as follows:

1) $(V_{ISP} – V_{ISN}) > 150mV$ for more than 300µs, or

2) $(V_{ISP} – V_{ISN}) > 700mV$ (typical), or

3) $V_{OUT} < (V_{IN} – 2V)$

If the LT3922 detects any one of these events, it immediately stops switching, turns off the external PMOS PWM switch, pulls down $\overline{FAULT}$ pin, and initiates a fault response routine using the SS pin. Note that $\overline{FAULT}$ pin is held low until the part successfully restarts.

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Soft-Start and Fault Modes

The LT3922's soft-start (SS) pin has two functions. First, it allows the user to program the output startup voltage ramp rate through the SS pin. An internal 20µA current pulls up the SS pin to $INTV_{CC}$. As shown in Figure 9, connecting an external capacitor C_{SS} at the SS pin to GND will

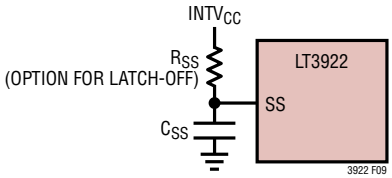


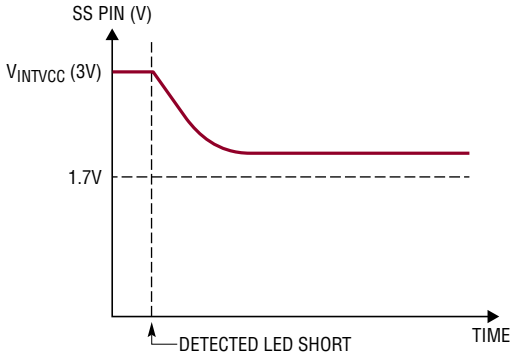
Figure 9. SS Capacitor and Resistor Configuration

generate a linear ramp voltage. This voltage ramp at the SS pin forces the LT3922 to regulate the FB pin voltage to track the SS pin voltage until V_{OUT} is high enough to drive the LED at the commanded current level.

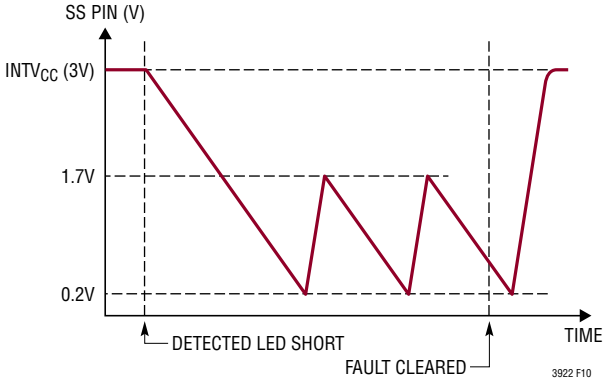
The SS pin is also used as a fault timer. After a shorted LED fault is detected, an internal 2µA current pulls down the voltage on the SS pin. The user can configure two different fault response routines by using or not using a pull-up resistor, R_{SS}, from the SS pin to $INTV_{CC}$. Figures 10a and 10b illustrate corresponding waveforms of the SS pin voltage for the two responses: latchoff and hiccup mode. With a 470k or smaller R_{SS}, the LT3922 will latch off until the user forces a reset by toggling the EN/UVLO pin. Without the R_{SS}, the LT3922 enters a hiccup mode operation. The 2µA pulls SS pin down to 0.2V, at which point the 20µA pull-up current turns on again to raise the SS pin voltage. If the fault condition has not been removed until the SS pin reaches 1.7V, the 2µA pull-down current source turns on again to start another cycle. This hiccup mode will continue until the fault is cleared. A typical C_{SS} value is 10nF.

Programming EN/UVLO and OVLO Thresholds

The LT3922 will stop switching, disable the PWMTG driver, and reset the soft-start when the voltage at the EN/UVLO pin drops below 1.33V, or the voltage at the OVLO pin rises above 1.205V. External voltage sources can be used to set the voltage at EN/UVLO and OVLO pins to enable



(a) Latchoff Mode



(b) Hiccup Mode

Figure 10. Fault Responses: (a) Latchoff and (b) Hiccup

or disable the LT3922. Alternatively, resistor networks can be placed from V_{IN} to these pins to set the operating range of V_{IN} voltage.

For instance, the V_{IN} undervoltage lockout (UVLO) threshold can be accurately set by an external resistor divider. Figure 11 illustrates how to set the falling EN/UVLO threshold and the rising hysteresis voltages in LT3922. The internal hysteresis is 25mV, but the user can program

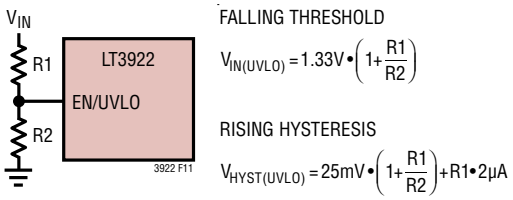


Figure 11. EN/UVLO Threshold and Hysteresis Voltages

APPLICATIONS INFORMATION

additional hysteresis through the external resistor as the EN/UVLO pin sinks 2µA current when the EN/UVLO pin voltage is below the threshold.

On the other hand, the V_{IN} overvoltage lockout (OVLO) threshold can be accurately set by the external resistor divider as well. Figure 12 illustrates how to set the rising OVLO threshold in LT3922. The internal hysteresis of the OVLO pin is 50mV.

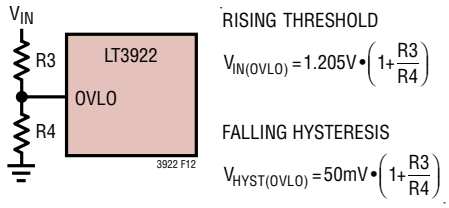


Figure 12. OVLO Threshold and Hysteresis Voltages

Both EN/UVLO and OVLO can be set precisely using a single resistor string consisting of three series resistors. Figure 13 shows the resistor string and the threshold and hysteresis voltages for EN/UVLO and OVLO.

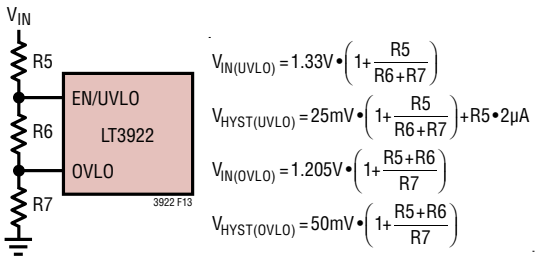


Figure 13. EN/UVLO–OVLO Threshold and Hysteresis Voltages

Tie EN/UVLO to V_{IN} and tie OVLO to GND if they are not used. Do not leave these pins open.

Planning for Thermal Shutdown

The LT3922 automatically stops switching when the internal temperature is too high. The temperature limit is guaranteed to be higher than the operational temperature of the part. During thermal shutdown, all switching is terminated, SS is forced low, and the LEDs are disconnected through the PWMTG driver.

The exposed pad on the bottom of the package must be soldered to a ground plane. Vias placed directly under the package are necessary to dissipate heat.

Designing the Printed Circuit Board (PCB)

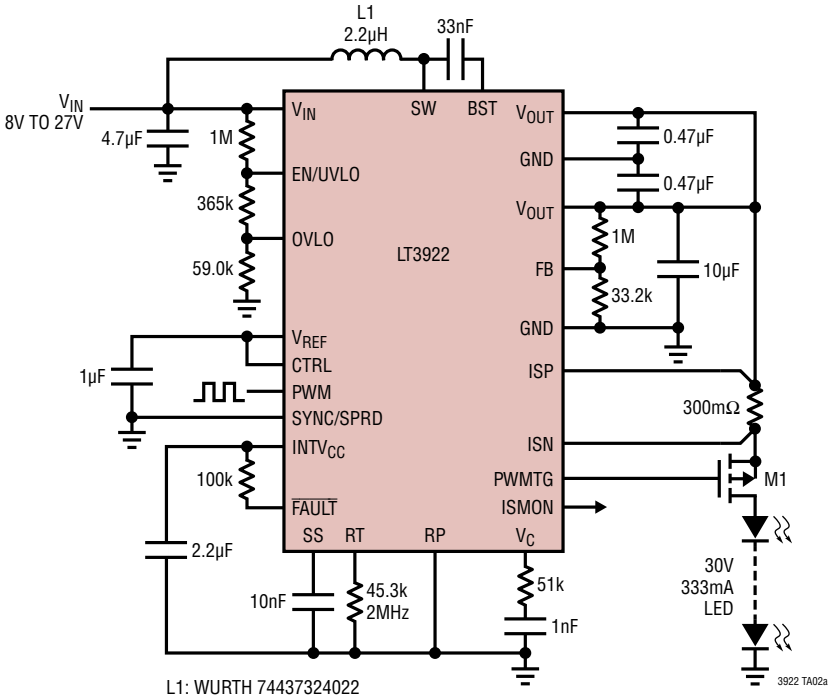
The output capacitors C_{OUT1} and C_{OUT2} of the LT3922 bypass large switched currents from V_{OUT} to GND (see Figure 5). The loops travelled by these currents should be made small as possible to these pins. These output capacitors, along with the inductor and the input capacitors, should be placed on the same side of the PCB, and their connections should be made on that layer.

Create a Kelvin ground network by keeping the ground connection for all of the other components separate. It should only join the ground for the input and output capacitors and the return path for the LED current at the exposed pad.

There are a few other aspects of the board design that improve performance. An unbroken ground plane on the second layer dissipates heat, but also reduces noise. Likewise minimizing the area of the SW and BST nodes reduces noise. The traces for FB and V_C should be kept short to lessen the susceptibility to noise of these high-impedance nodes. Matched Kelvin connections from the external current sense resistor to the ISP and ISN pins are essential for current regulation accuracy. The 2.2µF $INTV_{CC}$ and 1µF V_{REF} capacitors as well as the 33nF BST capacitor should be placed as closely as possible to their respective pins. Use bypass capacitors for the DC input nodes such as V_{IN}, CTRL, and PWM (for internal PWM) to reduce noise. Keep the RT and RP nodes small and away from noisy signals. Finally, a diode with anode connected to ground and cathode to the drain of the PWMTG MOSFET can protect that device from overvoltage caused by excessive inductance in the LED string. Please refer to the demo board layout of the LT3922 for more information.

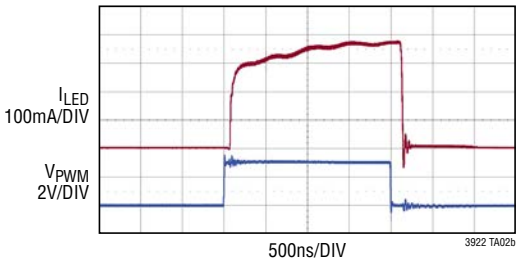
TYPICAL APPLICATIONS

333mA Boost LED Driver Using External PWM and Strobe



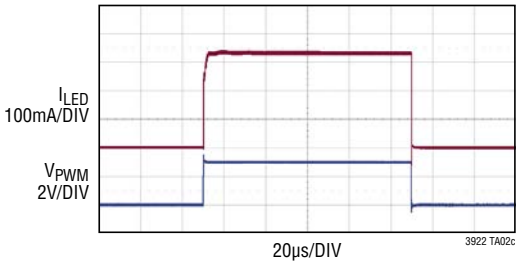
L1: WURTH 74437324022
M1: VISHAY Si2319CDS

5000:1 External PWM Dimming



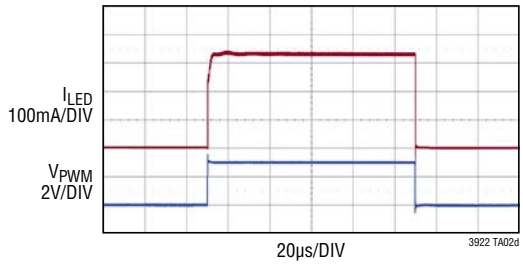
INFINITE PERSISTENCE
V_{IN} = 18V
f_{PWM} = 100Hz

100:1 External PWM Dimming



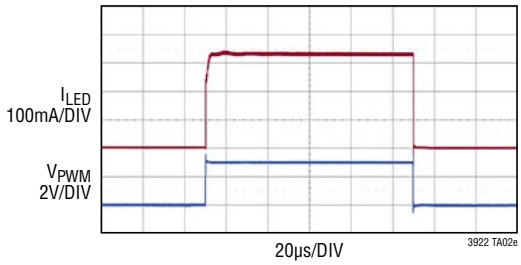
INFINITE PERSISTENCE
V_{IN} = 18V
f_{PWM} = 100Hz

100µs Strobe/1s Period



INFINITE PERSISTENCE
V_{IN} = 18V
f_{PWM} = 1Hz

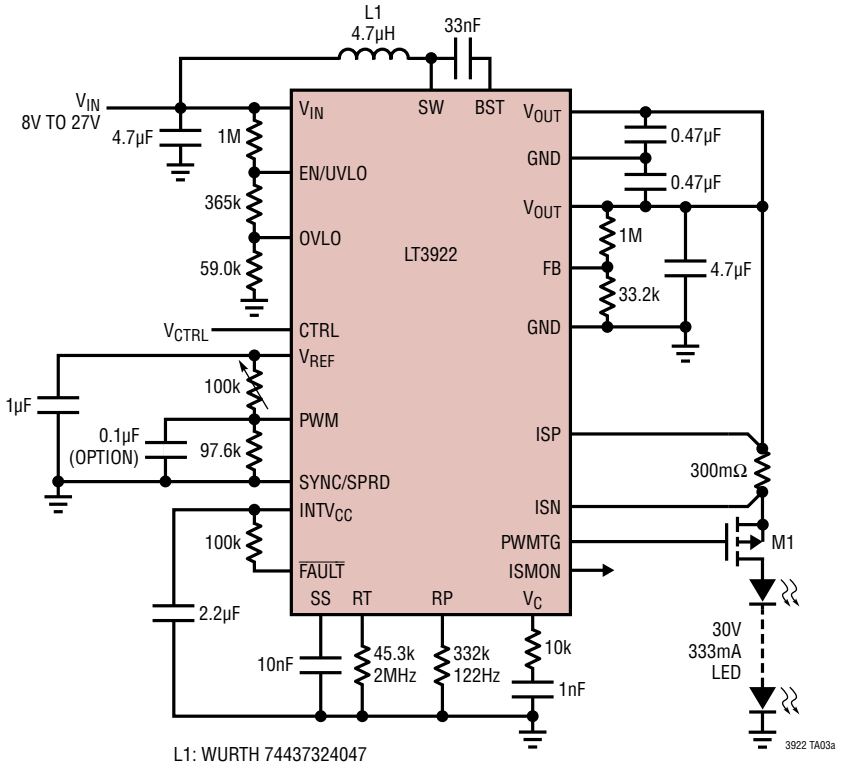
100µs Strobe/100s Period



INFINITE PERSISTENCE
V_{IN} = 18V
f_{PWM} = 0.01Hz

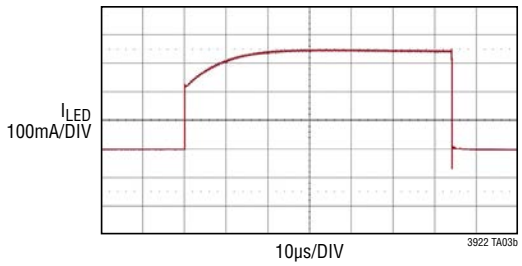
TYPICAL APPLICATIONS

333mA Boost LED Driver Using Internal PWM and Analog CTRL Dimming



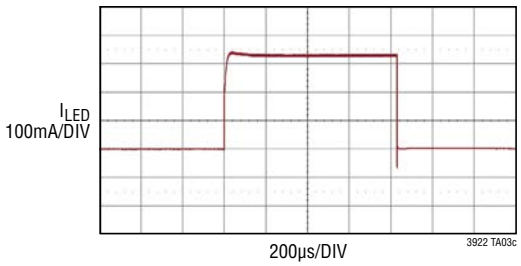
L1: WURTH 74437324047
M1: VISHAY Si2319CDS

128:1 Internal PWM Dimming



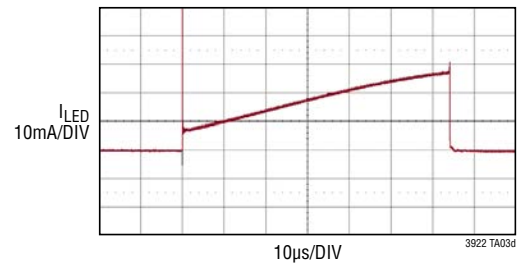
V_{CTRL} = 2V
V_{IN} = 12V
f_{PWM} = 122Hz

10:1 Internal PWM Dimming



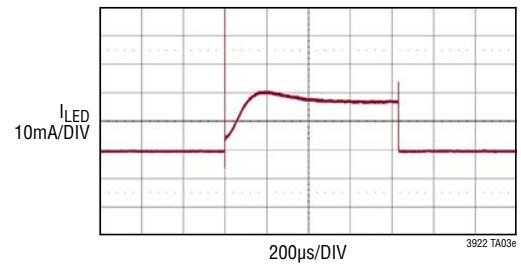
V_{CTRL} = 2V
V_{IN} = 12V
f_{PWM} = 122Hz

128:1 Internal PWM with 20:1 Analog CTRL Dimming



V_{CTRL} = 0.3V
V_{IN} = 12V
f_{PWM} = 122Hz

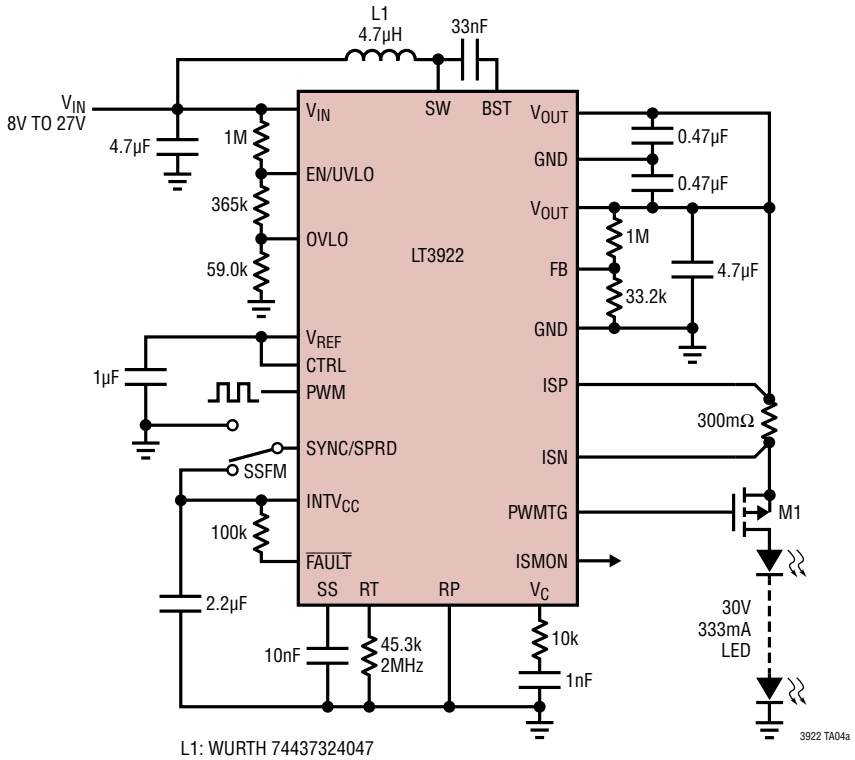
10:1 Internal PWM with 20:1 Analog CTRL Dimming



V_{CTRL} = 0.3V
V_{IN} = 12V
f_{PWM} = 122Hz

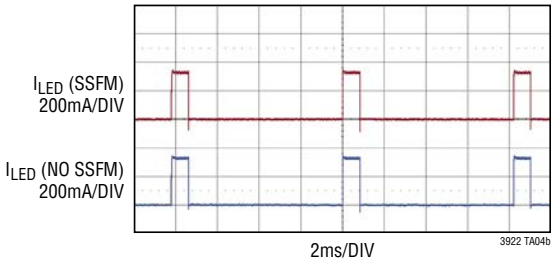
TYPICAL APPLICATIONS

333mA Boost LED Driver Using External PWM Dimming and SSFM



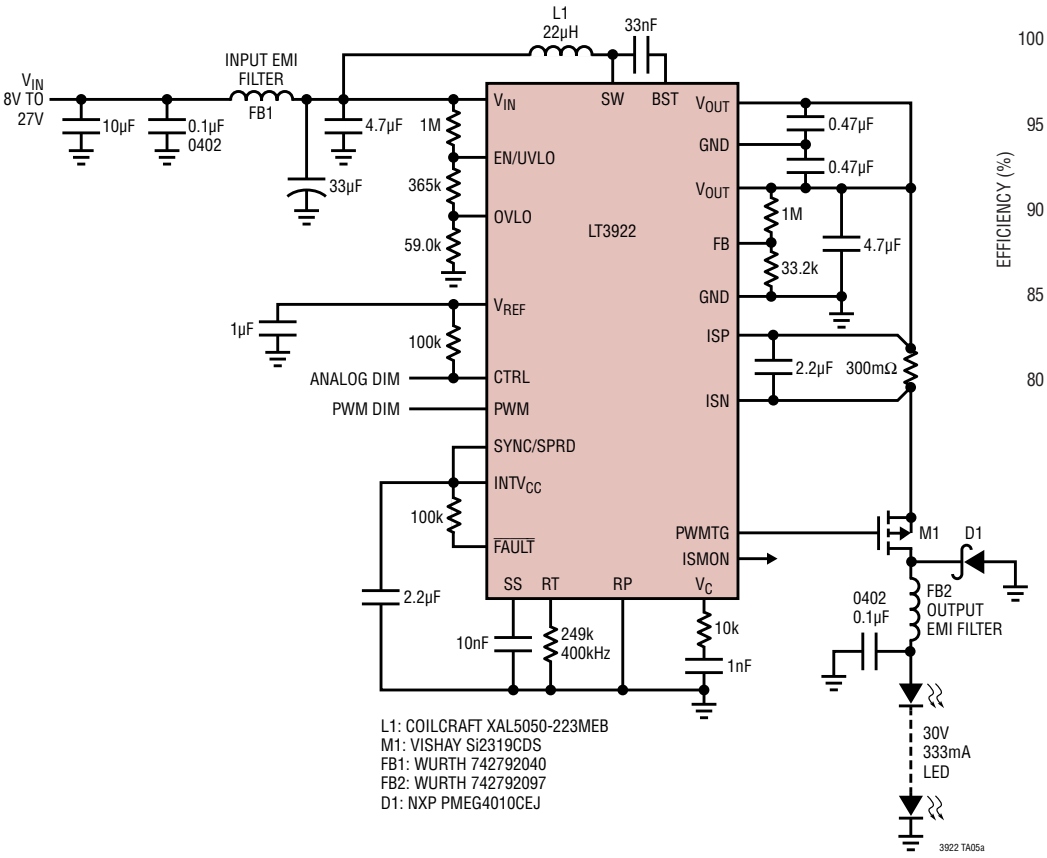
L1: WURTH 74437324047
M1: VISHAY Si2319CDS

122Hz 10:1 External PWM Dimming with and without SSFM

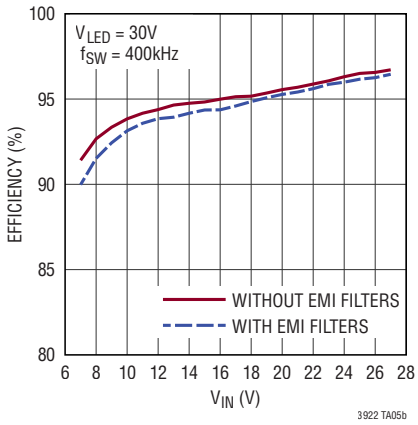


TYPICAL APPLICATIONS

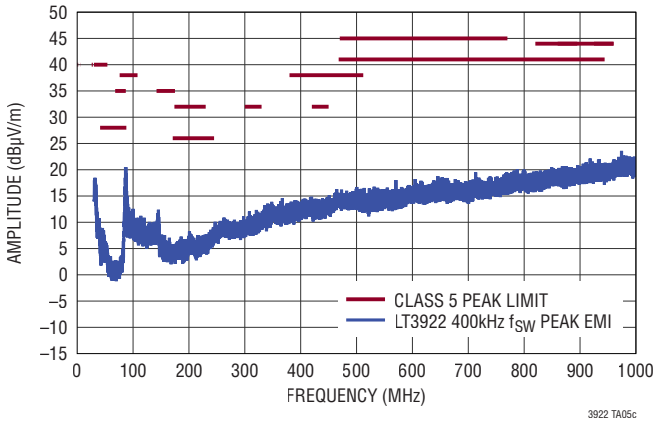
Low EMI 400kHz, 96% Efficient 10W (30V, 333mA) Boost LED Driver with SSFM



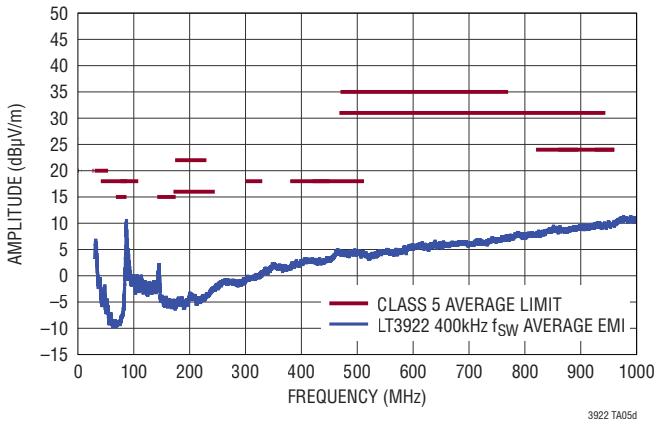
Efficiency vs V_{IN}



Peak Radiated EMI Performance (CISPR25)

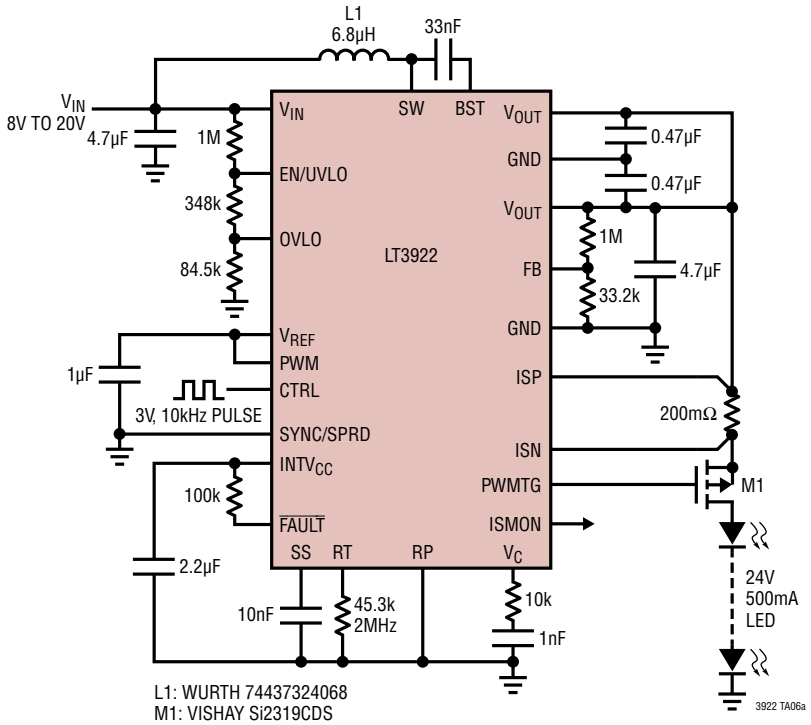


Average Radiated EMI Performance (CISPR25)

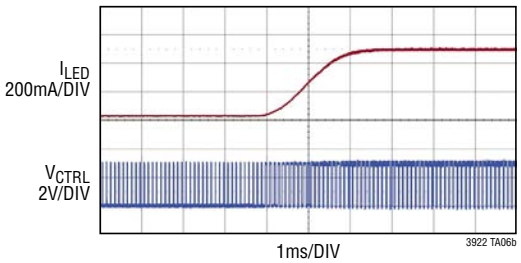


TYPICAL APPLICATIONS

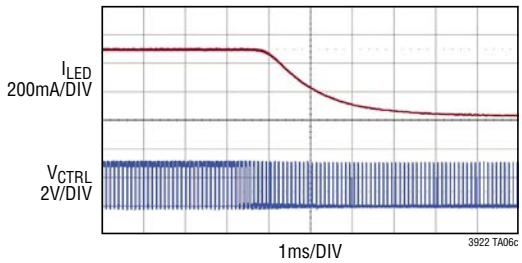
500mA Boost LED Driver Using Pulse Duty Cycle CTRL Input



V_{CTRL} Duty Cycle Stepped from 15% to 75%

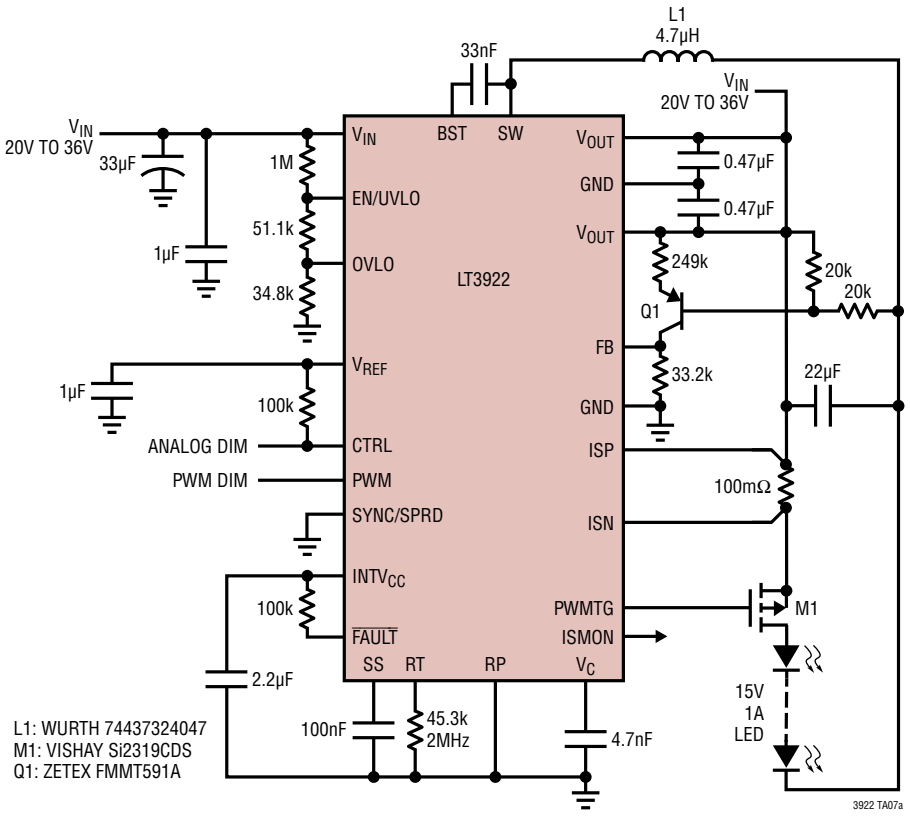


V_{CTRL} Duty Cycle Stepped from 75% to 15%

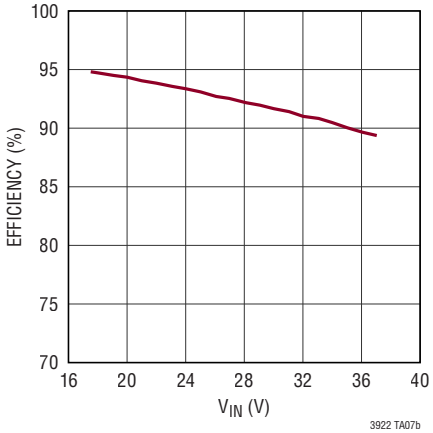


TYPICAL APPLICATIONS

2MHz, 95% Efficient 15W (15V, 1A) Buck Mode LED Driver

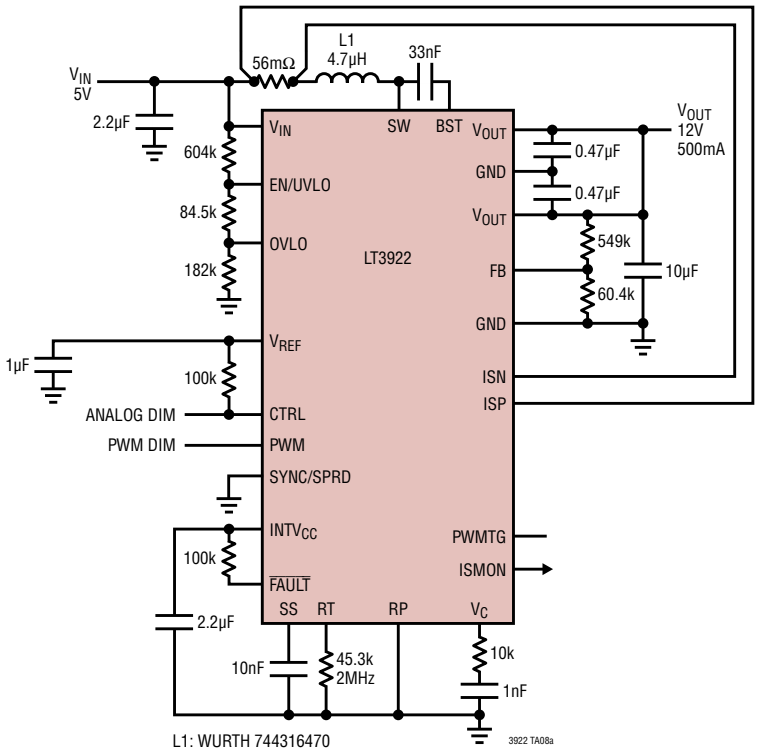


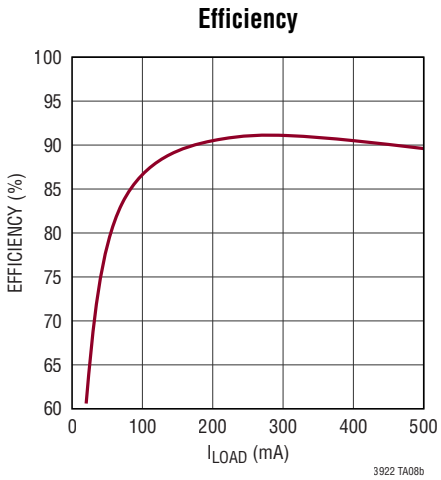
Efficiency vs V_{IN}



TYPICAL APPLICATIONS

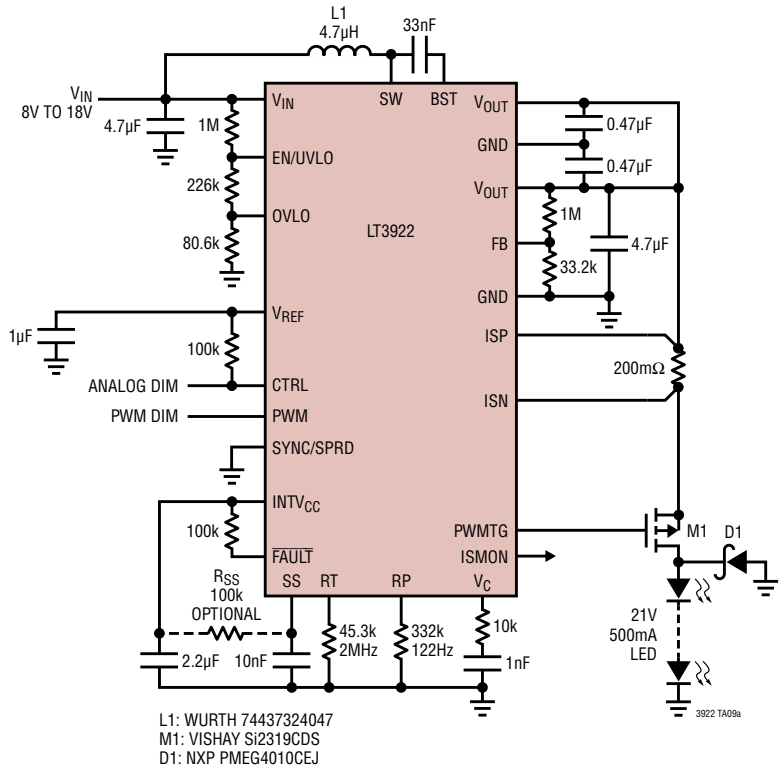
500mA, 5V to 12V Boost Converter with Accurate Input Current Limit





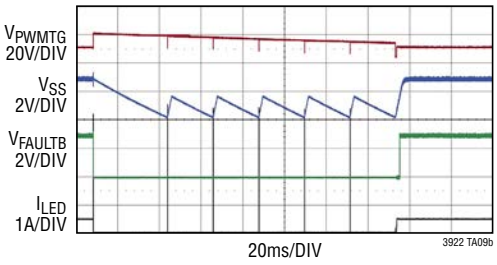
TYPICAL APPLICATIONS

Short-LED Robust Boost LED Driver

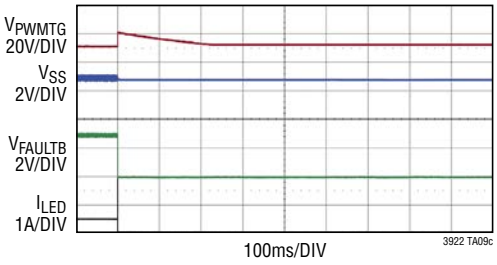


L1: WURTH 74437324047
M1: VISHAY Si2319CDS
D1: NXP PMEG4010CEJ

Shorted LED Protection without R_{SS}: Hiccup Mode

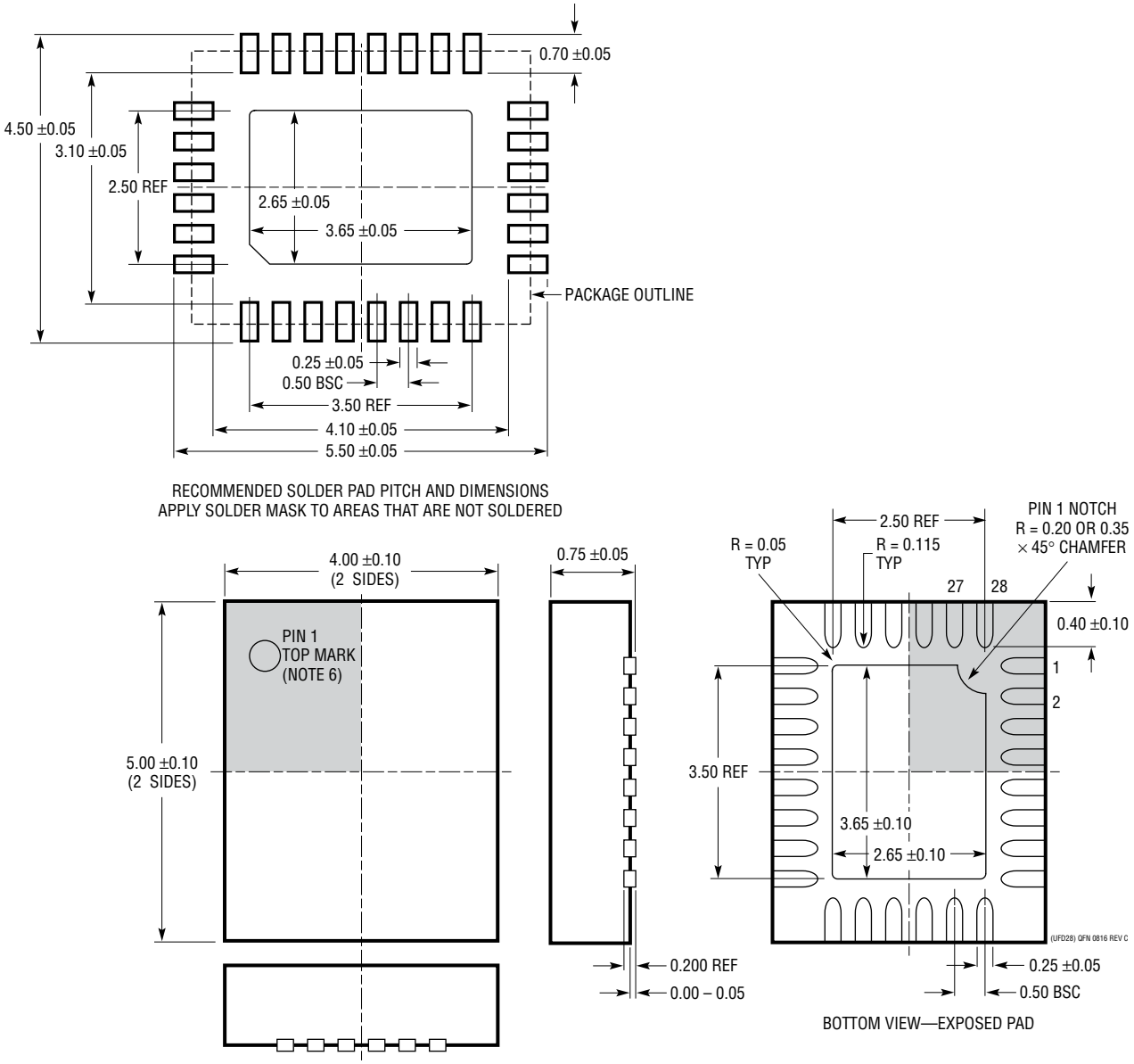


Shorted LED Protection with R_{SS}: Latchoff Mode



PACKAGE DESCRIPTION

UFD Package
28-Lead Plastic QFN (4mm × 5mm)
(Reference LTC DWG # 05-08-1712 Rev C)



NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGHD-3).
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	01/17	Revised Description	1
		Revised Electrical Characteristic values	3
		Revised Typical Performance Characteristics titles	6, 7, 9
		Revised Pin Functions description	11
		Revised Block Diagram	12
		Revised Operation description	13
		Revised Application Information description	15, 19
		Updated the Typical Application data	32
B	02/21	Updated LED current regulation to 2.5% accuracy	1
		Changed BST pin capacitor to 33nF	10, 12, 21-29, 32
		Clarified Absolute Maximum Ratings	2
		Clarified V_{REF} Voltage conditions	3
		Revised Electrical Characteristic values	3-4