36V, 2A Synchronous Buck-Boost Converter and LED Driver

FEATURES

- **4-Switch Single Inductor Architecture Allows V_{IN} Above, Below or Equal to V_{OUT}**
- **Constant Voltage and Constant Current Regulation**
- **Proprietary Peak-Buck Peak-Boost Current Mode**
- **3V to 36V Input Voltage Range**
- **0V to 36V Output Voltage Range**
- **±1.5% Output Voltage Regulation**
- **±3% Output Current Regulation**
- 5000:1 External and 128:1 Internal PWM Dimming
- Open and Short LED Protection with Fault Reporting
- 300kHz to 2MHz Fixed Switching Frequency with External Frequency Synchronization
- Flicker-Free Spread Spectrum for Low EMI
- Available in 28-Lead QFN (4mm × 5mm)
- AEC-Q100 Qualified for Automotive Applications

APPLICATIONS

- Voltage Regulator with Accurate Current Limit
- General Purpose LED Driver
- Automotive and Industrial Lighting

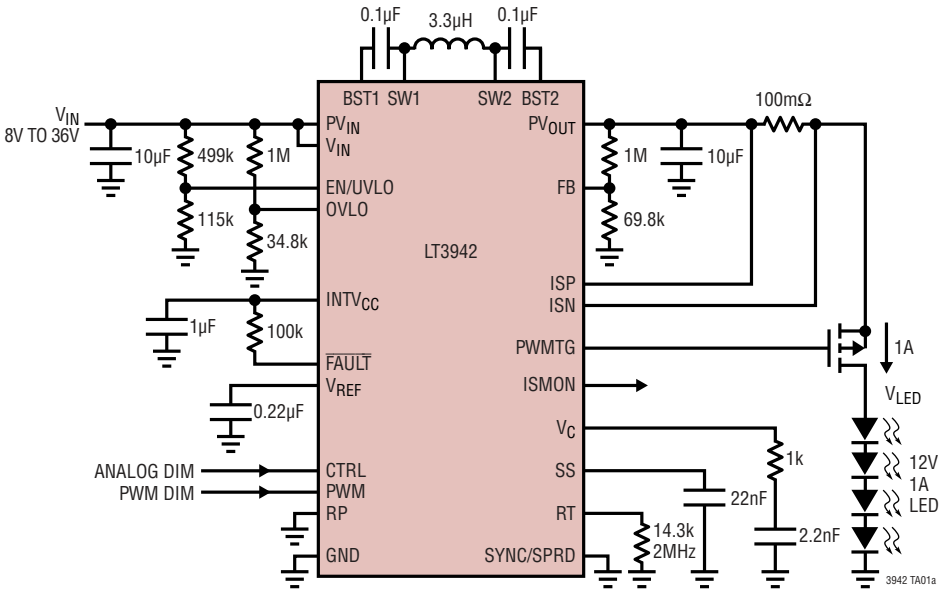
DESCRIPTION

The LT®3942 is a monolithic 4-switch synchronous buck-boost converter with constant voltage and constant current regulation, suitable for both voltage regulator and LED driver applications. The part can regulate the output voltage, or input/output current with input voltages above, below, or equal to the output voltage. The proprietary peak-buck peak-boost current mode control scheme allows adjustable and synchronizable 300kHz to 2MHz fixed frequency operation, or internal 25% triangle spread spectrum operation for low EMI. The LT3942 covers 3V to 36V input and 0V to 36V output with seamless low-noise mode transition.

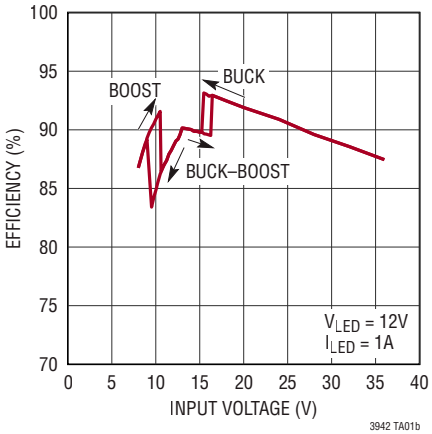
For voltage regulator applications, the LT3942 provides input or output current monitor. For LED driver applications, it provides current regulation with up to 128:1 internal and 5000:1 external PWM dimming using an optional high-side PMOS switch. Fault protection is also provided to detect output short-circuit condition and open or short LED condition.

TYPICAL APPLICATION

93% Efficient, 12W (12V, 1A) 2MHz Buck-Boost LED Driver



Efficiency vs V_{IN}



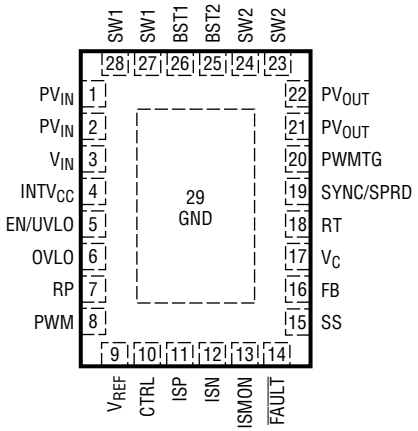
ABSOLUTE MAXIMUM RATINGS

(Note 1)

PV_{IN}, V_{IN}, EN/UVLO 40V
PV_{OUT}, ISP, ISN 40V
SW1, SW2.....40V
BST1, BST2.....45V
BST1–SW1, BST2–SW2, $INTV_{CC}$ 5V
OVLO, CTRL, FB, PWM, SYNC/SPRD, $\overline{FAULT}$ 5V
ISP–ISN .....–1V to 1V
Operating Junction Temperature (Notes 2, 3)
LT3942E ..... –40°C to 125°C
LT3942J/LT3942H ..... –40°C to 150°C
Storage Temperature Range ..... –65°C to 150°C

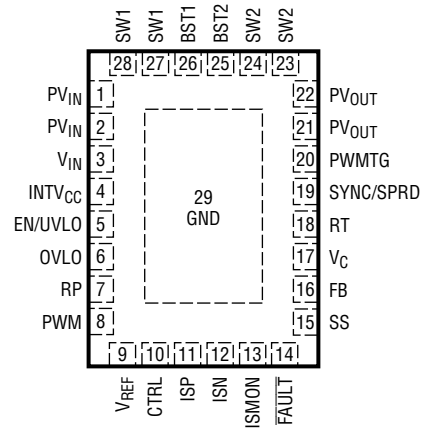
PIN CONFIGURATION

TOP VIEW



UFD PACKAGE
28-LEAD (4mm × 5mm) PLASTIC QFN
θ_{JA} = 43°C/W, θ_{JC} = 3.4°C/W
EXPOSED PAD (PIN 29) IS GND, MUST BE SOLDERED TO PCB

TOP VIEW



UFDM PACKAGE
28-LEAD (4mm × 5mm) PLASTIC SIDE WETTABLE QFN
θ_{JA} = 43°C/W, θ_{JC} = 3.4°C/W
EXPOSED PAD (PIN 29) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3942EUFD#PBF	LT3942EUFD#TRPBF	3942	28-Lead (4mm x 5mm) Plastic QFN	–40°C to 125°C
LT3942JUFD#PBF	LT3942JUFD#TRPBF	3942	28-Lead (4mm x 5mm) Plastic QFN	–40°C to 150°C
LT3942HUFD#PBF	LT3942HUFD#TRPBF	3942	28-Lead (4mm x 5mm) Plastic QFN	–40°C to 150°C
AUTOMOTIVE PRODUCTS**				
LT3942JUFDM#WPBF	LT3942JUFDM#WTRPBF	3942	28-Lead (4mm x 5mm) Plastic Side Solderable QFN	–40°C to 150°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

**Versions of this part are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. These models are designated with a #W suffix. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. PV_{IN} = V_{IN} = 12V, $V_{EN/UVLO}$ = V_{IN} unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input and Output						
PV_{IN}/V_{IN} Operating Voltage Range		●	3		36	V
PV_{IN}/V_{IN} Quiescent Current	$V_{EN/UVLO}$ = 0.3V $V_{EN/UVLO}$ = 1.3V, Not Switching			0.9 2.6	2 4	µA mA
PV_{OUT} Operating Voltage Range		●	0		36	V
PV_{OUT} Quiescent Current	$V_{EN/UVLO}$ = 0.3V, PV_{OUT} = 12V $V_{EN/UVLO}$ = 1.3V, PV_{OUT} = 12V, Not Switching		 20	0.1 40	0.5 60	µA µA
EN/UVLO Shutdown Threshold		●	0.3	0.6	0.9	V
EN/UVLO Enable Threshold	Falling	●	1.196	1.220	1.244	V
EN/UVLO Enable Hysteresis				15		mV
EN/UVLO Hysteresis Current	$V_{EN/UVLO}$ = 0.3V $V_{EN/UVLO}$ = 1.1V $V_{EN/UVLO}$ = 1.3V		–0.1 2.2 –0.1	0 2.5 0	0.1 2.8 0.1	µA µA µA
OVLO Threshold	Rising		1.196	1.220	1.244	V
OVLO Hysteresis				35		mV
Linear Regulators						
$INTV_{CC}$ Regulation Voltage	I_{INTVCC} = 10mA		3.5	3.65	3.8	V
$INTV_{CC}$ Load Regulation	I_{INTVCC} = 0mA to 30mA			0.8	2	%
$INTV_{CC}$ Line Regulation	I_{INTVCC} = 10mA, V_{IN} = 4V to 36V			0.1	0.5	%
$INTV_{CC}$ Current Limit	V_{INTVCC} = 3V			40		mA
$INTV_{CC}$ Dropout Voltage (V_{IN} – $INTV_{CC}$)	I_{INTVCC} = 10mA, V_{IN} = 3.3V			120	200	mV
$INTV_{CC}$ UVLO Threshold	Falling		2.27	2.37	2.47	V
$INTV_{CC}$ UVLO Hysteresis				120		mV
V_{REF} Regulation Voltage	I_{VREF} = 100µA	●	1.97	2.00	2.03	V
V_{REF} Load Regulation	I_{VREF} = 0mA to 1mA			0.5	1	%
V_{REF} Line Regulation	I_{VREF} = 100µA, V_{IN} = 4V to 36V			0.1	0.5	%
V_{REF} Current Limit	V_{REF} = 1.8V			2.5		mA
V_{REF} UVLO Threshold	Falling		1.78	1.84	1.90	V
V_{REF} UVLO Hysteresis				45		mV
Current Regulation Loop						
CTRL Pin Current	V_{CTRL} = 0.75V, Current Out of Pin		0	13	50	nA
CTRL Dim-Off Threshold	Falling	●	190	200	210	mV
CTRL Dim-Off Hysteresis				25		mV
Full Scale LED Current Regulation $V_{(ISP-ISN)}$	V_{CTRL} = 2V, V_{ISP} = 12V V_{CTRL} = 2V, V_{ISP} = 0V	● ●	97 97	100 100	103 103	mV mV
1/2 LED Current Regulation $V_{(ISP-ISN)}$	V_{CTRL} = 0.75V, V_{ISP} = 12V V_{CTRL} = 0.75V, V_{ISP} = 0V	● ●	47.5 47.5	50 50	52.5 52.5	mV mV
1/20th LED Current Regulation $V_{(ISP-ISN)}$	V_{CTRL} = 0.30V, V_{ISP} = 12V V_{CTRL} = 0.30V, V_{ISP} = 0V	● ●	3 3	5 5	7 7	mV mV
ISP Pin Current	V_{PWM} = 5V, V_{ISP} = V_{ISN} = 12V V_{PWM} = 5V, V_{ISP} = V_{ISN} = 0V $V_{EN/UVLO}$ = 0V, V_{ISP} = V_{ISN} = 12V or 0V		 –0.1	23 –10 0	 0.1	µA µA µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. PV_{IN} = V_{IN} = 12V, $V_{EN/UVLO}$ = V_{IN} unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
ISN Pin Current	V_{PWM} = 5V, V_{ISP} = V_{ISN} = 12V V_{PWM} = 5V, V_{ISP} = V_{ISN} = 0V $V_{EN/UVLO}$ = 0V, V_{ISP} = V_{ISN} = 12V or 0V		 –0.1	23 –10 0	 0.1	µA µA µA
ISP/ISN Input Common Mode Range		●	0		36	V
ISP/ISN Low Side to High Side Switchover Voltage	V_{ISP} = V_{ISN}			1.7		V
ISP/ISN High Side to Low Side Switchover Voltage	V_{ISP} = V_{ISN}			1.6		V
LED Current Regulation Amplifier g_m				2000		µS
Voltage Regulation Loop						
FB Pin Current	FB in Regulation, Current Out of Pin			17	40	nA
FB Regulation Voltage	V_C = 0.8V	●	0.985	1.00	1.015	V
FB Line Regulation	V_{IN} = 3V to 36V			0.02	0.1	%
FB Load Regulation				0.02	0.1	%
FB Voltage Regulation Amplifier g_m				650		µS
V_C Output Impedance				10		MΩ
V_C Standby Leakage Current	V_C = 1V, PWM dimming off		–20	0	20	nA
Power Switches						
Maximum Switch Current Limit	Peak-Buck Current Mode Peak-Boost Current Mode		2.2 2.2	2.5 2.5	2.8 2.8	A A
Switch A On-Resistance (From PV_{IN} to SW1)	I_{SW} = 1A			150		mΩ
Switch B On-Resistance (From SW1 to GND)	I_{SW} = 1A			150		mΩ
Switch C On-Resistance (From SW2 to GND)	I_{SW} = 1A			150		mΩ
Switch D On-Resistance (From PV_{OUT} to SW2)	I_{SW} = 1A			150		mΩ
Oscillator						
Switching Frequency	$V_{SYNC/SPRD}$ = 0V, R_T = 14.3kΩ $V_{SYNC/SPRD}$ = 0V, R_T = 43.2kΩ $V_{SYNC/SPRD}$ = 0V, R_T = 178kΩ	●	1900 925 275	2000 1000 300	2100 1075 325	kHz kHz kHz
SYNC/SPRD Pin Current	$V_{SYNC/SPRD}$ = 3.6V		–0.1	0	0.1	µA
SYNC Frequency			300		2000	kHz
SYNC/SPRD Threshold Voltage			0.4		1.5	V
Highest Spread Spectrum Above Oscillator Frequency	$V_{SYNC/SPRD}$ = 3.6V		19	22	25	%
Fault						
FB Overvoltage Threshold (V_{FB})	Rising	●	1.03	1.05	1.07	V
FB Overvoltage Hysteresis		●	20	25	30	mV
FB Open LED Threshold (V_{FB})	Rising, $V_{(ISP-ISN)}$ = 0V	●	0.93	0.95	0.97	V
FB Open LED Hysteresis	$V_{(ISP-ISN)}$ = 0V	●	40	50	60	mV
FB Short LED Threshold (V_{FB})	Falling	●	0.23	0.25	0.27	V
FB Short LED Hysteresis		●	40	50	60	mV
ISP/ISN Over Current Threshold $V_{(ISP-ISN)}$	V_{ISP} = 12V			700		mV
ISP/ISN Open LED Threshold $V_{(ISP-ISN)}$	Falling, V_{FB} = 1.0V		8	11	14	mV
ISP/ISN Open LED Hysteresis	V_{FB} = 1.0V			3		mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. PV_{IN} = V_{IN} = 12V, $V_{EN/UVLO}$ = V_{IN} unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$\overline{FAULT}$ Pull-Down Resistance				130	200	Ω
SS Hard Pull-Down Resistance				130	200	Ω
SS Pull-Up Current	V_{FB} = 0.8V, V_{SS} = 0V		11	12.5	14	µA
SS Pull-Down Current	V_{FB} = 1.0V, V_{SS} = 2V		1.1	1.25	1.4	µA
SS Fault Latch-Off Threshold				1.75		V
SS Fault Reset Threshold				0.2		V
Output Current Monitor						
ISMON Voltage	$V_{(ISP-ISN)}$ = 100mV, V_{ISP} = 12V/0V $V_{(ISP-ISN)}$ = 10mV, V_{ISP} = 12V/0V $V_{(ISP-ISN)}$ = 0mV, V_{ISP} = 12V/0V		1.22 0.32 0.22	1.25 0.35 0.25	1.28 0.38 0.28	V V V
PWM Dimming						
External PWM Dimming Threshold	Rising, RP = 10kΩ		1.3	1.4	1.5	V
External PWM Dimming Hysteresis				200		mV
Internal PWM Dimming Duty Cycle	V_{PWM} = 1V, RP ≥ 28.7kΩ V_{PWM} = 1.5V, RP ≥ 28.7kΩ V_{PWM} = 2V, RP ≥ 28.7kΩ		 47 97		3 53 	% % %
Switching Frequency to Internal PWM Dimming Frequency Ratio	RP = 28.7kΩ RP = 332kΩ			256 16384		
Minimum V_{OUT} for PWMTG to be On	PWM Dimming On			3	4.0	V
PWMTG On Voltage $V_{(VOUT-PWMTG)}$	V_{OUT} = 12V		4.6	5	5.4	V
PWMTG Off Voltage $V_{(VOUT-PWMTG)}$	V_{OUT} = 12V		–0.1	0	0.1	V
PWM to PWMTG Turn On Propagation Delay PWM to PWMTG Turn Off Propagation Delay	C_{PWMTG} = 3.3nF to V_{OUT}, 50% to 50% C_{PWMTG} = 3.3nF to V_{OUT}, 50% to 50%			130 120		ns ns

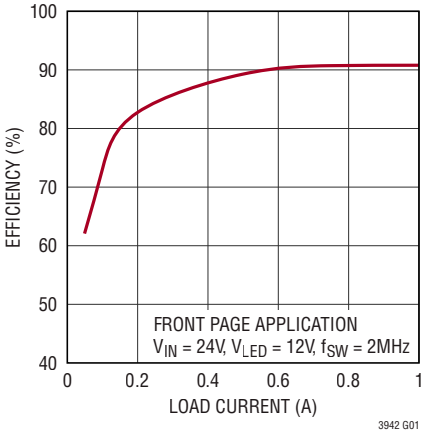
Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LT3942E is guaranteed to meet performance specifications from 0°C to 125°C operating junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT3942J and LT3942H are guaranteed over the –40°C to 150°C operating junction temperature range.

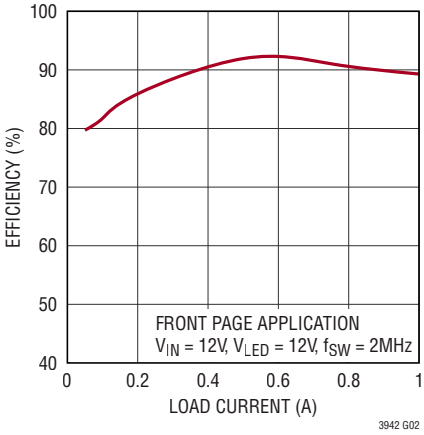
Note 3: The LT3942 includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 150°C when overtemperature protection is active. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability or permanently damage the device.

TYPICAL PERFORMANCE CHARACTERISTICS

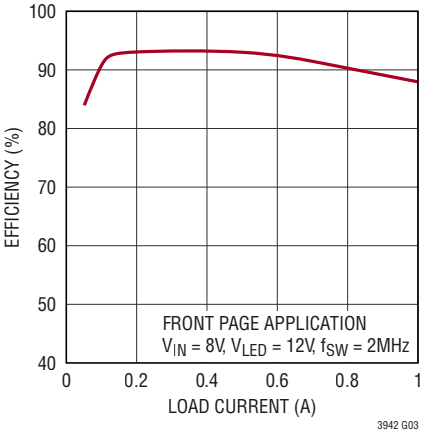
Efficiency vs LED Current (Buck Region)



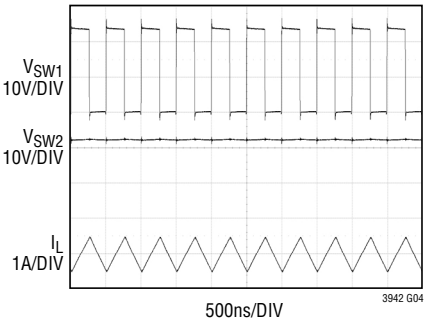
Efficiency vs LED Current (Buck-Boost Region)



Efficiency vs LED Current (Boost Region)

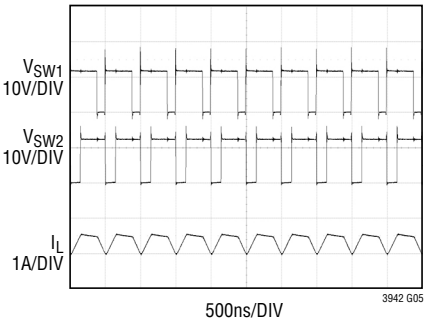


Switching Waveforms (Buck Region)



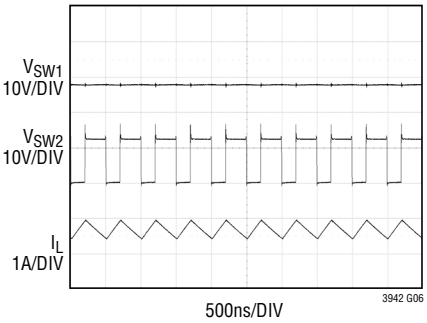
FRONT PAGE APPLICATION
V_{IN} = 24V, I_{LED} = 1A

Switching Waveforms (Buck-Boost Region)



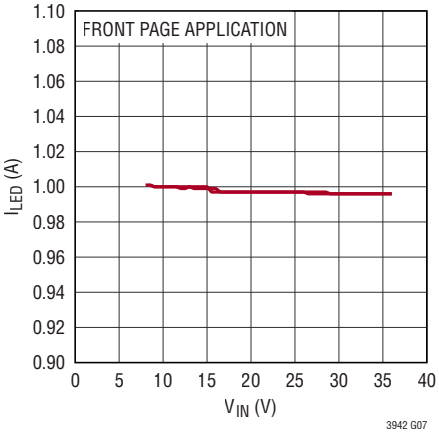
FRONT PAGE APPLICATION
V_{IN} = 12V, I_{LED} = 1A

Switching Waveforms (Boost Region)

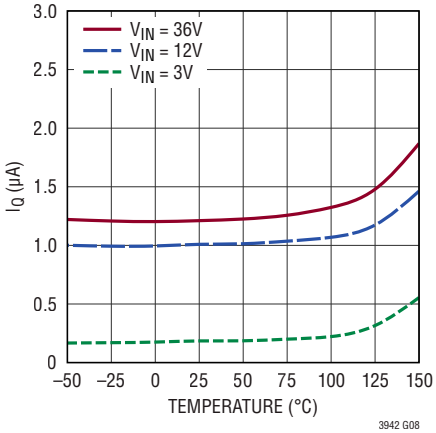


FRONT PAGE APPLICATION
V_{IN} = 8V, I_{LED} = 1A

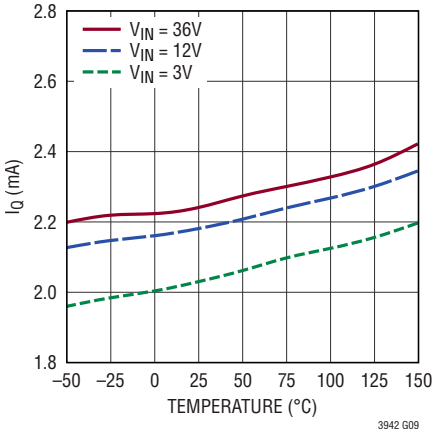
LED Current vs Combined PV_{IN}/V_{IN}



Combined PV_{IN}/V_{IN} Shutdown Current

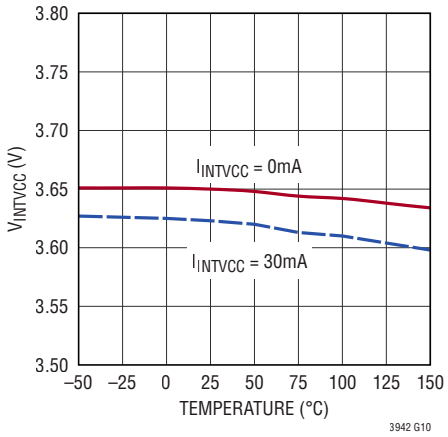


Combined PV_{IN}/V_{IN} Quiescent Current

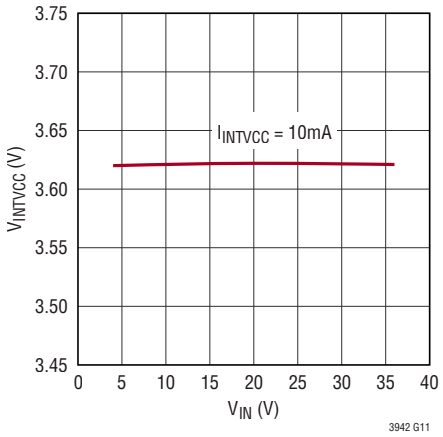


TYPICAL PERFORMANCE CHARACTERISTICS

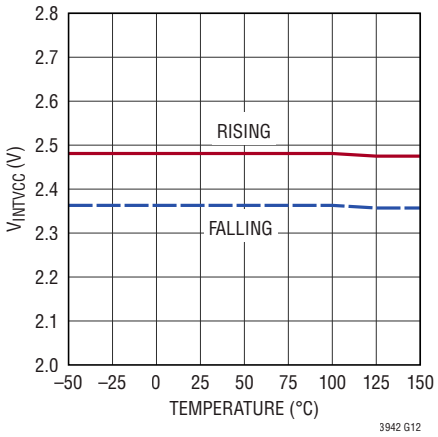
$INTV_{CC}$ Voltage vs Temperature



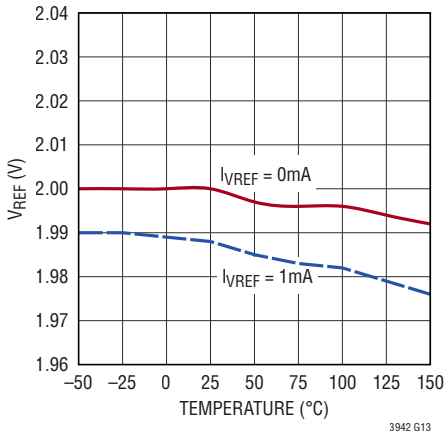
$INTV_{CC}$ Voltage vs V_{IN}



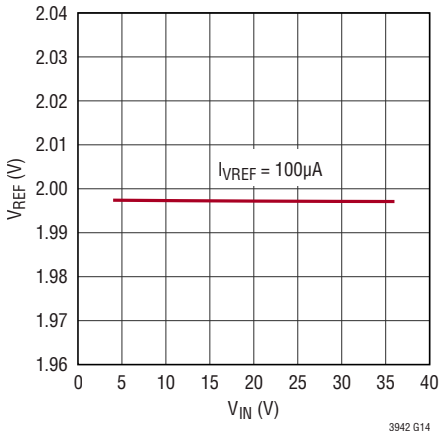
$INTV_{CC}$ UVLO Threshold



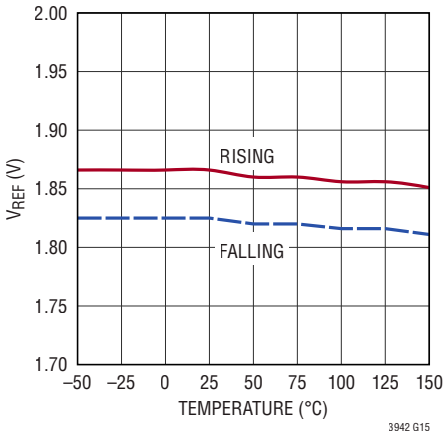
V_{REF} Voltage vs Temperature



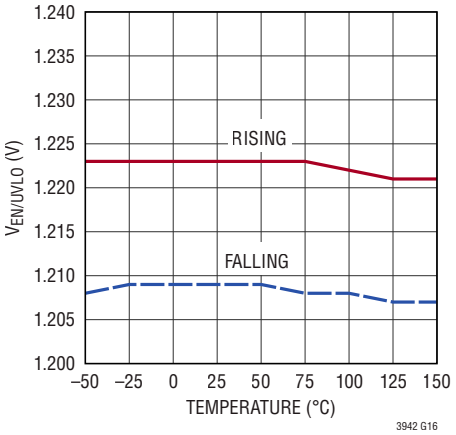
V_{REF} Voltage vs V_{IN}



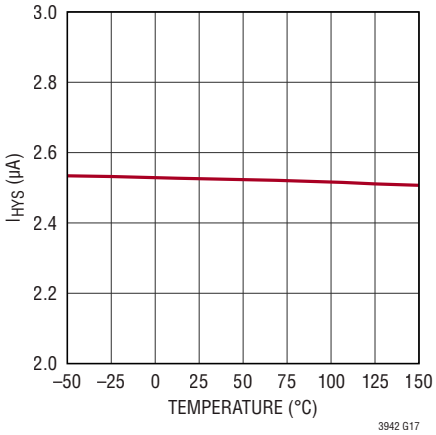
V_{REF} UVLO Threshold



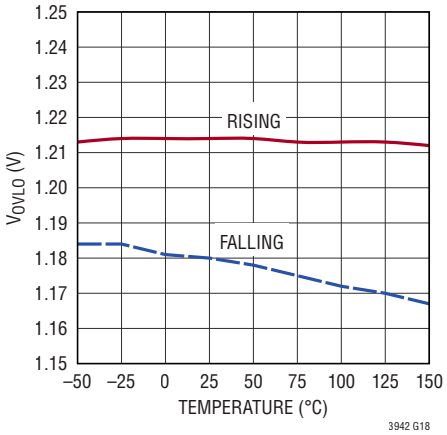
EN/UVLO Enable Threshold



EN/UVLO Hysteresis Current

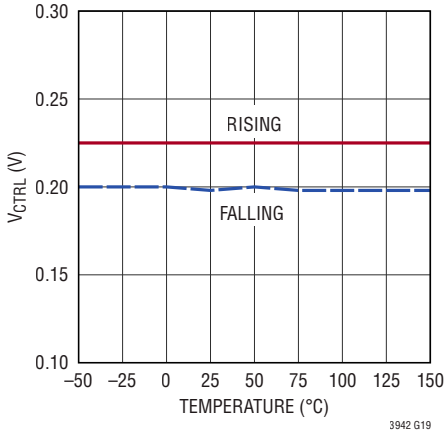


OVLO Threshold

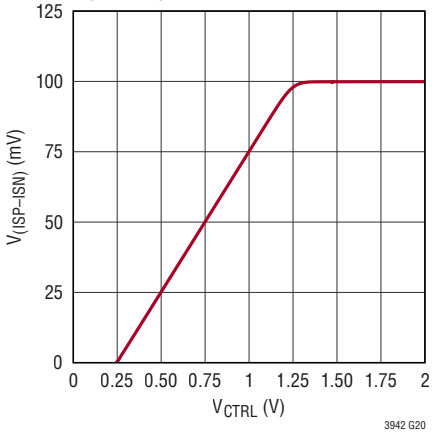


TYPICAL PERFORMANCE CHARACTERISTICS

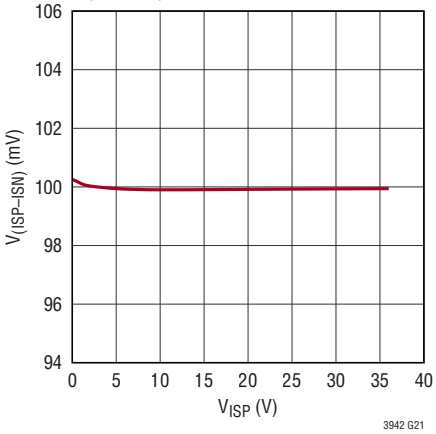
CTRL Dim-Off Threshold



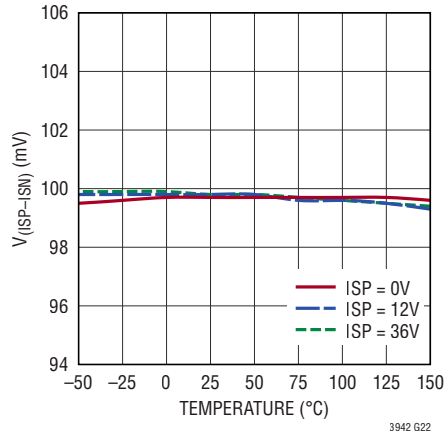
V(ISP-ISN) Regulation vs VCTRL



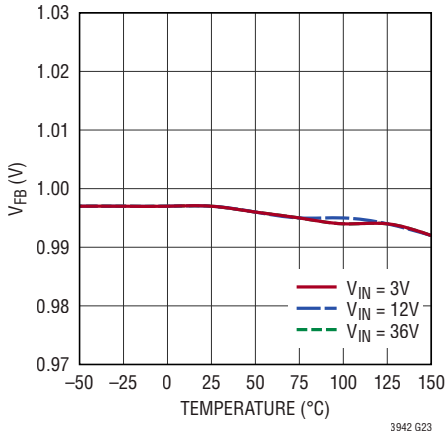
V(ISP-ISN) Regulation vs VISP



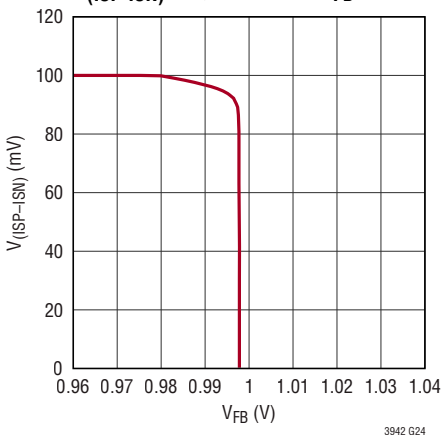
V(ISP-ISN) Regulation vs Temperature



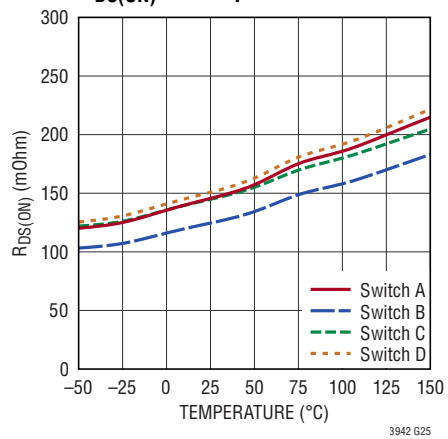
FB Regulation vs Temperature



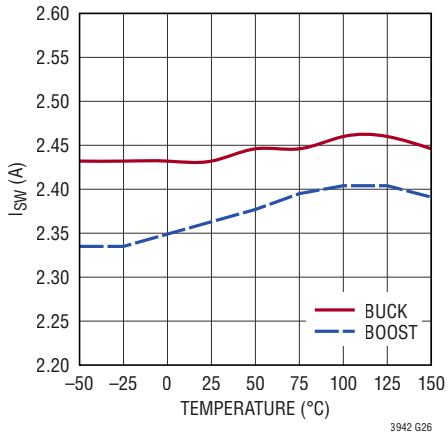
V(ISP-ISN) Regulation vs VFB



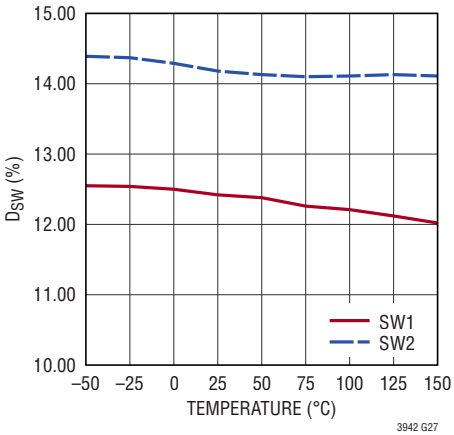
RDS(ON) vs Temperature



Peak Current vs Temperature

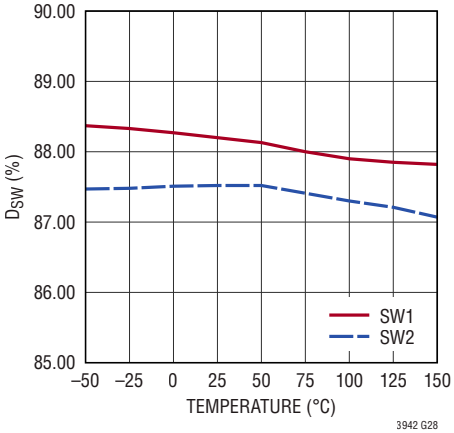


Minimum On-Time vs Temperature

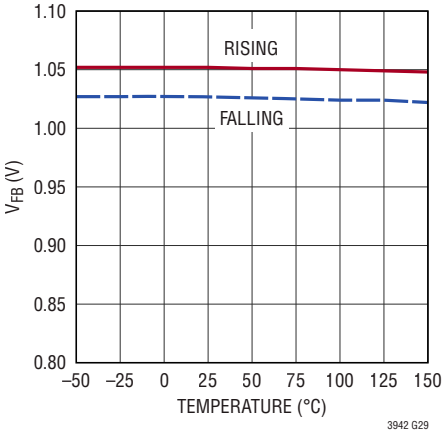


TYPICAL PERFORMANCE CHARACTERISTICS

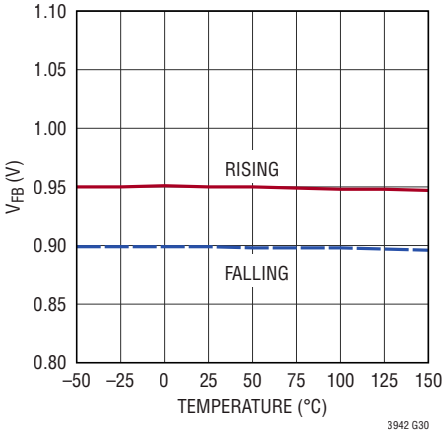
Maximum On-Time vs Temperature



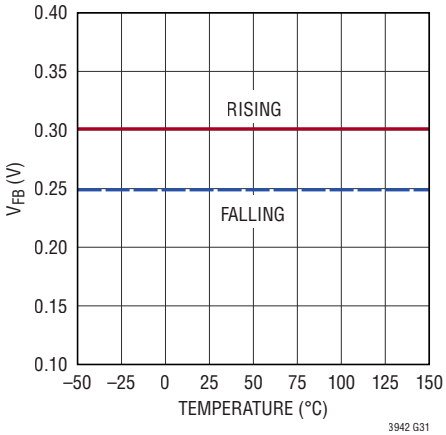
FB Overvoltage Threshold



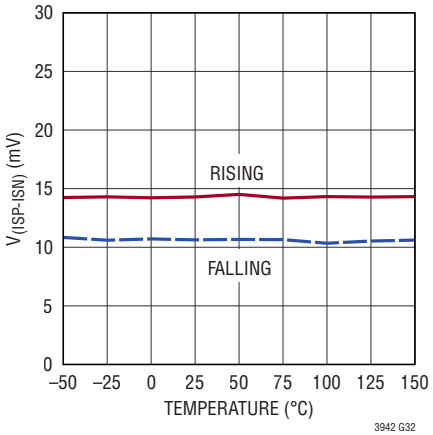
FB Open LED Threshold



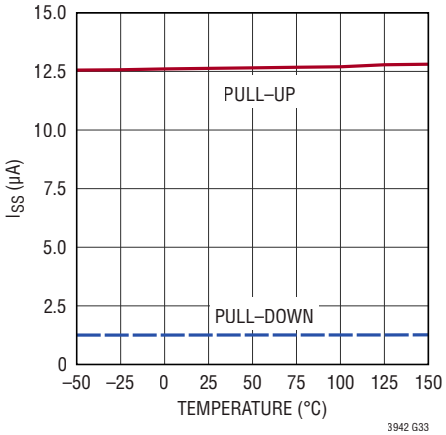
FB Short LED Threshold



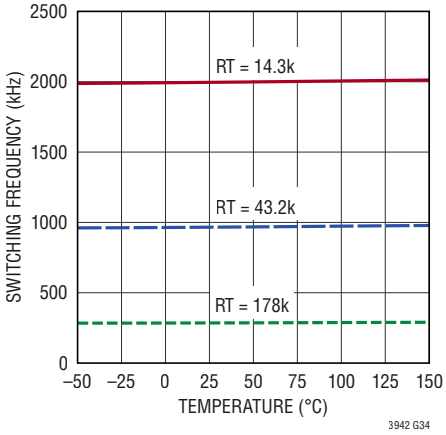
ISP/ISN Open LED Threshold



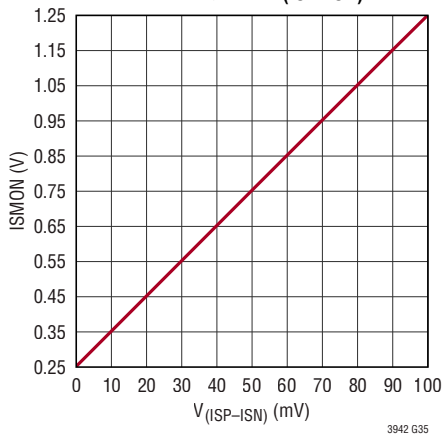
SS Current vs Temperature



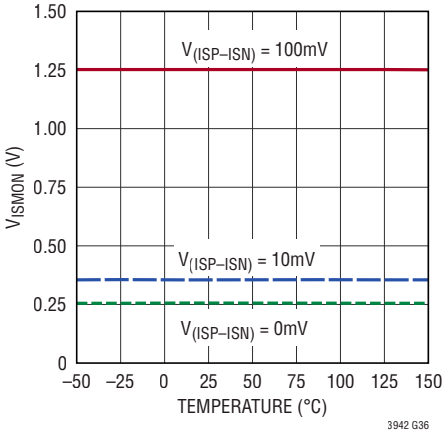
Frequency vs Temperature



ISMON Voltage vs $V_{(ISP–ISN)}$



ISMON vs Temperature



PIN FUNCTIONS

PV_{IN}: Power Input. The PV_{IN} pins connect to the power input of the converter. Bypass this pin to ground with a ceramic capacitor. The bypass capacitor should be placed as close to the chip as possible with vias directly down to the ground plane.

V_{IN}: Bias Supply. The V_{IN} pin supplies the internal circuitry and the $INTV_{CC}$ linear regulator. Connect this pin to PV_{IN} or another power supply. Bypass this pin to ground with a ceramic capacitor.

$INTV_{CC}$: Internal 3.6V Linear Regulator Output. Powered from the V_{IN} pin, the $INTV_{CC}$ supplies the internal control circuitry and gate drivers. Bypass this pin to ground with a minimum 1µF ceramic capacitor.

EN/UVLO: Enable and Undervoltage Lockout. Force the pin below 0.3V to shut down the chip and reduce V_{IN} quiescent current below 2µA. Force the pin above 1.235V for normal operation. The accurate 1.220V falling threshold can be used to program an undervoltage lockout (UVLO) threshold with a resistor divider from PV_{IN} to ground. An accurate 2.5µA pull-down current allows the programming of PV_{IN} UVLO hysteresis. If neither function is used, tie this pin directly to V_{IN}.

OVLO: Overvoltage Lockout. The OVLO pin can be used to program an overvoltage lockout (OVLO) threshold with a resistor divider from PV_{IN} to ground. Force the pin above 1.220V to pull SS pin to ground and stop switching. If not used, tie this pin to ground.

RP: Internal PWM Dimming Frequency Setting. The RP pin is used to set the internal PWM dimming frequency with a resistor to ground. Do not use a resistor larger than 1MΩ and do not leave this pin open. For external PWM dimming or voltage regulator, tie this pin to ground.

PWM: Load Switch Enable Input in Voltage Regulator or PWM Dimming Input in LED Driver. In Voltage Regulator, the pin is used to control the ON/OFF of high side PMOS load switch. If the load switch control is not used, tie this pin to V_{REF} or $INTV_{CC}$. In LED driver, the PWM pin can be used in two ways: external PWM dimming and internal PWM dimming. For external PWM dimming, drive this pin with a digital pulse from 0V to a voltage higher than 1.5V to control PWM dimming of the LED string. Make sure the RP pin is tied to ground this case. For internal PWM dimming, apply an analog voltage between 1V and 2V to generate an internal digital pulse. If PWM dimming is not used, tie this pin to $INTV_{CC}$. Forcing the pin low turns off all power switches, disconnects the V_C pin from all internal loads and turns off PWMTG.

V_{REF}: Voltage Reference Output. The V_{REF} pin provides an accurate 2V reference capable of supplying up to 1mA current. Bypass this pin to ground with a minimum 0.22µF ceramic capacitor.

CTRL: Control Input for ISP/ISN Current Sense Threshold. The CTRL pin is used to program the ISP/ISN regulation current:

$$I_{IS(MAX)} = \frac{MIN(V_{CTRL} - 0.25V, 1V)}{10 \bullet R_{IS}}$$

The V_{CTRL} can be set by an external voltage reference or a resistor divider from V_{REF} to ground. For $0.25V \le V_{CTRL} \le 1.15V$, the current sense threshold linearly goes up from 0mV to 90mV. For $V_{CTRL} \ge 1.35V$, the current sense threshold is constant at 100mV full scale value. For $1.15V \le V_{CTRL} \le 1.35V$, the current sense threshold smoothly transitions from the linear function of V_{CTRL} to the 100mV constant value. Tie CTRL pin to V_{REF} for the 100mV full scale threshold. Force the pin below 0.2V to stop switching.

ISP: Positive Terminal of ISP/ISN Current Sense Resistor (R_{IS}). Ensure accurate current sense with Kelvin connection.

ISN: Negative Terminal of ISP/ISN Current Sense Resistor (R_{IS}). Ensure accurate current sense with Kelvin connection.

ISMON: ISP/ISN Current Monitor Output. The ISMON pin generates a buffered voltage that is equal to ten times $V_{(ISP-ISN)}$ plus 0.25V offset voltage. The voltage on the

PIN FUNCTIONS

ISMON pin will be 1.25V when $V_{(ISP-ISN)}$ is equal to 100mV full scale.

$\overline{FAULT}$: LED Fault Open Drain Output. The $\overline{FAULT}$ pin is pulled low when any of the following conditions happens:

1. Open LED (V_{FB} > 0.95V and $V_{(ISP–ISN)}$ < 10mV)

2. Short LED (V_{FB} < 0.25V)

To function, this pin requires an external pull-up resistor. The $\overline{FAULT}$ status is updated only during PWM high state and latched during PWM low state.

SS: Soft-Start Timer Setting. The SS pin is used to set soft-start timer by connecting a capacitor to ground. An internal 12.5µA pull-up current charging the external SS capacitor gradually ramps up FB regulation voltage. A 22nF capacitor is recommended on this pin. Any UVLO, OVLO, or thermal shutdown immediately pulls SS pin to ground and stops switching. Using a single resistor from SS to V_{REF}, the LT3942 can be set in three different fault modes during open or short LED fault conditions: hiccup (no resistor), latch-off (499k) and keep-running (100k). In voltage regulator, always connect SS pin to V_{REF} with 100k resistor. See more details in the Applications Information section.

FB: Voltage Loop Feedback Input. The FB pin is used for constant-voltage regulation and LED fault protection. The internal error amplifier with its output V_C regulates V_{FB} to 1.00V through the LED driver. During open LED (V_{FB} > 0.95V and $V_{(ISP-ISN)}$ < 10mV) or short LED (V_{FB} < 0.25V) fault conditions, the part pulls the $\overline{FAULT}$ pin low and enters one fault mode per customer setting. During an overvoltage (V_{FB} > 1.05V) condition, the part turns off all power switches and PWMTG.

V_C: Error Amplifier Output to Set Inductor Current Comparator Threshold. The V_C pin is used to compensate the control loop with an external RC network. During PWM low state, the V_C pin is disconnected from all internal loads to store its voltage information for the highest PWM dimming performance.

RT: Switching Frequency Setting. Connect a resistor from this pin to ground to set the internal oscillator frequency from 300kHz to 2MHz.

SYNC/SPRD: Switching Frequency Synchronization or Spread Spectrum. Ground this pin for switching at the internal oscillator frequency. Apply a clock signal for external frequency synchronization. Tie to $INTV_{CC}$ for 25% triangle spread spectrum above internal oscillator frequency.

PWMTG: PWM Dimming Top Gate Drive. The PWMTG pin produces a buffered and inverted version of the PWM input signal and drives an external high side PMOS PWM switch with a voltage swing from the higher voltage between (PV_{OUT} – 5V) and 1.2V to PV_{OUT}. Leave this pin open if not used.

PV_{OUT}: Power Output. The PV_{OUT} pins connect to the power output of the converter and also serve as the positive rail for the PWMTG drive. Bypass this pin to ground with a ceramic capacitor. The bypass capacitor should be placed as close to the chip as possible with vias directly down to the ground plane.

SW2: Boost Side Switch Node. The SW2 pin connects to the internal power switches and swings from ground to a diode voltage above PV_{OUT}. Minimize the PCB area and trace length to keep EMI low.

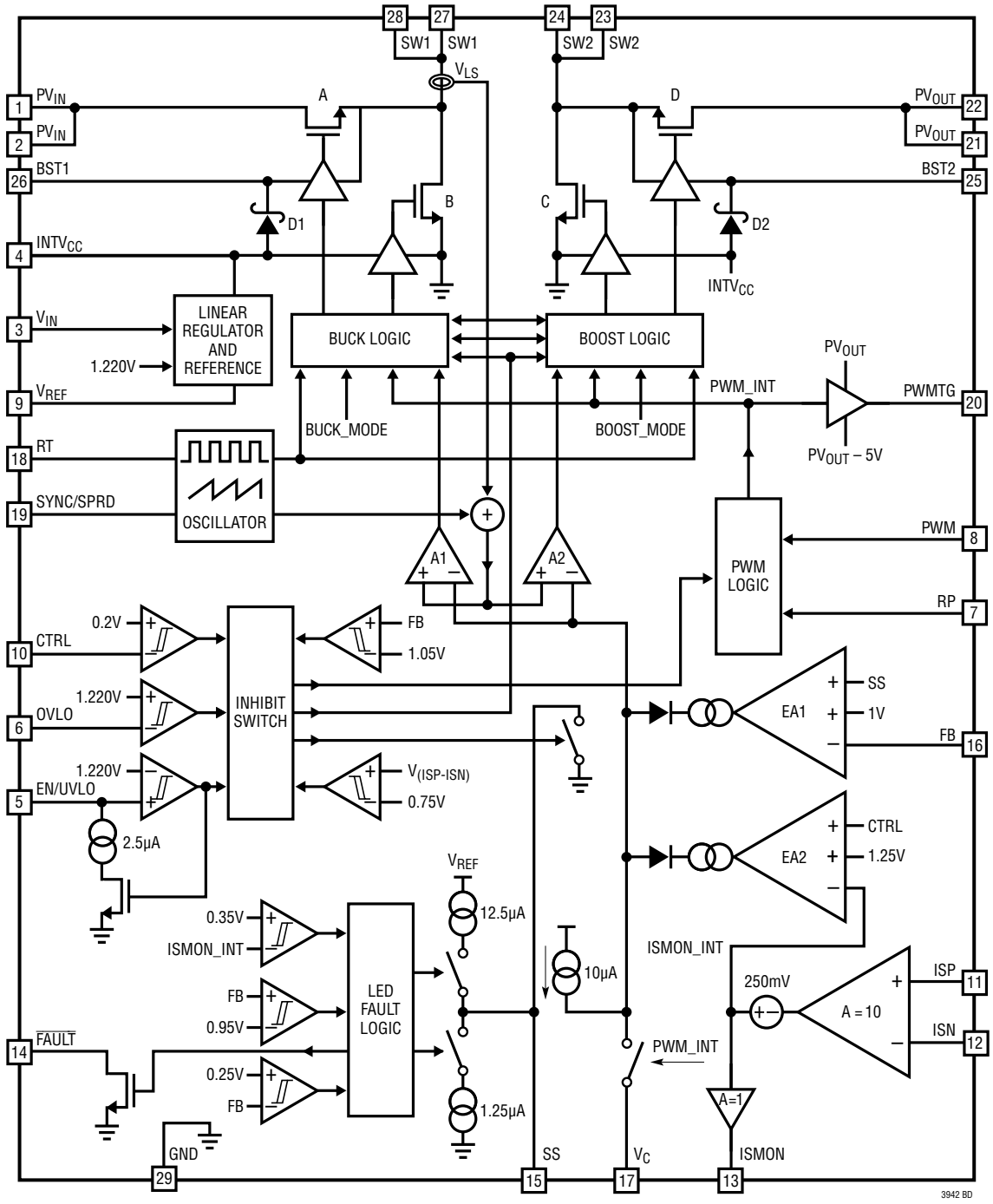
BST2: Boost Side Bootstrap Floating Driver Supply. The BST2 pin connects to an integrated bootstrap diode from the $INTV_{CC}$ pin and requires an external bootstrap capacitor to the SW2 pin.

BST1: Buck Side Bootstrap Floating Driver Supply. The BST1 pin connects to an integrated bootstrap diode from the $INTV_{CC}$ pin and requires an external bootstrap capacitor to the SW1 pin.

SW1: Buck Side Switch Node. The SW1 pin connects to the internal power switches and swings from a diode voltage drop below ground up to PV_{IN}. Minimize the PCB area and trace length to keep EMI low.

GND (Exposed Pad): Ground. Solder the exposed pad directly to the ground plane.

BLOCK DIAGRAM



OPERATION

The LT3942 is a current mode buck-boost converter with constant voltage and constant current regulation, which can regulate the output voltage or input/output current with input voltages above, below, or equal to output voltage. Four internal low resistance N-channel DMOS switches minimize the size of the application circuit and reduce power losses to maximize efficiency. Internal high side gate drivers, which require only the addition of two small external capacitors, further simplify the design process. The ADI proprietary peak-buck peak-boost current mode control scheme directly senses the inductor current across the internal power switches and provides smooth transition between buck region, buck-boost region and boost region. The LT3942 can be configured to operate over a wide range of switching frequencies, from 300kHz to 2MHz, allowing applications to be optimized for broad area and efficiency. Its operation can be best understood by referring to the Block Diagram.

Power Switch Control

Figure 1 shows the topology of the LT3942 power stage, which is comprised of four N-channel DMOS switches and their associated gate drivers. Figure 2 shows the current mode control as a function of PV_{IN}/PV_{OUT} ratio and Figure 3 shows the operation region as a function of PV_{IN}/PV_{OUT} ratio. The power switches are properly controlled to smoothly transition between modes and regions. Hysteresis is added to prevent chattering between modes and regions.

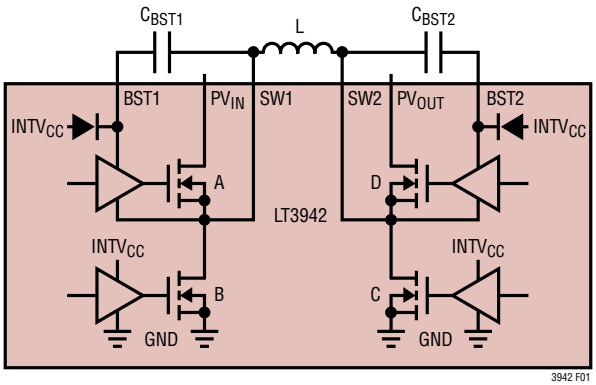


Figure 1. Power Stage Schematic

There are total four states: (1) peak-buck current mode control in buck region, (2) peak-buck current mode control in buck-boost region, (3) peak-boost current mode control in buck-boost region and (4) peak-boost current mode control in boost region. The following sections give detailed descriptions for each state with waveforms, in which the shoot-through protection dead time between switches A and B, between switches C and D are ignored for simplification.

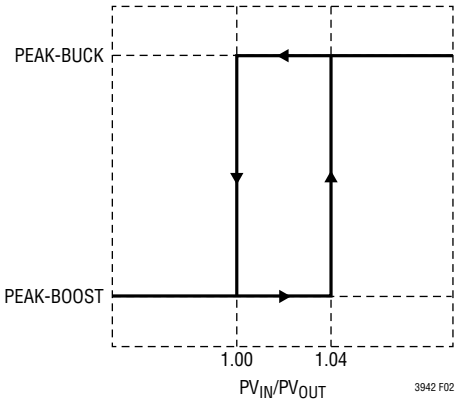


Figure 2. Current Mode vs PV_{IN}/PV_{OUT} Ratio

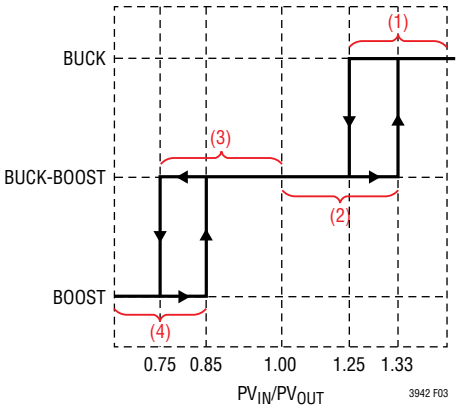


Figure 3. Operation Region vs PV_{IN}/PV_{OUT} Ratio

OPERATION

(1) Peak-Buck in Buck Region (PV_{IN} >> PV_{OUT})

When PV_{IN} is much higher than PV_{OUT}, the LT3942 uses peak-buck current mode control in buck region (Figure 4). Switch C is always off and switch D is always on. At the beginning of every cycle, switch A is turned on and the inductor current ramps up. When the inductor current hits the peak buck current threshold commanded by V_C voltage at buck current comparator A1 during (A+D) phase, switch A is turned off and switch B is turned on for the rest of the cycle. Switches A and B will alternate, behaving like a typical synchronous buck regulator.

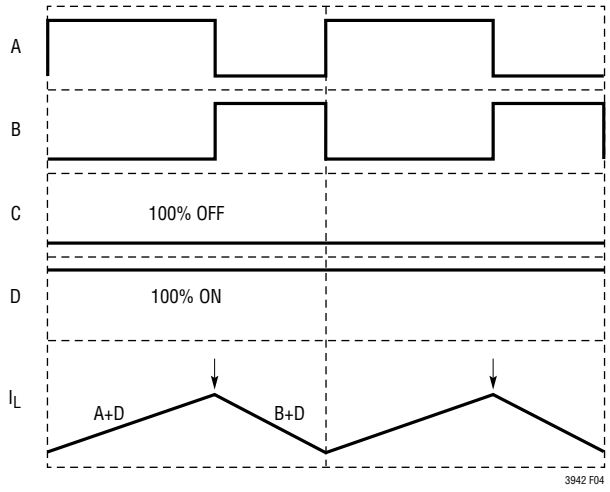


Figure 4. Peak-Buck in Buck Region (PV_{IN} >> PV_{OUT})

(2) Peak-Buck in Buck-Boost Region (PV_{IN} ~> PV_{OUT})

When PV_{IN} is slightly higher than PV_{OUT}, the LT3942 uses peak-buck current mode control in buck-boost region (Figure 5). Switch C is always turned on for the beginning 20% cycle and switch D is always turned on for the remaining 80% cycle. At the beginning of every cycle, switches A and C are turned on and the inductor current ramps up. After 20% cycle, switch C is turned off and switch D is turned on, and the inductor keeps ramping up. When the inductor current hits the peak buck current threshold commanded by V_C voltage at buck current comparator A1 during (A+D) phase, switch A is turned off and switch B is turned on for the rest of the cycle.

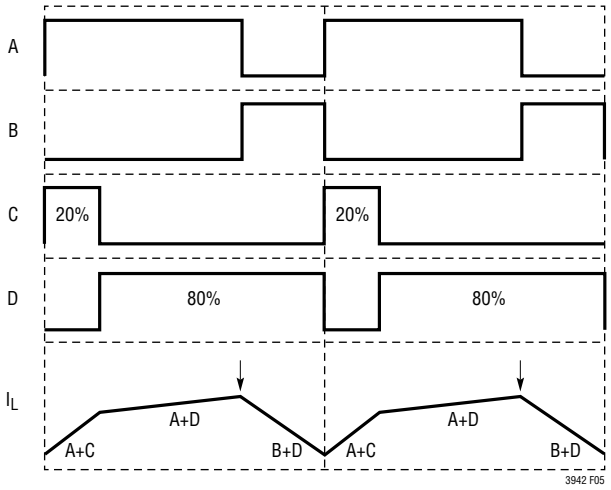


Figure 5. Peak-Buck in Buck-Boost Region (PV_{IN} ~> PV_{OUT})

(3) Peak-Boost in Buck-Boost Region (PV_{IN} <~ PV_{OUT})

When PV_{IN} is slightly lower than PV_{OUT}, the LT3942 uses peak-boost current mode control in buck-boost region (Figure 6). Switch A is always turned on for the beginning 80% cycle and switch B is always turned on for the remaining 20% cycle. At the beginning of every cycle, switches A and C are turned on and the inductor current ramps up. When the inductor current hits the peak boost current threshold commanded by V_C voltage at boost current comparator A2 during (A+C) phase, switch C is turned off and switch D is turned on for the rest of the cycle. After 80% cycle, switch A is turned off and switch B is turned on for the rest of the cycle.

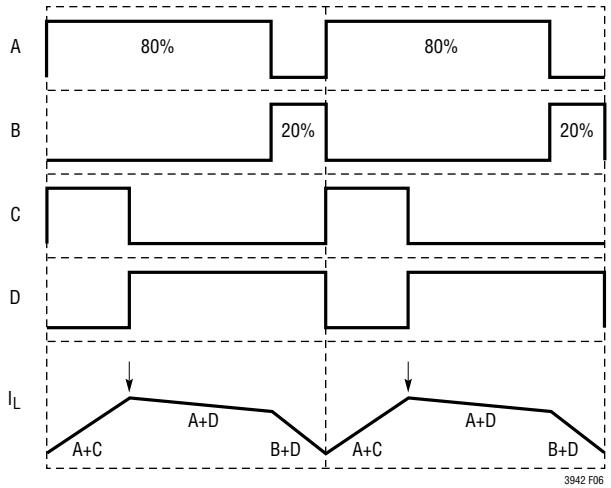


Figure 6. Peak-Boost in Buck-Boost Region (PV_{IN} <~ PV_{OUT})

OPERATION

(4) Peak-Boost in Boost Region (PV_{IN} << PV_{OUT})

When PV_{IN} is much lower than PV_{OUT}, the LT3942 uses peak-boost current mode control in boost region (Figure 7). Switch A is always on and switch B is always off. At the beginning of every cycle, switch C is turned on and the inductor current ramps up. When the inductor current hits the peak boost current threshold commanded by V_C voltage at boost current comparator A2 during (A+C) phase, switch C is turned off and switch D is turned on for the rest of the cycle. Switches C and D will alternate, behaving like a typical synchronous boost regulator.

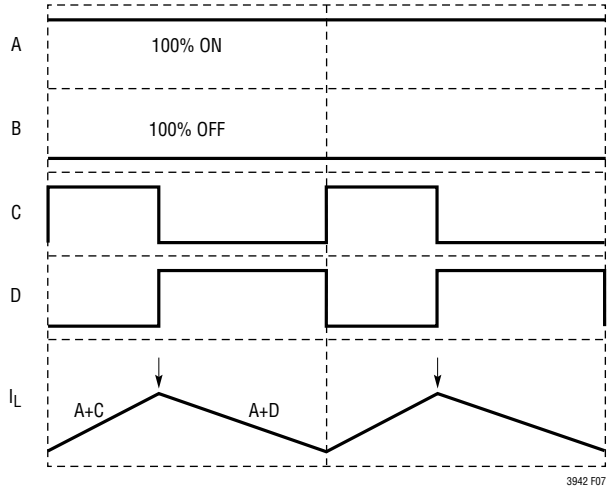


Figure 7. Peak-Boost in Boost Region (PV_{IN} << PV_{OUT})

Main Control Loop

The LT3942 is a fixed frequency current mode converter. The inductor current is directly sensed across the internal switch A. The current sense voltage is added to a slope compensation ramp signal from the internal oscillator. The summing signal is then fed into the positive terminals of the buck current comparator A1 and boost current comparator A2. The negative terminals of A1 and A2 are controlled by the voltage on the V_C pin, which is the diode-OR of error amplifiers EA1 and EA2.

Depending on the state of the peak-buck peak-boost current mode control, either the buck logic or the boost logic is controlling the four power switches so that either the FB voltage is regulated to 1V or the current sense voltage between the ISP and ISN pins is regulated by the CTRL pin during normal operation. The gains of EA1 and EA2 have been balanced to ensure smooth transition between constant-voltage and constant-current operation with the same compensation network.

Light Load Current Operation

At light load, the LT3942 typically still runs at its full switching frequency in discontinuous conduction mode. Both buck and boost reserve current sense thresholds are set to be zero, thus preventing any reverse current flowing from the output to the input. In the buck region, switch B is turned off whenever the buck reverse current threshold is triggered during (B+D) phase. In the boost region, switch D is turned off whenever the boost reverse current threshold is triggered during (A+D) phase. In the buck-boost region, switch D is turned off whenever the boost reverse current threshold is triggered during (A+D) phase, and both switches B and D are turned off whenever the buck reverse current threshold is triggered during (B+D) phase.

As the load becomes lower and lower, or when a smaller value inductor is used and the inductor current ripple is bigger, the LT3942 may run in pulse-skip mode, where the switches are held off for multiple cycles (i.e., skipping pulses) to maintain the regulation.

Internal Charge Path

Each of the two high side gate drivers is biased from its floating bootstrap capacitor C_{BST1} and C_{BST2}, which is normally recharged by $INTV_{CC}$ through the integrated bootstrap diode D1 and D2 when the top power switch is turned off. When the LT3942 operates exclusively in the buck or boost regions, one of the top power switches is constantly on. An internal charge path, from PV_{OUT} and BST2 to BST1 or from PV_{IN} and BST1 to BST2, charges the bootstrap capacitor to above 3.3V so that the top power switch can be kept on.

OPERATION

Shutdown and Power-On-Reset

The LT3942 enters shutdown mode and drains less than 2µA quiescent current when the EN/UVLO pin is below its shutdown threshold (0.3V minimum). Once the EN/UVLO pin is above its shutdown threshold (0.9V maximum), the LT3942 wakes up start-up circuitry, generates the band-gap reference and powers up the internal $INTV_{CC}$ LDO. The $INTV_{CC}$ LDO supplies the internal control circuitry and gate drivers. When the EN/UVLO is between 0.9V and 1.220V, the LT3942 enters undervoltage lockout (UVLO) mode with a hysteresis current (2.5µA typical) pulled into the EN/UVLO pin. When the $INTV_{CC}$ pin is charged above its rising UVLO threshold (2.49V typical), the EN/UVLO pin exceeds its rising enable threshold (1.235V typical) and the junction temperature is less than its thermal shut-down (165°C typical), the LT3942 enters enable mode and the EN/UVLO hysteresis current is turned off. When the voltage on the OVLO pin, which is programmed by a resistor divider from PV_{IN} to GND, exceeds its 1.220V rising threshold (with 35mV falling hysteresis), the LT3942 enters overvoltage lockout (OVLO) mode. Only when both UVLO and OVLO are cleared, the voltage reference V_{REF} can be charged up from ground to regulation. From the time of entering enable mode to the time of V_{REF} passing its rising UVLO threshold (1.89V typical), the LT3942 is going through a power-on-reset (POR), waking up the entire internal control circuitry and settling to the right initial conditions. After the POR, the LT3942 is ready and waiting for the signals on the CTRL and PWM pins to start switching.

Start-Up and Fault Protection

Figure 8 shows the start-up and fault sequence for the LT3942. In the POR state, the SS pin is hard pulled down with a 100Ω to ground. In a pre-biased condition, the SS pin has to be pulled below 0.2V to enter the INIT state, where the LT3942 wait 10µs so that the SS pin can be fully discharged to ground. After the 10µs, the LT3942 enters the UP/PRE state when the PWM_{ON} signal goes high. The PWM_{ON} high signal happens when the CTRL pin is above its rising dim-off thresholds (0.225V typical) and the external or internal PWM dimming is on.

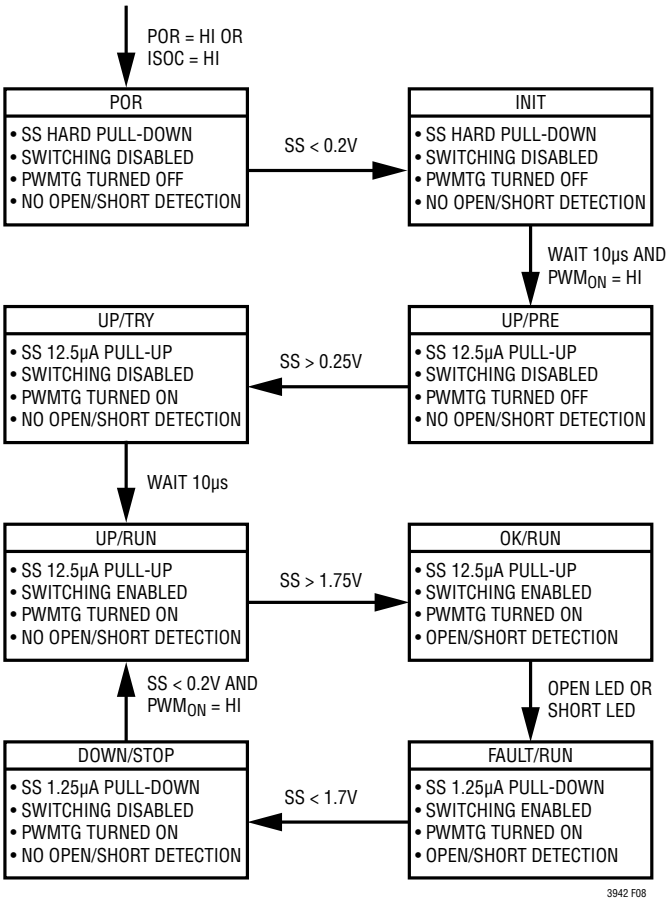


Figure 8. Start-Up and Fault Sequence

During the UP/PRE state, the SS pin is charged up by a 12.5µA pull-up current while the switching is disabled and the PWMTG is turned off. Once the SS pin is charged above 0.25V, the LT3942 enters the UP/TRY state, where the PWMTG is turned on first while the switching is still disabled. If an excessive current flowing through the current sense resistor triggers the ISP/ISN over current (ISOC) signal, it will reset the LT3942 back to the POR state. After 10µs in the UP/TRY state without triggering the ISOC signal, the LT3942 enters the UP/RUN state.

In the UP/RUN state, the switching is enabled and the start-up of the output voltage PV_{OUT} is controlled by the voltage on the SS pin. When the SS pin voltage is less than 1V, the LT3942 regulates the FB pin voltage to the SS pin voltage instead of the 1V reference. This allows the SS pin to be used to program soft-start by connecting an external capacitor from the SS pin to GND. The internal

OPERATION

12.5µA pull-up current charges up the capacitor, creating a voltage ramp on the SS pin. As the SS pin voltage rises linearly from 0.25V to 1V (and beyond), the output voltage PV_{OUT} rises smoothly to its final voltage.

Once the SS pin is charged above 1.75V, the LT3942 enters the OK/RUN state, where the LED fault (both open LED and short LED) detection is activated. The open LED indicates that V_{FB} > 0.95V and $V_{(ISP-ISN)}$ < 10mV, and the short LED indicates that V_{FB} < 0.25V. Both the open LED and short LED faults are reported to the $\overline{FAULT}$ pin. When either fault occurs, the LT3942 enters the FAULT/RUN state, where a 1.25µA pull-down current slowly discharges the SS pin. Once the SS pin is discharged below 1.7V, the LT3942 enters the DOWN/STOP state, where the switching is disabled and the LED fault detection is deactivated with the previous fault latched. Once the SS pin is discharged below 0.2V and the PWM_{ON} signal is still high, the LT3942 goes back to the UP/RUN state.

In an open or short LED condition, the LT3942 can be set to hiccup, latch-off, or keep-running fault protection mode with a resistor between the SS and V_{REF} pins. Without any resistor, the LT3942 will hiccup between 0.2V and 1.75V and go through the UP/RUN, OK/RUN, FAULT/RUN and DOWN/STOP states until the fault condition is cleared. With a 499k resistor, the LT3942 will latch off until the EN/UVLO is toggled. With a 100k resistor, the LT3942 will keep running regardless of the fault.

In voltage regulator, the LT3942 must be set to keep-running mode with a 100k resistor between SS and V_{REF} pins. In output short condition, the LT3942 output current is limited by pre-set ISP/ISN regulation or peak switch current limit.

APPLICATIONS INFORMATION

The front page shows a typical LT3942 application circuit. This Applications Information section serves as a guideline for selecting external components for typical applications. The examples and equations in this section assume continuous conduction mode unless otherwise specified.

Switching Frequency Selection

The LT3942 uses a constant frequency control scheme between 300kHz and 2MHz. Selection of the switching frequency is a trade-off between efficiency and component size. Low frequency operation improves efficiency by reducing switching losses, but requires larger inductor and capacitor values. For high power applications, consider operating at lower frequencies to minimize switching losses. For low power applications, consider operating at higher frequencies to minimize the total solution size. In addition, the specific application can play an important role in switching frequency selection. In a noise-sensitive system, the switching frequency is usually selected to keep the switching noise out of a sensitive frequency band.

Switching Frequency Setting

The switching frequency of the LT3942 can be set by the internal oscillator. With the SYNC/SPRD pin pulled to ground, the switching frequency is set by a resistor from the RT pin to ground. Table 1 shows R_T resistor values for common switching frequencies.

Table 1. Switching Frequency vs R_T Value (1% Resistor)

f_{OSC} (kHz)	R_T (kΩ)
300	178
400	124
600	78.7
800	56.2
1000	43.2
1200	33.2
1400	26.1
1600	21.5
1800	17.4
2000	14.3

Spread Spectrum Frequency Modulation

Switching regulators can be particularly troublesome for applications where electromagnetic interference (EMI) is a concern. To improve the EMI performance, the LT3942 implements a triangle spread spectrum frequency modulation scheme. With the SYNC/SPRD pin tied to $INTV_{CC}$, the LT3942 spreads its switching frequency 25% above the internal oscillator frequency. Figures 9 and 10 show the noise spectrum of the front page application with ferrite bead EMI filter and spread spectrum enabled.

CISPR 25 Average Conducted EMI

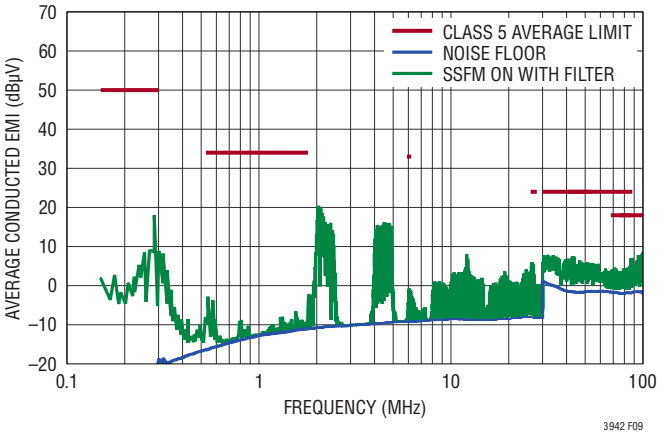


Figure 9. Conducted Average EMI Comparison

CISPR 25 Peak Conducted EMI

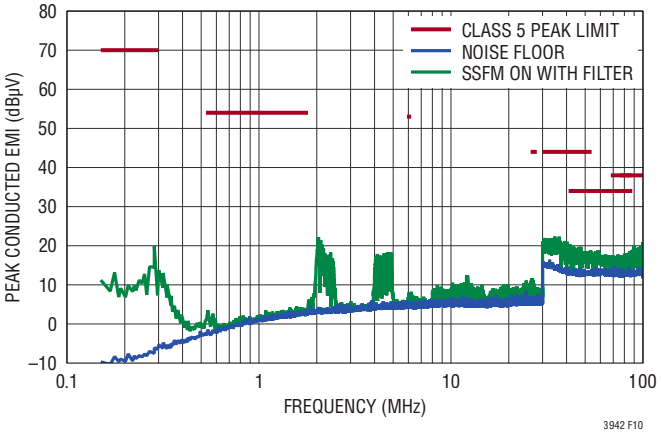


Figure 10. Conducted Peak EMI Comparison

APPLICATIONS INFORMATION

Frequency Synchronization

The LT3942 switching frequency can be synchronized to an external clock using the SYNC/SPRD pin. Driving the SYNC/SPRD with a 50% duty cycle waveform is always a good choice, otherwise maintain the duty cycle between 10% and 90%. Due to the use of a phase-locked loop (PLL) inside, there is no restriction between the synchronization frequency and the internal oscillator frequency. The rising edge of the synchronization clock represents the beginning of a switching cycle, turning on switches A and C, or switches A and D.

Maximum Output Current

The LT3942 uses the PV_{IN}/PV_{OUT} ratio to transition between modes and regions. The IR drop in the power path caused by $R_{DS(ON)}$ of power switches and DCR of inductor can limit the output current capability. The maximum output current at certain PV_{OUT} is typically determined by:

$$I_{OUT} \leq 0.1 \bullet V_{OUT}$$

The $R_{DS(ON)}$ and DCR increase at higher junction temperature and the process variation have been included in the calculation above.

Meanwhile, the maximum output current also depends on minimum PV_{IN}, maximum V_{OUT}, output current and switch peak current limit.

Inductor Selection

The switching frequency and inductor selection are interrelated in that higher switching frequencies allow the use of smaller inductor and capacitor values. The inductor value has a direct effect on ripple current. The highest current ripple $\Delta I_L\%$ happens in the buck region at $PV_{IN(MAX)}$ and the lowest current ripple $\Delta I_L\%$ happens in the boost region at $PV_{IN(MIN)}$. For any given ripple allowance, the minimum inductance can be calculated as:

$$L_{BUCK} > \frac{PV_{OUT} \bullet \left(PV_{IN(MAX)} - PV_{OUT}\right)}{f_{SW} \bullet I_{LED(MAX)} \bullet \Delta I_L\% \bullet PV_{IN(MAX)}}$$

$$L_{BOOST} > \frac{PV_{IN(MIN)}^2 \bullet \left(PV_{OUT} - PV_{IN(MIN)}\right)}{f_{SW} \bullet I_{LED(MAX)} \bullet \Delta I_L\% \bullet PV_{OUT}^2}$$

where:

f_{SW} is switching frequency

$\Delta I_L\%$ is allowable inductor current ripple

$PV_{IN(MIN)}$ is minimum power input voltage

$PV_{IN(MAX)}$ is maximum power input voltage

PV_{OUT} is output voltage

$I_{LED(MAX)}$ is maximum LED current

Slope compensation provides stability in constant frequency current mode control by preventing subharmonic oscillations at certain duty cycles. The minimum inductance required for stability can be calculated as:

$$L > \frac{V_{OUT}}{2 \bullet f_{SW} \bullet I_{SW(MAX)}}$$

where:

f_{SW} is switching frequency

$I_{SW(MAX)}$ is maximum switch current limit = 2A (Min)

For high efficiency, choose an inductor with low core loss, such as ferrite. Also, the inductor should have low DC resistance to reduce the I^2R losses and must be able to handle the peak inductor current without saturating. To minimize radiated noise, use a shielded inductor.

C_{IN} and C_{OUT} Selection

Input and output capacitance is necessary to suppress voltage ripple caused by discontinuous current moving in and out the regulator. A parallel combination of capacitors is typically used to achieve high capacitance and low equivalent series resistance (ESR). Dry tantalum, special polymer, aluminum electrolytic and ceramic capacitors are all available in surface mount packages. Capacitors with low ESR and high ripple current ratings, such as OS-CON and POSCAP are also available.

APPLICATIONS INFORMATION

Ceramic capacitors should be placed near the regulator input and output to suppress high frequency switching spikes. Ceramic capacitors, ≥ 1µF, should also be placed from PV_{IN}/V_{IN} to GND and PV_{OUT} to GND as close to the LT3942 pins as possible. Due to their excellent low ESR characteristics, ceramic capacitors can significantly reduce input ripple voltage and help reduce power loss in the higher ESR bulk capacitors. X5R or X7R dielectrics are preferred, as these materials retain their capacitance over wide voltage and temperature ranges. Many ceramic capacitors, particularly 0805 or 0603 case sizes, have greatly reduced capacitance at the desired operating voltage.

Input Capacitance C_{IN}

Discontinuous input current is highest in the buck region due to the switch A toggling on and off. Make sure that the C_{IN} capacitor network has low enough ESR and is sized to handle the maximum RMS current. In buck region, the input RMS current is given by:

$$I_{RMS} \approx I_{LED(MAX)} \bullet \frac{PV_{OUT}}{PV_{IN}} \bullet \sqrt{\frac{PV_{IN}}{PV_{OUT}} - 1}$$

The formula has a maximum at $PV_{IN} = 2PV_{OUT}$, where $I_{RMS} = I_{LED(MAX)}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief.

Output Capacitance C_{OUT}

Discontinuous current shifts from the input to the output in the boost region. Make sure that the C_{OUT} capacitor network is capable of reducing the output voltage ripple. The effects of ESR and the bulk capacitance must be considered when choosing the right capacitor for a given output ripple voltage. The maximum steady state ripple due to charging and discharging the bulk capacitance is given by:

$$\Delta V_{CAP(BOOST)} = \frac{I_{LED} \bullet \left(PV_{OUT} - PV_{IN(MIN)}\right)}{C_{OUT} \bullet PV_{OUT} \bullet f_{SW}}$$

$$\Delta V_{CAP(BUCK)} = \frac{PV_{OUT} \bullet \left(1 - \frac{PV_{OUT}}{PV_{IN(MAX)}}\right)}{8 \bullet L \bullet f_{SW}^2 \bullet C_{OUT}}$$

The maximum steady ripple due to the voltage drop across the ESR is given by:

$$\Delta V_{ESR(BOOST)} = \frac{PV_{OUT} \bullet I_{LED(MAX)}}{PV_{IN(MIN)}} \bullet ESR$$

$$\Delta V_{ESR(BUCK)} = \frac{PV_{OUT} \bullet \left(1 - \frac{PV_{OUT}}{PV_{IN(MAX)}}\right)}{L \bullet f_{SW}} \bullet ESR$$

$INTV_{CC}$ Regulator

An internal P-channel low dropout regulator produces 3.6V at the $INTV_{CC}$ pin from the V_{IN} supply pin. The $INTV_{CC}$ powers internal circuitry and gate drivers in the LT3942. The $INTV_{CC}$ regulator can supply a peak current of 40mA and must be bypassed to ground with a minimum of 1µF ceramic capacitor. Good local bypass is necessary to supply the high transient current required by power switch gate drivers.

Higher input supply voltage applications with higher switching frequencies may cause the maximum junction temperature rating for the LT3942 to be exceeded. The system supply current is normally dominated by the gate charge current that drives the four internal power switches.

To prevent maximum junction temperature from being exceeded, the input supply current must be checked operating in continuous mode at maximum PV_{IN}/V_{IN}.

High Side Gate Driver Supply (C_{BST1}, C_{BST2})

The high side gate drivers for the two top power switches, A and D, are driven between their respective SW and BST pin voltages. The boost voltages are biased from floating bootstrap capacitors C_{BST1} and C_{BST2}, which are normally recharged through internal bootstrap diodes D1 and D2

APPLICATIONS INFORMATION

when the respective top power switch is turned off. Both capacitors are charged to the same voltage as the $INTV_{CC}$ voltage. In most applications, a typical 0.1µF, X5R or X7R dielectric capacitor is adequate.

Programming PV_{IN} UVLO and OVLO

A resistor divider from PV_{IN} to the EN/UVLO pin implements PV_{IN} undervoltage lockout (UVLO). The EN/UVLO enable falling threshold is set at 1.220V with 15mV hysteresis. In addition, the EN/UVLO pin sinks 2.5µA when the voltage on the pin is below 1.220V. This current provides user programmable hysteresis based on the value of R1. The programmable UVLO thresholds are:

$$V_{IN(UVLO+)} = 1.235V \bullet \frac{R1+R2}{R2} + 2.5\mu A \bullet R1$$

$$V_{IN(UVLO-)} = 1.220V \bullet \frac{R1+R2}{R2}$$

Figure 11 shows the implementation of external shutdown control while still using the UVLO function. The NMOS grounds the EN/UVLO pin when turned on and puts the LT3942 in shutdown with quiescent current less than 2µA.

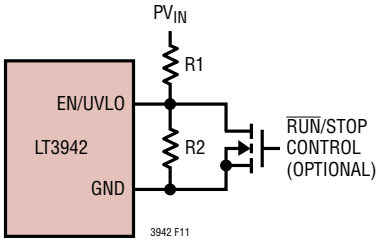


Figure 11. PV_{IN} Undervoltage Lockout (UVLO)

A resistor divider from PV_{IN} to the OVLO pin implements PV_{IN} overvoltage lockout (OVLO). The OVLO rising threshold is set at 1.220V with 35mV falling hysteresis. Figure 12 shows the implementation of PV_{IN} OVLO function. The programmable OVLO thresholds are:

$$V_{IN(OVLO+)} = 1.220V \bullet \frac{R3+R4}{R4}$$

$$V_{IN(OVLO-)} = 1.185V \bullet \frac{R3+R4}{R4}$$

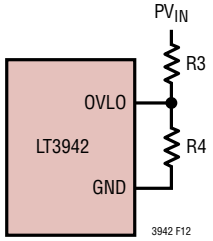


Figure 12. PV_{IN} Overvoltage Lockout (OVLO)

Programming Input/Output Current Limit or LED Current Regulation

The current is programmed by placing an appropriate value current sense resistor, R_{IS}, in the input or output power path. The voltage drop across R_{IS} is (Kelvin) sensed by the ISP and ISN pins. The CTRL pin should be tied to a voltage higher than 1.35V to obtain the full-scale 100mV obtain (typical) threshold across the sense resistor. The CTRL pin can be used to reduce the current to zero, although relative accuracy decreases with the decreasing sense threshold. When the CTRL pin voltage, V_{CTRL}, is less than 1.15V, the current is:

$$I_{IS(MAX)} = \frac{V_{CTRL} - 0.25V}{10 \bullet R_{IS}}$$

When V_{CTRL} is between 1.15V and 1.35V, the current varies with V_{CTRL}, but departs from the equation above by an increasing amount as V_{CTRL} increases. Ultimately, when V_{CTRL} > 1.35V the current no longer varies. The typical $V_{(ISP-ISN)}$ threshold vs V_{CTRL} is listed in Table 2.

Table 2. $V_{(ISP-ISN)}$ Threshold vs V_{CTRL}

V_{CTRL} (V)	$V_{(ISP-ISN)}$ (mV)
1.15	90
1.20	94.5
1.25	98
1.30	99.5
1.35	100

When V_{CTRL} is higher than 1.35V, the current is regulated to:

$$I_{IS(MAX)} = \frac{100mV}{R_{IS}}$$

APPLICATIONS INFORMATION

The CTRL pin should not be left open (tie to V_{REF} if not used). The CTRL pin can also be used in conjunction with a thermistor to provide overtemperature protection for the output load, or with a resistor divider to PV_{IN} to reduce output power and switching current when PV_{IN} is low. The presence of a time varying differential voltage ripple signal across ISP and ISN at the switching frequency is expected. The amplitude of this signal is increased by higher load current, lower switching frequency or smaller value output filter capacitor. Some level of ripple signal is acceptable, and the compensation capacitor on the V_C pin filters the signal so the average difference between ISP and ISN is regulated to the user-programmed value. The ripple voltage amplitude (peak-to-peak) in excess of 20mV should not cause mis-operation, but may lead to noticeable offset between the average value and the user-programmed value.

Monitoring Current

The ISMON pin provides a linear indication of the current flowing through the ISP/ISN current sense resistor, R_{IS}. It outputs a buffered and amplified value of the voltage difference between ISP and ISN pins. The equation for V_{ISMON} is:

$$V_{ISMON} = 10 \bullet V_{(ISP–ISN)} + 250mV$$

Dimming Control

There are two methods to control the LED current for dimming using the LT3942. One method uses the CTRL pin to adjust the current regulated in the LEDs. A second method uses the PWM pin to modulate the LED current between zero and full current to achieve a precisely programmed average current.

Compared to the analog dimming method, the PWM dimming method offers much higher dimming ratio without any color shift. To make PWM dimming more accurate, the switch demand current is stored on the V_C node when the PWM signal is low. This feature minimizes recovery time when the PWM signal goes high. To further improve the recovery time, a high side PMOS PWM switch should be used in the LED current path to prevent the output capacitor from discharging during the PWM signal low phase.

The choice of switching frequency, inductor value and loop compensation affects the minimum PWM on time, below which the LT3942 loses the LED current regulation. For the same application, the LT3942 achieves the highest PWM dimming ratio (up to 5000:1) in buck region, the medium PWM dimming ratio (up to 2500:1) in buck-boost region and the lowest PWM dimming ratio (up to 2000:1) in boost region.

In either fixed frequency operation set by RT resistor or spread spectrum frequency operation, the internal oscillator is synchronized to the PWM signal rising edge, thereby providing flicker-free PWM dimming performance. In external frequency synchronization operation, both SYNC and PWM signals must have synchronized rising edges to achieve flicker-free PWM dimming performance.

The LT3942 provides both external PWM dimming and internal PWM dimming. For external PWM dimming, choose RP resistor less than 30k and apply an external PWM clock signal to the PWM pin. For internal PWM dimming, choose RP resistor to one of the seven resistor values in Table 3 and apply analog DC voltage to the PWM pin. The RP resistor sets the internal PWM dimming frequency, and the 1V to 2V analog DC voltage on the PWM pin sets the internal PWM dimming duty ratio from 0% to 100% with a discrete 1/128 step size, as shown in Figure 13.

Table 3. Internal PWM Dimming Frequency vs R_P Value (1% Resistor)

R_P (kΩ)	f_{SW}	f_{SW} = 300kHz	f_{SW} = 1MHz	f_{SW} = 2MHz
< 20	External	External	External	External
28.7	$f_{SW}/2^8$	1.17kHz	3.91kHz	7.81kHz
47.5	$f_{SW}/2^9$	587Hz	1.95kHz	3.91kHz
76.8	$f_{SW}/2^{10}$	293Hz	977Hz	1.95kHz
118	$f_{SW}/2^{11}$	147Hz	488Hz	977Hz
169	$f_{SW}/2^{12}$	73Hz	244Hz	488Hz
237	$f_{SW}/2^{13}$	36Hz	122Hz	244Hz
332	$f_{SW}/2^{14}$	18Hz	61Hz	122Hz

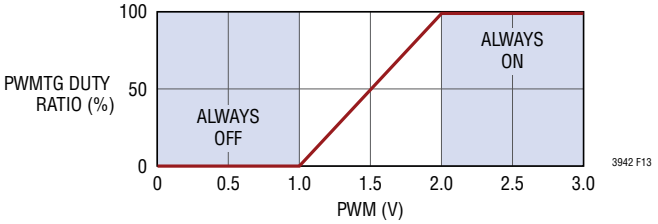


Figure 13. Internal PWM Dimming Duty Ratio vs PWM Voltage

APPLICATIONS INFORMATION

High Side PMOS PWM Switch Selection

A high side PMOS PWM switch is recommended in some voltage regulator application requiring load switch control or most of LED driver to maximize the PWM dimming ratio and protect the LED string during fault conditions. The high side PMOS PWM switch is typically selected for drain-source voltage V_{DS}, gate-source threshold voltage $V_{GS(TH)}$ and continuous drain current I_D. For proper operations, V_{DS} rating should exceed the voltage set by the FB pin, the absolute value of $V_{GS(TH)}$ should be less than 3V, and I_D rating should be above $I_{OUT(MAX)}$.

Programming Output Voltage and Thresholds

The LT3942 has a voltage feedback pin FB that can be used to program a constant-voltage output. The output voltage can be set by selecting the values of R5 and R6 (Figure 14) according to the following equation:

$$V_{OUT} = 1.00V \bullet \frac{R5 + R6}{R6}$$

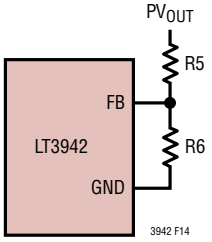


Figure 14. Feedback Resistor Connection

In addition, the FB pin also sets output overvoltage threshold, open LED threshold and short LED threshold. For an LED driver application with small output capacitors, the output voltage usually overshoots a lot during an open LED event. Although the 1.00V FB regulation loop tries to regulate the output, the loop is usually too slow to prevent the output from overshooting. Once the FB pin hits its overvoltage threshold 1.05V, the LT3942 stops switching by turning off all four power switches and also turns off PWMTG to disconnect the LED string for protection. The output overvoltage threshold can be set as:

$$V_{OUT(OVP)} = 1.05V \bullet \frac{R5 + R6}{R6}$$

Make sure the expected V_{FB} during normal operation stays between the short LED rising threshold 0.3V and the open LED falling threshold 0.9V:

$$0.3V \le V_{LED} \bullet \frac{R6}{R5 + R6} \le 0.9V$$

These equations set the maximum LED string voltage with full open LED protection for the LT3942 to be 34V.

$\overline{\text{FAULT}}$ Pin

The LT3942 provides an open-drain status pin, $\overline{\text{FAULT}}$, which is pulled low during either open LED or short LED conditions. The open LED condition happens when the FB pin is above 0.95V and the voltage across $V_{(ISP-ISN)}$ is less than 10mV. The short LED condition happens when the FB pin is below 0.25V. The $\overline{\text{FAULT}}$ status is updated when the SS pin is above 1.75V and the PWM signal is high.

Soft-Start and Fault Protection

As shown in Figure 8 and explained in the Operation section, the SS pin can be used to program soft-start by connecting an external capacitor from the SS pin to ground. The internal 12.5µA pull-up current charges up the capacitor, creating a voltage ramp on the SS pin. In voltage regulator, as the ss pin voltage rises linearly from 0.25V to 1V (and beyond), the output voltage rises smoothly into its final voltage regulation. The soft start time can be calculated as:

$$t_{SS} = 1V \bullet \frac{C_{SS}}{12.5\mu A}$$

In LED driver, as the SS pin voltage rises linearly from 0.25V to 1V (and beyond), the output voltage rises smoothly and transitions into LED current regulation. The soft-start range is defined to be the voltage range from 0V to the FB voltage in LED current regulation. The soft-start time can be calculated as:

$$t_{SS} = V_{LED} \bullet \frac{R6}{R5 + R6} \bullet \frac{C_{SS}}{12.5\mu A}$$

Make sure C_{SS} is at least five to ten times larger than the compensation capacitor on the V_C pin. A 22nF ceramic capacitor is a good starting point.

APPLICATIONS INFORMATION

In LED driver, the SS pin is also used as a fault timer. Once an open LED or a short LED fault is detected, a 1.25µA pull-down current source is activated. Using a single resistor from the SS pin to the V_{REF} pin, the LT3942 can be set to three different fault protection modes: hiccup (no resistor), latch-off (499k) and keep-running (100k).

With a 100k resistor in keep-running mode, the LT3942 continues switching normally, either regulating the programmed PV_{OUT} during open LED fault or regulating the current during short LED fault. With a 499k resistor in latch-off mode, the LT3942 stops switching until the EN/UVLO pin is pulled low and high to restart. With no resistor in hiccup mode, the LT3942 enters low duty cycle auto-retry operation. The 1.25µA pull-down current discharges the SS pin to 0.2V and then 12.5µA pull-up current charges the SS pin up. If the fault condition has not been removed when the SS pin reaches 1.75V, the 1.25µA pull-down current turns on again, initiating a new hiccup cycle. This will continue until the fault is removed.

Loop Compensation

The LT3942 uses an internal transconductance error amplifier, the output of which, V_C, compensates the control loop. The external inductor, output capacitor, and the compensation resistor and capacitor determine the loop stability.

The inductor and output capacitor are chosen based on performance, size and cost. The compensation resistor and capacitor on the V_C pin are set to optimize control loop response and stability. For a typical LED application, a 2.2nF compensation capacitor on the V_C pin is adequate, and a series resistor should always be used to increase the slew rate on the V_C pin to maintain tighter regulation of LED current during fast transients on the input supply of the converter.

For a typical voltage regulator application, a 680pF compensation capacitor on V_C pin is adequate, and a 75k series resistor should always be used to increase the slew rate on V_C pin to maintain tighter output voltage regulation during fast transient on the input supply of the converter.

Efficiency Considerations

The power efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Although all dissipative elements in circuits produce losses, four main sources account for most of the losses in LT3942 circuits:

1. DC I^2R losses. These arise from the resistances of the MOSFETs, sensing resistor, inductor and PC board traces and cause the efficiency to drop at high output currents.
2. Transition loss. This loss arises from the brief amount of time switch A or switch C spends in the saturated region during switch node transitions. It depends upon the input voltage, load current, driver strength and MOSFET capacitance, among other factors.
3. $INTV_{CC}$ current. This is the sum of the MOSFET driver and control currents.
4. C_{IN} and C_{OUT} loss. The input capacitor has the difficult job of filtering the large RMS input current to the regulator in buck region. The output capacitor has the difficult job of filtering the large RMS output current in boost region. Both C_{IN} and C_{OUT} are required to have low ESR to minimize the AC I^2R loss and sufficient capacitance to prevent the RMS current from causing additional upstream losses in fuses or batteries.

APPLICATIONS INFORMATION

When making adjustments to improve efficiency, the input current is the best indicator of changes in efficiency. If you make a change and the input current decreases, then the efficiency has increased. If there is no change in the input current, then there is no change in efficiency.

Voltage Regulator vs LED Driver

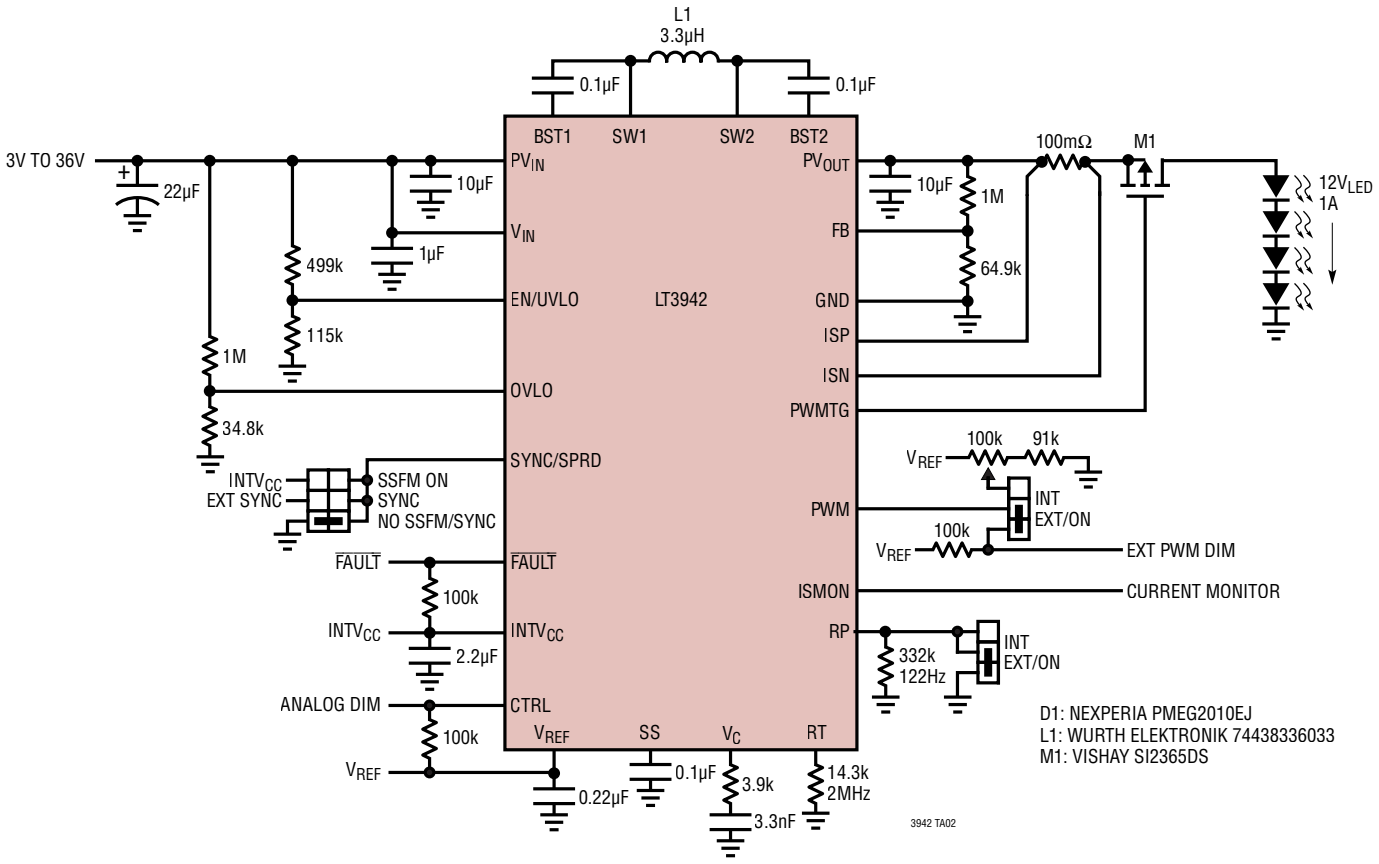
Thanks to constant voltage and constant current regulation loop, the LT3942 can be easily used for either voltage regulator or LED driver with different configuration. Table 4 lists the difference between two applications.

Table 4. Difference between Voltage Regulator and LED Driver

Pin Name	Voltage Regulator		LED Driver	
RP	Tie to GND		Int. PWM	R_P in Table 3
			Ext. PWM	Tie to GND
PWM	Tie to V_{REF} or $INTV_{CC}$		Int. PWM	V_{DC} between 1V and 2V
			Ext. PWM	V_{PULSE}
$V_{(ISP-ISN)}$	Current Limit		LED Current Regulation	
SS	Keep-Running	100k	Hiccup	No Resistor
			Keep-Running	100k
			Latch-Off	499k
FB	Output Voltage Regulation		Voltage Monitoring and Protection	

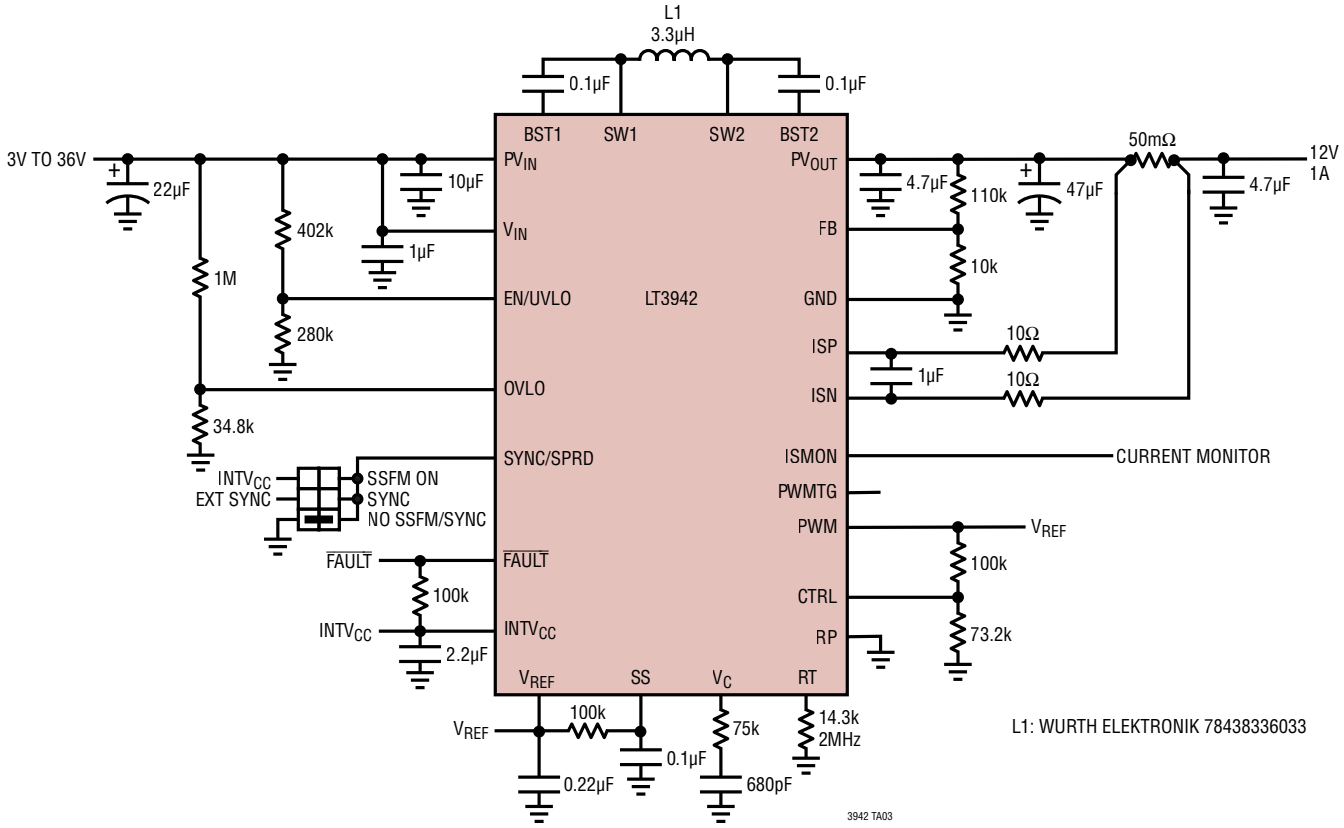
TYPICAL APPLICATIONS

93% Efficient 12W (12V, 1A) 2MHz Buck-Boost LED Driver



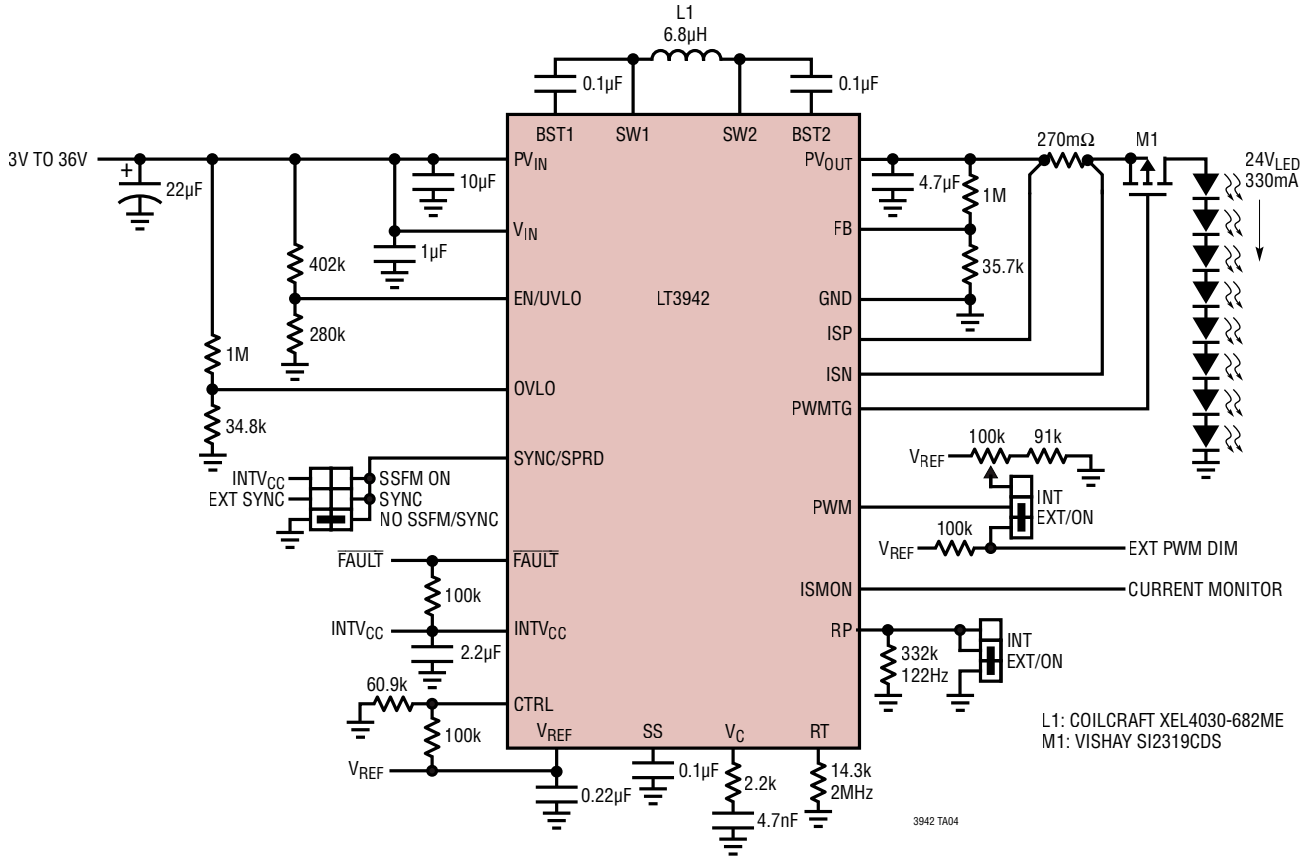
TYPICAL APPLICATIONS

12W (12V, 1A) 2MHz Buck-Boost Voltage Regulator



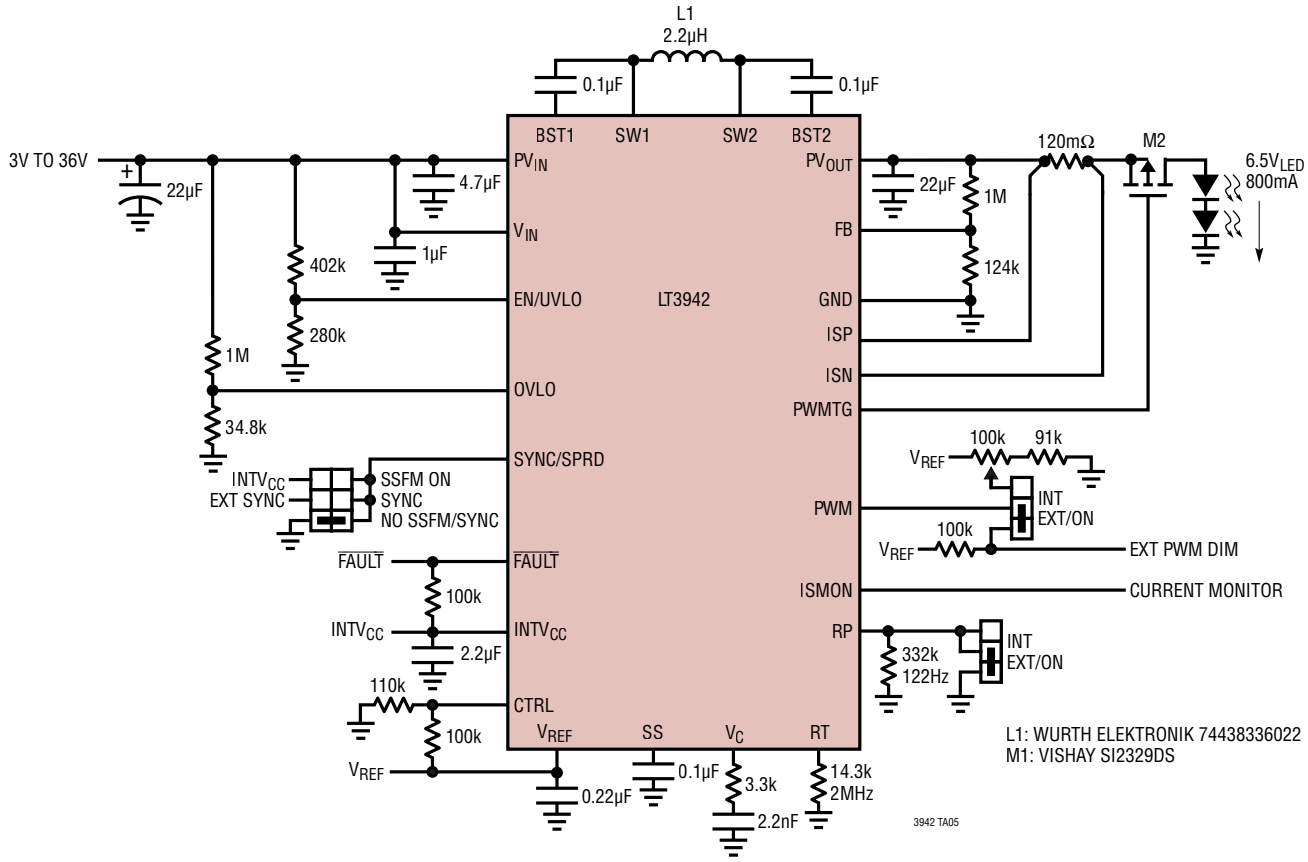
TYPICAL APPLICATIONS

8W (24V, 330mA) 2MHz Buck-Boost LED Driver



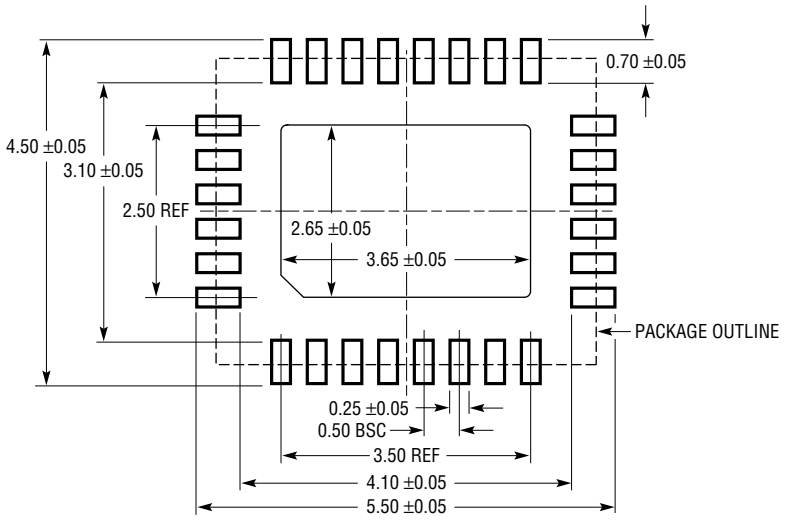
TYPICAL APPLICATIONS

5W (6.5V, 800mA) 2MHz Buck-Boost LED Driver

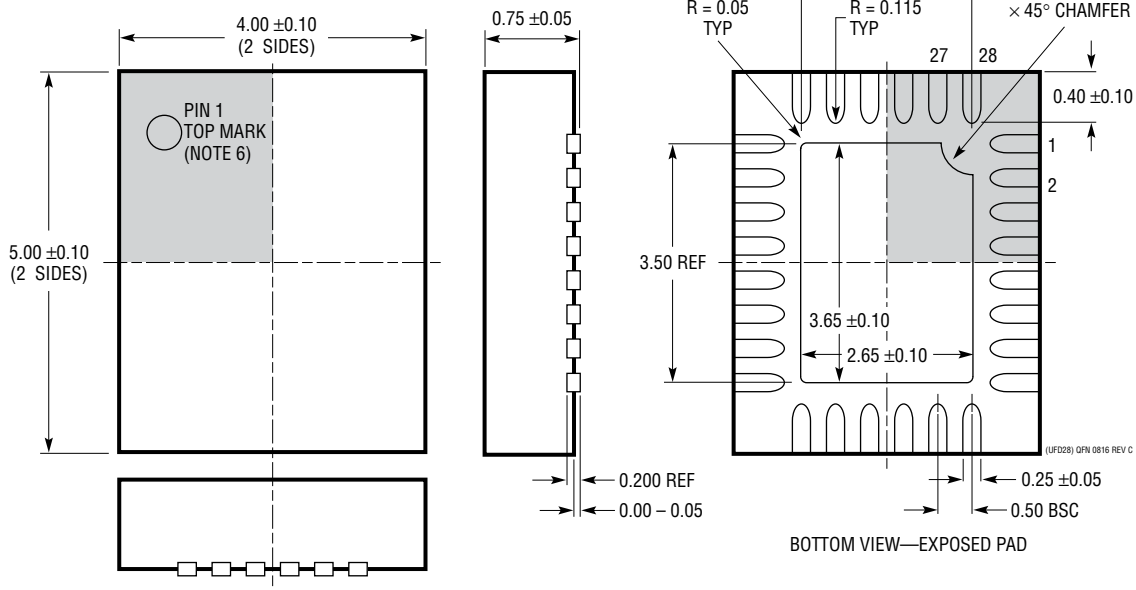


PACKAGE DESCRIPTION

UFD Package
28-Lead Plastic QFN (4mm × 5mm)
(Reference LTC DWG # 05-08-1712 Rev C)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED

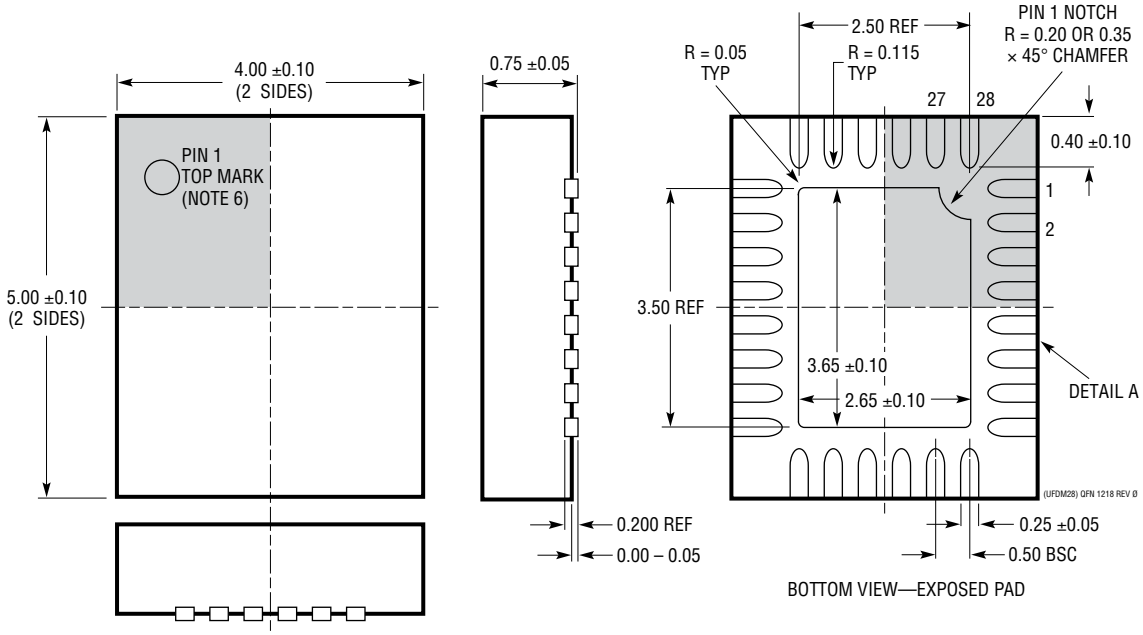


BOTTOM VIEW—EXPOSED PAD

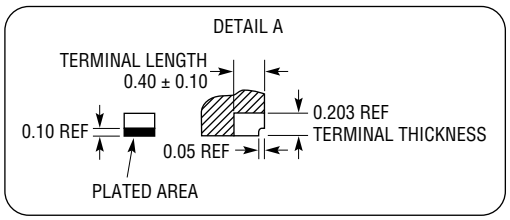
NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGHD-3).
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

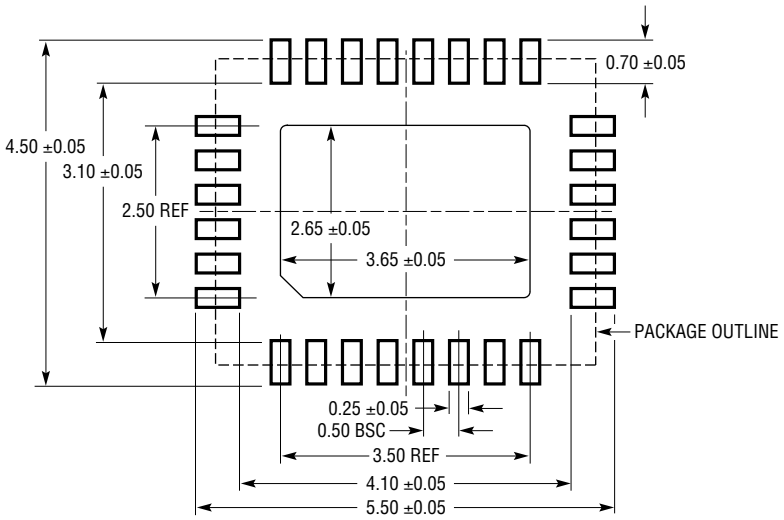
PACKAGE DESCRIPTION

UFDM Package
28-Lead Plastic Side Wettable QFN (4mm × 5mm)
(Reference LTC DWG # 05-08-1682 Rev Ø)



NOTE:
1. DRAWING NOT TO SCALE
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
4. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE





RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED

Rev. B

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	03/21	Update to Features and Description.	1
		Addition of Side-Solderable Package option.	2
		Updates to SS and PV_{OUT} Pin descriptions.	11
		Updates to text.	13, 15-17, 19, 21-24
		Addition of UFDM Package Description.	30
B	11/21	Update conditions and frequency specification in Electrical Characteristics.	3, 4
		Correct Figure 3 region labels.	13
		Update internal PWM dimming frequency for f_{SW} = 300kHz.	22