60V, 1.5A LED Driver with Internal Exponential Scale Dimming

FEATURES

- **Operates in Boost, SEPIC, Buck Mode and Buck-Boost Mode**
- **128:1 Internal Exponential Scale PWM Dimming**
- **Wide Input Voltage Range (3V to 60V)**
- **1.5A, 60V Internal Switch**
- **20000:1 External PWM Dimming at 100Hz**
- **±2% LED Current and Output Voltage Regulation**
- **PMOS Switch Driver for PWM Dimming**
- LED Short/Open Protection and Indication
- Constant Voltage and Constant Current Regulation
- Adjustable 300kHz to 2MHz Switching Frequency
- Adjustable 100Hz to 1kHz PWM Generator Frequency
- Internal Spread Spectrum Frequency Modulation
- Easy Synchronization to External Clock
- Programmable V_{IN} UVLO with Hysteresis
- Available in 16-Lead MSOP Package

APPLICATIONS

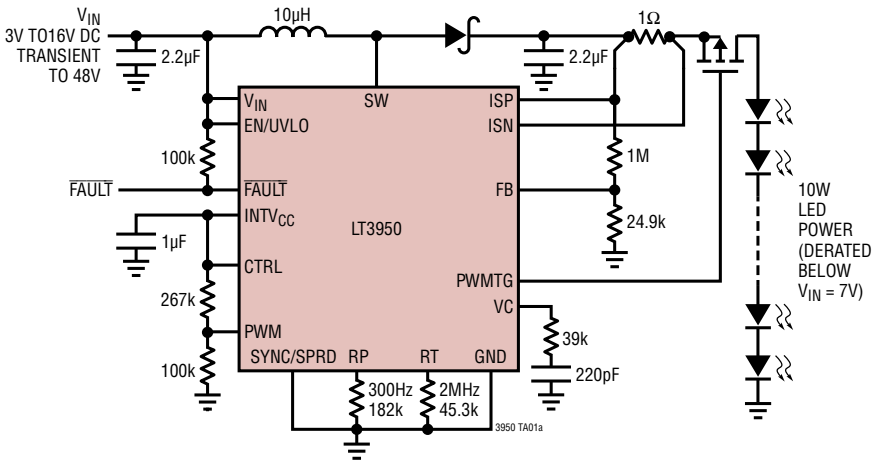
- Display Backlighting
- Automotive and Avionic Lighting

DESCRIPTION

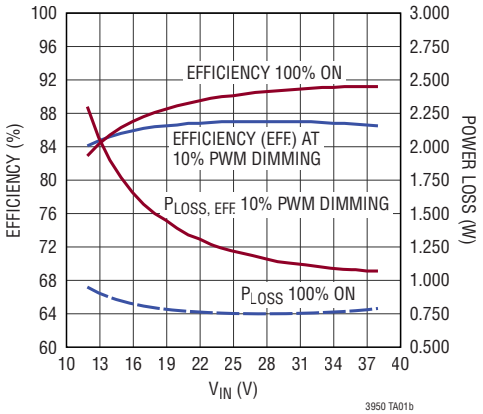
The LT®3950 is a multitopology DC/DC converter designed specifically to drive high current LEDs. It contains a 1.5A, 60V DMOS switch and supports an external PWM dimming PMOS. The LT3950 has an internal PWM generator for dimming that maps an analog control signal to an exponential scale used to define PWM dimming duty ratio. Using an exponential scale to define duty ratio preserves dimming resolution across a wide range of LED current. In addition to operating as a constant current source, the LT3950 also provides output voltage regulation. This can be used to prevent damage to the part in case of open LED events. A programmable switching frequency offers flexibility in design for higher efficiency or reduced component size. Enabling spread spectrum frequency modulation reduces EMI. The switching frequency can also easily be synchronized by driving the SYNC/SPRD pin with an external clock. LED current is programmed with a single external sense resistor and can be adjusted from zero to full-scale by an analog signal at the CTRL pin.

TYPICAL APPLICATION

10W LED Driver for Automotive, 2MHz, 90% Efficient



Efficiency and Power Loss with and without PWM Dimming

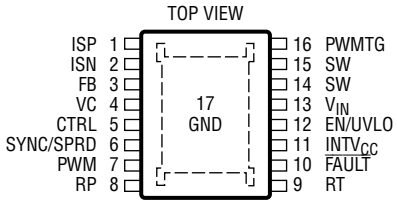


ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN}, SW, ISP, ISN, EN/UVLO, $\overline{FAULT}$ 62V
$V_{ISP} – V_{ISN}$ 2V
$INTV_{CC}$, RT, PWMTG..... (Note 2)
VC, RP..... $INTV_{CC}$ + 200mV
SYNC/SPRD, CTRL, PWM, FB 5.5V
Operating Junction Temperature (Notes 3, 5)
LT3950E ..... –40°C to 125°C
LT3950J..... –40°C to 150°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



MSE PACKAGE
16-LEAD PLASTIC MSOP
θ_{JA} = 40°C/W
EXPOSED PAD (PIN 17) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3950EMSE#PBF	LT3950EMSE#TRPBF	3950	16-Lead Plastic MSOP	–40°C to 125°C
LT3950JMSE#PBF	LT3950JMSE#TRPBF	3950	16-Lead Plastic MSOP	–40°C to 150°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. Unless otherwise noted, V_{IN} = EN/UVLO = 12V, $\overline{FAULT}$ = 100kΩ to 12V, ISP = ISN = 48V, SYNC/SPRD = 0V, CTRL = 1.5V, PWM = 3V, $INTV_{CC}$ = 1µF to GND, RT = 45.3kΩ to GND, RP = 100kΩ to GND, FB = 1V.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Supply Range		●	3		60	V
Input (V_{IN}) Quiescent Current	V_{FB} = 1.25V, Not Switching			1.8		mA
Input (V_{IN}) Shutdown Current	EN/UVLO = 0V EN/UVLO = 0.9V, CTRL = 0V			0 130	1 200	µA µA
EN/UVLO Shutdown Threshold (Falling)		●	1.15	1.25	1.35	V
EN/UVLO Rising Hysteresis	EN/UVLO Rising			32		mV
EN/UVLO Input Low Voltage	I_{VIN} < 1µA				0.4	V
EN/UVLO Pin Current (Device Off)	EN/UVLO = 1.2V			2		µA
EN/UVLO Pin Current (Device On)	EN/UVLO = 1.35V			0		µA
Internal LDO Regulator						
Internal Regulator Voltage	Not Switching, 1mA External Load	●	2.94	3	3.06	V
Line Regulation	Not Switching, 3.3V < V_{IN} < 60V			0.025		%/V
Load Regulation	Not Switching, 0.1mA < I_{LOAD} <10mA			0.05		%/mA
Max. Output Current	Not Switching, $INTV_{CC}$ = 2.8V		20			mA
Dropout Voltage	Not Switching, $INTV_{CC}$ Droop 1%, I_{LOAD} = 10mA			350		mV
LED Current Regulation (Note 4)						
ISP Common Mode Voltage Range		●	4		60	V
Current Sense Threshold (V_{ISP} – V_{ISN})	CTRL = 1.5V (100%) CTRL = 0.7V (50%) CTRL = 0.3V (10%)	● ● ●	248 121 20	250 125 25	255 129 30	mV mV mV
Current Sense Threshold (V_{ISP} – V_{ISN}) at GND	ISP = 0V			85		mV
CTRL OFF Threshold (Falling)		●	85	100	125	mV
CTRL OFF Hysteresis				35		mV
CTRL Pin Current			–100		100	nA
ISP, ISN Pin Current (Combined)	CTRL = 1.5V (Full Scale) CTRL = 0V (Stopped)			450 5		µA µA
Error Amp Transconductance				60		µS
Error Amp Output Resistance				20		MΩ
LED Voltage Regulation (Note 4)						
FB Regulation Threshold (V_{FB})		 ●	1.188 1.176	1.2 1.2	1.212 1.224	V V
FB Pin Current	Current Out of Pin			20	100	nA
ISP Voltage Regulation Threshold				60		V
FB Amplifier Transconductance				500		µS
FB Amplifier Output Resistance				20		MΩ
Oscillator						
Programmed Switching Frequency (f_{SW})	RT = 45.3k SYNC/SPRD = 0V RT = 402k SYNC/SPRD = 0V	● ●	1880 276	2000 300	2120 324	kHz kHz
Spread Spectrum Modulation Depth	SYNC/SPRD = 3V			25		%
Minimum Off Time		●	35	55	75	ns
Minimum On Time				45		ns

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. Unless otherwise noted, V_{IN} = EN/UVLO = 12V, $\overline{FAULT}$ = 100kΩ to 12V, ISP = ISN = 48V, SYNC/SPRD = 0V, CTRL = 1.5V, PWM = 3V, $INTV_{CC}$ = 1µF to GND, RT = 45.3kΩ to GND, RP = 100kΩ to GND, FB = 1V.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SYNC/SPRD Threshold (Rising)				0.85		V
SYNC/SPRD Hysteresis				50		mV
SYNC/SPRD Internal Pull-Down Resistance				100		kΩ
Minimum SYNC Pulse Width				25		ns
Power Switch						
$R_{DS(ON)}$	I_{SW} = 500mA			200		mΩ
Switch Current Limit		●	1.5	1.65	1.8	A
Switch Leakage Current	V_{SW} = 60V, EN/UVLO = 0V				3	µA
External PMOS Driver						
PWMTG ON (V_{ISP} – V_{PWMTG}) Voltage			6	7.5	9	V
PWMTG OFF (V_{ISP} – V_{PWMTG}) Voltage				0	0.3	V
Turn-on Time	C_{LOAD} = 470pF			100		ns
Turn-off Time	C_{LOAD} = 470pF			100		ns
Fault Detection and Reporting						
LED Open Threshold	V_{ISP} – V_{ISN} = 0		V_{FB} – 37mV	V_{FB} – 23mV	V_{FB} – 9mV	V
FB Overvoltage Threshold			V_{FB} + 60mV	V_{FB} + 80mV	V_{FB} + 100mV	V
FB Shorted LED Threshold				300	330	mV
Overcurrent Protection Threshold (V_{ISP} – V_{ISN})	V_{ISP} = 60V		600	700	800	mV
$\overline{FAULT}$ Pin Pull Down Current	$V_{\overline{FAULT}}$ = 0.2V, V_{FB} = 1.3V		1			mA
$\overline{FAULT}$ Pin Leakage Current	$V_{\overline{FAULT}}$ = 3V, V_{FB} = 0.7V		–100		100	nA
Internal PWM Generator						
PWM Pin Voltage for Max. Duty Ratio				1.2		V
PWM Pin Voltage for Min. Duty Ratio				0.2		V
Min. Duty Ratio	V_{PWM} = 0.2V			0.78		%
Max. Duty Ratio	V_{PWM} = 1.2V			100		%
PWM Pin Voltage Step per Duty Ratio Setting				7.8		mV
PWM Pin Current	PWM = 3V		–100		100	nA
PWM Clock Frequency	RP = 100k			400		Hz
Fraction of $INTV_{CC}$ for 10% Duty Ratio				27.2		%

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Do not apply a positive or negative voltage to $INTV_{CC}$, PWMTG, or RT pin, otherwise permanent damage may occur. Use these pins only as directed in the Pin Functions and Applications Information sections.

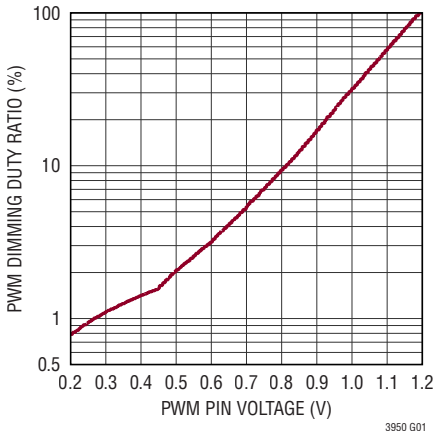
Note 3: The LT3950E is guaranteed to meet performance specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT3950J is guaranteed over the –40°C to 150°C operating junction temperature range. Operating lifetime is derated at junction temperatures greater than 125°C.

Note 4: LED Amplifier parameters measured in a servo loop with VC.

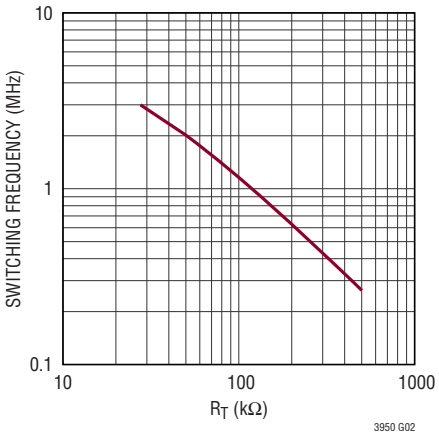
Note 5: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. The maximum rated junction temperature will be exceeded when this protection is active. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability or permanently damage the device.

TYPICAL PERFORMANCE CHARACTERISTICS

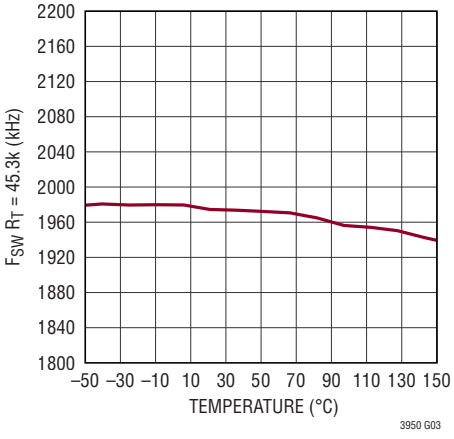
PWM Generator Duty Ratio vs PWM Pin Voltage



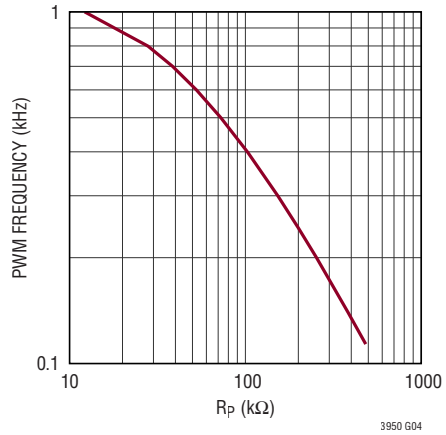
Switching Frequency vs R_T



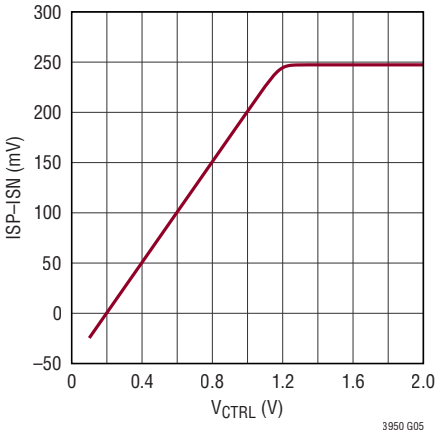
Switching Frequency vs Temperature



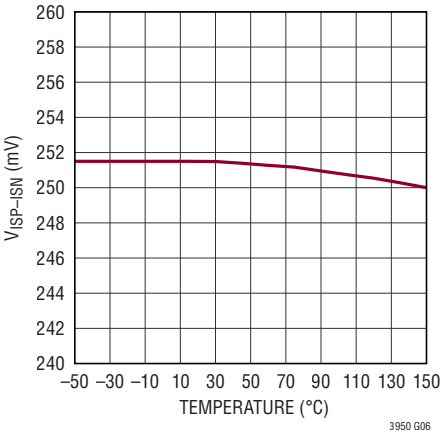
Internal PWM Frequency vs RP



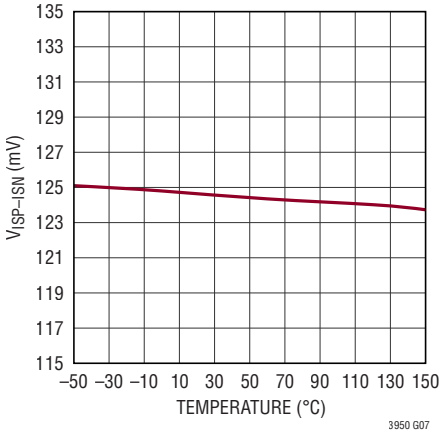
ISP–ISN Full-Scale Threshold vs CTRL Pin Voltage



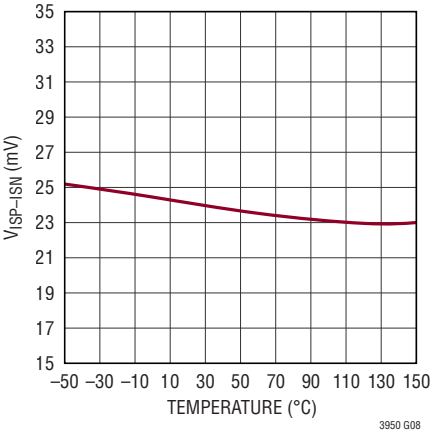
ISP–ISN Threshold (Full Scale) vs Temperature



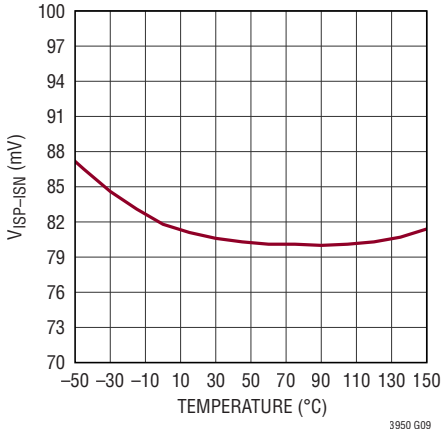
ISP–ISN Threshold (50% Scale) vs Temperature



ISP–ISN Threshold (10% Scale) vs Temperature

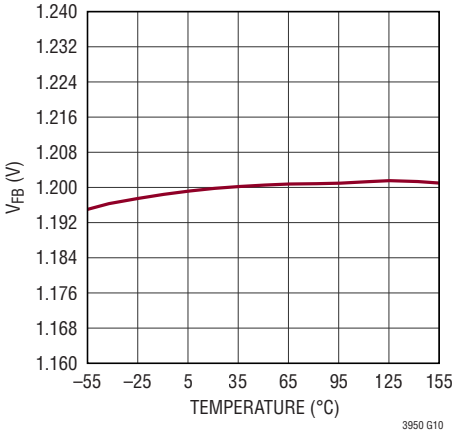


ISP–ISN Threshold (ISP = 0V) vs Temperature

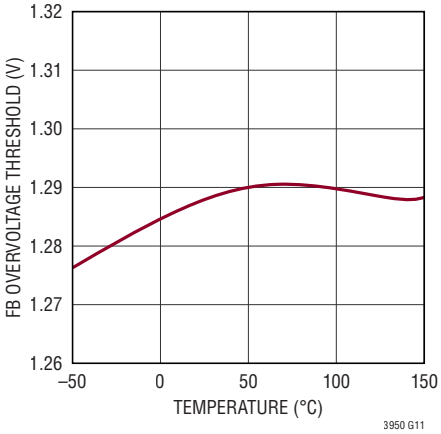


TYPICAL PERFORMANCE CHARACTERISTICS

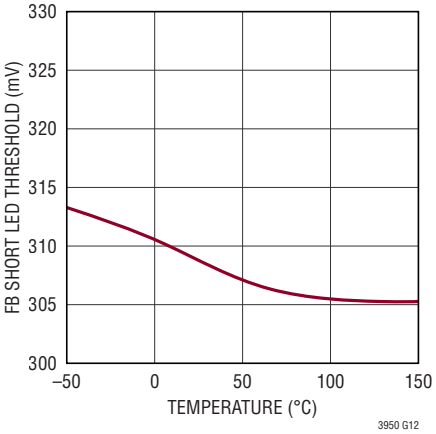
FB Regulation Voltage vs Temperature



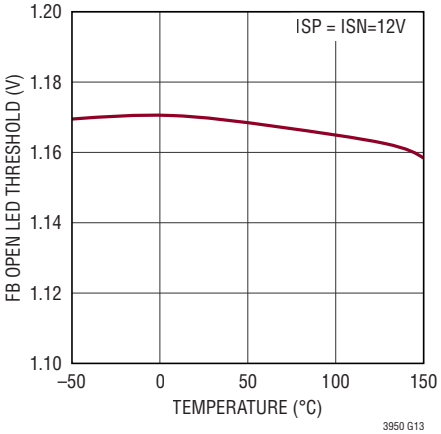
FB Overvoltage Threshold (Rising) vs Temperature



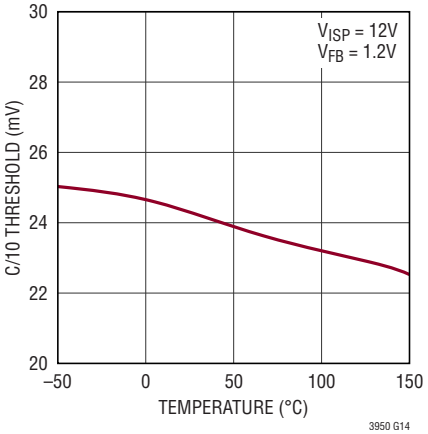
FB Short LED Threshold (Falling) vs Temperature



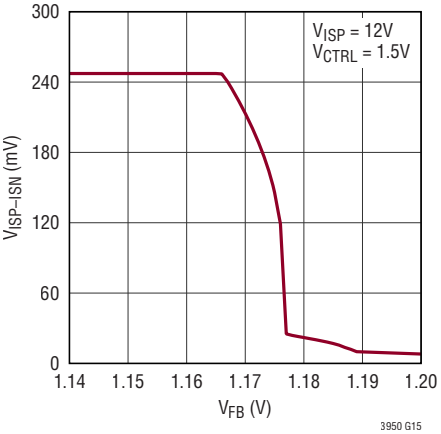
FB Open LED Threshold (Rising) vs Temperature



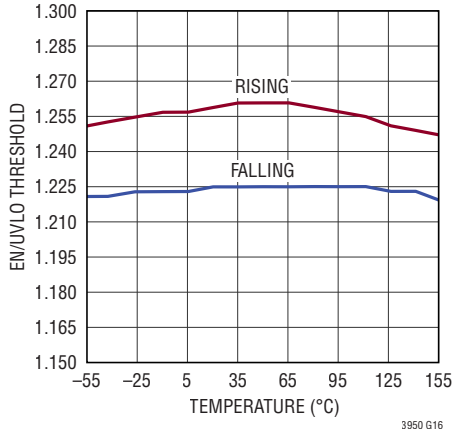
C/10 Threshold (Falling) vs Temperature



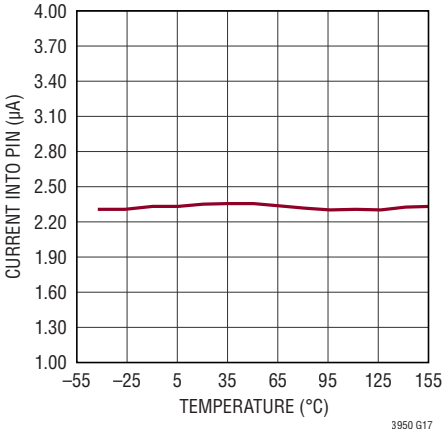
ISP–ISN Regulation Voltage vs FB Pin Voltage



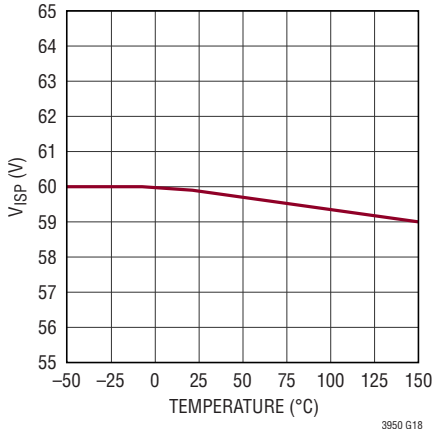
EN/UVLO Threshold vs Temperature



EN/UVLO Pin Current vs Temperature

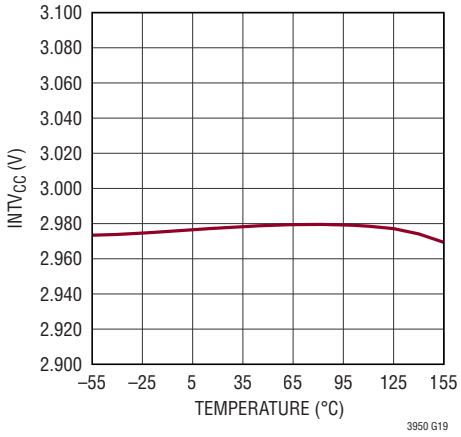


ISP Regulation Engagement Point

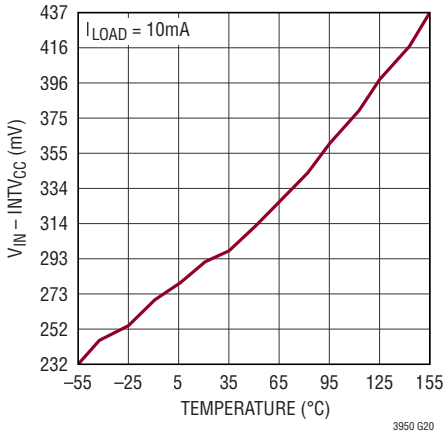


TYPICAL PERFORMANCE CHARACTERISTICS

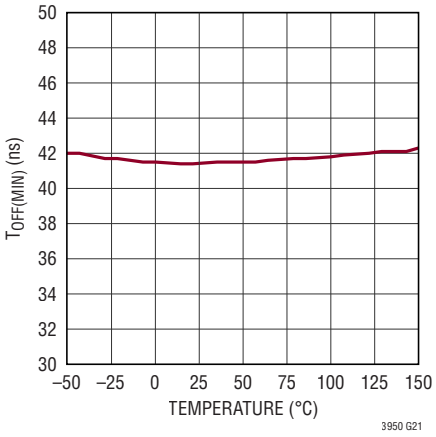
$INTV_{CC}$ Voltage vs Temperature



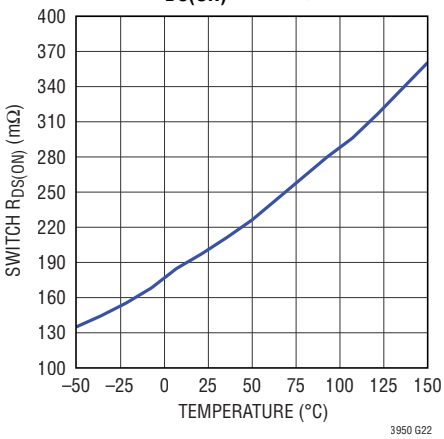
$INTV_{CC}$ Dropout vs Temperature



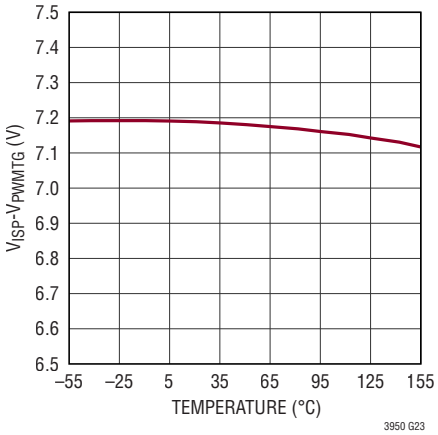
Minimum Off Time vs Temperature



Switch $R_{DS(ON)}$ vs Temperature



PWMTG On-Voltage vs Temperature



PIN FUNCTIONS

ISP: Kelvin connect this pin to the high side of the LED current feedback sense resistor. Current in the sense resistor is 250mV/ R_{SENSE} while the CTRL pin voltage exceeds 1.2V. It varies as (CTRL – 200mV)/(4 • R_{SENSE}) if the voltage at the CTRL pin is between 200mV and 1.2V.

ISN: Kelvin connect this pin to the low side of the LED current feedback sense resistor, see ISP for more details. If the voltage difference $V_{ISP} – V_{ISN}$ ever exceeds 700mV (typ.), switching stops and the part re-enters soft-start. The PWMTG pin goes high to disconnect the load, and the part signals an overcurrent event.

FB: Output Voltage Feedback Pin. This pin is used for output voltage regulation and limiting. Tie this pin to a resistive voltage divider from the output voltage. When the voltage at FB approaches 1.2V, the control loop will reduce switch current to regulate output voltage such that FB remains around 1.2V. If LED current falls below 10% (typ.) of full scale while the output voltage is in regulation, an LED Open event is signaled. If the voltage at FB exceeds 1.3V (typ.), PWMTG is driven high, switching stops, and the device signals an overvoltage event. If the voltage at FB falls below 300mV (typ.) after soft-start has finished, an LED Short event is signaled at $\overline{FAULT}$, PWMTG is driven high, switching stops and the part re-enters soft-start. See the Applications section for more info on the use of the FB pin for general applications.

CTRL: Analog Alternative to PWM Dimming. Tie to $INTV_{CC}$ to set R_{SENSE} current to full scale. Current in R_{SENSE} varies as (CTRL – 200mV)/(4 • R_{SENSE}) when the voltage at the CTRL pin varies from 200mV to 1.2V.

VC: An internal error amplifier node used for compensation. Stabilize the loop by connecting a capacitor or RC network between this pin and ground.

PWM: Pulse Width Modulation (PWM) Dimming Generator Control Pin. Connect an analog signal to this pin to use the internal exponential scale dimming PWM generator. When the voltage at this pin remains between 0.2V and 1.2V, the duty ratio of the internal PWM generator will vary with the pin voltage. A linear ramp of voltage on the PWM pin between 0.2V and 1.2V and lasting many PWM dimming cycles (set by RP) will result in an exponentially increasing PWM duty ratio. An external PWM signal can also drive this pin directly if the ON and OFF voltages are above 1.3V and below 100mV, respectively.

SYNC/SPRD: Switch Clock Synchronize / Spread Spectrum. Tie this pin to $INTV_{CC}$ to enable internal spread spectrum frequency modulation. An external clock can also drive this pin to synchronize switching. Choose RT such that the LT3950 clock would be close to the external clock, then drive this pin with that clock.

$INTV_{CC}$: Voltage Supply Used by Internal Circuitry. Tie a 1µF capacitor between this pin and ground. This pin is sometimes used as a reference voltage for other pins, however this pin is not intended for use as a power source for external loads, and connecting it to any external load may interfere with operation of the system. It is not recommended to connect $INTV_{CC}$ except as directed to LT3950.

RT: Connect a resistor between this pin and ground to set the switching frequency. Do not connect anything other than a resistor to this pin or the system may not function correctly.

RP: Connect a resistor between this pin and ground to set the PWM dimming generator frequency. Connect this pin to $INTV_{CC}$ to synchronize the PWM dimming clock to the switching clock ($f_{PWM} = f_{SW}/4096$).

$\overline{FAULT}$: Open-Drain Fault Indication Pin Indicating Short LED, Open LED, Overvoltage and Overcurrent Faults. Tie this pin through a 100k resistor to V_{IN} or $INTV_{CC}$, or use it as an open drain signal. LT3950 pulls this pin low to signal all reported fault events.

EN/UVLO: Enable/Undervoltage Lockout . When the voltage at this pin falls below 1.25V (typ.), with approximately

PIN FUNCTIONS

32mV of hysteresis when returning over 1.25V, switching stops and the part shuts down. Drive this pin high with a logic level greater than 1.4V or low with a logic level below 1V for simple ON/OFF functionality, or tie it through a resistive voltage divider to V_{IN} for a precise input undervoltage shutdown threshold.

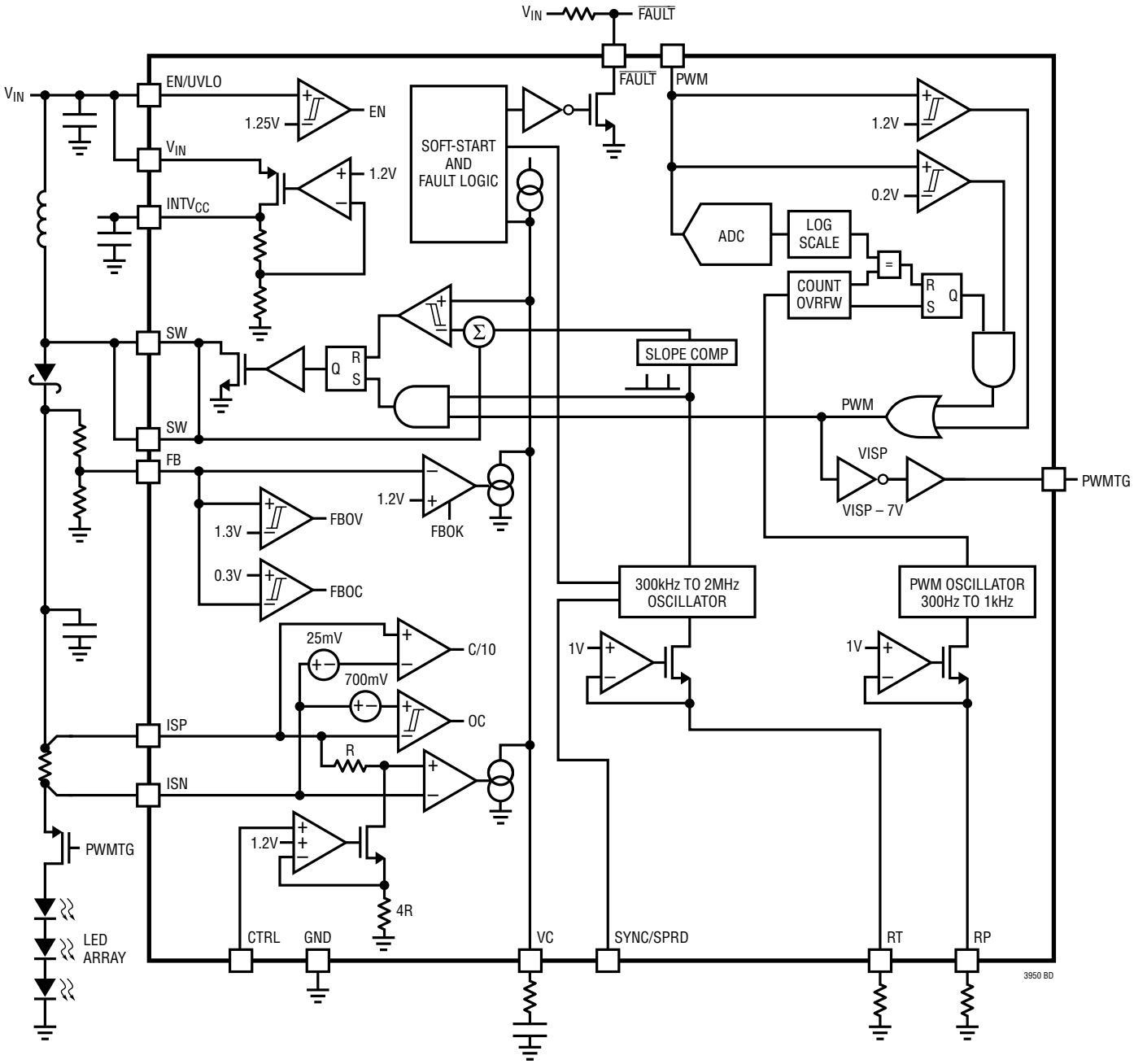
V_{IN}: Input Supply Pin. Must be locally bypassed.

PWMTG: High Side Gate Driver for External Series PMOS Switch. This pin is used to disconnect the load for PWM dimming as well as fault events. PWMTG drives the PMOS gate between V_{ISP} and V_{ISP} – 7.5V (typ.) to cut off the flow of residual charge from the output capacitor when the load should be disconnected, as well as to prevent the long transient that would result from needing to recharge the output capacitor at the end of a long PWM off period. Leave open if unused. The voltage at PWMTG is limited to 7.5V (typ.) below the voltage at ISP to protect the gate of the PMOS switch.

SW: Switch Pin. See PCB recommendations in the Applications section for details on reducing EMI.

GND (Exposed Pad): This is the ground connection. Must be soldered to PCB ground for the device to work.

BLOCK DIAGRAM



OPERATION

LT3950 is a constant-frequency, constant-current, constant voltage (CC/CV) power supply with integrated low side NMOS switch that can be configured as a boost, SEPIC, buck mode or buck-boost mode LED driver. The operation of the part can be best understood by looking at the block diagram. At the beginning of every clock cycle, the clock signal sets an SR latch controlling the switch driver. The switch turns on and connects the inductor to ground. The positive voltage drop across the inductor results in linearly increasing current in the inductor. The switch will remain on until the current comparator near the SR latch resets it. This reset will occur when the switch current exceeds the internal demand current. This demand current is determined by the error amplifier. The external LED current sense resistor used to program load current drives the error amplifier. The voltage drop across the sense resistor multiplied by the amplifier's transconductance establishes the demand current.

With no induced offset, the error amplifier would regulate the load to zero current based on the voltage across the LED current sense resistor. To establish the positive offset in the error amplifier needed to program the LED current, a small current is intentionally pulled from only one input of the amplifier through a series resistor. The CTRL pin establishes this offset current by varying the voltage dropped across a resistor to ground. These two resistors are internal to the IC. Changing the CTRL pin voltage will vary the LED current sense resistor regulation voltage between true zero and 250mV.

During constant current operation the FB pin provides overvoltage protection. While the FB pin voltage is below its regulation threshold, the FB amplifier has little effect on demand current. However, as the FB pin voltage approaches V_{FB}, the FB amplifier has an increasingly pronounced effect, until eventually it dominates the demand current. When the FB pin voltage exceeds the regulation threshold by 80mV (typ.) the $\overline{FAULT}$ pin is asserted to indicate an overvoltage event. Similarly, if the voltage at the FB pin ever falls below 300mV (typ.) (excluding start-up) then the $\overline{FAULT}$ pin is asserted to signal a shorted LED event.

In addition to regulating load current, the LED current sense amplifier also provides a digital indication of whether the load current is above or below 10% of the programmed full-scale value. If the load current drops below 10% of full-scale while the FB pin voltage is in regulation, the $\overline{FAULT}$ pin is asserted to indicate an Open LED event.

Fast overcurrent protection relies on a separate signal path than the main current sense amplifier. If the sense resistor voltage (V_{ISP}–V_{ISN}) exceeds 700mV (typ.), switching stops and the $\overline{FAULT}$ pin is asserted to indicate an overcurrent event. This event, along with Short LED, also triggers a brief interruption of switching while soft-start is reset, followed by a soft start of the switching.

Three different methods for dimming the LED load are provided with LT3950. First, the voltage at the CTRL pin, which sets the sense resistor regulation threshold, provides continuous, analog dimming of the LED load. In addition, two method of PWM dimming exist. The first, external PWM, relies on a user-provided PWM signal. This signal drives the PWM pin directly, causing the system to turn off and on (meaning stop and start switching, and also disconnect and reconnect the LED load to the output capacitor via PWMTG) based on the duty ratio of the PWM pin voltage. Alternatively, internal PWM dimming is available.

Internal PWM dimming uses an internal analog-to-digital converter to translate the voltage at the PWM pin to a 7-bit digital representation. This conversion uses a linear scale; every 7.8mV (typ.) the 7-bit value changes. Each particular value corresponds to a unique duty ratio that is separated exponentially from its neighbors. For example, moving by 7.8mV (typ.) near the 10% duty ratio region can result in a change from 9.6% to 10% duty ratio. Moving by the same difference, 7.8mV (typ.) near the 100% region can change the duty ratio from 96% to 100%. A smooth ramp at the PWM pin lasting many PWMTG dimming periods as set by RP will create an exponentially increasing PWM duty ratio for the LED load. This preserves dimming accuracy and resolution across a wide range of PWM dimming duty ratios.

APPLICATIONS INFORMATION

Introduction

LT3950 provides a variety of features to enable a wide range of application options. Due to the small package size and pin count, many pins perform more than one function. The simplest LT3950 application is realizable in only a few off-chip components and with very few design choices on the part of the user. To fully utilize the capability of the part, however, requires a good understanding of how the individual features play together. The detailed explanations of each feature below along with several example application circuits will help with developing a good understanding of the part.

Programming the LED Current

Full-scale current through the LED string is easily programmed using a single resistor (R_{SENSE}) connected in series with the LED string. The sense resistor should be placed on the high side of the LED string, and Kelvin connected to sense pins ISP and ISN. The loop will regulate a drop of 250mV across this sense resistor, scaled by the voltage at the CTRL pin, discussed later. A half-Watt resistor will usually be sufficient. Since the loop regulates the voltage across R_{SENSE}, typical full-scale load current (I_{FS}) is defined as

$$I_{FS} = \frac{1}{4R_{SENSE}} A$$

For the best performance and protection, sense at the highest potential in the LED string, and tie the source of the external PWM dimming PMOS to ISN. More details on the PWM dimming PMOS will be discussed later. Note that the loop is able to regulate LED current down to ISP = 0V, but a ground sensing configuration is not desirable. For more information see the Low Voltage (SEPIC) Startup section.

Adjusting LED Current with the CTRL Pin

The CTRL pin provides an analog alternative to PWM dimming. The value of the voltage regulated across the sense resistor can be adjusted with the CTRL pin. As the voltage present at this pin varies from 200mV to 1.2V, the regulated voltage drop across the sense resistor varies from 0V to 250mV. The system will supply no current if the CTRL pin voltage falls below 200mV, and will continue to supply full-scale current after the voltage at the CTRL pin exceeds 1.2V, all the way up to $INTV_{CC}$. Total LED current (I_{LED}), taking the effects of the CTRL pin into account is then:

$$I_{LED} = \frac{V_{CTRL} - 0.2V}{4R_{SENSE}} A,\ 0.2V < V_{CTRL} \leq 1.2V$$

Note the CTRL pin can also be used for PWM by driving it with a digital signal whose low value is below 100mV and whose high value is above 1.3V. This technique for PWM dimming will not allow very high frequency PWM signals. The frequency of PWM driving the CTRL pin should be below 1kHz. For higher frequency PWM, use the PWM pin, discussed later. A graphical depiction of the full range of CTRL pin voltage appears below.

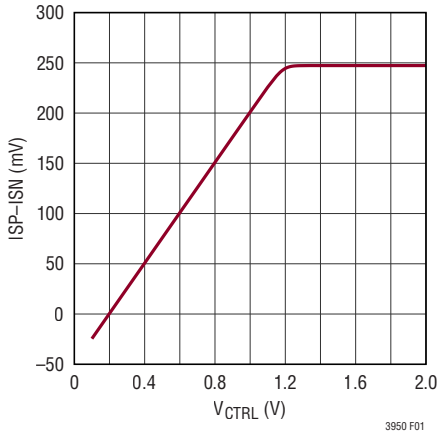


Figure 1. $V_{ISP-ISN}$ vs CTRL Pin Voltage

Setting the Output Regulation Voltage

In addition to output current regulation, LT3950 can also provide output voltage regulation. The loop will go into voltage regulation mode when the voltage at the FB pin approaches 1.2V. Regulating output voltage will reduce LED current below its programmed value. Voltage regulation mode is primarily included as a safety feature, allowing the part to gracefully manage Open LED and similar events.

To set the output regulation voltage, connect a resistive voltage divider from the output voltage to FB as shown below. Choose R_{FB1} and R_{FB2} to set the output voltage:

APPLICATIONS INFORMATION

$$V_{OUT} = \left(1 + \frac{R_{FB1}}{R_{FB2}}\right) \bullet 1.2V$$

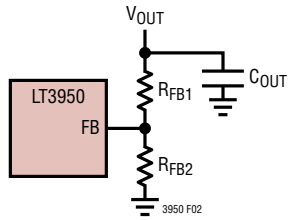


Figure 2. Voltage Feedback Network

It is important that the divider be Kelvin connected to the output capacitor. The resistors R_{FB1} and R_{FB2} should be chosen such that their total value is between 1k and 1M. For high dynamic range (>10,000:1) PWM dimming, a total resistance of up to 10M may be appropriate. If the part is regulating output voltage and the current drops below 10% of full-scale, an open LED event will be signaled at the $\overline{FAULT}$ pin.

In some configurations, such as buck mode, where the load voltage is not directly referred to ground, a level shifter may be needed to use constant voltage mode control. An example circuit to accomplish output voltage control for buck mode and buck-boost mode topologies is shown below.

$$V_{OUT} = 2 \bullet \left(V_{BE} + 1.2 \frac{R_{FB1}}{R_{FB2}}\right)$$

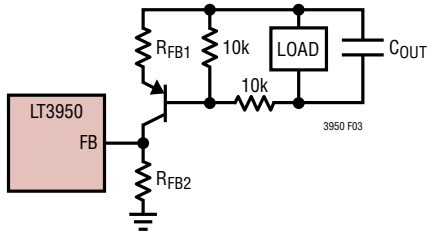


Figure 3. Voltage Feedback Network with Level Shifter

FB Overvoltage Lockout

As part of the safety feature offered by output voltage regulation, if the voltage at the FB pin reaches or exceeds 1.3V (typ.), switching stops, PWMTG pulls high to turn off the disconnect PMOS, and the device reports a fault at the $\overline{FAULT}$ pin.

Setting Switching and PWM Dimming Generator Frequency

To program the switching frequency of LT3950, simply connect a single resistor to ground from the RT pin. The table below includes several common R_T resistor values and corresponding switching frequency. It is important to connect nothing to the RT pin except this resistor.

Table 1. Selected R_T Values and Switching Frequency

R_T Value (kΩ)	Switching Frequency (MHz)
402	0.3
301	0.4
237	0.5
191	0.6
162	0.7
140	0.8
121	0.9
107	1
97.6	1.1
80.6	1.2
76.8	1.3
73.2	1.4
66.5	1.5
61.9	1.6
57.6	1.7
52.3	1.8
48.7	1.9
45.3	2

During start-up, the switching frequency is reduced to allow sufficient switch OFF time, especially for 2MHz operation, so that inductor current can ramp below current limit when there is minimal voltage across the inductor during the OFF time. This condition is encountered at start-up or after faults, when the output is still low. During start-up, or when restarting after faults, switching frequency will drop to around 40% of its nominal value, and step up every 16 cycles. For more information about this, see the section concerning soft-start.

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The PWM dimming generator clock offers two programming options. For a separate, free-running clock with respect to the switching frequency, connect a resistor from the RP pin to ground. Similar to the RT pin, the RP pin sets the frequency of PWM dimming as a function of resistance.

Table 2. Selected R_P Values and PWM Dimming Frequency

R_P Value (kΩ)	PWM Dimming Frequency (Hz)
634	100
274	200
162	300
107	400
75	500

Alternatively, the PWM dimming clock can lock to the switching clock. To do this, simply tie the RP pin to $INTV_{CC}$. In this mode, the PWM clock will be the switching clock divided by 4096.

Pulse Width Modulation (PWM) Dimming

Pulse width modulation (PWM) allows high dynamic range dimming of the LED load. When using PWM dimming, a pulse train with duty ratio proportional to desired LED current controls the load. During ON periods, the part operates normally. During OFF periods the part stops switching. While the part is not switching, the compensation node is high impedance to minimize changes to the compensation capacitor voltage. This reduces transient settling time when the next ON period arrives. In addition to this, LT3950 provides an optional load disconnect. Disconnecting the load makes turn-off much faster, as the output capacitor does not continue to conduct current into the load. Transient settling time is also shorter when turning back on, as the output capacitor's state is less affected by the load.

To use the external load disconnect, tie a PMOS in series with the load such that the source of the PMOS connects to the ISN node, and the drain to the LED load. Connect the gate of the PMOS to the PWMTG pin. The voltage at the PWMTG pin will vary between V_{ISP} and V_{ISP} – 7.5V to turn the PMOS off and on. Note that this configuration works for any of the supported power stage topologies. For more information on power stage topologies, see the example application circuits.

The PWM pin allows two modes of PWM dimming. The first mode is external PWM. In this mode, a digital signal created by some other device, such as a microprocessor, drives the PWM pin. This PWM signal directly controls the part: when this signal is high, the part runs, when this signal is low, the part does not run, and disconnects the load if an external PMOS is used. Tying the PWM pin to $INTV_{CC}$ results in continuous, uninterrupted operation. Conversely, tying the PWM pin to ground results in the system remaining idle indefinitely. For ON time < 1µs, use a low Q_G (<10nC) MOSFET and low or zero value for R_C at VC pin. External PWM supports dimming dynamic range up to 20,000:1.

The second mode of PWM dimming is internal. When using internal PWM dimming, the analog voltage at the PWM pin controls the duty ratio of the PWMTG signal. The voltage range for internal PWM dimming is from 0.2V to 1.2V at the PWM pin. The internal PWM generator converts the voltage at the PWM pin to a 7-bit digital representation. The analog to digital converter responsible for this uses a linear scale, each code is around 7.8mV wide. Each 7-bit code corresponds to a unique duty ratio value. The values of duty ratio are separated exponentially. Another way to phrase it is that each time the 7-bit code increases in value by 1, the duty ratio is multiplied by a constant scaling factor. A log-scale plot of duty ratio vs PWM pin voltage appears below.

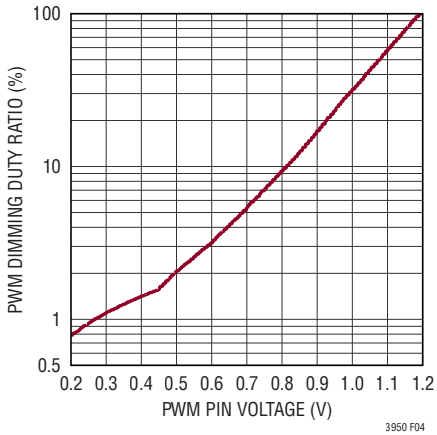

Figure 4. PWM Duty Ratio

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Synchronizing the Switching Frequency

To synchronize LT3950 to an external clock, simply drive the SYNC/SPRD pin with that clock signal. Choose the RT resistor such that the system's internal clock would be within 10% of the external clock frequency. It is best to have the RT programmed frequency as close as possible to the external clock frequency.

Spread Spectrum Frequency Modulation

Like all switching converters, LT3950 does produce some electromagnetic interference (EMI). Enabling spread spectrum frequency modulation can significantly attenuate this interference. Conditions such as switching frequency and printed circuit board (PCB) geometry affect the amount of attenuation achievable with spread spectrum frequency modulation. A variety of industry-standard tests exist to quantify these effects.

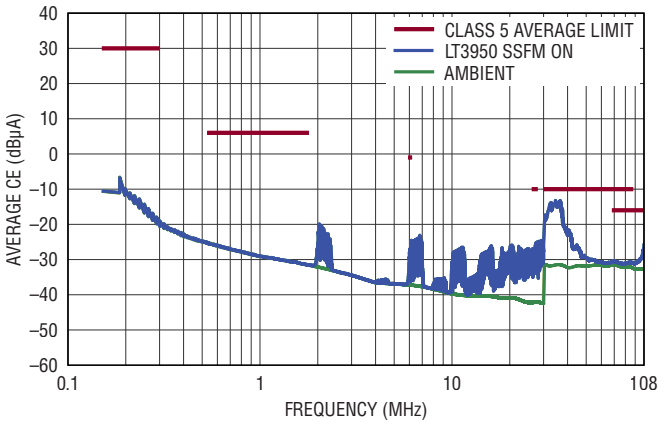
To enable internal spread spectrum frequency modulation, tie the SYNC/SPRD pin to $INTV_{CC}$. The modulating waveform is a triangle wave with steps at the positive and negative peaks. The modulation frequency is around 9kHz, and the switching frequency range is from 100-125% of the programmed value. Typical LT3950 EMI results are shown in Figure 5.

Maximum Duty Ratio

Since LT3950 uses a switch to connect an inductor from V_{IN} to ground, having a duty ratio of 100% would result in zero current flowing to the load. To prevent this situation, the part enforces a minimum off time. During this time, irrespective of load or demand, the switch turns off and allows the inductor current to flow into the load. The duty ratio can, therefore, never reach 100%. The maximum duty ratio varies with frequency. For the same minimum off time, a higher frequency signal will have a smaller maximum duty ratio. At lower frequencies in boost configuration and in Continuous Conduction Mode (CCM), the part can reach a duty ratio of 95% (that is, V_{ISP}/V_{IN} = 60/3, the maximum range for the part). However at higher frequencies, such as 2MHz, the part has a maximum duty ratio of around 90%. Maximum duty ratio at any frequency in CCM is given by the following relationship.

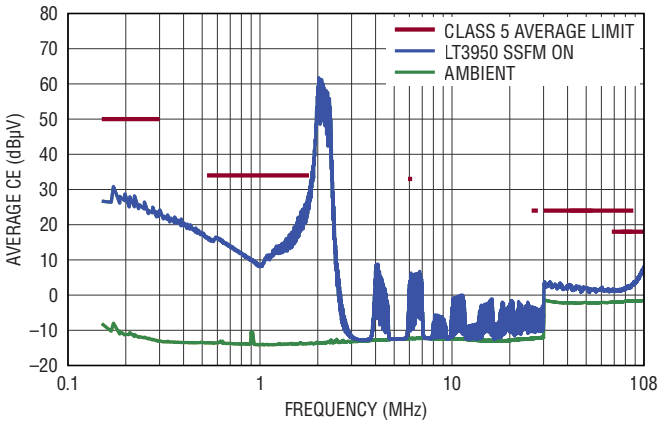
$$D_{MAX} = 1 - f_{SW} \bullet 50ns$$

CISPR25 Conducted EMI Performance Current Method



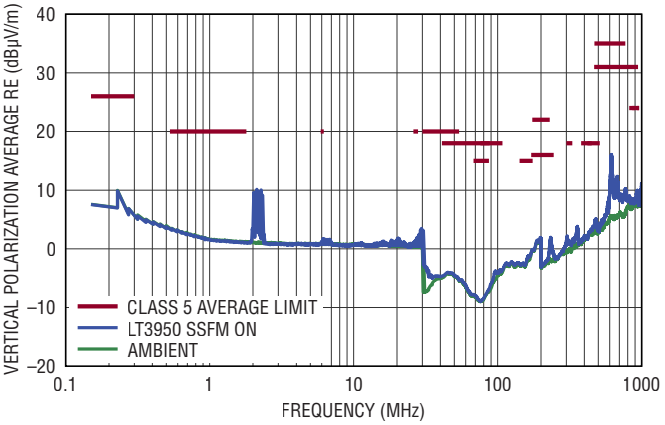
(a)

CISPR25 Conducted EMI Performance Voltage Method



(b)

CISPR25 Radiated EMI Performance



(c)

Figure 5. LT3950 Typical EMI (V_{IN} = 12V, V_{LED} = 25V, I_{LED} = 330mA, 2MHz)

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Maximum Switch and Load Current

An important system parameter is the current limit. This can prevent damage to the switch and external components by limiting the maximum instantaneous current conducting through the power switch. In a well-designed system, there will be margin between the maximum switch current to drive the LED load and the switch current limit. The LT3950 offers a current limit that does not change with duty ratio and also has sufficient slope compensation so that reaching the current limit during line and load transients does not result in subharmonic oscillations. A good rule of thumb for setting maximum LED current for boost and buck-boost power stages appears below. This equation assumes that the inductor selection used limits current ripple to around 30% of average current. For more information on inductor selection, see the External Component Selection section.

$$I_{LED,MAX(30\%ripple)} \approx 1.4A \bullet \frac{V_{IN}}{V_{ISP}}$$

In the boost and buck-boost mode topologies, average switch current is related to average LED current by the ratio of V_{IN} to V_{ISP}. In the buck topology, average LED current approximately equals average inductor current. For this reason the buck topology provides the highest possible LED current capability. The peak instantaneous switch current is thus the average LED current plus half of the peak to peak ripple current. This leads to the following result for buck mode current limit.

$$I_{LED,MAX(BUCK)} = 1.4A$$

For more information about power stage topologies, review the example application circuits included below.

Loop Compensation

Loop compensation normally will take the form of an RC network connected between the VC pin and ground. A single capacitor can fulfill stability requirements if PCB area is extremely limited. The addition of a series resistor, however, will increase response speed and can also recover phase margin. A schematic diagram of the typical compensation scheme is illustrated below.

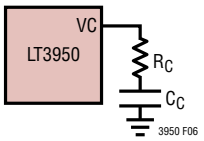

Figure 6. Typical Compensation

For many cases, a 1nF capacitor and 10kΩ resistor will suffice. This is a good place to start for all applications. If settling time is unacceptable, ringing is too large, or the loop remains unstable, the information below can help.

First, try reducing or eliminating the compensation resistor, R_C, especially if transient response is ringing or underdamped. Reducing the compensation resistor will cause longer settling time and larger deviation from load steps such as PWM dimming.

Next, increase the size of the compensation capacitor, C_C. This will reduce the frequency of the dominant (low frequency) pole and thereby the unity gain frequency. It will usually be possible to stabilize the loop given a big enough compensation capacitor. Increasing the compensation capacitor slows down the transient response to line and load activity. If the compensation capacitor cannot change by a small amount to achieve stability, consider instead increasing the output capacitor or decreasing the inductor to separate the load pole and right half plane zero.

EXTERNAL COMPONENT SELECTION

Input and Output Capacitor Selection

The input and output capacitors supply the transient current for the power stage and should be placed and chosen according to the transient current requirements. An X7R type ceramic capacitor is usually a good choice for both input and output capacitor. Even though X7R has less variation with temperature and DC bias voltage than many other materials, the effect of capacitance derating with voltage stress must be considered. It is generally a good rule of thumb to pick capacitors with a voltage rating about 60% higher than the application demands.

The switching frequency, output current, inductor ripple current, and tolerable input voltage ripple are key parameters to consider when determining the value of the input capacitor. Typically, boost, buck-boost mode, and SEPIC

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converters require a lower value input capacitor than buck mode converters. Use the following equations to estimate the value of the input capacitor. If the inductor is selected according to the directions in the Inductor Selection section, use the value 15% for the quantity $i_{L(RIPPLE)}/i_{L(DC)}$ in the following equation, otherwise use the fraction of average inductor current representing half of the peak to peak ripple current:

$$C_{IN(BOOST)} > \frac{i_{LED} t_{SW} \frac{i_{L(RIPPLE)}}{i_{L(DC)}} \frac{V_{LED(MAX)}}{V_{IN(MIN)}}}{\Delta V_{IN(MAX)}}$$

For a boost converter switching at 2MHz, a 2.2µF input capacitor will often suffice.

$$C_{IN(BUCK)} > \frac{i_{LED} t_{SW}}{\Delta V_{IN(MAX)}}$$

For the buck case at 2MHz, a 2.2µF input capacitor would be appropriate to ensure less than 100mV of input voltage ripple with i_{LED} = 0.3A. Additional margin is recommended (e.g., the 1.5µF result of evaluating the above equation may lead to selection of a 2.2µF input capacitor).

In the buck mode configuration, the input capacitor has large pulsed currents due to the current returned through the Schottky diode when the switch is off. In the buck converter case it is important to place the capacitor as close as possible to the Schottky diode and to the exposed pad of the IC. It is also important to consider the ripple current rating of the capacitor. For best reliability, this capacitor should have low ESR and ESL and have an adequate ripple current rating. Use the following equation to estimate the RMS input capacitor current for the buck converter case.

$$i_{CIN(RMS)} = i_{LED} \bullet \sqrt{\frac{V_{LED}}{V_{IN}} \left(1 - \frac{V_{LED}}{V_{IN}}\right)}$$

The selection of the output capacitor depends on load and power stage configuration. For example, a boost or buck-boost mode converter will require a much larger output capacitor than a buck mode converter for the same conditions. The boost and buck-boost mode configurations will also require similar low ESR and low ESL capacitors like the input capacitor of the buck mode case. Capacitor values will increase proportionally with decreasing switching frequency for the same ripple voltage. The equivalent resistance presented by an LED load is typically low, so larger capacitors may be needed to further reduce voltage ripple. It is likely that the appropriate output capacitor value will fall between 2.2µF and 47µF. Use the example applications as a starting point for output capacitor selection. Sources of quality ceramic capacitors are listed in Table 3.

Table 3. Capacitor Manufacturers

MANUFACTURER	WEBSITE
MURATA	www.murata.com
TDK	www.tdk.com
KEMET	www.kemet.com
TAIYO YUDEN	www.t-yuden.com
AVX	www.avx.com

Schottky Rectifier Selection

Choose a Schottky diode with reverse breakdown voltage rating at or above 60V and with average forward current rating greater than the programmed LED current with some margin. It is best to find a rectifier with low equivalent capacitance, around or below 350pF. Large equivalent capacitance and/or poor PCB layout can negatively interact with certain EMI mitigating features in LT3950. Pay attention to reverse leakage current if the part is to be used in low frequency PWM dimming (<200Hz) situations. The reverse leakage current can discharge the output capacitor. This can lead to lengthy turn-on transient effects that degrade maximum PWM dimming dynamic range. Note that reverse leakage current increases with temperature. For many LT3950 applications, the NXP PMEG6020 will suffice. Table 4 has some recommend component vendors.

Table 4. Schottky Rectifier Manufaturers

VENDOR	WEBSITE
ON Semiconductor	www.onsemi.com
Diodes, Inc.	www.diodes.com
Central Semiconductor	www.centralsemi.com
NXP	www.nxp.com

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Inductor Selection

Select an inductor for use with LT3950 that has a saturation current rating greater than 1.7A, additional margin is recommended. Choose the inductor value based on desired ripple current given input and output voltage and switching frequency. Use the equations below to select an inductor with around 30% peak to peak ripple.

$$L_{BOOST} > \frac{t_{SW} V_{IN}^2}{0.3 i_{LED} V_{LED}} \left(1 - \frac{V_{IN}}{V_{LED}}\right)$$

$$L_{BUCK} > \frac{t_{SW} V_{LED}}{0.3 i_{LED}} \left(1 - \frac{V_{LED}}{V_{IN}}\right)$$

Table 5. Inductor Manufacturers

VENDOR	WEBSITE
Sumida	www.sumida.com
Wurth Elektronik	www.we-online.com
Coiltronics	www.cooperet.com
Vishay	www.vishay.com
Coilcraft	www.coilcraft.com

Power PMOS Selection

For the PMOS to be used with PWMTG, select a device with drain-source voltage rating higher than 65V, additional margin is recommended. The gate-source voltage rating should be higher than 10V. The drain current rating should be sufficient to conduct the full programmed LED current with some margin. Ensure that the PWMTG drive voltage of 7.5V will fully enhance the PMOS device. Be careful when selecting a PMOS to consider the effect that higher current ratings have on gate charge (Q_g). A high Q_g (>20nC) PMOS will slow turn-on and turn-off time, which can reduce maximum PWM dimming dynamic range.

LED Fault Events

LT3950 provides a variety of fault detection and reporting functions to aid larger systems in responding to failures. While LT3950 has many self-protection features, only four types of faults will be reported to the outside world. Of these, three (LED Short, Overvoltage and Overcurrent) will cause the part to stop switching and, if an external PMOS is used according to instructions in the PWM Dimming section, disconnect the load from the output capacitor. The $\overline{FAULT}$ pin will be asserted. The part will not wait until the end of the clock cycle to take this action. The LED Open fault will only result in the $\overline{FAULT}$ pin being asserted; switching will continue as normal. A summary table of each type of fault appears at the end of this section.

Overcurrent fault detection uses the current programming sense resistor. If the voltage drop across the sense resistor is greater than 700mV (typ.), an overcurrent event is reported.

While overcurrent senses the actual current into the load, the LED Short fault senses load voltage. This can allow the detection of limited failures, such as one or two of the LEDs in a string becoming shorted. LT3950 senses the voltage at the FB pin and reports an LED Short fault if that voltage falls below 300mV (excluding during start-up). It is important to note that the FB resistor divider must be in place to use the LED Short fault detection.

To report an LED Open fault, the voltage at the FB pin must approach 1.2V while the load current falls below 10% of full-scale. It is important to note that the FB resistor divider must be in place to use the LED Open fault detection.

The Overvoltage fault occurs when the voltage at the FB pin exceeds 1.3V. Like the LED Open fault, the FB resistor divider must be in place to take advantage of the over voltage fault protection.

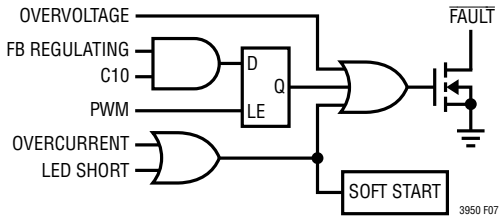

Figure 7. Fault Logic

All four types of faults result in the $\overline{FAULT}$ pull down turning on. Since the $\overline{FAULT}$ pin has an open-drain output, connecting a resistor from $\overline{FAULT}$ to $INTV_{CC}$, V_{IN}, or an external supply is required for operation. The open-drain output allows flexibility such as the ability to wire-OR many parts together to detect faults on an array of devices with a single digital I/O pin.

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Excepting LED Open, all reported faults will result in interruption of switching. The Short LED and Overcurrent faults trigger a cooldown period, after which the system will enter soft-start as if it had just been turned on via the EN/UVLO pin. Upon successful completion of the soft-start process with no faults, the $\overline{FAULT}$ signal will be de-asserted. During soft-start, the PWM Dimming logic low state is ignored for both internal and external PWM until soft start is complete or current in the LED reaches 10% of full scale value.

Table 6.

CONDITION (TYP.)	TYPE OF FAULT
FB Pin >1.3V	Overvoltage
1.17V < FB pin < 1.3V and $V_{ISP-ISN}$ < 25mV	Open LED
FB pin < 300mV	Short LED
$V_{ISP-ISN}$ > ~700mV	Overcurrent

Soft Start

To prevent a surge of current at start-up, LT3950 uses an internal soft-start. This feature affects both current limit and switching frequency. At start-up, the system will switch at around 40% f_{SW} with near zero current limit. As the clock runs, both constraints relax, leading to normal operation after ~1800 • $T_{SW(NOM)}$. Note that this process does not take 1800 cycles to complete, rather the above number takes into account the reduction in clock frequency enforced by the soft-start feature. In total, 1,024 cycles are spent in soft-start, with f_{SW} adjustments every 16 cycles.

The cooldown period triggered by certain faults discussed in the LED Faults Section lasts for at least 32,768 • $T_{SW(NOM)}$. At the end of the cooldown period, the system attempts to start again, and enters soft-start as if it had just been powered on for the first time.

Regardless of whether it is the first-time soft-start or a soft-start resulting from a fault condition, the LT3950 will wait until the first PWM dimming pulse arrives before beginning to power on the system. This PWM pulse can be from an external source or from the internal dimming PWM generator. At the arrival of the first PWM pulse, soft-start begins and operation continues until the system has reached steady state. Until the system either finishes soft-start or observes at least 10% of full-scale current flowing through the sense resistor, the PWM low logic state is ignored and the part runs continuously. If any fault condition caused the part to re-enter soft-start, the $\overline{FAULT}$ pin will remain asserted until the part successfully completes the soft-start process.

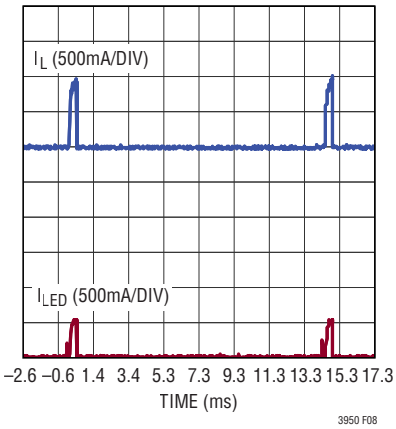


Figure 8. LED Short Hiccup Mode

Using the EN/UVLO Pin

The EN/UVLO pin offers two modes of operation. First, it can be driven high (above 1.4V) or low (below 1V) to act as an enable pin, turning the part on and off. In addition to this, the pin can also be used to create an accurate external under voltage lockout (UVLO). To use this feature, connect the EN/UVLO pin to a resistive voltage divider from the V_{IN} pin to ground. Select resistors to program the desired minimum V_{IN} value for operation.

$$V_{IN(FALLING)} = 1.25V \bullet \left(1 + \frac{R_{UV1}}{R_{UV2}}\right)$$

$$V_{IN(RISING)} = 1.28V \bullet \left(1 + \frac{R_{UV1}}{R_{UV2}}\right) + 2\mu A \bullet R_{UV1}$$

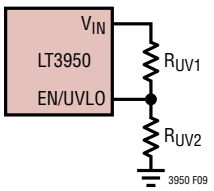


Figure 9. Programming V_{IN} Undervoltage Setpoint

APPLICATIONS INFORMATION

The EN/UVLO threshold has a hysteretic window to prevent oscillating between the ON and OFF states. When the EN/UVLO pin falls below its falling threshold (1.25V typ.), switching stops, soft-start is reset, and if an external PMOS is used according to instructions in the PWM Dimming section, the load is disconnected from the output capacitor.

Low Voltage (SEPIC) Startup

Certain power stage topologies, such as the SEPIC, may require the part to start up in the condition where ISP and ISN are both near (or at) 0V. This condition is handled differently than steady-state operation. Below around 2.5V at ISN, the part does not use the programmed offset defined by the CTRL pin, but instead uses a constant offset of around 85mV (typ.) across ISP and ISN. This ensures that the part starts in a reasonable amount of time. When ISN < 2.5V (typ), LED Open and LED Short faults are disabled. The ability of the error amplifier to tolerate an input common mode voltage of 0V should not lead the user to consider low-side sensing. Not only is the LED current sense amplifier most accurate above 4V on ISN, but also recall that ISP provides the positive rail for the driver of the external disconnect PMOS. Therefore the use of low side sensing of LED current is not recommended. Full-scale threshold accuracy is derated when V_{ISN} < 4V.

Planning for Thermal Shutdown

The LT3950 will automatically shut down when the internal temperature is above 170°C. This shutdown is guaranteed to always be outside of the operating region of the device. The effects of thermal shutdown are similar to that of certain load faults: switching stops, soft-start is reset, and if an external PMOS is used according to instructions in the PWM Dimming section, the load is disconnected from the output capacitor.

The exposed pad of LT3950 is ground, and must be soldered to a good, large ground plane with many vias to aid in thermal management. A simple electrical connection is not sufficient for high-power operation, good thermal conductivity is critical.

PCB Layout Guidelines and Information

Printed Circuit Board (PCB) layout profoundly affects performance of all power applications. Proper electrical and thermal connection between the IC and outside world will make or break any system. Do not neglect the thoughtful and detailed layout of any application PCB.

The exposed ground pad on the bottom of the package is the only path to ground for the IC, and it will not work correctly unless the exposed pad has a good, high-quality solder connection to a ground plane. The ground connection for analog functions such as RT, the compensation network, and any voltage dividers for PWM or CTRL should be Kelvin connected to the exposed pad. A separate power ground should exist for the input and output capacitors and LED load. If possible, the $INTV_{CC}$ bypass capacitor should have its own ground.

Proper power and ground planes provide both electrical and thermal connections between the IC and the outside world. It is imperative that at least one ground plane be present in any application of LT3950. Ground planes should not be interrupted by other traces, and should be continuous, very wide sheets of copper. If components connect to the ground plane by way of vias, use filled vias if possible. Connect the exposed pad of the IC to such a ground plane. Use as many vias as will fit in the exposed pad area to make the connection. Use filled vias if possible. Do not copy any particular layout for the exposed pad connection, but instead use as many vias as will fit given the capabilities of the PCB manufacturer.

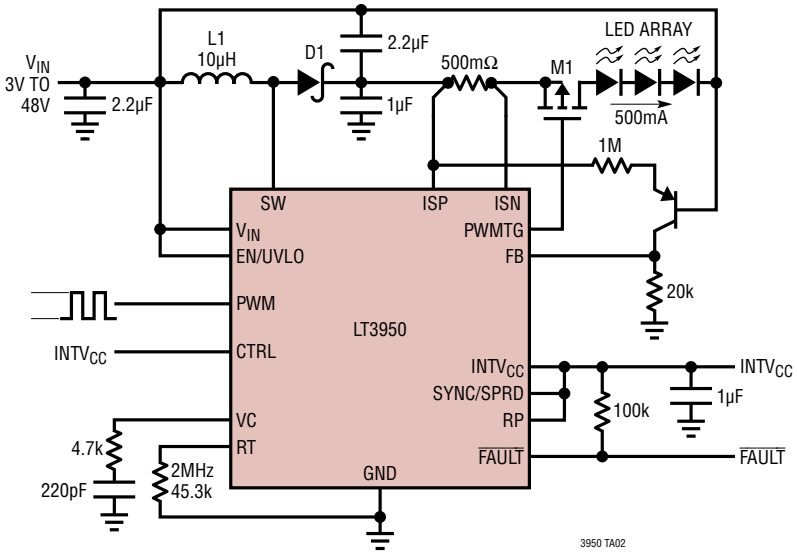
In addition to soldering down the exposed pad, it is critical to provide a good, robust layout for the rest of the power path. Use wide traces for V_{IN} and to connect to the load. Keep the sense resistor very close to the IC, and ensure that the ISP and ISN traces run as close to one another as possible. It is strongly recommended to not allow ISP and ISN to take different paths to the sense resistor, but instead to keep them beside one another as much as possible. Minimize the total area of any SW node traces; keep the output capacitor and external catch diode as close as possible to the IC to help this. Finally, use wide traces to

connect to the external PMOS switch, if used. Note, however, that the gate of the external PMOS should be connected by a narrow trace. Except for the external PMOS gate, avoid vias where possible in the power path. If vias are truly unavoidable, use many (more than 10) in parallel.

Despite the techniques used in the design of LT3950 to mitigate electromagnetic interference (EMI), proper PCB layout is critical for suppressing radiated and conducted noise. Minimizing the area of the SW node will decrease the amount of capacitance that the switch sees, and thus reduce the current spike seen during switching events. Failing to minimize the area of the so-called hot loop will dramatically degrade EMI performance. Keep the output capacitor and catch diode as close as possible to the SW pin of the IC to minimize the hot loop. For more information about hot loops see Analog Devices Application Notes AN136 and AN139.

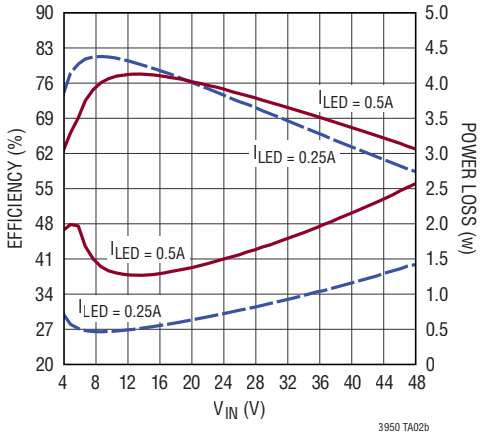
TYPICAL APPLICATIONS

5W Buck-Boost Mode LED Driver with Spread Spectrum Frequency Modulation



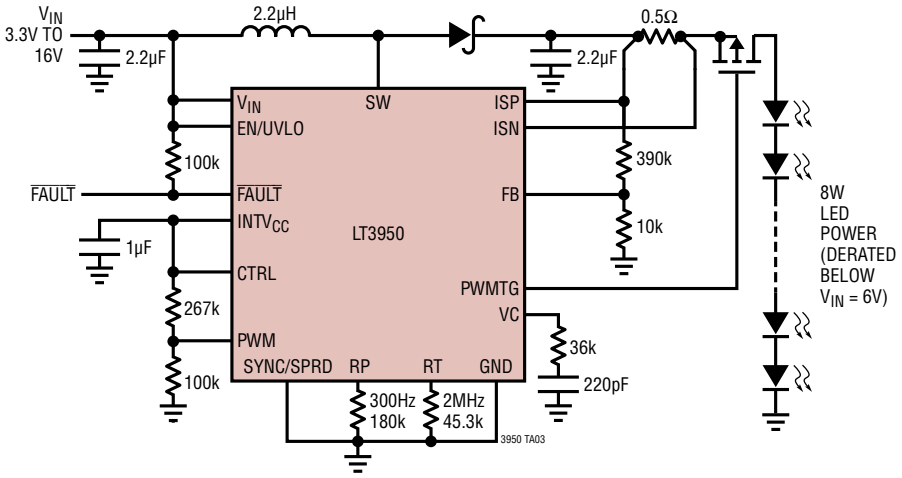
L1: WURTH 74437324100
D1: DIODES INC. DFLS260Q
M1: VISHAY SI7309

Efficiency and Power Loss



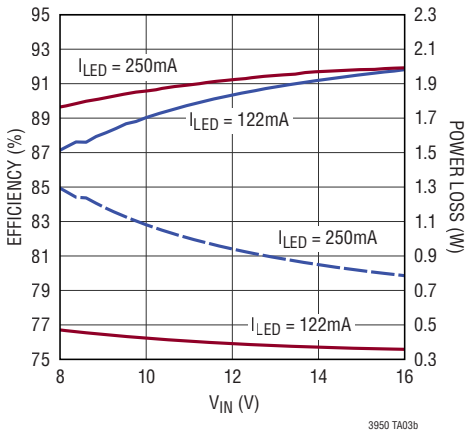
TYPICAL APPLICATIONS

8W Boost LED Driver with Internal 10% PWM Dimming

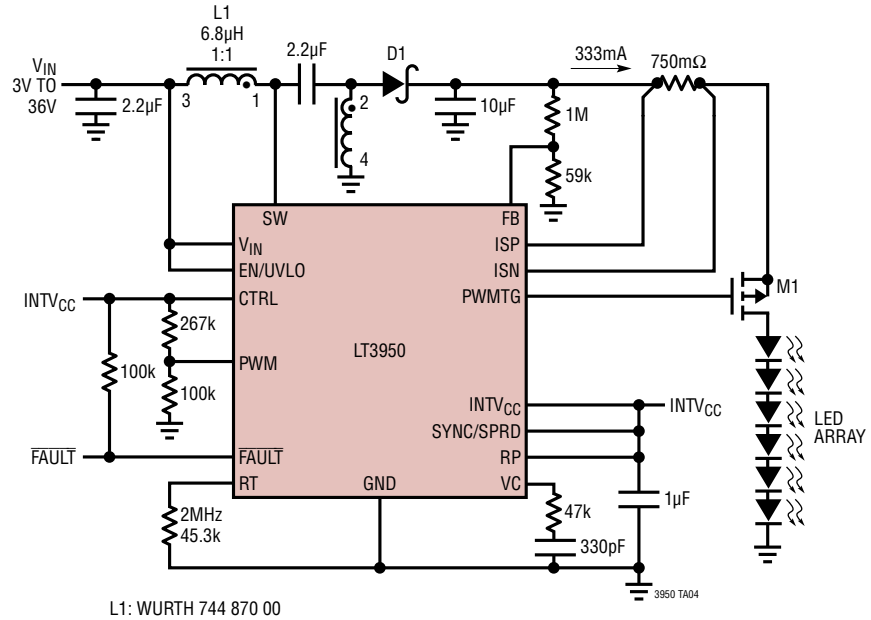


L1: WURTH 74437321022
D1: DIODES INC. DFLS260Q
M1: VISHAY SI7309

Efficiency

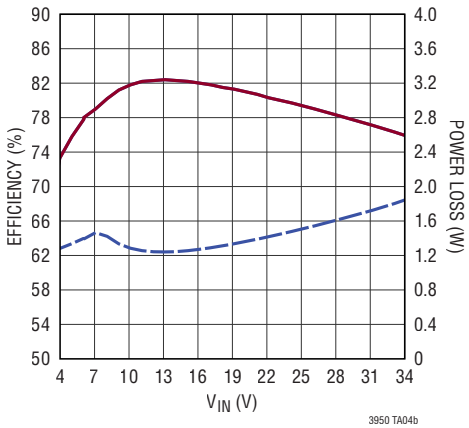


5W SEPIC LED Driver with Internal 10% PWM Dimming



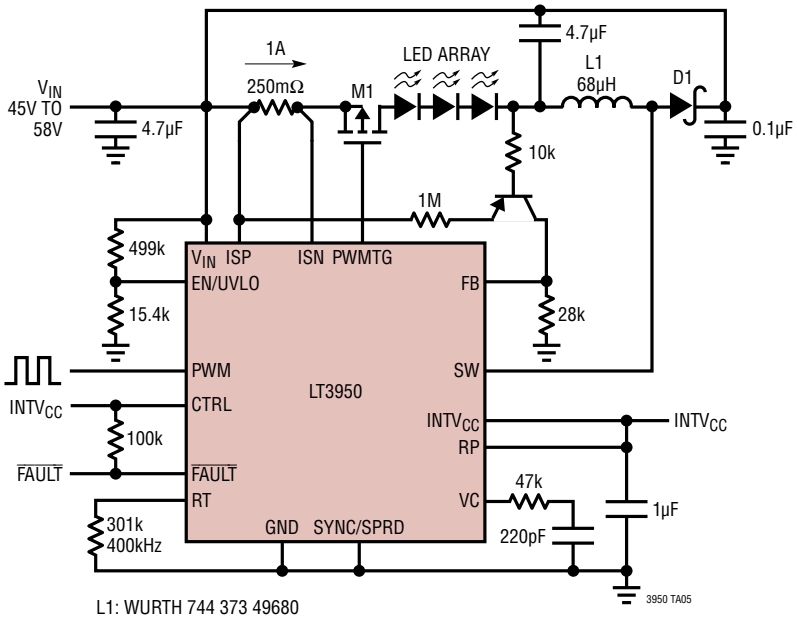
L1: WURTH 744 870 00
M1: VISHAY SI230
D1: DIODES INC DFLS160Q

Efficiency



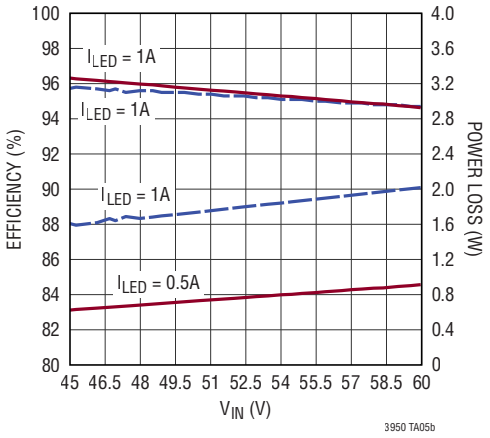
TYPICAL APPLICATIONS

36W Buck-Mode LED Driver



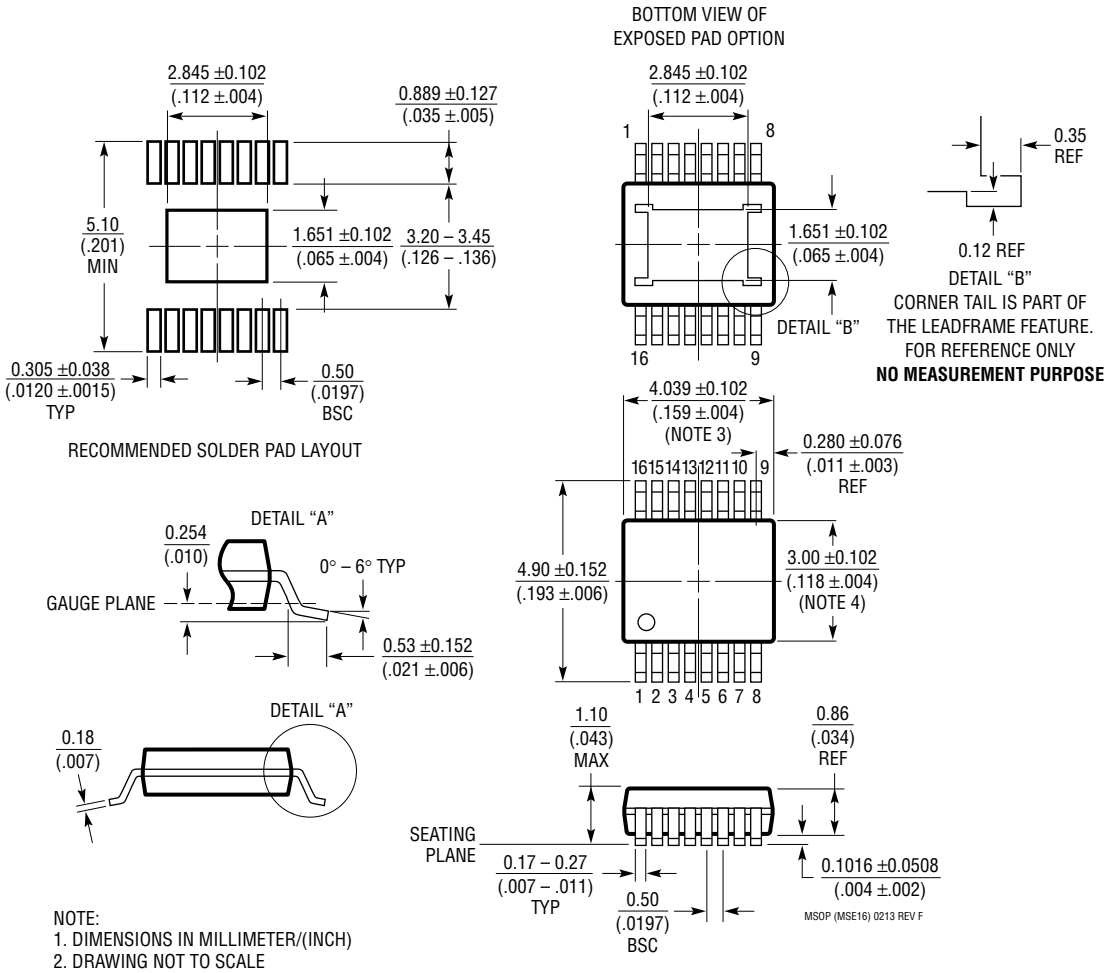
L1: WURTH 744 373 49680
D1: DIODES INC. DFLS260
M1: VISHAY SI7309

Efficiency



PACKAGE DESCRIPTION

MSE Package
16-Lead Plastic MSOP, Exposed Die Pad
(Reference LTC DWG # 05-08-1667 Rev F)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX
6. EXPOSED PAD DIMENSION DOES INCLUDE MOLD FLASH. MOLD FLASH ON E-PAD SHALL
   NOT EXCEED 0.254mm (.010") PER SIDE.

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	08/21	Minor graphical update.	1
		Clarified ISP, ISN Combined Pin Current Limits.	3
		Clarified $\overline{\text{FAULT}}$ Pin Pull Down Current Conditions.	4
		Updated overvoltage fault threshold operation.	11
		Minor graphical update to Typical Application circuit.	26