40V$_{IN}$ LED Converter with Internal PWM Generator

FEATURES

- **3000:1 True Color PWM™ Dimming for LEDs**
- **Wide V_{IN} Range: 4.5V to 40V**
- **Rail-to-Rail Current Sense Range: 0V to 40V**
- **Internal 40V/5A Switch**
- **Programmable PWM Dimming Signal Generator**
- **Constant Current (±3%) and Constant-Voltage (±2%) Regulation**
- **Accurate Analog Dimming**
- Drives LEDs in Boost, SEPIC, CUK, Buck Mode, Buck-Boost Mode, or Flyback Configuration
- Output Short-Circuit Protected Boost
- Open LED Protection and Reporting
- Adjustable Switching Frequency: 100kHz to 1MHz
- Programmable V_{IN} UVLO with Hysteresis
- C/10 Indication for Battery Chargers
- Low Shutdown Current: <1µA
- Thermally Enhanced 5mm × 6mm QFN Package

APPLICATIONS

- High Power LEDs
- Output Short-Circuit Protected Boost
- Battery and SuperCap Chargers
- Accurate Current Limited Voltage Regulators

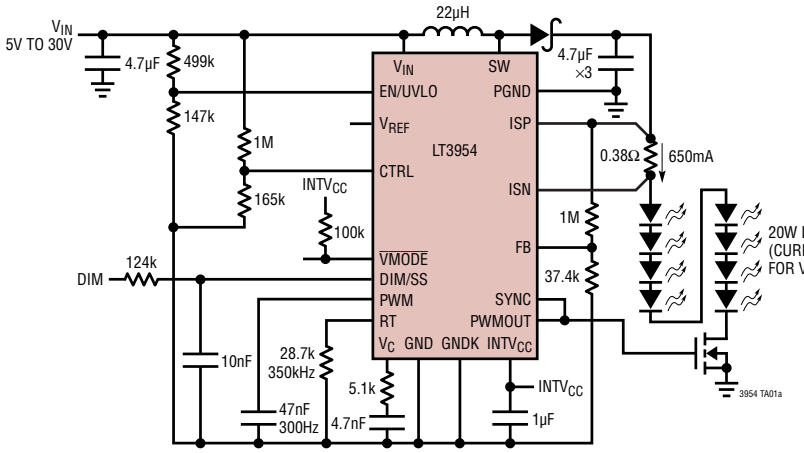
DESCRIPTION

The LT®3954 is a DC/DC converter designed to operate as a constant-current source and constant-voltage regulator. It features an internal low side N-channel MOSFET rated for 40V/5A. The LT3954 is ideally suited for driving high current LEDs, but also has features to make it suitable for charging batteries and supercapacitors. The fixed frequency, current mode architecture results in stable operation over a wide range of supply and output voltages. A voltage feedback pin serves as the input for several LED protection features, and also makes it possible for the converter to operate as a constant-voltage source. A frequency adjust pin allows the user to program the frequency from 100kHz to 1MHz to optimize efficiency, performance or external component size.

The LT3954 senses output current at the high side or at the low side of the load. The internal PWM generator can be configured to self-oscillate at fixed frequency with duty ratio programmable from 4% to 96%. When driven by an external signal, the PWM input provides LED dimming ratios of up to 3000:1. The CTRL input provides additional analog dimming capability.

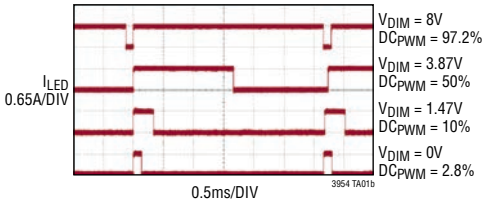
TYPICAL APPLICATION

95% Efficiency 20W Boost LED Driver with Internal PWM Dimming



NOTE: GND, GNDK AND SIGNAL LEVEL COMPONENTS MUST BE CONNECTED EXTERNALLY AS SHOWN.
AN INTERNAL CONNECTION BETWEEN GNDK AND PGND PINS PROVIDES GROUNDING TO THE SUPPLY

PWM Dimming Waveforms at Various DIM Voltage Settings



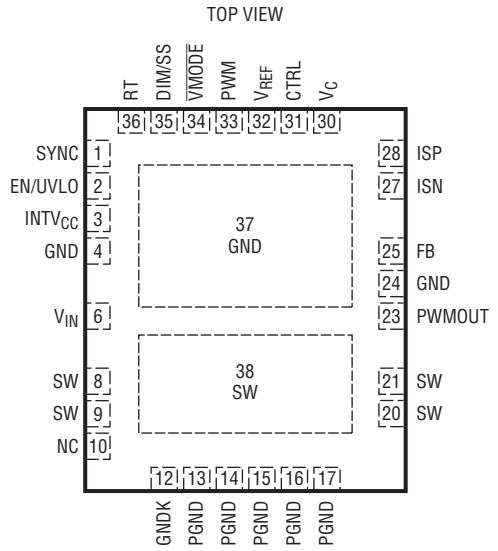
VIN = 24V
VLED = 32V

ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN}, EN/UVLO 40V
ISP, ISN, SW 40V
$INTV_{CC}$ ..... V_{IN} + 0.3V, 9.6V
PWMOUT ..... (Note 2)
CTRL, $\overline{VMODE}$ 15V
FB, PWM, SYNC 9.6V
V_C, V_{REF} 3V
RT, DIM/SS 1.5V
PGND, GNDK to GND ..... ±0.5V
Operating Ambient Temperature Range
(Notes 3, 4) ..... –40°C to 125°C
Maximum Junction Temperature ..... 125°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



UHE PACKAGE
36-LEAD (5mm × 6mm) PLASTIC QFN
θ_{JA} = 34°C/W, θ_{JC} = 3°C/W
EXPOSED PAD (PIN 37) IS GND, MUST BE SOLDERED TO GND PLANE
EXPOSED PAD (PIN 38) IS SW, MUST BE SOLDERED TO SW PLANE

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3954EUHE#PBF	LT3954EUHE#TRPBF	3954	36-Lead (5mm × 6mm) Plastic QFN	–40°C to 125°C
LT3954IUHE#PBF	LT3954IUHE#TRPBF	3954	36-Lead (5mm × 6mm) Plastic QFN	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 24V, EN/UVLO = 24V, CTRL = 2V, PWM = 5V, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN} Minimum Operating Voltage	V_{IN} Tied to $INTV_{CC}$	●			4.5	V
V_{IN} Shutdown I_Q	EN/UVLO = 0V, PWM = 0V EN/UVLO = 1.15V, PWM = 0V			0.1	1 6	µA µA
V_{IN} Operating I_Q (Not Switching)	PWM = 0V			1.8	2.2	mA
V_{REF} Voltage	–100µA ≤ I_{VREF} ≤ 0µA	●	1.965	2.02	2.06	V
V_{REF} Line Regulation	4.5V ≤ V_{IN} ≤ 40V			0.001		%/V
V_{REF} Pull-Up Current	V_{REF} = 0V	●	150	185	210	µA
SW Pin Current Limit		●	5.4	6.3	7.2	A
SW Pin Leakage	SW = 24V			5	10	µA
SW Pin Voltage Drop	I_{SW} = 3A			100		mV
DIM/SS Pull-Up Current	Current Out of Pin, DIM/SS = 0V	●	10	12	14	µA
DIM/SS Voltage Clamp	$I_{DIM/SS}$ = 0µA			1.2		V
Error Amplifier						
Full-Scale ISP/ISN Current Sense Threshold ($V_{ISP–ISN}$)	CTRL ≥ 1.2V, ISP = 24V CTRL ≥ 1.2V, ISN = 0V	● ●	242 243	250 257	258 268	mV mV
1/10th Scale ISP/ISN Current Sense Threshold ($V_{ISP–ISN}$)	CTRL = 0.2V, ISP = 24V CTRL = 0.2V, ISN = 0V	● ●	21 20	25 28	30 36	mV mV
Mid-Scale ISP/ISN Current Sense Threshold ($V_{ISP–ISN}$)	CTRL = 0.5V, ISP = 24V CTRL = 0.5V, ISN = 0V	● ●	96 94	100 105	104 115	mV mV
ISP/ISN Overcurrent Threshold				600		mV
ISP/ISN Current Sense Amplifier Input Common Mode Range (V_{ISN})			0		40	V
ISP/ISN Input Bias Current High Side Sensing (Combined)	PWM = 5V (Active), ISP = ISN = 24V PWM = 0V (Standby), ISP = ISN = 24V			100 0.1		µA µA
ISP/ISN Input Bias Current Low Side Sensing (Combined)	PWM = 5V, ISP = ISN = 0V			–230		µA
ISP/ISN Current Sense Amplifier g_m (High Side Sensing)	$V_{ISP–ISN}$ = 250mV, ISP = 24V			120		µS
ISP/ISN Current Sense Amplifier g_m (Low Side Sensing)	$V_{ISP–ISN}$ = 250mV, ISN = 0V			70		µS
CTRL Pin Range for Linear Current Sense Threshold Adjustment		●	0		1.0	V
CTRL Input Bias Current	Current Out of Pin			50	100	nA
V_C Output Impedance	0.9V ≤ V_C ≤ 1.5V			15		MΩ
V_C Standby Input Bias Current	PWM = 0V		–20		20	nA
FB Regulation Voltage (V_{FB})	ISP = ISN = 24V, 0V	●	1.225	1.255	1.275	V
FB Amplifier g_m	FB = V_{FB}, ISP = ISN = 24V			500		µS
FB Pin Input Bias Current	Current Out of Pin, FB = V_{FB}			40	100	nA
FB Open LED Threshold	$\overline{VMODE}$ Falling, ISP Tied to ISN	●	V_{FB} – 65mV	V_{FB} – 50mV	V_{FB} – 40mV	V
C/10 Inhibit for $\overline{VMODE}$ Assertion ($V_{ISP–ISN}$)	FB = V_{FB}, ISN = 24V, 0V		14	25	39	mV
FB Overvoltage Threshold	PWMOUT Falling		V_{FB} + 50mV	V_{FB} + 60mV	V_{FB} + 70mV	V
Oscillator						
Switching Frequency	R_T = 95.3kΩ R_T = 8.87kΩ	●	85 925	100 1000	115 1050	kHz kHz
SW Minimum Off-Time				160		ns
SW Minimum On-Time				180		ns
SYNC Input Low					0.4	V
SYNC Input High			1.5			V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 24V, EN/UVLO = 24V, CTRL = 2V, PWM = 5V, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Linear Regulator						
$INTV_{CC}$ Regulation Voltage	10V ≤ V_{IN} ≤ 40V	●	7.60	7.85	8.05	V
$INTV_{CC}$ Maximum Operating Voltage			8.1			V
$INTV_{CC}$ Minimum Operating Voltage					4.5	V
Dropout (V_{IN} – $INTV_{CC}$)	I_{INTVCC} = –10mA, V_{IN} = 7V			390		mV
$INTV_{CC}$ Undervoltage Lockout		●	3.9	4.1	4.4	V
$INTV_{CC}$ Current Limit	8V ≤ V_{IN} ≤ 40V, $INTV_{CC}$ = 6V		30	36	42	mA
$INTV_{CC}$ Current in Shutdown	EN/UVLO = 0V, $INTV_{CC}$ = 8V			8	13	µA
Logic Inputs/Outputs						
EN/UVLO Threshold Voltage Falling		●	1.180	1.220	1.260	V
EN/UVLO Rising Hysteresis				40		mV
EN/UVLO Input Low Voltage	I_{VIN} Drops Below 1µA				0.4	V
EN/UVLO Pin Bias Current Low	EN/UVLO = 1.15V		1.7	2.2	2.7	µA
EN/UVLO Pin Bias Current High	EN/UVLO = 1.33V			10	100	nA
$\overline{VMODE}$ Output Low	$I_{\overline{VMODE}}$ = 1mA				200	mV
$\overline{VMODE}$ Pin Leakage	FB = 0V, $\overline{VMODE}$ = 12V			0.1	5	µA
PWM Pin Signal Generator						
PWM Falling Threshold		●	0.78	0.83	0.88	V
PWM Threshold Hysteresis (V_{PWMHYS})	$I_{DIM/SS}$ = 0µA		0.35	0.47	0.6	V
PWM Pull-Up Current (I_{PWMUP})	PWM = 0.7V, $I_{DIM/SS}$ = 0µA		6	7.5	9	µA
PWM Pull-Down Current (I_{PWMDN})	PWM = 1.5V, $I_{DIM/SS}$ = 0µA		68	88	110	µA
PWM Fault-Mode Pull-Down Current	$INTV_{CC}$ = 3.6V			1.5		mA
PWMOUT Duty Ratio for PWM Signal Generator (Note 5)	$I_{DIM/SS}$ = –6.5µA $I_{DIM/SS}$ = 0µA $I_{DIM/SS}$ = 21.5µA $I_{DIM/SS}$ = 52µA		3.1 6.2 40 95	4.1 7.9 48 96.5	5.2 9.2 56 98	% % % %
PWMOUT Signal Generator Frequency	PWM = 47nF to GND, $I_{DIM/SS}$ = 0µA		170	300	390	Hz
PWMOUT Driver						
PWMOUT Driver Output Rise Time (t_r)	C_L = 560pF			35		ns
PWMOUT Driver Output Fall Time (t_f)	C_L = 560pF			35		ns
PWMOUT Output Low (V_{OL})	PWM = 0V				0.05	V
PWMOUT Output High (V_{OH})			$INTV_{CC}$ – 0.05			V

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Do not apply a positive or negative voltage or current source to PWMOUT pin, otherwise permanent damage may occur.

Note 3: The LT3954E is guaranteed to meet performance specifications from the 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT3954I is guaranteed over the full –40°C to 125°C operating junction temperature range.

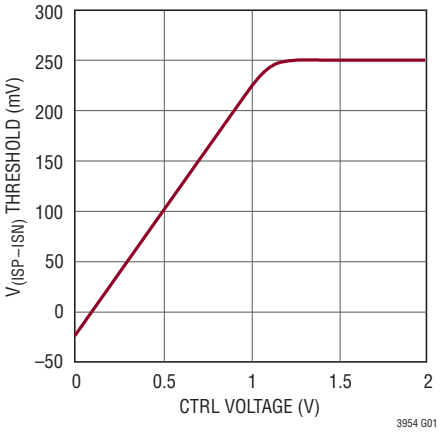
Note 4: The LT3954 includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed the maximum operating junction temperature when overtemperature protection is active. Continuous operation above the specified maximum junction temperature may impair device reliability.

Note 5: PWMOUT Duty Ratio is calculated:

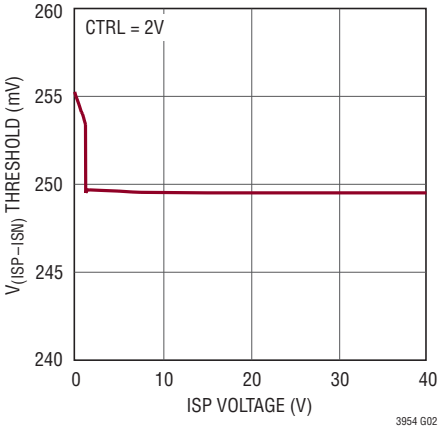
Duty = $I_{PWMUP}/(I_{PWMUP} + I_{PWMDN})$

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

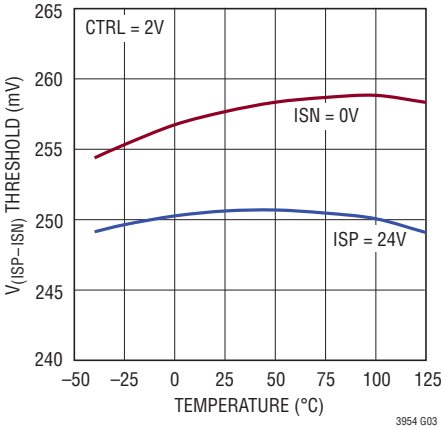
$V_{(ISP–ISN)}$ Threshold vs CTRL Voltage



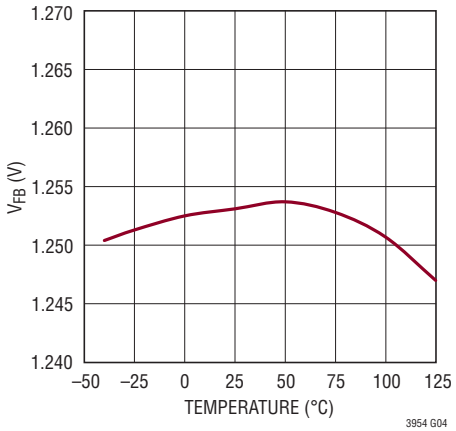
$V_{(ISP–ISN)}$ Threshold vs ISP Voltage



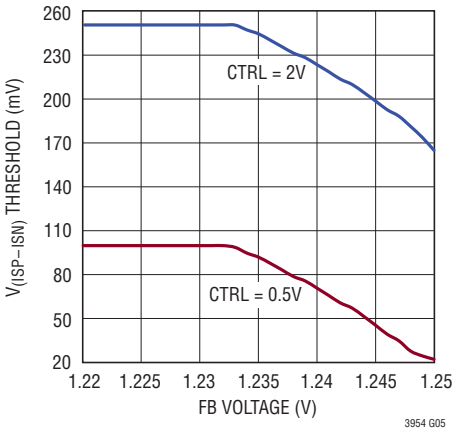
$V_{(ISP–ISN)}$ Threshold vs Temperature



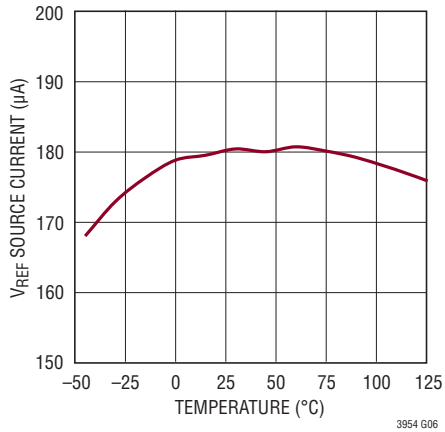
FB Regulation Voltage (V_{FB}) vs Temperature



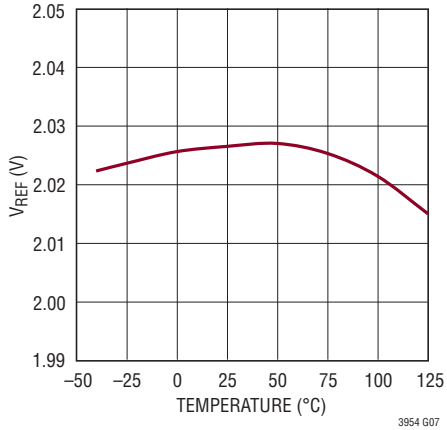
$V_{(ISP–ISN)}$ Threshold vs FB Voltage



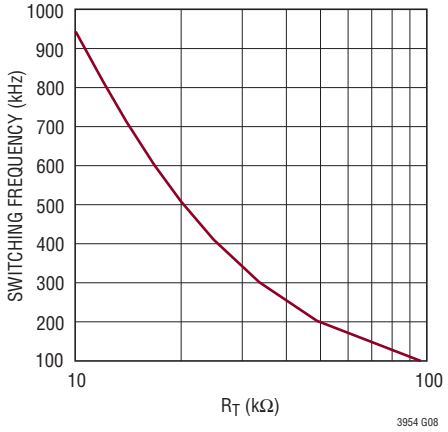
V_{REF} Source Current vs Temperature



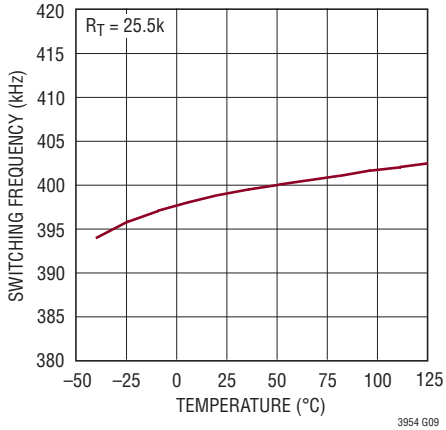
V_{REF} Voltage vs Temperature



Switching Frequency vs R_T

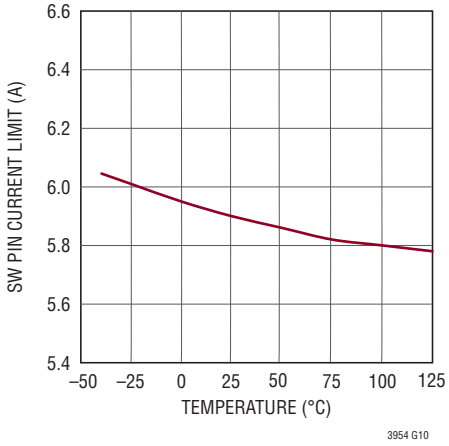


Switching Frequency vs Temperature

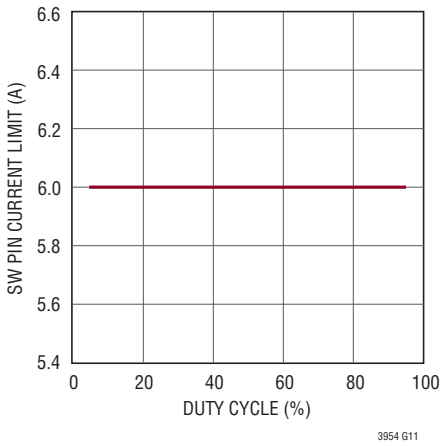


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

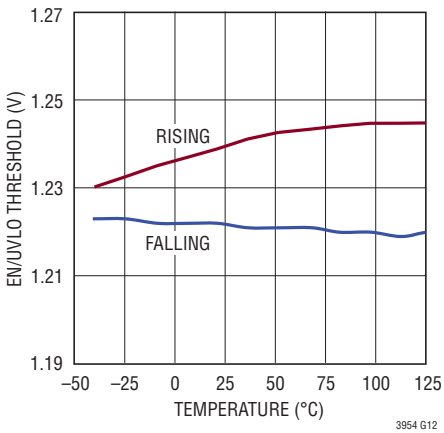
SW Pin Current Limit vs Temperature



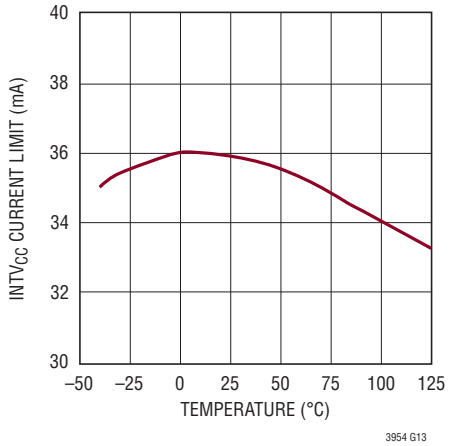
SW Pin Current Limit vs Duty Cycle



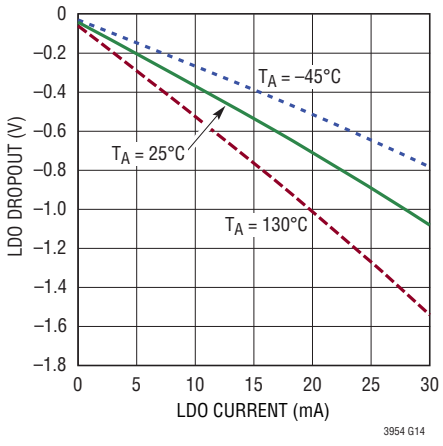
EN/UVLO Threshold vs Temperature



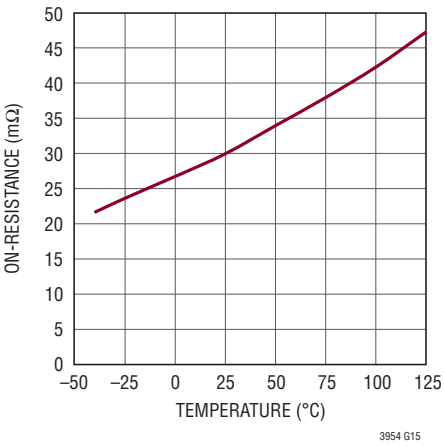
$INTV_{CC}$ Current Limit vs vs Temperature



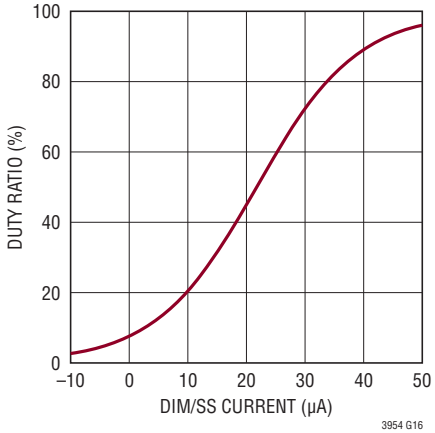
$INTV_{CC}$ Dropout Voltage vs Current, Temperature



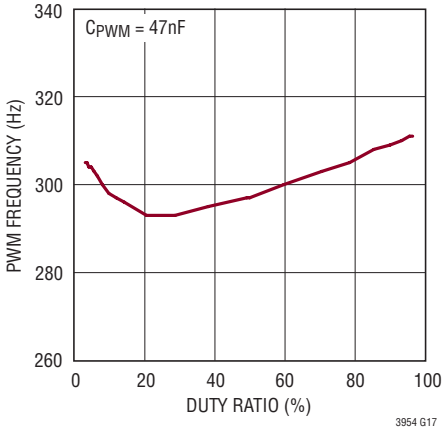
Internal Switch On-Resistance vs Temperature



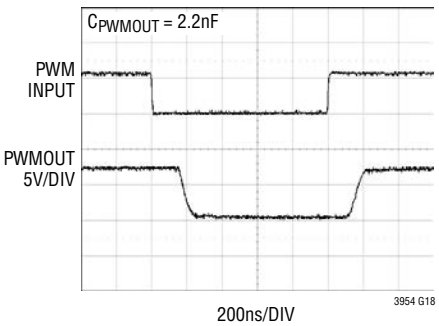
PWM Signal Generator Duty Ratio vs DIM/SS Current



PWM Signal Generator Frequency vs Duty Ratio



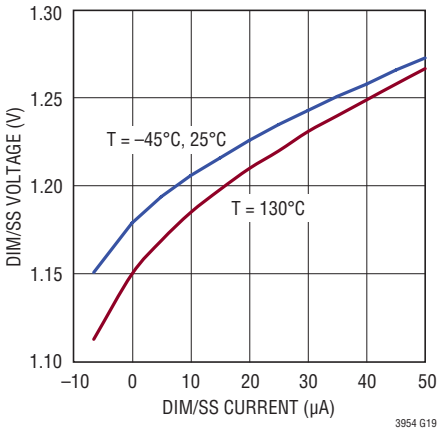
PWMOUT Waveform



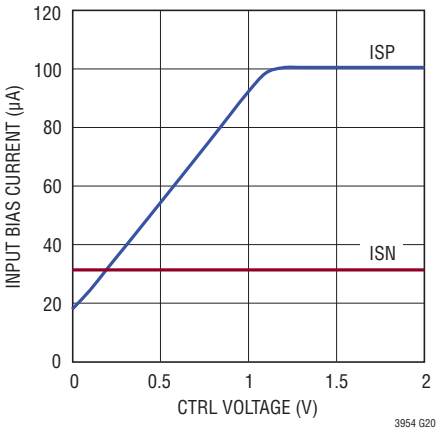
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

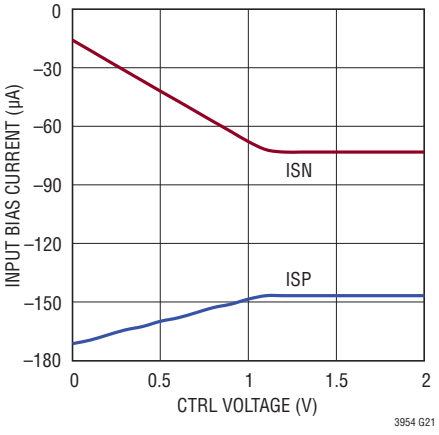
DIM/SS Voltage vs Current, Temperature



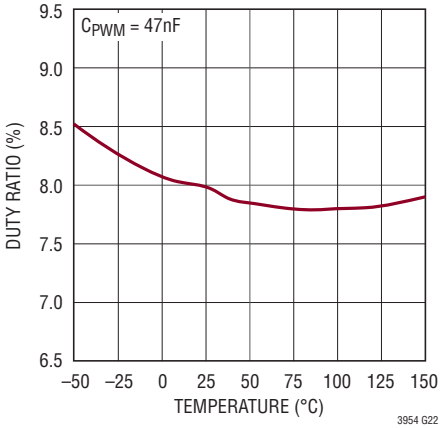
ISP/ISN Input Bias Current vs CTRL Voltage, ISP = 24V



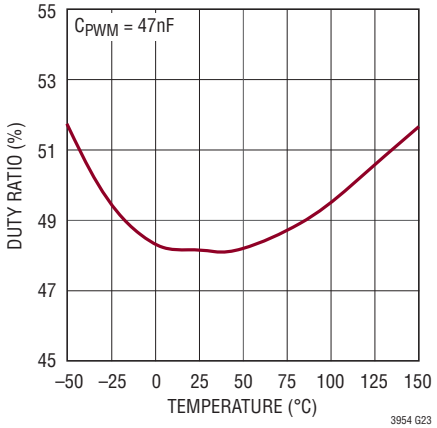
ISP/ISN Input Bias Current vs CTRL Voltage, ISN = 0V



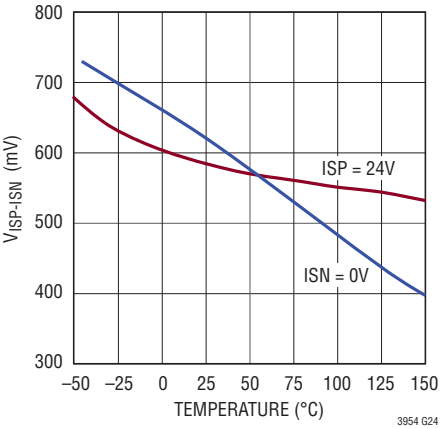
PWMOUT Duty Ratio vs Temperature, $I_{DIM/SS}$ = 0µA



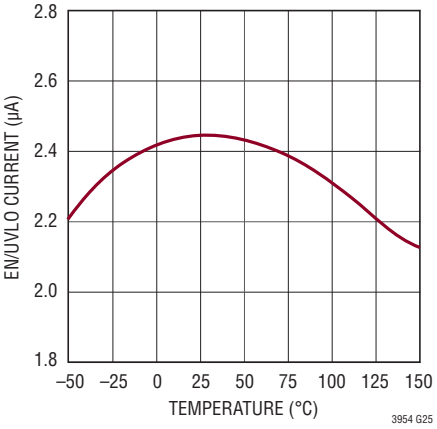
PWMOUT Duty Ratio vs Temperature, $I_{DIM/SS}$ = 21.5µA



VISP-ISN Overcurrent Threshold vs Temperature



EN/UVLO Hysteresis Current vs Temperature



PIN FUNCTIONS

SYNC (Pin 1): Frequency Synchronization Pin. Used to synchronize the internal oscillator to an outside clock. If this feature is used, an R_T resistor should be chosen to program a switching frequency 20% slower than SYNC pulse frequency. Tie the SYNC pin to PWMOUT if this feature is not used.

EN/UVLO (Pin 2): Enable and Undervoltage Detect Pin. An accurate 1.22V falling threshold with externally programmable hysteresis causes the switching regulator to shut down when power is insufficient to maintain output regulation. Above the 1.24V (typical) rising enable threshold (but below 2.5V), EN/UVLO input bias current is sub-µA. Below the 1.22V (typical) falling threshold, an accurate 2.2µA (typical) pull-down current is enabled so the user can define the rising hysteresis with the external resistor selection. An undervoltage condition causes the switch to turn off and the PWMOUT pin to transition low and resets soft-start. Tie to 0.4V, or less, to disable the device and reduce V_{IN} quiescent current below 1µA. Can be tied to V_{IN} through a 100k resistor.

$INTV_{CC}$ (Pin 3): Current limited, low dropout linear regulator regulates to 7.85V (typical) from V_{IN}. Supplies internal loads, SW and PWMOUT drivers. Must be bypassed with a 1µF ceramic capacitor placed close to the pin and to the exposed pad GND of the IC.

V_{IN} (Pin 6): Power Supply for Internal Loads and $INTV_{CC}$ Regulator. Must be locally bypassed with a 0.22µF (or larger) low ESR capacitor placed close to the pin.

GNDK (Pin 12): Kelvin Connection Pin between PGND and GND. Kelvin connect this pin to the GND plane close to the IC. See the Board Layout section.

PGND (Pins 13 to 17): Source Terminal Switch and the GND Input to the Switch Current Comparator.

PWMOUT (Pin 23): Buffered Version of PWM Signal for Driving LED Load Disconnect NMOS or Level Shift. This pin also serves in a protection function for the FB overvoltage condition—will toggle if the FB input is greater than the FB regulation voltage (V_{FB}) plus 60mV (typical). The PWMOUT pin is driven from $INTV_{CC}$. Use of a FET with gate cut-off voltage higher than 1V is recommended.

FB (Pin 25): Voltage Loop Feedback Pin. FB is intended for constant-voltage regulation or for LED protection and open LED detection. The internal transconductance amplifier with output VC will regulate FB to 1.25V (nominal) through the DC/DC converter. If the FB input exceeds the regulation voltage, V_{FB}, minus 50mV and the voltage between ISP and ISN has dropped below the C/10 threshold of 25mV (typical), the $\overline{VMODE}$ pull-down is asserted. This action may signal an open LED fault. If FB is driven above the FB overvoltage threshold, the PWMOUT pin will be driven low and the internal power switch is turned off, to protect the LEDs from an overcurrent event. Do not leave the FB pin open. If not used, connect to GND.

ISN (Pin 27): Connection Point for the Negative Terminal of the Current Feedback Resistor. The constant output current regulation can be programmed by $I_{LED} = 250mV/R_{LED}$ when CTRL > 1.2V or $I_{LED} = (CTRL – 100mV)/(4 • R_{LED})$. If ISN is greater than $INTV_{CC}$, input bias current is typically 20µA flowing into the pin. Below $INTV_{CC}$, ISN bias current decreases until it flows out of the pin.

ISP (Pin 28): Connection Point for the Positive Terminal of the Current Feedback Resistor. Input bias current depends upon CTRL pin voltage. When it is greater than $INTV_{CC}$ it flows into the pin. Below $INTV_{CC}$, ISP bias current decreases until it flows out of the pin. If the difference between ISP and ISN exceeds 600mV (typical), then an overcurrent event is detected. In response to this event, the switch is turned off and the PWMOUT pin is driven low to protect the switching regulator, a 1.5mA pulldown on PWM and a 9mA pulldown on the DIM/SS pin are activated for 4µs.

V_C (Pin 30): Transconductance Error Amplifier Output Pin Used to Stabilize the Switching Regulator Control Loop with an RC Network. The V_C pin is high impedance when PWM is low. This feature allows the V_C pin to store the demand current state variable for the next PWM high transition. Connect a capacitor between this pin and GND; a resistor in series with the capacitor is recommended for fast transient response.

PIN FUNCTIONS

CTRL (Pin 31): Current Sense Threshold Adjustment Pin. Constant current regulation point $V_{ISP-ISN}$ is one-fourth V_{CTRL} plus an offset for 0V ≤ CTRL ≤ 1V. For CTRL > 1.2V the $V_{ISP-ISN}$ current regulation point is constant at the full-scale value of 250mV. For 1V ≤ CTRL ≤ 1.2V, the dependence of $V_{ISP-ISN}$ upon CTRL voltage transitions from a linear function to a constant value, reaching 98% of full-scale value by CTRL = 1.1V. Do not leave this pin open.

V_{REF} (Pin 32): Voltage Reference Output Pin, Typically 2V. This pin drives a resistor divider for the CTRL pin, either for analog dimming or for temperature limit/compensation of LED load. It can be bypassed with 10nF or greater, or less than 50pF. Can supply up to 185µA (typical).

PWM (Pin 33): A signal low turns off switcher, idles the oscillator and disconnects the VC pin from all internal loads. PWMOUT pin follows the PWM pin, except in fault conditions. The PWM pin can be driven with a digital signal to cause pulse width modulation (PWM) dimming of an LED load. The digital signal should be capable of sourcing or sinking 200µA at the high and low thresholds. During start-up when DIM/SS is below 1V, the first rising edge of PWM enables switching which continues until $V_{ISP-ISN}$ ≥ 25mV or DIM/SS ≥ 1V. Connecting a capacitor from PWM pin to GND invokes a self-driving oscillator where internal pull-up and pull-down currents set a duty ratio for the PWMOUT pin for dimming LEDs. The capacitor must be placed close to the IC. The magnitudes of the pull-up/down currents are set by the current in the DIM/SS pin. The capacitor on PWM sets the frequency of the dimming signal. For hiccup mode response to output short-circuit faults, connect this pin as shown in the application titled Boost LED Driver with Output Short-Circuit Protection. If not used, connect the PWM pin to $INTV_{CC}$.

$\overline{\text{VMODE}}$ (Pin 34): An open-drain pull-down on this pin asserts if the FB input is greater than the FB regulation voltage (V_{FB}) minus 50mV (typical) AND the difference between current sense inputs ISP and ISN is less than 25mV. To function, the pin requires an external pull-up resistor, usually to $INTV_{CC}$. When the PWM input is low and the DC/DC converter is idle, the $\overline{\text{VMODE}}$ condition is latched to the last valid state when the PWM input was high. When PWM input goes high again, the $\overline{\text{VMODE}}$ pin will be updated. This pin may be used to report transition from constant current regulation to constant voltage regulation modes, for instance in a charger or current limited voltage supply.

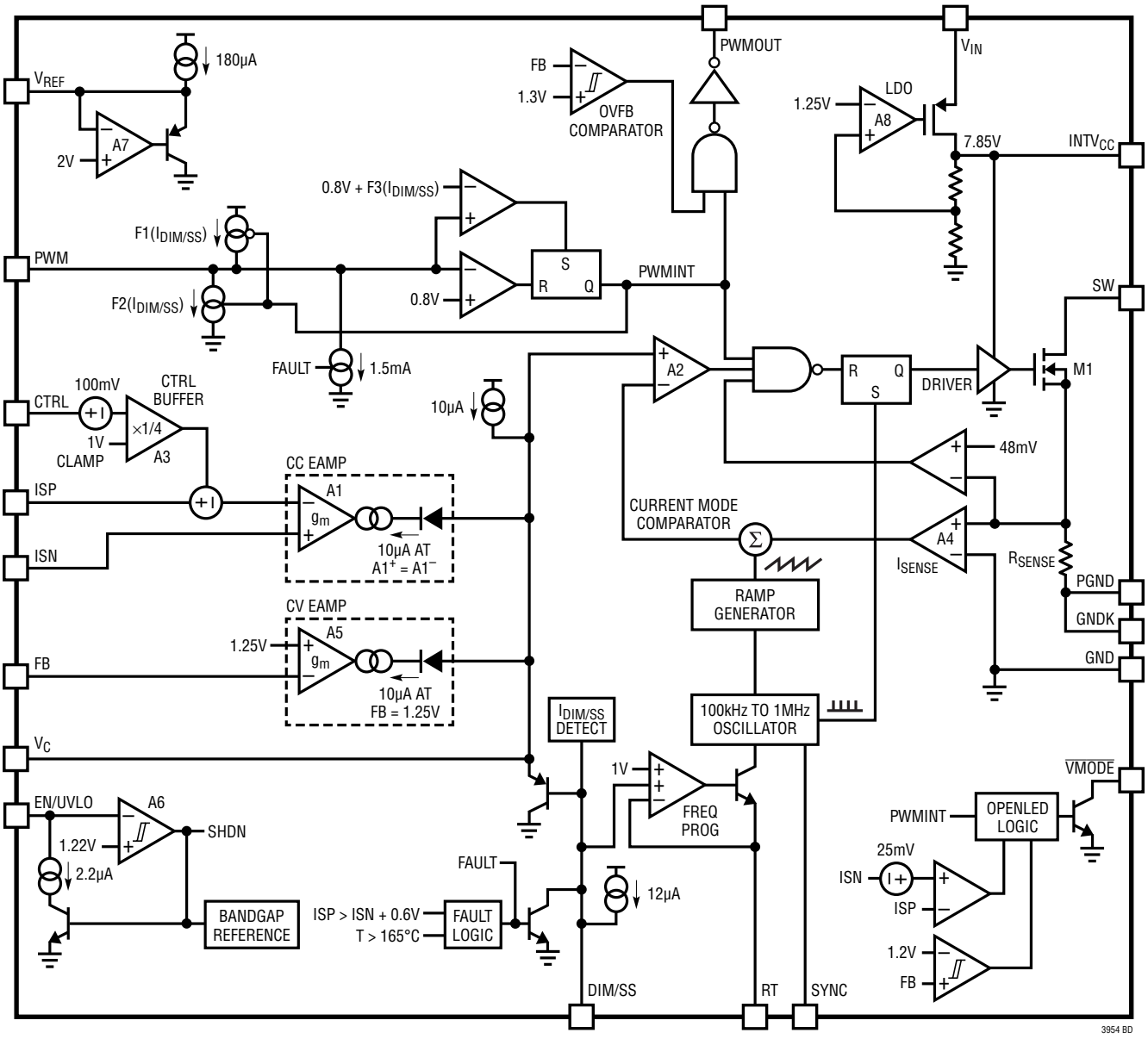
DIM/SS (Pin 35): Soft-Start and PWM Dimming Signal Generator Programming Pin. This pin modulates switching regulator frequency and compensation pin voltage (VC) clamp when it is below 1V. The soft-start interval is set with an external capacitor and the DIM/SS pin charging current. The pin has an internal 12µA (typical) pull-up current source. The soft-start pin is reset to GND by an undervoltage condition (detected at the EN/UVLO pin), $INTV_{CC}$ undervoltage, overcurrent event sensed at ISP/ISN, or thermal limit. After initial start-up with EN/UVLO, DIM/SS is forced low until the first PWM rising edge. When DIM/SS reaches the steady-state voltage (~1.17V), the charging current (sum of internal and external currents) is sensed and used to set the PWM pin charging and discharge currents and threshold hysteresis. In this manner, the SS charging current sets the duty cycle of the PWM signal generator associated with the PWM pin. This pin should always have a capacitor to GND, minimum 560pF value, when used with the PWM signal generator function. See typical performance curves for details on the variation of PWM pin parameters with SS charging current. Place the capacitor close to the IC.

RT (Pin 36): Switching Frequency Adjustment Pin. Set the frequency using a resistor to GND (for resistor values, see the Typical Performance curve or Table 2). Do not leave the RT pin open. Place the resistor close to the IC.

GND (Exposed Pad Pin 37, Pins 4, 24): Ground. Solder the exposed pads directly to the ground plane.

SW (Exposed Pad Pin 38, Pins 8, 9, 20, 21): Drain of Internal Power N-channel MOSFET.

BLOCK DIAGRAM



OPERATION

The LT3954 is a constant-frequency, current mode converter with a low side N-channel MOSFET switch. The switch and PWMOUT pin drivers, and other chip loads, are powered from $INTV_{CC}$, which is an internally regulated supply. In the discussion that follows it will be helpful to refer to the Block Diagram of the IC. In normal operation with the PWM pin low, the switch is turned off and the PWMOUT pin is driven to GND, the V_C pin is high impedance to store the previous switching state on the external compensation capacitor, and the ISP and ISN pin bias currents are reduced to leakage levels. When the PWM pin transitions high, the PWMOUT pin transitions high after a short delay. At the same time, the internal oscillator wakes up and generates a pulse to set the PWM latch, turning on the internal power MOSFET switch. A voltage input proportional to the switch current, sensed by an internal current sense resistor is added to a stabilizing slope compensation ramp and the resulting switch current sense signal is fed into the negative terminal of the PWM comparator. The current in the external inductor increases steadily during the time the switch is on. When the switch current sense voltage exceeds the output of the error amplifier, labeled V_C, the latch is reset and the switch is turned off. During the switch-off phase, the inductor current decreases. At the completion of each oscillator cycle, internal signals such as slope compensation return to their starting points and a new cycle begins with the set pulse from the oscillator.

Through this repetitive action, the PWM control algorithm establishes a switch duty cycle to regulate a current or voltage in the load. The V_C signal is integrated over many switching cycles and is an amplified version of the difference between the LED current sense voltage, measured between ISP and ISN, and the target difference voltage set by the CTRL pin. In this manner, the error amplifier sets the correct peak switch current level to keep the LED current in regulation. If the error amplifier output increases, more current is demanded in the switch; if it decreases, less current is demanded. The switch current is monitored during the on-phase and is not allowed to exceed the current limit threshold of 6.0A (typical). If the SW pin exceeds the current limit threshold, the SR latch is reset regardless of the output state of the PWM comparator. The difference between ISP and ISN is monitored to determine if the output is in a short-circuit condition. If the difference between ISP and ISN is greater than 600mV (typical), the SR latch will be reset regardless of the PWM comparator. The DIM/SS pin will be pulled down and the PWMOUT pin forced low and the SW pin turned off for at least 4µs. These functions are intended to protect the power switch as well as various external components in the power path of the DC/DC converter.

In voltage feedback mode, the operation is similar to that described above, except the voltage at the VC pin is set by the amplified difference of the internal reference of 1.25V and the FB pin. If FB is lower than the reference voltage, the switch current will increase; if FB is higher than the reference voltage, the switch demand current will decrease. The LED current sense feedback interacts with the FB voltage feedback so that FB will not exceed the internal reference and the voltage between ISP and ISN will not exceed the threshold set by the CTRL pin. For accurate current or voltage regulation, it is necessary to be sure that under normal operating conditions the appropriate loop is dominant. To deactivate the voltage loop entirely, FB can be connected to GND. To deactivate the LED current loop entirely, the ISP and ISN should be tied together and the CTRL input tied to V_{REF}.

Two LED specific functions featured on the LT3954 are controlled by the voltage feedback pin. First, when the FB pin exceeds a voltage 50mV lower (–4%) than the FB regulation voltage, and the difference voltage between ISP and ISN is below 25mV (typical), the pull-down driver on the $\overline{\text{VMODE}}$ pin is activated. This function provides a status indicator that the load may be disconnected and the constant-voltage feedback loop is taking control of the switching regulator. The $\overline{\text{VMODE}}$ pin de-asserts only when PWM is high and FB drops below the voltage threshold. FB overvoltage is the second protective function. When the FB pin exceeds the FB regulation voltage by 60mV (plus 5% typical), the PWMOUT pin is driven low, ignoring the state of the PWM input. In the case where the PWMOUT pin drives a disconnect NFET, this action isolates the LED load from GND, preventing excessive current from damaging the LEDs.

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$INTV_{CC}$ Regulator Bypassing and Operation

The $INTV_{CC}$ pin requires a capacitor for stable operation and to store the charge for the large internal MOSFET gate switching currents. Choose a 10V rated low ESR, X7R ceramic capacitor for best performance. A 1µF capacitor will be adequate for many applications. Place the capacitor close to the IC to minimize the trace length to the $INTV_{CC}$ pin and also to the IC ground.

An internal current limit on the $INTV_{CC}$ output protects the LT3954 from excessive on-chip power dissipation. The $INTV_{CC}$ pin has its own undervoltage disable set to 4.1V (typical) to protect the internal MOSFET from excessive power dissipation caused by not being fully enhanced. If the $INTV_{CC}$ pin drops below the UVLO threshold, the PWMOUT pin will be forced to 0V, the power switch will be turned off and the soft-start pin will be reset.

If the input voltage, V_{IN}, will not exceed 8.1V, then the $INTV_{CC}$ pin could be connected to the input supply. Be aware that a small current (less than 13µA) will load the $INTV_{CC}$ in shutdown. This action allows the LT3954 to operate from V_{IN} as low as 4.5V. If V_{IN} is normally above, but occasionally drops below the $INTV_{CC}$ regulation voltage, then the minimum operating V_{IN} will be close to 5V. This value is determined by the dropout voltage of the linear regulator and the $INTV_{CC}$ undervoltage lockout threshold mentioned above.

Programming the Turn-On and Turn-Off Thresholds with the EN/UVLO Pin

The power supply undervoltage lockout (UVLO) value can be accurately set by the resistor divider to the EN/UVLO pin. A small 2.2µA pull-down current is active when EN/UVLO is below the threshold. The purpose of this current is to allow the user to program the rising hysteresis. The following equations should be used to determine the value of the resistors:

$$V_{IN,FALLING} = 1.22 \bullet \frac{R1+R2}{R2}$$

$$V_{IN,RISING} = 2.2\mu A \bullet R1 + V_{IN,FALLING}$$

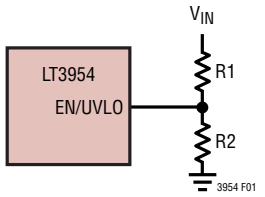

Figure 1. Resistor Connection to Set V_{IN} Undervoltage Shutdown Threshold

LED Current Programming

The LED current is programmed by placing an appropriate value current sense resistor, R_{LED}, in series with the LED string. The voltage drop across R_{LED} is (Kelvin) sensed by the ISP and ISN pins. A half watt resistor is usually a good choice. To give the best accuracy, sensing of the current should be done at the top of the LED string. If this option is not available then the current may be sensed at the bottom of the string, or in the source of the PWM disconnect NFET driven by the PWMOUT signal. Input bias currents for the ISP and ISN inputs are shown in the typical performance characteristics and should be considered when placing a resistor in series with the ISP or ISN pins.

The CTRL pin should be tied to a voltage higher than 1.2V to get the full-scale 250mV (typical) threshold across the sense resistor. The CTRL pin can also be used to dim the LED current to zero, although relative accuracy decreases with the decreasing voltage sense threshold. When the CTRL pin voltage is less than 1V, the LED current is:

$$I_{LED} = \frac{V_{CTRL} - 100mV}{R_{LED} \bullet 4}$$

When the CTRL pin voltage is between 1V and 1.2V the LED current varies with CTRL, but departs from the previous equation by an increasing amount as the CTRL voltage increases. Ultimately, the LED current no longer varies for CTRL ≥ 1.2V. At CTRL = 1.1V, the value of I_{LED} is ~98% of the equation's estimate. Some values are listed in Table 1.

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Table 1. (ISP-ISN) Threshold vs CTRL

V_{CRTL} (V)	(ISP-ISN) Threshold (mV)
1.0	225
1.05	236
1.1	244.5
1.15	248.5
1.2	250

When CTRL is higher than 1.2V, the LED current is regulated to:

$$I_{LED} = \frac{250mV}{R_{LED}}$$

The CTRL pin should not be left open (tie to V_{REF} if not used). The CTRL pin can also be used in conjunction with a thermistor to provide overtemperature protection for the LED load, or with a resistor divider to V_{IN} to reduce output power and switching current when V_{IN} is low. The presence of a time varying differential voltage signal (ripple) across ISP and ISN at the switching frequency is expected. The amplitude of this signal is increased by high LED load current, low switching frequency and/or a smaller value output filter capacitor. Some level of ripple signal is acceptable: the compensation capacitor on the VC pin filters the signal so the average difference between ISP and ISN is regulated to the user-programmed value. Ripple voltage amplitude (peak-to-peak) in excess of 50mV should not cause mis-operation, but may lead to noticeable offset between the current regulation and the user-programmed value.

Output Current Capability

An important consideration when using a switch with a fixed current limit is whether the regulator will be able to supply the load at the extremes of input and output voltage range. Several equations are provided to help determine this capability. Some margin to data sheet limits is included.

For boost converters:

$$I_{OUT(MAX)} \le 4.0A \frac{V_{IN(MIN)}}{V_{OUT(MAX)}}$$

For buck mode converters:

$$I_{OUT(MAX)} \le 4.0A$$

For SEPIC and buck-boost mode converters:

$$I_{OUT(MAX)} \le 4.0A \frac{V_{IN(MIN)}}{(V_{OUT(MAX)} + V_{IN(MIN)})}$$

These equations assume the inductor value and switching frequency have been selected so that inductor ripple current is ~800mA. Ripple current higher than this value will reduce available output current. Be aware that current limited operation at high duty cycle can greatly increase inductor ripple current, so additional margin may be required at high duty cycle.

If some level of analog dimming is acceptable at minimum supply levels, then the CTRL pin can be used with a resistor divider to V_{IN} (as shown on page 1) to provide a higher output current at nominal V_{IN} levels.

Programming Output Voltage (Constant Voltage Regulation) or Open LED/Overvoltage Threshold

For a boost or SEPIC application, the output voltage can be set by selecting the values of R3 and R4 (see Figure 2) according to the following equation:

$$V_{OUT} = 1.25 \bullet \frac{R3 + R4}{R4}$$

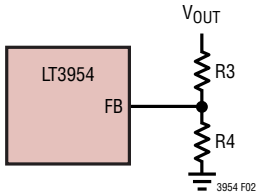

Figure 2. Feedback Resistor Connection for Boost or SEPIC LED Driver

For a boost type LED driver, set the resistor from the output to the FB pin such that the expected voltage level during normal operation will not exceed 1.17V. For an LED driver of buck mode or a buck-boost mode configuration, the output voltage is typically level-shifted to a signal with

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respect to GND as illustrated in Figure 3. The output can be expressed as:

$$V_{OUT} = V_{BE} + 1.25 \bullet \frac{R3}{R4}$$

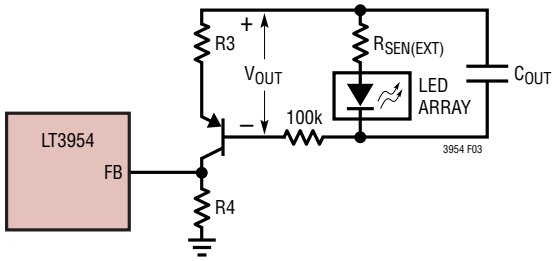

Figure 3. Feedback Resistor Connection for Buck Mode or Buck-Boost Mode LED Driver

ISP/ISN Short-Circuit Protection Feature

The ISP/ISN pins have a protection feature independent of their LED current sense feature. The purpose of this feature is to prevent the development of excessive currents that could damage the power components or the load. The action threshold ($V_{ISP-ISN}$ > 600mV, typical) is above the default LED current sense threshold, so that no interference will occur with current regulation. Exceeding the threshold activates pull-downs on the DIM/SS and PWM pins and causes the power switch to be turned off, and the PWMOUT pin to be driven low for at least 4µs. If an overcurrent condition is sensed at ISP/ISN and the PWM pin is configured either to make an internal dimming signal, or for always-on operation as shown in the application titled Boost LED Driver with Output Short-Circuit Protection, then the LT3954 will enter a hiccup mode of operation. In this mode, after the initial response to the fault, the PWMOUT pin re-enables the output switch at an interval set by the capacitor on the PWM pin. If the fault is still present, the PWMOUT pin will go low after a short delay (typically 7µs) and turn off the output switch. This fault-retry sequence continues until the fault is no longer present in the output.

PWM Dimming Control

There are two methods to control the current source for dimming using the LT3954. One method uses the CTRL pin to adjust the current regulated in the LEDs. A second method uses the PWM pin to modulate the current source between zero and full current to achieve a precisely programmed average current. To make PWM dimming more accurate, the switch demand current is stored on the V_C node during the quiescent phase when PWM is low. This feature minimizes recovery time when the PWM signal goes high. To further improve the recovery time, a disconnect switch may be used in the LED current path to prevent the ISP node from discharging during the PWM signal low phase.

The minimum PWM on or off time is affected by choice of operating frequency and external component selection. The best overall combination of PWM and analog dimming capability is available if the minimum PWM pulse is at least six switching cycles.

A low duty cycle PWM signal can cause excessive start-up times if it were allowed to interrupt the soft-start sequence. Therefore, once start-up is initiated by PWM > 1.3V, it will ignore a logical disable by the external PWM input signal. The device will continue to soft-start with switching and PWMOUT enabled until either the voltage at SS reaches the 1V level, or the output current reaches one-tenth of the full-scale current. At this point the device will begin following the dimming control as designated by PWM.

PWM Dimming Signal Generator

The LT3954 features a PWM dimming signal generator with programmable duty cycle. The frequency of the square wave signal at PWMOUT is set by a capacitor C_{PWM} from the PWM pin to GND according to the equation:

$$f_{PWM} = 14kHz \bullet nF/C_{PWM}$$

The duty cycle of the signal at PWMOUT is set by a µA scale current into the DIM/SS pin (see Figure 4).

Internally generated pull-up and pull-down currents on the PWM pin are used to charge and discharge its capacitor between the high and low thresholds to generate the duty cycle signal. These current signals on the PWM pin are small enough so they can be easily overdriven by a digital signal from a microcontroller to obtain very high dimming performance. The practical minimum duty cycle

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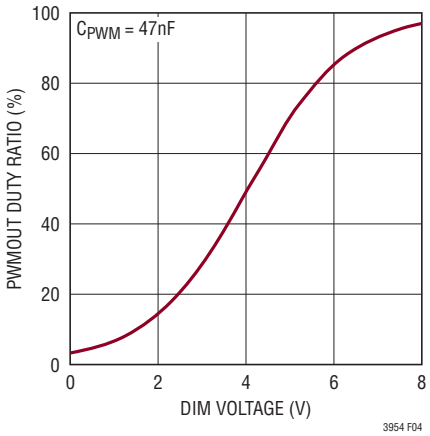

Figure 4. PWMOUT Duty Ratio vs DIM Voltage for R_{DIM} = 124k

using the internal signal generator is about 4% if the DIM/SS pin is used to adjust the dimming ratio. Consult the factory for techniques for and limitations of generating a duty ratio less than 4% using the internal generator. For always on operation, the PWM pin should be connected as shown in the application Boost LED Driver with Output Short-Circuit Protection.

Internal PWM Oscillator Operation

The PWM oscillator operation is similar to a 555 timer (bi-stable multi-vibrator). However, the currents that charge and discharge the capacitor are not directly proportional to the controlling current.

$$I_{PULL\text{-}UP} = F1(I_{DIM/SS}) = 7.2\mu A \bullet \exp(0.056 \bullet I_{DIM/SS})$$

$$I_{PULL\text{-}DOWN} = F2(I_{DIM/SS}) = 84\mu A \bullet \exp(-0.056 \bullet I_{DIM/SS})$$

The negative sign in the exponential makes $I_{PULL\text{-}DOWN}$ decrease when $I_{DIM/SS}$ increases.

Voltage on the external cap ramps up at $dV/dt = I_{PULL\text{-}UP}/C_{PWM}$. When the PWM pin reaches the high threshold ($0.8V + F3(I_{DIM/SS})$), the flip flop SETs and $I_{PULL\text{-}UP}$ goes to zero and current $I_{PULL\text{-}DOWN}$ goes to $F2(I_{DIM/SS})$.

$$\text{Duty Cycle} = \frac{T1}{T1+T2}$$

$$T1 = \frac{dV}{\left(\frac{I_{PULL-DOWN}}{C_{PWM}}\right)}$$

$$T2 = \frac{dV}{\left(\frac{I_{PULL-UP}}{C_{PWM}}\right)}$$

After simplification, one can obtain the formula for duty cycle of PWMOUT as a function of $I_{DIM/SS}$:

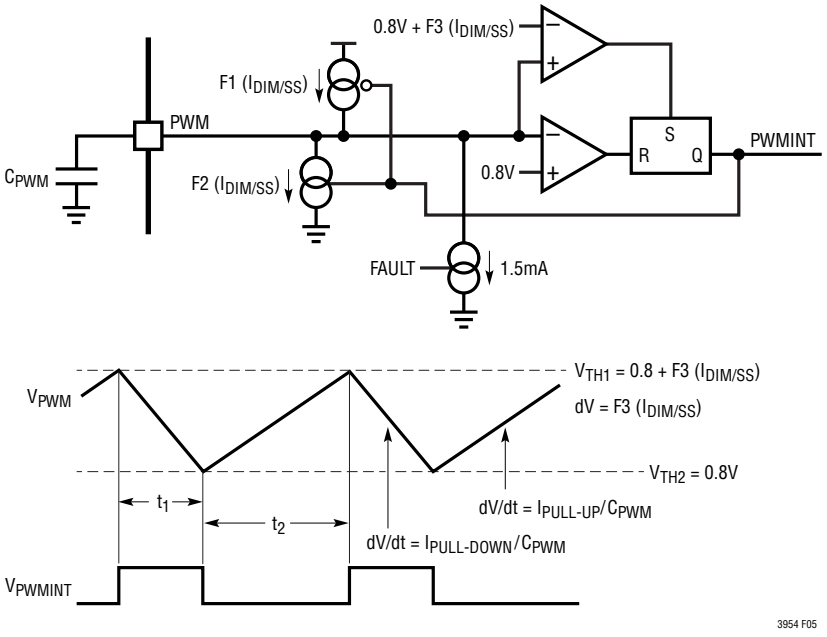

Figure 5. Internal PWM Oscillator Logic and Waveform

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$$\text{Duty Cycle} = \frac{1}{1+11.6 \bullet \exp(-0.112 \bullet I_{DIM/SS})}$$

To calculate the duty cycle of the internal PWM generator given a voltage of the DIM signal, determine first the current into the DIM/SS pin by the equation (referring to Figure 6):

$$I_{DIM/SS} = \frac{V_{DIM} - 1.17V}{R_{DIM} + 2.5k\Omega} \text{ in } \mu A$$

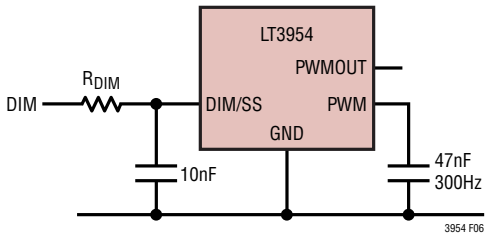

Figure 6. Configuration of Dimming Resistor, R_{DIM}

Knowing the $I_{DIM/SS}$ in µA , the duty cycle of the PWMOUT pin can be calculated for the range $-10\mu A < I_{DIM/SS} < 55\mu A$:

$$\text{Duty (in\%)} = \frac{100\%}{1+11.6 \bullet \exp(-0.112 \bullet I_{DIM/SS})}$$

These equations can be worked in reverse starting with a desired duty cycle using 20%, for example, and solving for a resistor value, R_{DIM}, placed between V_{REF} and DIM/SS:

$$I_{DIM/SS} = 8.93 \bullet \ln\left(11.6 \bullet \frac{\text{Duty}}{(1-\text{Duty})}\right)$$

$$= 8.93 \bullet \ln\left(11.6 \bullet \frac{0.2}{0.8}\right) = 9.51\mu A$$

$$R_{DIM} = -2.5k\Omega + \frac{V_{REF} - 1.17}{I_{DIM/SS}}$$

$$= -2.5k\Omega + \frac{2.015 - 1.17}{0.00951} = 86.4k\Omega$$

For some applications, a duty cycle lower than 3% is desired. It is possible to achieve a discrete value of duty cycle that is lower than range attainable using DIM/SS current. A resistor, R_{PD}, and switch driven by PWMOUT can be added as shown in Figure 7.

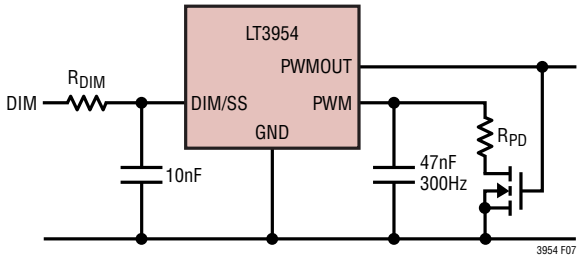

Figure 7. Configuration for Sub 4% PWM Dimming

The addition of this resistor increases the pull-down current on PWM, thus decreasing the duration of the on-phase of the switching regulator. Since PWM frequency at low duty cycle is primarily determined by the pull-up current, the additional pull-down current from R_{PD} has little effect on the PWM period, so frequency calculation remains the same.

An example solving for R_{PD} given a 1% duty cycle is provided below. For this example, the $I_{DIM/SS}$ current flowing in R_{DIM} is assumed zero, which normally provides an ~8% duty cycle. The average voltage on the PWM pin is approximately 1.05V at this $I_{DIM/SS}$ setting.

$$\text{Duty} = \frac{I_{PULL-UP}}{I_{PULL-UP} + I_{PULL-DOWN} + I_{RPD}}$$

$$= \frac{7.2}{7.2+84+I_{RPD}} = 0.01$$

$$I_{RPD} = 629\mu A = \frac{1.05V}{R_{PD}}$$

Therefore, R_{PD} ~ 1.65kΩ

Programming the Switching Frequency

The RT frequency adjust pin allows the user to program the switching frequency (f_{SW}) from 100kHz to 1MHz to optimize efficiency/performance or external component size. Higher frequency operation yields smaller component size but increases switching losses and gate driving current, and may not allow sufficiently high or low duty

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cycle operation. Lower frequency operation gives better performance at the cost of larger external component size. For an appropriate R_T resistor value see Table 2. An external resistor from the RT pin to GND is required—do not leave this pin open.

Table 2. Switching Frequency (f_{SW}) vs R_T Value

f_{SW} (kHz)	R_T (kΩ)
100	95.3
200	48.7
300	33.2
400	25.5
500	20.5
600	16.9
700	14.3
800	12.1
900	10.7
1000	8.87

Duty Cycle Considerations

Switching duty cycle is a key variable defining converter operation, therefore, its limits must be considered when programming the switching frequency for a particular application. The minimum duty cycle of the switch is limited by the fixed minimum on-time and the switching frequency (f_{SW}). The maximum duty cycle of the switch is limited by the fixed minimum off-time and f_{SW}. The following equations express the minimum/maximum duty cycle:

Min Duty Cycle = 220ns • f_{SW}

Max Duty Cycle = 1 – 170ns • f_{SW}

Besides the limitation by the minimum off-time, it is also recommended to choose the maximum duty cycle below 95%.

$$D_{BOOST} = \frac{V_{LED} - V_{IN}}{V_{LED}}$$

$$D_{BUCK\_MODE} = \frac{V_{LED}}{V_{IN}}$$

$$D_{SEPIC}, D_{CUK} = \frac{V_{LED}}{V_{LED} + V_{IN}}$$

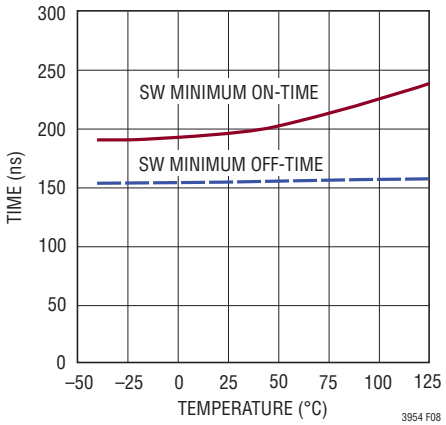

Figure 8. Typical Switch Minimum On and Off Pulse Width vs Temperature

Thermal Considerations

The LT3954 is rated to a maximum input voltage of 40V. Careful attention must be paid to the internal power dissipation of the IC at higher input voltages to ensure that a junction temperature of 125°C is not exceeded. This junction limit is especially important when operating at high ambient temperatures. If LT3954 junction temperature reaches 165°C, the power switch will be turned off and the PWMOUT pin will be driven to GND and the soft-start (DIM/SS) pin will be discharged to GND. Switching will be enabled after device temperature is reduced 10°C. This function is intended to protect the device during momentary thermal overload conditions.

The major contributors to internal power dissipation are the current in the linear regulator to drive the switch, and the ohmic losses in the switch. The linear regulator power is proportional to V_{IN} and switching frequency, so at high V_{IN} the switching frequency should be chosen carefully to ensure that the IC does not exceed a safe junction temperature. The internal junction temperature of the IC can be estimated by:

$$T_J = T_A + [V_{IN} \bullet (I_Q + f_{SW} \bullet 7nC) + I_{SW}^2 \bullet 0.04\Omega \bullet D_{SW}] \bullet \theta_{JA}$$

where T_A is the ambient temperature, I_Q is the quiescent current of the part (maximum 2.2mA) and θ_{JA} is the package thermal impedance (34°C/W for the 5mm × 6mm QFN package). For example, an application with $T_{A(MAX)}$ = 85°C,

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$V_{IN(MAX)}$ = 40V, f_{SW} = 400kHz, and having an average switching current of 4A at 70% duty cycle, the maximum IC junction temperature will be approximately:

$$T_J = 85°C + [(4A)^2 • 0.04Ω • 0.7 + 40V • (2.2mA + 400kHz • 7nC)] • 34°C/W = 107°C$$

The exposed pad on the bottom of the package must be soldered to a ground plane. This ground should then be connected to an internal copper ground plane with thermal vias placed directly under the package to spread out the heat dissipated by the IC.

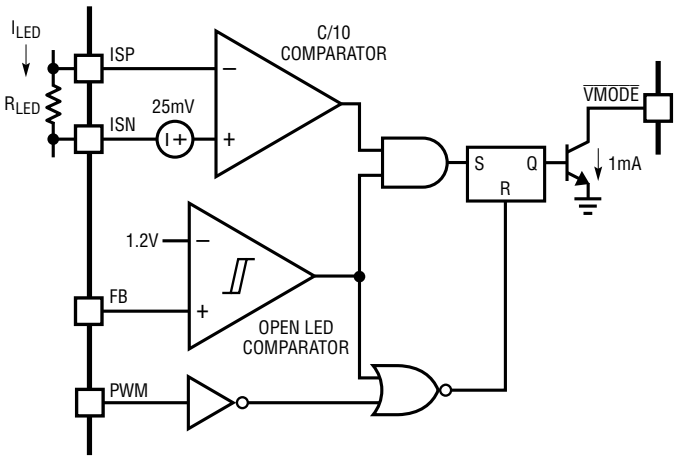
Open LED Reporting – Constant Voltage Regulation Status Pin

The LT3954 provides an open-drain status pin, $\overline{VMODE}$, that pulls low when the FB pin is within 50mV of its 1.25V regulated voltage AND output current sensed by $V_{ISP-ISN}$ has reduced to 25mV, or 10% of the full-scale value. The 10% output current qualification (C/10) is unique for an LED driver but fully compatible with open LED indication – the qualification is always satisfied since for an open load zero current flows in the load. The C/10 feature is particularly useful in the case where $\overline{VMODE}$ is used to indicate the end of a battery charging cycle and terminate charging or transition to a float charge mode.

For monitoring the LED string voltage, if the open LED clamp voltage is programmed correctly using the FB resistor divider then the FB pin should not exceed 1.18V when LEDs are connected. If the $\overline{VMODE}$ pulldown is asserted when the PWM pin transitions low, the pulldown will continue to be asserted until the next rising edge of PWM even if FB falls below the $\overline{VMODE}$ threshold. Figure 9 shows the $\overline{VMODE}$ logic block diagram.

Input Capacitor Selection

The input capacitor supplies the transient input current for the power inductor of the converter and must be placed and sized according to the transient current requirements. The switching frequency, output current and tolerable input voltage ripple are key inputs to estimating the capacitor value. An X7R type ceramic capacitor is usually the best choice since it has the least variation with temperature and



1. $\overline{VMODE}$ ASSERTS WHEN $V_{ISP-ISN}$ < 25mV **AND** FB > 1.2V, AND IS LATCHED
2. $\overline{VMODE}$ DE-ASSERTS WHEN FB < 1.19V, **AND** PWM = LOGIC "1"
3. ANY FAULT CONDITION RESETS THE LATCH, SO LT3955 STARTS UP WITH $\overline{VMODE}$ DE-ASSERTED

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Figure 9. $\overline{VMODE}$ (CV Mode) Logic Block Diagram

DC bias. Typically, boost and SEPIC converters require a lower value capacitor than a buck mode converter. Assuming that a 100mV input voltage ripple is acceptable, the required capacitor value for a boost converter can be estimated as follows:

$$C_{IN}(\mu F) = I_{LED}(A) • \frac{V_{OUT}}{V_{IN}} • t_{SW}(\mu s) • \left(\frac{\mu F}{A • \mu s}\right)$$

Therefore, a 10µF capacitor is an appropriate selection for a 400kHz boost regulator with 12V input, 36V output and 1A load.

With the same V_{IN} voltage ripple of 100mV, the input capacitor for a buck converter can be estimated as follows:

$$C_{IN}(\mu F) = I_{LED}(A) • t_{SW}(\mu s) • 4.7 • \left(\frac{\mu F}{A • \mu s}\right)$$

A 10µF input capacitor is an appropriate selection for a 400kHz buck mode converter with a 1A load.

In the buck mode configuration, the input capacitor has large pulsed currents due to the current returned through the Schottky diode when the switch is off. In this buck converter case it is important to place the capacitor as close

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as possible to the Schottky diode and to the GND return of the switch (i.e., the sense resistor). It is also important to consider the ripple current rating of the capacitor. For best reliability, this capacitor should have low ESR and ESL and have an adequate ripple current rating.

Table 3. Recommended Ceramic Capacitor Manufacturers

MANUFACTURER	WEB
TDK	www.tdk.com
Kemet	www.kemet.com
Murata	www.murata.com
Taiyo Yuden	www.t-yuden.com

Output Capacitor Selection

The selection of the output capacitor depends on the load and converter configuration, i.e., step-up or step-down and the operating frequency. For LED applications, the equivalent resistance of the LED is typically low and the output filter capacitor should be sized to attenuate the current ripple. Use of X7R type ceramic capacitors is recommended.

To achieve the same LED ripple current, the required filter capacitor is larger in the boost and buck-boost mode applications than that in the buck mode applications. Lower operating frequencies will require proportionately higher capacitor values.

Soft-Start Capacitor Selection

For many applications, it is important to minimize the inrush current at start-up. The built-in soft-start circuit significantly reduces the start-up current spike and output voltage overshoot. Connect a capacitor from the DIM/SS pin to GND to use this feature. The soft-start interval is set by the soft-start capacitor selection according to the equation:

$$T_{SS} = C_{SS} \bullet \frac{1.2V}{12\mu A} = C_{SS} \bullet \frac{100\mu s}{nF}$$

provided there is no additional current supplied to the DIM/SS pin for programming the duty cycle of the PWM dimming signal generator. A typical value for the soft-start capacitor is 10nF which gives a 1ms start-up interval. The soft-start pin reduces the oscillator frequency and the maximum current in the switch.

The soft-start capacitor discharges if one of the following events occurs: the EN/UVLO falls below its threshold; output overcurrent is detected at the ISP/ISN pins; IC overtemperature; or $INTV_{CC}$ undervoltage. During start-up with EN/UVLO, charging of the soft-start capacitor is enabled after the first PWM high period. In the start-up sequence, after switching is enabled by PWM the switching continues until $V_{ISP-ISN}$ > 25mV or DIM/SS > 1V. PWM pin negative edges during this start-up interval are not processed until one of these two conditions are met so that the regulator can reach steady state operation shortly after PWM dimming commences.

Schottky Rectifier Selection

The power Schottky diode conducts current during the interval when the switch is turned off. Select a diode rated for the maximum SW voltage of the application and the RMS diode current. If using the PWM feature for dimming, it may be important to consider diode leakage, which increases with the temperature, from the output during the PWM low interval. Therefore, choose the Schottky diode with sufficiently low leakage current. Table 4 has some recommended component vendors. The diode current and V_F should be considered when selecting the diode to be sure that power dissipation does not exceed the rating of the diode. The power dissipated by the diode in a converter is:

$$P_D = I_D \bullet V_F \bullet (1\text{-}D_{MAX})$$

It is prudent to measure the diode temperature in steady state to ensure that its absolute maximum ratings are not exceeded.

Table 4. Schottky Rectifier Manufacturers

MANUFACTURER	WEB
On Semiconductor	www.onsemi.com
Central Semiconductor	www.centralsemi.com
Diodes, Inc.	www.diodes.com

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Inductor Selection

The inductor used with the LT3954 should have a saturation current rating appropriate to the maximum switch current of 7.2A. Choose an inductor value based on operating frequency, input and output voltage to provide a current mode signal of approximately 0.8A magnitude. The following equations are useful to estimate the inductor value for continuous conduction mode operation (use the minimum value for V_{IN} and maximum value for V_{LED}):

$$L_{BUCK} = \frac{V_{LED}(V_{IN} - V_{LED})}{V_{IN} \bullet 0.8A \bullet f_{OSC}}$$

$$L_{BUCK\text{-}BOOST} = \frac{V_{LED} \bullet V_{IN}}{(V_{LED} + V_{IN}) \bullet 0.8A \bullet f_{OSC}}$$

$$L_{BOOST} = \frac{V_{IN}(V_{LED} - V_{IN})}{V_{LED} \bullet 0.8A \bullet f_{OSC}}$$

Use the equation for Buck-Boost when choosing an inductor value for SEPIC – if the SEPIC inductor is coupled, then the equation's result can be used as is. If the SEPIC uses two uncoupled inductors, then each should have a inductance double the result of the equation.

Table 5 provides some recommended inductor vendors.

Table 5. Recommended Inductor Manufacturers

MANUFACTURER	WEB
Coilcraft	www.coilcraft.com
Cooper-Coiltronics	www.cooperet.com
Würth-Midcom	www.we-online.com
Vishay	www.vishay.com

Loop Compensation

The LT3954 uses an internal transconductance error amplifier whose V_C output compensates the control loop. The external inductor, output capacitor and the compensation resistor and capacitor determine the loop stability. The inductor and output capacitor are chosen based on performance, size and cost. The compensation resistor and capacitor at VC are selected to optimize control loop response and stability. For typical LED applications, a 4.7nF compensation capacitor at VC is adequate, and a series resistor should always be used to increase the slew rate on the VC pin to maintain tighter regulation of LED current during fast transients on the input supply to the converter.

Disconnect Switch Selection

An NMOS in series with the LED string at the cathode is recommended in most LT3954 applications to improve the PWM dimming. The NMOS BV_{DSS} rating should be as high as the open LED regulation voltage set by the FB pin, which is typically the same rating as the power switch of the converter. The maximum continuous drain current $I_{D(MAX)}$ rating should be higher than the maximum LED current.

A PMOS high side disconnect is needed for buck mode, buck-boost mode or an output short circuit protected boost. A level shift to drive the PMOS switch is shown in the application schematic Boost LED Driver with Output Short Circuit Protection. In the case of a high side disconnect follow the same guidelines as for the NMOS regarding voltage and current ratings. It is important to include a bypass diode to GND at the drain of the PMOS switch to ensure that the voltage rating of this switch is not exceeded during transient fault events.

The DC-Coupling Capacitor Selection for SEPIC LED Driver

The DC voltage rating of the DC-coupling capacitor C_{DC} connected between the primary and secondary inductors of a SEPIC should be larger than the maximum input voltage:

$$V_{CDC} > V_{IN(MAX)}$$

C_{DC} has nearly a rectangular current waveform. During the switch off-time, the current through C_{DC} is I_{VIN}, while approximately $-I_{LED}$ flows during the on-time. The C_{DC} voltage ripple causes current distortions on the primary and secondary inductors. The C_{DC} should be sized to limit its voltage ripple. The power loss on the C_{DC} ESR reduces

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the LED driver efficiency. Therefore, the sufficient low ESR ceramic capacitors should be selected. The X5R or X7R ceramic capacitor is recommended for C_{DC}.

Short-Circuit Protection for a Boosted Output

The LT3954 has two features that provide protection from a shorted circuit load on a boost. The first of these is the ISP/ISN based overcurrent response. The second is the FB overvoltage response. The primary mode of action for both features is to drive the PWMOUT pin low, which turns off the switch connecting the output to the load. The ISP/ISN short-circuit protection also drives the PWM and DIM/SS pins low for a brief period of time. For best protection, a PMOS disconnect switch M1 is placed as shown in Figure 10. During an overcurrent event caused by a short across the LED string, the current in Rs increases until PNP Q1 turns on and pulls up the gate of M1, throttling back the current. In approximately 1µs, the ISP/ISN overcurrent response will cause the PWMOUT pin to drive low, which will turn off M1 altogether. If an external PWM signal is used, then the circuit including Q3, the 1N4148 diode and two resistors must be used to ensure the switch remains off while the output is in a faulted state. This sub-circuit drives the FB pin into the overvoltage state

If the PWM pin is configured (with a capacitor load) as shown in the application titled Boost LED Driver with Output Short Protection, then the small circuit driving FB may be omitted. In this case, the boost converter will demonstrate a hiccup mode response, turning on M1 at an interval determined by the PWM capacitor, then turning off after ~1µs due to excessive current, until the fault clears.

Board Layout

The high speed operation of the LT3954 demands careful attention to board layout and component placement. The exposed pads of the package are important for thermal management of the IC. It is crucial to achieve a good electrical and thermal contact between the GND exposed pad and the ground plane of the board. To reduce electromagnetic interference (EMI), it is important to minimize the area of the high dV/dt switching node between the inductor,

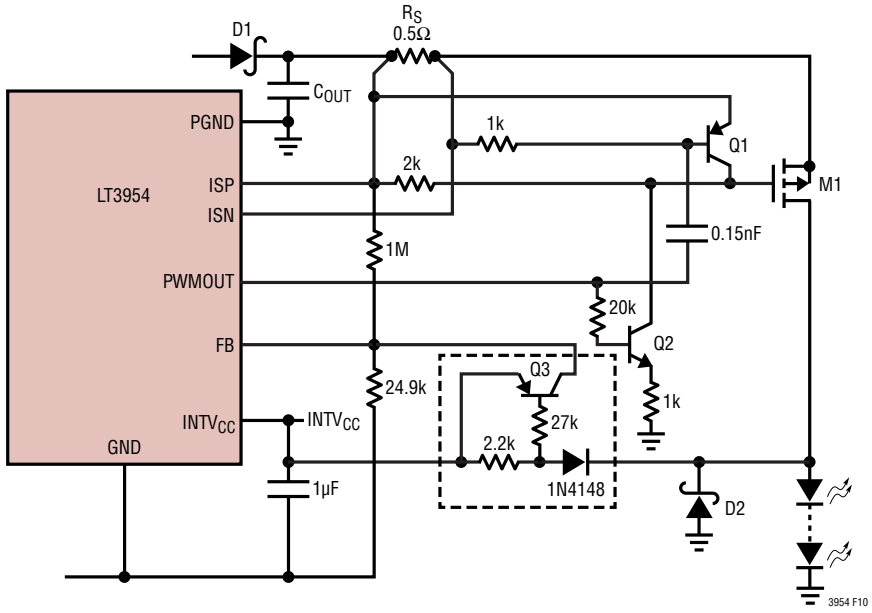

Figure 10. Protection Circuit for Fault to Ground on LED Load. Includes Fast Level Shift for PWM Switch M1

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SW pin and anode of the Schottky rectifier. Use a ground plane under the switching node to eliminate interplane coupling to sensitive signals. The lengths of the high dI/dt traces from the switch node through the Schottky rectifier and filter capacitor to PGND, should be minimized. The output capacitors should terminate as close as possible to the PGND pins. The PGND and GND planes on the PCB should not be connected together. Instead, a single pin named GNDK (Pin 12) should be connected to the GND plane and pins through vias. This pin is internally attached to the PGND pins, but provides a proper connection between the GND and PGND pins when the IC is placed on the PCB, as shown in the suggested layout (Figure 11). Likewise, the ground terminal of the bypass capacitor for the $INTV_{CC}$ regulator should be placed near the GND of the IC. The ground for the compensation network and other DC control signals should be star connected to the GND Exposed Pad of the IC. Do not extensively route high impedance signals such as FB and V_C, as they may pick up switching noise. Since there is a small variable DC input bias current to the ISN and ISP inputs, resistance in series with these pins should be minimized to avoid creating an offset in the current sense threshold.

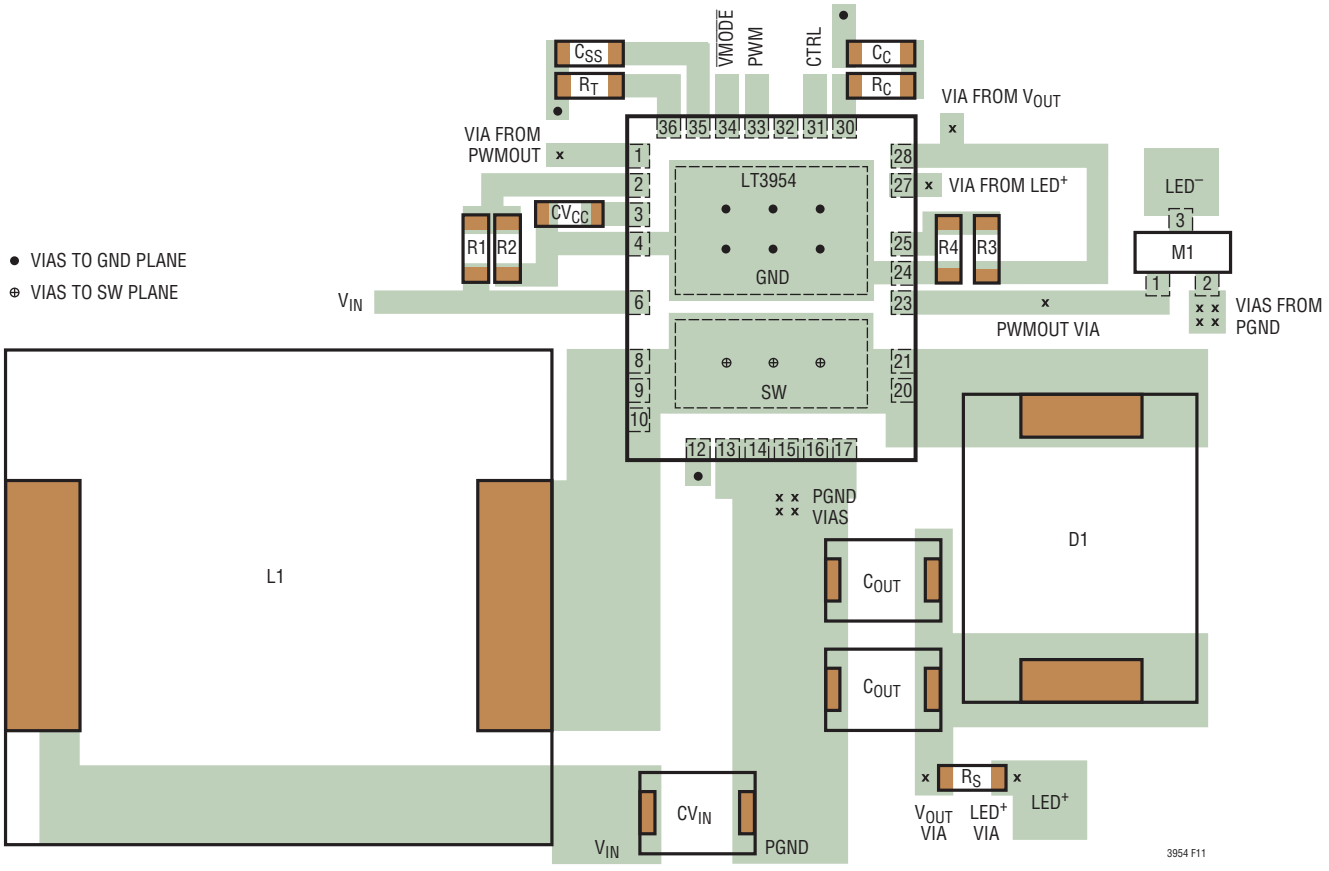
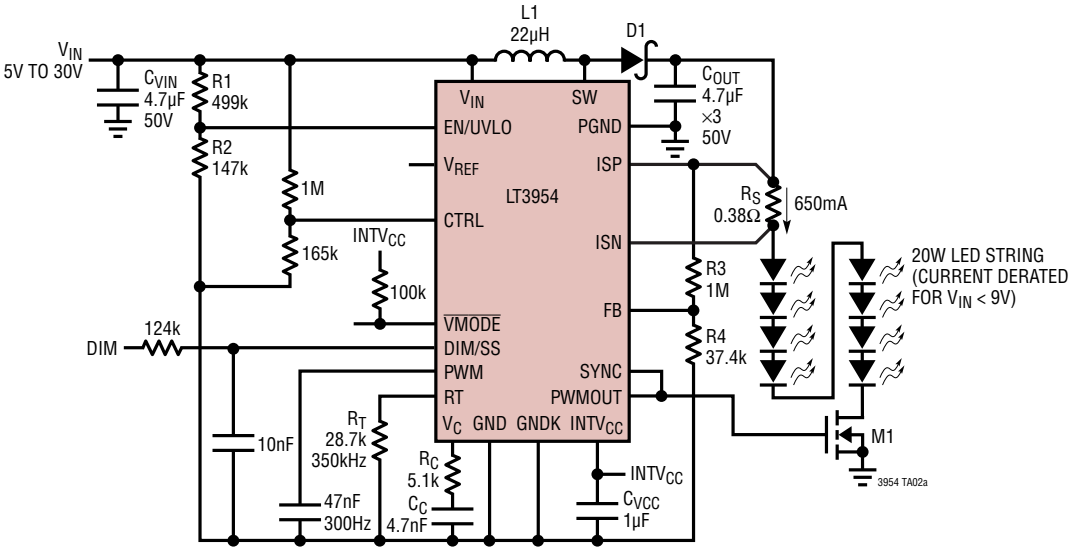


Figure 11. Boost Converter Suggested Layout

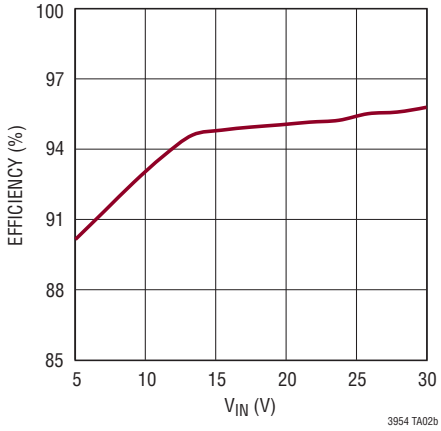
TYPICAL APPLICATION

95% Efficiency 20W Boost LED Driver with Internal PWM Dimming



M1: VISHAY Si4840BDY
L1: COILTRONICS DR125-220-R
D1: DIODES PDS3100

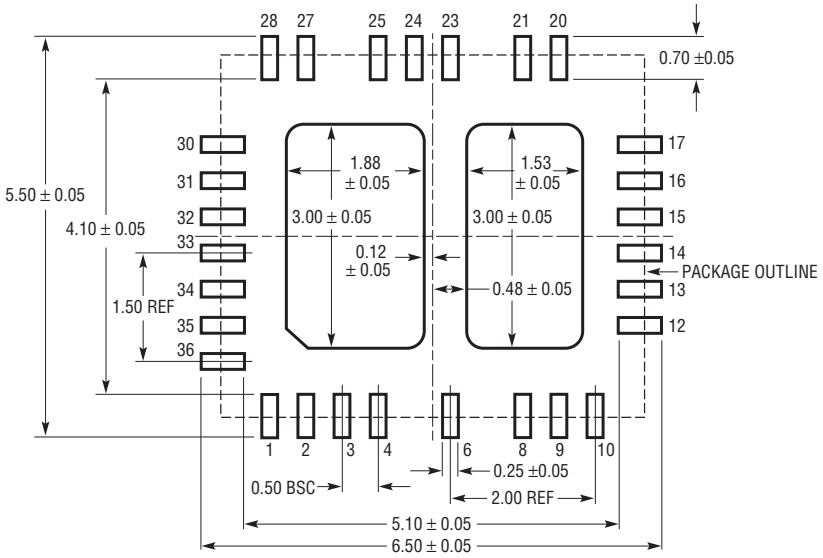
Efficiency vs V_{IN}



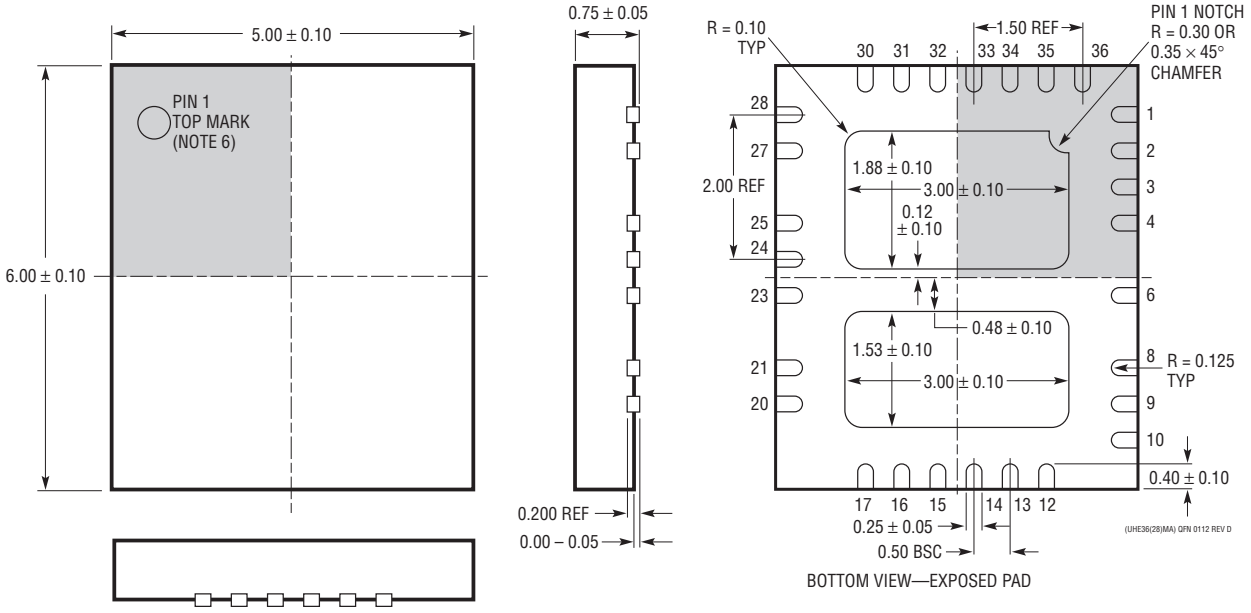
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

UHE Package
Variation: UHE36(28)MA
36(28)-Lead Plastic QFN (5mm × 6mm)
(Reference LTC DWG # 05-08-1836 Rev D)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	6/15	Clarified EN/ULVO Graph	4, 7
		Clarified PWM (Pin 32) Description	9
		Clarified Internal PWM Oscillator Operation	15,16
		Clarified Short-Circuit Protection for a Boosted Output Section	21
		Clarified Figure 10	21