8-Switch Matrix LED Dimmer

FEATURES

- Eight Independent 17V 330mΩ NMOS Switches
- Independent On/Off/Dimming Control of 1 to 4 LEDs for Each Switch
- I²C Multidrop Serial Interface with Programmable Open LED and Shorted LED Fault Reporting
- 16 Unique I²C Addresses
- V_{DD} Range: 2.7V to 5.5V and V_{IN} Range: 8V to 60V
- Digital Programmable 256:1 PWM Dimming
- Fade Transition Between PWM Dimming States
- Optional Internal Clock Generator or External Clock Source for PWM Dimming
- Open LED Overvoltage Protection
- Flicker Free PWM Dimming
- AEC-Q100 Qualified for Automotive Applications

APPLICATIONS

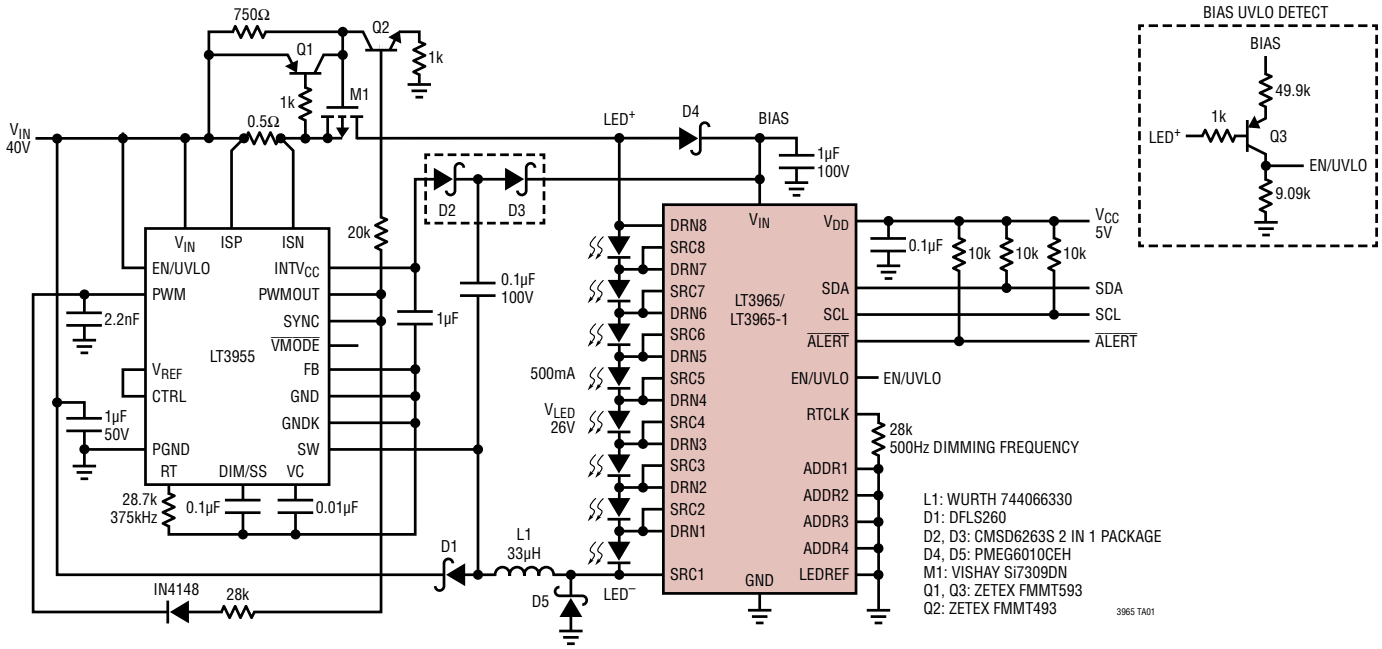
- Automotive LED Headlight Clusters
- Large LED Displays
- Automated Camera Flash Equipment
- RGBW Color Mixing Lighting

DESCRIPTION

The LT®3965/LT3965-1 is an LED bypass switching device for dimming individual LEDs in a string using a common current source. It features eight individually controlled floating source 17V/330mΩ NMOS switches. The eight switches can be connected in parallel and/or in series to bypass current around one or more LEDs in a string. The LT3965 is initialized with all switches off (LEDs on), and the LT3965-1 is initialized with all switches on (LEDs off)The LT3965/LT3965-1 uses the I²C serial interface to communicate with the microcontroller. Each of the eight channels can be independently programmed to bypass the LED string in constant on or off, or PWM dimming with or without fade transition. Using the fade option provides 11-bit resolution logarithmic transition between PWM dimming states. The LT3965/LT3965-1 provides an internal clock generator and also supports external clock source for PWM dimming. The LT3965/LT3965-1 reports fault conditions for each channel such as open LED and shorted LED. The four address select pins allow 16 LT3965/LT3965-1 devices to share the I²C bus. The device is available in a 28-lead TSSOP package.

TYPICAL APPLICATION

Matrix LED Dimmer Powered by a Buck Mode LED Driver



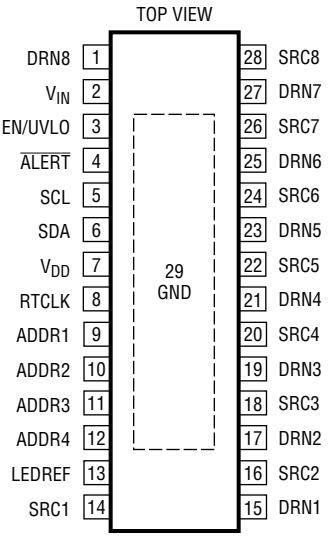
Rev. B

ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN} 60V
V_{IN}-SRC[8:1] .....–0.3V
DRN[8:1] 60V
SRC[8:1].....60V
LEDREF.....60V
DRN[8:1]-SRC[8:1] (Each Channel) .....–0.3V, 25V
EN/UVLO.....12V
V_{DD} 6V
SDA, SCL, $\overline{ALERT}$ ..... –0.3V to V_{DD} + 0.3V
RTCLK.....6V
ADDR[4:1] 6V
Operating Junction Temperature Range (Note 2)
LT3965E/LT3965E-1/LT3965I/LT3965I-1 –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



FE PACKAGE
28-LEAD PLASTIC TSSOP

θ_{JC} = 10°C/W
EXPOSED PAD (PIN 29) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3965EFE#PBF	LT3965EFE#TRPBF	LT3965FE	28-Lead Plastic TSSOP	–40°C to 125°C
LT3965EFE-1#PBF	LT3965EFE-1#TRPBF	LT39651FE	28-Lead Plastic TSSOP	–40°C to 125°C
LT3965IFE#PBF	LT3965IFE#TRPBF	LT3965FE	28-Lead Plastic TSSOP	–40°C to 125°C
LT3965IFE-1#PBF	LT3965IFE-1#TRPBF	LT39651FE	28-Lead Plastic TSSOP	–40°C to 125°C
AUTOMOTIVE PRODUCTS**				
LT3965EFE#WPBF	LT3965EFE#WTRPBF	LT3965FE	28-Lead Plastic TSSOP	–40°C to 125°C
LT3965IFE#WPBF	LT3965IFE#WTRPBF	LT3965FE	28-Lead Plastic TSSOP	–40°C to 125°C
LT3965EFE-1#WPBF	LT3965EFE-1#WTRPBF	LT39651FE	28-Lead Plastic TSSOP	–40°C to 125°C
LT3965IFE-1#WPBF	LT3965IFE-1#WTRPBF	LT39651FE	28-Lead Plastic TSSOP	–40°C to 125°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

**Versions of this part are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. These models are designated with a #W suffix. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 40V, V_{DD} = EN/UVLO = 5V, LEDREF = 3V, SRC = 0V, ADDR[4:1] not connected, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD} Input Supply Voltage		●	2.7		5.5	V
V_{DD} Operating I_Q	SCL = SDA =5V (I^2C Bus Idle), R_{TCLK} = 28k			1.3	1.8	mA
V_{DD} Shutdown I_Q	EN/UVLO < 0.4V EN/UVLO = 1.15V			0.1	1 8	µA µA
V_{IN} Operating Voltage	All Channels V_{OTH}[1:0] = V_{STH}[1:0] = "00" (Note 3)	●	8		60	V
V_{IN} Operating I_Q (Channel Not Switching)	All Channels V_{OTH}[1:0] = V_{STH}[1:0] = "00", LED ON			1	1.4	mA
	All Channels V_{OTH}[1:0] = V_{STH}[1:0] = "11", LED OFF			2.5	3.3	mA
	All Channels V_{OTH}[1:0] = "11", V_{STH}[1:0] = "00", LED ON			1.5	2	mA
V_{IN} Shutdown I_Q	EN/UVLO < 1.15V			0.1	1	µA
DRN[8:1] Operating Voltage		●			V_{IN} – 3V	V
SRC[8:1] Operating Voltage		●			V_{IN} – 7.1V	V
Current Out of SRC[8:1] Pins (Each Channel)	Channel LED Is On (Channel Switch Is Off) Channel LED Is Off (Channel Switch Is On)	● ●		9 40	13 55	µA µA
Switch On-Resistance				330		mΩ
Switch Leakage Current	DRN = 16V, V_{OTH}[1:0] = 11				5	µA
Switch Transition Time (t_r/t_f)	DRN to 10V through 50Ω Resistor		0.35	0.5	0.65	µs
DRN[8:1] to SRC[8:1] Crowbar Protection Clamp Voltage	LED or Switch Bypass Current is 500mA	●		22	25	V
Response Time from SW Crowbar Protection to SW Secure Protection	LED or Switch Bypass Current is 500mA	●		1	1.6	µs
Programmable Open LED Threshold (V_{OTH})	V_{OTH}[1:0] = "00" (Note 3) V_{OTH}[1:0] = "01" (LT3965-1 POR State) V_{OTH}[1:0] = "10" V_{OTH}[1:0] = "11" (LT3965 POR State)	● ● ● ●	4.25 8.5 12.75 17	4.5 9 13.5 18	4.75 9.5 14.25 19	V V V V
Programmable Shorted LED Threshold (V_{STH}) for LEDREF = 0V	V_{STH}[1:0] = "00" (Note 3) V_{STH}[1:0] = "01" V_{STH}[1:0] = "10" V_{STH}[1:0] = "11"	● ● ● ●	0.85 0.85 0.85 0.85	1 1 1 1	1.15 1.2 1.25 1.3	V V V V
Programmable Shorted LED Threshold (V_{STH}) for LEDREF = 3V	V_{STH}[1:0] = "00" (Note 3) V_{STH}[1:0] = "01" V_{STH}[1:0] = "10" V_{STH}[1:0] = "11"	● ● ● ●	0.85 3.8 6.7 9.6	1 4 7 10	1.15 4.2 7.3 10.4	V V V V
Programmable Shorted LED Threshold (V_{STH}) for LEDREF ≥ 4V	V_{STH}[1:0] = "00" (Note 3) V_{STH}[1:0] = "01" V_{STH}[1:0] = "10" V_{STH}[1:0] = "11"	● ● ● ●	0.85 4.7 8.5 12.3	1 5 9 13	1.15 5.3 9.5 13.7	V V V V
EN/UVLO Threshold Voltage Falling		●	1.15	1.24	1.35	V
EN/UVLO Threshold Voltage Rising Hyst.				10		mV
EN/UVLO Input Bias Current Low	EN/UVLO = 1.15V		2.2	2.7	3.2	µA
EN/UVLO Input Bias Current High	EN/UVLO = 1.33V			10	100	nA
RTCLK Programmable Internal Oscillator or External Clock Source						
LED PWM Dimming Frequency (=RTCLK Programmed Oscillator Frequency/2048 or External Clock Frequency/2048)	R_{TCLK} = 80.6kΩ R_{TCLK} = 28kΩ R_{TCLK} = 10kΩ	● ● ●	170 450 950	195 500 1090	220 550 1250	Hz Hz Hz

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 40V, V_{DD} = EN/UVLO = 5V, LEDREF = 3V, SRC = 0V, ADDR[4:1] not connected, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
RTCLK Output Voltage (Using Internal Oscillator)	R_{TCLK} = 28kΩ		0.83	0.88	0.93	V
RTCLK Input Low Threshold (RT_{VIL})		●			0.4	V
RTCLK Input High Threshold (RT_{VIH})		●	1.5			V
RTCLK Input Clock Frequency					2.5	MHz
RTCLK Input Clock Pulse Width High (T_{RTH})			100			ns
RTCLK Input Clock Pulse Width Low (T_{RTL})			100			ns
RTCLK Input Clock Ramp Time between RT_{VIL} and RT_{VIH} (T_{RTRAMP})	T_{RTL} = 10µs				2.3	µs
Address Select						
ADDR[4:1] Input Low		●			$0.25V_{DD}$	V
ADDR[4:1] Input High		●	$0.75V_{DD}$			V
ADDR[4:1] Pull-Up Resistance to V_{DD}			300	500	700	kΩ
Alert Status Output						
$\overline{ALERT}$ Output Low Voltage	$I_{\overline{ALERT}}$ = 3mA			0.3	0.4	V
$\overline{ALERT}$ Output High Leakage Current	$\overline{ALERT}$ = 5.5V				0.1	µA
External LED Reference Voltage for Shorted LED Detection						
LEDREF Input Linear Range			0		4	V
LEDREF Input Bias Current	0V ≤ LEDREF ≤ 4V		–100		100	nA
I^2C Port (See Note 5 for I^2C Timing Diagram)						
SDA and SCL Input Threshold Rising		●	$0.7V_{DD}$			V
SDA and SCL Input Threshold Falling		●			$0.25V_{DD}$	V
SDA and SCL Input Hysteresis		●	$0.05V_{DD}$			V
SDA and SCL Input Current	SDA = SCL = 0V to 5.5V		–250		250	nA
SDA Output Low Voltage	I_{SDA} = 3mA	●			0.4	V
SCL Clock Operating Frequency		●			400	kHz
(Repeated) Start Condition Hold Time (t_{HD_STA})		●	0.6			µs
Repeated Start Condition Set-Up Time (t_{SU_STA})		●	0.6			µs
Stop Condition Setup Time (t_{SU_STO})		●	0.6			µs
Data Hold Time Output ($t_{HD\_DAT(O)}$)		●	0		900	ns
Data Hold Time Input ($t_{HD\_DAT(I)}$)		●	0			ns
Data Set-Up Time (t_{SU_DAT})		●	100			ns
SCL Clock Low Period (t_{LOW})		●	1.3			µs
SCL Clock High Period (t_{HIGH})		●	0.6			µs
Data Rise Time (t_r)	C_B = Capacitance of One BUS Line (pF) (Note 4)		$20 + 0.1C_B$		300	ns
Data Fall Time (t_f)	C_B = Capacitance of One BUS Line (pF) (Note 4)		$20 + 0.1C_B$		300	ns
Input Spike Suppression Pulse Width (t_{SP})					50	ns
Bus Free Time (t_{BUF})		●			1.3	µs

ELECTRICAL CHARACTERISTICS

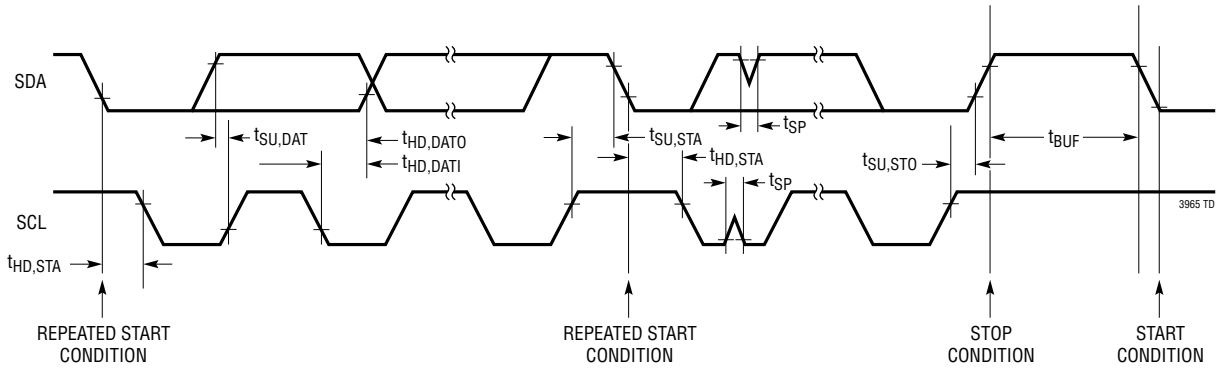
Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LT3965E/LT3965E-1 is guaranteed to meet performance specifications from the 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT3965I/LT3965I-1 is guaranteed over the full –40°C to 125°C operating junction temperature range. High junction temperatures degrade operating lifetimes. Operating lifetime is derated at junction temperatures greater than 125°C.

Note 3: V_{OTH}[1:0] and V_{STH}[1:0] register bits are set by LT3965/LT3965-1 I^2C commands. V_{OTH}/V_{STH} programmed by $V_{OTH[1:0]}/V_{STH[1:0]}$ refer to the open/shorted LED threshold between DRN and SRC of a channel. For a channel, $V_{IN} > V_{SRC} + V_{OTH} + 2.5V$ is required for accurate open LED detection.

Note 4: Rise and fall times are measured at 30% and 70% levels.

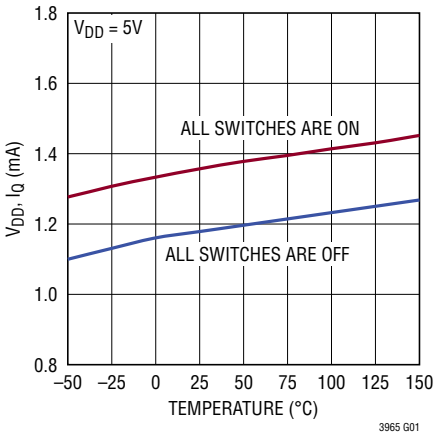
Note 5: I^2C interface timing diagram.



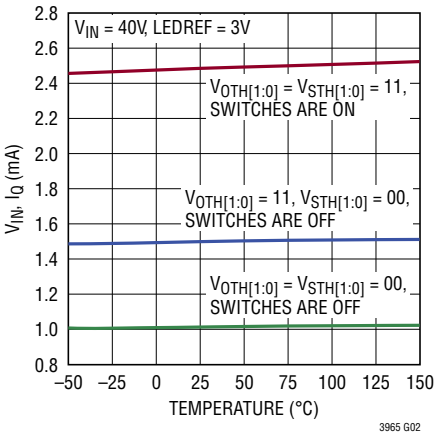
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

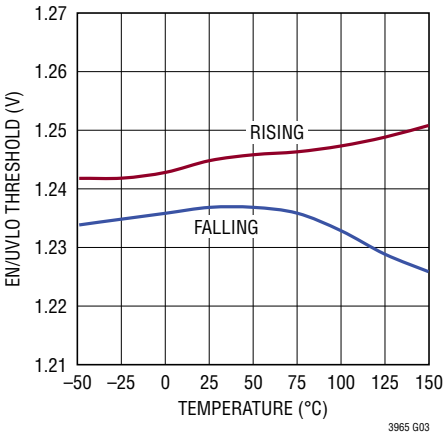
V_{DD} Quiescent Current vs Temperature



V_{IN} Quiescent Current vs Temperature

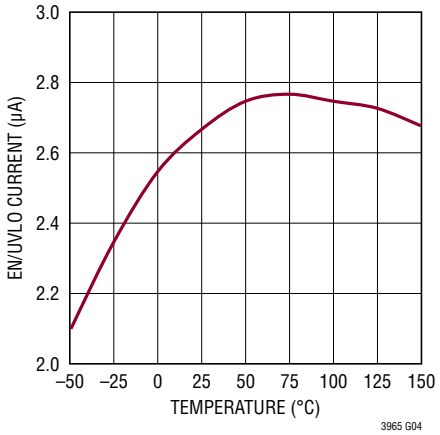


EN/UVLO Threshold vs Temperature

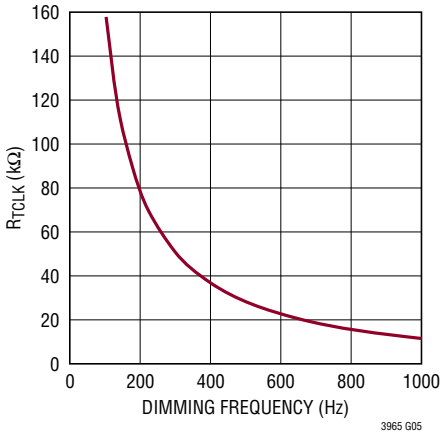


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

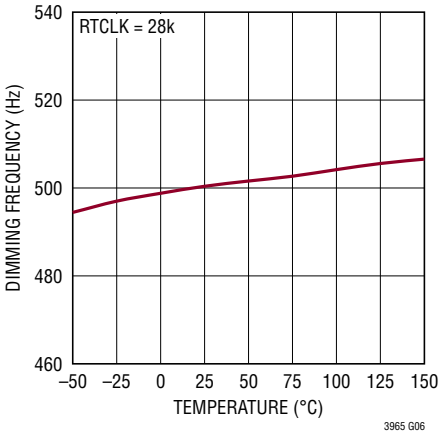
EN/UVLO Hysteresis Current vs Temperature



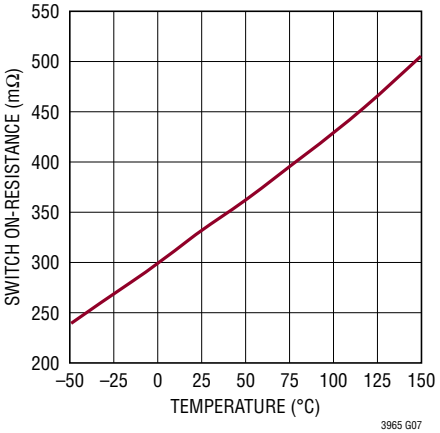
R_{TCLK} vs PWM Dimming Frequency



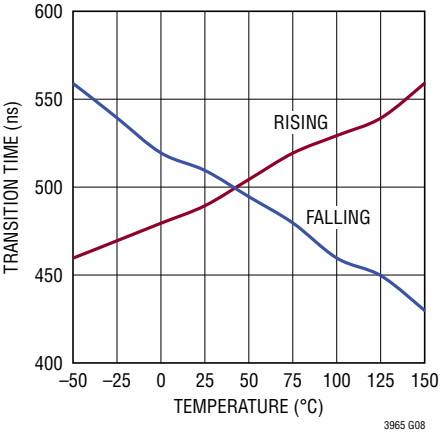
PWM Dimming Frequency vs Temperature



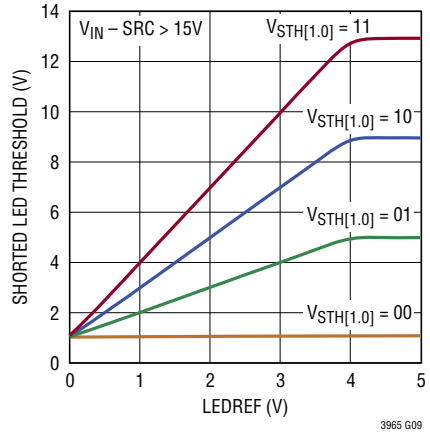
Switch On-Resistance vs Temperature



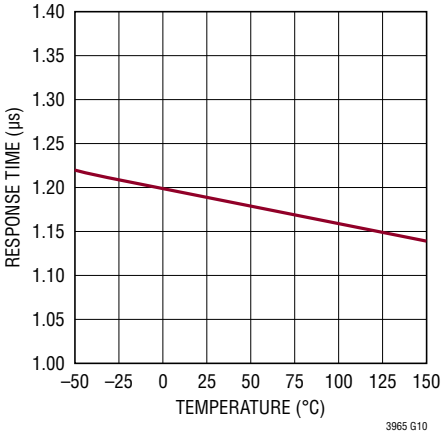
Switching Transition Time vs Temperature



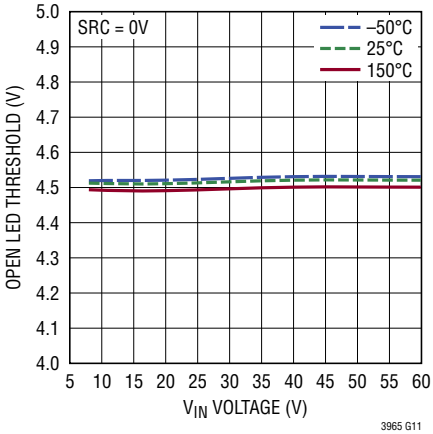
Shorted LED Threshold Falling vs LEDREF



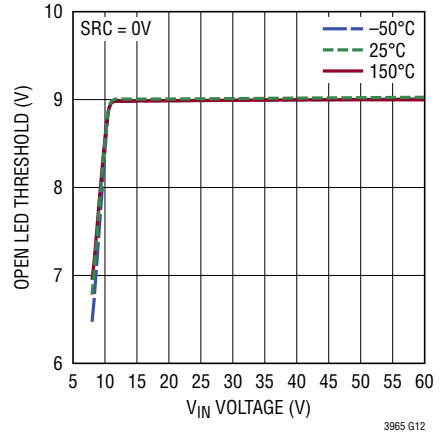
Switch Open LED Protection Response Time vs Temperature



Open LED Threshold Rising vs V_{IN}, Temperature for V_{OTH}[1:0] = 00

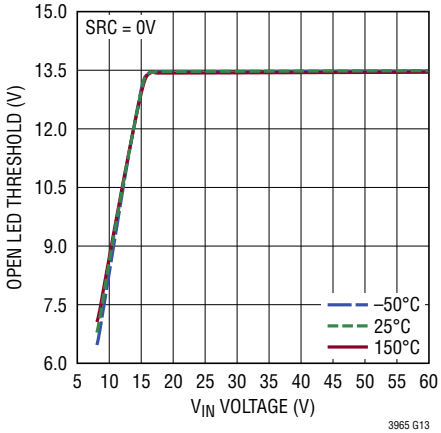


Open LED Threshold Rising vs V_{IN}, Temperature for V_{OTH}[1:0] = 01

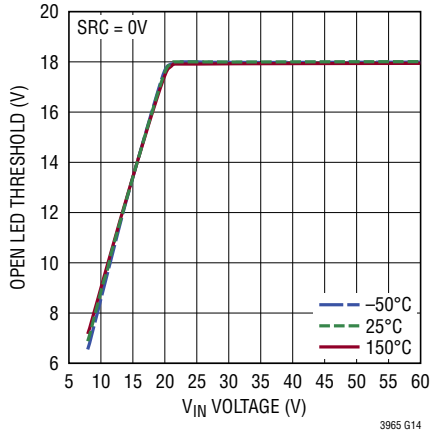


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

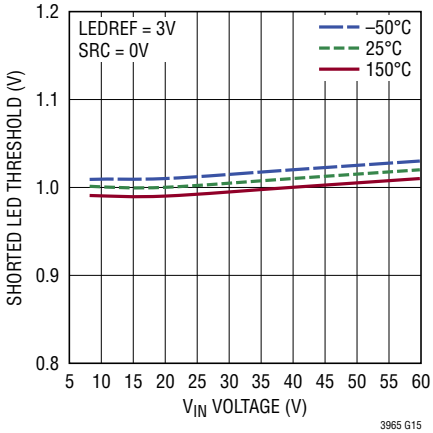
Open LED Threshold Rising vs V_{IN}, Temperature for V_{OTH}[1:0] = 10



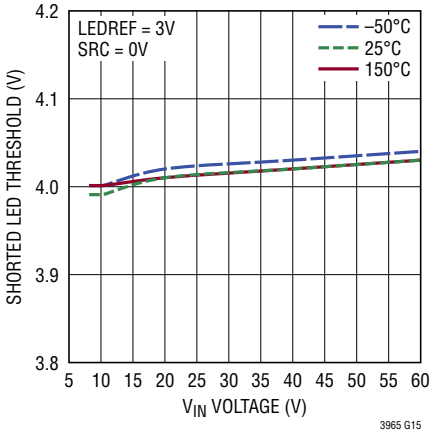
Open LED Threshold Rising vs V_{IN}, Temperature for V_{OTH}[1:0] = 11



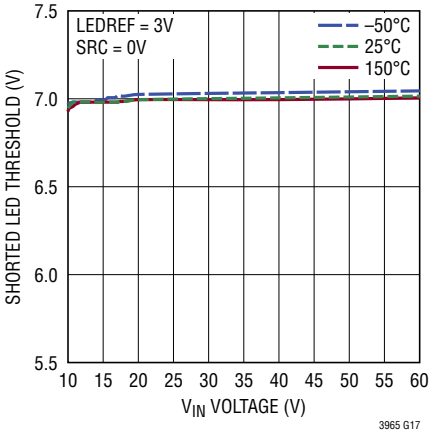
Shorted LED Threshold Falling vs V_{IN}, Temperature for V_{OTH}[1:0] = 00



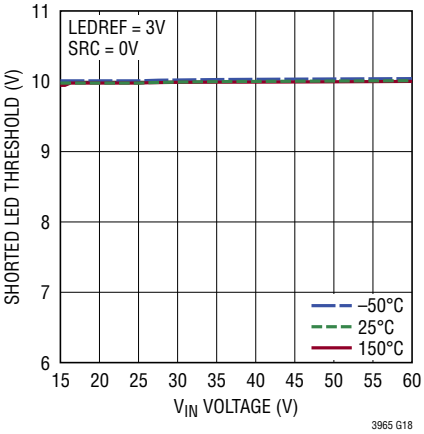
Shorted LED Threshold Falling vs V_{IN}, Temperature for V_{STH}[1:0] = 01



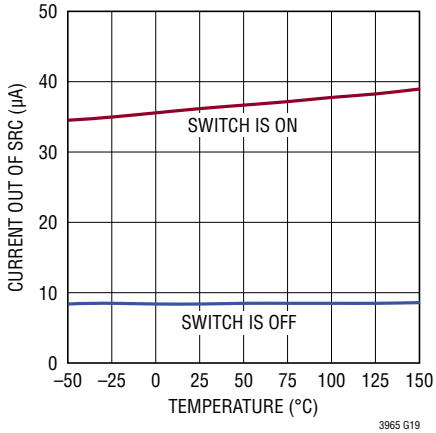
Shorted LED Threshold Falling vs V_{IN}, Temperature for V_{STH}[1:0] = 10



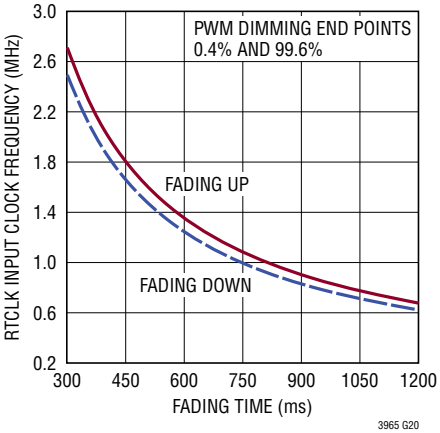
Shorted LED Threshold Falling vs V_{IN}, Temperature for V_{STH}[1:0] = 11



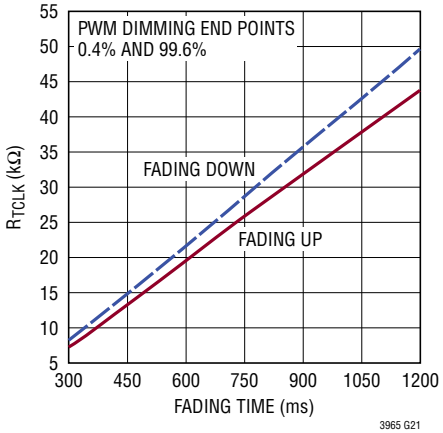
Current Out of SRC Pin vs Temperature



RTCLK Input Clock Frequency vs Fading Time



R_{TCLK} vs Fading Time



PIN FUNCTIONS

V_{IN}: Input Supply Pin for LED Bypass Switches and Fault Detectors. Must be locally by-passed with a 1µF (or larger) capacitor placed close to this pin. For proper channel switch bypass operation, V_{IN} must be at least 7.1V higher than channel source voltage.

EN/UVLO: Shutdown and Undervoltage Detect Pin. An accurate 1.24V (nominal) falling threshold with externally programmable hysteresis detects when V_{IN} – SRC is okay to enable the part. Rising hysteresis is generated by an external resistor and an accurate internal 2.7µA pull-down current. EN/UVLO going high (from below the falling threshold to above the rising threshold) resets the device to an initial power-on condition, which all registers are loaded with a default value. Tie to 0.4V, or less, to disable the device and reduce V_{DD} and V_{IN} quiescent current below 1µA. Typically this pin is tied to a PNP based level shifter to ensure the part is enabled only when V_{IN} is at least 7.1V higher than channel source voltage.

$\overline{\text{ALERT}}$: Alert Output for Fault Condition Report. $\overline{\text{ALERT}}$ pin is asserted (pulled low) to indicate that an open LED fault condition or/and a shorted LED fault condition or/and an overheat fault condition are detected. The $\overline{\text{ALERT}}$ pin is deasserted (released to high) after the part sends its Alert Response Address successfully or the fault condition is cleared by an I^2C write command.

RTCLK: External PWM Clock Input and Internal Oscillator Frequency Programming Pin. Set the internal oscillator frequency using a resistor to GND if the internal oscillator is used for PWM dimming. An external clock source able to sink 500µA at 0.4V can be used for PWM dimming by driving RTCLK above and below V_{IH} and V_{IL} respectively to override the internal oscillator. Do not leave the RTCLK pin open. Place the resistor close to the IC if a resistor is used to set the internal oscillator frequency. LED PWM dimming frequency equals the programmed internal oscillator frequency divided by 2048 or the external clock frequency divided by 2048.

LEDREF: LED Reference Voltage Input. This pin is used to set the normal operating V_F of the LED. The shorted LED threshold V_{STH} can be programmed through I^2C Serial Interface to one of the following four values: 1V, V_{LEDREF} + 1V, 2 • V_{LEDREF} + 1V and 3 • V_{LEDREF} + 1V. Connecting this pin to GND sets the shorted LED threshold to 1V. The internal value of V_{LEDREF} becomes fixed at 4V if more than 4V is applied to this pin. Do not leave this pin open.

V_{DD}: Supply Voltage for I^2C Serial Port and Input Supply Pin for Internal Bias and Logic. This pin sets the logic reference level of I^2C SCL and SDA pins. SCL and SDA logic levels are scaled to V_{DD}. When the V_{DD} pin is 2.7V or above, the I^2C interface is active. The LT3965/LT3965-1 will acknowledge communications to its address and data can be written to and read back from LT3965/LT3965-1 registers. This is true even if EN/UVLO is low. However, when EN/UVLO goes high, the LT3965/LT3965-1 resets all registers to default values (see Table 1 and Table 2 for default values). Connect a 0.1µF (or larger) decoupling capacitor from this pin to ground.

SCL: Clock Input Pin for the I^2C Serial Port. The I^2C logic levels are scaled with respect to V_{DD}.

SDA: Data Input and Output Pin for the I^2C Serial Port. The I^2C logic levels are scaled with respect to V_{DD}.

ADDR[4:1]: Programmable Address Select Pins. The device address is 010xxxx0 for all channel mode (ACMODE) write, 010xxxx1 for all channel mode (ACMODE) read, 101xxxx0 for single channel mode (SCMODE) write, and 101xxxx1 for single channel mode (SCMODE) read. ADDR[4] is MSB and ADDR[1] is LSB. A total of 16 LT3965/LT3965-1 devices can be connected to the same I^2C bus. ADDR[4:1] are pulled up to V_{DD} through a 500k resistor inside the LT3965/LT3965-1, so ADDR[4:1] default value is 1111. Each bit of ADDR[4:1] default value can be overwritten by connecting the pin to the ground. For robust design, use an external resistor to connect ADDR pins to V_{DD} or to GND.

DRN[8:1]: Floating N-Channel FET Drain Side Pins. Tie to V_{DD} with a 100k resistor if not used.

SRC[8:1]: Floating N-Channel FET Source Side Pins. The channel source voltage (SRC[8:1]) must be at least 7.1V lower than V_{IN} for proper channel switch bypass operation. Tie to GND if not used.

GND: Exposed Pad Pin. Solder the exposed pad directly to ground plane (GND).

BLOCK DIAGRAM

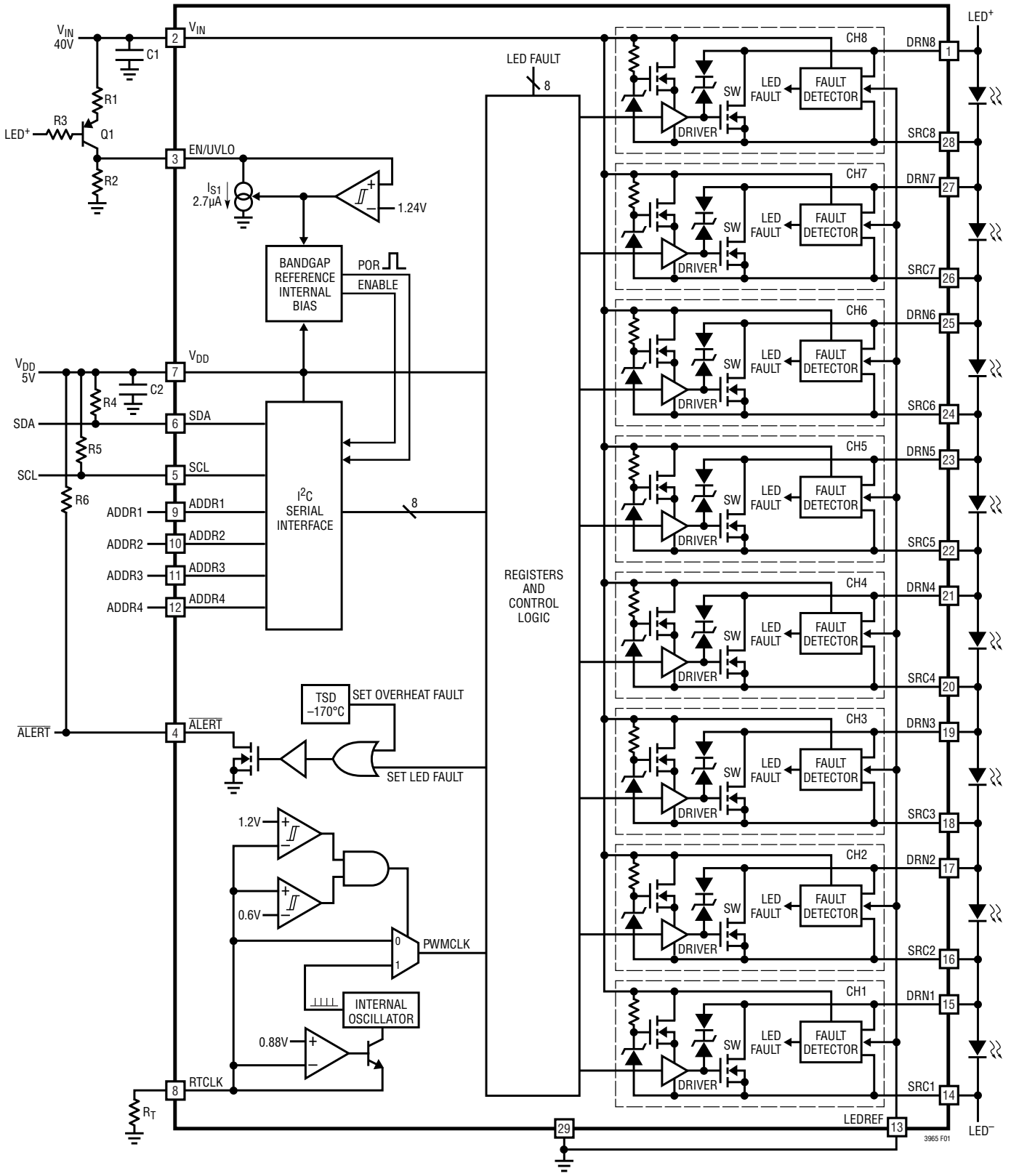


Figure 1. Block Diagram

APPLICATIONS INFORMATION

OVERVIEW

The LT3965/LT3965-1 is an 8-channel LED bypass switching device with I²C serial interface, designed for dimming LED strings using a common current source. Each of the eight channels can be independently programmed to bypass the LED string in constant on or off, or dimming with or without fade transition. Operation can be best understood by referring to the block diagram in Figure 1.

The LT3965/LT3965-1 operates over the V_{DD} input supply range of 2.7V to 5.5V. The eight channel switches are powered by the V_{IN} input supply and can be connected in parallel and/or in series. Each of the eight channel switches can bypass one or more LEDs up to 17V in a string.

Each channel has an LED fault detector which can be programmed to detect an open LED fault at one of the four threshold levels: 4.5V, 9V (default setting of LT3965-1), 13.5V and 18V (default setting of LT3965). If EN/UVLO is high, when an open LED fault is detected in a channel, the channel switch will be turned on to bypass the faulty LED to maintain the continuity of the string and for self protection. The PWM dimming for this channel is interrupted until reset by the serial interface. With a proper LED reference voltage (<4V) applied to the LEDREF pin, each channel LED fault detector can be programmed to detect a single-shorted LED fault (default setting), a 2-shorted LED fault, a 3-shorted LED fault or a 4-shorted LED fault in a multi-LED segment. When a shorted LED fault is detected in a channel, the channel switch will continue with the programmed PWM dimming. Besides LED faults, the LT3965/LT3965-1 also detects and reports an overheat fault condition (≥170°C). The LT3965/LT3965-1 asserts (pulls down) the $\overline{\text{ALERT}}$ pin to interrupt the bus master when an LED fault and/or an overheat fault is detected. The master can use the alert response address (ARA) to determine which device is sending the alert.

The LT3965/LT3965-1 I²C serial interface contains nine command registers for configuring channel switches and LED fault detectors. It also contains two read-only fault status registers for reporting the LED and overheat faults.

The I²C serial interface supports random addressing of any register. The LT3965/LT3965-1 address select pins ADDR4, ADDR3, ADDR2 and ADDR1 allow up to 16 LT3965/LT3965-1 devices to share the I²C bus.

If a resistor is connected between the RTCLK pin and the ground, the internal oscillator is chosen and the LED dimming frequency is set by the resistor. If the RTCLK pin is driven by an external clock source, the external clock source is used to override the internal oscillator and the dimming frequency equals the external clock frequency divided by 2048.

DIFFERENCES BETWEEN LT3965 AND LT3965-1

The LT3965 and the LT3965-1 have different default command register values, which result in different initial switch states and different open LED threshold settings after POR (Power On Reset). Otherwise they are the same (see Table 1 and Table 2 for default register values).

Details of the LT3965/LT3965-1 operation are found in the following sections.

EN/UVLO SHUTDOWN

The EN/UVLO pin resets the internal logic and controls whether the LT3965/LT3965-1 is enabled or is in shutdown state. The LT3965/LT3965-1 indicates that the part is in shutdown state by setting all OLFREG and SLFREG register bits high and deasserting the $\overline{\text{ALERT}}$ pin. In the shutdown state, the serial interface is alive as long as V_{DD} is applied. Any data written while EN/UVLO is low will be reset when it transitions high. The eight channel switches are off and the alert function is disabled in shutdown condition. Because V_{IN} must be at least 7.1V higher than the channel source voltage for proper channel switch bypass operation, it is recommended to enable the IC when V_{IN} is at least 7.1V higher than V_{LED}^+. The PNP based level shifter shown in Figure 1 can be used to generate EN/UVLO input signal. A micropower 1.24V reference, a comparator and controllable current source, I_{S1}, allow the user to accurately program the $V_{IN} - V_{LED}^+$ voltage at which the IC turns on and off (see Figure 1). When EN/UVLO is above 0.7V, and below the 1.24V threshold, the small pull-down current source, I_{S1}, (typical 2.7µA) is active. The purpose of this current is to allow the user to program the rising hysteresis. The typical falling threshold voltage and rising threshold voltage can be calculated by the following equations:

$$(V_{IN} - V_{LED}^+)_{(FALLING)} = 1.24 \bullet \frac{R1}{R2} + V_{BE}$$

$$(V_{IN} - V_{LED}^+)_{(RISING)} = 2.7\mu A \bullet R1 + (V_{IN} - V_{LED}^+)_{(FALLING)}$$

APPLICATIONS INFORMATION

Typically V_{BE} is 0.6V. The recommended value of R1 is 49.9k and therefore the rising hysteresis is 0.14V. Then the value of R2 can be chosen to ensure that $(V_{IN} – V_{LED}^{+})_{(FALLING)}$ is greater than 7.1V when the part is enabled.

POWER-ON RESET AND DIMMING CYCLE INITIALIZATION

When the EN/UVLO pin is toggled high, an internal power-on reset (POR) signal is generated to set all registers to their default states. The eight channel switches are in off state (all channel LEDs are on) upon the POR. The POR also initializes each channel's PWM dimming counter with one-eighth dimming cycle shift, which can avoid simultaneous channel switching at the beginning of dimming cycle to reduce switching transients (see Figure 2). When in PWM dimming mode (with or without fade transition), the channel LED string is always being turned on at the beginning of its dimming cycle. The channel LED string will be turned off if the value of the channel counter, which is clocked by the internal oscillator or an external clock source, equals the dimming value stored in the channel SCMREG command register. Once the channel LED string is turned off, it remains off until its next dimming cycle starts.

DIMMING WITHOUT FADE TRANSITION VS DIMMING WITH FADE TRANSITION

Each channel of the LT3965/LT3965-1 can be independently programmed to perform dimming without fade transition or dimming with fade transition. For dimming without fade transition, the dimming changes from the initial value to the target value in one dimming cycle. For dimming with fade transition, the dimming changes transitionally from the initial value to the target value step by step in multiple dimming cycles, following a predetermined logarithmic curve, which can favor the approximately logarithmic response of the human eye to brightness. The initial value is an existing 8-bit dimming value stored in channel SCMREG register. The target value comes from a SCMODE long format write command and will be stored in the register to replace the initial value when the STOP condition is received. For dimming with fade transition, each transitional step value is calculated using 11 bits according to the following formula: $DV_{NEXT} = DV_{PRESENT} \bullet CF$, where DV represents a transitional step dimming value, CF is a constant factor. CF is 1.0625 for up transition and 0.9375 for down transition. The transition process begins with the initial value served as the first $DV_{PRESENT}$, and ends with the target value when the last DV_{NEXT} is no less than the target value in up transition or no more than the target value in down transition.

The number of the transitional steps depends on the distance between the initial value and the target value. The maximum number of transitional steps from 1(/256) dimming to 255(/256) dimming is 100 (see Figure 3) and the maximum number of transitional steps from 255(/256) dimming to 1(/256) dimming is 92 (see Figure 4). Each step runs 4 PWM dimming cycles, and each dimming cycle consists of 2048 RTCLK clock cycles. Then $T_{STEP} = T_{PWM} \bullet 4 = T_{RTCLK} \bullet 8192$

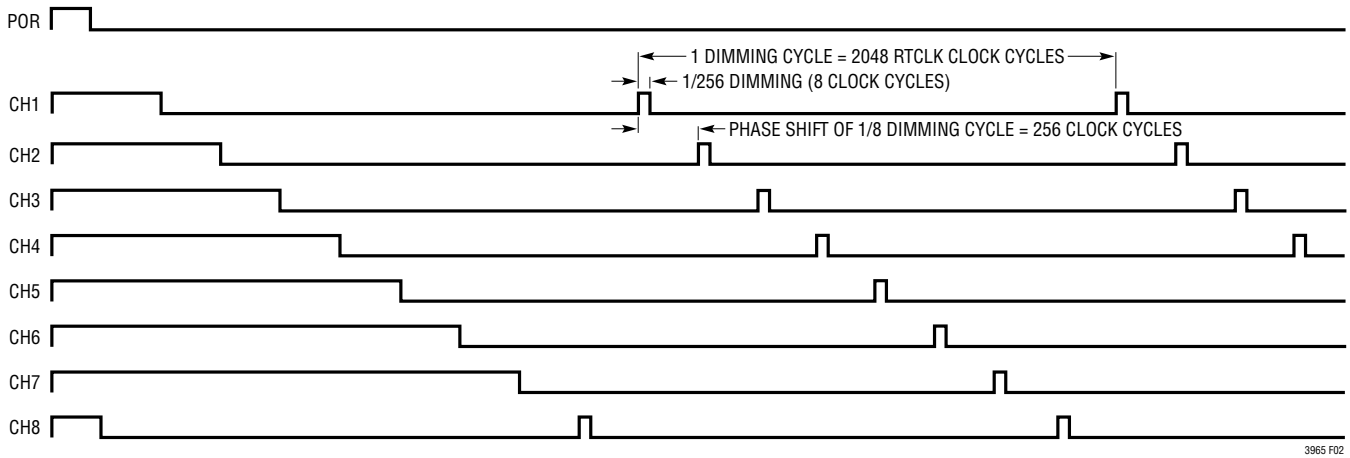


Figure 2. POR Dimming Cycle Initialization Diagram

APPLICATIONS INFORMATION

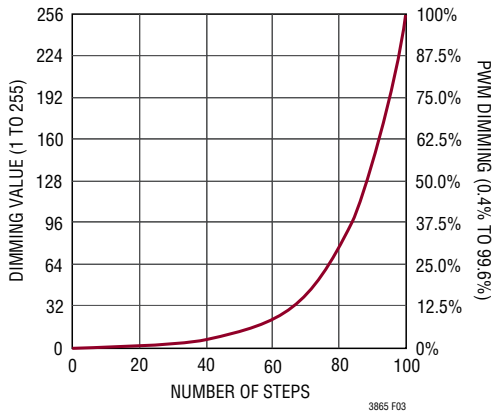


Figure 3. LT3965/LT3965-1 Up Transition Dimming Curve

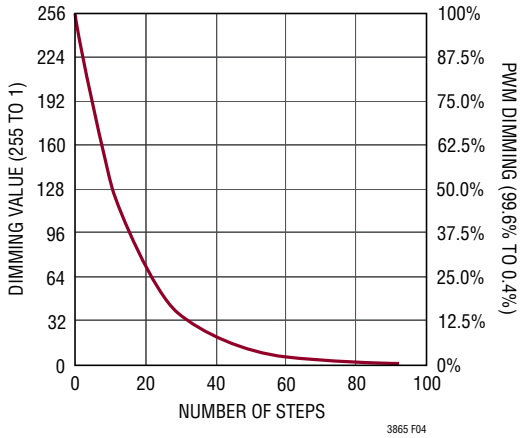


Figure 4. LT3965/LT3965-1 Down Transition Dimming Curve

LT3965/LT3965-1 I²C REGISTERS

The LT3965/LT3965-1 has nine command registers (see Table 1 and Table 2) and two read-only fault status registers (see Table 3). The command registers are used to store the configuration bits sent by a master. The fault status registers are used to store the LED/overheat fault status bits. Both the command registers and the fault status registers can be read by the master.

LT3965/LT3965-1 COMMAND REGISTERS AND CHANNEL CONTROL

Upon the POR with EN/UVLO, all eight channel switches of LT3965 are set to off, whereas all eight channel switches of LT3965-1 are set to on, which is controlled by the ACMREG register default value ("11111111" for LT3965; "00000000" for LT3965-1). After data is written, each channel switch is controlled either by the ACMODE register or by the channel SCMREG register, depending on which register has been last updated (see Figure 5). If SCMODE registers are dominant, the data in the ACMODE register is retained until it is overwritten or a POR occurs.

I²C SERIAL INTERFACE

The LT3965/LT3965-1 communicates through an I²C serial interface. The I²C serial interface is a 2-wire open-drain interface supporting multiple slaves and multiple masters on a single bus. Each device on the I²C bus is recognized by a unique address stored in the device and can only operate either as a transmitter or receiver, depending on the function of the device. A master is the device which initiates a data transfer on the bus and generates the clock signals to permit the transfer. Devices addressed by the master are considered slaves. The LT3965/LT3965-1 can only be addressed as a slave. Once addressed, it can receive configuration data or transmit register contents. The serial clock line (SCL) is always an input to the LT3965/LT3965-1 and the serial data line (SDA) is bidirectional. The LT3965/LT3965-1 can only pull the serial data line (SDA) LOW and can never drive it HIGH. SCL and SDA are required to be externally connected to the V_{DD} supply through a pull-up resistor. When the data line is not being driven LOW, it is HIGH. Data on the I²C bus can be transferred at rates up to 100kbits/s in the standard mode and up to 400kbits/s in the fast mode.

THE START AND STOP CONDITIONS

When the bus is idle, both SCL and SDA must be HIGH. A bus master signals the beginning of a transmission with a START condition by transitioning SDA from HIGH to LOW while SCL is HIGH. When the master has finished communicating with the slave, it issues a STOP condition by transitioning SDA from LOW to HIGH while SCL is HIGH. The bus is then free for another transmission. However, if the master still wishes to communicate on the bus, it can generate a repeated START condition (Sr) and address the same or another slave without first generating a STOP condition. When the bus is in use, it stays busy if a repeated START (Sr) is generated instead of a STOP

APPLICATIONS INFORMATION

Table 1. All Channel Mode (ACMODE) Command Register (8 Bits Long. See 1) All Channel Mode (ACMODE) Command section for how to access this register).

NAME	B[7]	B[6]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]	DEFAULT
ACMREG	Control Bit for CH8 1: LED On 0: LED Off	Control Bit for CH7 1: LED On 0: LED Off	Control Bit for CH6 1: LED On 0: LED Off	Control Bit for CH5 1: LED On 0: LED Off	Control Bit for CH4 1: LED On 0: LED Off	Control Bit for CH3 1: LED On 0: LED Off	Control Bit for CH2 1: LED On 0: LED Off	Control Bit for CH1 1: LED On 0: LED Off	11111111 (LT3965) 00000000 (LT3965-1)

Table 2. Single Channel Mode (SCMODE) Command Registers (14 Bits Long. See 2) Single Channel Mode (SCMODE) Command section for how to access these register bits).

NAME	B[13:12] OPEN LED THRESHOLD PROGRAMMABLE BITS	B[11:10] SHORTED LED THRESHOLD PROGRAMMABLE BITS	B[9:8] MODE CONTROL BITS	B[7:0] DIMMING VALUE	DEFAULT
SCMREG1 (for CH1, the channel address: 000)	V_{OTH}[1:0] = "00": 4.5V "01": 9.0V "10": 13.5V "11": 18.0V	V_{STH}[1:0] = "00": 1V "01": V_{LEDREF} + 1V "10": 2 • V_{LEDREF} + 1V "11": 3 • V_{LEDREF} + 1V	MC[1:0] = "00": LED Off "01": LED On "10": LED Dimming without Fade Transition "11": LED Dimming with Fade Transition	DV[7:0] = "00000001": 1/256 Dimming "00000010": 2/256 Dimming ……. "11111111": 255/256 Dimming	110001 00000001 (LT3965) 010000 00000001 (LT3965-1)
SCMREG2 (for CH2, the channel address: 001)	V_{OTH}[1:0] = "00": 4.5V "01": 9.0V "10": 13.5V "11": 18.0V	V_{STH}[1:0] = "00": 1V "01": V_{LEDREF} + 1V "10": 2 • V_{LEDREF} + 1V "11": 3 • V_{LEDREF} + 1V	MC[1:0] = "00": LED Off "01": LED On "10": LED Dimming without Fade Transition "11": LED Dimming with Fade Transition	DV[7:0] = "00000001": 1/256 Dimming "00000010": 2/256 Dimming ……. "11111111": 255/256 Dimming	110001 00000001 (LT3965) 010000 00000001 (LT3965-1)
SCMREG3 (for CH3, the channel address: 010)	V_{OTH}[1:0] = "00": 4.5V "01": 9.0V "10": 13.5V "11": 18.0V	V_{STH}[1:0] = "00": 1V "01": V_{LEDREF} + 1V "10": 2 • V_{LEDREF} + 1V "11": 3 • V_{LEDREF} + 1V	MC[1:0] = "00": LED Off "01": LED On "10": LED Dimming without Fade Transition "11": LED Dimming with Fade Transition	DV[7:0] = "00000001": 1/256 Dimming "00000010": 2/256 Dimming ……. "11111111": 255/256 Dimming	110001 00000001 (LT3965) 010000 00000001 (LT3965-1)
SCMREG4 (for CH4, the channel address: 011)	V_{OTH}[1:0] = "00": 4.5V "01": 9.0V "10": 13.5V "11": 18.0V	V_{STH}[1:0] = "00": 1V "01": V_{LEDREF} + 1V "10": 2 • V_{LEDREF} + 1V "11": 3 • V_{LEDREF} + 1V	MC[1:0] = "00": LED Off "01": LED On "10": LED Dimming without Fade Transition "11": LED Dimming with Fade Transition	DV[7:0] = "00000001": 1/256 Dimming "00000010": 2/256 Dimming ……. "11111111": 255/256 Dimming	110001 00000001 (LT3965) 010000 00000001 (LT3965-1)
SCMREG5 (for CH5, the channel address: 100)	V_{OTH}[1:0] = "00": 4.5V "01": 9.0V "10": 13.5V "11": 18.0V	V_{STH}[1:0] = "00": 1V "01": V_{LEDREF} + 1V "10": 2 • V_{LEDREF} + 1V "11": 3 • V_{LEDREF} + 1V	MC[1:0] = "00": LED Off "01": LED On "10": LED Dimming without Fade Transition "11": LED Dimming with Fade Transition	DV[7:0] = "00000001": 1/256 Dimming "00000010": 2/256 Dimming ……. "11111111": 255/256 Dimming	110001 00000001 (LT3965) 010000 00000001 (LT3965-1)
SCMREG6 (for CH6, the channel address: 101)	V_{OTH}[1:0] = "00": 4.5V "01": 9.0V "10": 13.5V "11": 18.0V	V_{STH}[1:0] = "00": 1V "01": V_{LEDREF} + 1V "10": 2 • V_{LEDREF} + 1V "11": 3 • V_{LEDREF} + 1V	MC[1:0] = "00": LED Off "01": LED On "10": LED Dimming without Fade Transition "11": LED Dimming with Fade Transition	DV[7:0] = "00000001": 1/256 Dimming "00000010": 2/256 Dimming ……. "11111111": 255/256 Dimming	110001 00000001 (LT3965) 010000 00000001 (LT3965-1)
SCMREG7 (for CH7, the channel address: 110)	V_{OTH}[1:0] = "00": 4.5V "01": 9.0V "10": 13.5V "11": 18.0V	V_{STH}[1:0] = "00": 1V "01": V_{LEDREF} + 1V "10": 2 • V_{LEDREF} + 1V "11": 3 • V_{LEDREF} + 1V	MC[1:0] = "00": LED Off "01": LED On "10": LED Dimming without Fade Transition "11": LED Dimming with Fade Transition	DV[7:0] = "00000001": 1/256 Dimming "00000010": 2/256 Dimming ……. "11111111": 255/256 Dimming	110001 00000001 (LT3965) 010000 00000001 (LT3965-1)
SCMREG8 (for CH8, the channel address: 111)	V_{OTH}[1:0] = "00": 4.5V "01": 9.0V "10": 13.5V "11": 18.0V	V_{STH}[1:0] = "00": 1V "01": V_{LEDREF} + 1V "10": 2 • V_{LEDREF} + 1V "11": 3 • V_{LEDREF} + 1V	MC[1:0] = "00": LED Off "01": LED On "10": LED Dimming without Fade Transition "11": LED Dimming with Fade Transition	DV[7:0] = "00000001": 1/256 Dimming "00000010": 2/256 Dimming ……. "11111111": 255/256 Dimming	110001 00000001 (LT3965) 010000 00000001 (LT3965-1)

Note: The dimming value range is 00000001 to 11111111. If the invalid dimming value 00000000 is received, 00000001 will be written to the register instead.

APPLICATIONS INFORMATION

Table 3. Read-Only Fault Status Register (See 1) All Channel Mode (ACMODE) Command section and 2) Single Channel Mode (SCMODE) Command section for how to access these register bits).

NAME	B[7]	B[6]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]	DEFAULT
OLFREG	Open LED Status Bit for CH8 1: Fault 0: No Fault	Open LED Status Bit for CH7 1: Fault 0: No Fault	Open LED Status Bit for CH6 1: Fault 0: No Fault	Open LED Status Bit for CH5 1: Fault 0: No Fault	Open LED Status Bit for CH4 1: Fault 0: No Fault	Open LED Status Bit for CH3 1: Fault 0: No Fault	Open LED Status Bit for CH2 1: Fault 0: No Fault	Open LED Status Bit for CH1 1: Fault 0: No Fault	00000000
SLFREG	Shorted LED Status Bit for CH8 1: Fault 0: No Fault	Shorted LED Status Bit for CH7 1: Fault 0: No Fault	Shorted LED Status Bit for CH6 1: Fault 0: No Fault	Shorted LED Status Bit for CH5 1: Fault 0: No Fault	Shorted LED Status Bit for CH4 1: Fault 0: No Fault	Shorted LED Status Bit for CH3 1: Fault 0: No Fault	Shorted LED Status Bit for CH2 1: Fault 0: No Fault	Shorted LED Status Bit for CH1 1: Fault 0: No Fault	00000000

Note: The LT3965/LT3965-1 sets all OLFREG and SLFREG register bits high and asserts the $\overline{\text{ALERT}}$ pin to indicate the overheat fault condition (≥170°C). (See LED/Overheat Fault Detection and Reporting section for detail.) The LT3965/LT3965-1 indicates that the part is in shutdown state by setting all OLFREG and SLFREG register bits high and deasserting the $\overline{\text{ALERT}}$ pin.

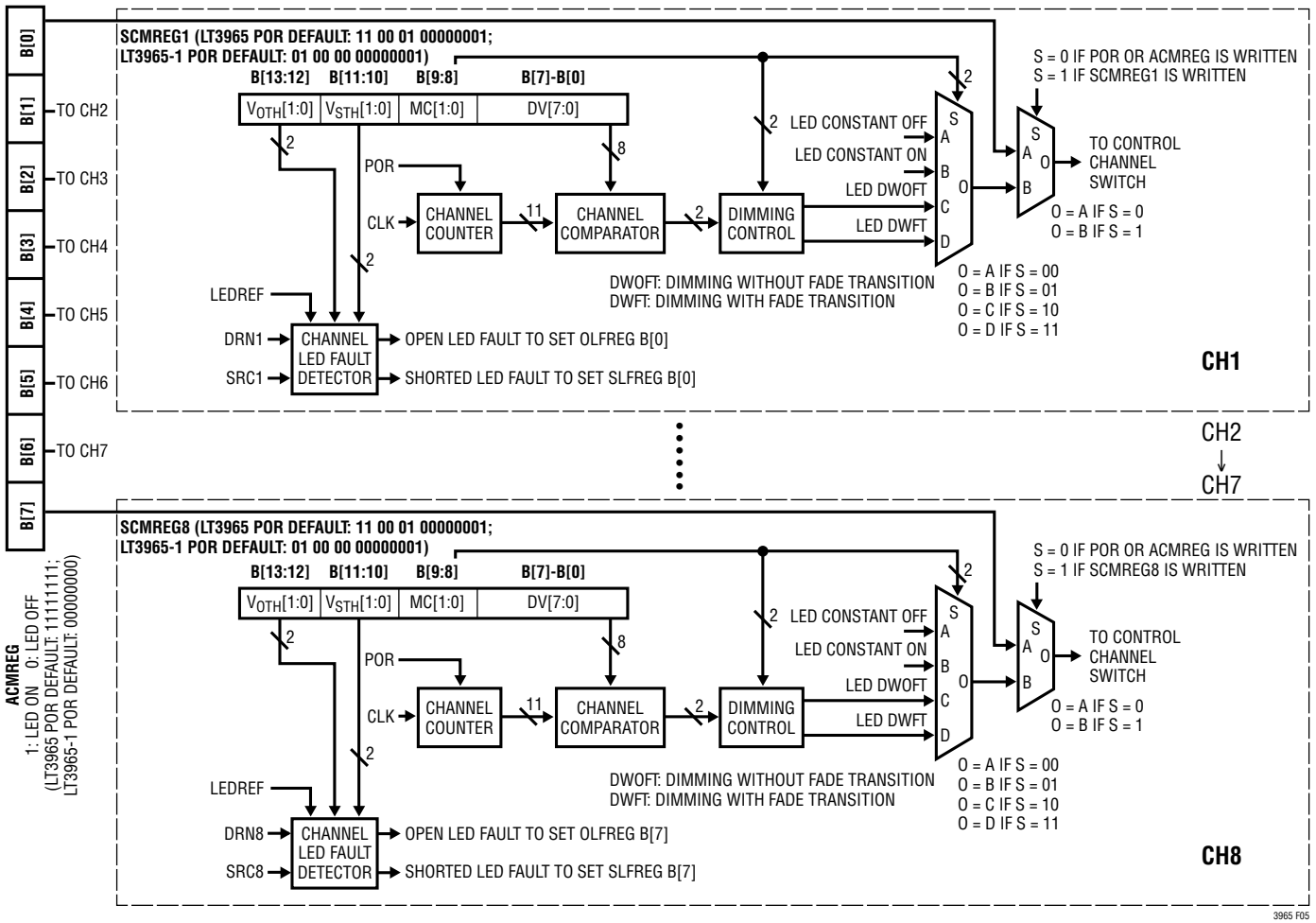


Figure 5. LT3965/LT3965-1 Command Registers and Channel Control Diagram

APPLICATIONS INFORMATION

condition. The repeated START (Sr) conditions are functionally identical to the START (S). Various combinations of read/write commands are then possible within such a transfer, except that the BCMODE write command for dimming cycle synchronization and the BCMODE read command for alert inquiry and the ACMODE write command for clearing the overheat fault bits must be self-contained with a terminating STOP condition.

I²C SERIAL PORT DATA TRANSFER

After the START condition, the I²C bus is busy and data transfer can begin between the master and the addressed LT3965/LT3965-1 slave. Data is transferred over the bus in group of nine bits, one byte followed by one acknowledge (ACK) bit. The acknowledge signal is used for handshaking between the master and the slave.

When the LT3965/LT3965-1 is written to, it acknowledges its device write address and subsequent data bytes. The data byte is transferred to an internal holding latch upon the return of its acknowledge by the LT3965/LT3965-1. If desired a repeated START (Sr) condition may be initiated by the master to address another device on the I²C bus for data transfer. The LT3965/LT3965-1 remembers the valid data it has received. Once selected channels of the devices on the I²C bus have been addressed and sent valid data, the master issues a STOP condition to finish the communication. The LT3965/LT3965-1 will update its command registers with the data it has received upon the STOP condition, except that the V_{OTH}[1:0] and V_{STH}[1:0] bits are updated in the channel SCMREG command register upon the return of its acknowledge by the LT3965/LT3965-1.

When reading from the LT3965/LT3965-1, the LT3965/LT3965-1 acknowledges its device read address and the master acknowledges subsequent data bytes it has received except the last one followed by a STOP or a repeated START condition.

The master can free the I²C bus by issuing a STOP condition after the data transfer. If desired the master can verify the data bytes written to the internal holding latches prior to updating them to the command registers by reading them back before sending a STOP condition.

LT3965/LT3965-1 I²C COMMANDS AND WRITE/READ PROTOCOLS

Only a master can issue an I²C command to start a write or read operation. The first command byte is always an I²C device address sent by a master. If the master issues a write command, all the remaining bytes of the command will be transmitted by the master. Otherwise, all the remaining bytes of the command will be transmitted by the addressed LT3965/LT3965-1 slave. The LT3965/LT3965-1 I²C commands can be divided into three categories based on their purposes:

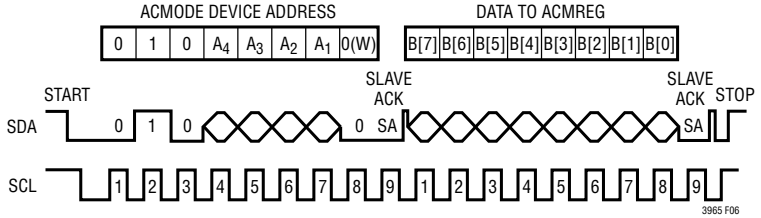


Figure 6. LT3965/LT3965-1 I²C Serial Port ACMODE Write Protocol

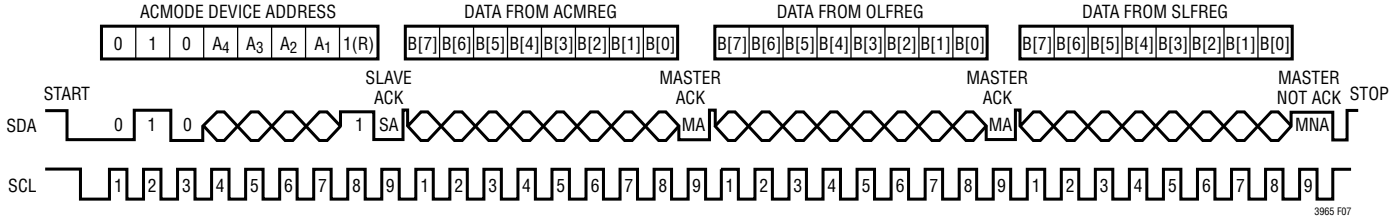


Figure 7. LT3965/LT3965-1 I²C Serial Port ACMODE Read Protocol

APPLICATIONS INFORMATION

1) All Channel Mode (ACMODE) Command

The ACMODE write command (see Figure 6) is used to set the ACMREG register bits (see Table 1) to control the eight channel switches together. The command is two bytes long. The first byte is the ACMODE device write address and the second byte is the data byte to be written to the ACMREG register.

The ACMODE read command (see Figure 7) is used to read back the ACMREG register bits and to get the LED and overheat fault conditions. The command is four bytes long. The first byte is the ACMODE device read address followed by three data bytes read respectively from the ACMREG register, the OLFREG register and the SLFREG register.

The LT3965/LT3965-1 ACMODE device address is $010A_4A_3A_2A_1$ followed by an eighth bit which is a data direction bit (R/$\overline{W}$)—a 0 indicates a write transmission (the master writes to the addressed LT3965/LT3965-1), a 1 indicates a read transmission (the master reads from the addressed LT3965/LT3965-1). $A_4A_3A_2A_1$ is an input logic value from the programmable address select pins ADDR4, ADDR3, ADDR2 and ADDR1.

ACMODE Write Command Latency

The ACMODE write command can be conveniently used for quick status control of the eight channel LEDs. Each ACMODE write command is two bytes long and takes about 47µs to transmit if 400kHz SCL clock is chosen. The command latency between the STOP condition and channel switching on (LED turning off) is about 0.3µs, and the command latency between the STOP condition and channel switching off (LED turning on) is about 1µs. Therefore, the minimum time from initiating to executing an ACMODE write command is about 48µs if 400kHz SCL clock is used.

ACMODE Write Command and Simultaneous Channel Switching

The ACMODE write command can control all 8 channels to switch together. It is possible to switch all LEDs from on/off to off/on simultaneously using a single ACMODE write command. A fast LED driver can respond well to a sudden output voltage change caused by simultaneous channel switching. An LED driver with slower response may trigger false faults due to large transients in the string current. When working with a slow LED driver, you should avoid sending an ACMODE write command which can cause simultaneous channel switching. Instead you can use multiple ACMODE write commands, and each of them makes one channel switch at a time.

2) Single Channel Mode (SCMODE) Command

The SCMODE write command is used for setting the addressed channel SCMREG register bits to control the channel switch and to set the channel LED fault detecting thresholds. The SCMODE write command has two formats: short format (see Figure 8) and long format (see Figure 9). Both the formats configure the channel SCMREG register. Choosing the short format or the long format depends on which bits of the channel SCMREG register you want to configure.

The SCMODE write command short format can program the channel open LED threshold by setting V_{OTH}[1:0] (B[13:12]) and change the channel switch mode by setting MC[1:0] (B[9:8]). The SCMODE write command long format can program the channel shorted LED threshold by setting V_{STH}[1:0] (B[11:10]) and change the channel switch mode by setting MC[1:0] (B[9:8]) and set a new dimming value by updating DV[7:0] (B[7:0]) in the channel SCMREG register.

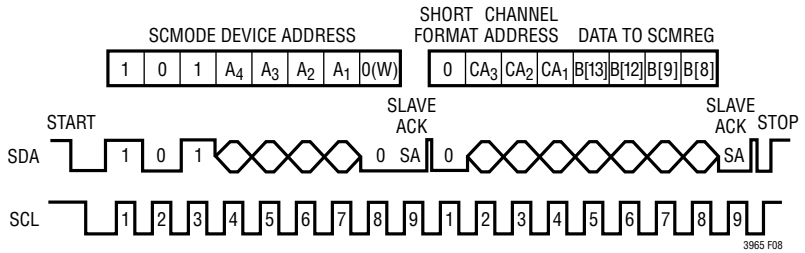


Figure 8. LT3965/LT3965-1 I²C Serial Port SCMODE Write Short Format Protocol

APPLICATIONS INFORMATION

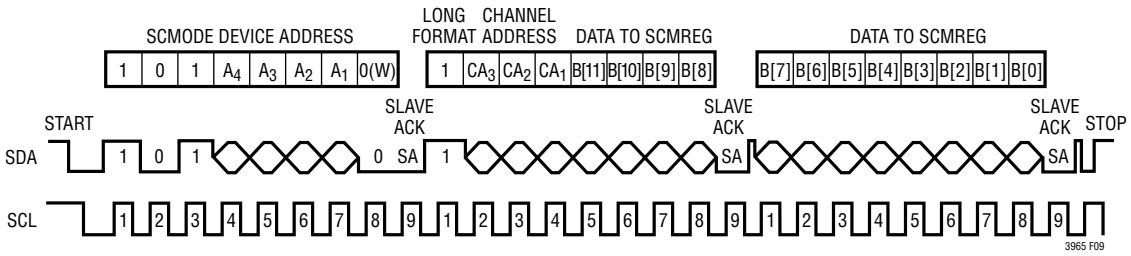


Figure 9. LT3965/LT3965-1 I²C Serial Port SCMODE Write Long Format Protocol

The SCMODE write command short format is two bytes long (see Figure 8). The first byte is the SCMODE device write address. The second byte consists of 3 sections—the first section (bit 7) must be 0 to indicate the short format, the second section (bit 6, bit 5 and bit 4) is the channel address indicating which channel SCMREG register is written to, the last section is the configuration data (bit 3, bit 2 for V_{OTH}[1:0] and bit 1, bit 0 for MC[1:0]).

The SCMODE write command long format is three bytes long (see Figure 9). The first byte is the SCMODE device write address. The second byte consists of 3 sections—the first section (bit 7) must be 1 to indicate the long format, the second section (bit 6, bit 5 and bit 4) is the channel address indicating which channel SCMREG register is written to, the last section is the configuration data (bit 3, bit 2 for V_{STH}[1:0] and bit 1, bit 0 for MC[1:0]). The third byte is the dimming value DV[7:0].

Channel Open LED Threshold (V_{OTH}) Programming

By using the SCMODE write command short format, you can overwrite B[13:12] bits (i.e., V_{OTH}[1:0]) of the channel SCMREG register to program the channel open LED threshold (refer to Table 2, Figure 8 and Figure 5).

$$V_{OTH} = 4.5V \bullet (1 + V_{OTH}[1:0])$$

Where V_{OTH}[1:0] represents the possible decimal value 0, 1, 2 or 3 of the two programmable bits. Therefore, the channel open LED threshold V_{OTH} can be programmed to one of these four values: 4.5V, 9V, 13.5V and 18V. The POR default V_{OTH} of LT3965 is 18V. The POR default V_{OTH} of LT3965-1 is 9V.

When programming V_{OTH}, please follow the advice below to avoid false detection or missed detection of open LED condition:

1) Do not set V_{OTH} to a threshold equal to or greater than the V_{IN} supply voltage. It is recommended to set V_{OTH} to a threshold at least 3V lower than the V_{IN} supply voltage.

2) Set V_{OTH} to the lowest threshold, but at least one-fifth of the V_{OTH} higher than the channel LED-on voltage. For example, if channel LED-on voltage is 3.5V or less, to set V_{OTH} to 4.5V is preferred. If channel LED-on voltage is 3.8V, to set V_{OTH} to 9V is preferred.

It is recommended to adjust the V_{OTH} from its default value (18V on LT3965; 9V on LT3965-1) to a proper threshold based on the V_{IN} supply voltage and each channel LED-on voltage, once the application circuit is powered on.

Channel Shorted LED Threshold (V_{STH}) Programming

By using the SCMODE write command long format, you can overwrite B[11:10] bits (i.e., V_{STH}[1:0]) of the channel SCMREG register to program the channel shorted LED threshold (refer to Table 2, Figure 9 and Figure 5).

$$V_{STH} = 1V + (N_{LED} - 1) \bullet V_{LEDREF}$$

$$N_{LED} = 1 + V_{STH}[1:0]$$

Where N_{LED} is the number of LEDs in series driven by the channel, which is programmed by V_{STH}[1:0], and V_{LEDREF} is a reference voltage set by the LEDREF pin (refer to the curve Shorted LED Threshold Falling vs LEDREF in Typical Performance Characteristics).

APPLICATIONS INFORMATION

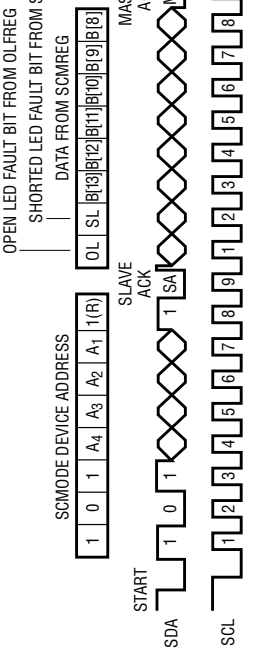


Figure 10. LT3965/LT3965-1 I²C Serial Port SCMODE Read Protocol

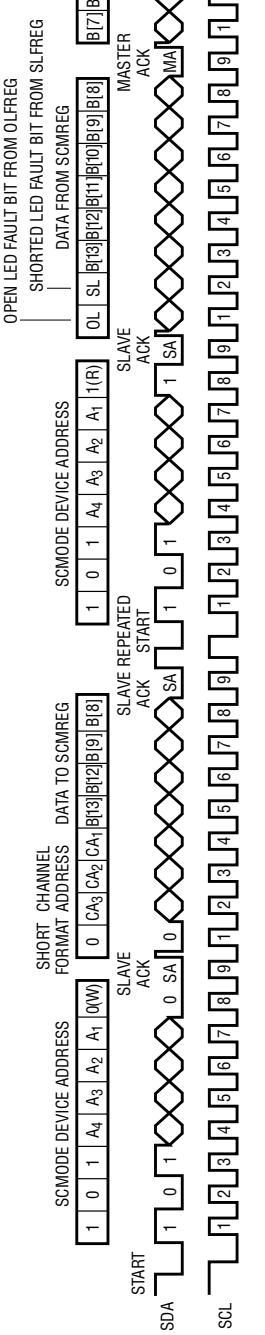


Figure 11. LT3965/LT3965-1 I²C Serial Port SCMODE Write Short Format Followed by SCMODE Read

APPLICATIONS INFORMATION

If the LEDREF pin is set to a voltage other than 0V, the channel shorted LED threshold V_{STH} can be programmed to one of these four values: 1V, 1V + V_{LEDREF}, 1V + 2 • V_{LEDREF} and 1V + 3 • V_{LEDREF}. The POR default V_{STH} of the LT3965/LT3965-1 is 1V. By using this feature, each channel is able to detect 1, 2, 3, or 4 shorted LEDs.

This feature can be turned off by grounding the LEDREF pin. When the LEDREF pin is set to 0V, the V_{STH} will be set to 1V, no matter how the V_{STH}[1:0] bits are programmed.

The SCMODE read command (see Figure 10 and Figure 11) is used to read back the addressed channel SCMREG register bits and to get the channel LED fault conditions. The SCMODE read command is three bytes long. The first byte is the SCMODE device read address. The second byte comprises (from MSB to LSB) one addressed channel bit from the OLFREG register, one addressed channel bit from the SLFREG register, and 6 bits (V_{OTH}[1:0], V_{STH}[1:0] and MC[1:0]) from the addressed SCMREG register. The third byte is the dimming value DV[7:0] from the addressed SCMREG register.

Unlike the SCMODE write command, the SCMODE read command does not contain the channel address. Actually the channel address received from the last SCMODE write command is stored and will be used as the channel address for incoming SCMODE read operations. In other words, a SCMODE read command always reads the channel SCMREG register addressed by the last SCMODE write command. If no SCMODE write command has ever been received, the default channel address 000 (CH1) is used.

The LT3965/LT3965-1 SCMODE device address is $101A_4A_3A_2A_1$ followed by an eighth bit which is a data direction bit (R/W)— a 0 indicates a write transmission (the master writes to the addressed LT3965), a 1 indicates a read transmission (the master reads from the addressed LT3965/LT3965-1). $A_4A_3A_2A_1$ is an input logic value from the programmable address select pins ADDR4, ADDR3, ADDR2 and ADDR1.

3) Broadcast Mode (BCMODE) Command

The BCMODE write command (see Figure 12) is used to synchronize the dimming cycles among the multiple LT3965/LT3965-1 slaves on the I^2C bus. The LT3965/LT3965-1 slaves must be operating with a common external clock in order to be synchronized. The BCMODE write command is only one byte long: 00011000. The command does not modify any register bits. It only resets each channel counter to synchronize the dimming cycles.

The BCMODE read command (see Figure 13) is used to inquire about which LT3965/LT3965-1 slave on the bus is sending the alert (see LT3965/LT3965-1 LT3965/LT3965-1 Alert Response Protocol Using Alert Response Address (ARA) section for detail). This command is two bytes long. The first byte is the broadcast read address 00011001. The second byte $010A_4A_3A_2A_11$ is sent by the alerting slave to indicate its ACMODE device read address to the master. $A_4A_3A_2A_1$ is an input logic value from the programmable address select pins ADDR4, ADDR3, ADDR2 and ADDR1.

If the BCMODE read command is issued when no LT3965/LT3965-1 slave on the bus is sending alert, the master receives no acknowledgement.

LT3965/LT3965-1 ALERT RESPONSE PROTOCOL USING ALERT RESPONSE ADDRESS (ARA)

In a system where several slaves share a common interrupt line, the master can use the alert response address (ARA) to determine which device initiated the interrupt. The master initiates the ARA procedure with a START condition and the special 7-bit ARA bus address (0001100) followed by the read bit (R) = 1. If the LT3965/LT3965-1 is asserting the $\overline{ALERT}$ pin, it acknowledges and responds by sending its 7-bit bus address ($010A_4A_3A_2A_1$) and a 1. While it is sending its address, it monitors the SDA pin to see if another device is sending an address at the same time using standard I^2C bus arbitration. If the LT3965/LT3965-1 is sending a 1 and reads a 0 on the SDA pin on

APPLICATIONS INFORMATION

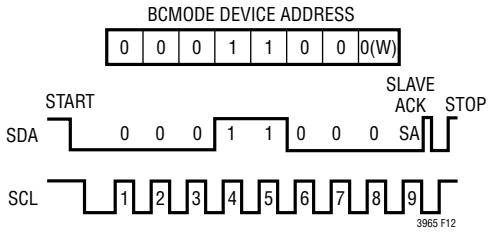


Figure 12. LT3965/LT3965-1 I²C Serial Port BCMODE Write Protocol

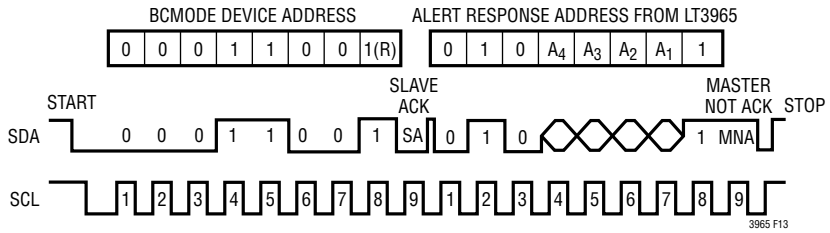


Figure 13. LT3965/LT3965-1 I²C Serial Port BCMODE Read Protocol

the rising edge of SCL, it assumes another device with a lower address is sending and the LT3965/LT3965-1 immediately aborts its transfer and waits for the next ARA cycle to try again. If transfer is successfully completed, the LT3965/LT3965-1 will deassert its $\overline{\text{ALERT}}$ pin and will not respond to further ARA requests until a new alert event occurs. Please note that the successfully completed ARA cycle deasserts the $\overline{\text{ALERT}}$ pin only. It does not clear the fault status bit set in the OLFREG/SLFREG register.

LED/OVERHEAT FAULT DETECTION AND REPORTING

The LT3965/LT3965-1 detects and reports open LED, shorted LED and overheat fault conditions via the $\overline{\text{ALERT}}$ pin and I²C serial interface. (See the following sections for detail.)

OPEN LED FAULT DETECTION AND ALERT ASSERTION

An open LED fault will be triggered when the voltage between the channel DRN pin and the channel SRC pin exceeds 22V (nominal) or when the voltage between the channel DRN pin and the channel SRC pin exceeds the programmed open LED threshold but less than 22V (nominal) for more than 15µs (nominal). Once an open LED fault is triggered in a channel, the fault status bit matching the channel will be set in the OLFREG status register, which will cause the $\overline{\text{ALERT}}$ pin to be asserted (pulled down) and the channel switch to be turned on for the switch protection and to maintain continuity of the string for good LEDs. The switch can be turned off and PWM dimming reestablished by updating its registers with the serial interface.

SHORTED LED FAULT DETECTION AND ALERT ASSERTION

A shorted LED fault will be triggered when the voltage between the channel DRN pin and the channel SRC pin falls below the programmed shorted LED threshold for more than 15µs (nominal). Once a shorted LED fault is triggered in a channel, the fault status bit matching the channel will be set in the SLFREG status register, which will cause the $\overline{\text{ALERT}}$ pin to be asserted (pulled down). However, unlike the open LED fault, the channel switch will continue with the programmed PWM dimming.

LED FAULT STATUS BIT CLEARANCE

The fault status bit set in the OLFREG/SLFREG register by an open/shorted LED fault can only be cleared by an ACMODE write command or a SCMODE write command

APPLICATIONS INFORMATION

accessing the channel. If the open/shorted LED fault no longer exists when the write command is updating the command register at the I^2C STOP condition, the fault status bit matching the channel will be cleared and the $\overline{ALERT}$ pin will be deasserted. Otherwise, the fault status bit will remain set, and the $\overline{ALERT}$ pin will remain asserted or be asserted again if previously deasserted.

OVERHEAT FAULT DETECTION AND ALERT ASSERTION

An overheat fault will be triggered when the IC temperature exceeds 170°C. Once an overheat fault is triggered, all status bits in both the OLFREG register and the SLFREG register will be set, which will cause the $\overline{ALERT}$ pin to be asserted (pulled down) and all eight channel switches to be turned on (LEDs to be turned off) for cooling down the system.

OVERHEAT STATUS BITS CLEARANCE

The fault status bits set in the OLFREG register and the SLFREG register by an overheat fault can only be cleared by an ACMODE write command with all 1s in its data byte. If the IC temperature is below 160°C when the ACMODE write command is updating the ACMREG register at the I^2C STOP condition, the fault status bits will be cleared and the $\overline{ALERT}$ pin will be deasserted. Otherwise, the fault status bits will remain set, and the $\overline{ALERT}$ pin will remain asserted or be asserted again if previously deasserted.

ALERT DEASSERTION

The LT3965LT3965-1 deasserts the $\overline{ALERT}$ pin in either of the following two situations:

1) The LT3965/LT3965-1 has successfully completed the ARA procedure initiated by the master. Please note that the successfully completed ARA procedure does not clear fault status bits. It only deasserts the $\overline{ALERT}$ pin.
2) The LT3965/LT3965-1 has received an ACMODE or SCMODE write command which cleared the fault status bits, resulting in the $\overline{ALERT}$ pin deassertion.

PRINTED CIRCUIT BOARD LAYOUT

When laying out the printed circuit board, the following checklist should be followed to ensure proper operation of the LT3965/LT3965-1:

1. Connect the exposed pad of the package (Pin 29) directly to a large ground plane to minimize thermal and electrical impedance.
2. Keep the LED connection traces as short as possible.
3. Place power supply bypass capacitors as close as possible to the supply pins.
4. Place the RTCLK resistor as close as possible to the IC if a resistor is used to set LED dimming frequency.

Long Wires or Cables Between LT3965/LT3965-1 and LEDs

The best practice is to place the LT3965/LT3965-1 and the LEDs it controls on the same PCB and to keep LED connection traces as short as possible. Long wires (>>10cm) between the LT3965/LT3965-1 and the LEDs introduce parasitic inductance that leads to an underdamped RLC response (ringing) in the switching voltage when channel is switching on and off. A meter of 30-gage wire can introduce about 1µH of parasitic inductance. The ringing can trigger open LED protection due to false open LED detection, and cause the channel to bypass good LEDs. In extreme cases, the ringing may exceed absolute maximum ratings and damage the part. The parasitic inductance also generates a step voltage waveform (relative to GND) at the switches at the frequency of the switching regulator. The magnitude of this step waveform depends upon the current ripple in the source and the parasitic inductance. The fast edges of the step waveform can cause unintended toggling of the LT3965/LT3965-1 switches.

RC snubber circuits (shown in Figure 14) can suppress the ringing and allow use of wires up to 1 meter with no false fault detection. The snubber should be placed close to the IC. Please note that an 8-LED string requires 9 snubbers: one snubber across each of the 8 switches and a snubber across all 8 switches (R9, C9). The 9th snubber (R9, C9) softens the stepped waveform edges.

APPLICATIONS INFORMATION

With the snubbers, the LT3965/LT3965-1 can control the LEDs through a 1 meter ribbon cable (9 wires total) passing 0.5A with no false faults detected. The snubber value shown here is good for most applications.

Schottky Clamping Diode for LT3965/LT3965-1 Protection

A Schottky clamping diode (D1 shown in Figure 15) connecting the top of the LED string (LED^+ node) to the V_{IN} pin is required to guarantee that the absolute maximum rating $V_{IN} – SRC \geq –0.3V$ is met.

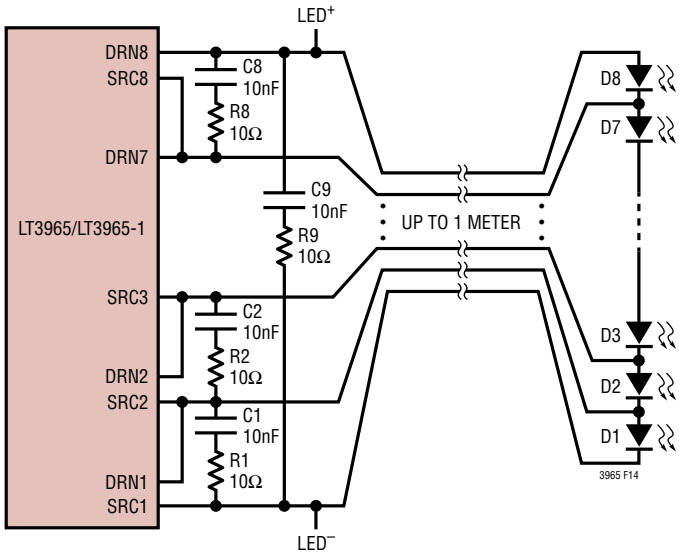


Figure 14. RC Snubbers In Long Wire Application

For the boost-buck configuration, where the voltage at the LED string bottom ($LED^–$ node) may go below 0V, a Schottky clamping diode (D2 shown in Figure 15) connecting the IC ground to the $LED^–$ node is required to keep $SRC \geq –0.3V$.

In applications with wires longer than 30cm, there is potential for an open or shorted LED to cause ringing at channel DRN-SRC beyond the absolute maximum rating of –0.3V. The LT3965/LT3965-1 can be protected by placing Schottky clamping diodes (D3 to D10 shown in Figure 15) near the IC across channel pins.

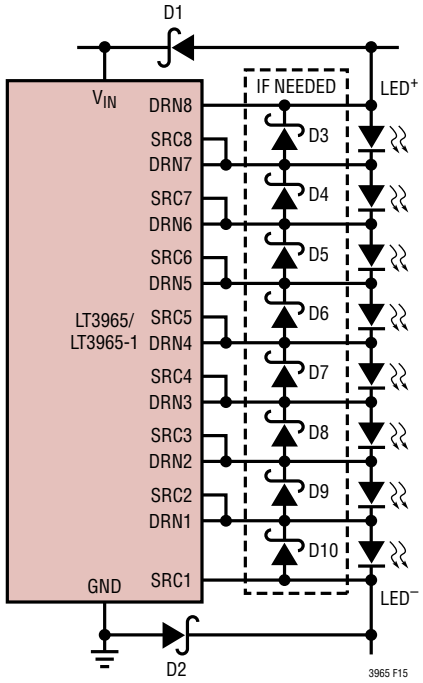
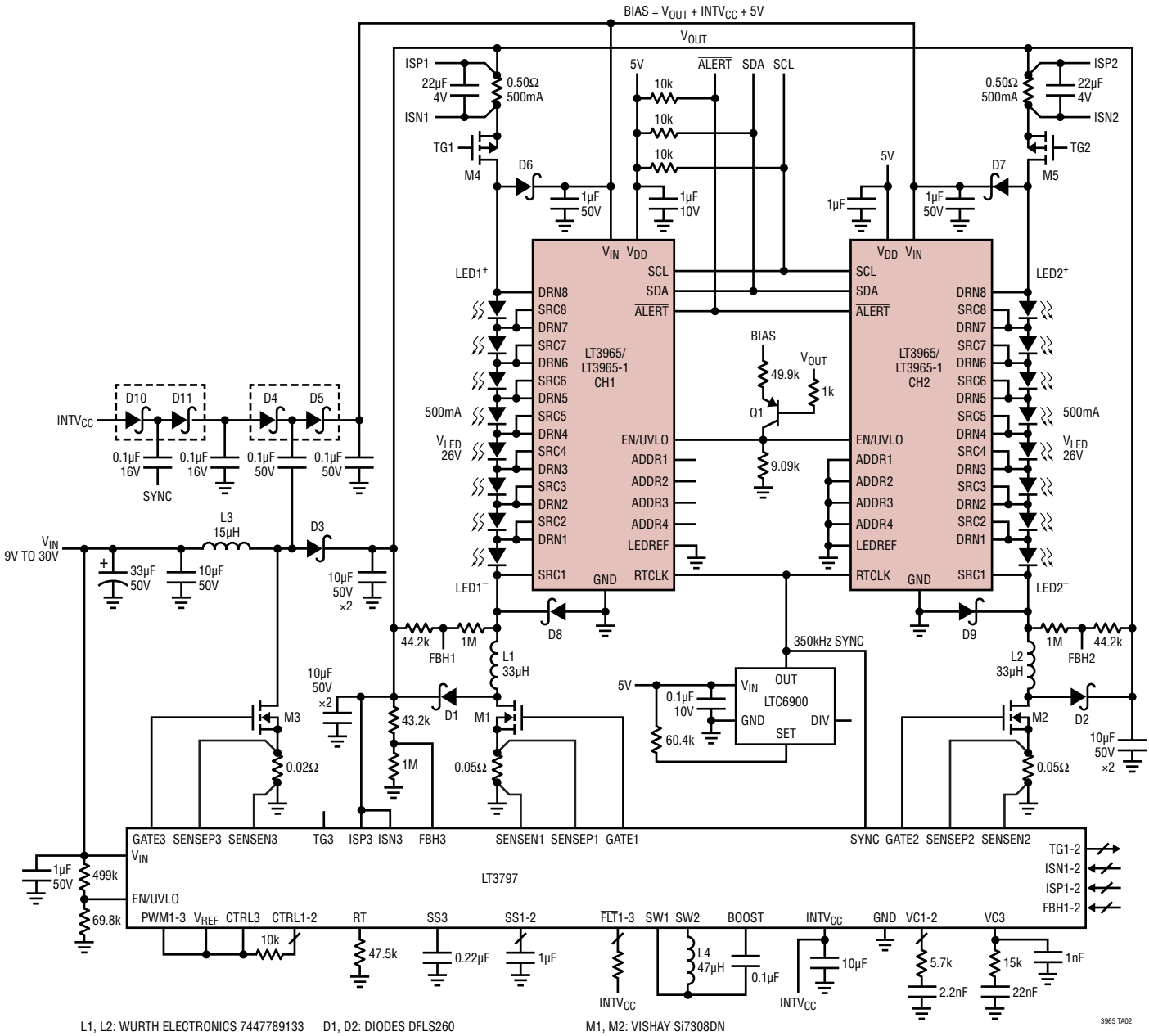


Figure 15. Clamping Diode For LT3965/LT3965-1 Protection

TYPICAL APPLICATIONS

Matrix LED Dimmer Powered by a Dual Buck Mode LED Driver with a Boost Pre-Regulator



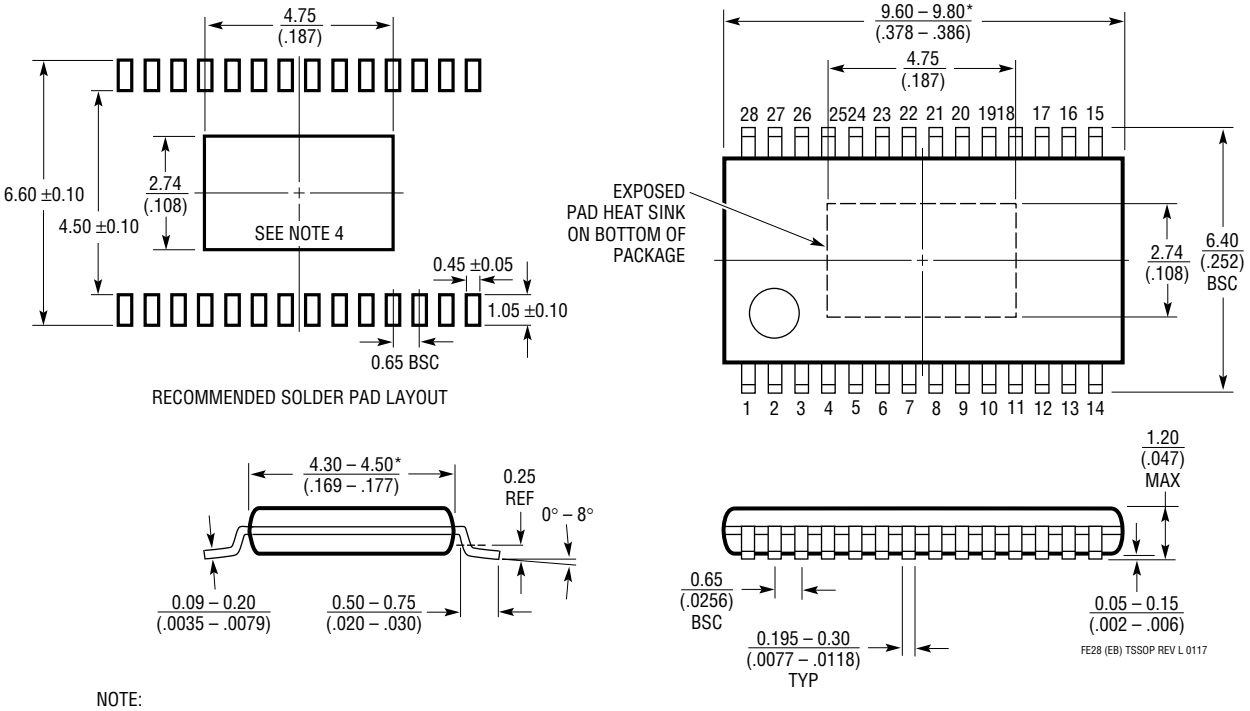
L1, L2: WURTH ELECTRONICS 7447789133
L3: WURTH ELECTRONICS 7443551151
L4: COOPER BUSSMANN SD25-470-R

D1, D2: DIODES DFLS260
D3: DIODES PDS360
D4, D5, D10, D11: CENTRAL SEMI CMSD6263S 2 IN 1 PACKAGE
D6, D7: NXP SEMI PMEG6010CEH
D8, D9: NXP SEMI PMEG4010CEH
Q1: ZETEX FMMT591

M1, M2: VISHAY Si7308DN
M3: VISHAY Si7850DP
M4, M5: VISHAY Si7309DN

PACKAGE DESCRIPTION

FE Package
28-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1663 Rev L)
Exposed Pad Variation EB



NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN MILLIMETERS (INCHES)
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT

*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	04/17	Added LT3965-1 Option	All
		Clarified Block Diagram	9
B	12/19	Added Automotive Products	2