I²C Programmable Quad Monolithic Boost LED Driver

FEATURES

- **Four Independent DC/DC Channels**
- **I²C Programmable**
- **8192:1 True Color PWM™ Dimming**
- **8-Bit Analog Dimming Pin Scaled by DAC**
- **11-Channel, 8-Bit ADC with 2 External Inputs**
- **1.6A, 60V Internal DMOS Switches**
- **Input Voltage: 3V to 60V**
- **Output Voltage and Current Monitoring to 60V**
- High Side PMOS Disconnect and PWM Switch Driver
- Adjustable Frequency: 300kHz to 4MHz with Optional Frequency Synchronization
- Thermally Enhanced 6mm × 6mm 40-Lead QFN Package
- AEC-Q100 Qualification in Progress

APPLICATIONS

- Backlighting
- Heads Up Displays

DESCRIPTION

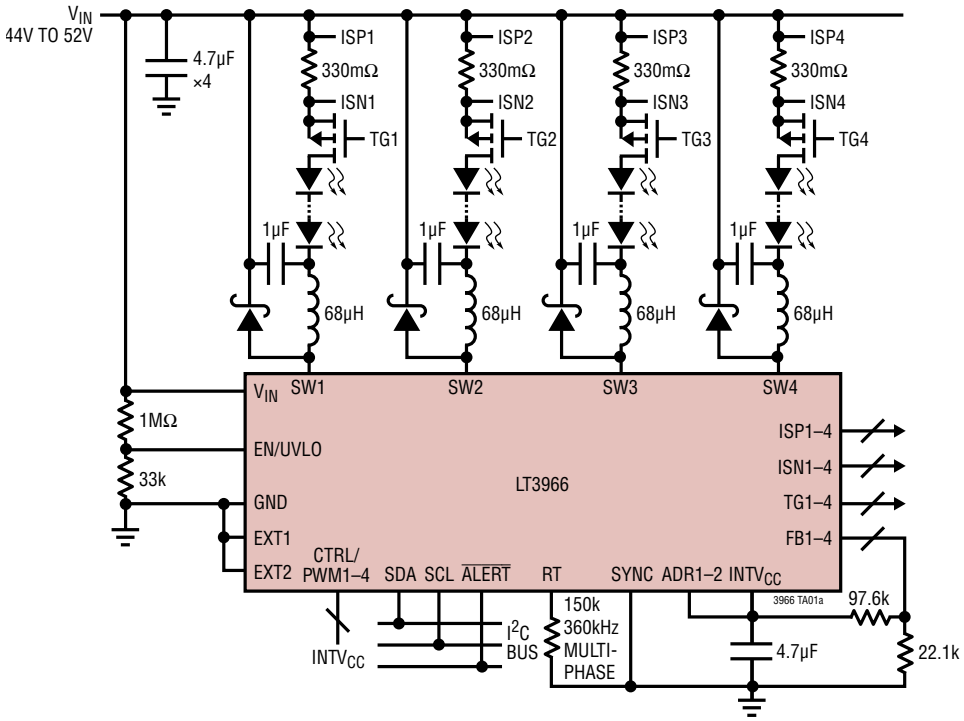
The LT®3966 is an I²C programmable monolithic boost LED driver with four independent channels. Each channel provides a 60V current mode boost converter with an internal 1.6A DMOS power switch, as well as internal and external analog and PWM dimming features. I²C programmable features include a 13-bit (8192:1) digital PWM generator, 8-bit analog dimming DAC, and flexible fault reporting and handling.

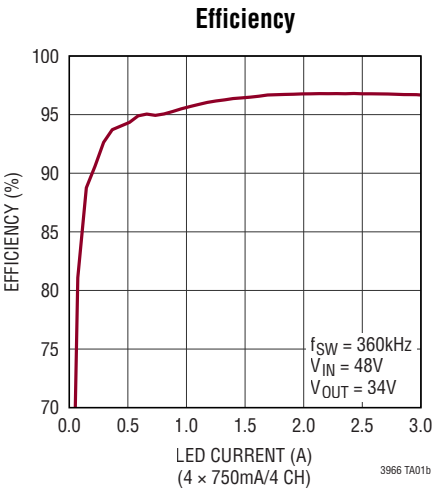
An onboard 8-bit ADC allows measurement of each channel's output voltage and output current, as well as chip input voltage and two external measurements. In addition, independent shutdown and standby control of each channel provides flexible solutions for multitopology applications.

The LT3966 is available in a thermally enhanced 6mm × 6mm 40-Lead QFN package.

TYPICAL APPLICATION

100W Buck Mode LED Driver with I²C Dimming



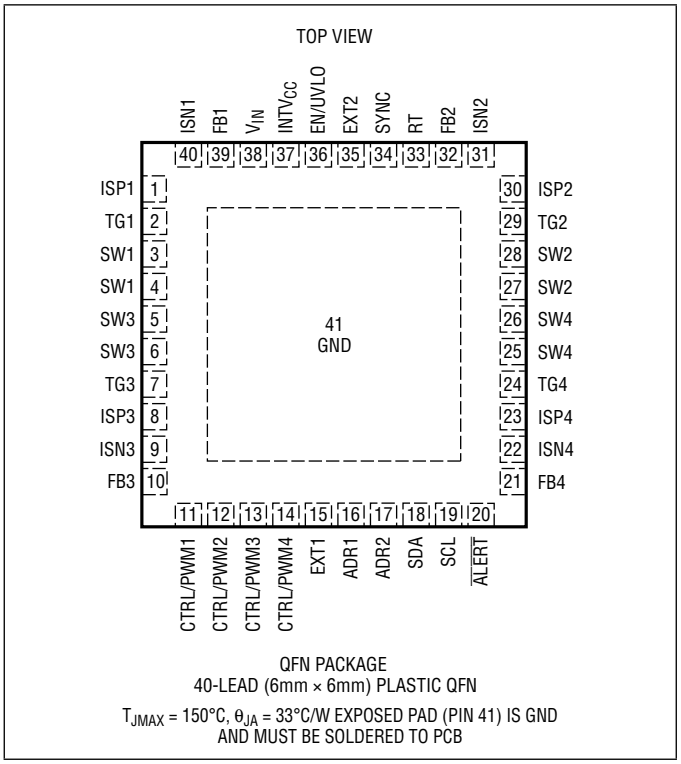


ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN}, EN/UVLO, SW1, SW2, SW3, SW4, ISP1, ISP2, ISP3, ISP4, ISN1, ISN2, ISN3, ISN4 ..... 62V
ISP–ISN (Any Channel) 2V
TG1–4 ..... (Note 2)
$INTV_{CC}$ ..... (Note 3)
FB1–4, EXT1–2, CTRL/PWM1–4, ADR1–2, $\overline{ALERT}$, SDA, SCL, SYNC 5.5V
RT 2V
Operating Junction Temperature Range (Notes 4, 5)
LT3966E ..... –40°C to 125°C
LT3966J ..... –40°C to 150°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



QFN PACKAGE
40-LEAD (6mm × 6mm) PLASTIC QFN

T_{JMAX} = 150°C, θ_{JA} = 33°C/W EXPOSED PAD (PIN 41) IS GND AND MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3966EUJ#PBF	LT3966EUJ#TRPBF	LT3966UJ	40-Lead (6mm × 6mm) Plastic QFN	–40°C to 125°C
LT3966JUJ#PBF	LT3966JUJ#TRPBF	LT3966UJ	40-Lead (6mm × 6mm) Plastic QFN	–40°C to 150°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications that apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN} Operating Range		●	3		60	V
V_{IN} Quiescent Current	CTRL/PWM = 0V, EN/UVLO = 1.3V			2.7	3.3	mA
V_{IN} Shutdown Current	EN/UVLO = 0V EN/UVLO = 1.15V, CTRL/PWM = 0V			0 190	1 230	µA µA
EN/UVLO Shutdown Threshold Falling		●	1.20	1.23	1.26	V
EN/UVLO Rising Hysteresis	EN/UVLO Rising			15		mV
EN/UVLO Input Low Voltage	I_{VIN} < 1µA				0.4	V

ELECTRICAL CHARACTERISTICS

The ● denotes specifications that apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
EN/UVLO Bias Current Low	EN/UVLO = 1.15V			2		µA
EN/UVLO Bias Current High	EN/UVLO = 1.3V			10	100	nA
LDO Regulator						
$INTV_{CC}$ Regulation Voltage	I_{INTVCC} = –1mA, Not Switching	●	2.9	3	3.1	V
$INTV_{CC}$ Line Regulation	3V ≤ V_{IN} ≤ 60V			0.03		%/V
$INTV_{CC}$ Load Regulation	–20mA ≤ I_{INTVCC} ≤ 0mA, Not Switching			0.04		%/mA
$INTV_{CC}$ Undervoltage Lockout	$INTV_{CC}$ Falling	●	2.6	2.7	2.8	V
$INTV_{CC}$ Undervoltage Lockout Hysteresis	$INTV_{CC}$ Rising			75		mV
$INTV_{CC}$ Current Limit	V_{IN} = 12V, $INTV_{CC}$ = 2.8V			36		mA
$INTV_{CC}$ Dropout Voltage	V_{IN} = 3V, I_{INTVCC} = –15mA			320		mV
Analog-to-Digital Converter						
Converter Resolution				8		Bits
Converter Full-Scale Voltage			1.266	1.275	1.284	V
Converter LSB Size			4.95	5	5.05	mV
Conversion Time (t_{CONV})	R_t = 100kΩ, MPHASE = 0, AUTO = 0			20		µs
EXT1, EXT2 Input Impedance	V_{EXT1} = V_{EXT2} = 1V		10	100		MΩ
EXT1, EXT2 Internal Voltage Clamp	I_{EXT1} = I_{EXT2} = 100µA	●	1.4	1.7	1.9	V
EXT1, EXT2 Internal Voltage Clamp Impedance	V_{EXT1} = V_{EXT2} = 2V to 5.5V			2.2		kΩ
Channel 1–4 LED Current Sense Amplifiers						
ISP Common Mode Voltage Range		●	3		55	V
Full-Scale Current Sense Threshold (V_{ISP}–V_{ISN})	ISP = 55V, CTRL/PWM =1.5V, ADIM[7:0] = 0xFF ISP = 3V, CTRL/PWM = 1.5V, ADIM[7:0] = 0xFF	● ●	242 242	250 250	255 255	mV mV
Externally Adjusted Half-Scale Threshold (V_{ISP}–V_{ISN})	ISP = 55V, CTRL/PWM = 0.7V, ADIM[7:0] = 0xFF ISP = 3V, CTRL/PWM = 0.7V, ADIM[7:0] = 0xFF	● ●	122 122	125 125	128 128	mV mV
Externally Adjusted 1/10th Scale Threshold (V_{ISP}–V_{ISN})	ISP = 55V, CTRL/PWM = 0.3V, ADIM[7:0] = 0xFF ISP = 3V, CTRL/PWM = 0.3V, ADIM[7:0] = 0xFF	● ●	20 20	25 25	31 31	mV mV
Internally Adjusted Half-Scale Threshold (V_{ISP}–V_{ISN})	ISP = 55V, CTRL/PWM = 1.5V, ADIM[7:0] = 0x7F ISP = 3V, CTRL/PWM = 1.5V, ADIM[7:0] = 0x7F	● ●	121 121	125 125	129 129	mV mV
Internally Adjusted 1/10th Scale Threshold (V_{ISP}–V_{ISN})	ISP = 55V, CTRL/PWM = 1.5V, ADIM[7:0] = 0x19 ISP = 3V, CTRL/PWM = 1.5V, ADIM[7:0] = 0x19	● ●	20 20	25 25	31 31	mV mV
Overcurrent Protection Threshold (V_{ISP}–V_{ISN})	ISP = 60V			370		mV
C/10 Threshold	ISP = 60V		14	22	30	mV
ISP/ISN Input Bias Current (Combined)	CTRL/PWM = 3V (Active), ISP = ISN = 55V CTRL/PWM = 0V (Standby), ISP = ISN = 55V			440 13	 17	µA µA
PWM Threshold	CTRL/PWM Falling	●	90	103	115	mV

ELECTRICAL CHARACTERISTICS

The ● denotes specifications that apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
ISP Voltage Regulation Threshold				62		V
Channel 1–4 Voltage Feedback Amplifiers						
FB Regulation Threshold (V_{FB})	CTRL/PWM = 2V	 ●	1.188 1.170	1.200 1.200	1.208 1.218	V V
FB Overvoltage Threshold			V_{FB} + 50mV	V_{FB} + 60mV	V_{FB} + 70mV	V
FB Open LED Threshold			V_{FB} – 40mV	V_{FB} – 50mV	V_{FB} – 60mV	V
FB Shorted LED Threshold		●	280	300	320	mV
FB Input Bias Current	Current Out of Pin, FB = 1V			10	100	nA
FB Line Regulation	3.3V ≤ V_{IN} ≤ 60V			0.0004		%/V
Oscillator						
RT Pin Voltage				1.0		V
Switching Frequency in Single-Phase Mode	R_T = 261kΩ R_T = 100kΩ R_T = 47.5kΩ	● ● ●	370 0.93 1.85	400 1.00 2.00	430 1.07 2.15	kHz MHz MHz
Switching Frequency in Multiphase Mode	R_T = 174kΩ R_T = 47.5kΩ R_T = 21kΩ	● ● ●	279 0.93 1.85	300 1.00 2.00	321 1.07 2.15	kHz MHz MHz
Minimum Off Time			30	50	65	ns
Minimum On Time			35	60	75	ns
SYNC Input High (SYNC In Mode)	SYNCOUT = 0		1.5			V
SYNC Input Low (SYNC In Mode)	SYNCOUT = 0				0.4	V
SYNC Input Duty Cycle			10		90	%
SYNC Resistance to GND (SYNC In Mode)	SYNCOUT = 0			95		kΩ
SYNC Output Mode Duty Cycle	SYNCOUT = 1		45	55	65	%
SYNC Output Voltage High (SYNC Out Mode)	SYNCOUT = 1, Load = 3kΩ	●	2.4			V
SYNC Output Voltage Low (SYNC Out Mode)	SYNCOUT = 1, Load = 3kΩ	●			0.4	V
Channel 1–4 Power Switch						
SW On-Resistance	I_{SW} = 200mA			200		mΩ
SW Current Limit		●	1.6	2	2.4	A
SW Leakage Current	V_{SW} = 62V				3	µA
External PMOS Gate Driver						
TG ON Voltage (V_{ISP}–V_{TG})	ISP = 24V		7.4	8.2	9	V
TG OFF Voltage (V_{ISP}–V_{TG})	ISP = 24V			0	0.3	V
TG Turn-On Time	C_{LOAD} = 470pF, ISP = 24V			50		ns
TG Turn-Off Time	C_{LOAD} = 470pF, ISP = 24V			60		ns
I^2C Port						
I^2C Address	Programmed by ADR2, ADR1 Pins			101XXXX[R/$\overline{W}$]		
ADR1, ADR2 Input High Voltage		●	0.9 • V_{INTVCC}			V
ADR1, ADR2 Input Low Voltage		●			0.1 • V_{INTVCC}	V
ADR1, ADR2 Pull-Down Current in HIGH State	V_{ADR1}, V_{ADR2} = 3V, Current Into Pin	●	9	13	17	µA
ADR1, ADR2 Pull-Up Current in LOW State	V_{ADR1}, V_{ADR2} = 0V, Current Out of Pin	●	9	13	17	µA
SDA, SCL Input High Voltage		●	1.5			V
SDA ,SCL Input Low Voltage		●			0.4	V

ELECTRICAL CHARACTERISTICS

The ● denotes specifications that apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SDA, SCL Input Low Leakage	Current Out of Pin, SDA = SCL = 0V				50	nA
SDA, SCL Input High Leakage	Current Into Pin, SDA = SCL = 3V				50	nA
SDA Output Low Voltage	I_{SDA} = 3mA				0.4	V
$\overline{ALERT}$ Output Low Voltage	$I_{\overline{ALERT}}$ = 3mA				0.4	V
I^2C Clock Operating Frequency					400	kHz
Bus Free Time Between Stop and Start Condition (t_{BUF})			1.3			µs
Hold Time After Repeated Start Condition (t_{HD_SDA})			0.6			µs
Repeated Start Condition Set-Up Time (t_{SU_STA})			0.6			µs
Stop Condition Set-Up Time (t_{SU_STO})			0.6			µs
Data Hold Time Output ($t_{HD\_DAT(O)}$)			0		900	ns
Data Hold Time Input ($t_{HD\_DAT(I)}$)			0			ns
Data Set-Up Time (t_{SU_DAT})			100			ns
SCL Clock Low Period (t_{LOW})			1.3			µs
SCL Clock High Period (t_{HIGH})			0.6			µs
Clock/Data Fall Time	C_B = Capacitance of One Bus Line (pF)		20 + 0.1C_B		300	ns
Clock/Data Rise Time	C_B = Capacitance of One Bus Line (pF)		20 + 0.1C_B		300	ns
Input Spike Suppression Pulse Width (t_{SP})					50	ns
Watchdog Timeout Period	WDTEN = 1		75	100	125	ms

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

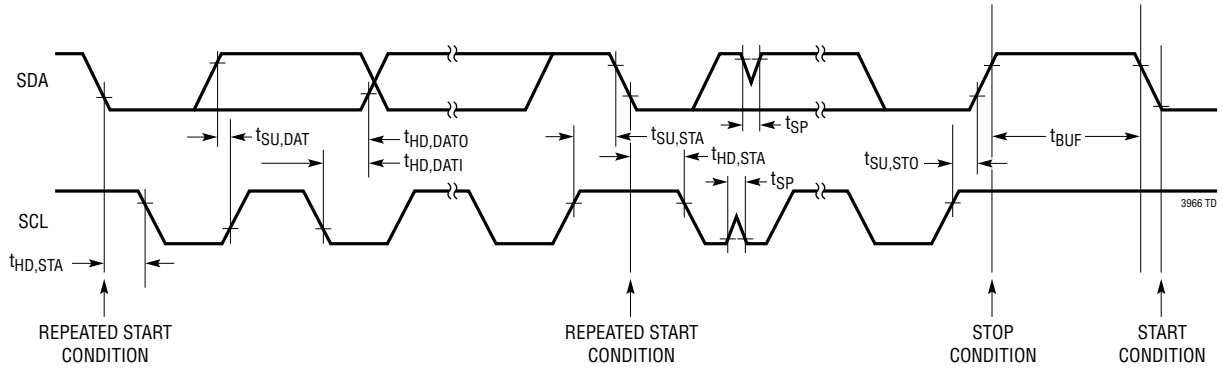
Note 2: Do not apply a positive or negative voltage source to TG pins, otherwise permanent damage may occur.

Note 3: Do not apply a positive or negative voltage source to $INTV_{CC}$ pin, otherwise permanent damage may occur. I_{INTVCC} = 2mA is the maximum external load that can be applied.

Note 4: The LT3966E is guaranteed to meet performance specifications from the 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT3966J is guaranteed to meet performance specifications over the full –40°C to 150°C operating junction temperature range. High junction temperatures degrade operating lifetimes. Operating lifetime is derated at junction temperatures greater than 125°C.

Note 5: The LT3966 includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed the maximum operating junction temperature when overtemperature is active. Continuous operating above the specified maximum operating junction temperature may impair device reliability.

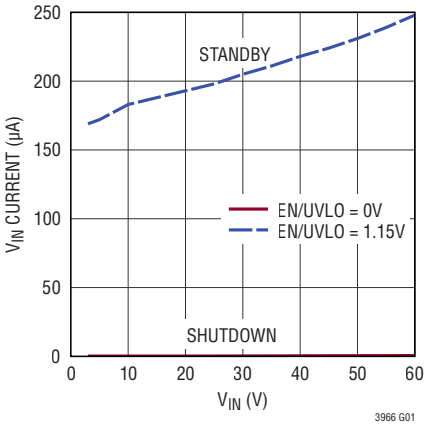
Note 6: Guaranteed by a combination of design, testing, and characterization over the operating temperature range, and automated testing at ambient temperature.



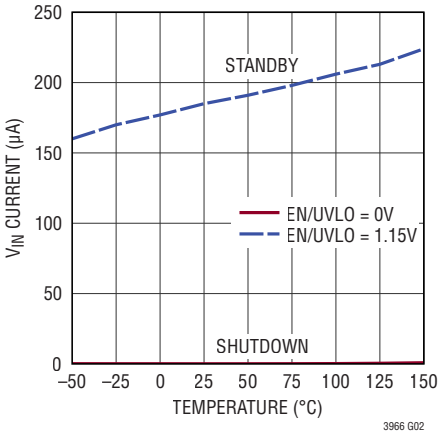
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

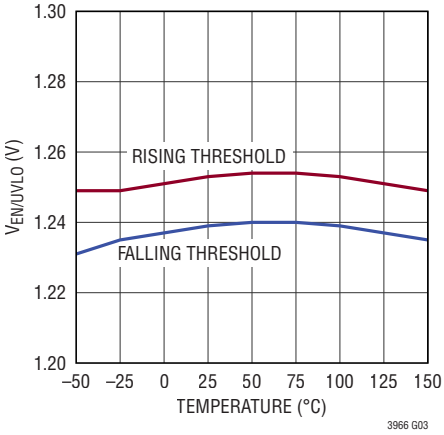
Shutdown and Standby Current vs Input Voltage



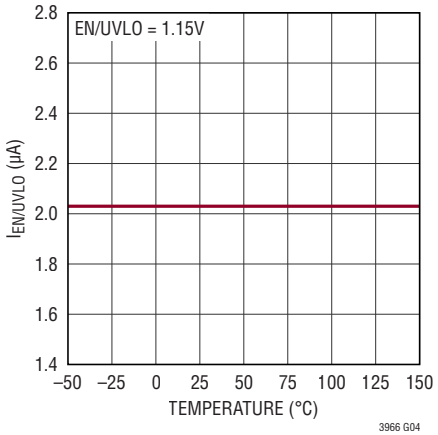
Shutdown and Standby Current vs Temperature



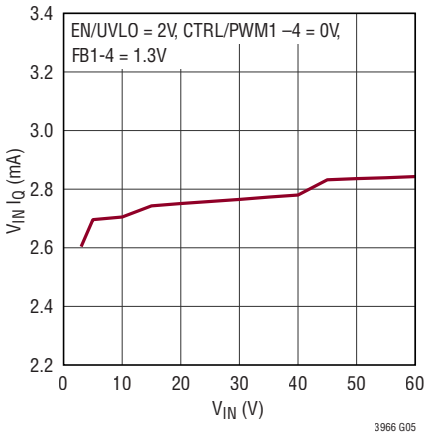
EN/UVLO Thresholds vs Temperature



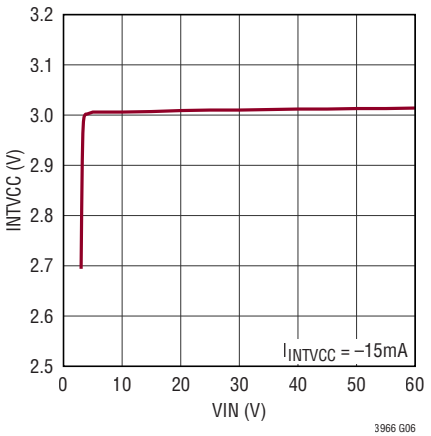
EN/UVLO Hysteresis Current vs Temperature



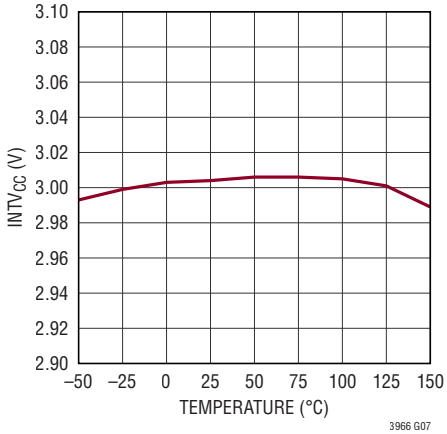
Quiescent Current vs Input Voltage



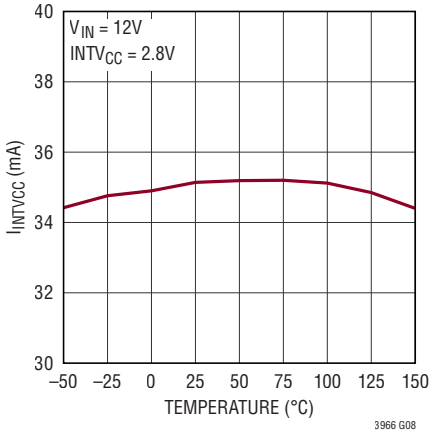
$INTV_{CC}$ Voltage vs Input Voltage



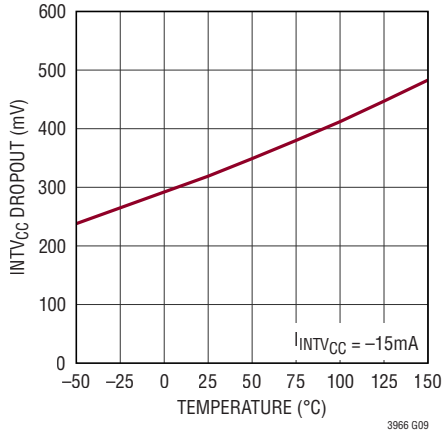
$INTV_{CC}$ Voltage vs Temperature



$INTV_{CC}$ Current Limit vs Temperature



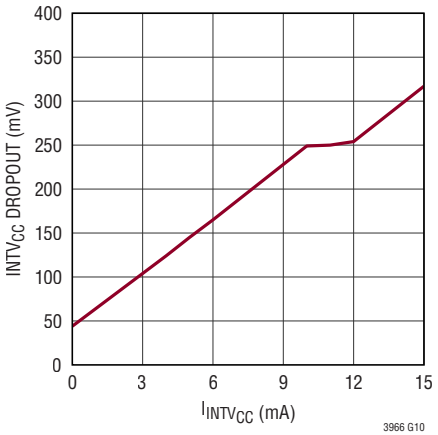
$INTV_{CC}$ Dropout vs Temperature



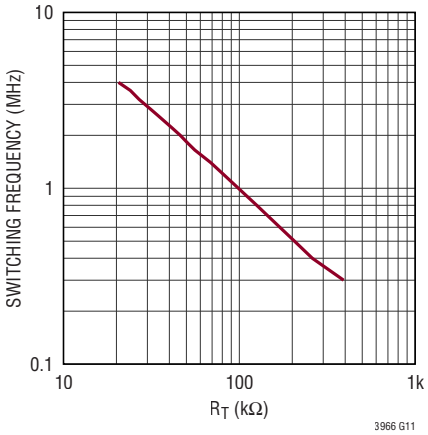
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

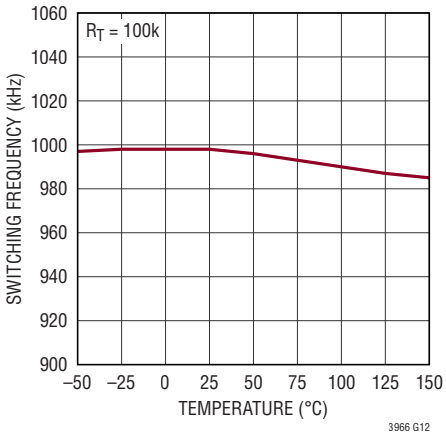
$INTV_{CC}$ Dropout vs Temperature Load



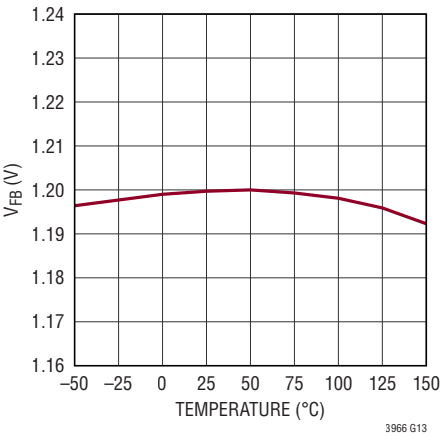
Switching Frequency vs R_T



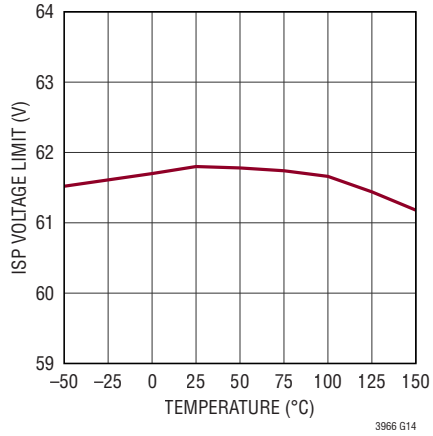
Switching Frequency vs Temperature



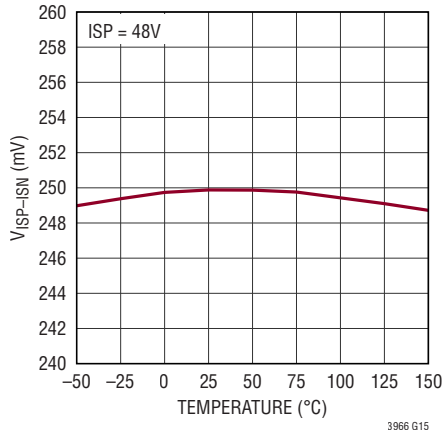
V_{FB} vs Temperature



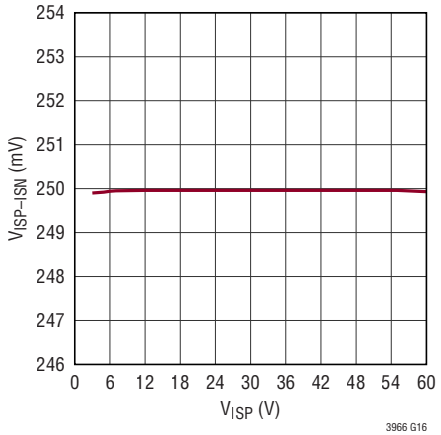
ISP Voltage Limit vs Temperature



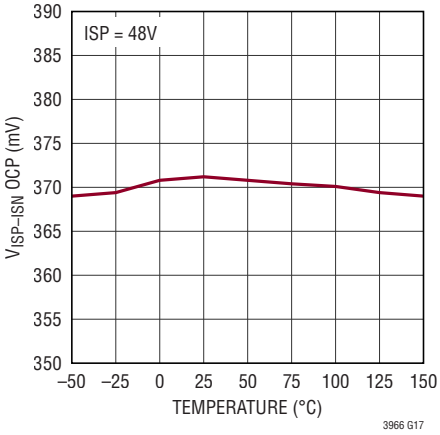
$V_{ISP–ISN}$ vs Temperature



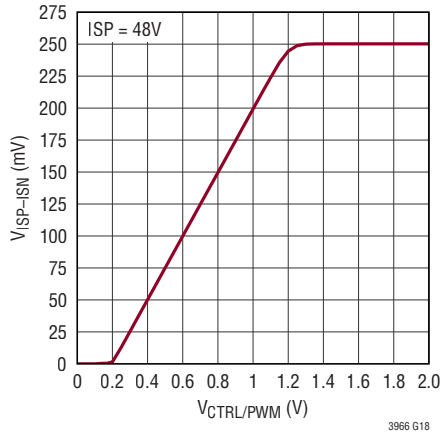
$V_{ISP–ISN}$ vs V_{ISP}



$V_{ISP–ISN}$ Threshold vs Temperature Overcurrent Protection



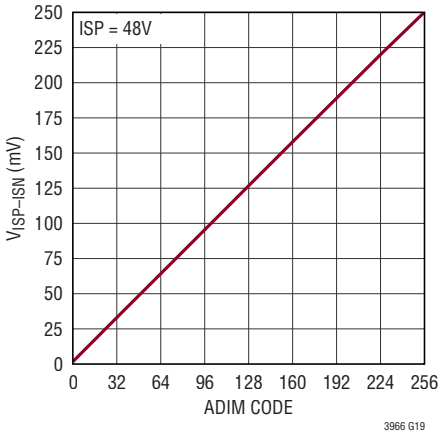
$V_{ISP–ISN}$ vs ADIM $V_{CTRL/PWM}$



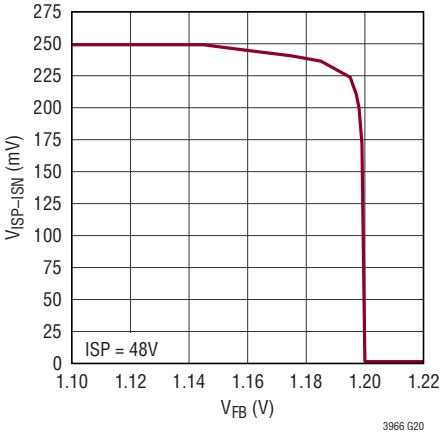
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

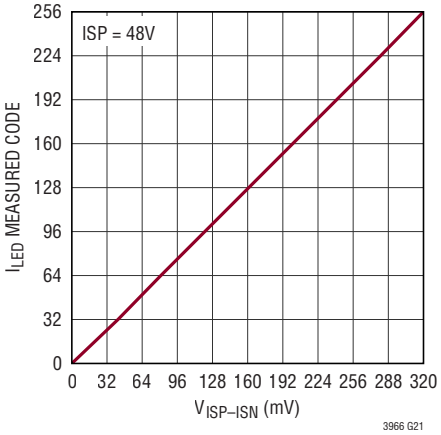
$V_{ISP–ISN}$ vs ADIM V_{FB}



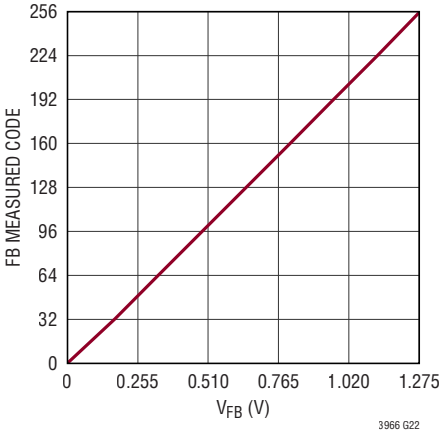
$V_{ISP–ISN}$ vs V_{FB}



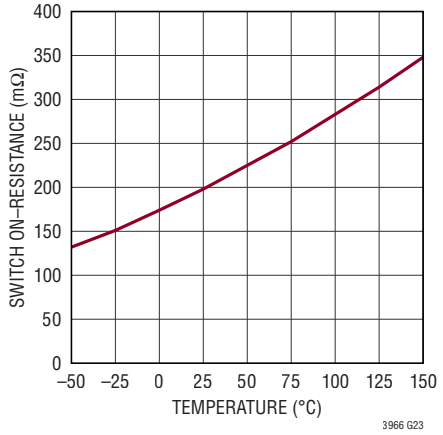
I_{LED} Measured Code vs $V_{ISP–ISN}$



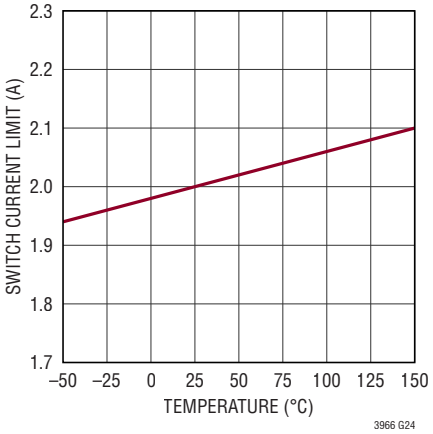
FB Measured Code vs V_{FB}



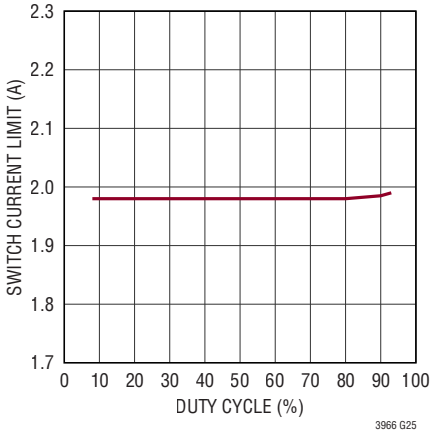
Switch On-Resistance vs Temperature



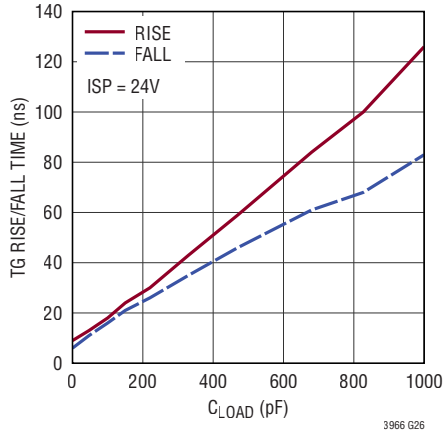
Switch Current Limit vs Temperature



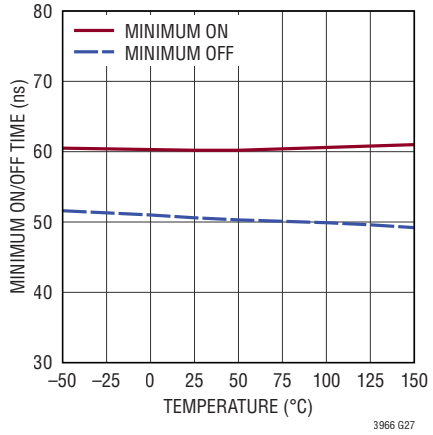
Switch Current Limit vs Duty Cycle



TG Rise/Fall Time vs C_{LOAD}



Minimum On/Off Time vs Temperature



PIN FUNCTIONS

FB1, FB2, FB3, FB4 (Pins 39, 32, 10, 21): Voltage Feedback Pin. The FB pin is used for output voltage regulation and limiting. Tie to a resistor divider from the output voltage. When FB reaches 1.2V, the switch current will reduce in order to maintain the output voltage at this level. If ISP/ISN senses less than 10% of full output current when FB reaches regulation, an OPENLED condition will be flagged for that channel. If FB is driven above 1.26V, the external PMOS will be switched off and an OVFB condition will be flagged. If FB remains below 0.3V after the internal soft start has completed, a SHORTLED condition will be flagged. See the Applications Information section for more information on faults and fault handling.

ISP1, ISP2, ISP3, ISP4 (Pins 1, 30, 8, 23): Positive Terminal of the LED Current Sense Amplifier. Also serves as the positive supply of the TG gate driver. Connect to positive side of LED current sense resistor and minimize resistance in this path.

ISN1, ISN2, ISN3, ISN4 (Pins 40, 31, 9, 22): Negative Terminal of the LED Current Sense Amplifier. Kelvin connects to negative side of LED current sense resistor.

TG1, TG2, TG3, TG4 (Pins 2, 29, 7, 24): Top Gate Driver Output. Connect to gate of external PMOS pass transistor. TG is an inverted and level-shifted version of the PWM dimming signal, and drives between V_{ISP} (OFF) and V_{ISP}–8.2V (ON) for LED PWM dimming as well as fault mode disconnect. Leave unconnected if not used.

SW1, SW2, SW3, SW4 (Pins 3–4, 27–28, 5–6, 25–26): Power DMOS Drain. Connect to switching end of the inductor. Minimize copper area to increase efficiency and reduce EMI.

CTRL/PWM1, CTRL/PWM2, CTRL/PWM3, CTRL/PWM4 (Pins 11, 12, 13, 14): Combination Analog/PWM Dimming Input. Drive from below 100mV to above 1.5V for full-scale PWM dimming. Or drive with an analog voltage from 0.2V to 1.2V for 0% to 100% analog dimming. Do not leave these pins floating, tie to $INTV_{CC}$ if unused.

EXT1, EXT2 (Pins 15, 35): External Input to ADC. The working range of the EXT input is 0V (Code 0) to 1.275V (Code 255). These pins are internally clamped to 1.7V. Tie to GND if unused.

ADR1, ADR2, (Pins 16, 17): I^2C Address Select. These pins are configured as three-state inputs (HIGH, LOW, FLOAT). See Table 1 for address selection.

$\overline{\text{ALERT}}$ (Pin 20): Chip Status Reporting Pin. Depending on channel configuration, the $\overline{\text{ALERT}}$ pin can be pulled low due to any of the following faults: FB Overvoltage, Open LED, Shorted LED, and LED Overcurrent. See the Applications Information section for more information on faults and fault handling.

SDA (Pin 18): Serial Data Line for I^2C Communications. Combination input and open-drain output.

SCL (Pin 19): Serial Clock for I^2C Communications.

SYNC (Pin 34): Oscillator Synchronization Pin. By default, this pin acts as an input for an external clock to define the switching frequency of the LT3966. By setting the SYNCOUT configuration bit, the input function is disabled and instead SYNC becomes a clock output for driving other external circuits.

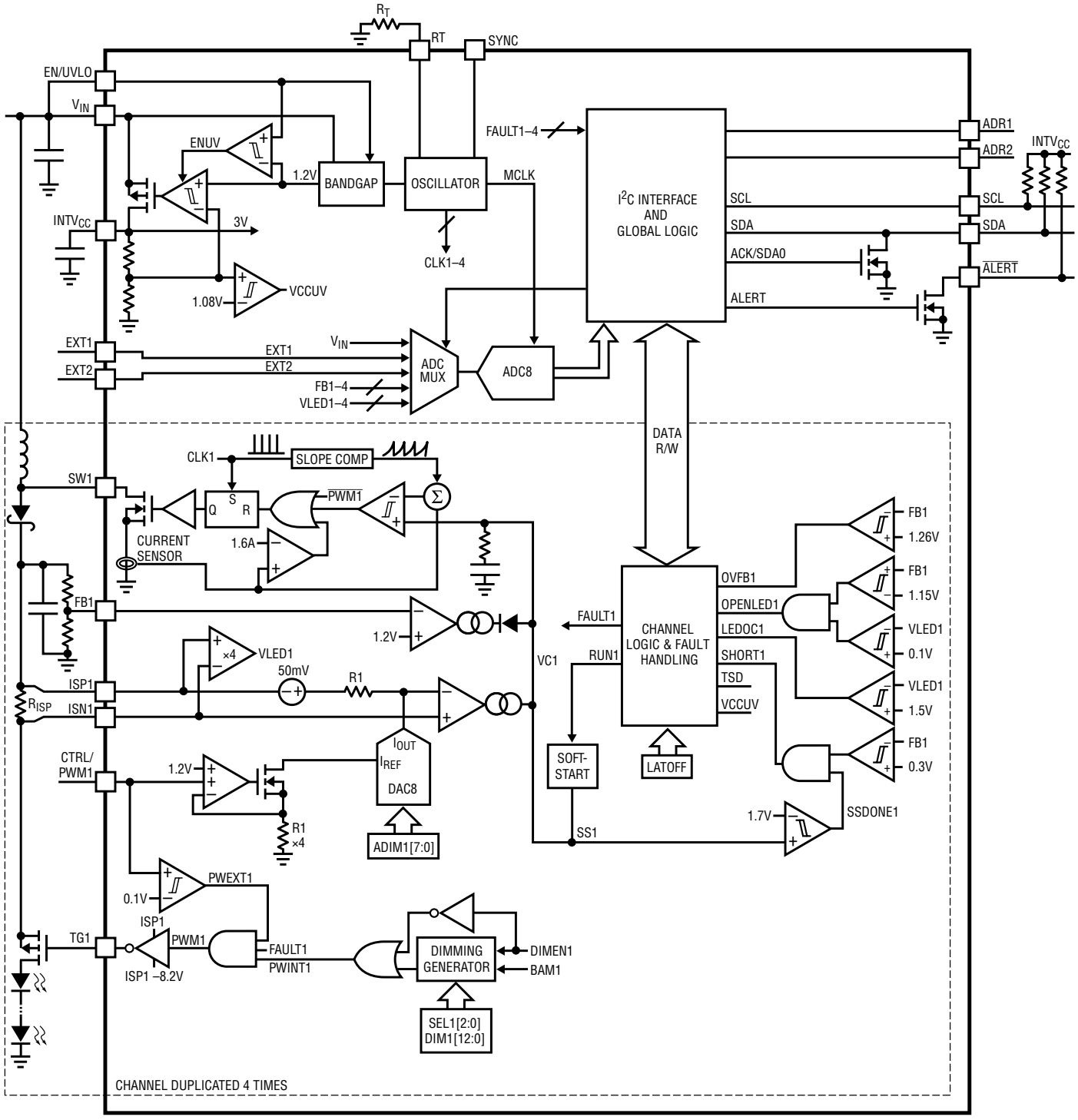
RT (Pin 33): Timing Resistor Set Pin. Set the master clock frequency using a resistor to GND. Do not leave the RT pin open.

EN/UVLO (Pin 36): Enable/Undervoltage Lockout Pin. This pin is used for general ON/OFF control and to enable the LT3966 at a specific input voltage. Drive with a logic level greater than 1.5V for simple ON/OFF control, or tie to a resistor divider of input voltage for precision shutdown threshold. This pin has a falling threshold of 1.23V, rising hysteresis of roughly 15mV, and a 2µA hysteresis current when below threshold. Tie this pin to V_{IN} if unused.

$INTV_{CC}$ (Pin 37): Internal 3V LDO Output. This pin is the LDO output and power supply for all internal circuitry. Place a 4.7µF filter capacitor to GND as close to this pin as possible. Do not drive this pin externally. Users may apply a load of up to 2mA to this pin.

V_{IN} (Pin 38): Input Voltage Supply. This pin is the power supply input to the LDO and the rest of the internal circuitry. It must be locally bypassed with a capacitor to GND as close to the pin as possible.

BLOCK DIAGRAM



OPERATION

OVERVIEW

The LT3966 is a 4-channel monolithic boost LED driver with I²C programmability and onboard ADC. The 4 independent LED driver channels each consist of a 1.6A monolithic boost converter with high side LED current sensing and high side gate driver for PWM dimming and fault protection. The analog LED current setpoint can be controlled externally and also programmed through I²C. The LED dimming can be controlled with an external PWM signal or through I²C using the internal PWM generator. Additionally, the LT3966 contains an 11-input, 8-bit ADC used to measure regulation parameters of each of the LED driver channels as well as input voltage, die temperature, and two external inputs.

LT3966 operates from input voltages of 3V to 60V. The 1.23V EN threshold allows programmable external UVLO using a resistor divider from the input voltage. All internal circuitry is powered from an onboard LDO regulator supplying 3V at the $INTV_{CC}$ pin. Although the internal circuitry operates at 3V, all I/O pins are 5V tolerant. The LDO is current limited to 36mA and should not be externally loaded, and the device provides an internal UVLO to prevent switching when $INTV_{CC}$ falls below 2.7V. Bypass and filtering of the LDO require a capacitor of at least 4.7µF from $INTV_{CC}$ to GND located close to the pins.

The boost converters are internally compensated current mode converters with a 1.6A power FET each. The boost converters can operate from 300Hz to 4MHz, and switching can be synchronized to an external clock. Through I²C, the LT3966 allows the options of multiphase switching for lower input ripple as well as clock sync output.

The LED drivers use high side current sensing with a 250mV threshold. This analog threshold is externally adjustable by using the CTRL/PWM pin, and is also internally programmable through I²C. A high side gate driver for an external PMOS transistor allows accurate PWM dimming, fast fault protection, and output disconnect.

PWM dimming can be controlled externally by toggling CTRL/PWM, or internally programmed using the LT3966 onboard PWM generator. This PWM generator offers resolution from 6-bit (64:1) to 13-bit (8192:1), as well as the choice between standard PWM modulation and optional BAM (Bit Angle Modulation) control.

The LED drivers have detection and protection from overvoltage, overcurrent, open LED, and shorted LED conditions. Fault handling is autonomous, with optional readback, fault reporting, and latchoff functions using I²C.

The device I²C address is programmable to one of eight different addresses or standalone mode using the two tri-mode ADR pins. Reliable and robust I²C communication is ensured by use of CRC error checking and an optional watchdog timer.

I²C OPERATION

I²C Transactions and Error Correction Operation

I²C communication revolves around read and write transactions. In LT3966, Packet Error Checking (PEC) is used to guarantee reliable communication between the host system and the device. This consists of a trailing byte on both the read and write transactions that offers a CRC check of all bytes since the last start. The CRC polynomial used in LT3966 is identical to that used in SMBus: $X^8 + X^2 + X^1 + 1$.

The structure of an I²C write is shown in Figure 1. Data being written to LT3966 must follow this format. The PEC code (Figure 2) should be computed by the host system using the CRC formula on the Chip Address, Sub Address, and Data Bytes. If a valid PEC is received, the LT3966 will acknowledge (ACK) on the 9th clock of the PEC transfer, and the data will be transferred to the LT3966 register. If an invalid PEC is received, the LT3966 will not ACK, and the data will be discarded.

OPERATION

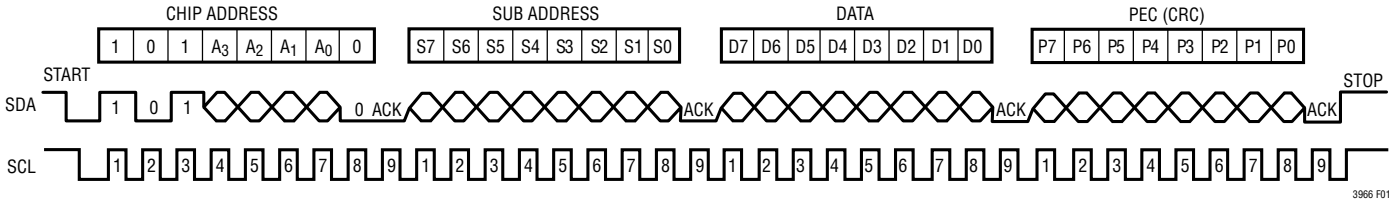


Figure 1. I²C Write Transaction with PEC

```
// Bytewise CRC-8 for LT3966 using X8 + X2 + X + 1
// Takes a running sum (or 0) as <in>, and current byte to CRC as <data>
// Returns the CRC-8 of <in> and <data> for sending or further CRC'ing
int8_t doCRC(int8_t in, int8_t data){
  int8_t crc;
  int8_t i;
  crc = in ^ data;                    // XOR the incoming bytes
  for(i = 0; i < 8; i++){             // Step through each bit
    if (crc & 0x80) {                 // If MSB is set
      crc <<= 1;                      // Shift up, then
      crc ^= 0x07;                    // XOR with the low byte of polynomial
    } else {                          // If MSB is unset
      crc <<= 1;                      // Simply shift up
    }
  }                                   // Repeat for rest of bits
  return crc;                         // Finally, send back the result
}

// Usage, where CHIPADDR, SUBADDR, and DATA are the bytes to send to LT3966
int8_t myCRC;
myCRC = doCRC(0, CHIPADDR);
myCRC = doCRC(myCRC, SUBADDR);
myCRC = doCRC(myCRC, DATA);
// myCRC now holds the completed PEC byte for sending to LT3966
```

Figure 2. Example Linduino® Code for Calculating CRC-8 PEC

Multiple transactions can take place before an I²C stop by using the repeated start signaling. Any start, including a repeated start, restarts the CRC calculation for the new transaction. The host system should calculate a new PEC code for the bytes of that transaction, and the LT3966 will evaluate the PEC code on a per transaction basis. A failure in a single transaction will cause only that transaction's data to be discarded, and other successful transaction data would be accepted.

Once all transactions are completed, the host system can execute a stop signal to transfer the written data to the output of the registers. The written data does not take effect until a stop signal is detected. In this manner, several writes can take place with their action occurring simultaneously upon execution of the stop signal.

Structure of an I²C read is shown in Figure 3. It begins with a write of Chip Address and Sub Address to set the internal pointer. No PEC is required to set the pointer. A stop/start pair, or repeated start, ends the write portion and starts the read portion of the transaction. During a read transaction, the PEC code is generated by LT3966 over the Chip Address and Data bytes, and is sent to the host after the data byte. Reading the PEC code is mandatory. The host system should evaluate the PEC for validity and respond accordingly.

OPERATION

I²C OPERATION – I²C ADDRESS SETTINGS

Normal and Standalone Mode

ADR2, ADR1 = GND, GND programs the LT3966 into a special standalone mode that does not require I²C communication. All channels are enabled, and all channel dimming generators are disabled (100% on time). The device will start up and immediately begin soft-start switching. Analog and PWM dimming in standalone mode are controlled by the channel CTRL/PWM pins. Faults are not latched, but are indicated on the $\overline{\text{ALERT}}$ line.

All other address selections start up with channels and dimming generators enabled, but with the PWM DIM register set to code 0 (0% on time). The converter channels are active, but not switching since the DIM register is set to 0. To enable light output, write a value to the channel's DIM register, or write a channel's DIMEN bit to 0 to disable dimming and provide 100% LED on time. Faults will be indicated in a channel's STATUS register, but not indicated on the $\overline{\text{ALERT}}$ pin unless the mask bit is enabled for that channel.

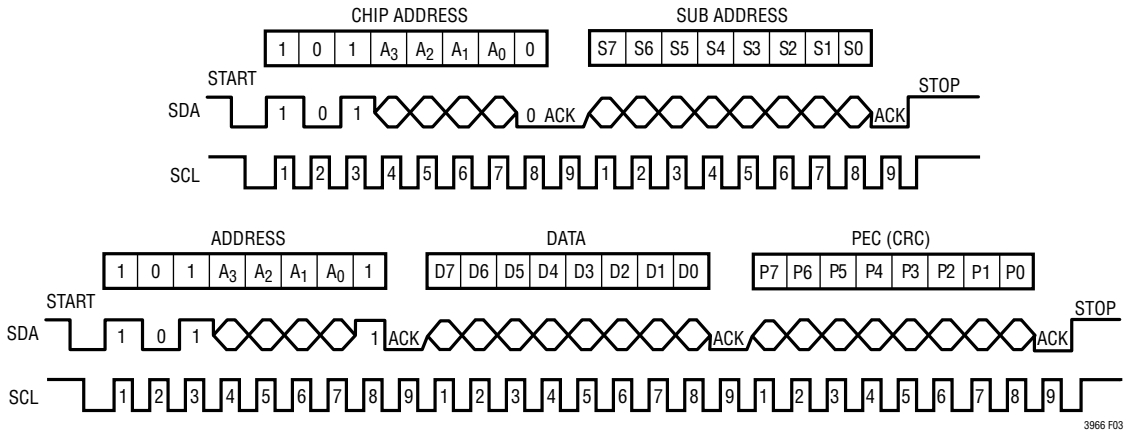


Figure 3. I²C Read Transaction with PEC

Table 1. I²C Address Settings

ADR2	ADR1	A3	A2	A1	A0	Write Address	Read Address	Mode
GND	GND	0	0	0	0	0xA0	0xA1	Standalone
GND	Float	0	0	0	1	0xA2	0xA3	Normal
GND	V_{CC}	0	0	1	1	0xA6	0xA7	Normal
Float	GND	0	1	0	0	0xA8	0xA9	Normal
Float	Float	0	1	0	1	0xAA	0xAB	Normal
Float	V_{CC}	0	1	1	1	0xAE	0xAF	Normal
V_{CC}	GND	1	1	0	0	0xB8	0xB9	Normal
V_{CC}	Float	1	1	0	1	0xBA	0xBB	Normal
V_{CC}	V_{CC}	1	1	1	1	0xBE	0xBF	Normal

APPLICATIONS INFORMATION

PROGRAMMING THE LED CURRENT

The LED current is programmed using an external current sense resistor and an adjustable sense threshold. The full-scale value of this threshold is 250mV. Choose a current sense resistor which will develop 250mV at the maximum LED current, I_{LED}, Equation 1.

$$R_{ISP} = \frac{0.250mV}{I_{LED}} \quad (1)$$

Adjustment of this current sense threshold in LT3966 is generated from the combination of the external CTRL/PWM pin voltage and the register value of an internal multiplying DAC (MDAC). The relevant circuitry from the block diagram is shown in Figure 4.

Both the CTRL/PWM pin and the ADIM register have the ability to adjust the current sense threshold, and they can be used independently or in combination. In general, the CTRL/PWM pin is used for externally controlled applications and the ADIM register is used for internally controlled applications.

The CTRL/PWM pin provides a linear adjustment of the current sense threshold over the range of 0.2V to 1.2V. The low side of the CTRL/PWM range is set to allow a true zero current setting while tolerating offset in any external circuitry. Below 0.2V, the CTRL/PWM pin will be requesting zero LED current, and below 0.1V on CTRL/PWM will be interpreted as a PWM off signal.

On the high side of the CTRL/PWM range, the threshold adjustment will roll over to a fixed maximum of 250mV threshold as the CTRL/PWM pin exceeds 1.2V. To use the fixed 250mV threshold, it is recommended to tie the CTRL/PWM pin to a voltage higher than 1.2V. For convenience, the CTRL/PWM pin can simply be tied to $INTV_{CC}$.

The required CTRL/PWM voltage for a desired current sense threshold is given by Equation 2.

$$V_{CTRLPWM} = 4 \bullet V_{(ISP–ISN)} + 0.2V \quad (2)$$

The overall profile of current sense threshold vs CTRL/PWM voltage is shown in Figure 5.

The ADIM register takes the setpoint programmed by the CTRL/PWM pin and applies to it an 8-bit DAC function, where code 0 is equal to 1/256th of the CTRL/PWM threshold and code 255 is equal to the full CTRL/PWM threshold. For the case of the fixed 250mV threshold, the ADIM-adjusted threshold can be computed by Equation 3.

$$V_{(ISP–ISN)} = \frac{250mV \bullet (ADIM + 1)}{256} \quad (3)$$

When adjusting with both external and internal control in combination, it is important to consider the accuracy of the overall system: Although it is possible to program both the CTRL/PWM pin and the ADIM register to very small values, the product of those two small values may be too tiny for the amplifier to accurately regulate.

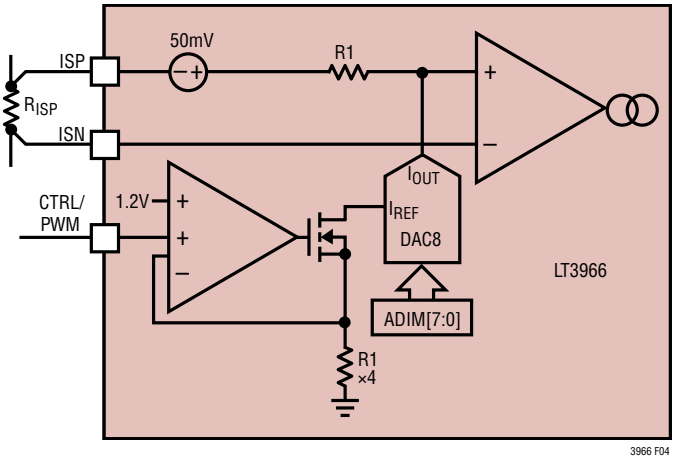


Figure 4.

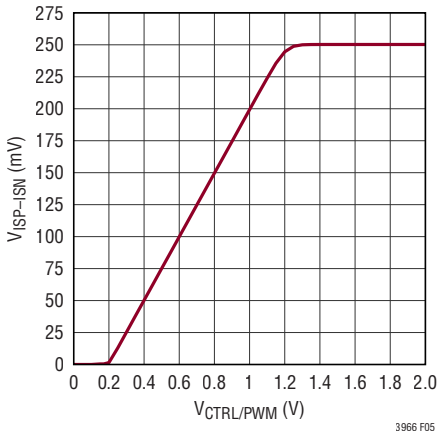


Figure 5.

APPLICATIONS INFORMATION

FAULT DETECTION USING ISP, ISN

LT3966 uses the ISP, ISN sense amplifier to detect overcurrent conditions in the LED. If the voltage between ISP/ISN exceeds 150% of the regulation threshold (370mV), an overcurrent fault is detected. The LT3966 will terminate switching on the faulted channel and pull TG high to disconnect the output. The fault status will be latched in the channel's OC status bit, and the $\overline{\text{ALERT}}$ flag will assert if reporting is enabled by the channel's OC_EN bit.

Response to overcurrent will depend on the state of that channel's LATOFF bit. If LATOFF is not set, the channel will enter a 7168-cycle cooldown mode before retrying a new soft-start cycle. This is commonly referred to as "hiccup" mode. If the LATOFF bit is set, the channel will stay in the off state until the fault or the LATOFF bit is cleared by the host.

For the case of a problem with the LT3966 voltage feedback, an additional limiter is incorporated to regulate the ISP pin to a maximum of 62V. If the ISP pin reaches 62V, the switching setpoint will be reduced to prevent the ISP pin from exceeding 62V.

TG DRIVER AND EXTERNAL PMOS SELECTION

PWM dimming and output disconnect are controlled by the TG pin through the use of an external PMOS pass device. TG provides a level-shifted MOSFET driver intended to drive the gate of the external PMOS between V_{ISP} and V_{ISP} – 8.2V.

Since the gate charging current passes through the LED current sense resistor, 2µs blanking time is added to the LED overcurrent sensing to avoid false tripping during TG transitions. This problem is most often seen when using a high value sense resistor for a small LED current. An alternative for this case is to use a smaller value sense resistor and a lower ISP–ISN threshold by adjusting the CTRL/PWM pin or ADIM register.

PWM DIMMING

PWM dimming of LEDs provides efficiency, accuracy, and color rendering benefits over analog dimming. The LT3966 provides both internal and external control of LED dimming. During PWM dimming off time, the switching is suspended, the TG pin is pulled up to turn off the external PMOS, and the internal control voltages are tri-stated to hold their value. In this manner, the chip can quickly resume its appropriate operating condition at next LED turn-on.

External LED dimming is controlled using the CTRL/PWM pin, and internal dimming is controlled using the onboard dimming generator. The final dimming control signal is the logical AND of both the CTRL/PWM input and the internal dimming generator. When the dimming generator is disabled by the DIMEN bit or by standalone mode, the dimming is controlled solely by the CTRL/PWM pin. The logical representation is shown in Figure 7.

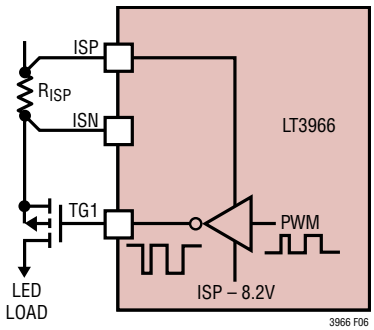


Figure 6.

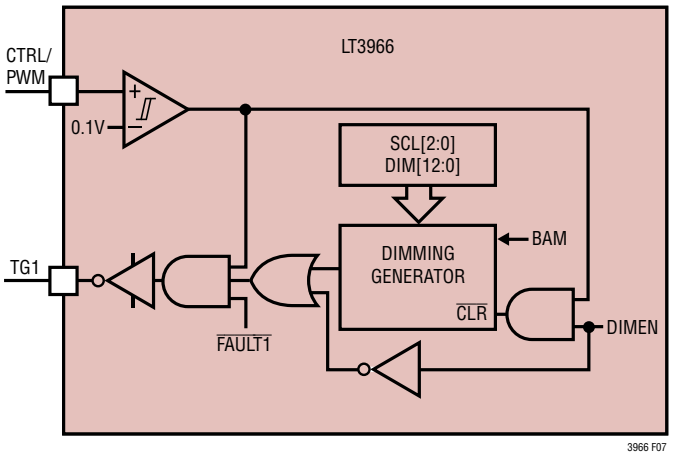


Figure 7.

APPLICATIONS INFORMATION

It is important to note that both the DIMEN signal and the CTRL/PWM pin have the ability to clear the dimming generator's counter. This is advantageous when using a combination of internal dimming and external ON/OFF control with CTRL/PWM. By restarting the dimming generator's counter in sync with the external ON/OFF signal, light output remains flicker free from full duty cycle to zero.

The CTRL/PWM threshold for PWM dimming is 0.1V. For simple on/off control, the PWM pin can be driven with any standard logic signal between 1.5V and 5V. For dimming with analog control, drive the pin with a DAC providing output shutdown, or simply shunt a resistor divider using a small NMOS transistor (Figure 8).

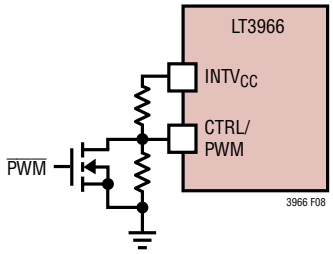


Figure 8.

The internal dimming generator is based on a variable-length counter updated at the master clock rate, determined by R_T. An overview of the logic is shown in Figure 9.

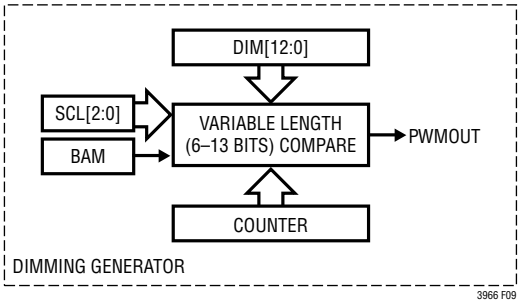


Figure 9.

The scale (SCL[2:0]) bits set the compare length and cycle length of the dimming generator, from 6-bit at SCL = 000b, to 13-bit at SCL = 111b. This cycle length determines the dimming resolution, and also the dimming frequency based on the MCLK value set by R_T, Equation 4.

$$f_{DIM} = \frac{f_{SW}}{2^{(6+SCL)}} \quad (4)$$

For example, a 13-bit dimming cycle using SCL = 111b would provide 8192:1 resolution at a dimming frequency of 244Hz using a 2MHz MCLK frequency (R_T = 47.5k).

The DIM[12:0] and BAM registers control the duty cycle and modulation strategy of the dimming generator. In PWM (Pulse-Width Modulation) dimming mode (BAM = 0), the PWMOUT signal is high while the value in the DIM register is greater than the Counter. In BAM (Bit-Angle Modulation) mode, the PWMOUT signal is high anytime the MSB of the Counter matches the position of a 1 in the value in the DIM register.

A comparison of the resulting waveforms of each of these strategies is shown in Figure 10. For a DIM value of 13, PWM mode provides a single pulse of 13 clock cycles starting at the 1st counter cycle. BAM mode provides pulses of duration 1, 4, and 8 cycles at the 1st, 4th, and 8th counter cycle, respectively. The total pulse duration in BAM mode still equals 13-clock cycles.

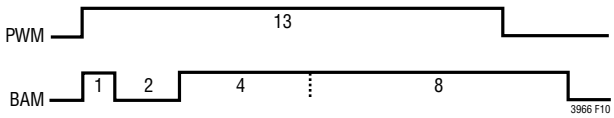


Figure 10.

The duty cycle of the dimming generator can be computed using Equation 5.

$$Duty = \frac{DIM}{2^{(6+SCL)}} \quad (5)$$

The system should be aware of the counter scale as defined by SCL, and avoid writing DIM values larger than the maximum value of counter. In the case where a DIM value is larger than the counter range, the DIM value will be truncated below bit (6+SCL). A DIM value of 0 0000 0000 0001 would be interpreted as 0 in all cases except SCL = 111b.

APPLICATIONS INFORMATION

DIMMING CODE CHANGES AND DIMMING SYNCHRONIZATION

To ensure glitch-free changes of the DIM, a new value of DIM is only loaded upon completion of the previous dimming cycle, at the rollover of the counter to 0. This prevents short or otherwise malformed pulses at the output, but will introduce a small latency depending on the dimming cycle length.

If a channel's dimming generator is disabled by setting the DIMEN bit to 0 or by bringing the channel's CTRL/PWM pin low, the counter for that channel will be halted and cleared to 0. Upon re-enabling the dimming generator, the counter value may not be synchronized to the other channels.

LT3966 allows all dimming generators on the I²C bus to be synchronized by initiating a write to the broadcast address, 0x18 (Figure 11).

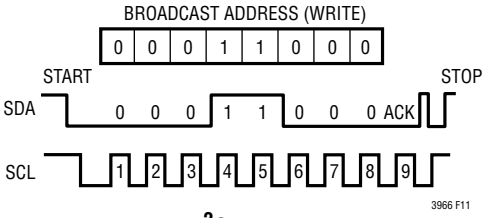


Figure 11. I²C Broadcast Write

When synchronizing the dimming generators or enabling a dimming generator by changing the DIMEN bit from 0 to 1, a one-clock low time will be seen at the output as the device clears the counter and loads the latest DIM code.

FB OUTPUT VOLTAGE SETTING

An output voltage limit is required for the case of an open LED strand. By connecting FB to a resistor divider between the output voltage and GND, a maximum output voltage limit can be set (see Figure 12).

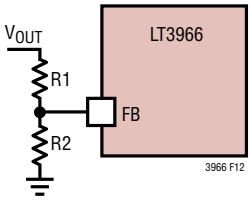


Figure 12.

Choose R1 and R2 so that the output voltage reaches the desired maximum when FB reaches its 1.2V regulation point, Equation 6.

$$V_{OUT} = 1.2 \bullet \left(1+\frac{R1}{R2}\right) \quad (6)$$

For the case of driving LEDs, the output voltage setting should be programmed higher than the maximum forward voltage of the LEDs being driven, when accounting for process and temperature variation.

FAULT DETECTION USING FB

LT3966 uses the FB pin voltage to detect shorted and overvoltage output conditions, as well as open output conditions. The conditions for these faults and response are as follows:

- A shorted output is detected by the FB voltage remaining at 300mV or lower after the device's soft-start has completed. In response, the channel's SHORT status bit will be asserted, and the device's $\overline{\text{ALERT}}$ pin will also assert if SHORT_EN is set. The device will either latchoff or enter a hiccup retry cycle dependent on the state of the faulted channel's LATOFF bit.
- Output overvoltage is detected by the FB pin exceeding the regulation point by 60mV (1.26V total). In response, the channel's OVFB status bit will be asserted, and the device's $\overline{\text{ALERT}}$ pin will also assert if OVFB_EN is set. The device will stop switching and raise TG to disconnect the output, and will resume normal operation once the FB has fallen by 25mV.
- An open output is detected by the combination of FB voltage reaching at least 1.15V and the LED current falling to less than 10% of full-scale value. In response, the channel's OPEN status bit will be asserted, and the $\overline{\text{ALERT}}$ pin will also assert if OPEN_EN is set. This condition is considered to be standard constant voltage regulation, and the channel will continue to switch while regulating FB to 1.2V.

APPLICATIONS INFORMATION

ENABLE AND EXTERNAL UVLO

The LT3966 enable pin provides a high voltage tolerant precision comparator and a 2µA hysteresis current source for generating programmable external UVLO.

The EN pin can be driven with a logic level signal greater than 1.5V for simple ON/OFF control, or can be tied to the input (up to 60V) for always-on operation. The pin is internally clamped to 6V through a 1MEG resistor, and will draw a small amount of current when driven to a voltage greater than 6V.

To use the EN pin as an external UVLO, simply tie the EN pin to a resistor divider between V_{IN} and GND (Figure 13). The shutdown (falling threshold) is 1.23V and the rising threshold provides 15mV internal hysteresis plus user-programmable external hysteresis through the use of a 2µA hysteresis current that is active anytime the EN pin is below the threshold.

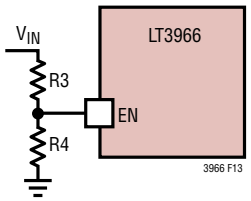


Figure 13.

To select an appropriate resistor divider for the EN pin, first determine the top resistor required for the desired hysteresis. Larger value resistors provide more external hysteresis due to the 2µA hysteresis current source, Equation 7.

$$R3 = \frac{V_{HYST} - 0.015V}{2\mu A} \quad (7)$$

A common choice is 487k for roughly 1V total hysteresis.

Next, determine the bottom resistor value by programming the accurate falling UVLO threshold based on R3 and the 1.23V EN falling threshold, Equation 8.

$$R4 = \frac{R3}{\left(\frac{V_{EN-FALL}}{1.23}\right) - 1} \quad (8)$$

The UVLO rising threshold will therefore be given by Equation 9.

$$V_{EN-RISE} = \frac{1 + R3}{R4} + 2\mu A \bullet R3 \quad (9)$$

If the EN pin is used in a multiple-tap resistor divider, be aware that although the pin voltage may safely reach 60V, a small amount of current will be drawn when EN is greater than 6V.

FREQUENCY SETTING USING RT

LT3966 uses a single master oscillator from which all internal clocks and the switching clocks are derived. Through I^2C, the channels can be programmed to switch 90° out of phase.

Switching frequency is set with a single resistor from the RT pin to GND.

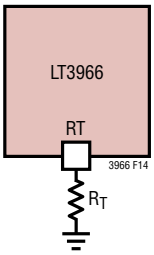


Figure 14.

Determine the proper R_T value for a desired switching frequency using Table 2 or Table 3.

Table 2. Single-Phase Switching Frequency vs R_T Value

SWITCHING FREQUENCY (SINGLE-PHASE)	R_T (kΩ)
300kHz	499
400kHz	261
500kHz	205
600kHz	174
700kHz	147
800kHz	127
900kHz	113
1MHz	100
1.2MHz	82.5
1.4MHz	69.8
1.6MHz	59
1.8MHz	52.3
2MHz	47.5

APPLICATIONS INFORMATION

Table 3. Multi-Phase Switching Frequency vs R_T Value

SWITCHING FREQUENCY (MULTI-PHASE)	R_T (kΩ)
300kHz	174
400kHz	127
500kHz	100
600kHz	82.5
700kHz	69.8
800kHz	59
900kHz	52.3
1MHz	47.5
1.2MHz	37.4
1.4MHz	31.6
1.6MHz	27.4
1.8MHz	23.7
2MHz	21

RT LIMITS

In order to provide safe and reliable operation, both minimum and maximum limits are set on the oscillator range using RT. For the case of an open circuit on RT, a low limit of roughly 230kHz is provided through a small internal bias. The RT pin itself is also current limited to provide an upper limit and to protect against a short circuit on the RT pin. This limit is 125µA, corresponding to a maximum frequency of roughly 7.5MHz.

FREQUENCY SYNCHRONIZATION INPUT AND OUTPUT

The LT3966 provides a bidirectional clock synchronization pin, SYNC, for synchronization input and output. The default state of SYNC is an input, used to synchronize the LT3966 to an external clock source. Drive the SYNC input with any logic-level clock output from 1.5V to 5V to provide external synchronization. Duty cycle of the external clock is not critical as long as the high time of the incoming clock is greater than 100ns. When synchronizing to an external clock, the R_T resistor should be set to give an unsynchronized frequency roughly 5% lower than the expected synchronization frequency. This minimizes disturbances during any transitions from internal to external clock.

The SYNC pin can also be programmed as an output, to provide a synchronization signal to other LT3966 in the system. In this mode, the SYNC pin outputs a 50% duty square wave of 0V to 2.5V. To use SYNC as an output, the SYNCOUT register bit should be set to 1. Do not drive the SYNC pin with an external clock when the SYNCOUT bit is set.

MULTIPHASE SWITCHING

To reduce input ripple current, the four boost converters can operate in 4-phase mode, where the rising edge of each converter's switching cycle is separated by 90° of phase shift.

To enable multiphase operation, set the MPHASE register bit to 1. In multiphase operation, the boost converter clocks run at half the speed of MCLK set by R_T, and their phase is shifted by 90° per channel as illustrated in Figure 15.

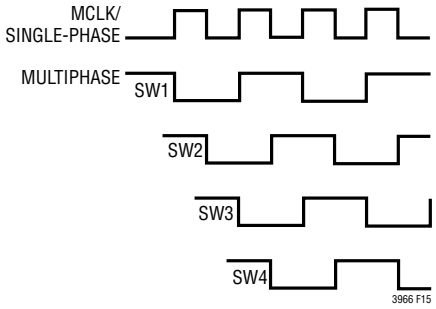


Figure 15.

Typically, the MCLK frequency is set using R_T to be equal to 2× the desired switching frequency when multiphase switching is used.

Although the boost channels operate at half frequency, the system MCLK continues to operate at the frequency determined by R_T. This simplifies synchronization to other LT3966 devices, since the SYNC output and SYNC input always uses the full MCLK frequency determined by R_T regardless of the multiphase setting of any individual LT3966. However, since the ADC converter is clocked from the master clock, using very high frequency MCLK settings may require the use of the ADC clock prescaler. More details on this setting are available in the ADC section.

APPLICATIONS INFORMATION

IN PHASE/OUT OF PHASE DIMMING

To reduce input ripple current, each channel's dimming operation can be independently programmed in one of the two modes: in-phase mode and out-of-phase mode (see Figure 16). When operating in in-phase mode, the start of CH2/CH3/CH4's dimming cycle is aligned with CH1's. When operating in out-of-phase mode, the start of CH2/CH3/CH4's dimming cycle is behind of CH1's by a quarter/a half/three quarters of CH2/CH3/CH4's dimming cycle. To enable the in-phase/out-of-phase operation, set the INPH register bit to 1/0. Please note that after the INPH bit change, an I^2C broadcast write (see Figure 11) is required to reset all dimming generators for this function to work properly.

POWER COMPONENT SELECTION

Since the LT3966 is an internally-compensated converter, the external power components are selected to ensure system stability. By following a few simple guidelines, this process can be made simple and streamlined.

Inductor Selection

Inductor selection consists of two parameters: saturation current rating, and inductance value. Higher switching frequency allows the use of smaller inductance value at the expense of increased switching loss.

The saturation current rating of the inductor should be selected appropriately for the 2.4A current limit of the LT3966. An approximation for maximum inductor current (efficiency = 100%) is based on the maximum LED current and the input-output ratio, Equation 10.

$$I_L = \frac{V_{OUT}}{V_{IN}} \bullet I_{LED} \quad (10)$$

The desired inductance is determined by the steady-state current ripple. A typical rule of thumb is to set the inductor current ripple to a maximum of 20% of the maximum inductor current, Equation 11, Equation 12 and Equation 13.

Boost:

$$L_{BOOST} \geq \left(\frac{V_{IN(MIN)} \bullet (V_{OUT(MAX)} - V_{IN(MIN)})}{V_{OUT(MAX)} \bullet 0.45A \bullet f_{SW}} \right) \quad (11)$$

Buck:

$$L_{BUCK} \geq \left(\frac{V_{OUT(MAX)} \bullet (V_{IN(MIN)} - V_{OUT(MAX)})}{V_{IN(MIN)} \bullet 0.45A \bullet f_{SW}} \right) \quad (12)$$

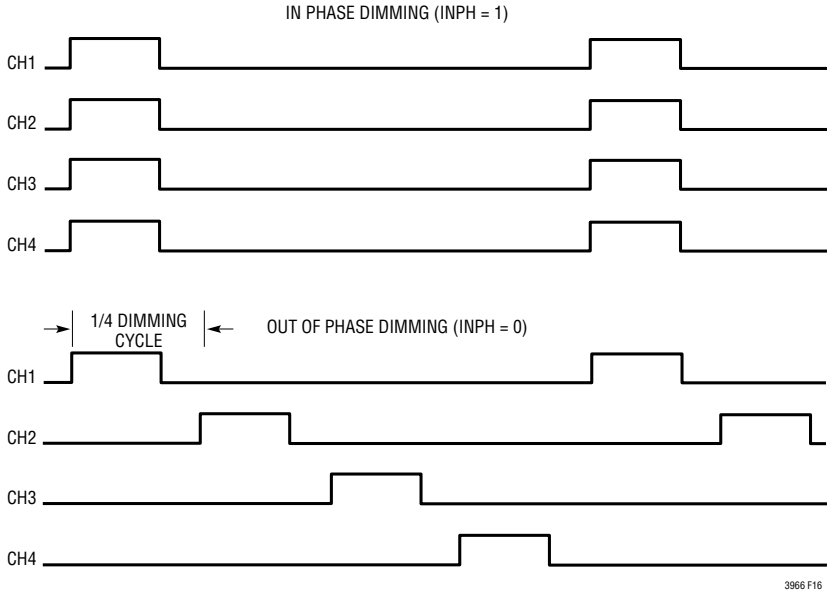


Figure 16.

APPLICATIONS INFORMATION

Buck-Boost:

$$L_{BUCK} \geq \left(\frac{V_{IN(MIN)} \bullet V_{OUT(MAX)} / V_{IN(MIN)} + V_{OUT(MAX)}}{0.45A \bullet f_{SW}} \right) \quad (13)$$

Table 4 provides some recommended inductor vendors.

Table 4. Inductor Manufacturers

VENDOR	WEB
Wurth Elektronik	www.we-online.com
Coilcraft	www.coilcraft.com
Cooper	www.cooperet.com

Output Capacitor Selection

In addition to smoothing the output voltage, the output capacitor in combination with the small signal forward resistance of the LEDs provides an output pole for the frequency compensation.

The LED forward resistance (R_{LED}) is determined from the LED data sheet, and is roughly 10Ω for the case of a typical 150mA LED. Forward resistance is highest at low currents, and lowest at the maximum drive current. The total forward resistance of a series strand of LED is $n \bullet R_{LED}$, where n is the number of LEDs in the strand.

For the LT3966, we choose C_{OUT} to keep the minimum frequency of the output pole > 2kHz, Equation 14.

$$C_{OUT} \leq \frac{1}{12500 \bullet n \bullet R_{LED}} \quad (14)$$

In most cases, a 2.2µF output capacitor is a suitable choice.

Schottky Rectifier Diode

The power Schottky diode conducts the switching current during the power switch off time. Select a diode rated for at least $1.5 \bullet I_{LED}$ to provide operating margin. The reverse breakdown voltage should be at least 20% greater than the maximum output voltage expected in circuit. Keep in mind that in the case of disconnected LEDs, the output voltage will be driven to the limit defined by the FB divider.

FAULTS AND FAULT HANDLING

Status Bits and $\overline{\text{ALERT}}$

The LT3966 has independent fault handling for each LED driver channel. Four types of faults are detected: LED Overcurrent, Shorted LED, Open LED, and Output Overvoltage. Additional information on the detection conditions is provided in the LED current sense amplifier, and FB amplifier sections.

As described, each type of fault is indicated in a channel's status bit and can optionally be indicated on the open-drain $\overline{\text{ALERT}}$ pin through the setting of fault enable bits in the same register. When a fault's enable bit is set, the fault status will be latched and the $\overline{\text{ALERT}}$ pin will be asserted if a fault is detected. Write a 0 to the status bit to clear, or write a 0 to the status bit enable bit to clear and disable the fault. If a fault's EN mask bit is not set, reading the status bit will always give the status of the fault at that time, but the status will not be latched nor indicated on the $\overline{\text{ALERT}}$ pin.

In standalone mode, the mask bits are ignored and the logical OR of all faults is indicated on the $\overline{\text{ALERT}}$ pin. This indicator is not latched, and will only be asserted as long as a fault is present. The $\overline{\text{ALERT}}$ pin will return to high impedance when no faults are detected in standalone mode.

Hiccup and Latchoff Mode

The LED overcurrent and shorted LED conditions result in an internal fault response that is dependent on the state of the channels' latchoff (LATOFF) bit. In the case of one of these faults, switching is terminated, the channel's TG pin is pulled high to disconnect the output, and the device waits for a 7168-cycle cooldown period.

At this point if the channel's LATOFF bit is set, the device will stay in this non-switching rest state until reset by toggling the EN pin or system power, toggling the channel's OFF bit, or by clearing the LATOFF bit itself.

If the channel's LATOFF bit is not set, the device will attempt a new soft-start cycle after completion of the cooldown period. Sustained faults will result in continuing cooldown and retry attempts, often referred to as "hiccup" mode (see Figure 17 and Figure 18).

APPLICATIONS INFORMATION

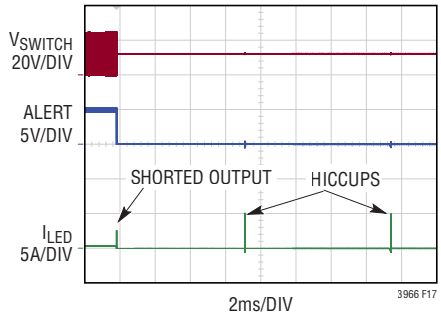


Figure 17. Scope Shot – HICCUP

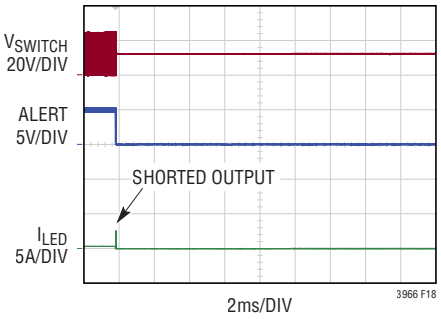


Figure 18. Scope Shot – LATOFF

Broadcast Alert Response

In order to determine which device on a common bus is faulted, the LT3966 supports Broadcast Alert Response on the standard address of 0001100 (Figure 19). Any LT3966 with a fault on an enabled fault status bit will enter arbitration upon receiving a broadcast read command (0x19). PEC is not used during arbitration. It is neither sent, not expected. During arbitration, the faulted LT3966 will attempt to clock out its own address to the host. Since the I^2C data line is common drain, the device with the lowest address will eventually win arbitration by outputting a 0 when other devices attempt to output a 1. If the LT3966 fails arbitration, it will stop and wait for a new broadcast attempt while keeping the $\overline{\text{ALERT}}$ line asserted. Once LT3966 successfully completes arbitration it will release its' pull-down on the $\overline{\text{ALERT}}$ line. The fault status bits can then be read by the host to determine the cause of the $\overline{\text{ALERT}}$.

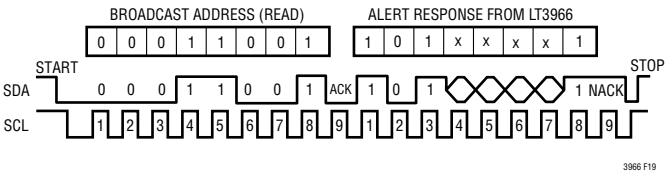


Figure 19. I^2C Broadcast Alert Response

Once an ARA arbitration has released the $\overline{\text{ALERT}}$ line, the LT3966 will not pull the $\overline{\text{ALERT}}$ line low again until the faulted status bit has been cleared, and a new fault has been detected.

ADDITIONAL FEATURES

Watchdog Timer

To ensure reliability against a break in the I^2C bus, an optional watchdog timer feature is available. The watchdog timer is enabled through the WDTEN bit in register 0x00.

The watchdog timer contains a standalone 40kHz oscillator and 100ms counter that is reset by the detection of any I^2C start condition on the bus. Once enabled, the watchdog requires the host to occasionally initiate an I^2C transaction using an I^2C start. Data transfer is not required to reset the watchdog timer.

In the event that the 100ms watchdog period expires without detecting an I^2C start, the LT3966 will reset to the power-on default conditions and the watchdog flag bit (WDTFLAG) will be set in register 0x00.

Device ID Register

The LT3966 contains a device identifier in the highest three addresses in the register space. When read, the addresses 0xFD, 0xFE, and 0xFF will contain the BCD-encoded values 03, 96 and 60, respectively.

ANALOG-TO-DIGITAL CONVERTER OPERATION

ADC Structure and Operation

LT3966 contains an 11-input, 8-bit SAR ADC used to measure various parameters of the system. These parameters include FB voltage and LED current for each of the 4 LED driver channels, scaled input voltage, and two uncommitted external inputs. An overview of the ADC architecture is shown in Figure 20.

APPLICATIONS INFORMATION

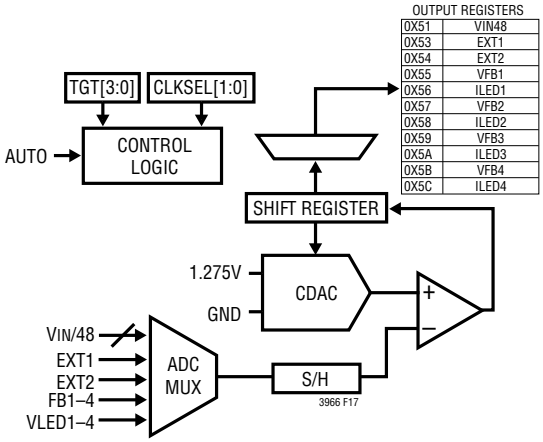


Figure 20. Scope Shot – LATOFF

When measuring a voltage, the range of the ADC is 0V to 1.275V and the LSB is 5mV.

The ADC can be used in manual (single) or automatic mode. In manual mode, one conversion is taken for a single target specified by the TGT[3:0] register, and the result is stored in the target's data register. The ADC powers down after completion. In automatic mode (RUN = AUTO = 1), all active targets will be continuously measured in a round-robin fashion. When the last target is completed, the converter will start again with the first target. This ensures that fresh data is available for all enabled targets at any given time.

Manual Mode – Repeated Conversions

In manual mode (RUN = 1, AUTO = 0), multiple repeated conversions on the same target can be performed with little overhead. The first conversion starts upon detection of the I^2C Stop signal in the transfer in which the ADC's RUN bit is written to 1. The ADC completes one conversion and enters sleep mode. Reading the ADC result without clearing the RUN bit will trigger a new conversion at the I^2C Stop signal following the data read. In this manner, an unlimited number of conversions and reads can be executed in series.

When repeated conversions are used, a conversion time (t_{CONV}) of at least 20ADC clock periods between an I^2C Stop and the next I^2C Start is required to complete the conversion before data can be read. This time is dependent upon R_T and the value in the ADC's CLKSEL register bits. If a new I^2C Start occurs before the data is ready, the data read will be the prior conversion's data, and the new data will be transferred upon the next I^2C Stop. The appropriate timing is shown in Figure 21.

Automatic Mode

The ADC will operate in automatic mode when the AUTO bit is set. In this mode, the ADC runs continuously, measuring each active input and updating the target data register. This sequence repeats indefinitely, and does not wait for an I^2C Stop to begin the next round of conversions. Additionally, data can be read at any time. In this manner, automatic mode will always provide fresh data for all active targets.

In the case of a disabled channel (OFF = 1), both the FB and I_{LED} measurements for that channel will be skipped. For a channel that is enabled, but is in a PWM off time from either CTRL/PWM or dimming generator low time, the converter will not skip that channel but will instead wait for the channel's PWM signal to rise before sampling. Be aware that when using CTRL/PWM for external dimming, long off times in the external signal will result in equivalent pauses in the ADC converter's measurement sequence.

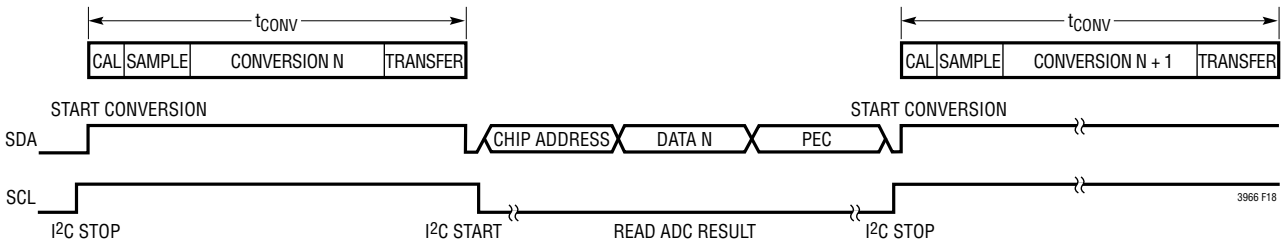


Figure 21.

APPLICATIONS INFORMATION

When switching from manual to automatic mode, conversion will start from the target specified by TGT[3:0].

ADC Target 0 – VIN/48

The first target (TGT = 000) is a 1/48th scaled version of the chip input voltage, suitable for monitoring input voltage or battery state. The resolution of 5mV/LSB and 48× scale results in a resolution at the input of roughly 240mV/LSB. Input range for V_{IN} is 3V to 60V, resulting in a code range of roughly 12 to 250 decimal. To determine the input voltage from the conversion data, use Equation 15.

$$V_{IN}\ (V) = 0.24 \bullet V_{IN}[7:0] \quad (15)$$

ADC Targets 2–3 – External Inputs

LT3966 provides two external analog inputs to the ADC, on EXT1 and EXT2. The working range of these inputs are 0V to 1.275V, and the conversion resolution is 5mV/LSB.

The EXT1 and EXT2 inputs are internally clamped to 1.7V with a 2k series resistance, but the pins are rated up to 5.5V ABSMAX. If the clamp voltage of 1.7V is exceeded, the EXT1 and EXT2 inputs will draw current but no damage will occur. For any voltage above 1.275V, the ADC conversion will read full scale, 0xFF.

ADC Targets 4–11 – LED Driver Parameters

The final 8 targets are FB voltage, and LED current for each of the 4 channels in turn. The FB measurement is a direct representation of the voltage at the FB pin, and the LED current measurement is a 4× multiplied version of the sense voltage between ISP and ISN.

ADC Clock Selection

The ADC clock is derived from the system master clock, MCLK, programmed by R_T. For best results, an ADC clock between 1µs and 2µs is recommended. Scaling down of MCLK to ADC clock is accomplished through the use of the CLKSEL[1:0] bits.

CLKSEL[1:0]	ADC CLOCK
00	MCLK
01	MCLK/2
10	MCLK/4
11	MCLK/8

REGISTER TABLE

ADDR	NAME	DESCRIPTION	b7	b6	b5	b4	b3	b2	b1	b0
Global Registers										
0x00	GLBCFG	Global Config	WDTFLAG	WDTEN	MPHASE	CLKOUT	OFF4	OFF3	OFF2	OFF1
Channel 1										
0x10	STAT1	Status/Status CFG	OC_EN 1	SHORT_EN1	OPEN_EN1	OVFB_EN1	OC1	SHORT1	OPEN1	OVFB1
0x11	CFG1	Channel 1 Config	x	x	x	x	INPH1	FLAT1	BAM1	DIMEN1
0x12	DIM1H	PWM Dim Value CH1	SCL12	SCL11	SCL10	DIM14	DIM13	DIM12	DIM11	DIM10
0x13	DIM1L	PWM Dim Value CH1	DIM112	DIM111	DIM110	DIM19	DIM18	DIM17	DIM16	DIM15
0x14	ADIM1	Analog Dimming CH1	ADIM17	ADIM16	ADIM15	ADIM14	ADIM13	ADIM12	ADIM11	ADIM10
Channel 2										
0x20	STAT2	Status/Status CFG	OC_EN 2	SHORT_EN2	OPEN_ EN2	OVFB_EN2	OC2	SHORT2	OPEN2	OVFB2
0x21	CFG2	Channel 2 Config	x	x	x	x	INPH2	FLAT2	BAM2	DIMEN2
0x22	DIM2H	PWM Dim Value CH2	SCL22	SCL21	SCL20	DIM24	DIM23	DIM22	DIM21	DIM20
0x23	DIM2L	PWM Dim Value CH2	DIM212	DIM211	DIM210	DIM29	DIM28	DIM27	DIM26	DIM25
0x24	ADIM2	Analog Dimming CH2	ADIM27	ADIM26	ADIM25	ADIM24	ADIM23	ADIM22	ADIM21	ADIM20
Channel 3										
0x30	STAT3	Status/Status CFG	OC_EN3	SHORT_EN3	OPEN_EN3	OVFB_EN3	OC3	SHORT3	OPEN3	OVFB3
0x31	CFG3	Channel 3 Config	x	x	x	x	INPH3	FLAT3	BAM3	DIMEN3
0x32	DIM3H	PWM Dim Value CH3	SCL32	SCL31	SCL30	DIM34	DIM33	DIM32	DIM31	DIM30
0x33	DIM3L	PWM Dim Value CH3	DIM312	DIM311	DIM310	DIM39	DIM38	DIM37	DIM36	DIM35
0x34	ADIM3	Analog Dimming CH3	ADIM37	ADIM36	ADIM35	ADIM34	ADIM33	ADIM32	ADIM31	ADIM30
Channel 4										
0x40	STAT4	Status/Status CFG	OC_EN4	SHORT_EN4	OPEN_EN4	OVFB_EN4	OC4	SHORT4	OPEN4	OVFB4
0x41	CFG4	Channel 4 Config	x	x	x	x	INPH4	FLAT4	BAM4	DIMEN4
0x42	DIM4H	PWM Dim Value CH4	SCL42	SCL41	SCL40	DIM44	DIM43	DIM42	DIM41	DIM40
0x43	DIM4L	PWM Dim Value CH4	DIM412	DIM411	DIM410	DIM49	DIM48	DIM47	DIM46	DIM45
0x44	ADIM4	Analog Dimming CH4	ADIM47	ADIM46	ADIM45	ADIM44	ADIM43	ADIM42	ADIM41	ADIM40
Analog-to-Digital Converter										
0x50	ADCCFG	ADC Config	RUN	AUTO	CLKSEL1	CLKSEL0	TGT3	TGT2	TGT1	TGT0
0x51	VIN	Scaled Input Voltage	VIN7	VIN6	VIN5	VIN4	VIN3	VIN2	VIN1	VIN0
0x53	EXT1	External Voltage 1	EXT17	EXT16	EXT15	EXT14	EXT13	EXT12	EXT11	EXT10
0x54	EXT2	External Voltage 2	EXT27	EXT26	EXT25	EXT24	EXT23	EXT22	EXT21	EXT20
0x55	VFB1	Ch 1 FB Voltage	VFB17	VFB16	VFB15	VFB14	VFB13	VFB12	VFB11	VFB10
0x56	ILED1	Ch 1 LED Current	ILED17	ILED16	ILED15	ILED14	ILED13	ILED12	ILED11	ILED10
0x57	VFB2	Ch 2 FB Voltage	VFB27	VFB26	VFB25	VFB24	VFB23	VFB22	VFB21	VFB20
0x58	ILED2	Ch 2 LED Current	ILED27	ILED26	ILED25	ILED24	ILED23	ILED22	ILED21	ILED20
0x59	VFB3	Ch 3 FB Voltage	VFB37	VFB36	VFB35	VFB34	VFB33	VFB32	VFB31	VFB30
0x5A	ILED3	Ch 3 LED Current	ILED37	ILED36	ILED35	ILED34	ILED33	ILED32	ILED31	ILED30
0x5B	VFB4	Ch 4 FB Voltage	VFB47	VFB46	VFB45	VFB44	VFB43	VFB42	VFB41	VFB40
0x5C	ILED4	Ch 4 LED Current	ILED47	ILED46	ILED45	ILED44	ILED43	ILED42	ILED41	ILED40

REGISTER TABLE

ADDR	NAME	DESCRIPTION	b7	b6	b5	b4	b3	b2	b1	b0
Part ID (BCD Encoded, "03 96 60")										
0xFD	ID0	Part ID High	0	0	0	0	0	0	1	1
0xFE	ID1	Part ID Mid	1	0	0	1	0	1	1	0
0xFF	ID2	Part ID Low	0	1	1	0	0	0	0	0

GLOBAL CONFIGURATION REGISTER

Default Value: 0000 0000

ADDR	NAME	DESCRIPTION	b7	b6	b5	b4	b3	b2	b1	b0
0x00	GLBCFG	Channel Config	WDTFLAG	WDTEN	MPHASE	CLKOUT	OFF3	OFF2	OFF1	OFF0

Bit Description

b[7] **WDTFLAG:** Watchdog Timer Status. This bit indicates if the device has been reset by the WDT. It is cleared by disabling the WDT.

b[6] **WDTEN:** Watchdog Timer Enable. When set, LT3966 requires an I^2C start condition every 100ms to verify the communication interface is good. If the WDT expires without an I^2C start being detected, the chip will force a power-on-reset to the default state.

b[5] **MPHASE:** Multiphase DC/DC Converter Clocking. When MPHASE is set, the 4 DC/DC channels operate at MCLK/2, with 90° of phase shift between each channel.

b[4] **CLKOUT:** SYNC Pin Direction. Default = 0, SYNC = Input. When set, the SYNC pin becomes an output and drives the MCLK signal, for synchronizing other devices. The output frequency is always that of MLCK, regardless of the state of MPHASE. This allows a slave LT3966 to run at equal frequency to the master LT3966 even in multiphase mode.

b[3:0] **OFF[3:0]:** OFF/ON Control for Each Channel. Channels are all on by default, and controlled by EN. Set the OFF bit to disable a channel.

REGISTER DETAILS

LED DRIVER CHANNEL REGISTERS

Each of the 4 LED driver channels is configured through its 4-register bank. The channel registers are located at address 0x10–0x13, 0x20–0x23, 0x30–0x33, and 0x40–0x43 for the 4 channels, respectively.

Default Values: 0000 0000, 0000 0000, 0000 0000, 1111 1111

OFFSET	NAME	DESCRIPTION	b7	b6	b5	b4	b3	b2	b1	b0
0x00	STAT	Status/Status CFG	OC_EN	SHORT_EN	OPEN_EN	OVFB_EN	OC	SHORT	OPEN	OVFB
0x01	CFG	Channel Config	x	x	x	x	INPH	LATOFF	BAM	DIMEN
0x02	DIMH	PWM Dim Value	SCL2	SCL1	SCL0	DIM4	DIM3	DIM2	DIM1	DIM0
0x03	DIML	PWM Dim Value	DIM12	DIM11	DIM10	DIM9	DIM8	DIM7	DIM6	DIM5
0x04	ADIM	Analog Dimming	ADIM7	ADIM6	ADIM5	ADIM4	ADIM3	ADIM2	ADIM1	ADIM0

Bit Descriptions

STAT

OFFSET	NAME	DESCRIPTION	b7	b6	b5	b4	b3	b2	b1	b0
0x00	STAT	Status/Status CFG	OC_EN	SHORT_EN	OPEN_EN	OVFB_EN	OC	SHORT	OPEN	OVFB

b[7] **OC_EN:** LED Overcurrent Reporting Enable. Set this bit high to enable LED overcurrent fault reporting on the $\overline{\text{ALERT}}$ pin. If clear, $\overline{\text{ALERT}}$ is not triggered during an LED overcurrent event.

b[6] **SHORT_EN:** Shorted LED Reporting Enable. Set this bit high to enable SHORTLED fault reporting on the $\overline{\text{ALERT}}$ pin. If clear, $\overline{\text{ALERT}}$ is not triggered during a SHORTLED event.

b[5] **OPEN_EN:** Open LED Reporting Enable. Set this bit high to enable OPENLED fault reporting on the $\overline{\text{ALERT}}$ pin. If clear, $\overline{\text{ALERT}}$ is not triggered during an OPENLED event.

b[4] **OVFB_EN:** FB Overvoltage Reporting Enable. Set this bit high to enable FB overvoltage fault reporting on the $\overline{\text{ALERT}}$ pin. If clear, $\overline{\text{ALERT}}$ is not triggered during an OPENLED event.

b[3] **OC:** LED Overcurrent Status. This bit is asserted when a differential of 375mV or greater is detected at the ISP–ISN sense amplifier. If the corresponding OC_EN bit is enabled, $\overline{\text{ALERT}}$ is asserted and the status bit is latched until either OC or OC_EN is written to 0 by the host. If the corresponding enable bit is clear, the status is not latched and will reflect the present state of the LED overcurrent detector.

If the channel's LATOFF (latchoff) bit is set, an LED overcurrent fault will result in latched shutdown of the faulted channel until either OC or LATOFF is written to 0 by the host. If the channel's LATOFF bit is not set, the faulted channel will enter the hiccup cycle of shutdown and attempted restart.

REGISTER TABLE

b[2] **SHORT:** Shorted LED Status. This bit is asserted when the corresponding channel's FB pin is below 300mV and the internal soft start has completed. If the corresponding SHORT_EN bit is enabled, $\overline{\text{ALERT}}$ is asserted and the fault status is latched until either SHORT or SHORT_EN is written to 0 by the host. If the corresponding enable bit is clear, the status is not latched and will reflect the present state of the Shorted LED detector.

If the channel's LATOFF (latchoff) bit is set, a Shorted LED fault will result in latched shutdown of the faulted channel until either SHORT or LATOFF is written to 0 by the host. If the channel's LATOFF bit is not set, the faulted channel will enter the hiccup cycle of shutdown and attempt to restart.

b[1] **OPEN:** OPENLED Status. This bit is asserted when the corresponding channel's FB pin is above 1.15V and ISP–ISN is less than 25mV. If the corresponding OPEN_EN bit is enabled, $\overline{\text{ALERT}}$ is asserted and the fault status is latched until either OPEN or OPEN_EN is written to 0 by the host. If the corresponding enable bit is clear, the status is not latched and will reflect the present state of the open LED detector.

Open LED does not generate a hiccup or latchoff event.

b[0] **OVFB:** FB Overvoltage Status. This bit is asserted when the corresponding channel's FB pin is above 1.26V. If the corresponding OVFB_EN bit is enabled, $\overline{\text{ALERT}}$ is asserted and the status bit is latched until either OVFB or OVFB_EN is written to 0 by the host. If the corresponding enable bit is clear, the status is not latched and will reflect the present state of the FB overvoltage detector.

FB overvoltage does not generate a hiccup or latchoff event.

LED Driver Configuration

OFFSET	NAME	DESCRIPTION	b7	b6	b5	b4	b3	b2	b1	b0
0x01	CFG	Channel Config	x	x	x	x	INPH	LATOFF	BAM	DIMEN

Bit Description

b[7:4] **RFU:** Reserved for Future Use. Bits read as 0, writes do nothing.

b[3] **INPH:** In Phase Mode Select. When set to 1, the dimming is in phase, which means that the start of the channel's dimming cycle is aligned with CH1's. When set to 0, the dimming is out of phase. In this case, the start of CH2/CH3/CH4's dimming cycle is behind of CH1's by a quarter/a half/three quarters of CH2/CH3/CH4's dimming cycle.

b[2] **LATOFF:** Latchoff Mode. When set, OC or SHORT fault cause channel to latchoff until the fault bit is cleared by master. When LATOFF is clear, channel will enter hiccup mode to retry.

b[1] **BAM:** Bit Angle Modulation Select. When set to 1, the dimming generator outputs Bit-Angle-Modulation. When set to 0, the dimming generator outputs Pulse Width Modulation.

b[3:0] **DIMEN:** Dimming Generator Enable Bits. PWM dimming is the logical AND of the dimming generator output and the CTRL/PWM comparator output. When DIMEN = 0, the PWM generator is disabled and bypassed and dimming is controlled solely by the CTRL/PWM comparator.

REGISTER TABLE

LED Driver Dimming Generator

OFFSET	NAME	DESCRIPTION	b7	b6	b5	b4	b3	b2	b1	b0
0x02	DIMH	PWM Dim Value	SCL2	SCL1	SCL0	DIM4	DIM3	DIM2	DIM1	DIM0
0x03	DIML	PWM Dim Value	DIM12	DIM11	DIM10	DIM9	DIM8	DIM7	DIM6	DIM5

Bit Description

b[7] **SCL[2:0]:** PWM Cycle Length Select. Value from 0 to 7 chooses PWM counter length from 6 to 13 bits. This sets the period of the PWM generator to $n = 2^{(6 + SEL)}$ counts of the master clock. In the case where a DIM value is larger than the counter length, the DIM value will be truncated below bit (6+SCL). A DIM value of 0 0000 0000 0001 would be interpreted as 0 in all cases except SCL = 111b.

b[4] **DIM[12:0]:** PWM Dimming Setpoint. Specifies the on time of the PWM generator, where period is defined by SEL. PWM duty cycle is therefore: DIM/n and ranges from 0 to (n-1)/n. To reach 100% on time, simply disable the dimming generator using the DIMEN bit.

LED Driver Analog Dimming

Offset	Name	Description	b7	b6	b5	b4	b3	b2	b1	b0
0x04	ADIM	Analog Dimming	ADIM7	ADIM6	ADIM5	ADIM4	ADIM3	ADIM2	ADIM1	ADIM0

Bit Description

b[7] **ADIM[7:0]:** Modulates the external current sense threshold set by CTRL by the value in the ADIM register. The default value for ADIM[7:0] is 255.

ANALOG-TO-DIGITAL CONVERTER REGISTERS

ADC Configuration

Default Value: 0000 0000

ADDR	NAME	DESCRIPTION	b7	b6	b5	b4	b3	b2	b1	b0
0x50	ADCCFG	ADC Config	RUN	AUTO	CLKSEL1	CLKSEL0	TGT3	TGT2	TGT1	TGT0

REGISTER TABLE

Bit Description

ADCCFG1

b[7] **RUN:** Set to 1 to start conversion.

b[6] **AUTO:** Set to 0 for single conversion on a target specified by TGT[3:0]. Set to 1 for automatic continuous conversion. In automatic continuous mode, all active inputs will be repeatedly measured in a round-robin fashion. **Any channels that are disabled (OFF) will be skipped, but channels that are enabled yet in PWM low will cause the ADC to wait for the next PWM high. Upon PWM high, a conversion will take place and the sequence will continue**. Data is double-buffered so result registers will always contain valid data.

b[5:4] **CLKSEL[1:0]:** Choose ADC clock divider. For best results, set ADC bit time >1µs.

CLKSEL[1:0]	ADC CLOCK
00	MCLK
01	MCLK/2
10	MCLK/4
11	MCLK/8

b[3:0] **TGT[3:0]:** Only used in single conversion mode. Sets conversion target as shown in the table below.

TGT[3:0]	TARGET
0x00	Scaled V_{IN}
0x01	Not Valid
0x02	External 1
0x03	External 2
0x04	CH1 V_{FB}
0x05	CH1 I_{LED}
0x06	CH2 V_{FB}
0x07	CH2 I_{LED}

TGT[3:0]	TARGET
0x08	CH3 V_{FB}
0x09	CH3 I_{LED}
0x0A	CH4 V_{FB}
0x0B	CH4 I_{LED}
0x0C	Not valid
0x0D	Not valid
0x0E	Not valid
0x0F	Not valid

REGISTER TABLE

ADC Result Registers

Default Value: Indeterminate Until Written by ADC

ADDR	NAME	DESCRIPTION	b7	b6	b5	b4	b3	b2	b1	b0
0x51	VIN	VIN/48	VIN7	VIN6	VIN5	VIN4	VIN3	VIN2	VIN1	VIN0
0x53	EXT1	External Voltage 1	EXT17	EXT16	EXT15	EXT14	EXT13	EXT12	EXT11	EXT10
0x54	EXT2	External Voltage 2	EXT27	EXT26	EXT25	EXT24	EXT23	EXT22	EXT21	EXT20
0x55	VFB1	Ch 1 FB Voltage	VFB17	VFB16	VFB15	VFB14	VFB13	VFB12	VFB11	VFB10
0x56	ILED1	Ch 1 LED Current	ILED17	ILED16	ILED15	ILED14	ILED13	ILED12	ILED11	ILED10
0x57	VFB2	Ch 2 FB Voltage	VFB27	VFB26	VFB25	VFB24	VFB23	VFB22	VFB21	VFB20
0x58	ILED2	Ch 2 LED Current	ILED27	ILED26	ILED25	ILED24	ILED23	ILED22	ILED21	ILED20
0x59	VFB3	Ch 3 FB Voltage	VFB37	VFB36	VFB35	VFB34	VFB33	VFB32	VFB31	VFB30
0x5A	ILED3	Ch 3 LED Current	ILED37	ILED36	ILED35	ILED34	ILED33	ILED32	ILED31	ILED30
0x5B	VFB4	Ch 4 FB Voltage	VFB47	VFB46	VFB45	VFB44	VFB43	VFB42	VFB41	VFB40
0x5C	ILED4	Ch 4 LED Current	ILED47	ILED46	ILED45	ILED44	ILED43	ILED42	ILED41	ILED40

Registers 0x51 and 0x53–0x5C hold the ADC results for the 11 channels. They are read-only registers.

All measurements are 5mV per LSB

0x51: V_{IN}. A scaled (1/48) measurement of the chip input voltage.

0x53: EXT1. External Input 1. Working range is 0V–1.275V, pin is clamped at 1.7V.

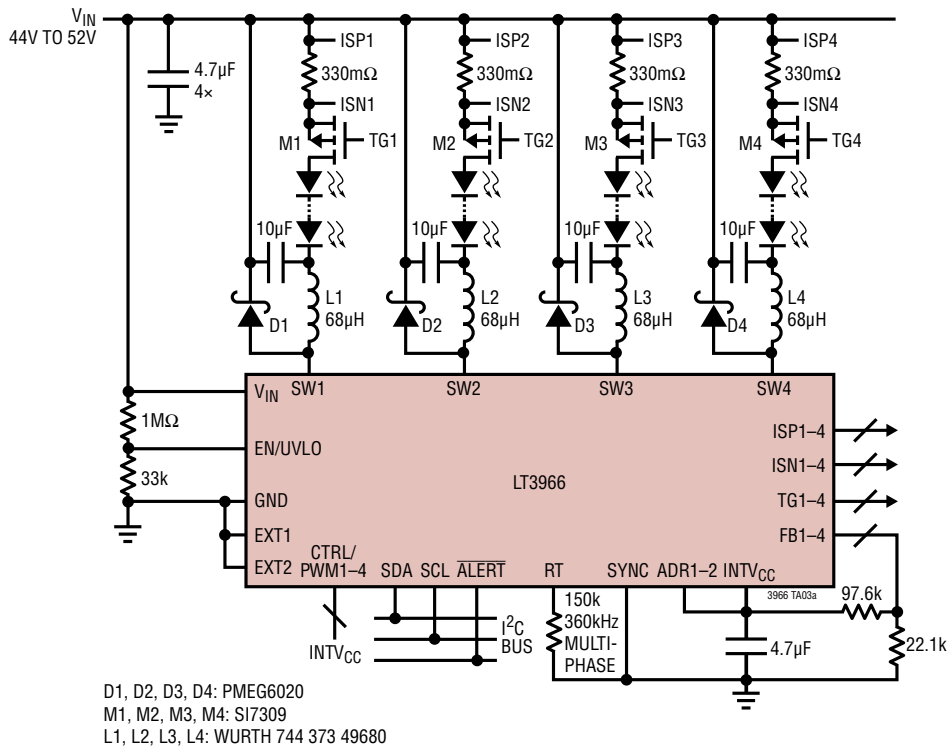
0x54: EXT2. External Input 1. Working range is 0V–1.275V, pin is clamped at 1.7V.

0x55, 0x57, 0x59, 0x5A: FB1–4. Channel feedback voltage measurement.

0x56, 0x58, 0x5A, 0x5C: VLED1–4. LED current measurement. Equal to 4× the sensed voltage on ISP–ISN.

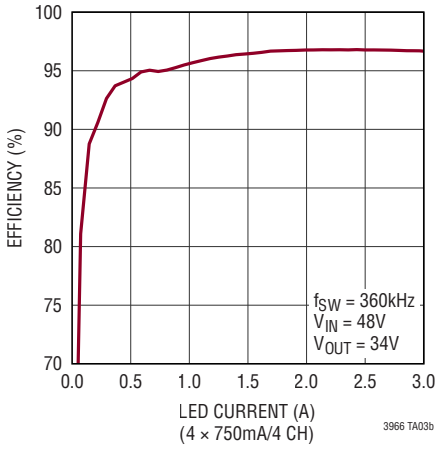
TYPICAL APPLICATIONS

100W, Quad 750mA × 12 LED Buck Mode Driver with I²C Dimming

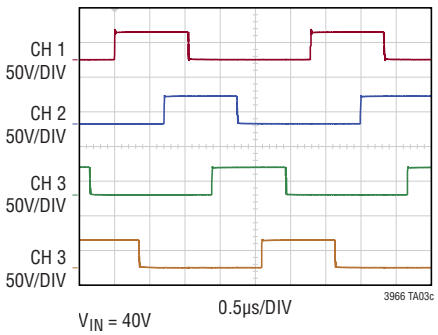


D1, D2, D3, D4: PMEG6020
M1, M2, M3, M4: SI7309
L1, L2, L3, L4: WURTH 744 373 49680

Efficiency

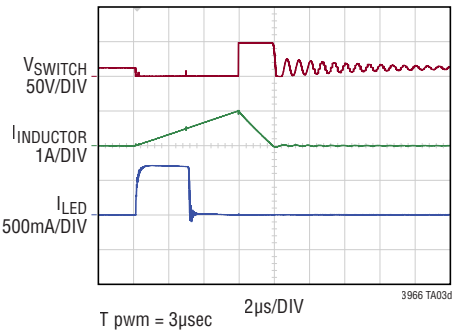


Multiphase



VIN = 40V
VOUT = 23V

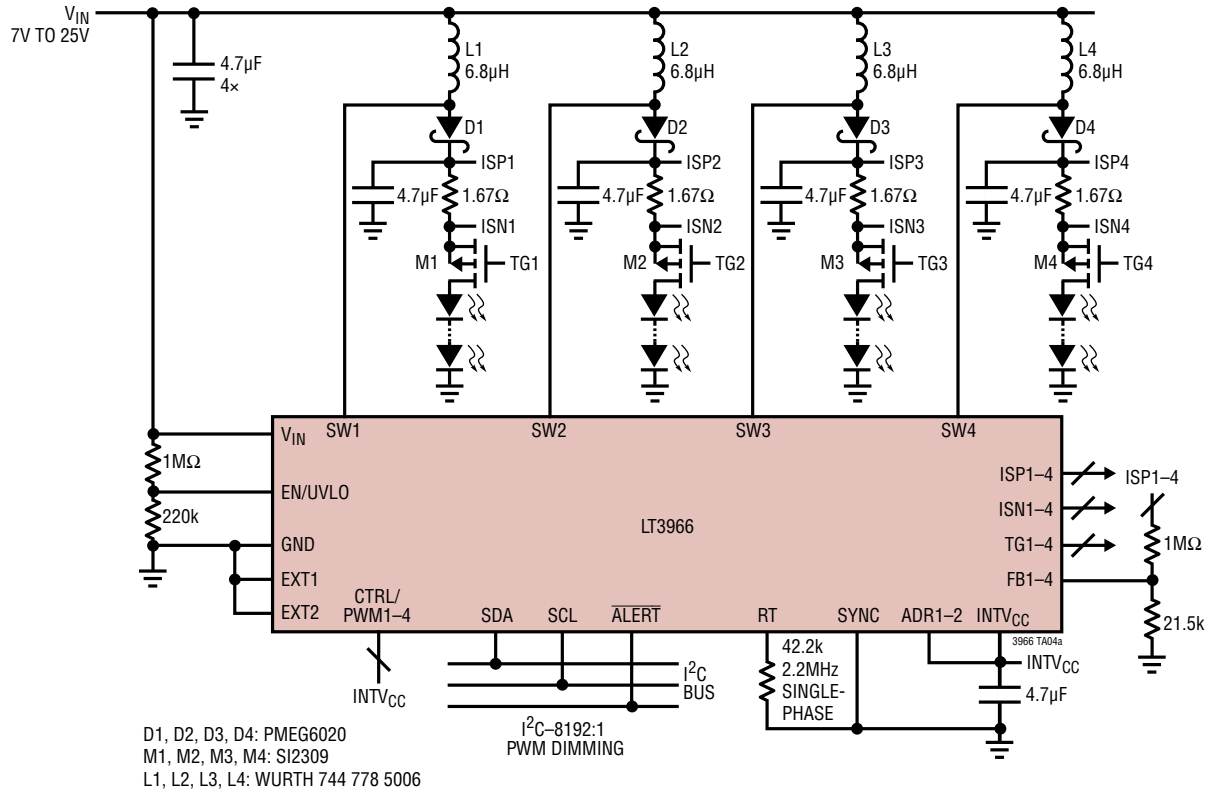
8192:1 Dimming



T pwm = 3µsec
VIN = 48V
VOUT = 34V
ILED = 0.75A

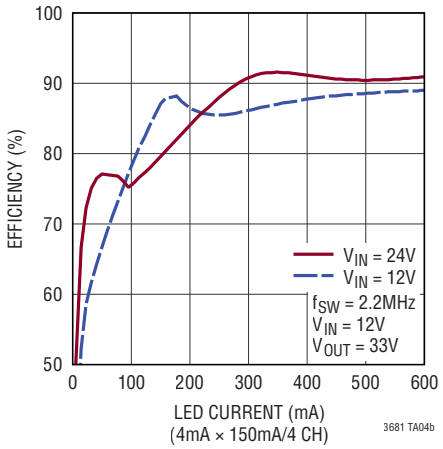
TYPICAL APPLICATIONS

2.2MHz, 4 × 150mA × 12 Boost White LED Backlight with 8192:1 Dimming Ratio

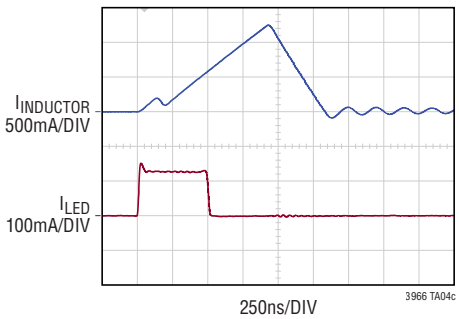


D1, D2, D3, D4: PMEG6020
M1, M2, M3, M4: SI2309
L1, L2, L3, L4: WURTH 744 778 5006

Efficiency



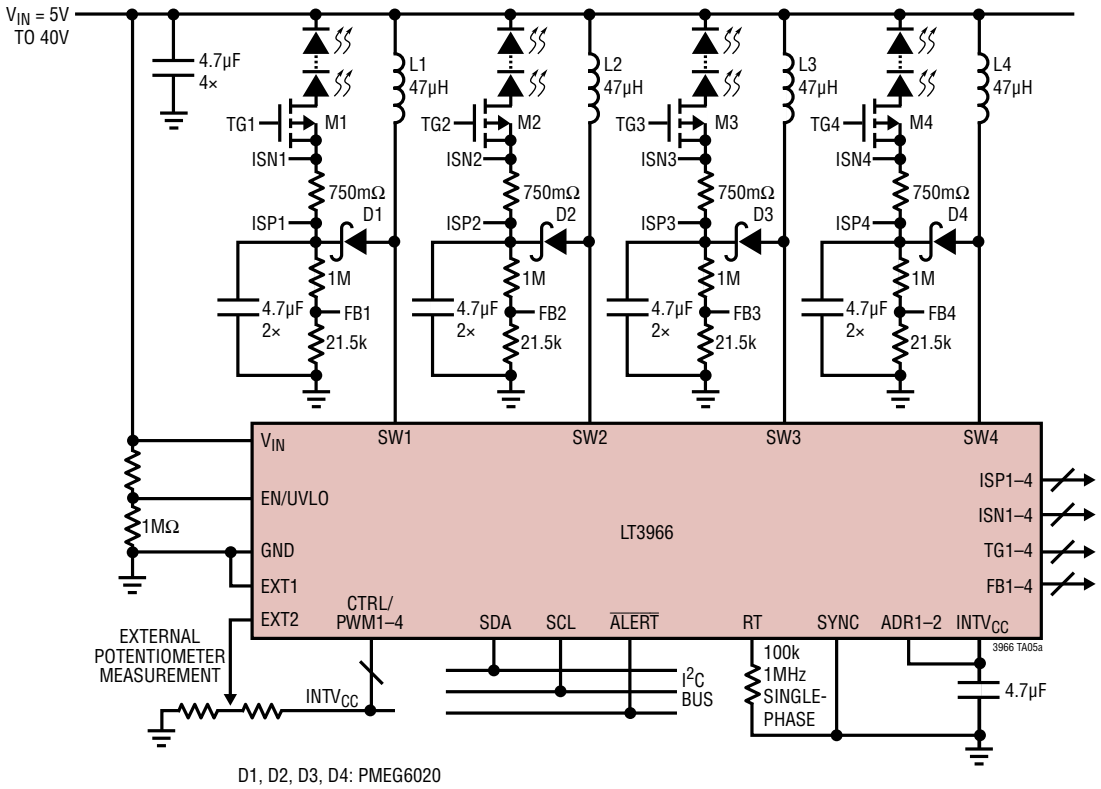
8192:1 Dimming



T pwm = 500nsec
VIN = 12V
VOUT = 33V

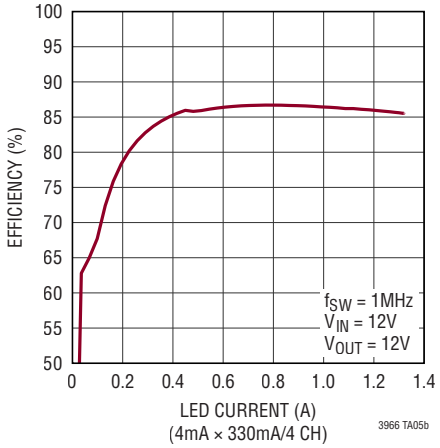
TYPICAL APPLICATIONS

5V to 40V Buck-Boost Mode Driver for 4 Series 330mA LEDs

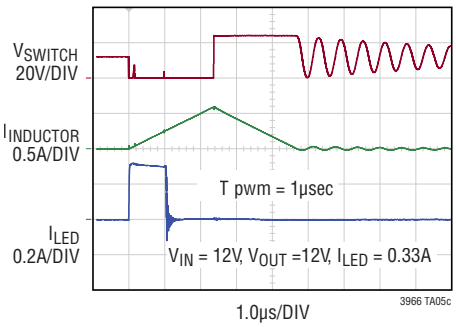


D1, D2, D3, D4: PMEG6020
M1, M2, M3, M4: SI2309
L1, L2, L3, L4: WURTH 744 373 49470

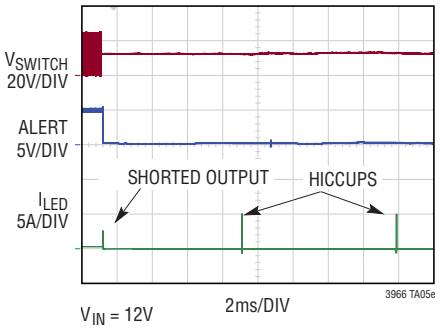
Efficiency



8192:1 Dimming



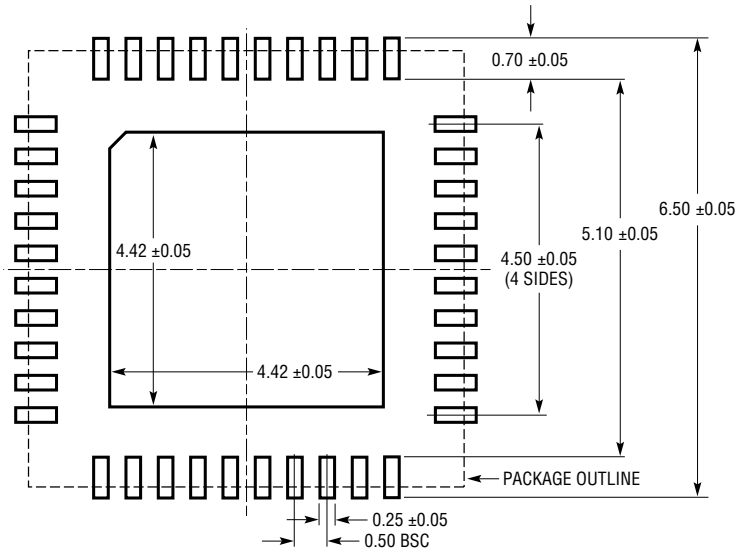
Hiccup Mode



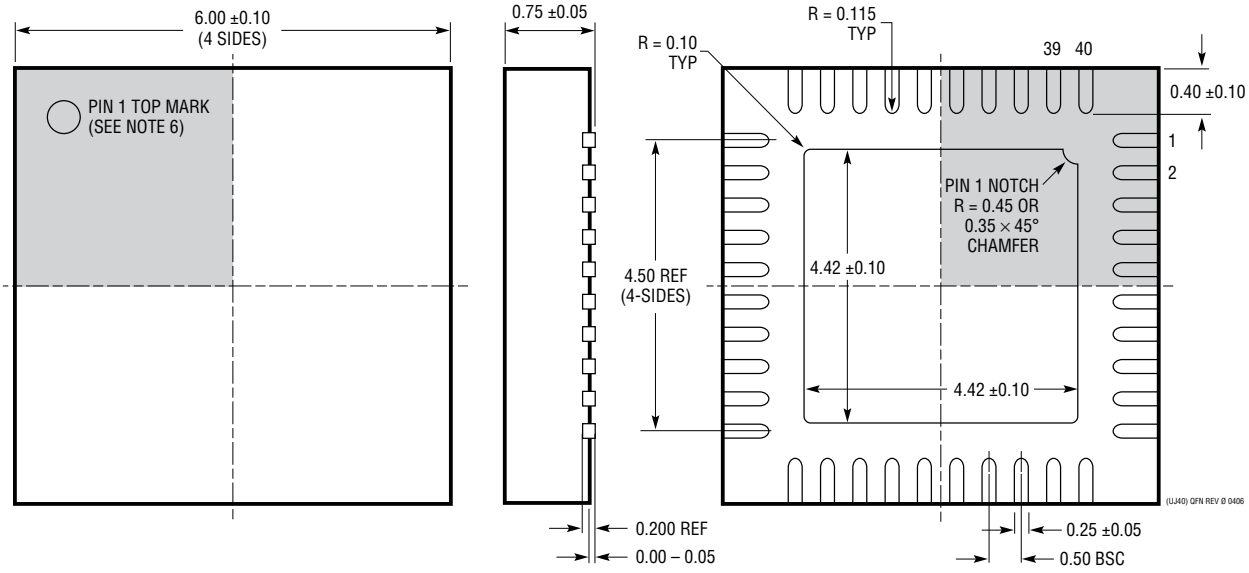
VIN = 12V
VOUT = 12V
ILED = 0.33A

PACKAGE DESCRIPTION

UJ Package
40-Lead Plastic QFN (6mm × 6mm)
(Reference LTC DWG # 05-08-1728 Rev Ø)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING IS A JEDEC PACKAGE OUTLINE VARIATION OF (WJJD-2)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE, IF PRESENT
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE