50A Hot Swap E-Fuse with Guaranteed SOA

FEATURES

- **Allows Safe Board Insertion into Live Backplane**
- **Wide Operating Voltage Range: 2.9V to 15V**
- **Guaranteed Safe Operating Area: 7.5W√s**
- **1.2mΩ MOSFET with Current Sense Element**
- **±4% Current Monitor Output**
- Adjustable Current Limit Threshold
- Temperature Monitor Output
- Overtemperature Protection
- Adjustable Current Limit Timer Before Fault
- Power Good and Fault Outputs
- Adjustable Inrush Current Control
- ±2.5% Accurate Undervoltage and Overvoltage Protection
- Available in a 36-Pin (5mm × 8mm) QFN Package

APPLICATIONS

- High Availability Servers
- Solid State Drives

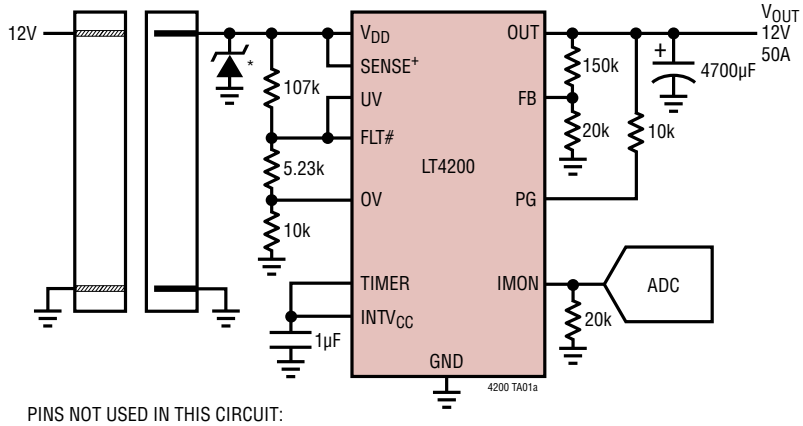
DESCRIPTION

The LT®4200 is an integrated solution for hot swap applications that allows a board to be safely inserted and removed from a live backplane. The part integrates a hot swap controller, power MOSFET and current sense resistor into a single package for small form-factor applications. The MOSFET safe operating area is production tested and guaranteed for the stresses in hot swap applications.

The LT4200 allows 50A of continuous operation at up to 85°C ambient temperature. It provides separate inrush current control and a ±12% accurate 57A current limit with output dependent foldback. The current limit threshold can be adjusted dynamically using the ISET pin. Additional features include a current monitor output for ground referenced current sensing and a MOSFET temperature monitor output. Thermal limit, overvoltage, undervoltage and power good monitoring are also provided.

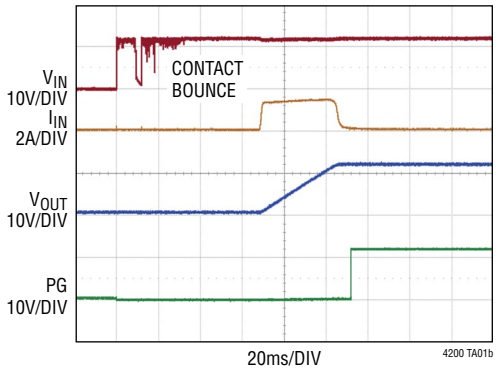
TYPICAL APPLICATION

12V, 50A Card Resident Application with Auto-Retry



PINS NOT USED IN THIS CIRCUIT:
GATE, ISET
*TVS: DIODES INC. SMCJ15A

Power-Up Waveform



ABSOLUTE MAXIMUM RATINGS

(Notes 1 and 2)

Supply Voltage (V_{DD}), SENSE⁻ ..... –0.3V to 28V

Input Voltages

- FB, OV, UV ..... –0.3V to 12V
- TIMER ..... –0.3V to 3.5V
- SENSE⁺ ..... V_{DD} – 0.3V to V_{DD} + 10V

Output Voltages

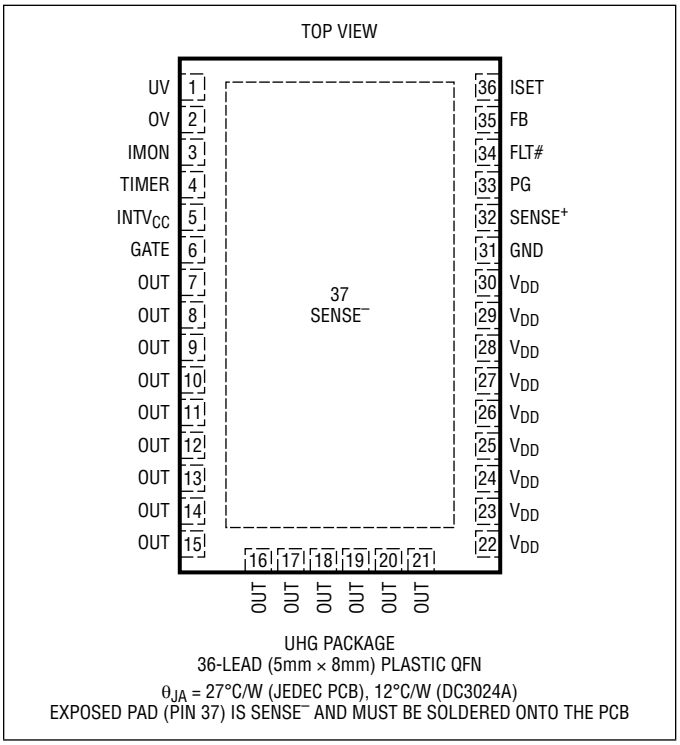
- ISET, IMON ..... –0.3V to 3V
- PG, FLT# ..... –0.3V to 35V
- OUT ..... –0.3V to V_{DD} + 0.3V
- $INTV_{CC}$ ..... –0.3V to 3.5V
- GATE (Note 3) ..... –0.3V to 33V

Operating Junction Temperature Range (Note 4)

- LT4200R ..... –40°C to 150°C

Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



UHG PACKAGE
36-LEAD (5mm × 8mm) PLASTIC QFN

θ_{JA} = 27°C/W (JEDEC PCB), 12°C/W (DC3024A)
EXPOSED PAD (PIN 37) IS SENSE⁻ AND MUST BE SOLDERED ONTO THE PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT4200RUHG#PBF	LT4200RUHG#TRPBF	4200	36-Lead (5mm × 8mm) Plastic QFN	–40°C to 150°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{DD} = 12V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
DC Characteristics							
V_{DD}	Input Supply Range		●	2.9		15	V
I_{DD}	Input Supply Current	MOSFET On, No Load	●		1.6	3	mA
$V_{DD(UVL)}$	Input Supply Undervoltage Lockout	V_{DD} Rising	●	2.63	2.73	2.85	V
I_{OUT}	OUT Leakage Current	V_{OUT} = V_{GATE} = 0V, V_{DD} = 15V,	●	–700		700	µA
	OUT Operating Current	V_{OUT} = V_{GATE} = 12V, V_{DD} = 12V	●	1	2	4	µA
$dV_{GATE/dt}$	OUT Turn-On Ramp Rate	GATE Open	●	0.15	0.35	0.6	V/ms
R_{ON}	MOSFET On-Resistance	Including Current Sense Resistor	●	0.6	1.2	2.2	mΩ
$I_{LIM(TH)}$	Current Limit Threshold	V_{FB} = 1.35V, ISET Open V_{FB} = 0V, ISET Open V_{FB} = 1.35V, R_{SET} = 20k	● ● ●	50.2 4.6 23	57 6.8 28	63.8 9 33	A A A
SOA	MOSFET Safe Operating Area	12.6V, 6.8A Folded Back, 7.5W$\sqrt{s}$ (Note 5)		7.7			ms
Inputs							
I_{IN}	OV, UV, FB Input Current	V = 1.2V	●		0	±1	µA
$I_{SENSE^+(IN)}$	SENSE+ Input Current	V_{SENSE^+} = 12V	●		4	±10	µA
V_{TH}	OV, UV, FB Threshold Voltage	V_{PIN} Rising	●	1.205	1.235	1.265	V
$\Delta V_{OV(HYST)}$	OV Hysteresis		●	10	20	30	mV
$\Delta V_{UV(HYST)}$	UV Hysteresis		●	50	80	110	mV
$V_{UV(RTH)}$	UV Reset Threshold Voltage	V_{UV} Falling	●	0.55	0.62	0.7	V
$\Delta V_{FB(HYST)}$	FB Power Good Hysteresis		●	10	20	30	mV
R_{ISET}	ISET Internal Resistor		●	19	20	21	kΩ
Outputs							
V_{INTVCC}	$INTV_{CC}$ Output Voltage	V_{DD} = 5V,15V, I_{LOAD} = 0mA, –10mA	●	2.7	3.1	3.4	V
V_{OL}	PG, FLT# Output Low Voltage	I = 2mA	●		0.4	0.8	V
I_{OH}	PG, FLT# Input Leakage Current	V = 30V	●		0	±10	µA
$V_{TIMER(H)}$	TIMER High Threshold	V_{TIMER} Rising	●	1.2	1.235	1.28	V
$V_{TIMER(L)}$	TIMER Low Threshold	V_{TIMER} Falling	●	0.1	0.21	0.3	V
$I_{TIMER(UP)}$	TIMER Pull-Up Current	V_{TIMER} = 0V	●	–80	–100	–120	µA
$I_{TIMER(DN)}$	TIMER Pull-Down Current	V_{TIMER} = 1.2V	●	1.4	2	2.6	µA
$I_{TIMER(RATIO)}$	TIMER Current Ratio ITIMER(DN)/ITIMER(UP)		●	1.6	2	2.7	%
A_{IMON}	IMON Current Gain	20A to 50A, T_J = 0°C to 125°C		1.92	2	2.08	µA/A
BW_{IMON}	IMON Bandwidth				250		kHz
$I_{OFF(IMON)}$	IMON Offset Current	I_{OUT} = 1.5A, T_J = 0°C to 125°C				±3	µA
$I_{GATE(UP)}$	Gate Pull-Up Current	Gate Drive On, V_{GATE} = V_{OUT} = 12V	●	–18	–24	–29	µA
$I_{GATE(DN)}$	Gate Pull-Down Current	Gate Drive Off, V_{GATE} = 22V, V_{OUT} = 12V	●	165		500	µA
$I_{GATE(FST)}$	Gate Fast Pull-Down Current	Fast Turn Off, V_{GATE} = 22V, V_{OUT} = 12V			140		mA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{DD} = 12V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
AC Characteristics							
$t_{PHL(GATE)}$	Input High (OV), Input Low (UV) to GATE Low Propagation Delay	V_{GATE} < 21.8V Falling	●		8	25	µs
$t_{PHL(ILIM)}$	Short-Circuit to GATE Low	V_{FB} = 0, Step SENSE$^+$ – SENSE$^-$ to 50mV, V_{GATE} < 15V Falling	●		1	5	µs
$t_{D(ON)}$	Turn-On Delay	Step V_{UV} to 2V, V_{GATE} > 13V	●	24	48	72	ms
$t_{D(FAULT)}$	UV Low to Clear Fault Latch Delay				1		µs
$t_{D(CB)}$	Circuit Breaker Filter Delay Time (Internal)	V_{FB} = 0, Step SENSE$^+$ – SENSE$^-$ to 50mV	●	0.25	0.45	0.7	ms
$t_{D(COOL\_DOWN)}$	Cool Down Delay (Internal)	TIMER = $INTV_{CC}$	●	600	900	1200	ms

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All currents into pins are positive; all voltages are referenced to GND unless otherwise specified.

Note 3: An internal clamp limits the GATE pin to a minimum of 10V above OUT. Driving this pin to voltages beyond the clamp may damage the device.

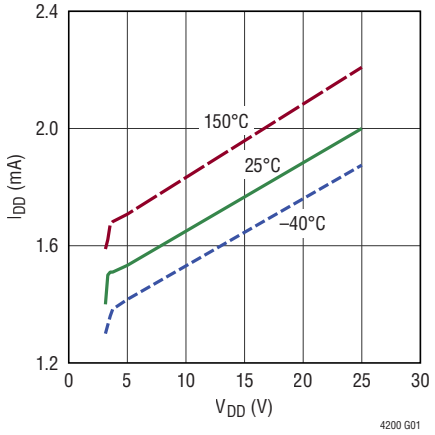
Note 4: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 150°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 5: SOA is tested with current limit folded back, V_{DD} = 12V + 5% or 12.6V and output shorted to GND. This condition is near the Spirito region of the SOA curve. See the SOA Curve in the Typical Performance Characteristic section.

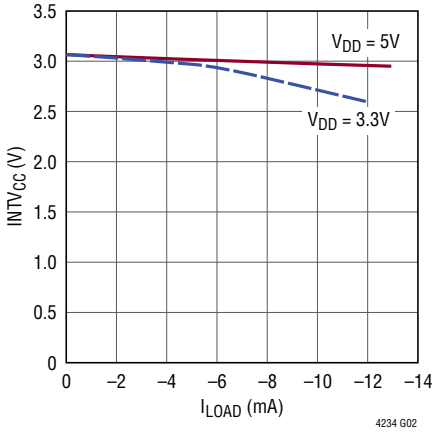
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{DD} = 12V unless otherwise noted.

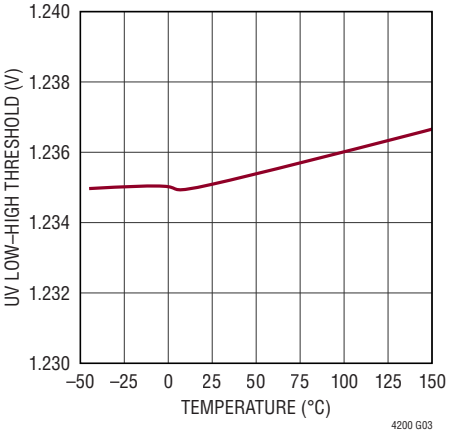
I_{DD} vs V_{DD}



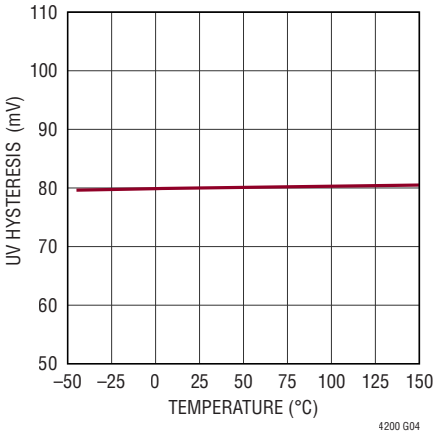
$INTV_{CC}$ Load Regulation



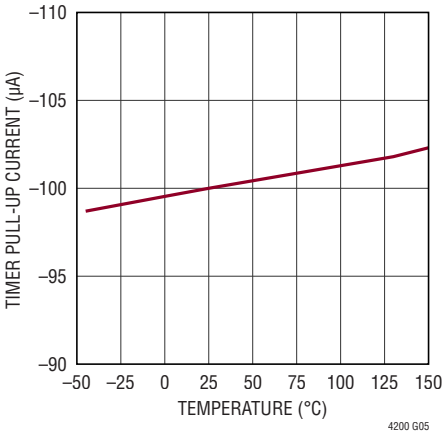
UV Low-High Threshold vs Temperature



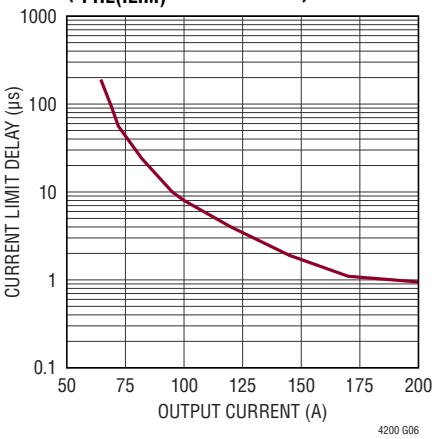
UV Hysteresis vs Temperature



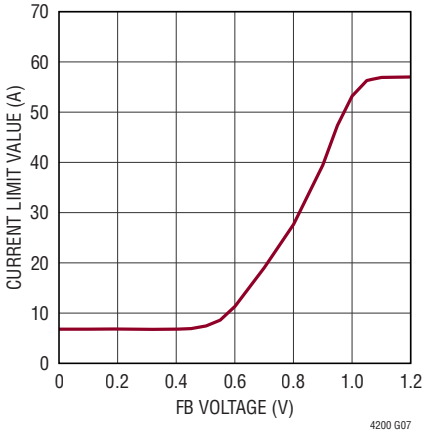
Timer Pull-Up Current vs Temperature



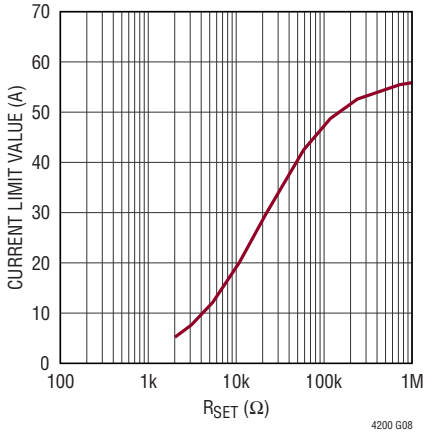
Current Limit Delay ($t_{PHL(ILIM)}$ vs Overdrive)



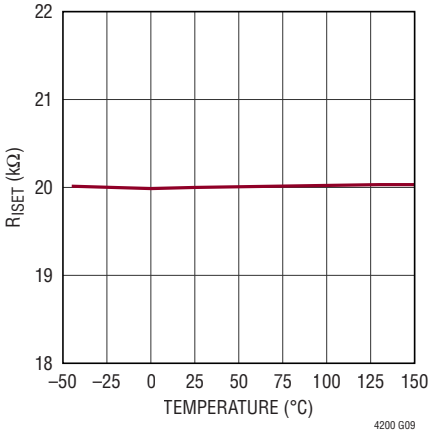
Current Limit Threshold Foldback



Current Limit Adjustment (I_{OUT} vs R_{SET})



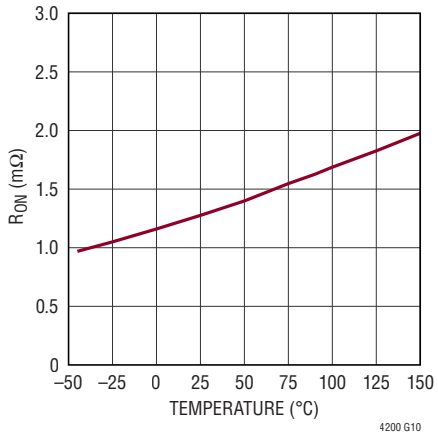
R_{ISET} vs Temperature



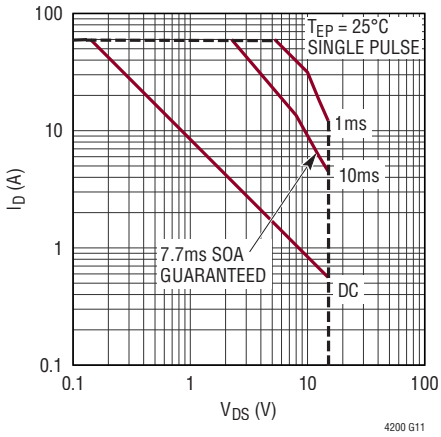
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{DD} = 12V unless otherwise noted.

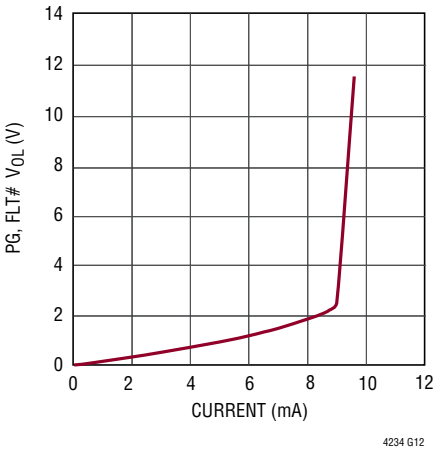
R_{ON} vs Temperature



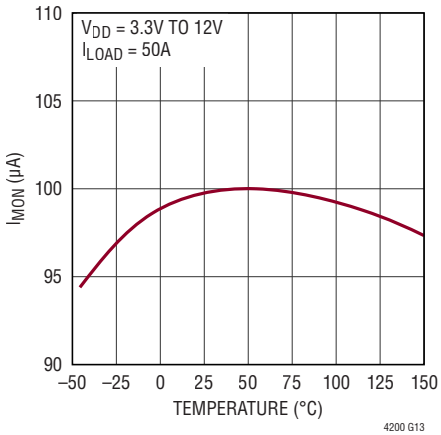
Guaranteed MOSFET SOA Curve



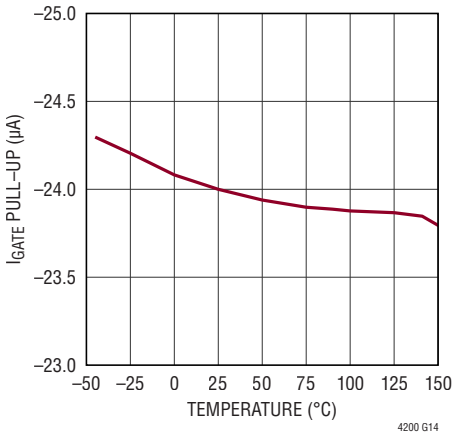
PG, FLT# V_{OUT} Low vs I_{LOAD}



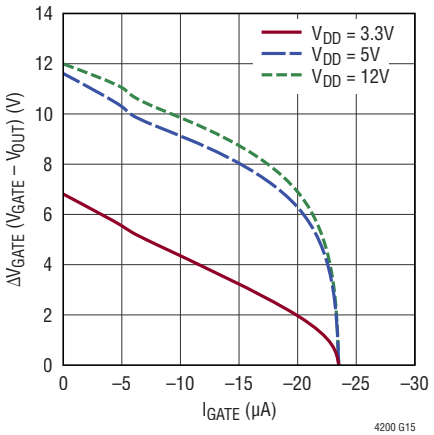
IMON vs Temperature



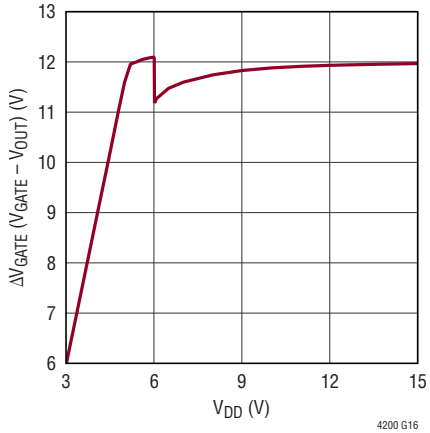
GATE Pull-Up Current vs Temperature



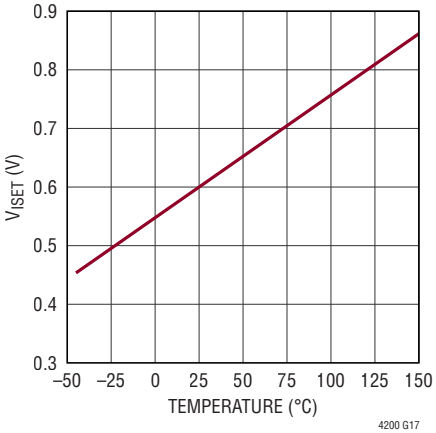
Gate Drive vs GATE Pull-Up Current



Gate Drive vs V_{DD}



V_{ISET} vs Temperature



PIN FUNCTIONS

UV (Pin 1): Undervoltage Comparator Input. Connect this pin to an external resistive divider from V_{DD}. If the UV pin voltage falls below 1.15V, an undervoltage is detected and the switch turns off. Pulling this pin below 0.62V resets the overcurrent fault and allows the switch to turn back on (see Application Information section for details). If overcurrent auto-retry is desired, then tie UV to the FLT# pin. Tie UV to $INTV_{CC}$ if unused.

OV (Pin 2): Overvoltage Comparator Input. Connect this pin to an external resistive divider from V_{DD}. If the voltage at this pin rises above 1.235V, an overvoltage is detected, and the switch turns off. Tie to GND if unused.

IMON (Pin 3): Current Monitor Output. The current in the internal MOSFET switch is divided by 500,000 and sourced from this pin. Placing a 20k resistor on this pin allows a 0V to 2V voltage swing when current ranges from 0A to 50A.

TIMER (Pin 4): Current Limit Timer Input. Connect a capacitor between this pin and ground to set a 12ms/µF duration for current limit before the switch is turned off. If the UV pin is toggled low while the MOSFET switch is off, the switch will turn on again following cool down time of 4.14s/µF duration. Tie this pin to $INTV_{CC}$ for a fixed 0.5ms overcurrent delay and 900ms cool down time.

$INTV_{CC}$ (Pin 5): Internal 3.1V Supply Decoupling Output. This pin must have a 1µF or larger bypass capacitor. Overloading this pin can disrupt internal operation.

GATE (Pin 6): Gate Drive for Internal N-Channel MOSFET. An internal 24µA current source charges the gate of the N-channel MOSFET. At start-up, the GATE pin ramps up at a 0.35V/ms rate determined by internal circuitry. During an undervoltage or overvoltage condition, a 250µA pull-down current turns the MOSFET off. During a short-circuit or undervoltage lockout condition, a 140mA pull-down current source between GATE and OUT is activated.

OUT (Pins 7–21): Output of Internal MOSFET Switch. Connect this pin directly to the load.

V_{DD} (Pins 22–30): Supply Voltage and Current Sense Input. These pins must be soldered to input power. V_{DD} has an undervoltage lockout threshold of 2.73V.

GND (Pin 31): Device Ground.

$SENSE^-$ (Pin 32): Current Sense Node and MOSFET Drain. The exposed pad on the UHG package is connected to $SENSE^-$ and should be soldered to an electrically isolated printed circuit board trace to properly transfer the heat out of the package.

$SENSE^+$ (Pin 32): Current Limit and Current Monitor Amplifier Input. The current limit circuit controls the GATE pin to limit the voltage between the $SENSE^+$ and $SENSE^-$ pin to 17mV (57A) or less depending on the voltage at the FB pin and ISET. This pin must be connected to V_{DD} pin (connect Pin 32 to Pin 26).

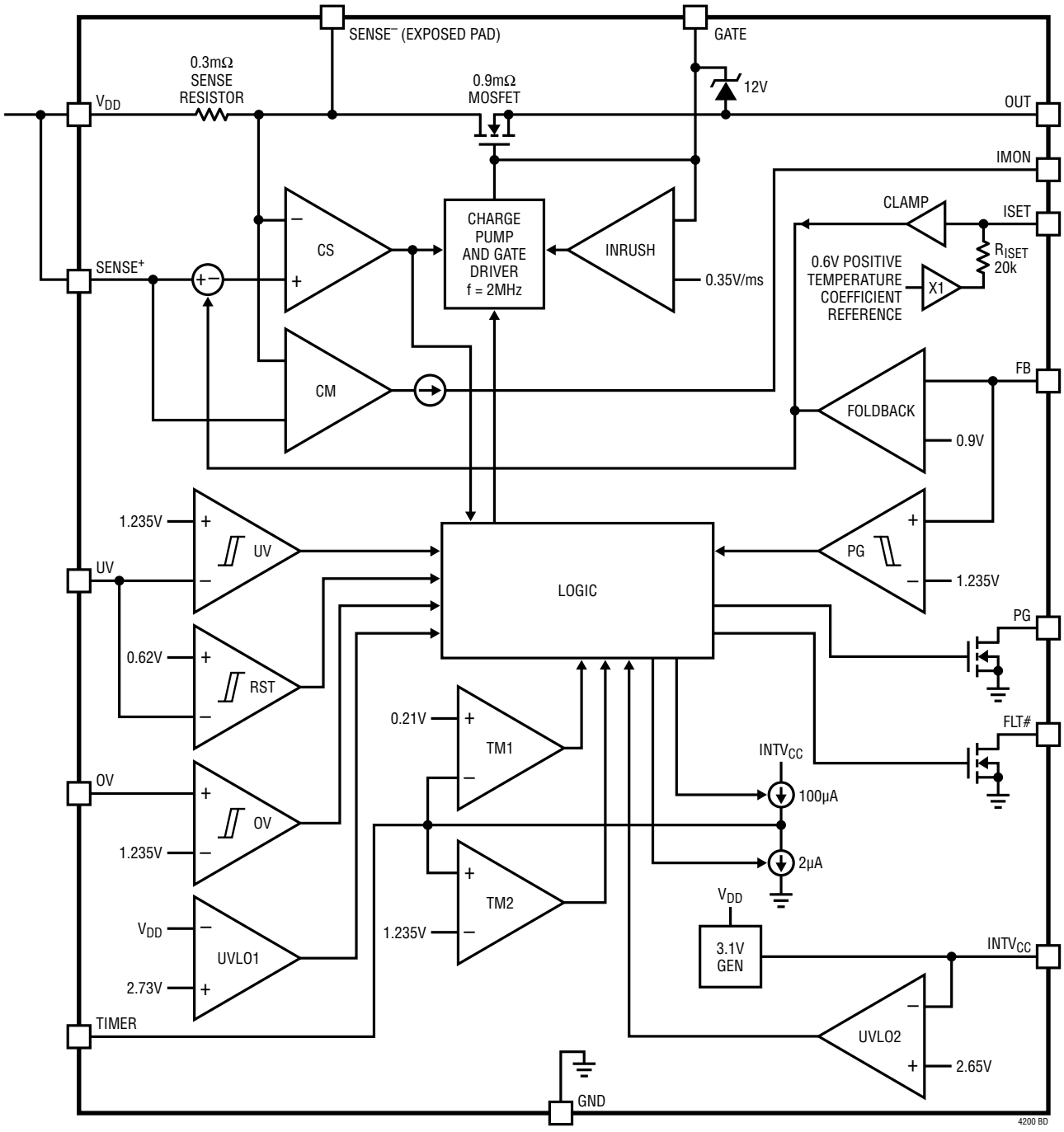
PG (Pin 33): Power Good Indicator. Open-drain output pulls low when the FB pin drops below 1.21V indicating the power is bad. If the voltage at FB rises above 1.235V and the GATE-to-OUT voltage exceeds 4.2V, the open-drain pull-down releases the PG pin to go high.

FLT# (Pin 34): Overcurrent Fault Indicator. Open-drain output pulls low when an overcurrent fault has occurred and the circuit breaker trips. For overcurrent auto-retry tie FLT# to UV pin (see Applications Information section for details).

FB (Pin 35): Foldback and Power Good Input. Connect this pin to an external resistive divider from OUT. If the voltage falls below 0.9V, the current limit is reduced using a foldback profile (see the Typical Performance Characteristics section). If the voltage falls below 1.21V, the PG pin will pull low to indicate the power is bad.

ISET (Pin 36): Current Limit Adjustment Pin. For 57A current limit value, open this pin. This pin is driven by a 20k resistor in series with a voltage source. The pin voltage is used to generate the current limit threshold. The internal 20k resistor (R_{ISET}) and an external resistor (R_{SET}) between ISET and ground create an attenuator that lowers the current limit value. Due to circuit tolerance R_{SET} should not be less than 2k. In order to match the temperature variation of the sense resistor, the voltage on this pin increases at the same rate as the sense resistance increases. Therefore the voltage at ISET pin is made proportional to temperature of the MOSFET switch.

FUNCTIONAL DIAGRAM



OPERATION

The Functional Diagram displays the main circuits of the device. The LT4200 is designed to turn a board's supply voltage on and off in a controlled manner allowing the board to be safely inserted and removed from a live backplane. The LT4200 includes a 0.9mΩ MOSFET and a 0.3mΩ current sense resistor. During normal operation, the charge pump and gate driver turn on the pass MOSFET's gate to provide power to the load. The inrush current control is accomplished by the INRUSH circuit. This circuit limits the GATE ramp rate to 0.35V/ms and hence controls the voltage ramp rate of the output capacitor.

The current sense (CS) amplifier monitors the load current by using the voltage sensed across the current sense resistor. The CS amplifier limits the current in the load by reducing the GATE-to-OUT voltage in an active control loop. It is simple to adjust the current limit threshold using the current limit adjustment (ISET) pin. This allows a different threshold during other times such as start-up. Note there must be a connection between $SENSE^+$ to V_{DD} (Pin 32 to Pin 26) in order to monitor current.

A short circuit on the output to ground causes significant power dissipation during active current limiting. To limit this power dissipation, the foldback amplifier reduces the current limit value from 57A to 6.8A in a linear manner as the FB pin drops below 0.9V (see the Typical Performance Characteristics).

If an overcurrent condition persists, the TIMER pin ramps up with a 100µA current source until the pin voltage exceeds 1.235V (comparator TM2). This indicates to the logic that it is time to turn off the pass MOSFET to prevent overheating. At this point the TIMER pin ramps down using the 2µA current source until the voltage drops below 0.21V (Comparator TM1) which completes one timer cycle. After eight TIMER pin cycles (ramping to 1.235V and then below 0.21V), the logic starts the 48ms debounce time. At this point, the pass transistor has cooled and it is safe to turn it on again. It is suitable in many applications to use an internal 0.5ms overcurrent timer with a 900ms cool down by tying the TIMER pin to $INTV_{CC}$. Latchoff is the normal operating condition following overcurrent turnoff. Retry is initiated by pulling the UV pin low for a minimum of 1µs then high. Auto-retry is implemented by tying the FLT# to the UV pin.

The output voltage is monitored using the FB pin and the PG comparator to determine if power is available for the load. The power good condition is signaled by the PG pin using an open-drain pull-down transistor.

The Functional Diagram shows the monitoring blocks of the LT4200. The two comparators on the left side include the UV and OV comparators. These comparators are used to determine if the external conditions, typically input voltage, are valid prior to turning on the MOSFET. But first, the undervoltage lockout circuits UVLO1 and UVLO2 must validate the input supply and the internally generated 3.1V supply ($INTV_{CC}$), generating the power-up initialization to the logic circuits. If the external conditions remain valid for 48ms, the MOSFET is allowed to turn on.

Other features include MOSFET current and temperature monitoring. The current monitor (CM) outputs a current proportional to the sense resistor current. This current can drive an external resistor or other circuits for monitoring purposes. A voltage proportional to the MOSFET temperature is output to the ISET pin. The MOSFET is protected by a thermal shutdown circuit.

APPLICATIONS INFORMATION

The typical LT4200 application is in a high availability system that uses a positive voltage supply to distribute power to individual cards. The application circuit is shown in Figure 1. External component selection is discussed in detail in the following sections.

Turn-On Sequence

Several conditions must be present before the internal pass MOSFET can be turned on. First, the supply V_{DD} must exceed its undervoltage lockout level. Next, the internally generated supply $INTV_{CC}$ must cross its 2.65V undervoltage threshold. This generates a 25µs power-on-reset pulse which clears the fault register and initializes internal latches.

After the power-on-reset pulse, the UV and OV pins must indicate that the input voltage is within the acceptable range. All of these conditions must be satisfied for a duration of 48ms to ensure that any contact bounce during the insertion has ended.

The inrush current into the load capacitor, C_L, is controlled by limiting the dv/dt on the MOSFET's GATE pin. The same dv/dt will be generated on the OUTPUT pin. Figure 2 illustrate the turn-on ramp rate without C_{GATE}. This internal gate slope of 0.35V/ms will result in an inrush current defined by Equation 1.

$$I_{INRUSH} = C_L \bullet 0.35[V/ms] \quad (1)$$

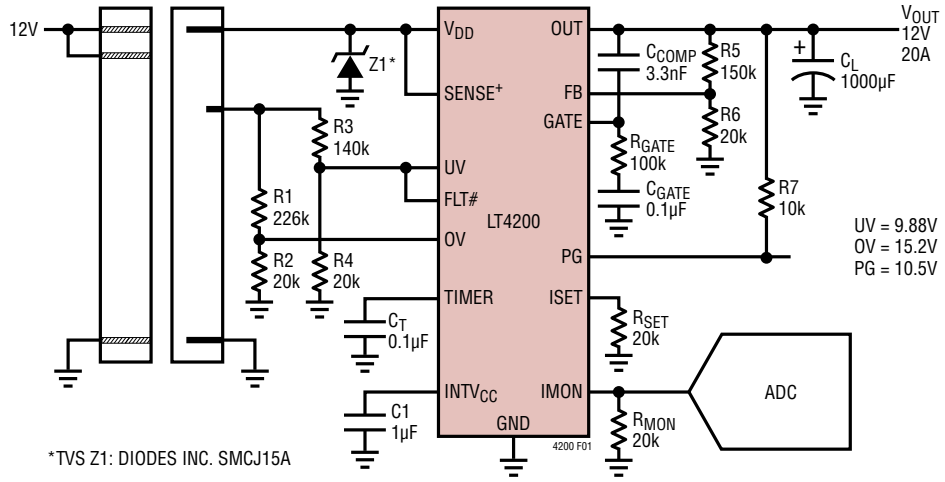


Figure 1. 20A, 12V Card Resident Application, Auto-Retry

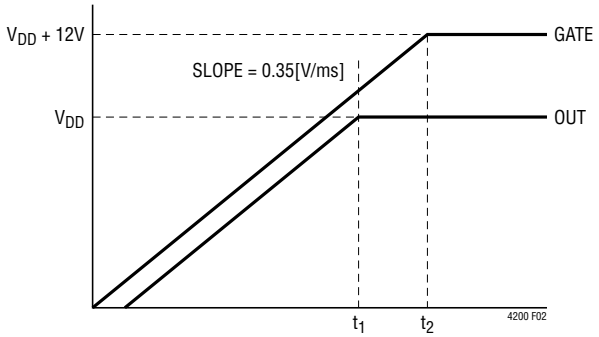


Figure 2. Supply Turn-On without C_{GATE}

APPLICATIONS INFORMATION

This gate slope is designed to charge up a 1000µF capacitor to 12V in 34ms, with an inrush current of 350mA. This allows the inrush current to stay under the folded back current limit threshold (6.8A) for capacitors less than 8mF. The average power dissipation of 12V at 350mA for 34ms amounts to 0.387W$\sqrt{s}$, which is safely below the LT4200 P$\sqrt{t}$ spec of 7.5W$\sqrt{s}$.

The default configuration results in an inrush current that stays under the folded back current limit threshold (6.8A) for charging capacitors less than 7667µF. If the load capacitor, C_L, is greater than 7667µF or a reduced inrush current is desired, an RC network can be added to the GATE pin. This is illustrated in Figure 1. With the RC network the inrush current is defined by Equation 2. The resistor should be 100k. A 3.3nF, C_{COMP}, is necessary to compensate the current limit.

$$I_{INRUSH} = \frac{C_L}{C_{GATE}} \bullet 24\mu A \quad (2)$$

When the GATE voltage reaches the MOSFET threshold voltage, the switch begins to turn on and the OUT voltage follows the GATE voltage as it increases. Once OUT reaches V_{DD}, the GATE will ramp up until clamped by the 12V Zener between GATE and OUT.

As the OUT voltage rises, so will the FB pin which is monitoring it. Once the FB pin crosses its 1.235V threshold and the GATE to OUT voltage exceeds 4.2V, the PG pin will cease to pull low and indicate that the power is good.

Parasitic MOSFET Oscillation

When the N-channel MOSFET ramps up the output during power-up it operates as a source follower. The source follower configuration may self-oscillate in the range of 25kHz to 300kHz when the load capacitance is less than 10µF, especially if the wiring inductance from the supply to V_{DD} pin is greater than 3µH. The possibility of oscillations will increase as the load current (during power-up) increases. There are two ways to prevent this type of oscillation. The simplest way is to avoid load capacitances below 10µF. For wiring inductances larger than 20µH, the minimum load capacitance may extend to 100µF.

A second choice is to connect an external gate capacitor $C_P > 1.5$nF as shown in Figure 3.

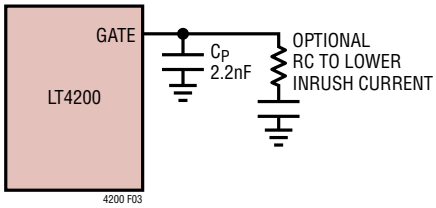


Figure 3. Compensation for Small C_{LOAD}

Turn-Off Sequence

The switch can be turned off by a variety of conditions. A normal turn-off is initiated when the UV pin goes below its 1.235V threshold. Additionally, several fault conditions will turn off the switch. These include an input overvoltage (OV pin), overcurrent circuit breaker ($SENSE^+$ pin) or overtemperature. Normally, the switch is turned off with a 250µA current pulling down the GATE pin to ground. With the switch turned off, the OUT voltage drops which pulls the FB pin below its threshold. The PG then pulls low to indicate output power is no longer good.

If V_{DD} drops below 2.65V for greater than 5µs or $INTV_{CC}$ drops below 2.5V for greater than 1µs, a fast shut down of the switch is initiated. The GATE is pulled down with a 140mA current to the OUT pin.

Overcurrent Fault

The LT4200 features an adjustable current limit with foldback that protects against short circuits and excessive load current. To protect against excessive power dissipation in the switch during active current limit, the available current is reduced as a function of the output voltage sensed by the FB pin. A graph in the Typical Performance Characteristics curves shows the current limit threshold foldback.

An overcurrent fault occurs when the current limit circuitry has been engaged for longer than the timeout delay set by the TIMER. Current limiting begins when the MOSFET current reaches 6.8A to 57A (depending on the foldback). The GATE pin is then brought down with a

APPLICATIONS INFORMATION

140mA GATE-to-OUT current. The voltage on the GATE is regulated in order to limit the current to 57A. At this point, a circuit breaker time delay starts by charging the external timing capacitor with a 100µA pull-up current from the TIMER pin. If the TIMER pin reaches its 1.235V threshold, the internal switch turns off (with a 250µA current from GATE to ground). Included in the Typical Performance Characteristics curves is a graph of the safe operating area for the MOSFET. From this graph, one can determine the MOSFET's maximum time in current limit for a given output power.

Tying the TIMER pin to $INTV_{CC}$ will force the part to use the internally generated (circuit breaker) delay of 0.5ms. In either case the FLT# pin is pulled low to indicate an overcurrent fault has turned off the pass MOSFET. For a given circuit breaker time delay, the equation for setting the timing capacitor's value is given by Equation 3.

$$C_T = t_{CB} \bullet 0.083[\mu F/ms] \quad (3)$$

After the switch is turned off, the TIMER pin begins discharging the timing capacitor with a 2µA pull-down current. When the TIMER pin reaches its 0.21V threshold, it completes one timer cycle. After eight TIMER pin cycles (ramping to 1.235V and then below 0.21V) plus the 48ms debounce time, the switch is allowed to turn on again if the overcurrent fault latch has been cleared. Bringing the UV pin below 0.6V for a minimum of 1µs and then high will clear the fault latch. If the TIMER pin is tied to $INTV_{CC}$ then the switch is allowed to turn on again (after an internal 900ms cool down time plus the 48ms debounce time), if the overcurrent fault latch is cleared.

Tying the FLT# pin to the UV pin allows the part to self-clear the fault and turn the MOSFET on as soon as TIMER pin has ramped below 0.21V for the eighth time followed by the 48ms debounce time. In this auto-retry mode, the LT4200 repeatedly tries to turn on after an overcurrent at a period determined by the capacitor on the TIMER pin. The auto retry mode also functions when the TIMER pin is tied to $INTV_{CC}$.

The waveform in Figure 4 shows how the output latches off following a short-circuit. The current in the MOSFET is 6.8A as the TIMER pin ramps up.

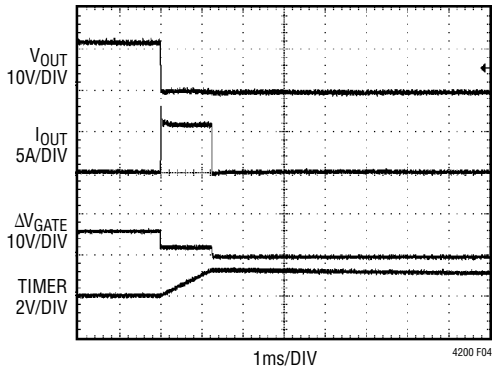


Figure 4. Short-Circuit Waveform

Current Limit Adjustment

The default value of the active current limit is 57A. The current limit threshold can be adjusted lower by placing a resistor between the ISET pin and ground. As shown in the Functional Diagram the voltage at the ISET pin (via the clamp circuit) sets the CS amplifier's built-in offset voltage. This offset voltage directly determines the active current limit value. With the ISET pin open, the voltage at the ISET pin is determined by a positive temperature coefficient reference. This voltage is set to 0.618V which corresponds to a 57A current limit at room temperature.

An external resistor R_{SET} placed between the ISET pin and ground forms a resistive divider with the internal 20k R_{ISET} sourcing resistor. The divider acts to lower the voltage at the ISET pin and therefore lower the current limit threshold. The overall current limit threshold precision is reduced to ±15% when using a 20k resistor to halve the threshold.

The R_{SET} resistor for a desired current limit level can be calculated using the Equation 4.

$$R_{SET} = \frac{20k\Omega}{\left(\frac{57}{I_{LIM}} - 1\right)} \quad (4)$$

where:
R_{SET} = value of the resistor in Ω
I_{LIM} = Current Limit in A, $5.2 < I_{LIM} < 57$

Using a switch (connected to ground) in series with R_{SET} allows the active current limit to change only when the switch is closed. This feature can be used to program a

APPLICATIONS INFORMATION

reduced running current while the maximum available current limit is used at start-up.

Monitor MOSFET Temperature

The voltage at the ISET pin increases linearly with increasing temperature. The temperature profile of the ISET pin is shown in the Typical Performance Characteristics section. Using a comparator or ADC to measure the ISET voltage provides an accurate indication of the MOSFET temperature. The I_{SET} voltage follows Equation 5.

$$V_{ISET} = \frac{R_{SET}}{R_{SET} + R_{ISET}} \bullet (T + 273°C) \bullet 2.093\ [mV/°C] \quad (5)$$

The MOSFET temperature is calculated using R_{ISET} of 20k (Equation 6).

$$T = \frac{(R_{SET} + 20k) \bullet V_{ISET}}{R_{SET} \bullet 2.093\ [mV/°C]} - 273°C \quad (6)$$

When R_{SET} is not present, T is given by Equation 7.

$$T = \frac{V_{ISET}}{2.093\ [mV/°C]} - 273°C \quad (7)$$

There is an overtemperature circuit in the LT4200 that monitors an internal voltage similar to the ISET pin voltage. When the die temperature exceeds 155°C the circuit turns off the MOSFET until the temperature drops to 135°C.

Monitor MOSFET Current

The current in the MOSFET passes through an internal 0.3mΩ sense resistor. The voltage on the sense resistor is converted to a current that is sourced out of the IMON pin. The gain of I_{SENSE} amplifier is 2µA/A referenced from the MOSFET current. This output current can be converted to a voltage using an external resistor to drive a comparator or ADC. The voltage compliance for the IMON pin is from 0V to $INTV_{CC}$ – 0.7V.

A microcontroller with a built-in comparator can build a simple integrating single-slope ADC by resetting a capacitor that is charged with this current. When the capacitor voltage trips the comparator and the capacitor is reset, a timer is started. The time between resets will indicate the MOSFET current.

Monitor OV and UV Faults

Protecting the load from an overvoltage condition is the main function of the OV pin. In Figure 1 an external resistive divider (driving the OV pin) connects to a comparator to turn off the MOSFET when the V_{DD} voltage exceeds 15.2V. If the V_{DD} pin subsequently falls back below 14.9V, the switch will be allowed to turn on immediately. In the LT4200 the OV pin threshold is 1.235V when rising, and 1.215V when falling out of overvoltage.

The UV pin functions as an undervoltage protection pin or as an "ON" pin. In the Figure 1 application the MOSFET turns off when V_{DD} falls below 9.23V. If the V_{DD} pin subsequently rises above 9.88V for 48ms, the switch will be allowed to turn on again. The LT4200 UV turn-on/off threshold are 1.235V (rising) and 1.155V (falling).

In the case of an undervoltage or overvoltage, the MOSFET turns off and there is indication on the PG status pin. When the overvoltage is removed, the MOSFET's gate ramps up immediately at the rate determined by the INRUSH circuit.

Power Good Indication

In addition to setting the foldback current limit threshold, the FB pin is used to determine a power good condition. The Figure 1 application uses an external resistive divider on the OUT pin to drive the FB pin. On the LT4200 the PG comparator drives high when the FB pin rises above 1.235V and low when it falls below 1.215V.

Once the PG comparator is high the GATE pin voltage is monitored with respect to the OUT pin. Once the GATE minus OUT voltage exceeds 4.2V the PG pin goes high. This indicates to the system that it is safe to load the OUT pin while the MOSFET is completely turned "on". The PG pin goes low when the GATE is commanded off (using the UV, OV or $SENSE^+$ pins) or when the PG comparator drives low.

APPLICATIONS INFORMATION

Design Example

Consider the following design example (Figure 5): T_A = 25°C, V_{IN} = 12V, I_{MAX} = 50A. I_{INRUSH} = 700mA, C_L = 2000µF, V_{UV} = 9.88V, V_{OV} = 15.2V, V_{PG} = 10.5V. A current limit fault triggers an automatic restart of the power-up sequence.

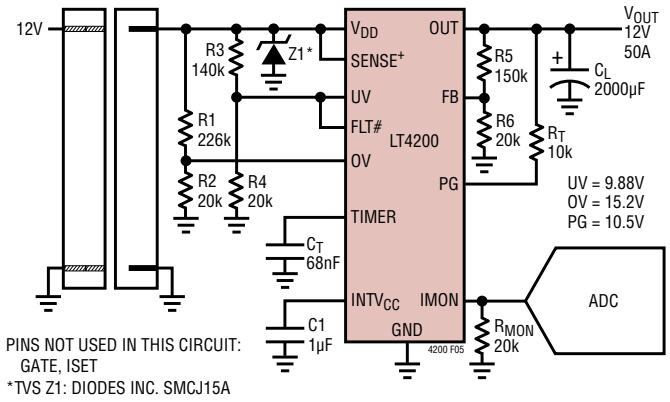


Figure 5. 50A, 12V Card Resident Application

The inrush current is defined by the current required to charge the output capacitor using the fixed 0.35V/ms GATE charge up rate. The inrush current is defined by Equation 8.

$$I_{INRUSH} = C_L \bullet \left(\frac{0.35V}{ms}\right) = 2000\mu F \bullet \left(\frac{0.35V}{ms}\right) = 700mA \quad (8)$$

As mentioned previously the charge-up time is the output voltage (12V) divided by the output rate of 0.35V/ms resulting in 34ms. The average power dissipation of 12V at 700mA (or 4.2W) must not exceed the SOA of the pass MOSFET for 34ms. This works out to be 0.774W$\sqrt{s}$, since the MOSFET sees a V_{DS} ramp of 0V to 12V. This is below the LT4200 P$\sqrt{t}$ spec of 7.5W$\sqrt{s}$.

Next the power dissipated in the MOSFET during overcurrent must be limited. The active current limit uses a timer to prevent excessive energy dissipation in the MOSFET. The worst-case power dissipation occurs when the voltage versus current profile of the foldback current limit is at the maximum. This occurs when the current is 53.2A and the FB voltage is 1V, V_{OUT} = 8.5V and MOSFET V_{DS} = 3.5V. See the Current Limit Threshold Foldback in the Typical Performance Characteristics section to view this profile. In order to survive 186W, the MOSFET SOA dictates a maximum current limit timeout.

T_J is calculated with Equation 9 from the ambient temperature, package thermal impedance (θ_{JA}) and the I^2R heating.

$$T_J = (\theta_{JA} \bullet I^2 \bullet R_{ON}) + T_A = 12°C/W \bullet (50A)^2 \bullet 2.2m\Omega + 25°C = 91°C \quad (9)$$

The maximum current limit timeout is calculated from the P$\sqrt{t}$ constant and the 186W dissipated in current limit as shown in Equation 10.

$$P\sqrt{t} = 7.5W\sqrt{s}$$

$$t_{MAX} = \left(\frac{7.5W\sqrt{s}}{P}\right)^2$$

$$t_{MAX} = \left(\frac{7.5W\sqrt{s}}{186}\right)^2 \quad (10)$$

$$t_{MAX} = 1.63ms$$

Therefore, it is acceptable to set the current limit timeout using C_T to be 0.8ms (Equation 11).

$$C_T = \frac{0.8ms}{12[ms/\mu F]} = 68nF \quad (11)$$

To configure the LT4200 for auto retry after overcurrent fault, connect the FLT# to the UV pin.

After the 0.8ms timeout the FLT# pin pulls down on the UV pin restart the power-up sequence.

The resistive divider values for overvoltage (15.2V), undervoltage (9.88V) and power good (10.5V) thresholds can be calculated as follow: First, choose the bottom resistors (R2, R4 and R6) to be 20k, this makes the resistive divider draw 62µA of current if the input voltage is near the threshold. The top resistor values are calculated using Equation 12, Equation 13, and Equation 14.

$$R1 = R2 \bullet \left(\frac{V_{OV}}{1.235V} - 1\right) = 226k \quad (12)$$

APPLICATIONS INFORMATION

$$R3 = R4 \bullet \left(\frac{V_{UV}}{1.235V} - 1 \right) = 140k \quad (13)$$

$$R5 = R6 \bullet \left(\frac{V_{PG}}{1.235V} - 1 \right) = 150k \quad (14)$$

The final schematic in Figure 5 results in very few external components. The pull-up resistor, R7, connects to the PG pin while the 20k (R_{MON}) converts the IMON current to a voltage at a ratio given by Equation 15.

$$V_{IMON} = 2[\mu A/A] \bullet 20k \bullet I_{OUT} = 0.04[V/A] \bullet I_{OUT} \quad (15)$$

In addition there is a 1µF bypass (C1) on the $INTV_{CC}$ pin and note the connection between $SENSE^+$ to V_{DD} (Pin 32 to Pin 22).

Layout Considerations

In hot swap applications where load currents can be 50A, narrow PCB tracks exhibit more resistance than wider tracks and operate at elevated temperatures. The minimum trace width requirement for 2oz copper foil is 0.01" per amp to make sure the trace stays at a reasonable temperature. Using 0.02" per amp or wider is recommended. Note that 2oz copper exhibits a sheet resistance of about 0.25mΩ/square. Small resistances add up quickly in high current applications.

The $SENSE^+$ pin can be connected to the middle of the wide V_{DD} trace near pin 26 to provide Kelvin sensing for V_{DD} (see Figure 6). Make sure to minimize the solder joint resistance at these V_{DD} pins by applying solder along the whole length of the V_{DD} bar that connects pin 22 to 30. High solder joint resistance will add error to the IMON gain and $I_{LIM(TH)}$ accuracy.

During normal operation, the power dissipated in the MOSFET could be as high as 3W. To remove this heat, solder the $SENSE^-$, exposed pad to a copper trace that contains vias underneath the pad. The OUT pins conduct substantial heat from the MOSFET. Connect all the OUT pins to a plane of 2oz copper. Since the trace that connects OUT pins must accommodate high current, this area of copper is usually present. It is also important to put C1, the bypass capacitor for the $INTV_{CC}$ pin, as close as possible between $INTV_{CC}$ and GND.

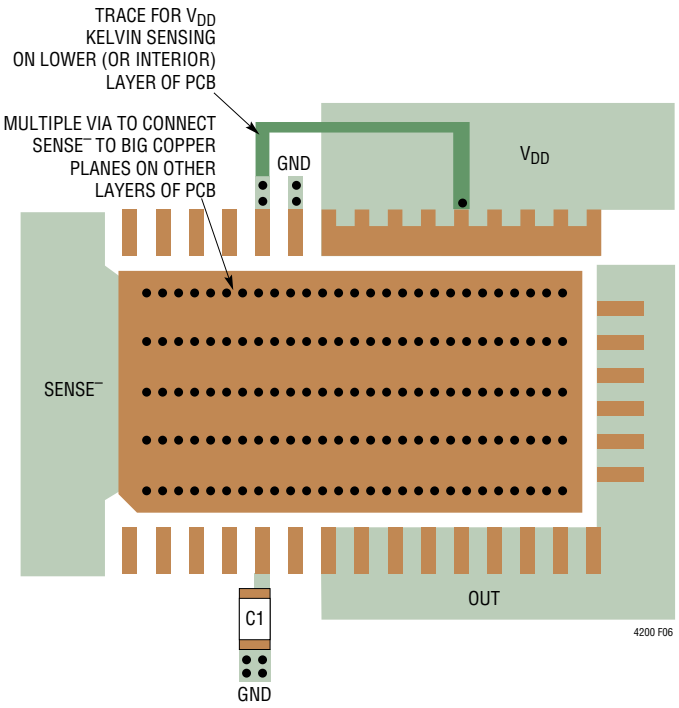


Figure 6. Recommended Layout

Thermal Considerations

If the LT4200 operates near its maximum load current of 50A, the junction temperature can rise to a level near the thermal shutdown temperature if insufficient heat sinking is used. Always maximize the PCB copper area and thickness connected to the $SENSE^-$, OUT and V_{DD} pins. The V_{DD} and OUT pins require a wide copper trace to carry the 50A current which will also help to conduct the heat away from the LT4200. The $SENSE^-$ exposed pad, although not carrying any current, should be as big as possible to help in the heat dissipation of the internal MOSFET. As shown in Figure 6, the $SENSE^-$ exposed pad can be connected through via to the other layers of the PCB with large copper planes. The size and thickness of these copper planes will affect the junction temperature of the LT4200. For example, the temperature rise is 38°C at 50A with an 8-layer PCB (2oz copper for top/bottom PCB layers with the rest 1oz thick) and with a large copper area of 17 inch square connected to $SENSE^-$ on the middle layers. If we reduce the copper area on the middle layers to 1-inch square, the temperature rise increases by another 20°C at 50A.

APPLICATIONS INFORMATION

Additional Applications

The LT4200 has a wide operating range from 2.9V to 15V. The UV, OV and PG thresholds are set with few resistors. All other functions are independent of supply voltage.

In addition to hot swap applications, the LT4200 also functions as a backplane resident switch for removable load cards (see Figure 7).

Figure 8 shows a 3.3V application with a UV threshold of 2.87V, an OV threshold of 3.77V and a PG threshold of 3.05V.

The last page shows a 100A parallel application where the two LT4200 parts each provide 50A to the load. The PNPs prevent one LT4200 from faulting off in current limit until both parts hit the 57A limit. The PNPs are disconnected when power good is false via the series MOSFETs M1 and M2.

TYPICAL APPLICATIONS

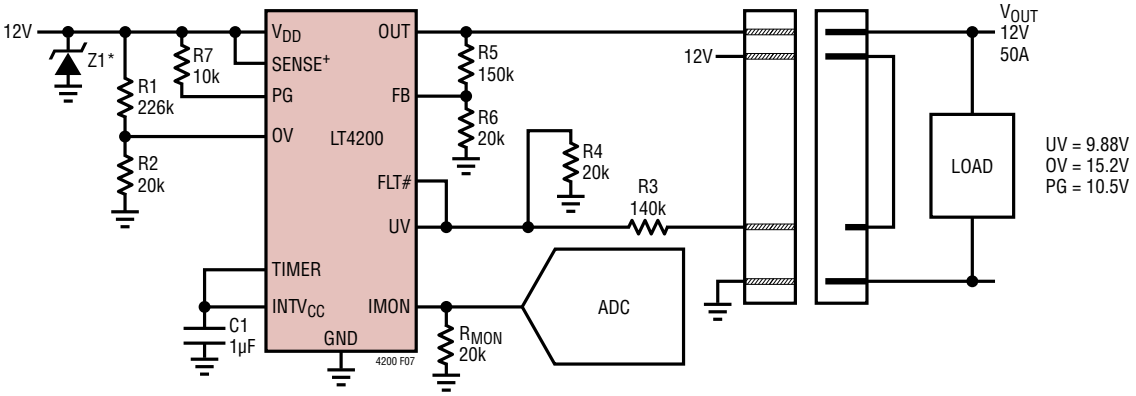


Figure 7. 12V, 50A Backplane Resident Application with Insertion Activated Turn-On

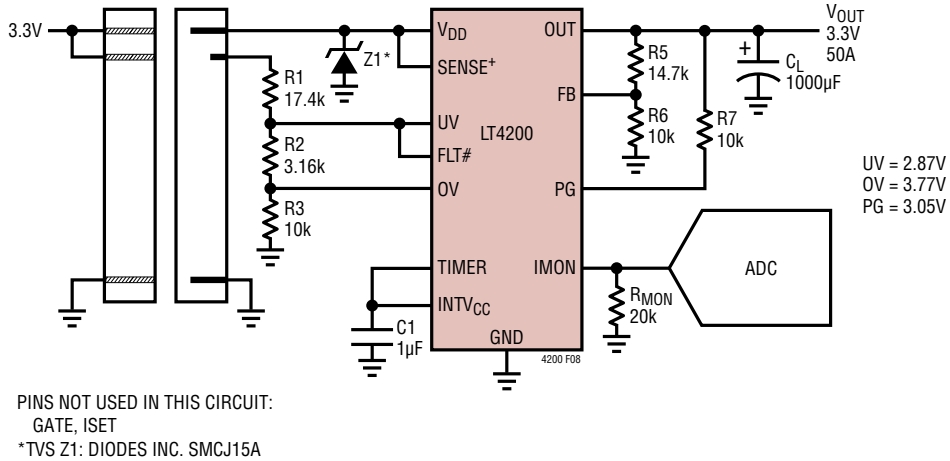
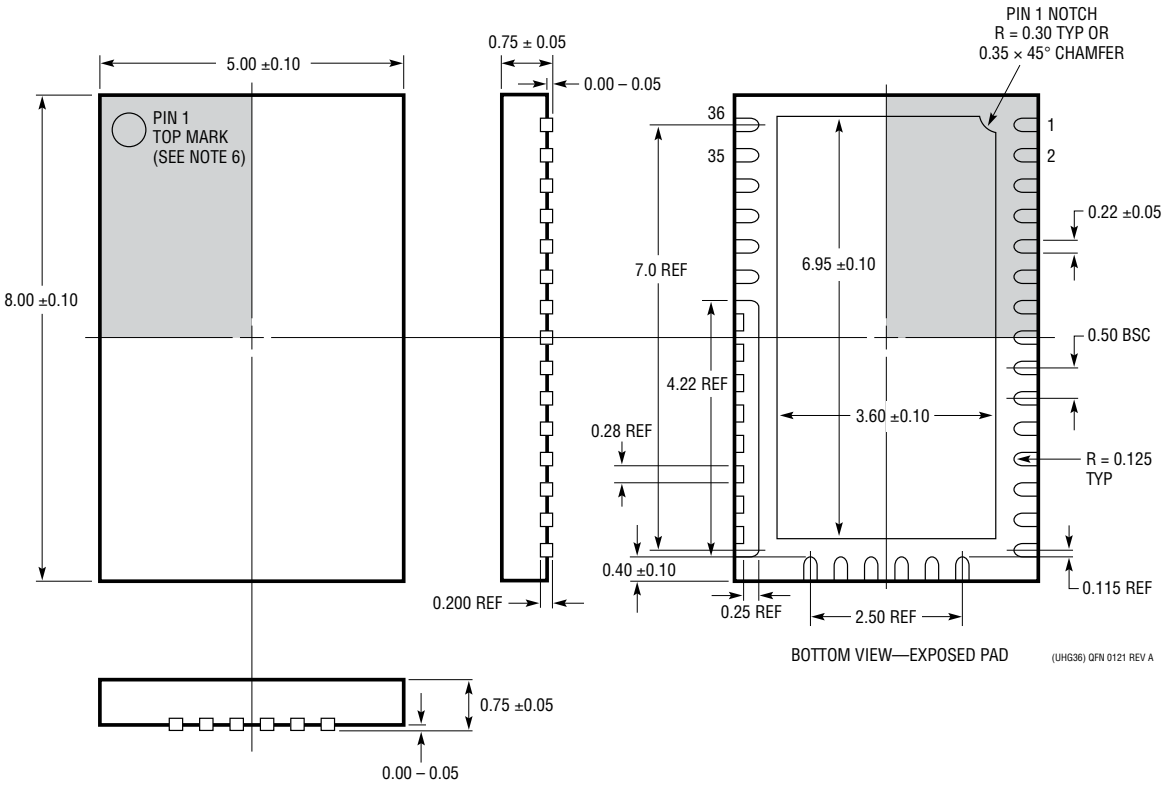


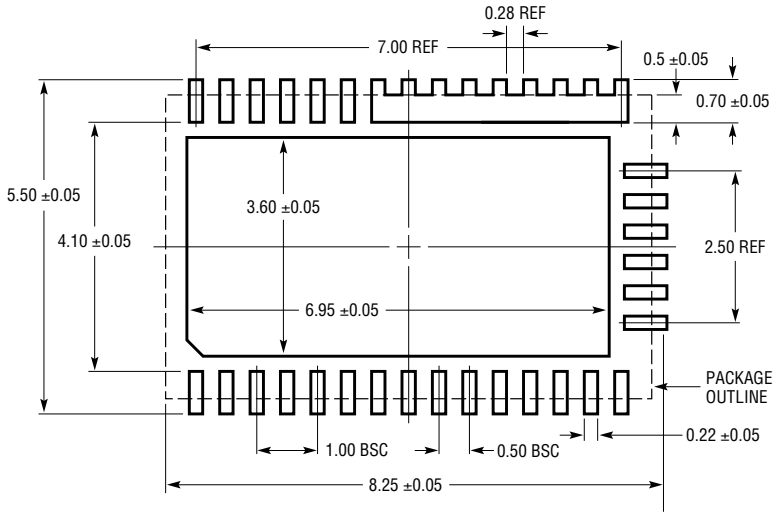
Figure 8. 3.3V, 50A Card Resident Application with Auto-Retry

PACKAGE DESCRIPTION

UHG Package
36-Lead Plastic QFN (5mm × 8mm)
(Reference LTC DWG # 05-08-1790 Rev A)



NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED