High Current Hot Swap Controller with Current Monitor Output

FEATURES

- **Allows Safe Board Insertion into Live Backplane**
- **Wide Operating Voltage Range: 4V to 20V**
- **Dual Gate Drivers for High Current Applications**
- **Withstands Surge Voltage without Protection TVS**
- **Monitors V_{GS} and V_{DS} for MOSFET Health**
- **Accurate 10mV ± 5% Circuit Breaker Threshold**
- Boost Mode for Load Surges
- Current Monitor Output
- 12V Gate Drive for Lower MOSFET $R_{DS(ON)}$
- Adjustable Start-Up and Overcurrent Fault Delay
- Input Undervoltage Protection
- Fault and Power Good Output
- 16-Lead 4mm × 3mm DFN Package

APPLICATIONS

- Electronic Circuit Breaker
- Enterprise Servers and Data Storage Systems
- Network Routers and Switches

DESCRIPTION

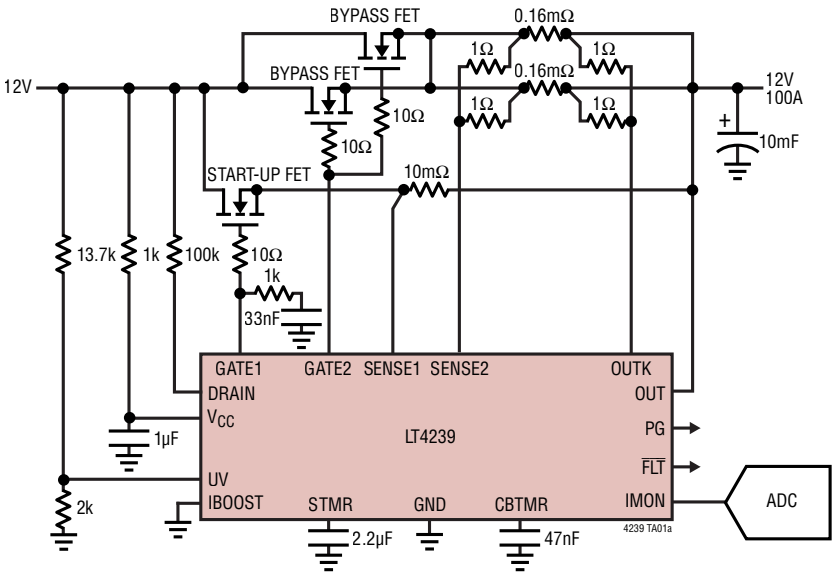
The LT®4239 hot swap controller allows a board to be safely inserted and removed from a live backplane. Using external N-channel pass transistors, board supply voltage and inrush current are ramped up at a controlled rate. Dual 12V gate drive supports high current loads by providing a two-stage start-up that first charges the load capacitance followed by enabling a low on-resistance path to the load. The supply output is protected against short-circuit faults with a fast-acting electronic circuit breaker.

By placing the sense resistor on the output side and an RC filter at the device's supply pin, the MOSFET avalanching can suppress the surge voltage when it is abruptly turned off without the additional TVS at the board supply input.

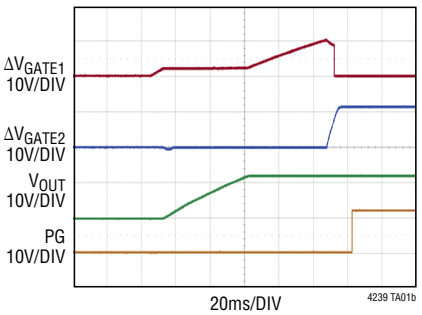
The LT4239 features a current monitor that amplifies the voltage across an external sense resistor. It also provides undervoltage protection, and reports fault and power good status for the supply. A boost mode allows the circuit breaker and current limit thresholds to be raised to ride through load surges without generating a fault.

TYPICAL APPLICATION

12V, 100A Application



Start-Up Waveforms



Rev. 0

ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltages
- V_{CC} ..... –0.3V to 25V

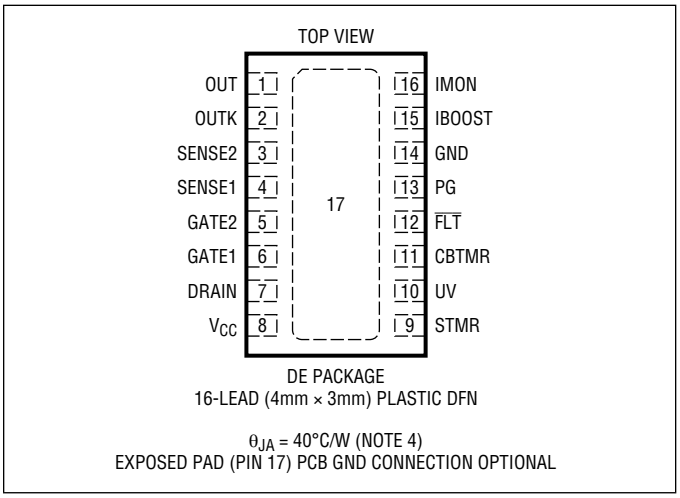
Input Voltages
- DRAIN, IBOOST, UV ..... –0.3V to 25V
- OUT, OUTK, SENSE1, SENSE2 ..... –0.3V to 30V
- CBTMR, STMR ..... –0.3V to 5V
- V_{CC} – DRAIN ..... –5V to 5V
- V_{CC} – SENSE1, V_{CC} – SENSE2 ..... –10V to 25V
- V_{CC} – OUT, V_{CC} – OUTK ..... –10V to 25V
- V_{CC} – GATE1, V_{CC} – GATE2 ..... –10V to 25V
- SENSE2 – OUTK ..... –5V to 5V
- GATE1 – OUT, GATE2 – OUT (Note 3) .... –0.3V to 10V
- I_{DRAIN} 2mA

Output Voltages
- IMON ..... –0.3V to 6V
- $\overline{FLT}$, PG ..... –0.3V to 25V
- GATE1, GATE2 (Note 3) ..... –0.3V to 40V

Operating Junction Temperature Range
- LT4239A ..... –40°C to 125°C

Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



ORDER INFORMATION

LEAD FREE FINISH	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT4239ADE#PBF	4239	16-Lead (4mm × 3mm) Plastic DFN	–40°C to 125°C

Contact the factory for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 12V, IBOOST = 0V, R_{DRAIN} = 100kΩ, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supplies							
V_{CC}	Input Supply Range		●	4		20	V
I_{CC}	Input Supply Current	V_{CC} = 4V to 13.2V	●		0.6	1	mA
$V_{CC(UVL)}$	V_{CC} Undervoltage Lockout	V_{CC} Rising	●	3.3	3.6	3.8	V
$\Delta V_{CC(HYST)}$	V_{CC} Undervoltage Lockout Hysteresis				100		mV
Circuit Breaker and Current Limit							
$\Delta V_{SENSE2(CB)}$	Circuit Breaker Trip Threshold ($V_{SENSE2} - V_{OUTK}$)	IBOOST = 0V, OUT = V_{CC} IBOOST = 3V, OUT = V_{CC}	● ●	9.5 19	10 20	10.5 21	mV mV
$\Delta V_{SENSE2(ACL)}$	Analog Current Limit Threshold ($V_{SENSE2} - V_{OUTK}$)	IBOOST = 0V IBOOST = 3V	● ●	13 26	15 30	17 34	mV mV
$\Delta V_{SENSE2(FAST)}$	Fast Comparator Trip Threshold ($V_{SENSE2} - V_{OUTK}$)	IBOOST = 0V IBOOST = 3V	● ●	30 60	40 80	50 100	mV mV
$\Delta V_{SENSE1(ACL)}$	Analog Current Limit Threshold ($V_{SENSE1} - V_{OUTK}$)		●	45	50	55	mV
I_{SENSE1}	SENSE1 Current	SENSE1 = SENSE2 = OUTK = 12V	●	20	50	100	µA
I_{SENSE2}	SENSE2 Current	SENSE1 = SENSE2 = OUTK = 12V	●	20	70	140	µA
I_{OUTK}	OUTK Current	SENSE1 = SENSE2 = OUTK = 12V	●	40	100	200	µA
I_{OUT}	OUT Current	OUT = 12V	●	0.1	0.45	1	mA
Gate Drive							
ΔV_{GATE}	Gate Drive	I_{GATE1} = 0, –1µA	●	10	12	14	V
		I_{GATE2} = 0, –5µA	●	10	12	14	V
$\Delta V_{GATE(TH)}$	Gate Threshold for Start-Up and Power Good		●	10			V
$I_{GATE1(UP)}$	Gate Pull-Up Current	Gate Drive On, ΔV_{GATE1} = 0V	●	–7	–10	–13	µA
$I_{GATE2(UP)}$	Gate Pull-Up Current	Gate Drive On, ΔV_{GATE2} = 0V	●	–35	–50	–65	µA
$I_{GATE1(DN)}$	Gate Off Pull-Down Current	Gate Drive Off, OUT=12V, ΔV_{GATE1} = 10V	●	5	10	25	mA
$I_{GATE2(DN)}$	Gate Off Pull-Down Current (UV Turn-Off) (Overcurrent Fault)	Gate Drive Off, OUT=12V, ΔV_{GATE2} = 10V Gate Drive Off, OUT=12V, ΔV_{GATE2} = 10V	● ●	5 30	10 50	25 70	mA mA
$I_{GATE1(FPD)}$	Gate Fast Pull-Down Current	Fast Turn-Off, OUT=12V, ΔV_{GATE1} = 10V	●	50	130	300	mA
$I_{GATE2(FPD)}$	Gate Fast Pull-Down Current	Fast Turn-Off, OUT=12V, ΔV_{GATE2} = 10V	●	0.3	0.6	1.5	A
Comparator Inputs							
ΔV_{DS1}	Voltage to Enable GATE2 Start-Up ($V_{CC} - V_{OUTK}$)	Falling	●	0.8	1	1.3	V
ΔV_{DS2}	Voltage to Start Power Good Delay ($V_{CC} - V_{OUTK}$)	Falling	●	80	100	130	mV
$\Delta V_{DS(FET-BAD)}$	FET-Bad Fault Threshold After Power Good ($V_{CC} - V_{OUTK}$)	IBOOST = 0V IBOOST = 3V	● ●	80 160	100 200	120 240	mV mV
$\Delta V_{DS(FETSHORT)}$	FETShort Fault Threshold During Debounce ($V_{CC} - V_{OUTK}$)		●	1.1	1.3	1.5	V
$V_{UV(TH)}$	UV Threshold Voltage	UV Rising	●	1.207	1.232	1.257	V
$\Delta V_{UV(HYST)}$	UV Hysteresis				50		mV
$V_{UV(RESET)}$	UV Fault Reset Threshold Voltage	UV Falling	●	0.45	0.6	0.65	V
$V_{IBOOST(TH)}$	IBOOST High Threshold Voltage		●	1.6			V
	IBOOST Low Threshold Voltage		●			0.8	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 12V, IBOOST = 0V, R_{DRAIN} = 100kΩ, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$I_{(LEAK)}$	UV, IBOOST Input Leakage Current	V = 5V	●		0	±1	µA
$V_{OUT(G2OFF)}$	OUT Voltage to Turn Off GATE2 After Power Good	OUT Falling	●	3.5	3.7	3.9	V
Timer							
$V_{TMR(H)}$	STMR, CBTMR High Threshold Voltage	Rising	●	1.207	1.232	1.257	V
$V_{TMR(L)}$	STMR, CBTMR Low Threshold Voltage	Falling	●	0.15	0.2	0.25	V
$I_{STMR(UP)}$	STMR Pull-Up Current	STMR = 1V, GATE1 Start-Up	●	-8	-10	-12	µA
$I_{STMR(DN)}$	STMR Pull-Down Current	STMR = 1V	●	80	125	170	µA
$I_{CBTMR(UP)}$	CBTMR Pull-Up Current	CBTMR = 1V, In Overcurrent Fault	●	-8	-10	-12	µA
$I_{CBTMR(DN)}$	CBTMR Pull-Down Current	CBTMR = 2V, No Faults CBTMR = 2V, In Cool-Off Cycle	● ●	8 3	10 4	12 5	µA µA
D_{RETRY}	Retry Duty Cycle During Overcurrent Fault		●	0.03	0.06	0.1	%
Current Monitor							
$\Delta V_{SENSE2(FS)}$	Input Sense Voltage Full-Scale ($V_{SENSE2} - V_{OUTK}$)	IBOOST = 0V, OUT = 12V IBOOST = 3V, OUT = 12V	● ●	15 30			mV mV
$V_{IMON(OS)}$	IMON Input Offset Voltage	ΔV_{SENSE2} = 0V, OUT = 12V	●			±800	µV
A_{IMON}	IMON Voltage Gain	ΔV_{SENSE2} = 1mV to 15mV, OUT = 12V	●	97	100	103	V/V
$V_{IMON(MAX)}$	IMON Maximum Output Voltage	ΔV_{SENSE2} = 50mV, OUT = 12V	●	4.5	4.9	5.5	V
$R_{IMON(OUT)}$	IMON Internal Resistance	ΔV_{SENSE2} = 0V, OUT = 12V	●	15	20	25	kΩ
BW_{IMON}	IMON Bandwidth				200		kHz
Outputs							
V_{OL}	$\overline{FLT}$, PG Output Low Voltage	I = 5mA	●		0.2	0.4	V
I_{OH}	$\overline{FLT}$, PG Input Leakage Current	V = 5V	●		0	±1	µA
Timing Delays							
$t_{PHL(SENSE1)}$	ΔV_{SENSE1} Voltage High to GATE1 Low	ΔV_{SENSE1} = 0V Step to 300mV	●		0.5	1	µs
$t_{PHL(SENSE2)}$	ΔV_{SENSE2} Voltage High to GATE2 Low	ΔV_{SENSE2} = 0V Step to 80mV	●		0.5	1	µs
$t_{TMR(ACL)}$	Overcurrent Fault Timer Delay	ΔV_{SENSE1} = 0V Step to 100mV ΔV_{SENSE2} = 0V Step to 25mV	● ●	80 90	100 100	115 110	µs µs
$t_{TMR(FET-BAD)}$	FET-Bad Fault Timer Delay		●	17	20	23	ms
$t_{D(PG)}$	Power Good Delay		●	8	10	12	ms
$t_{D(GATE1)}$	Debounced Turn-On Delay	UV = 0V Step to 2V	●	20	25	30	ms
$t_{OFF(GATE)}$	GATE Turn-Off Propagation Delay	UV = 2V Step to 0.8V	●	170	220	270	µs
$t_{OFF(GATE2)}$	GATE2 Turn-Off Delay After Power Good	OUT = 12V Step to 0V	●		1	2	µs
$t_{RST(UV)}$	UV Low to $\overline{FLT}$ High	UV = 2V Step to 0V	●		20	40	µs

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All currents into device pins are positive; all currents out of the device pins are negative. All voltages are referenced to GND unless otherwise specified.

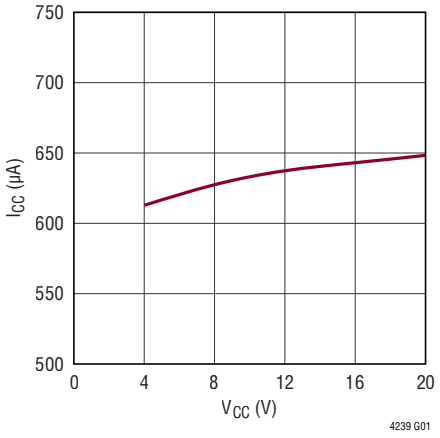
Note 3: Limits on maximum rating is defined as whichever limit occurs first. Internal clamps limit the GATE pins to a minimum of 10V above OUT and a diode below OUT. Driving the GATE pins to voltages beyond the clamps may damage the device.

Note 4: Thermal resistance is specified when the exposed pad is soldered to a 3-inch × 5-inch, four layer, FR4 board.

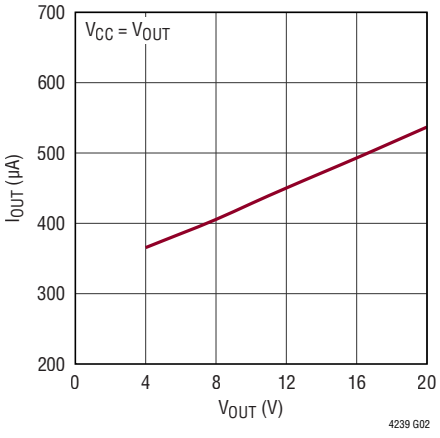
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{CC} = 12V, IBOOST = 0V, R_{DRAIN} = 100kΩ, unless otherwise noted.

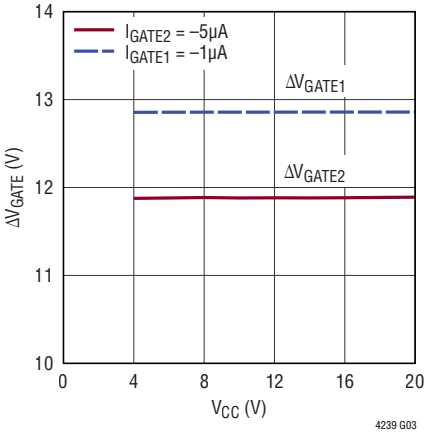
V_{CC} Supply Current vs Voltage



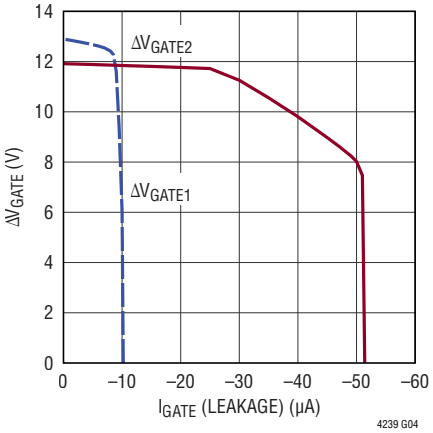
OUT Current vs Voltage



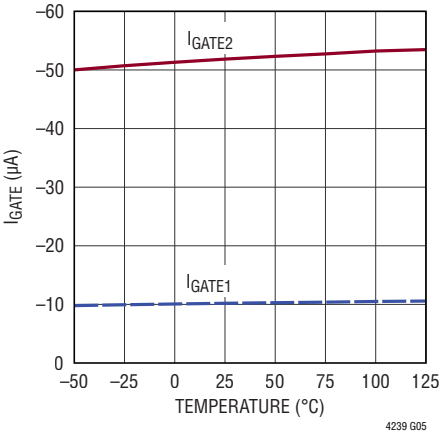
MOSFET Gate Drive vs V_{CC} Voltage



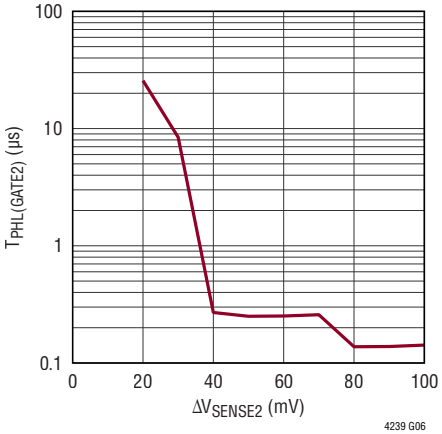
MOSFET Gate Drive vs Gate Leakage Current



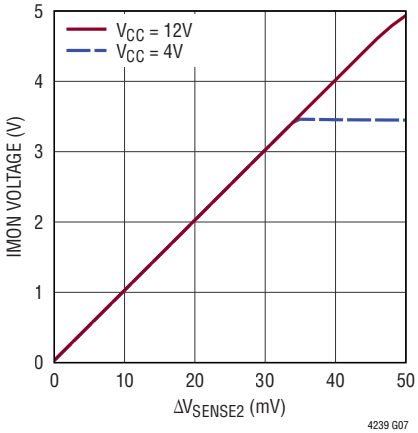
MOSFET Gate Drive Pull-Up Current vs Temperature



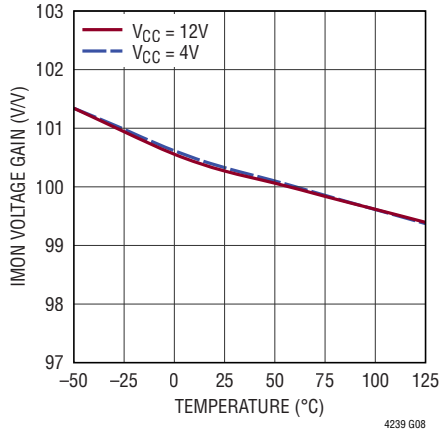
Current Limit Propagation Delay vs Sense Voltage



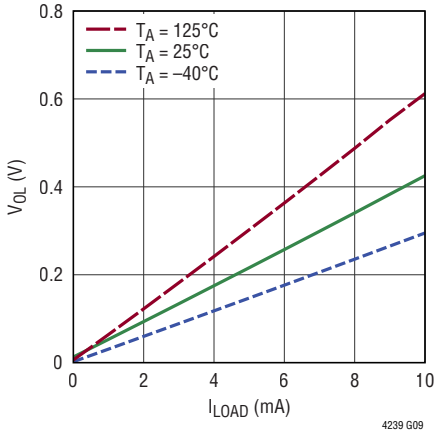
IMON Voltage vs Sense Voltage



IMON Voltage Gain vs Temperature



$\overline{FLT}$ and PG Output Low Voltage vs Load Current



PIN FUNCTIONS

OUT (Pin 1): MOSFET Gate Drive Return. Connect this pin to the output side of the current sense resistor. The gate fast pull-down current returns through this pin when gates are discharged. GATE2 is pulled low quickly when OUT falls below 3.7V after power good.

OUTK (Pin 2): Negative Current Sense Input. Connect to the output terminal of the current sense resistor.

SENSE1, SENSE2 (Pins 4, 3): Positive Current Sense Input. Connect to the input side of the current sense resistor. The current limit circuit controls GATE1 to limit the voltage between SENSE1 and OUTK to 50mV for 100µs before fault latched-off during start-up. After GATE2 turns on, the circuit breaker will trip when the voltage between SENSE2 and OUTK exceeds 10mV longer than the overcurrent fault timer period. During an overload condition, GATE2 is regulated to maintain 15mV of voltage drop across SENSE2 and OUTK for 100µs before fault latched-off.

GATE2 (Pin 5): Gate Drive for External N-Channel MOSFETs. An internal 50µA current source starts charging up the gate of the Bypass MOSFET when ΔV_{GATE1} is higher than 10V and $V_{IN} - V_{OUT} < 1V$. GATE2 is limited to 12V above OUT by internal clamps. A 10mA current source keeps the MOSFET off when the part is in undervoltage condition. When a short-circuit condition is detected, GATE2 is pulled down to OUT by a 50mA current source. This current increases to 600mA when a severe output short is detected.

GATE1 (Pin 6): Gate Drive for External N-Channel MOSFET. An internal 10µA current source charges up the gate of the Start-up MOSFET. The inrush current can be limited by the additional R-C network from GATE1 to GND by controlling its slew rate. GATE1 is limited to 12V above OUT by internal clamps. GATE1 turns off when power good condition, $\Delta V_{GATE2} \geq 10V$ and $V_{IN} - V_{OUT} < 100mV$, are achieved. A 10mA current source keeps the MOSFET off when the part is in undervoltage condition. When a short-circuit condition is detected, GATE1 is pulled down to OUT by a 10mA current source. This current increases to 130mA when a severe output short is detected.

DRAIN (Pin 7): External MOSFET's Drain Sense Input. Connect a 100k resistor between this pin and the drain of the external N-Channel MOSFET to monitor the difference between MOSFET's drain and OUTK voltages. The voltage sensed at this pin enables the GATE2 start-up and power good delay after GATE1 is fully enhanced. If the voltage between the MOSFET's drain and OUTK rises above 100mV after power good, a 20ms FET-Bad fault timer will be activated.

V_{CC} (Pin 8): Positive Supply Input. If supply voltage spikes might exceed 25V, connect an RC filter at this pin. This pin has an undervoltage lockout threshold of 3.6V that will turn off all the MOSFETs.

STMR (Pin 9): Start-Up Timer. Connect a capacitor between this pin and ground to set a 123ms/µF duration for start-up. If either the MOSFET gate drive at GATE1 remains below 10V or the voltage between MOSFET's drain and OUTK is greater than 100mV at the end of the start-up timer ramp-up, the start-up cycle is aborted. GATE1 pulls low turning off the MOSFET and $\overline{FLT}$ pulls low to indicate a start-up fault.

UV (Pin 10): Undervoltage Comparator Input. Connect to an external resistive voltage divider from the input supply to monitor the supply voltage. This pin has a 25ms debounce time on the rising edge before GATE1 start-up. If the voltage at this pin falls below 1.182V, an undervoltage fault is detected and all the MOSFETs will be turned off. Pulling the UV pin below 0.6V resets the fault latch after a fault due to start-up failure, overcurrent, or FET short. Connect to V_{CC} if unused.

CBTMR (Pin 11): Overcurrent Fault Timer. Connect a capacitor between this pin and ground to set a 123ms/µF duration for circuit breaker timeout, after which an overcurrent fault is generated and GATE2 is pulled low. The duration of the cool down time is 185s/µF when the device is configured for auto-retry, resulting in a 0.06% duty cycle.

PIN FUNCTIONS

$\overline{\text{FLT}}$ (Pin 12): Open Drain Fault Output. Output that pulls low when a fault occurs. It can be a start-up fault, or a fault timer expired due to a FET-Bad or an overcurrent fault. Otherwise, it goes high impedance and requires an external pull-up resistor to a positive supply. Leave unconnected if unused.

PG (Pin 13): Open Drain Power Good Status Output. The pin is kept low until a power good condition is valid for 10ms. To initiate the 10ms power good timer, ΔV_{GATE2} needs to be above 10V and the voltage difference across the Bypass MOSFET is less than 100mV. Connect a resistor from this pin to a positive supply voltage. Leave unconnected if unused.

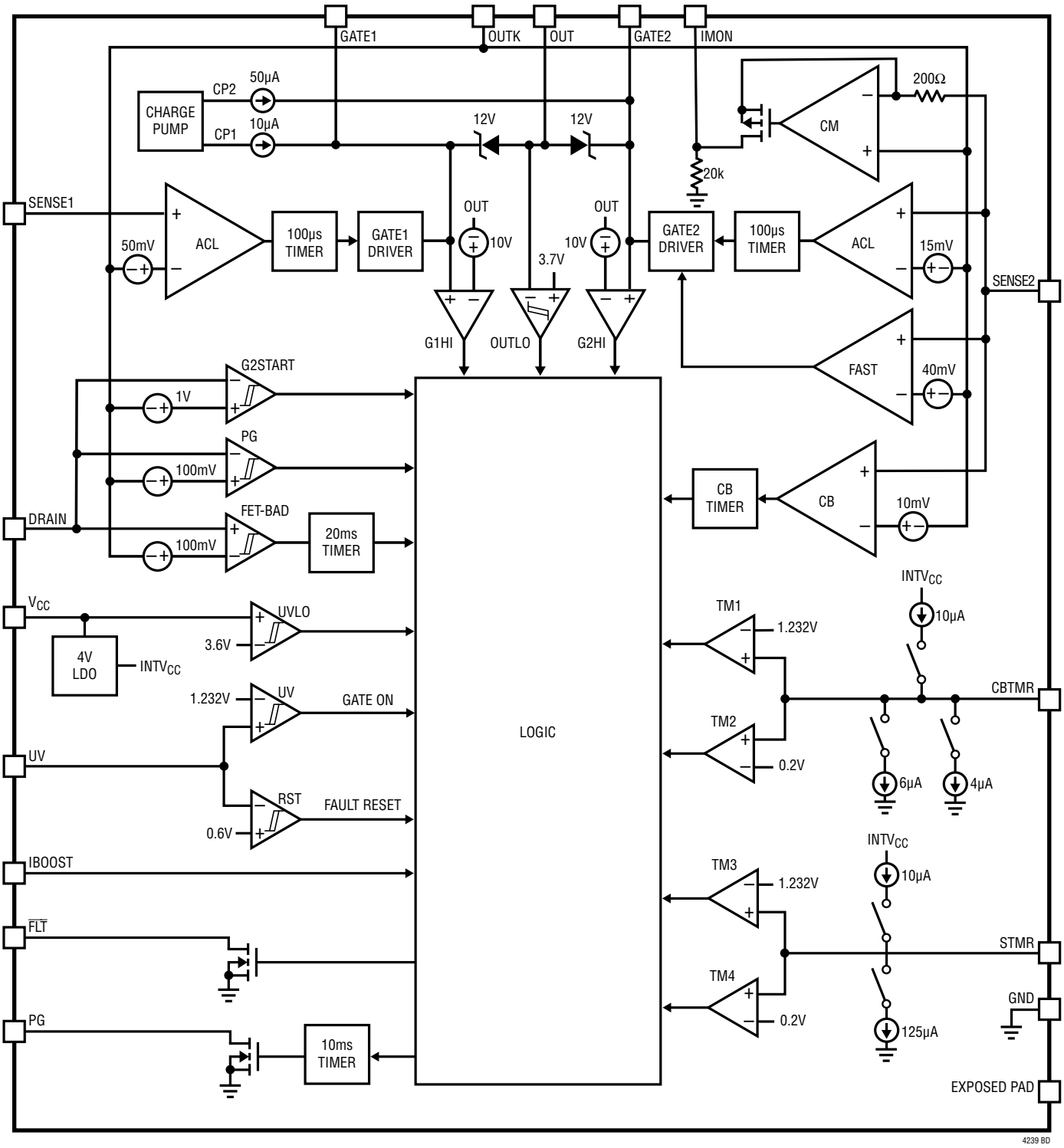
GND (Pin 14): Device Ground.

IBOOST (Pin 15): Extra Loading Request Input. Pulls this pin high to double both the circuit breaker and active current limit thresholds. This allows the Bypass MOSFET to supply higher current without triggering either the circuit breaker or the current limit timers. Connect to GND to disable this function.

IMON (Pin 16): Current Sense Monitor Output. This voltage at the pin is proportional to the sense voltage monitored between the SENSE2 and OUTK pins with a voltage gain of 100. An internal 20k resistor is connected from this pin to ground. The measurement is valid only when OUT is above 3.7V and PG is pulled high, otherwise the pin is pulled low to ground. Leave unconnected if unused.

Exposed Pad (Pin 17): May be left open or connected to device ground.

BLOCK DIAGRAM



OPERATION

The LT4239 is designed to turn a board's supply voltage on and off in a controlled manner, allowing the board to be safely inserted or removed from a live backplane. Input protection devices such as Transient Voltage Suppressors (TVS) are not required with this architecture. The avalanching of the MOSFET will limit the voltage spike on the input while the RC filter connected to the V_{CC} pin protects it from this transitory voltage.

LT4239 features a "Low Stress Staged Start" technique using two gate drives to sequence the turn-on of the external MOSFETs. At initial power-up, if UV is pulled above its turn-on threshold, a 25ms debounce cycle is initiated to ensure the input supply is firmly connected. After debounce, GATE1 is charged up with a 10µA current source. MOSFET M1 turns on and charges the output capacitor with a current level that is set by the slew rate at GATE1 and the output capacitance. Since the inrush current level is usually much smaller than the maximum load current, a small MOSFET can be chosen for M1. The current flowing through M1 is constantly monitored through the voltage drop on the sense resistor R_{S1}. This voltage is regulated to 50mV lasting for 100µs before the part turns off and $\overline{FLT}$ pulls low during an overcurrent condition.

When the output voltage rises to within 1V of the input's and ΔV_{GATE1} is greater than 10V, M2 turns on with a strong gate pull-up current of 50µA. A lower SOA rated and lower $R_{DS(ON)}$ MOSFET can be used to keep the MOSFET's cost down. For high current applications, multiple MOSFETs can be connected in parallel reducing the voltage drop and power dissipation. When the output voltage reaches within 100mV of the input supply and ΔV_{GATE2} is more than 10V, GATE1 turns off.

Upon the completion of the 10ms power good timer, PG goes high impedance indicating to the system that M2 is fully enhanced and ready to supply the load. The total duration from the completion of the debounce time to the start of the power good timer is set by a capacitor connected from the STMR pin to ground. If due to any reasons, such as output soft short, bad MOSFET connection or design mistake, PG timer does not start before the start-up timer expires, LT4239 latches off and pulls $\overline{FLT}$ low. Pull the UV pin below the 0.6V reset threshold to restart the part.

At any time if the current flowing through M2 creates more than 10mV of voltage drop across sense resistor R_{S2}, a circuit breaker timer will start with the duration set by a capacitor at the CBTMR pin. At the expiration of the CB timer, M2 turns off and $\overline{FLT}$ pulls low. If the current flowing through M2 is large, such as during an output short-circuit, the voltage drop across R_{S2} is regulated to 15mV for 100µs. Connecting the $\overline{FLT}$ pin to the UV pin will allow an automatic retry after a long cool-down period.

LT4239 monitors the MOSFETs condition constantly even after PG goes high impedance. If during the operation the voltage drop from input to output is more than 100mV or ΔV_{GATE2} drops below 10V, a FET-Bad timer of 20ms starts. After the timer expires, GATE2 latches off and $\overline{FLT}$ pulls low. Restart the part by lowering the V_{CC} pin below the 3.6V undervoltage lockout threshold momentarily as UV cannot reset such fault.

A boost mode allowing extra current to flow through the pass transistors without triggering fault timers is included in the LT4239. Pull IBOOST pin above 1.6V to double both the circuit breaker and current limit thresholds. The FET-Bad fault threshold is also doubled to allow temporarily load surge.

A current sense amplifier (CM) that is active during normal operating condition provides accurate monitoring of current through the current sense resistor R_{S2}. The sense voltage is amplified by 100 times and level shifted to a ground-referred output at the IMON pin. This analog output voltage can be digitized by an external ADC.

APPLICATIONS INFORMATION

In most high current Hot Swap applications, multiple parallel MOSFETs are used to minimize the voltage drop, power loss and accompanying temperature rise on the pass transistors. Due to the gate threshold variation, parallel MOSFETs driven by a single gate driver tend to concentrate the current into a single MOSFET during initial turn-on or current limit. As a result, expensive MOSFETs with enough SOA to withstand such events are needed. The LT4239 offers a low-cost solution by providing two gate drivers to separately control the initial turn-on and the power distribution. Only start-up MOSFET is needed for initial turn-on and one or more parallel MOSFETs with low $R_{DS(ON)}$ bypass the start-up for power distribution. The following sections cover turn-on, turn-off, and various faults that the LT4239 detects and acts upon. External component selection is discussed in detail in the Design Example section.

A typical LT4239 application circuit operating at 12V supply with a 100A load in a high availability system is shown in Figure 1. The board power supply at the OUT pin is controlled with external N-Channel MOSFETs (M1, M2) placed in the power path. M1 is a trickle MOSFET for start-up while M2 can be a group of parallel MOSFETs for passing the power. The current through the MOSFETs is monitored with sense resistors (R_{S1}, R_{S2}) connected on the source side of the MOSFETs. Resistors R10 – R13 are part of the sense resistor averaging network. Resistors R1 and R2 at the UV pin define an undervoltage level of the input supply to turn on the MOSFETs. R_{VCC} and C1 protect the V_{CC} pin from input supply transient spikes and help holding up the V_{CC} voltage when the input supply collapses during output short. The MOSFET's drain voltage is monitored through R_{DRAIN} at the DRAIN pin. R3 and R4 prevent high frequency self-oscillations in M1 and M2 respectively. The R-C network, R_{G1} and C_{G1} at GATE1 pin limit the inrush to the load capacitance during start-up.

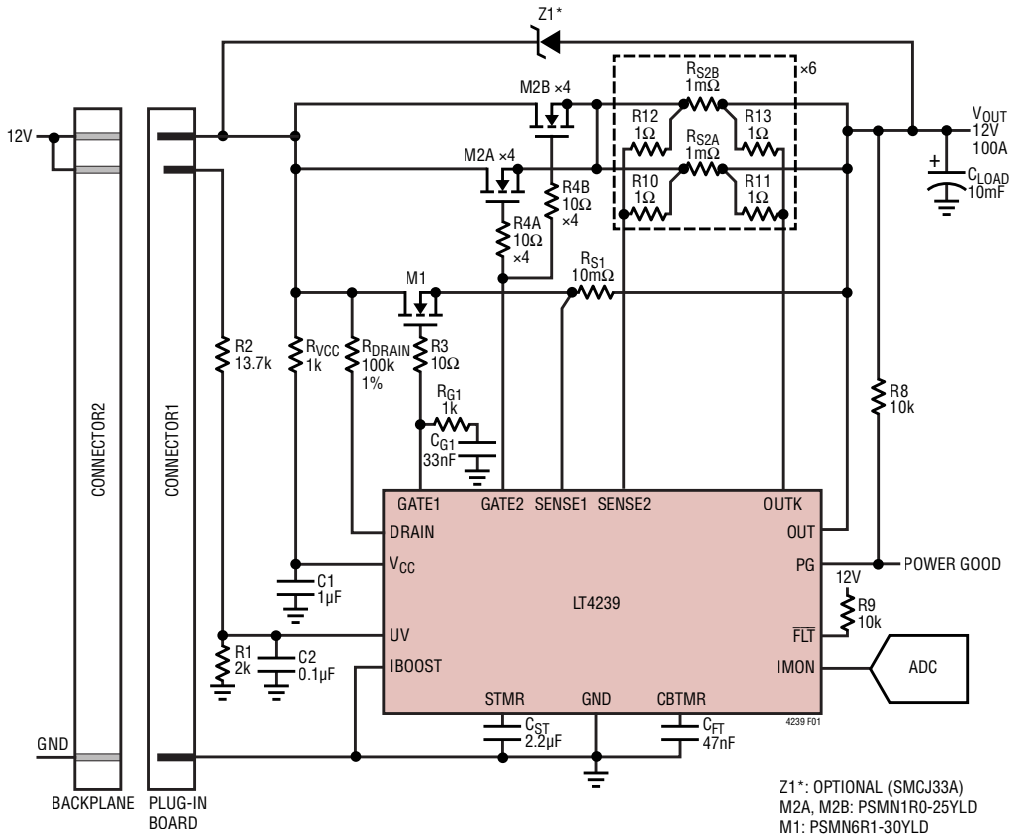


Figure 1. Typical Application

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Turn-On Sequence

Before the MOSFETs are turned on, the V_{CC} supply must exceed its 3.6V undervoltage lockout level. The N-Channel MOSFETs are then turned on in two stages with dual gate drive to pass the load current. When the input supply rises above the UV undervoltage threshold set by a R1/R2 divider, it initiates an internal 25ms debounce delay. During the debounce cycle, the external MOSFET's health is monitored at the MOSFET's drain and OUTK pin. If the voltage difference is less than 1.3V indicating a MOSFET's drain/source short, $\overline{FLT}$ will be pulled low at the end of the debounce cycle. Otherwise, the MOSFET M1 is turned on first by charging up GATE1 with a 10µA current source from the charge pump. Concurrently, STMR pin voltage will start ramping up with a 10µA current source. Connect a capacitor from STMR to GND to set the total allowed start-up time. The voltage at the GATE1 pin rises with a slope equal to $10\mu A/C_{G1}$ and the inrush current flowing into the load capacitor C_{LOAD} is limited to $(10\mu A/C_{G1}) \bullet C_{LOAD}$.

The OUT voltage follows GATE1 after M1 has reached its threshold voltage. If too small of C_{G1} is used, the current flowing through R_{S1} may become too high and reach the current limit, which triggers an internally set 100µs timer. When the timer expires, the $\overline{FLT}$ pin pulls low to indicate a fault condition. With appropriate C_{G1} selected, the current can be kept below the current limit allowing GATE1 to charge up turning on M1. When the gate drive for M1 exceeds 10V and the voltage difference between the MOSFET's drain and the OUTK pin is less than 1V, GATE2 charges up with a 50µA current source.

As GATE2 rises, M2 turns on when its threshold voltage is exceeded. When GATE2 is fully on and the voltage between the MOSFET's drain and the OUTK pin falls below 100mV, GATE1 pulls down to OUT turning off M1. The STMR pin is reset to ground by a 125µA current. A 10ms power-good timer is initiated while GATE2 continues to charge up until it is limited by the internal 12V clamp between GATE2 and OUT. At the end of the timer delay, the PG is released to pull high to indicate power is good and the load may be activated. The capacitance value at the STMR pin should be chosen such that the ramp-up period is long enough for GATE2 to be started up successfully without STMR reaching its fault threshold.

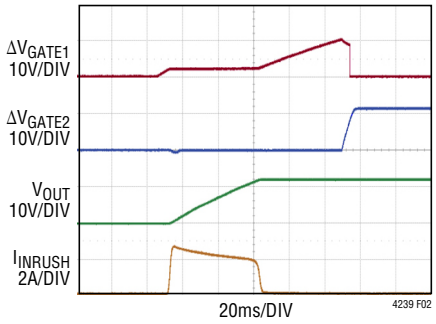

Figure 2. Normal Start-Up Waveforms

Turn-Off Sequence

A normal turn-off is initiated by pulling the UV pin below its 1.182V threshold (50mV hysteresis). The MOSFETs are turned off with 10mA currents pulling down the GATE pins to OUT. Additionally, several fault conditions can cause turn-off of the GATE pins. These include FET short and FET-Bad detection as well as an extended overcurrent condition either during start-up or after power good. During output overcurrent fault condition, GATE2 is pulled down to OUT with 50mA. When a severe output short is detected, either during inrush or normal operation period, a current source of 130mA or 600mA pulls GATE1 or GATE2, respectively to OUT. If the V_{CC} pin falls below its 3.6V undervoltage lockout threshold, both GATE1 and GATE2 pins are also pulled down to the OUT pin with 130mA and 600mA, respectively.

Constant Current Start-Up Using a GATE R-C Network

A R-C network must be used on the trickle MOSFET M1 for start-up. The series resistor and capacitor network from GATE1 to ground (R_{G1} and C_{G1} in Figure 1) limits the GATE1 slew rate and inrush current to less than the current limit. The internal 100µs fault timer will not run since the current limit is not engaged during start-up, which allows the use of MOSFET with smaller safe operating area for M1. R_{G1} should be chosen such that $I_{GATE1(UP)} \bullet R_{G1}$ is less than the MOSFET's threshold voltage to avoid a current spike at the beginning of start-up. Using a too small value for R_{G1} can degrade the stability of the current limit circuit. For proper operation, the value of R_{G1} should be $\geq 470\Omega$ and C_{G1} should be $\leq 100nF$.

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Parasitic MOSFET Oscillations

Not all circuit oscillations can be ascribed to the current limit loop. Some higher frequency oscillations can arise from the MOSFETs themselves. (See Rarely Asked Questions—Issue 151, High-Side Current Sensing). There are two possible parasitic oscillation mechanisms. The first type of oscillation occurs at high frequencies, typically above 1MHz. This high frequency oscillation is easily damped with gate resistors R3 and R4 as shown in Figure 1. In some applications, one may find that these resistors help in short-circuit transient recovery as well. However, too large of a resistor will slow down the turn-off time. The recommended range for R3 and R4 is between 5Ω and 500Ω. 10Ω provides stability without affecting turn-off time. These resistors must be located next to the MOSFET gate pin with no other connections between them. Connect each of the gate resistors to every MOSFET when several MOSFETs are connected in parallel.

A second type of parasitic oscillation occurs at frequencies between 200kHz and 800kHz when the MOSFET source is loaded with less than 10µF, and the drain is fed with an inductive impedance such as contributed by wiring inductance. To prevent this second type of oscillation, load the source with more than 10µF and bypass the input supply with a series 10Ω, 100nF snubber to ground.

Overcurrent Fault During GATE1 Start-Up

The LT4239 features an active current limit to protect the MOSFET M1 against short circuits or excessive current during start-up. A rail-to-rail active current limit (ACL) amplifier monitors the voltage across the sense resistor R_{S1} which is located on the source side of the MOSFET M1. When an overcurrent event appears, the ACL amplifier regulates the gate of the MOSFET to maintain 50mV across the sense resistor. At this point, an internal fault timer runs for 100µs until it times out. The MOSFET is turned off with GATE1 pulled to OUT by 10mA, and the fault latched-off with the $\overline{FLT}$ pin pulling low.

In the event of a severe short-circuit fault occurring during start-up, the output current can momentarily surge to tens of amperes. The LT4239 responds within 1µs to bring the current under control by pulling the GATE1 to OUT. Almost immediately, the gate of the MOSFET M1 recovers due to the R_{G1} and C_{G1} network, and the current is actively limited until the 100µs fault timer expires.

Overcurrent Fault After Power Good

Once the load capacitor is fully charged up through MOSFET M1 after GATE1 start-up, MOSFET M2 will be turned on to pass the load current in the power path. There are three mechanisms to protect MOSFET M2 from damage when an overcurrent event develops after power good. The first one is the electronic circuit breaker (ECB) with an adjustable timer. The second is the active current limit (ACL) while the last one is a comparator detecting the output falling below 3.7V.

An accurate electronic circuit breaker (ECB) and an active current limit (ACL) amplifier monitor the voltage across the sense resistor R_{S2} which is located on the source side of MOSFET M2. The electronic circuit breaker will turn off the MOSFET if the voltage across the sense resistor exceeds the ECB threshold $\Delta V_{SENSE2(CB)}$ (10mV) for longer than the fault filter delay configured at the CBTMR pin. The fault filter starts the timeout with a 10µA current charging the CBTMR pin capacitor. Otherwise, it discharges with 10µA if the sense voltage falls below the ECB threshold. If the CBTMR pin voltage exceeds its 1.232V threshold, the MOSFET turns off with GATE2 pulled to OUT by 50mA, and the fault is latched-off with the $\overline{FLT}$ pin pulling low. For a given circuit breaker time delay, t_{CB}, the value for setting the external capacitor C_{FT} is given by Equation 1.

$$C_{FT} = t_{CB} \bullet 0.008[\mu F/ms] \quad (1)$$

After the MOSFET turns off, the CBTMR pin capacitor is discharged with a 4µA pull-down current until its threshold reaches 0.2V. This is followed by a cool-off cycle whereby the CBTMR pin will cycle up and down with 10µA and 4µA 512 times to allow the MOSFET to cool down. When configured in a circuit shown in Figure 8 for auto-retry, the resulting overcurrent duty cycle is 1:1280. During the cool-off period, the $\overline{FLT}$ pin remains low, and the output cannot be restarted by pulling the UV pin below 0.6V.

Active current limiting begins when the sense voltage exceeds the ACL threshold $\Delta V_{SENSE2(ACL)}$ (15mV), which is 1.5 times the ECB threshold $\Delta V_{SENSE2(CB)}$. The ACL

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amplifier regulates the gate of the MOSFET to maintain the ACL threshold across the sense resistor. At this point, an internal fault timer runs for 100µs until it times out. The MOSFET is turned off with GATE2 pulled to OUT by 50mA, and the $\overline{FLT}$ pin also pulls low.

In the event of a severe short-circuit fault on the 12V output after power good, the output current can rapidly surge. If the fast comparator threshold $\Delta V_{SENSE2(FAST)}$ (40mV) is exceeded, the LT4239 responds within 1µs to bring the current under control by pulling GATE2 to OUT without latching off the fault. If the OUT voltage falls below 3.7V, GATE2 will also be pulled down to OUT quickly to turn off the MOSFET and the fault is latched-off with the $\overline{FLT}$ pin pulling low. All the overcurrent faults will activate the cool-off cycle for the MOSFETs to cool down before the output can be restarted.

The waveforms in Figure 3 show how the output turns off following an overcurrent fault after power good.

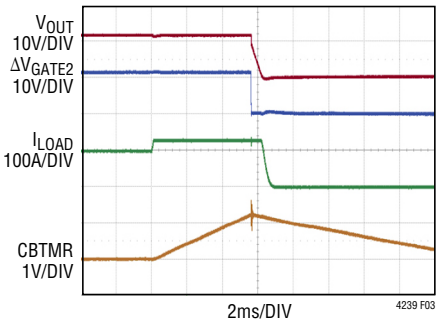

Figure 3. Overcurrent Fault After Power Good

Undervoltage Fault

The UV pin functions as a turn-on control and input supply monitor. A resistive divider connected between the supply input and GND at the UV pin monitors the supply for an undervoltage condition. The undervoltage threshold is set by proper selection of the resistors at the UV rising threshold voltage (1.232V). For Figure 1, if R1 = 2k, R2 = 13.7k, the input supply undervoltage threshold is set to 9.7V.

An undervoltage fault occurs if the input supply falls below its undervoltage threshold. If the UV pin voltage falls below 1.182V for longer than 270µs but remains above 0.6V, the MOSFETs are turned off by a 10mA pull-down current from both GATE1 and GATE2 to OUT. However, if the UV pin voltage drops below 0.6V, it turns off the MOSFETs and clears the fault latch. The GATE1 can start up again only after a debounce delay when the input supply is restored above its undervoltage threshold.

During the undervoltage fault condition, $\overline{FLT}$ will not be pulled low, but PG will be pulled low as both GATE pins are pulled low.

FET-Bad Fault

In a Hot Swap application, several possible faults can prevent the MOSFETs from turning on and reaching a low impedance state. A damaged MOSFET may have leakage from gate to drain or have degraded $R_{DS(ON)}$. Debris on the board may also produce leakage or a short-circuit from the MOSFET's gate to the source, the drain, or to ground.

Under these conditions, the LT4239 may not be able to pull the GATE pins high enough to fully enhance the MOSFETs. If GATE1 or GATE2 voltage fail to reach their 10V thresholds above OUT when the STMR voltage reaches its 1.232V threshold, a start-up fault condition is generated. $\overline{FLT}$ pin will be pulled low, and the GATE pins are pulled down to OUT with a 10mA current source. A start-up fault will not activate the 512 timing cycles at CBTMR pin for MOSFET cool-off.

If FET-Bad conditions occur after the load is turned on, the MOSFET M2 may not reach the intended $R_{DS(ON)}$ when the GATE2 drive is fully enhanced. This can put the MOSFET in a condition where the power in the MOSFET is higher than its continuous power capability, even though the current is below the current limit. The LT4239 monitors the integrity of the MOSFET M2 in two ways, and acts on them in the same manner.

First, the LT4239 monitors the voltage between the MOSFET's drain and the OUTK pin that include the sense resistor drop. A bad M2 MOSFET's Drain-to-Source voltage is detected if the voltage is greater than the 100mV FET-Bad fault threshold.

Second, the LT4239 monitors the GATE2 voltage. A damaged MOSFET may cause the GATE2 voltage to fall due to a resistive short from the gate to either the source or drain

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terminals. If the GATE2 drive falls below its 10V threshold, a FET-Bad condition is detected.

When either FET-Bad condition is present, an internal 20ms FET-Bad fault timer will be activated. The timer resets whenever the FET-Bad condition disappears. After the timer expires, the $\overline{FLT}$ pin pulls low and the GATE2 is pulled down to OUT with a 10mA current. A FET-Bad fault detection can only be cleared by lowering the V_{CC} below its 3.6V undervoltage lockout threshold.

FET Short Fault

The LT4239 monitors the integrity of the MOSFETs during the debounce cycle. A FET short fault is detected if the voltage between the MOSFET's drain and OUTK pin remains below 1.3V at the end of the 25ms debounce cycle. The $\overline{FLT}$ pin will be pulled low after the debounce cycle. The LT4239 will enter a cool-off period of 512 timing cycles before the fault is cleared and the part can restart.

Resetting Faults

Faults generated during start-up or after power good will cause the LT4239 to latch-off and $\overline{FLT}$ pin to be pulled low. Pulling the UV pin below 0.6V will reset the latched fault. If UV is pulled low during the cool-off period, it will not reset the fault. But if UV continues to stay low until the cool-off cycle is over, the fault will be reset at the end of the cool-off period. If UV is pulled low after the cool-off period, it will reset the fault instantly. When UV goes high again after the fault latch is cleared, a debounce timing cycle is initiated followed by GATE1 start-up.

The LT4239 can be configured for auto-retry by tying the $\overline{FLT}$ to UV in a circuit shown in Figure 8. Whenever the $\overline{FLT}$ pin is pulled low due to a fault, the UV pin will also be pulled below 0.6V to reset the fault latch. For faults that are followed by a cool-off cycle, the output will only restart again at the end of the cool-off period when the fault resets. However, for faults that don't trigger the cool-off cycle, the fault will be reset instantly allowing the debounce timing cycle to restart. There is an exception for a FET-Bad fault detected after power good, the $\overline{FLT}$ pin will remain low prohibiting the debounce timing cycle from starting.

Lowering the input supply until the V_{CC} falls below its undervoltage lockout threshold (3.6V) shuts off all the MOSFETs and resets the fault latch. That includes resetting the fault while the device in cool-off cycle.

Using IBOOST to Double the Circuit Breaker and Current Limit Thresholds

The IBOOST pin can be used to double the circuit breaker, current limit thresholds and the FET-Bad fault threshold to ride through load surges after power good. It doesn't increase the current limit threshold of the start-up channel. Pulling the IBOOST pin above 1.6V will double those thresholds allowing large current to pass through the pass transistors without generating a fault. However, higher current limit settings will result in higher MOSFET power dissipation in the event of an output short. Proper choice of the MOSFET must accommodate high power dissipation under the worst-case short-circuit if the IBOOST pin function is used.

Monitor MOSFET Current

The current through the sense resistor R_{S2} is monitored by LT4239's current sense amplifier at the SENSE2 and OUTK pins. See Figure 4. The sense amplifier is supplied from the OUT voltage that must be greater than 3.7V for the IMON output to be valid. An internal resistor R_{IN} of 200Ω is connected between the amplifier's negative input terminal and SENSE2 pin. Another internal resistor R_{OUT} of 20k is connected between the IMON and GND pins. The IMON output voltage is equal to $(R_{OUT}/R_{IN}) \bullet V_{SENSE}$. The resistor ratio R_{OUT}/R_{IN} defines the voltage gain of the sense amplifier and is set to 100. Full scale input sense voltage to the sense amplifier is 30mV, corresponding to an output of 3V at IMON pin. For input supply voltage greater than 5V, the output clamps at 4.9V if the allowable input sense voltage range is exceeded. The IMON pin is held at ground potential if the OUT voltage is less than 3.7V.

A capacitor connected from the IMON pin to GND will reduce noise at the output and may also be useful as a charge reservoir to keep the pin steady while driving a switching circuit such as an ADC.

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Supply Transients

In card-resident applications, an output short-circuits working against the inductive nature of the supply can cause the input to collapse almost to ground resulting in supply brown-out. The architecture of the LT4239 allows a simple RC filter to be connected at the V_{CC} pin to preserve the supply voltage not falling below its undervoltage lockout threshold when the event happens. Meanwhile, the LT4239's fast comparator begins to engage and turn off the MOSFETs in less than 1µs once the short-circuit current through the sense resistor rises above its trip threshold. When that happens, the input supply voltage rapidly recovers and overshoots to a very high value due to inductive kick. With the RC filter connected damping the transient spikes, the V_{CC} pin is protected from damage. This removes the need for a transient voltage suppressor (TVS) connected from V_{CC} to GND. Without the help of a TVS at the input, the voltage spikes can rise to a level causing the MOSFET to breakdown and discharge the inductor energy to the output. The MOSFET can be damaged if the specified avalanche current or energy is exceeded. A TVS (Z1) across the MOSFET can be added from supply input to output for more protection. See Figure 1.

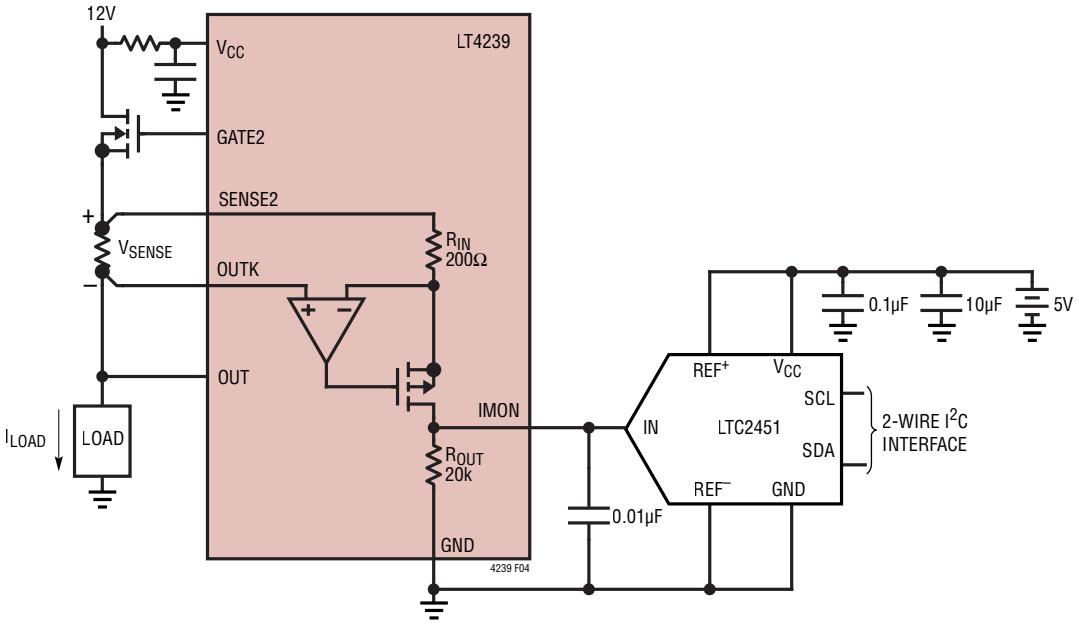

Figure 4. Low Side Current Monitor with LTC2451 ADC

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Design Example

As a design example, consider the following specifications: V_{IN} = 12V, $I_{LOAD(MAX)}$ = 100A, C_{LOAD} = 10mF and V_{UV} = 9.7V, using a trickle MOSFET with current limit set at 50mV for start-up and a group of parallel MOSFETs with current limit set at 10mV for load current conduction (see Figure 1).

First, select the appropriate value of the current sense resistors R_{S1} and R_{S2}. Calculate R_{S2} value based on the maximum load current $I_{LOAD(MAX)}$ and the lower limit for the circuit breaker trip threshold $\Delta V_{SENSE2(CB)(MIN)}$ (see Equation 2).

$$R_{S2} = \frac{\Delta V_{SENSE2(CB)(MIN)}}{I_{LOAD(MAX)}} = \frac{9.5mV}{100A} = 0.095m\Omega \quad (2)$$

As the sense resistor value is very low, several larger value sense resistors are connected in parallel to improve the sensing accuracy and keep the power dissipation within limits. In this design, 12 parallel sense resistors of 1mΩ value with 1% tolerance are used for R_{S2}.

To achieve the specific resistance with the parallel sense resistors, the averaging resistors, R_A, should be selected with the same ratio, k, as the sense resistors they connect to. See Figure 5. This allows the current limit circuit to measure the correct sense voltage for this effective sense resistor. The smallest averaging resistor should not exceed 1Ω.

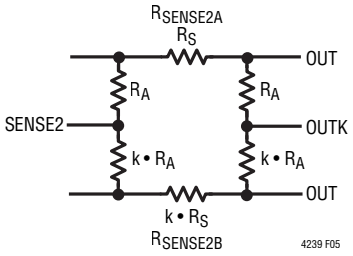

Figure 5. Weighted Averaging Sense Voltages

Next, calculate the R_{S1} value based on the inrush current I_{INRUSH} and the lower limit for the current limit threshold $\Delta V_{SENSE1(ACL)(MIN)}$. The inrush current is set to 4A to fully charge 10mF of C_{LOAD} to 12V in 30ms. A capacitor, C_{G1}, is added to the gate of M1 to achieve the inrush current (Equation 3).

$$C_{G1} = \frac{C_{LOAD} \bullet I_{GATE1(UP)}}{I_{INRUSH}} = \frac{10mF \bullet 10\mu A}{4A} = 25nF \quad (3)$$

Choose a practical value of 33nF with 10% tolerance for C_{G1} (Equation 4).

$$R_{S1} = \frac{\Delta V_{SENSE1(ACL)(MIN)}}{I_{INRUSH}} = \frac{45mV}{4A} = 11m\Omega \quad (4)$$

Choose a 10mΩ sense resistor with 1% tolerance for R_{S1}.

The MOSFET M1 is selected to handle the power dissipation during inrush when load capacitor C_{LOAD} is being charged at power up. The method to determine the power dissipation is based on the principle that the energy dissipated in the MOSFET is the same as the energy stored in the load capacitor, and is given by Equation 5.

$$E_{CL} = \frac{1}{2} C_{LOAD} V_{IN}^2 = \frac{1}{2}(10mF)(12V)^2 = 0.72J \quad (5)$$

Calculate the time it takes to charge C_{LOAD} (Equation 6).

$$t_{CHARGE} = \frac{C_{LOAD} \bullet V_{IN}}{I_{INRUSH}} = \frac{10mF \bullet 12V}{4A} = 30ms \quad (6)$$

Use Equation 7 to calculate the average power dissipated in the MOSFET M1.

$$P_{DISS} = \frac{E_{CL}}{t_{CHARGE}} = \frac{0.72J}{30ms} = 24W \quad (7)$$

The SOA (Safe Operating Area) curves of the selected MOSFET must be evaluated to ensure that the thermal capacity of the package tolerates 24W for 30ms. The SOA curve of the PSMN6R1-30YLD shows 30W (3A at 10V) for 100ms, satisfying this requirement.

If the circuit starts up into an output-short, the short-circuit current will be limited for 100µs before the fault is latched-off. Use Equation 8 to calculate the maximum short-circuit current using the maximum active current limit threshold, $\Delta V_{SENSE1(ACL)(MAX)}$ and minimum R_{S1} value.

$$I_{SHORT1(MAX)} = \frac{\Delta V_{SENSE1(ACL)(MAX)}}{R_{S1(MIN)}} = \frac{55mV}{9.9m\Omega} = 5.6A \quad (8)$$

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Thus, the maximum power dissipated in the MOSFET M1 during active current limiting is 5.6A • 12V = 67.2W for 100µs. The SOA curve of the PSMN6R1-30YLD shows 500W (50A at 10V) for 100µs, satisfying this requirement.

The start-up timer capacitor (C_{ST}) determines the total time allowed for a successful startup from the completion of the debounce to the start of the PG timer. For the STMR ramp-up time of 200ms which is 2 times longer than the time before the PG timer starts (Equation 9).

$$C_{ST} = 200ms \bullet 0.008[\mu F/ms] \cong 1.6\mu F \quad (9)$$

Since the MOSFET M2 turns on only after the load capacitor is fully charged through M1, the MOSFET is selected to handle the power dissipation during active current limiting for 100µs.

Use Equation 10 to calculate the maximum short-circuit current using the maximum active current limit threshold, $\Delta V_{SENSE2(ACL)(MAX)}$ and minimum R_{S2} value where there are 12 parallel 1mΩ sense resistors for R_{S2}.

$$I_{SHORT2(MAX)} = \frac{\Delta V_{SENSE2(ACL)(MAX)}}{R_{S2(MIN)}/12} = \frac{17mV}{0.99m\Omega/12} = 206A \quad (10)$$

If the output is shorted to a voltage below 3.7V, the MOSFET M2 will be turned off instantly without active current limiting and the fault is latched-off. Thus, the maximum power dissipated in the MOSFET during active current limiting if the 12V output collapsed to 4V is 206A • (12V – 4V) = 1648W for 100µs. Though the MOSFETs operate in parallel during active current limiting, they only provide the SOA of a single MOSFET due to offset mismatch between the gate thresholds. The MOSFET with the lowest threshold may carry more current than the others and as it gets hotter, it carries even more current since threshold voltage has a negative temperature coefficient. The SOA curve of the PSMN1R0-25YLD shows 2500W (250A at 10V) for 100µs, satisfying this requirement.

Another selection criterion is to use a smaller $R_{DS(ON)}$ of 1mΩ or less for the MOSFET to minimize the voltage drop keeping the power dissipation within limits at maximum load current. In the design, eight MOSFETs in parallel are used to reduce the dissipated power in each MOSFET. The effective $R_{DS(ON)}$ is kept low enough to avoid triggering the FET-Bad fault threshold.

The fault timer capacitor (C_{FT}) at CBTMR pin is used to prevent power dissipation in the MOSFET M2 from exceeding its SOA rating during an overcurrent fault. Use Equation 11 to calculate the worst-case short-circuit current during the fault timer period before active current limiting is activated.

$$I_{SHORT2(WORST)} = \frac{\Delta V_{SENSE2(ACL)(MAX)} - \Delta V_{SENSE2(CB)(MIN)}}{R_{S2(MIN)}/12}$$
$$I_{SHORT2(WORST)} = \frac{17mV - 9.5mV}{0.99m\Omega/12} = 91A \quad (11)$$

Assuming the short-circuit current is divided equally amongst the eight parallel MOSFETs, the maximum power dissipated in each MOSFET during the fault timer period if the 12V output collapsed to 4V is (91A/8) • (12V – 4V) = 91W. The SOA curve of the PSMN1R0-25YLD shows 200W (20A at 10V) for 10ms.

The MOSFET's SOA rating requirement is satisfied for a fault timer period of 5ms (Equation 12).

$$C_{FT} = 5ms \bullet 0.008[\mu F/ms] \cong 47nF \quad (12)$$

Finally, select the values for the resistive voltage divider at the UV pin that defines the undervoltage threshold of 9.7V for the 12V supply. Since the leakage current for the UV pin can be as high as ±1µA, the total resistance in the divider should be low enough to minimize the resulting offset error. Calculate the bottom resistor R1 based on Equation 13 to obtain less than ±0.2% error due to leakage current.

$$R1 = \left(\frac{V_{UV(TH)}}{I_{(LEAK)}}\right) \bullet 0.2\% = \left(\frac{1.232V}{1\mu A}\right) \bullet 0.2\% = 2.4k \quad (13)$$

Choose R1 to be 2kΩ to achieve less than ±0.2% error and then solving Equation 14 for R2, results in R2 = 13.7kΩ.

$$R2 = \left(\frac{V_{IN(UV)}}{V_{UV(TH)}} - 1\right) \bullet R1$$
$$R2 = \left(\frac{9.7V}{1.232V} - 1\right) \bullet 2k = 13.7k \quad (14)$$

A 0.1µF capacitor C2 is placed on the UV pin to prevent supply glitches from turning off the MOSFETs.

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In addition, a resistor R_{DRAIN} of 100kΩ with1% tolerance is placed on the DRAIN pin for sensing the MOSFET's drain voltage accurately. A RC filter consisting of a 1kΩ resistor and a 1µF ceramic bypass capacitor is also placed on the V_{CC} pin so that TVS is not required from the input supply to ground.

Layout Considerations

To achieve accurate current sensing, Kelvin connections for the sense resistors are required. The PCB layout of Kelvin sensing traces should be balanced and symmetrical to balance the parasitics on the PCB. Even with a good PCB layout, it is necessary to use a resistor network to average the voltages sensed across the individual parallel sense resistors. In the 12V/100A application shown in Figure 11, the SENSE2 and OUTK pins of the LT4239 are joined to the six 0.5mΩ sense resistors with an array of 1Ω resistors. The resulting voltage between the SENSE2 and OUTK pins is the average of all the voltages across the 0.5mΩ sense resistors, effectively Kelvin sensing the six 0.5mΩ resistors. The same arrangement can also be expanded for Kelvin sensing twelve 1mΩ resistors. The Kelvin sensing connection from R_{S1} 10mΩ is not connected to OUTK so as not to affect the effective sense resistance between the SENSE2 and OUTK pins. A recommended PCB layout is shown in Figure 6.

The PCB traces associated with the power path through the MOSFETs should have low resistance. The suggested trace width for 2oz copper foil is 0.01-inch per ampere or wider to keep PCB trace resistance, voltage drop, and temperature rise to a minimum. Note that 2oz copper foil exhibits a sheet resistance of about 0.25mΩ/square. Small resistances add up quickly in high current applications.

To improve noise immunity, place the resistive divider to the UV pin close to the device and keep traces to supply input and GND short. It is also important to place the bypass capacitor C1 as close as possible between V_{CC} and ground. A 0.1µF capacitor C2 from the UV pin to ground also helps reject supply noise. The 100kΩ resistor R_{DRAIN} for monitoring the MOSFET's drain voltage should also be placed near the DRAIN pin. If a surge suppressor, Z1, is used, it should be placed between the IN and OUT using wide traces.

Try to avoid placing the ground plane immediately under the power MOSFETs. If the MOSFETs fail and overheat, that could result in a catastrophic failure as the input supply gets shorted to ground when the insulation between them fails.

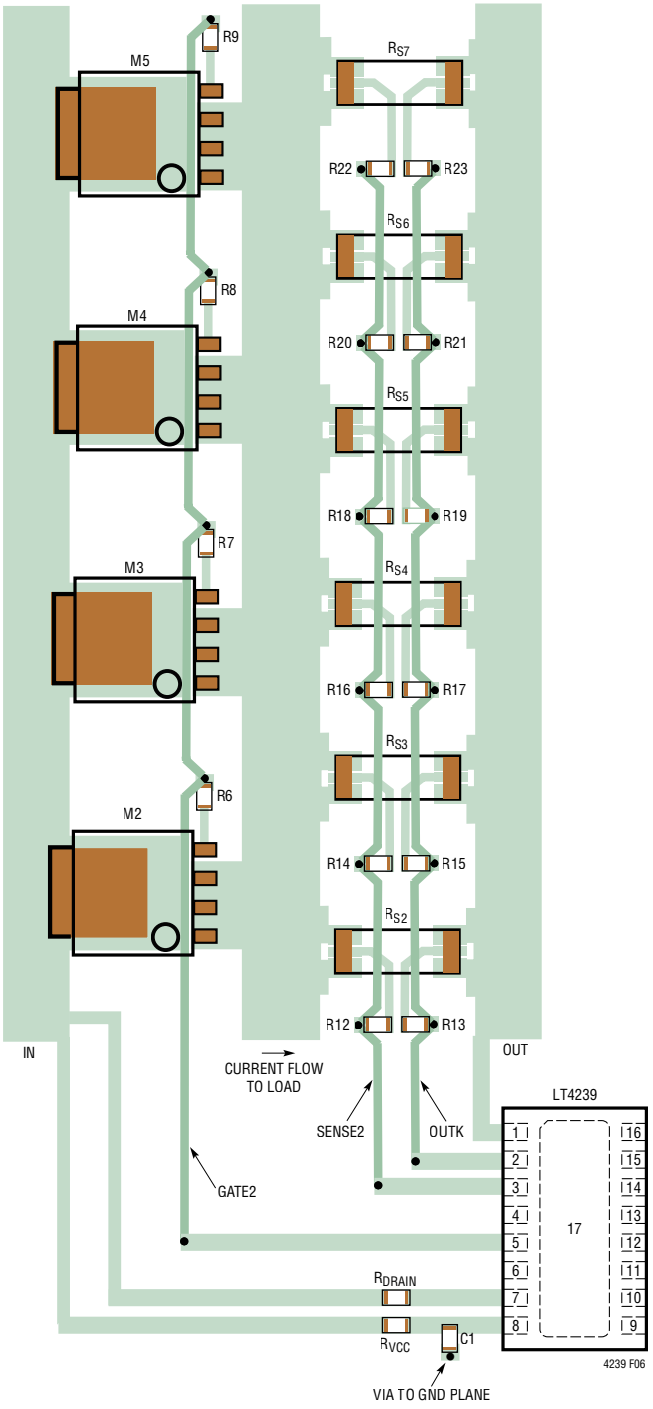


Figure 6. Recommended Layout

TYPICAL APPLICATIONS

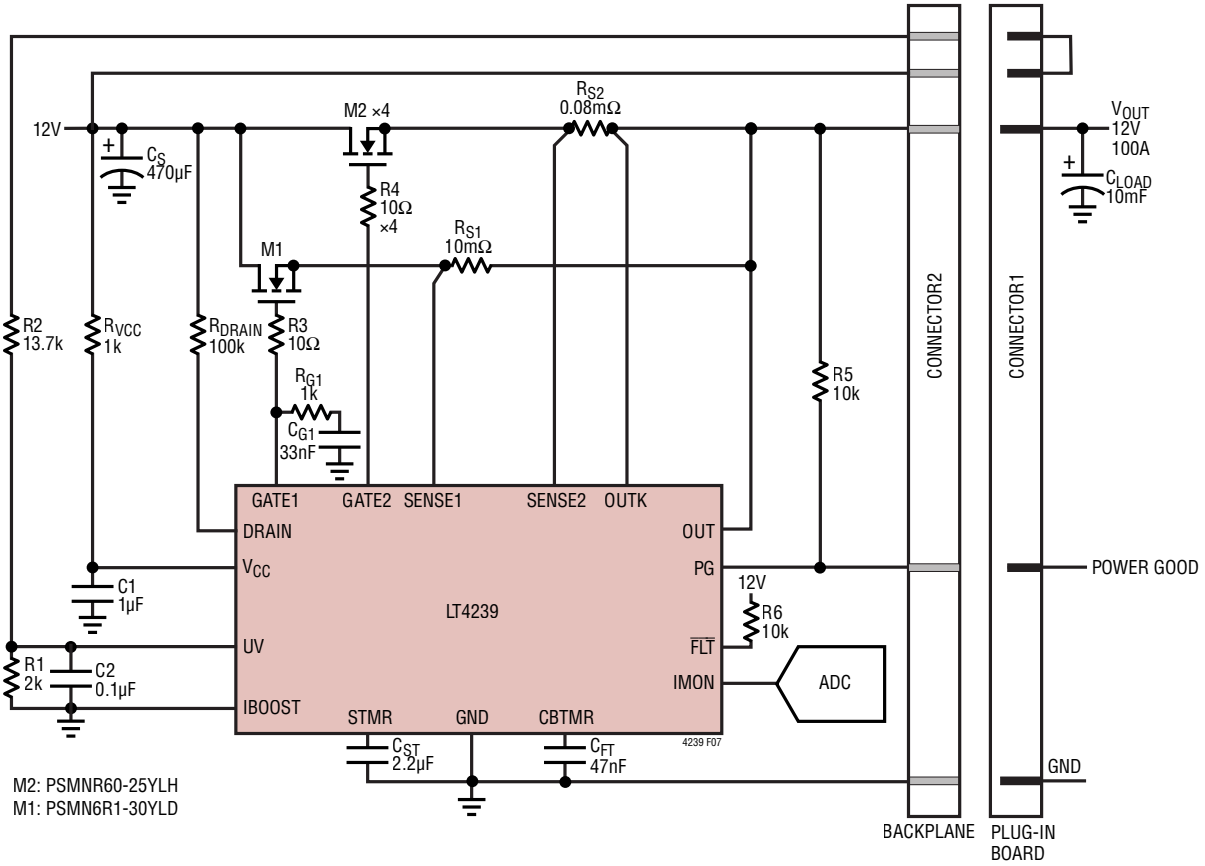


Figure 7. 12V, 100A Backplane Resident Application

TYPICAL APPLICATIONS

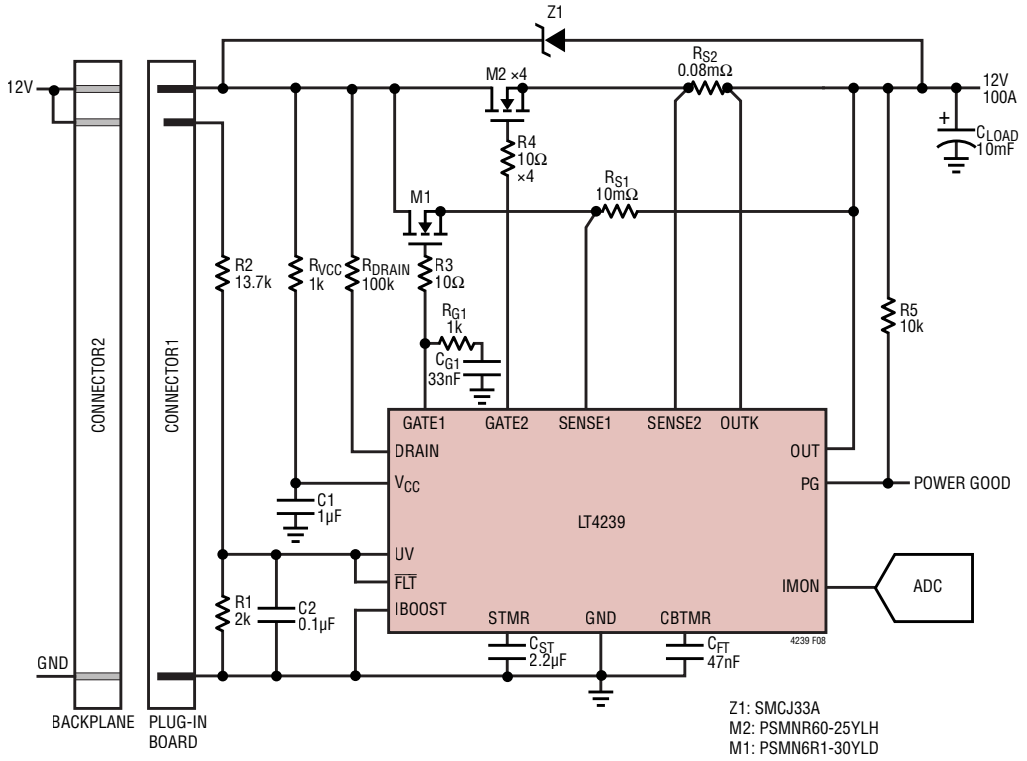


Figure 8. 12V, 100A Application with Auto-Retry After a Fault

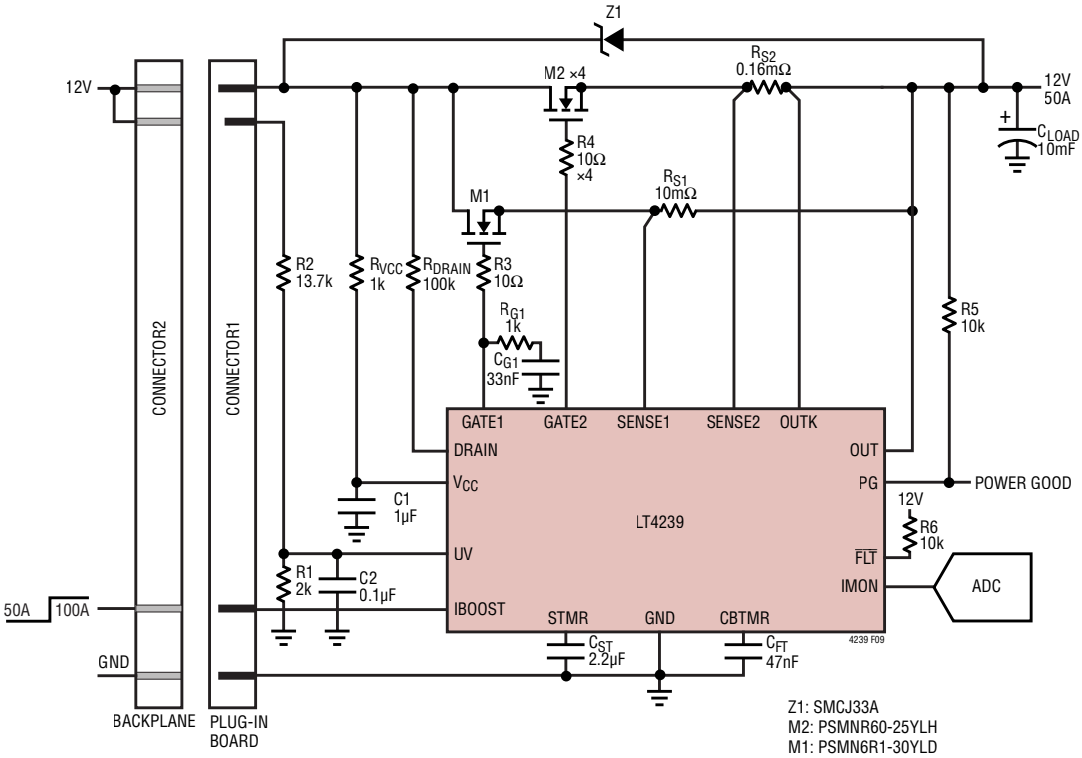


Figure 9. 12V, 50A Application with IBOOST Pin Control

TYPICAL APPLICATIONS

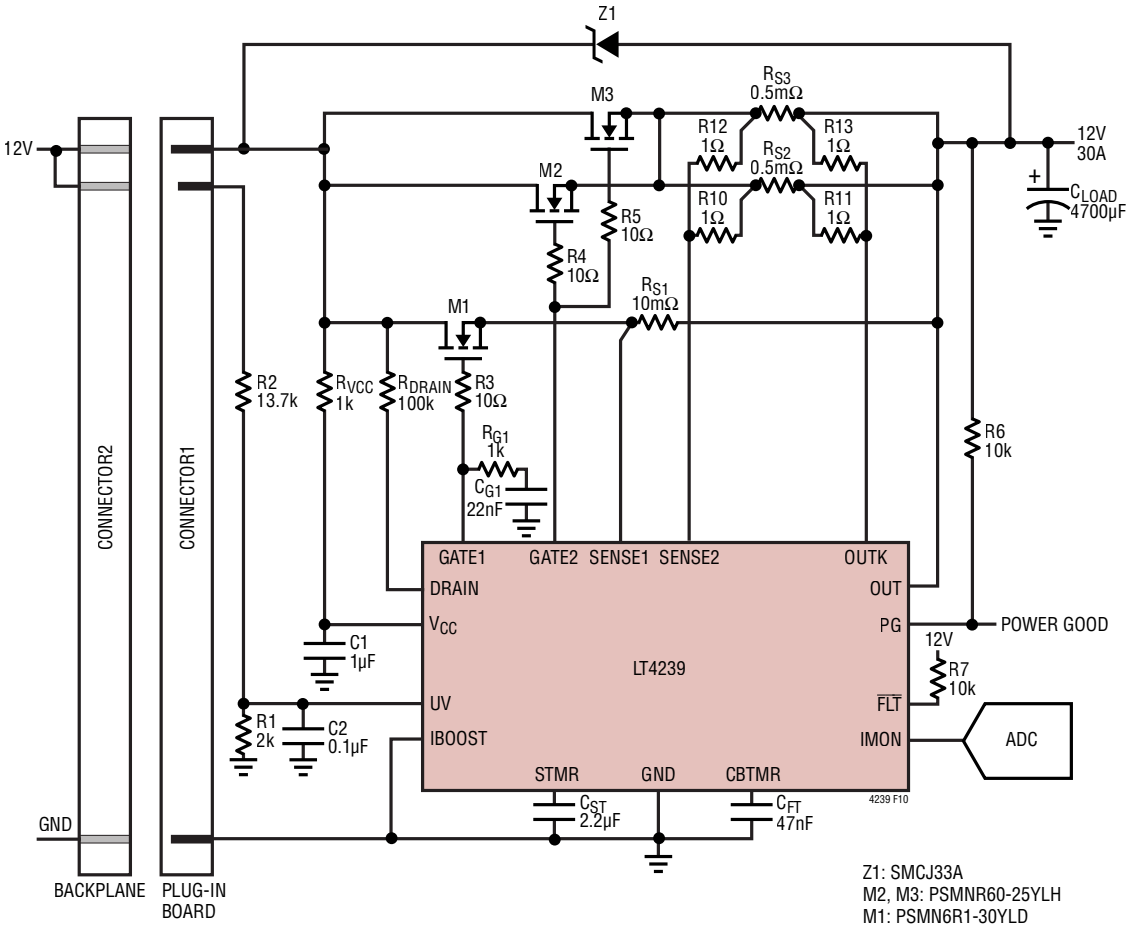


Figure 10. 12V, 30A Card Resident Application

TYPICAL APPLICATIONS

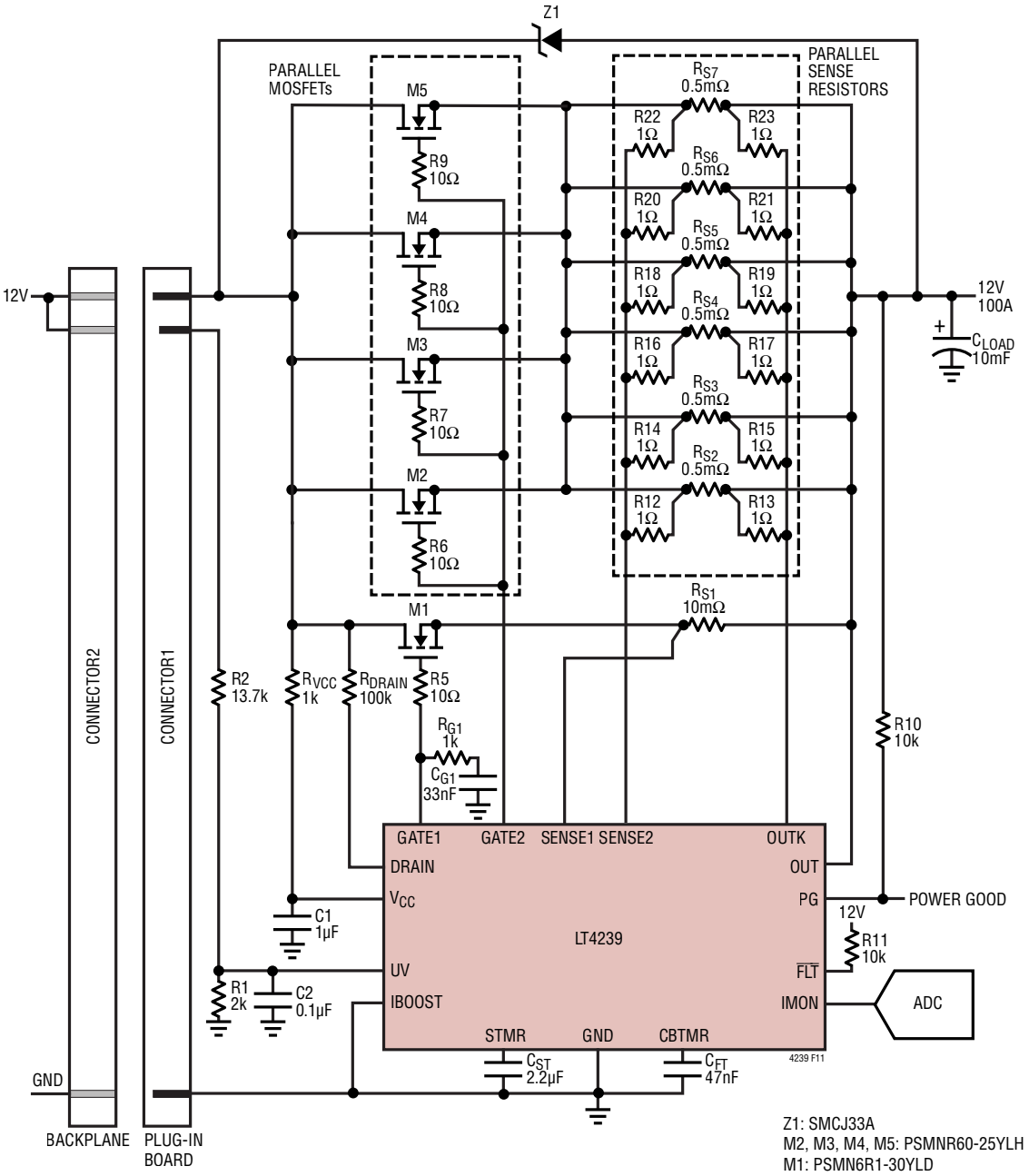
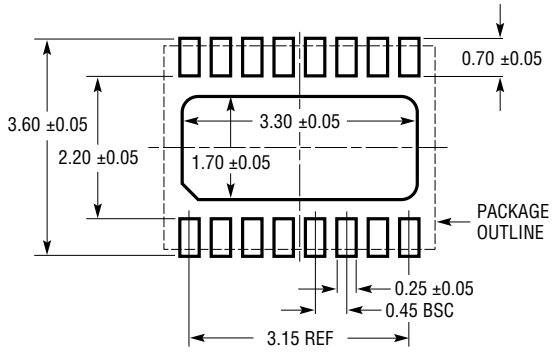


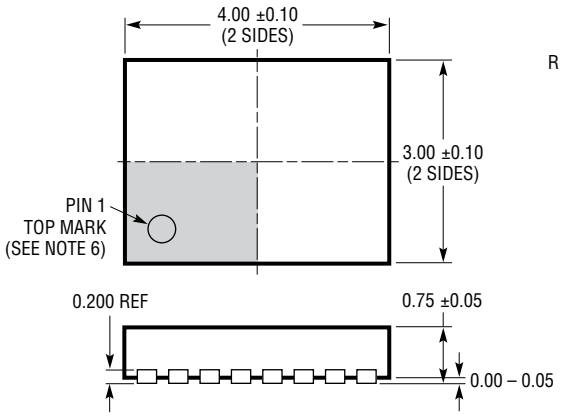
Figure 11. 12V, 100A Application with Parallel MOSFETs and Current Sense Resistor Averaging Network

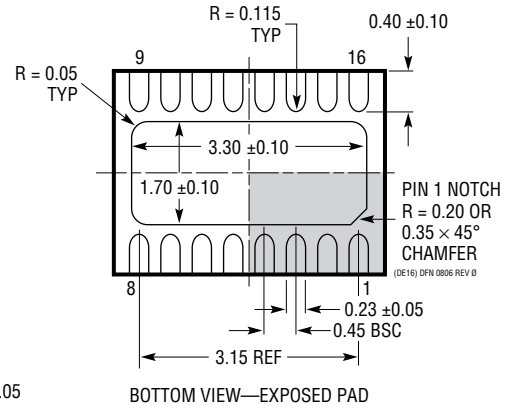
PACKAGE DESCRIPTION

DE Package
16-Lead Plastic DFN (4mm × 3mm)
(Reference LTC DWG # 05-08-1732 Rev Ø)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED





BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING PROPOSED TO BE MADE VARIATION OF VERSION (WGED-3) IN JEDEC PACKAGE OUTLINE MO-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE