Positive High Voltage Hot Swap Controller with Open-Circuit Detect

FEATURES

- **Allows Safe Board Insertion and Removal from a Live Backplane**
- **Controls Supply Voltage from 10.8V to 80V**
- **Foldback Current Limiting**
- **Open Circuit and Overcurrent Fault Detect**
- Drives an External N-Channel MOSFET
- Automatic Retry or Latched Off Operation After Overcurrent Fault
- Programmable Supply Voltage Power-Up Rate
- Open MOSFET Detection
- 1% Over and Undervoltage Detection Accuracy
- Available in a 16-Lead SSOP Package

APPLICATIONS

- Hot Board Insertion
- Electronic Circuit Breaker/Power Bussing
- Industrial High Side Switch/Circuit Breaker
- 24V/48V Industrial/Alarm Systems
- Ideally Suited for 12V, 24V and 48V Distributed Power Systems
- 48V Telecom Systems

DESCRIPTION

The LT®4256-3 is a high voltage Hot Swap™ controller that allows a board to be safely inserted and removed from a live backplane. An internal driver controls the high side N-channel MOSFET gate for supply voltages ranging from 10.8V to 80V. The part features an open-circuit detect (OPEN) output that indicates abnormally low load current conditions.

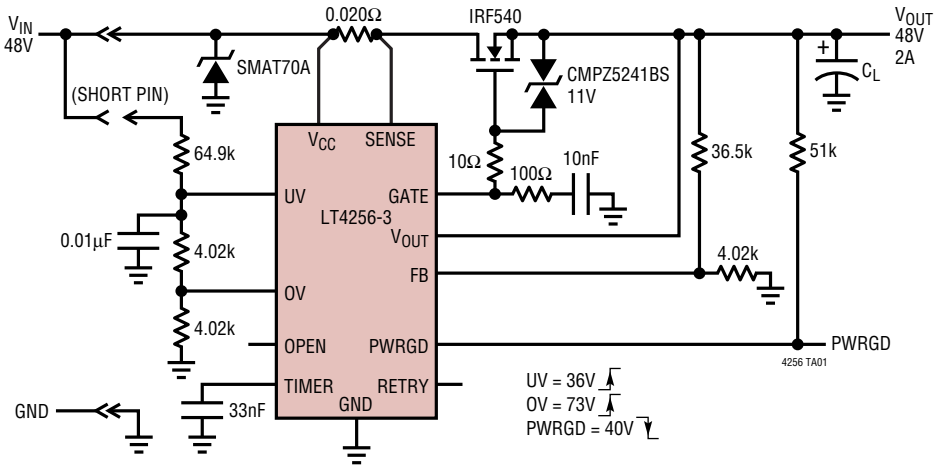
The LT4256-3 also features an adjustable analog foldback current limit. If the supply remains in current limit for more than a programmable time, the N-channel MOSFET shuts off, the PWRGD output asserts low and the LT4256-3 either automatically restarts after a time-out delay or latches off until the UV pin is cycled low (depending on the status of the RETRY pin).

The PWRGD output indicates when the output voltage rises above a programmed level. An external resistor string from V_{CC} provides programmable undervoltage and overvoltage protection.

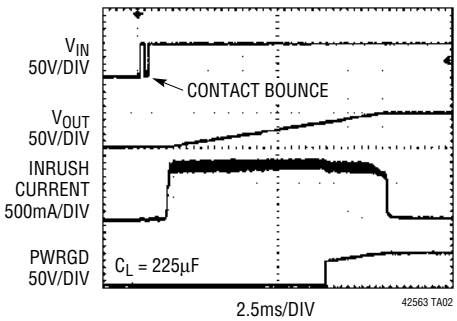
The LT4256-3 is available in a 16-lead SSOP package.

TYPICAL APPLICATION

48V, 2A Hot Swap Controller



LT4256-3 Start-Up Behavior

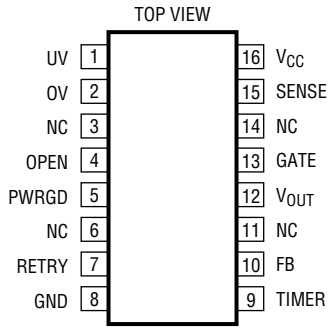


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage (V_{CC}) ..... –0.3 to 100V
SENSE, PWRGD ..... –0.3 to 100V
GATE Voltage (Note 2) ..... –0.3V to V_{CC} + 10V
GATE Maximum Current 200µA
V_{OUT} ..... –3V to 100V
FB, UV, OPEN ..... –0.3 to 44V
OV ..... –0.3 to 18V
RETRY ..... –0.3 to 15V
TIMER Voltage ..... –0.3V to 4.3V
Maximum Input Current (TIMER) 100µA
Operating Temperature
LT4256-3C ..... 0°C to 70°C
LT4256-3I ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



GN PACKAGE
16-LEAD PLASTIC SSOP
T_{JMAX} = 125°C, θ_{JA} = 130°C/W

ORDER PART NUMBER
LT4256-3CGN LT4256-3IGN
GN PART MARKING
42563 42563I

Order Options Tape and Reel: Add #TR
Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: http://www.linear.com/leadfree/

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Note: NC is a pin that is "Not Connected."

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 48V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC}	Operating Voltage		●	10.8		80	V
I_{CC}	Operating Current				1.8	3.9	mA
V_{UVLH}	Undervoltage Threshold	V_{CC} Low-to-High Transition	●	3.96	4	4.04	V
V_{UVHYS}	Hysteresis			0.25	0.4	0.55	V
I_{INUV}	UV Input Current	UV ≥ 1.2V UV = 0V			–0.1 –1.5	–1 –3	µA µA
V_{UVRTH}	Fault Latch Reset Threshold Voltage		●	0.4	0.85	1.2	V
V_{OVLH}	Overvoltage Threshold	V_{CC} Low-to-High Transition	●	3.96	4	4.04	V
V_{OVHYS}	Hysteresis			0.25	0.4	0.55	V
I_{INOV}	OV Input Current	0V ≤ OV < 7V			0.1	1	µA
V_{OPEN}	Open-Circuit Voltage Threshold (V_{CC} – V_{SENSE})		●	1.5	3	6.5	mV
V_{OLOPEN}	OPEN Output Low Voltage	I_O = 2mA I_O = 5mA			0.20 0.75	0.5 1.3	V V
I_{INOPEN}	Leakage Current	V_{OPEN} = 5V			0.1	1	µA
$V_{SENSETRIP}$	SENSE Pin Trip Voltage (V_{CC} – V_{SENSE})	FB = 0V FB ≥ 2V	● ●	7 45	14 55	22 65	mV mV
I_{INSNS}	SENSE Pin Input Current	V_{SENSE} = V_{CC}			40	70	µA
I_{PU}	GATE Pull-Up Current	Charge Pump On, ΔV_{GATE} = 7V	●	–16	–32	–63	µA
I_{PD}	GATE Pull-Down Current	Any Fault, V_{GATE} > V_{OUT}		40	62	80	mA
I_{PDL}	V_{OUT} Pull-Down Current, Fault Condition	Any Fault, V_{GATE} = V_{OUT} + ΔV_{GATEL}, V_{OUT} = 48V			130		µA
ΔV_{GATE}	External N-Channel Gate Drive (Note 2)	V_{GATE} – V_{OUT}, 10.8V ≤ V_{CC} ≤ 20V 20V ≤ V_{CC} ≤ 80V	● ●	4.5 10	8.8 11.6	12.5 12.8	V V
ΔV_{GATEL}	External N-Channel Gate Drive, Fault Condition	V_{GATE} – V_{OUT}, V_{OUT} = 48V			–2		V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 48V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{FB}	FB Voltage Threshold	FB High-to-Low Transition FB Low-to-High Transition	● ●	3.95 4.20	3.99 4.45	4.03 4.65	V V
V_{FBHYS}	FB Hysteresis Voltage			0.3	0.45	0.60	V
V_{OLPGD}	PWRGD Output Low Voltage	I_O = 1.6mA I_O = 5mA			0.25 0.60	0.4 1.0	V V
I_{PWRGD}	PWRGD Pin Leakage Current	V_{PWRGD} = 80V			0.1	1	µA
I_{INFB}	FB Input Current	FB = 4.5V			–0.1	–1	µA
$I_{TIMERPU}$	TIMER Pull-Up Current	TIMER = 3V, During Fault	●	–63	–105	–147	µA
$I_{TIMERPD}$	TIMER Pull-Down Current	TIMER = 3V	●	1.5	3	5	µA
$V_{THTIMER}$	TIMER Shutdown Threshold	C_{TIMER} = 10nF	●	4.3	4.65	5	V
D_{TIMER}	Duty Cycle (RETRY Mode)		●	1.5	3	4.5	%
$V_{RETRYTH}$	RETRY Threshold		●	0.4	0.85	1.2	V
I_{INRTR}	RETRY Input Current	RETRY = GND			–87	–130	µA
t_{PHLUV}	UV Low to GATE Low	C_{GATE} = 100pF			1.7	3	µs
t_{PLHUV}	UV High to GATE High	C_{GATE} = 100pF			6	9	µs
t_{PHLFB}	FB Low to PWRGD Low				0.8	2	µs
t_{PLHFB}	FB High to PWRGD High				3.2	5	µs
$t_{PHLSENSE}$	(V_{CC} – V_{SENSE}) High to GATE Low	V_{CC} – V_{SENSE} = 275mV			1	3	µs

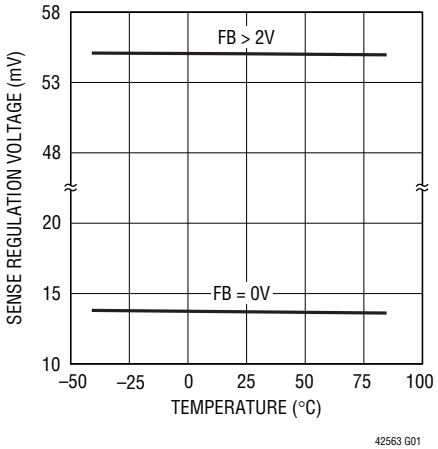
Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: An internal clamp limits the GATE pin to a minimum of 10V above V_{CC}. Driving this pin to a voltage beyond the clamp voltage may damage the part.

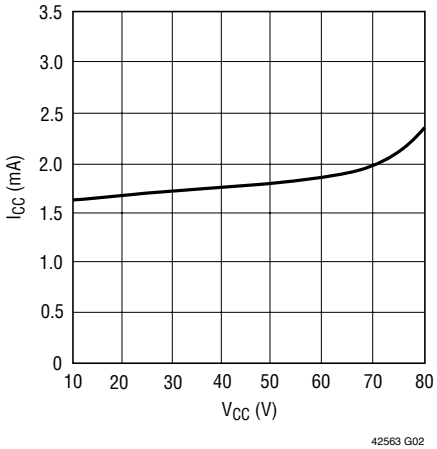
TYPICAL PERFORMANCE CHARACTERISTICS

Specifications are at T_A = 25°C unless otherwise noted.

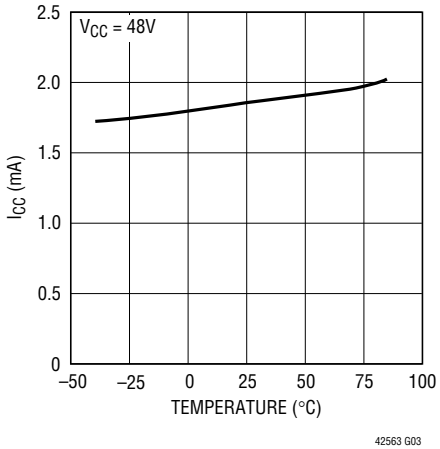
SENSE Regulation Voltage vs Temperature



I_{CC} vs V_{CC}



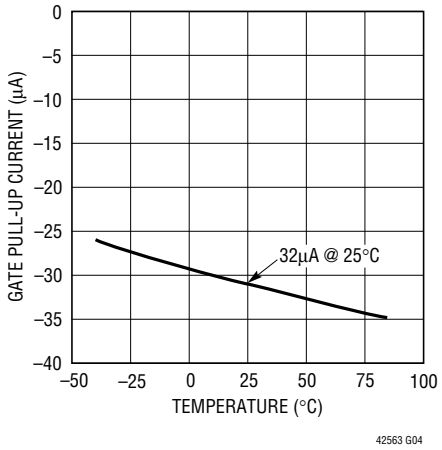
I_{CC} vs Temperature



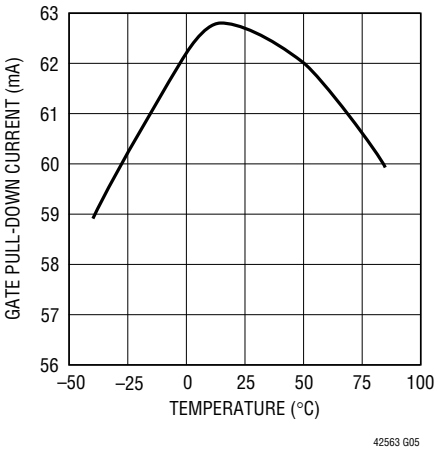
TYPICAL PERFORMANCE CHARACTERISTICS

Specifications are at T_A = 25°C unless otherwise noted.

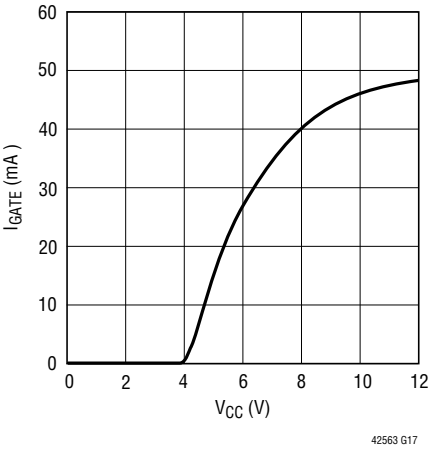
GATE Pull-Up Current vs Temperature



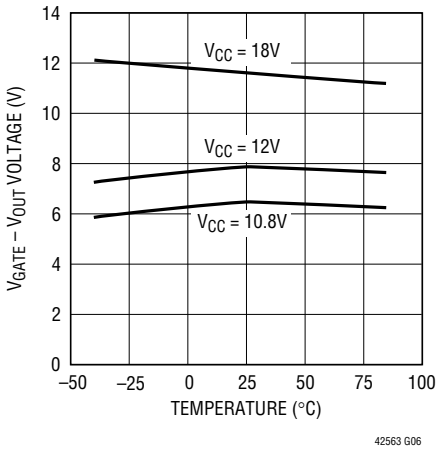
GATE Pull-Down Current vs Temperature



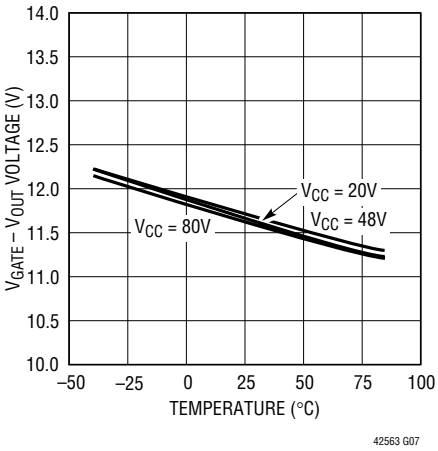
GATE Pull-Down Capability vs V_{CC} Below Minimum Operating Voltage



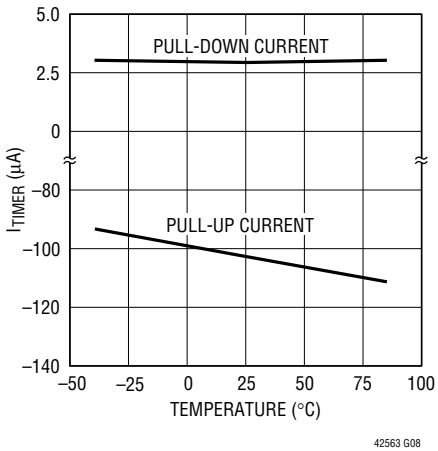
$V_{GATE} – V_{OUT}$ Voltage vs Temperature



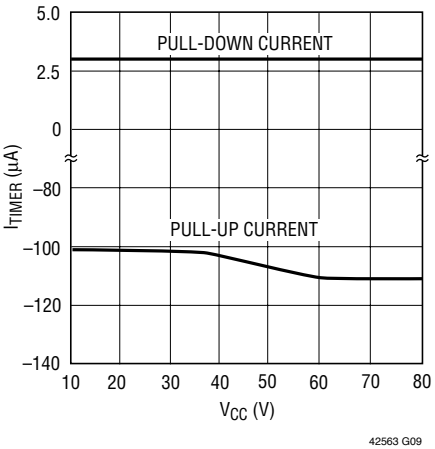
$V_{GATE} – V_{OUT}$ Voltage vs Temperature



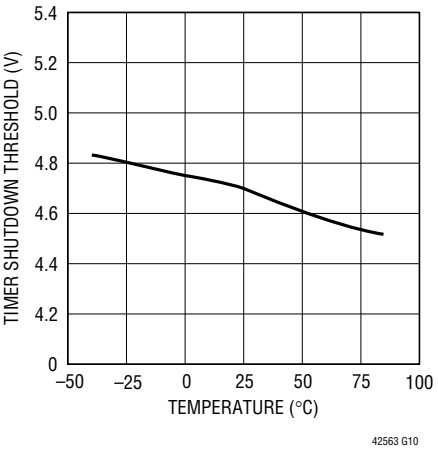
TIMER Currents vs Temperature



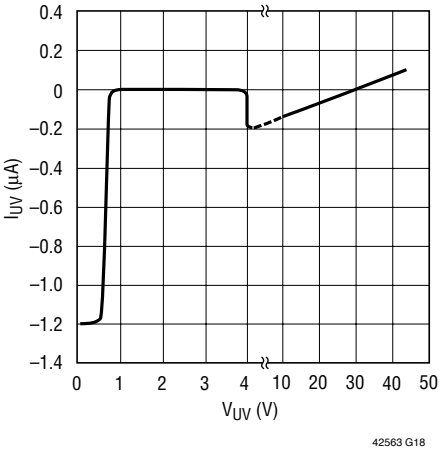
TIMER Currents vs V_{CC}



TIMER Shutdown Threshold vs Temperature



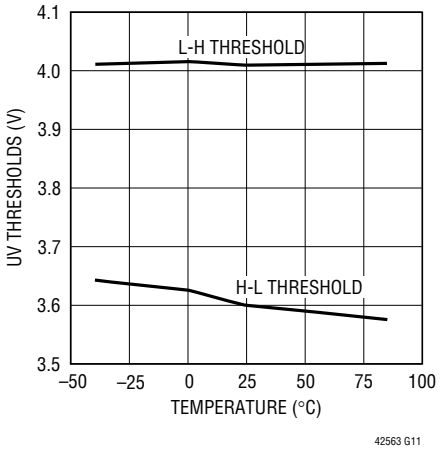
UV Current vs UV Voltage



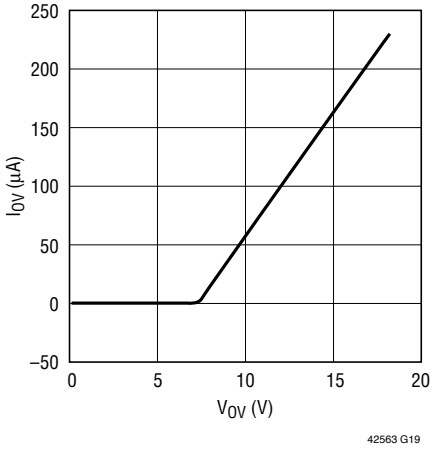
TYPICAL PERFORMANCE CHARACTERISTICS

Specifications are at T_A = 25°C unless otherwise noted.

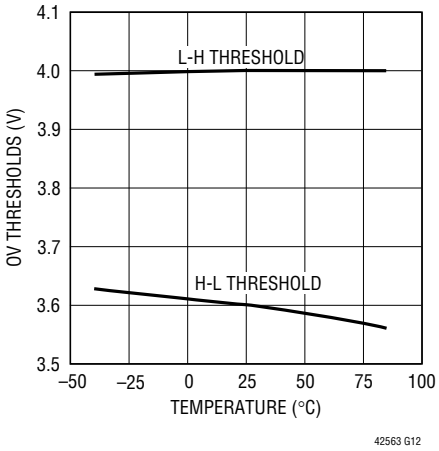
UV Thresholds vs Temperature



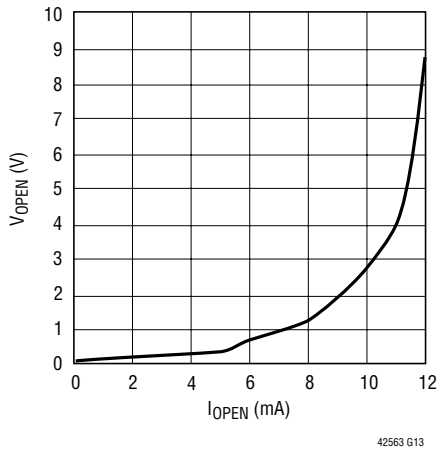
OV Current vs OV Voltage



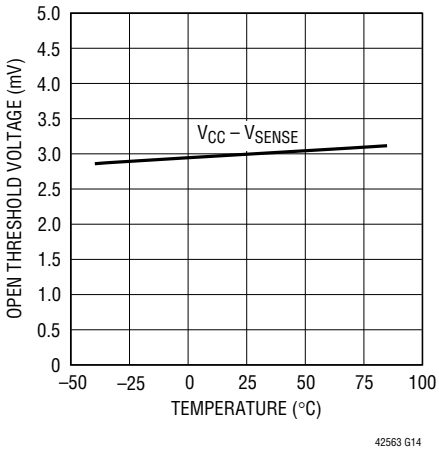
OV Thresholds vs Temperature



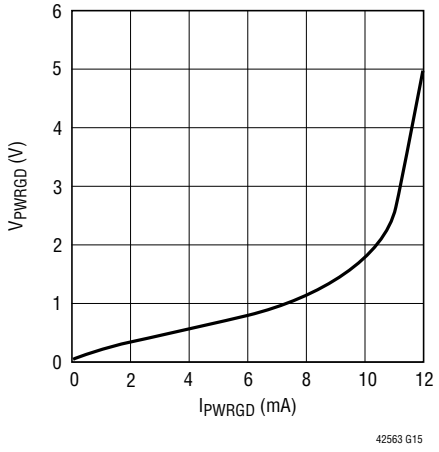
OPEN Output Voltage vs I_{OPEN}



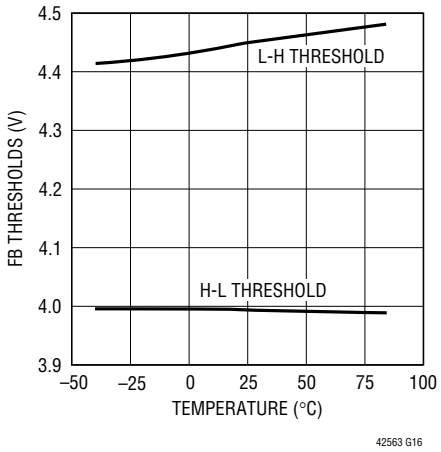
OPEN Threshold Voltage vs Temperature



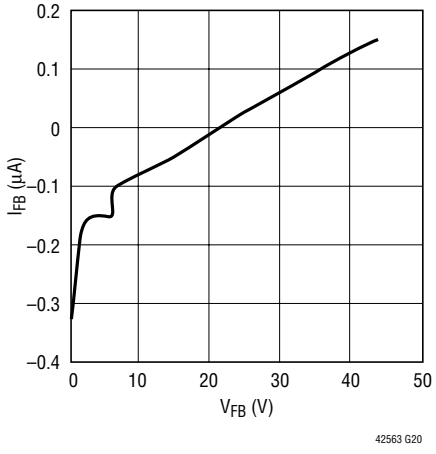
PWRGD Output Voltage vs I_{PWRGD}



FB Thresholds vs Temperature



FB Current vs FB Voltage



PIN FUNCTIONS

UV (Pin 1): Undervoltage Sense Input. UV is an input that enables the output voltage. When UV is driven above 4V, GATE will start charging and the output turns on. When UV goes below 3.6V, GATE discharges and the output shuts off.

Pulsing UV to below 0.4V for at least 5µs after a current limit fault cycle resets the fault latch (when RETRY pin is low, commanding latch off operation) and allows the part to turn back on. This command is only accepted after TIMER is discharged below 0.65V. To disable UV sensing, connect the pin to a voltage between 5V and 44V.

OV (Pin 2): Overvoltage Sense Input. OV is an input that disables the output voltage. If OV ever goes above 4V, GATE is discharged and the output shuts off. When OV goes below 3.6V, GATE starts charging and the output turns back on. To disable overvoltage sensing, connect pin to ground.

NC (Pins 3, 6, 11, 14): No Connect. Not connected to any internal circuitry.

OPEN (Pin 4): Open Circuit Detect Output. This pin is an open collector output that releases and is pulled high through an external resistor if the load current is less than (3mV)/R5.

PWRGD (Pin 5): Power Good Output. PWRGD is pulled low whenever the voltage on FB falls below the high-to-low threshold voltage. It goes into a high impedance state when the voltage on FB exceeds the low-to-high threshold voltage. An external pull-up resistor can pull PWRGD to a voltage higher or lower than V_{CC}.

RETRY (Pin 7): Current Fault Retry Input. RETRY commands the operational mode of the current limit. If RETRY is floating, the LT4256-3 automatically restarts after a current fault. If it is connected to a voltage below 0.4V, it will latch off after a current fault (which requires that UV be cycled low in order to start normal operation again).

GND (Pin 8): Device Ground. This pin must be tied to a ground plane for best performance.

TIMER (Pin 9): Timing Input. An external timing capacitor from TIMER to GND programs the maximum time the part is allowed to remain in current limit. When the part goes into current limit, a 105µA pull-up current source starts to charge the timing capacitor. When the voltage on TIMER reaches 4.65V (typ), GATE is pulled low; the TIMER pull-up current will be turned off and the capacitor is discharged by a 3µA pull-down current. When TIMER falls below 0.65V (typ), GATE turns on again if RETRY is high (if RETRY is low, UV must be pulsed low to reset the internal fault latch before GATE will turn on). If RETRY is grounded and UV is not cycled low, GATE remains latched off and TIMER will be discharged to near ground. UV must be cycled low after TIMER has discharged below 0.65V (typ) to reset the part.

If RETRY is floating or connected to a voltage above its 1.2V threshold, the LT4256-3 automatically restarts after a current fault. Under an output short-circuit condition, the LT4256-3 cycles on and off with a 3% on-time duty cycle.

FB (Pin 10): Power Good Comparator Input. FB monitors the output voltage through an external resistive divider. When the voltage on FB is lower than the high-to-low threshold of 3.99V, PWRGD is pulled low and released when FB is pulled above the 4.45V low-to-high threshold.

The voltage present on FB affects foldback current limit (see Figure 8 and related discussion).

V_{OUT} (Pin 12): Output Voltage Sense Input. This pin should be connected to the source of the external MOSFET. It is used to sense when the MOSFET is shut off (during any fault mode) and to reduce the pull-down current on GATE. This protects the LT4256-3 from excessive power dissipation when large output capacitors are used.

PIN FUNCTIONS

GATE (Pin 13): High Side Gate Drive for the External N-Channel MOSFET. An internal charge pump guarantees at least 10V of gate drive for V_{CC} supply voltages above 20V and 4.5V of gate drive for V_{CC} supply voltages between 10.8V and 20V. The rising slope of the voltage on GATE is set by an external capacitor connected from GATE to GND and an internal 32µA pull-up current source from the charge pump output.

If the current limit is reached, the GATE voltage is adjusted to maintain a constant voltage across the sense resistor while the timing capacitor starts to charge. If the TIMER voltage ever exceeds 4.65V, GATE is pulled low.

GATE is also pulled to GND whenever UV is pulled low; the V_{CC} supply voltage drops below the externally programmed undervoltage threshold, above the overvoltage threshold or below the internal UVLO threshold (9.8V).

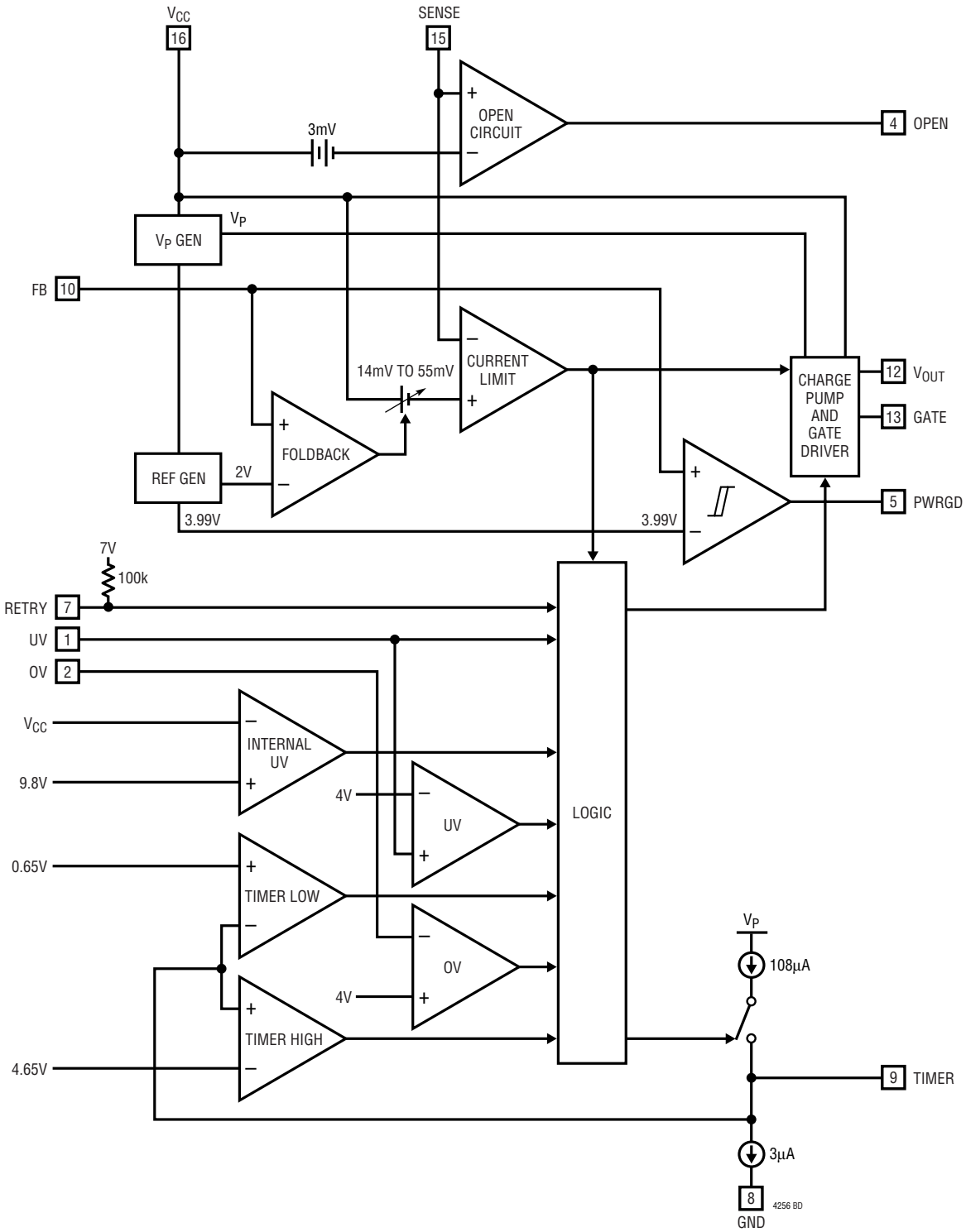
GATE is clamped internally to a maximum voltage of 11.6V (typ) above V_{OUT} under normal operating conditions. Driving this pin beyond the clamp voltage may damage the part. GATE is also clamped to 2V (typ) below V_{OUT}. When the gate is commanded off due to a fault condition, it is discharged quickly by a 62mA (typ) capable switch until GATE is 2V (typ) below V_{OUT}. When GATE is below V_{OUT} by 2V, the 62mA is reduced to 130µA to protect the LT4256-3 against damage if V_{OUT} has large capacitance. A Zener diode is needed between the gate and source of the external MOSFET to protect its gate oxide under instantaneous short-circuit conditions. See Applications Information.

SENSE (Pin 15): Current Limit Sense Input. A sense resistor is placed in the supply path between V_{CC} and SENSE. The current limit circuit regulates the voltage across the sense resistor (V_{CC} – SENSE) to 55mV while in current limit when FB is 2V or higher. If FB drops below 2V, the regulated voltage across the sense resistor decreases linearly and stops at 14mV when FB is 0V. The OPEN output also uses SENSE to detect when the output current is less than (3mV)/R5.

To defeat current limit, connect SENSE to V_{CC}.

V_{CC} (Pin 16): Input Supply Voltage. The positive supply input ranges from 10.8V to 80V for normal operation. I_{CC} is typically 1.8mA. An internal circuit disables the LT4256-3 for inputs less than 9.8V (typ).

BLOCK DIAGRAM



TEST CIRCUIT

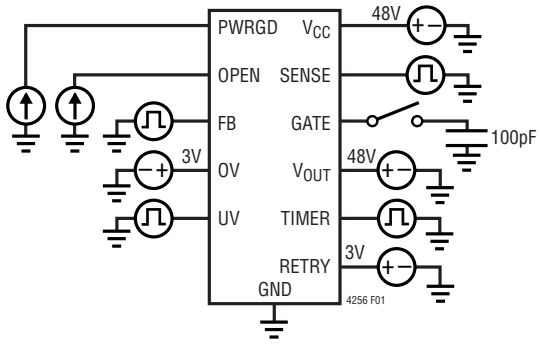


Figure 1

TIMING DIAGRAMS

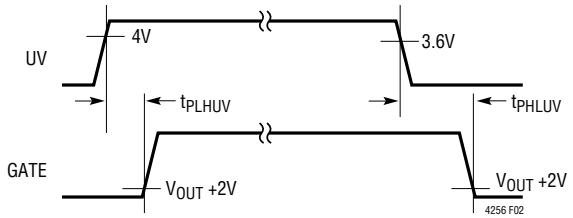


Figure 2. UV to GATE Timing

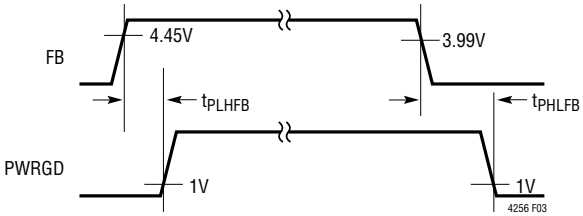


Figure 3. V_{OUT} to PWRGD Timing

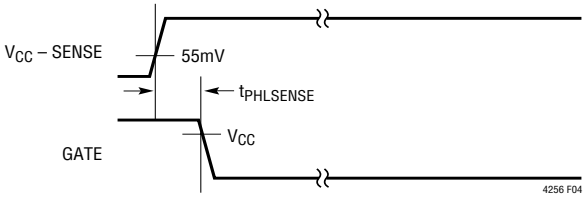


Figure 4. SENSE to GATE Timing

APPLICATIONS INFORMATION

Hot Circuit Insertion

When circuit boards are inserted into a live backplane, the supply bypass capacitors on the boards draw high peak currents from the backplane power bus as they charge. The transient currents can permanently damage the connector pins and glitch the system supply, causing other boards in the system to reset.

The LT4256-3 is designed to turn on a board's supply voltage in a controlled manner, allowing the board to be safely inserted or removed from a live backplane. The device also provides undervoltage and overvoltage as well as overcurrent protection while a power good output signal indicates when the output supply voltage is ready with a high output.

Power-Up Sequence

An external N-channel MOSFET pass transistor (Q1) is placed in the power path to control the power up of the supply voltage (Figure 5). Resistor R5 provides current detection and capacitor C1 controls the GATE slew rate. Resistor R7 compensates the current control loop while R6 prevents high frequency oscillations in Q1.

When the power pins first make contact, transistor Q1 is held off. If the voltage on V_{CC} is between the externally programmed undervoltage and overvoltage thresholds, V_{CC} is above 9.8V and the voltage on TIMER is less than 4.65V (typ), transistor Q1 will be turned on (Figure 6). The voltage on GATE rises with a slope equal to 32µA/C1 and the supply inrush current is set at:

$$I_{INRUSH} = C_L \bullet 32\mu A/C1 \quad (1)$$

where C_L is the total load capacitance.

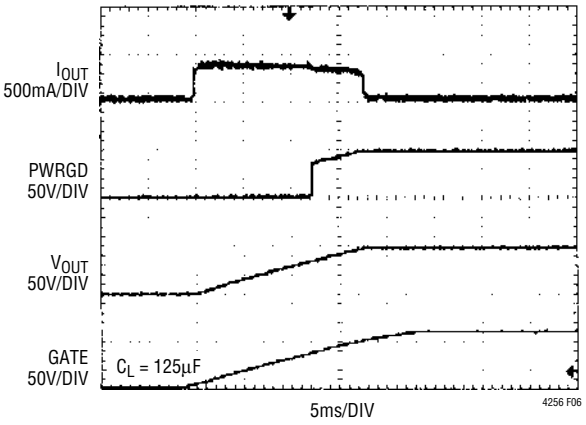


Figure 6. Start-Up Waveforms

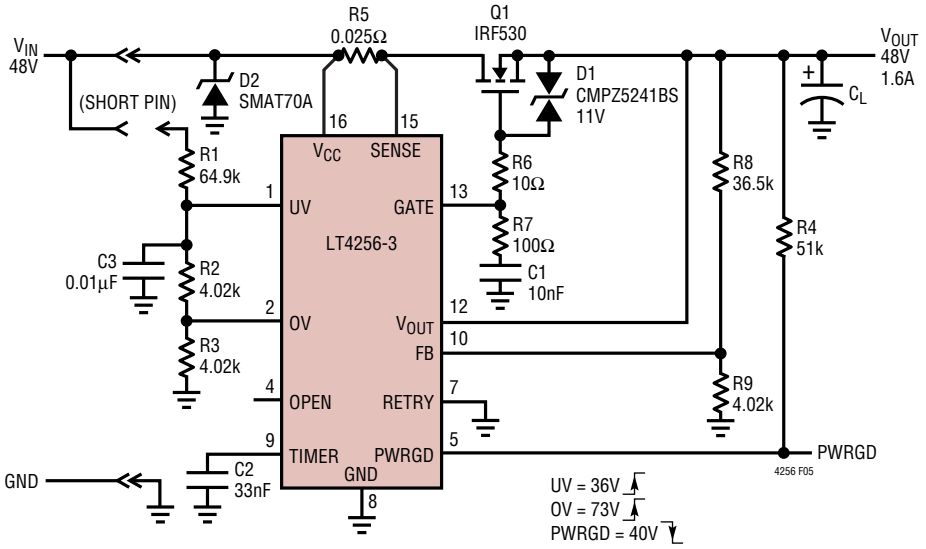


Figure 5. 1.6A, 48V Latchoff Application

APPLICATIONS INFORMATION

To reduce inrush current, increase C1 or decrease load capacitance. If the voltage across the current sense resistor R5 reaches $V_{SENSETRIP}$, the inrush current will be limited by the internal current limit circuitry. The voltage on GATE is adjusted to maintain a constant voltage across the sense resistor and TIMER begins to charge.

When the FB voltage goes above the low-to-high V_{FB} threshold, PWRGD goes high.

Undervoltage and Overvoltage Detection

The LT4256-3 uses UV and OV to monitor the V_{CC} voltage to determine when it is safe to turn on the load and allow the user the greatest flexibility for setting the operational thresholds. UV and OV are internally connected to an analog window comparator. Any time that UV goes below 3.6V or OV goes above 4V, GATE will be pulled low until the UV/OV voltages return to the normal operation voltage window (4V and 3.6V, respectively).

The UV threshold should never be set below the internal UVLO threshold (9.8V typically) because the benefit of the UV's hysteresis will be lost, making the LT4256-3 more susceptible to noise (V_{CC} must be at least 9.8V when UV is at its 3.6V threshold). UV is filtered with C3 to prevent noise spikes and capacitively coupled glitches from shutting down the LT4256-3 output erroneously.

To calculate UV and OV thresholds, use the following equations:

$$R1 = (R2 + R3)\left(\frac{V_{THUVLH}}{4V} - 1\right) \quad (2a)$$

$$R3 = \frac{R1 + R2}{\frac{V_{THOVLH}}{4} - 1} \quad (2b)$$

$$20k\Omega \le R1 + R2 + R3 \le 200k\Omega \quad (3)$$

$$V_{THUVHL} = 3.6V\left(1 + \frac{R1}{R2 + R3}\right); \quad (4)$$

$$V_{THOVHL} = 3.6V\left(1 + \frac{R1 + R2}{R3}\right)$$

where V_{THULH} and V_{THOVLH} are the desired UV and OV threshold voltages when V_{CC} is rising (L – H).

Figure 7 shows how the LT4256-3 is commanded to shut off with a logic signal. This is accomplished by pulling the gate of the open-drain MOSFET, Q2, (tied to UV) high.

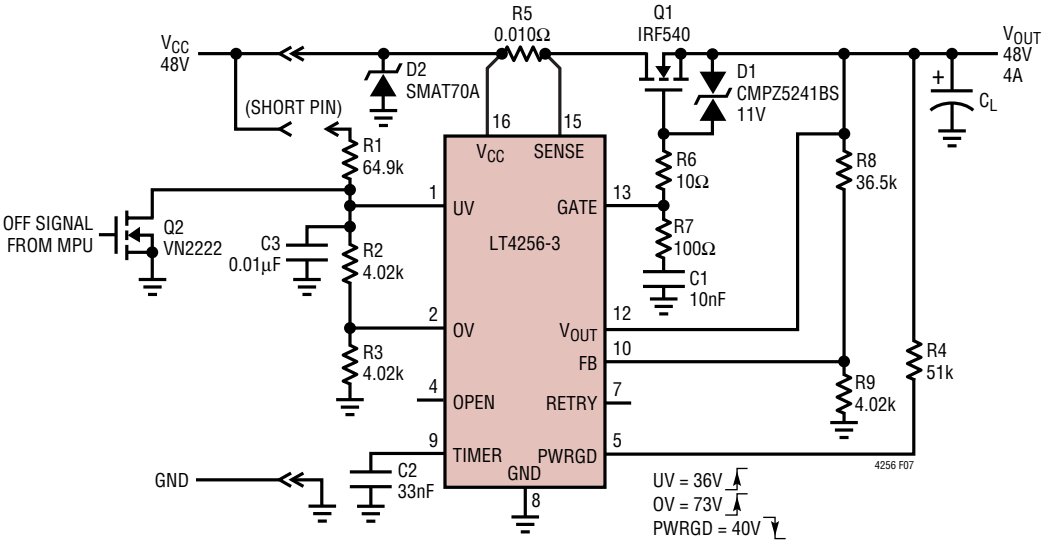


Figure 7. How to Use a Logic Signal to Control the LT4256-3 Turn On/Off

APPLICATIONS INFORMATION

Short-Circuit Protection

The LT4256-3 features a programmable foldback current limit with an electronic circuit breaker that protects against short circuits or excessive load currents. The current limit is set by placing a sense resistor (R5) between V_{CC} and SENSE. The current limit threshold is calculated as:

$$I_{LIMIT} = 55mV/R5 \quad (5)$$

To limit excessive power dissipation in the pass transistor and to reduce voltage spikes on the input supply during short-circuit conditions at the output, the current folds back as a function of the output voltage, which is sensed internally on FB.

If the LT4256-3 goes into current limit when the voltage on FB is 0V, the current limit circuit drives GATE to force a constant 14mV drop across the sense resistor. As the output at FB increases, the voltage across the sense resistor increases until FB reaches 2V, at which point the voltage across the sense resistor is held constant at 55mV (see Figure 8).

For a 0.025Ω sense resistor, the typical current limit is set at 2200mA and folds back to 560mA when the output is shorted to ground. Thus, MOSFET peak power dissipation under short-circuit conditions is reduced from 106W to 27W. See the Layout Considerations section for important information about board layout to minimize current limit threshold error.

The LT4256-3 also features a variable overcurrent response time. The time required for the part to regulate the GATE voltage is a function of the voltage across the sense resistor connected between V_{CC} and SENSE. This helps to eliminate sensitivity to current spikes and transients that might otherwise unnecessarily trigger a current limit response and increase MOSFET dissipation. Figure 9 shows the response time as a function of the overdrive at SENSE.

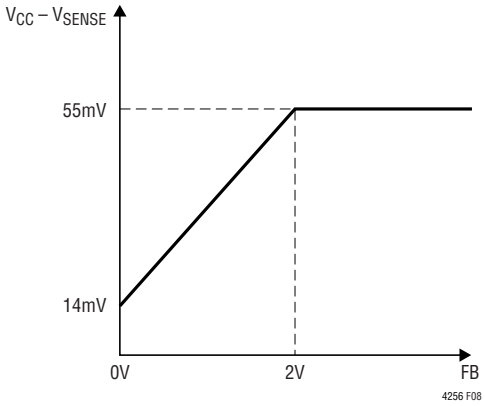


Figure 8. Current Limit Sense Voltage vs Feedback Pin Voltage

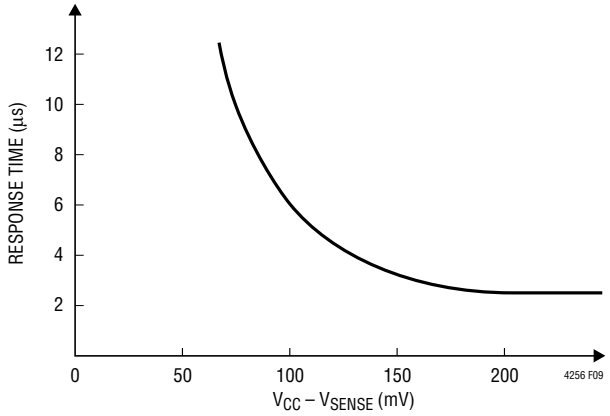


Figure 9. Response Time to Overcurrent

APPLICATIONS INFORMATION

TIMER

TIMER provides a method for programming the maximum time the part is allowed to operate in current limit. When the current limit circuitry is not active, TIMER is pulled to GND by a 3µA current source. When the current limit circuitry becomes active, a 108µA pull-up current source is connected to TIMER and the voltage will rise with a slope equal to 105µA/C_{TIMER} as long as the circuitry stays active. Once the desired maximum current limit time is known, the capacitor value is:

$$C\left[nF\right] = 25 \bullet t\left[ms\right];\ C = \frac{105\mu A}{4.65V} \bullet t \qquad (6)$$

Whenever TIMER reaches 4.65V (typ), the internal fault latch is set causing GATE to be pulled low and TIMER to be discharged to GND by the 3µA current source. The part is not allowed to turn on again until the voltage on TIMER falls below 0.65V (typ).

Whenever GATE is commanded off by any fault condition, it is discharged with a high current, turning off the external MOSFET. The waveform in Figure 10 shows how the output latches off following a current fault. The drop across the sense resistor is held at 55mV as the timer ramps up. Once TIMER reaches its shutdown threshold (4.65V typically), the circuit latches off.

Automatic Restart

If RETRY is floating, then the device automatically restarts after a current overload fault.

When the voltage at TIMER ramps back down to 0.65V (typ), the LT4256-3 turns on again. If the short-circuit condition at the output still exists, the cycle will repeat itself indefinitely. The duty cycle under short-circuit conditions is 3% which prevents Q1 from overheating. Figure 11 shows representative waveforms during a short circuit.

Latch Off Operation

If RETRY is grounded, the LT4256-3 will latch off after a current fault. After the part latches off, it may be commanded to start back up. This is accomplished by cycling UV to ground and then back high (this command can only be accepted after TIMER discharges below the 0.65V typ threshold, which prevents overheating transistor Q1).

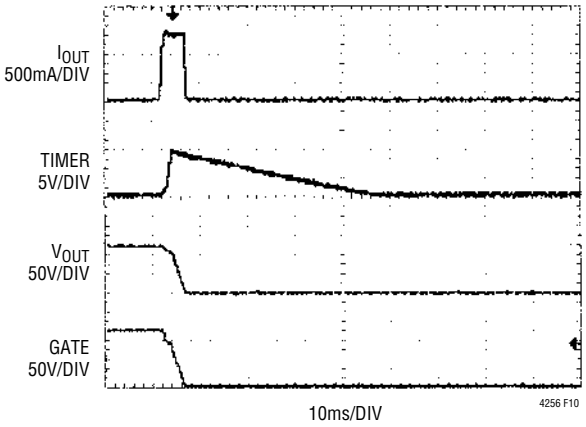


Figure 10. Latch Off Waveforms

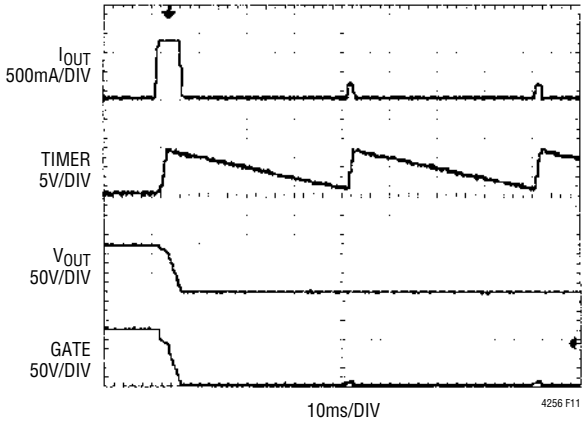


Figure 11. RETRY Waveforms

APPLICATIONS INFORMATION

Therefore, using RETRY only, the LT4256-3 will either latch off after an overcurrent fault condition or it will go into a hiccup mode.

Power Good Detection

The LT4256-3 includes a comparator for monitoring the output voltage. The output voltage is sensed through the FB pin via an external resistor string. The comparator's output (PWRGD) is an open collector capable of operating from a pull-up as high as 80V.

PWRGD can be used to directly enable/disable a power module with an active high enable input. Figure 12 shows how to use PWRGD to control an active low enable input power module. Signal inversion is accomplished by transistor Q2 and R10.

The thresholds for the FB pin are 4.45V (low to high) and 3.99V (high to low). To calculate the PWRGD thresholds, use the following equations:

$$R8 = \left(\frac{V_{THPWRGD}}{3.99V} - 1\right) \bullet R9, \text{ high to low} \quad (7)$$

$$20k\Omega \le R8 + R9 \le 200k\Omega \quad (8a)$$

$$V_{THPWRGD} = 4.45V\left(1 + \frac{R8}{R9}\right), \text{ low to high} \quad (8b)$$

OPEN Pin/Open FET Detection

OPEN is an output which signals abnormally low load currents. When the voltage across the sense resistor is less than 3mV, the open collector pull-down device is shut off allowing OPEN to be externally pulled high. OPEN is always active when V_{CC} is above 9.8V. If V_{CC} is below 9.8V (the internal UVLO threshold), OPEN is pulled low.

Open-circuit MOSFETs are detected with the LT4256-3 by monitoring the voltage across R5 with OPEN while monitoring the output voltage with PWRGD. An open FET condition is signalled when OPEN is high and PWRGD is low (after the part has completed its start-up cycle).

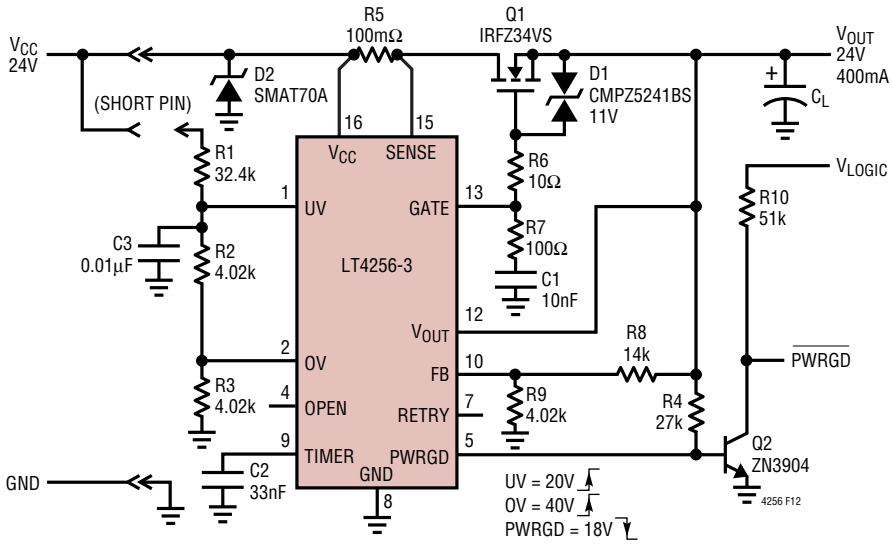


Figure 12. Active Low Enable PWRGD Application

APPLICATIONS INFORMATION

This open FET condition can be falsely signalled during start-up if the load is not activated until after PWRGD goes high. To avoid this false indication, OPEN and PWRGD should not be polled for a period of time, $t_{STARTUP}$, given by:

$$t_{STARTUP} = \frac{3 \bullet V_{CC} \bullet C1}{32\mu A} \quad (9)$$

This can be accomplished either by a microcontroller (if available) or by placing an RC filter as shown in Figure 13.

Once the OPEN voltage exceeds the monitoring logic threshold, V_{THRESH}, and PWRGD is low, an open FET condition is signalled. In order to prevent a false indication, the RC product should be set with the following equation:

$$RC > \frac{3 \bullet V_{CC} \bullet C1}{32\mu A\left(\ln\left(\frac{V_{LOGIC}}{V_{LOGIC} - V_{THRESH}}\right)\right)} \quad (10)$$

Another condition that can cause a false indication is if the LT4256-3 goes into current limit during start-up. This will cause $t_{STARTUP}$ to be longer than calculated. Also, if the LT4256-3 stays in current limit long enough for TIMER to fully charge up to its threshold, the LT4256-3 will either latch off (RETRY = 0) or go into the current limit hiccup mode (RETRY = floating). In either case, an open FET condition will be falsely signalled. If the LT4256-3 does go into current limit during start-up, C1 can be increased (see Power-Up Sequence).

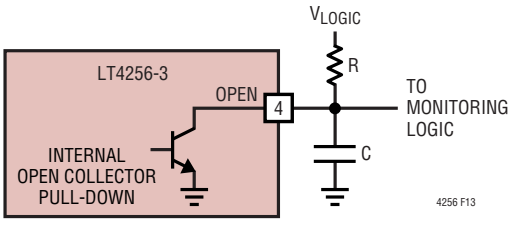


Figure 13. Delay Circuit for OPEN FET Detection

Supply Transient Protection

The LT4256-3 is 100% tested and guaranteed to be safe from damage with supply voltages up to 80V. However, voltage transients above 100V may cause permanent damage. During a short-circuit condition, the large change in currents flowing through the power supply traces can cause inductive voltage transients which could exceed 100V. To minimize the voltage transients, the power trace parasitic inductance should be minimized by using wider traces or heavier trace plating and a bypass capacitor should be placed between V_{CC} and GND. A surge suppressor (TransZorb®) at the input can also prevent damage from voltage transients.

GATE Pin

A curve of gate drive vs V_{CC} is shown in Figure 14. GATE is clamped to a maximum voltage of 12.8V above V_{OUT}. This clamp is designed to withstand the internal charge pump current. An external Zener diode must be used as shown in all applications. At a minimum input supply voltage of 10.8V, the minimum gate drive voltage is 4.5V. When the input supply voltage is higher than 20V, the gate drive voltage is at least 10V and a standard threshold MOSFET can be used. In applications from 12V to 15V range, a logic level MOSFET must be used.

TransZorb is a registered trademark of General Instruments, GSI.

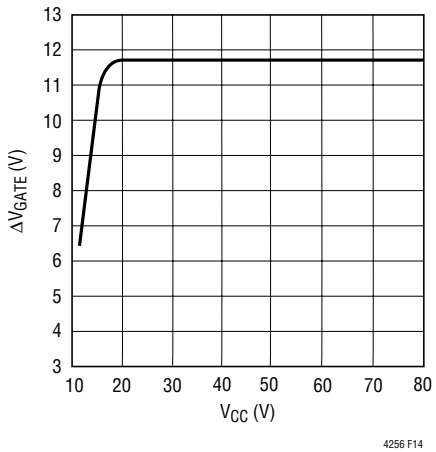


Figure 14. ΔV_{GATE} vs V_{CC}

APPLICATIONS INFORMATION

In some applications it may be possible for V_{OUT} to ring below ground (due to the parasitic trace inductance). Higher current applications, especially where the output load is physically far away from the LT4256-3 will be more susceptible to these transients. This is normal and the LT4256-3 has been designed to allow for some ringing below ground. However, if the application is such that V_{OUT} can ring more than 3V below ground, damage may occur to the LT4256-3 and an external diode, D2, from ground (anode) to V_{OUT} (cathode) will have to be added to the circuit as shown in Figure 15 (it is critical that the reverse breakdown voltage of the diode be higher than the highest expected V_{CC} voltage). A capacitor placed from ground to V_{OUT} directly at the LT4256-3 pins can help reduce the amount of ringing on V_{OUT} but it may not be enough for some applications.

During a fault condition, the LT4256-3 pulls down on GATE with a switch capable of sinking about 62mA. Once GATE drops below the output voltage by a diode forward voltage, the external Zener will forward bias and V_{OUT} will also be discharged to GND. In addition to the GATE capacitance, the output capacitance will be discharged through the LT4256-3.

In applications utilizing very large external N-channel MOSFETs, the possibility exists for the MOSFET to turn on when initially inserted into a live backplane (before the LT4256-3 becomes active and pulls down on GATE). This is due to the MOSFET intrinsic drain to gate capacitance forcing current into R7 and C1 when the drain voltage steps up from ground to V_{CC} with an extremely fast rise time. To alleviate this situation, a diode, D3, should be put across R7 with the cathode connected to C1 as shown in Figure 16.

Whenever the LT4256-3 turns the MOSFET off, GATE pulls the MOSFET gate to ground with an open collector capable of sinking 62mA. If the output is held up by a large reservoir capacitor, the stored energy is dissipated in the pull-down transistor via a sneak path through the (now forward biased) Zener, D1. The LT4256-3 has a proprietary feature that reduces on-chip power dissipation by sensing when the MOSFET is off and reducing the pull-down current significantly. See V_{GATE} Turn-Off for more information about using this feature.

V_{GATE} Turn-Off

The LT4256-3 has a proprietary feature that reduces power dissipation by sensing when the MOSFET is off and reducing the pull-down current significantly. As the GATE pin is discharged during any fault, the LT4256-3 monitors the GATE pin and V_{OUT} pin. When the GATE pin is 2V below V_{OUT}, the pull-down current is reduced from 62mA to about 130µA.

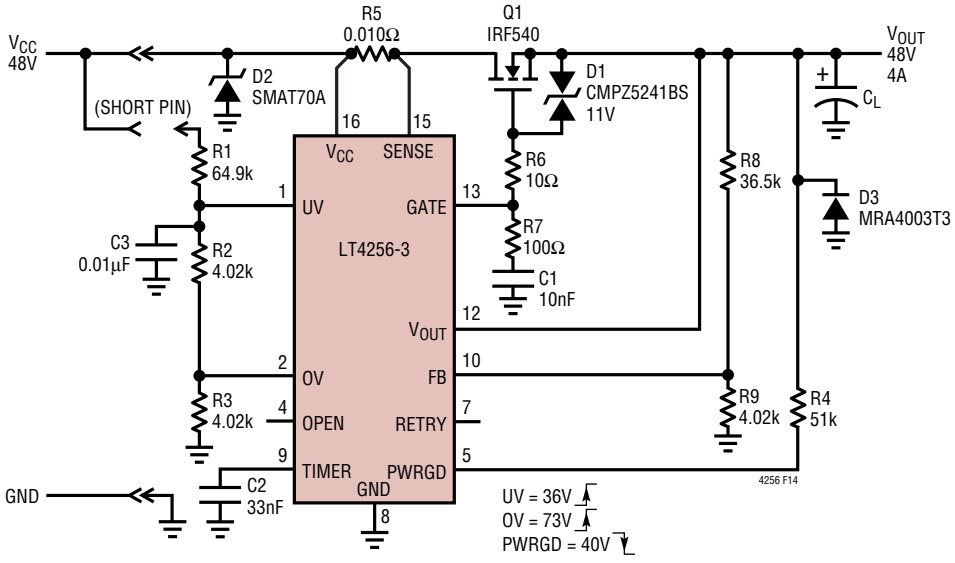


Figure 15. Negative Output Voltage Protection Diode Application

APPLICATIONS INFORMATION

In order to use this feature as designed, a bidirectional Zener diode is needed for D1. When the LT4256-3 commands the MOSFET off (and a bidirectional Zener is used), the output discharges very slowly ($t_{OFF} = (C_{LOAD} \bullet V_{OUT})/130\mu A$). Several variations can be implemented to discharge the output faster. The recommeded method is shown in Figure 17 and uses an external PNP transistor, diode and resistor to discharge the output quickly.

The equation to set the nominal discharge current is:

$$I_{DISCHG} = \frac{5000}{R_{PROG}}(130\mu A) \quad (11)$$

where R_{PROG} must be less than 1k.

The maximum current equation is:

$$I_{MAX} = \frac{7000}{R_{PROG}}(350\mu A) \quad (12)$$

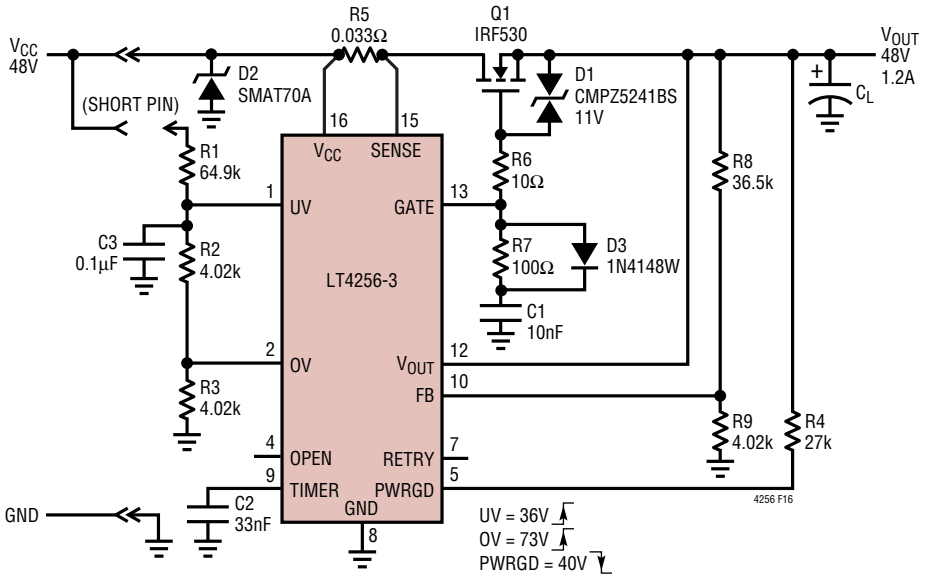


Figure 16. High dV/dt MOSFET Turn-On Protection Circuit

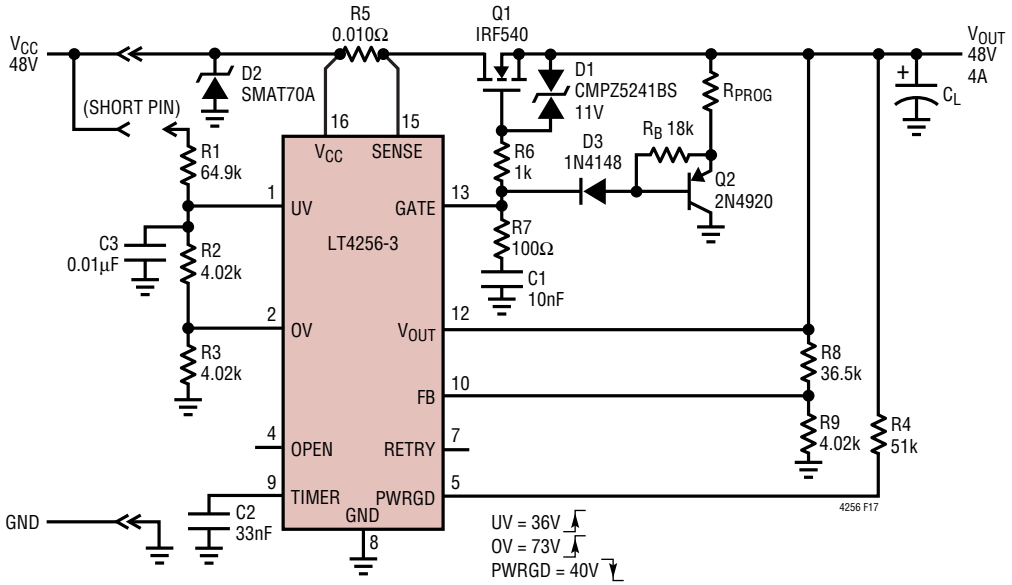


Figure 17. Enhanced Output Pull-Down Circuit

APPLICATIONS INFORMATION

Layout Considerations

To achieve accurate current sensing, a Kelvin connection to the current sense resistor (R5 in typical application circuit) is recommended. Note that 1oz copper exhibits a sheet resistance of about 530μΩ/❑. Small resistances can cause large errors in high current applications. Noise immunity will be improved significantly by locating resistor dividers close to the pins with short V_{CC} and GND traces. The minimum trace width for 1oz copper foil is 0.02" per amp to make sure the trace stays at a reasonable temperature. 0.03" per amp or wider is recommended. Figure 18 shows a layout that meets these requirements.

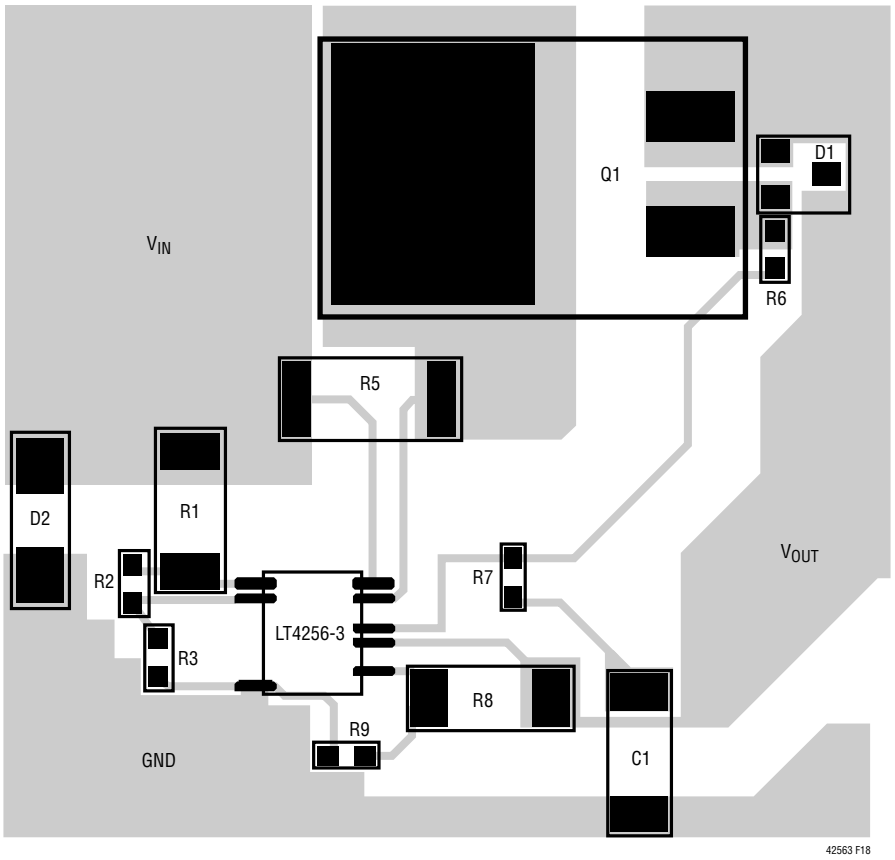
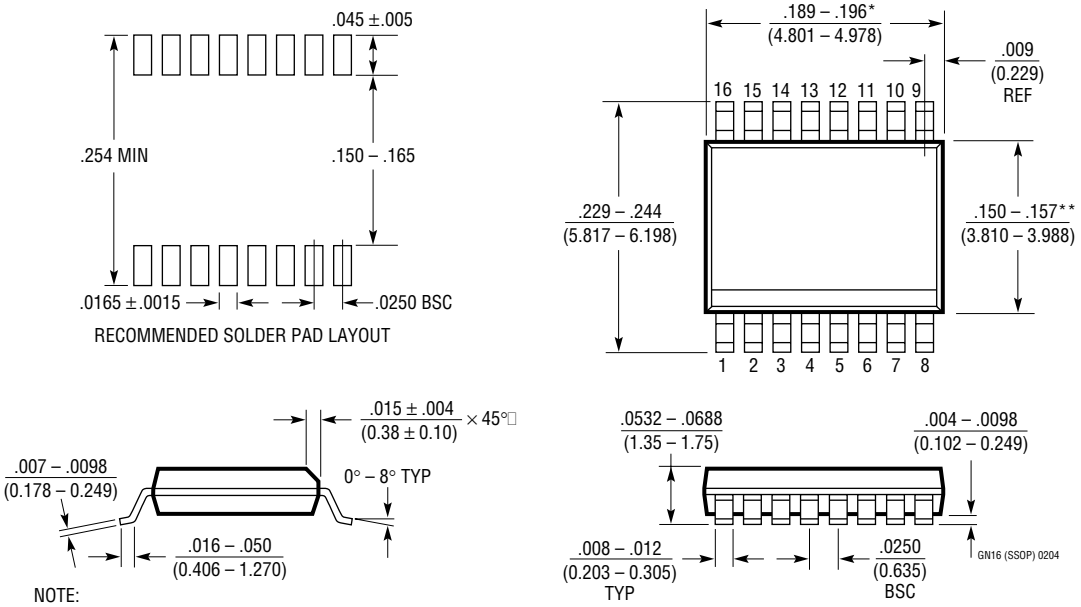


Figure 18. Recommended Component Placement

PACKAGE DESCRIPTION

GN Package
16-Lead Plastic SSOP (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1641)



NOTE:
1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
3. DRAWING NOT TO SCALE

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE