IEEE 802.3bt PD Interface Controller

FEATURES

- **IEEE 802.3af/at/bt Powered Device (PD) Controller**
- **Supports Up to 71.3W PDs**
- **5-Event Classification Sensing**
- **Superior Surge Protection (100V Absolute Maximum)**
- **Wide Junction Temperature Range (–40°C to 125°C)**
- Overtemperature Protection
- Integrated Signature Resistor
- External Hot Swap N-Channel MOSFET for Lowest Power Dissipation and Highest System Efficiency
- Configurable Aux Power Support as Low as 9V
- Easy Migration Between LTPoE++® PDs and IEEE 802.3bt PDs
- Pin Compatible with LT4275A/B/C
- Available in 10-Lead MSOP and 3mm × 3mm DFN Packages

APPLICATIONS

- High Power Wireless Data Systems
- Outdoor Security Camera Equipment
- Commercial and Public Information Displays
- High Temperature Industrial Applications

DESCRIPTION

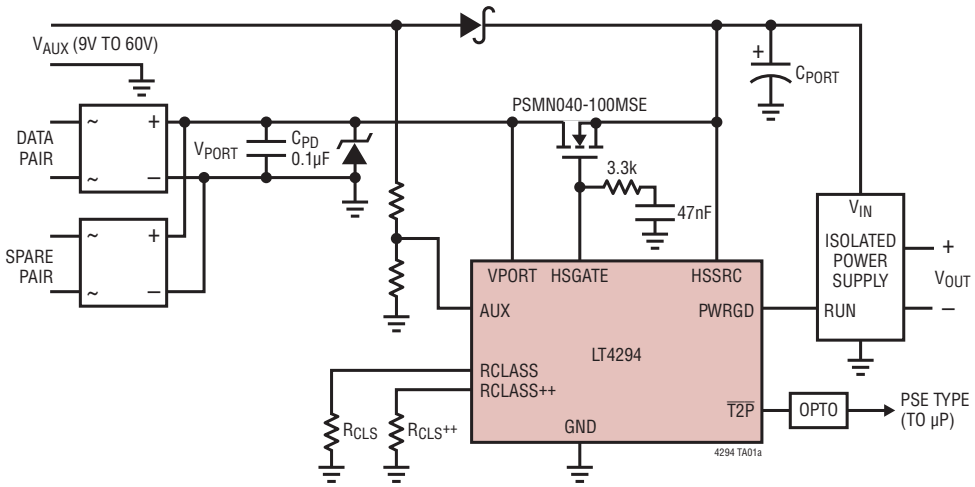
The LT®4294 is an IEEE 802.3af/at/bt-compliant powered device (PD) interface controller. The $\overline{T2P}$ output indicates the number of classification events received during IEEE 802.3bt-compliant mutual identification and negotiation of available power.

The LT4294 utilizes an external, low $R_{DS(ON)}$ N-channel hot swap MOSFET and supports the LT4320/LT4321 ideal diode bridges, to extend the end-to-end power delivery efficiency and eliminate costly heat sinks. The LT4294 also includes a power good output, onboard signature resistor, undervoltage lockout, and thermal protection. Start-up inrush current is adjustable with an external capacitor. Auxiliary power override is supported as low as 9V with the AUX pin.

The LT4294 can be configured to support all possible 802.3bt, 802.3at and 802.3af power levels with external component changes. Pin-for-pin compatibility with the LT4275 family of PD Interface Controllers enables easy migration between LTPoE++ PDs and IEEE 802.3bt-compliant PDs.

TYPICAL APPLICATION

IEEE 802.3bt Single-Signature Powered Device Interface



SINGLE-SIGNATURE POWER CLASSIFICATION (AT PD INPUT)

CLASS	POWER
0	13W
1	3.84W
2	6.49W
3	13W
4	25.5W
5	40W
6	51W
7	62W
8	71.3W

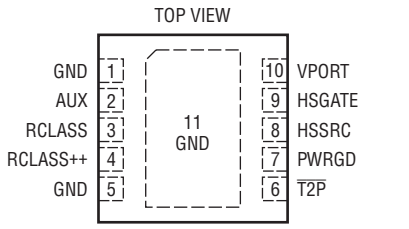
ABSOLUTE MAXIMUM RATINGS

(Notes 1, 3)

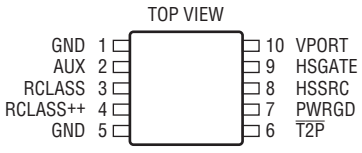
VPORT, HSSRC Voltages ..... –0.3V to 100V
HSGATE Current..... ±20mA
RCLASS, RCLASS++
Voltages..... –0.3V to 8V (and ≤ VPORT)
AUX Current..... ±1.4mA
$\overline{T2P}$, PWRGD Voltage ..... –0.3V to 100V
$\overline{T2P}$, PWRGD Current 5mA

Operating Junction Temperature Range (Note 4)
LT4294I.....–40°C to 85°C
LT4294H .....–40°C to 125°C
Storage Temperature Range .....–65°C to 150°C
Lead Temperature (Soldering, 10 sec.).....300°C

PIN CONFIGURATION



DD PACKAGE
10-LEAD (3mm × 3mm) PLASTIC DFN
T_{JMAX} = 150°C, θ_{JC} = 5°C/W
SED PAD (PIN 11) IS GND, MUST BE SOLDERED TO PCB



MS PACKAGE
10-LEAD PLASTIC MSOP
T_{JMAX} = 150°C, θ_{JC} = 45°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT4294IDD#PBF	LT4294IDD#TRPBF	LHBX	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C
LT4294HDD#PBF	LT4294HDD#TRPBF	LHBX	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LT4294IMS#PBF	LT4294IMS#TRPBF	LTHBW	10-Lead Plastic MSOP	–40°C to 85°C
LT4294HMS#PBF	LT4294HMS#TRPBF	LTHBW	10-Lead Plastic MSOP	–40°C to 125°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	VPORT Operating Input Voltage	At VPORT Pin	●			60	V
V_{SIG}	VPORT Signature Range	At VPORT Pin	●	1.5		10	V
V_{CLASS}	VPORT Classification Range	At VPORT Pin	●	12.5		21	V
V_{MARK}	VPORT Mark Range	At VPORT Pin, Preceded by V_{CLASS}	●	5.6		10	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	VPORT Aux Mode Range	At VPORT Pin, AUX > V_{AUXT}	●	8		60	V
	Signature/Class Hysteresis Window		●	1.0			V
V_{RESET}	Reset Threshold	At VPORT Pin, Preceded by V_{CLASS}	●	2.6		5.6	V
V_{HSON}	Hot Swap Turn-On Voltage		●		35	37	V
V_{HSOFF}	Hot Swap Turn-Off Voltage		●	30	31		V
	Hot Swap On/Off Hysteresis Window		●	3			V
Supply Current							
	Supply Current	V_{VPORT} = V_{HSSRC} = 57V	●			2	mA
	Supply Current During Classification	V_{VPORT} = 17.5V, RCLASS and RCLASS++ Open	●	0.4	0.7	0.9	mA
	Supply Current During Mark Event	V_{VPORT} = V_{MARK} After 1st Classification Event	●	0.5		2.2	mA
Detection and Classification Signature							
	Detection Signature Resistance	V_{SIG} (Note 2)	●	23.7	24.4	25.2	kΩ
	Resistance During Mark Event	V_{MARK} (Note 2)	●	5.8	8.3	11	kΩ
	RCLASS/RCLASS++ Operating Voltage	–10mA ≥ I_{RCLASS} ≥ –36mA, V_{CLASS}	●	1.32	1.40	1.43	V
	Classification Signature Stability Time	V_{VPORT} Step to 17.5V, 34.8Ω from RCLASS or RCLASS++ to GND	●			2	ms
Analog/Digital Interface							
V_{AUXT}	AUX Threshold		●	6.1	6.3	6.5	V
I_{AUXH}	AUX Pin Hysteresis Current	V_{AUX} = 6.1V	●	3.2	5	7	µA
	$\overline{T2P}$ Output Low	1mA Load	●			0.8	V
	PWRGD Output Low	1mA Load	●			0.8	V
	PWRGD Leakage Current	V_{PWRGD} = 60V	●			5	µA
	$\overline{T2P}$ Leakage Current	$\overline{T2P}$ = 60V	●			5	µA
Hot Swap Control							
I_{GPU}	HSGATE Pull-Up Current	V_{HSGATE} – V_{HSSRC} = 5V (Note 6)	●	–27	–22	–18	µA
V_{GOC}	HSGATE Open Circuit Voltage	–10µA Load, with Respect to HSSRC	●	10		18	V
	HSGATE Pull-Down Current	V_{HSGATE} – V_{HSSRC} = 5V	●	200			µA
Timing							
f_{T2P}	$\overline{T2P}$ Frequency	After PWRGD Valid, if IEEE802.3bt PSE Is Mutually Identified	●	690	840	990	Hz
	$\overline{T2P}$ Duty Cycle in PoE Operation (Note 5)	After 4-Event Classification After 5-Event Classification (RCLASS++ Has Resistor to GND)			50 25		% %
	$\overline{T2P}$ Duty Cycle in Auxiliary Supply Operation (Note 5)	V_{AUX} > V_{AUXT}, and RCLASS++ Has Resistor to GND			25		%

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Signature resistance specifications do not include resistance added by the external diode bridge which can add as much as 1.1k to the port resistance.

Note 3: All voltages with respect to GND unless otherwise noted. Positive currents are into pins; negative currents are out of pins unless otherwise noted.

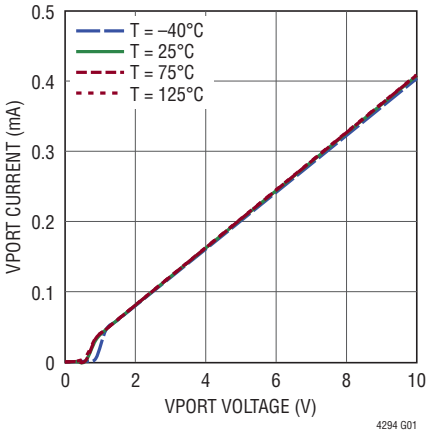
Note 4: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 150°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 5: Specified as the percentage of the period which $\overline{T2P}$ is low impedance with respect to GND.

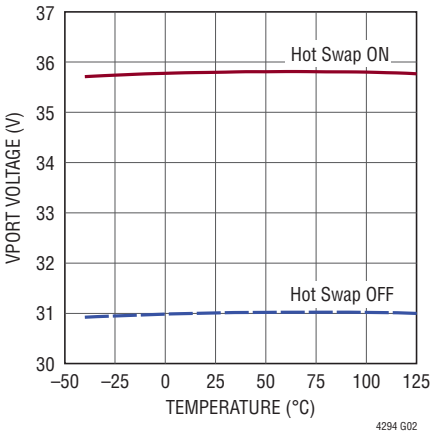
Note 6: I_{GPU} available in PoE powered operation. That is, available after V_{VPORT} > V_{HSON} and V_{AUX} < V_{AUXT}, over the range where V_{VPORT} is between V_{HSOFF} and 60V.

TYPICAL PERFORMANCE CHARACTERISTICS

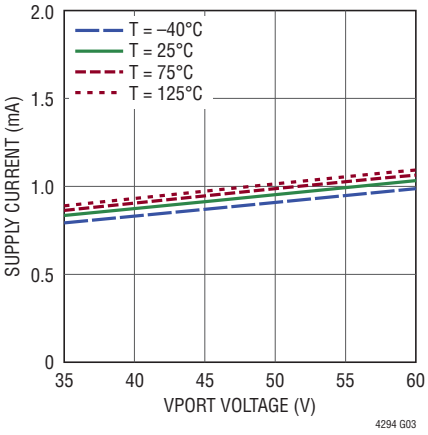
Input Current vs Input Voltage 25k Detection Signature Range



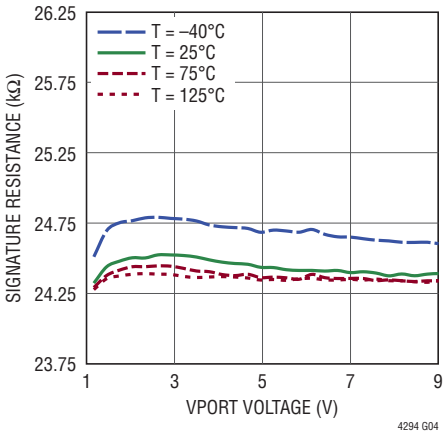
VPORT Hot Swap Thresholds



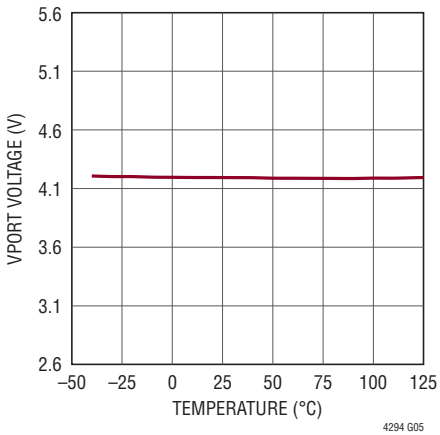
Supply Current During Power-On



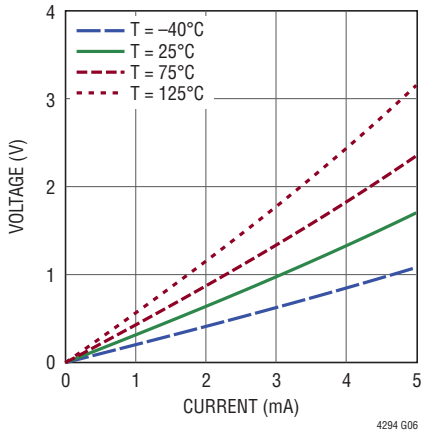
Detection Signature Resistance vs Input Voltage



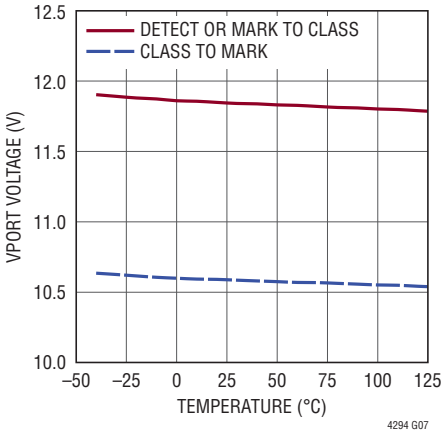
Reset Threshold



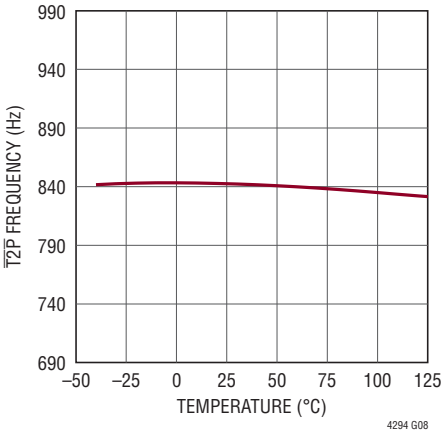
PWRGD, $\overline{T2P}$ Output Low Voltage vs Current



VPORT Classification Thresholds



$\overline{T2P}$ Frequency



PIN FUNCTIONS

GND (Pins 1, 5, DFN Exposed Pad Pin 11): Device Ground. Exposed Pad must be electrically and thermally connected to pin 5 and PCB GND.

AUX (Pin 2): Auxiliary Sense. A resistive divider from the auxiliary power input to AUX sets the voltage at which the auxiliary supply takes over. In auxiliary power operation, HSGATE pulls down, the signature resistor disconnects, classification is disabled, the PWRGD pin is high impedance and $\overline{T2P}$ indicates max available power. The AUX pin sinks I_{AUXH} when below its threshold voltage of V_{AUXT} to provide hysteresis. Connect to GND when not used.

RCLASS (Pin 3): Configurable PoE Classification Resistor. See Table 2.

RCLASS++ (Pin 4): Configurable PoE Classification Resistor. See Table 2.

$\overline{T2P}$ (Pin 6): PSE Type Indicator, Open-Drain Output. See the $\overline{T2P}$ Output section for pin behavior.

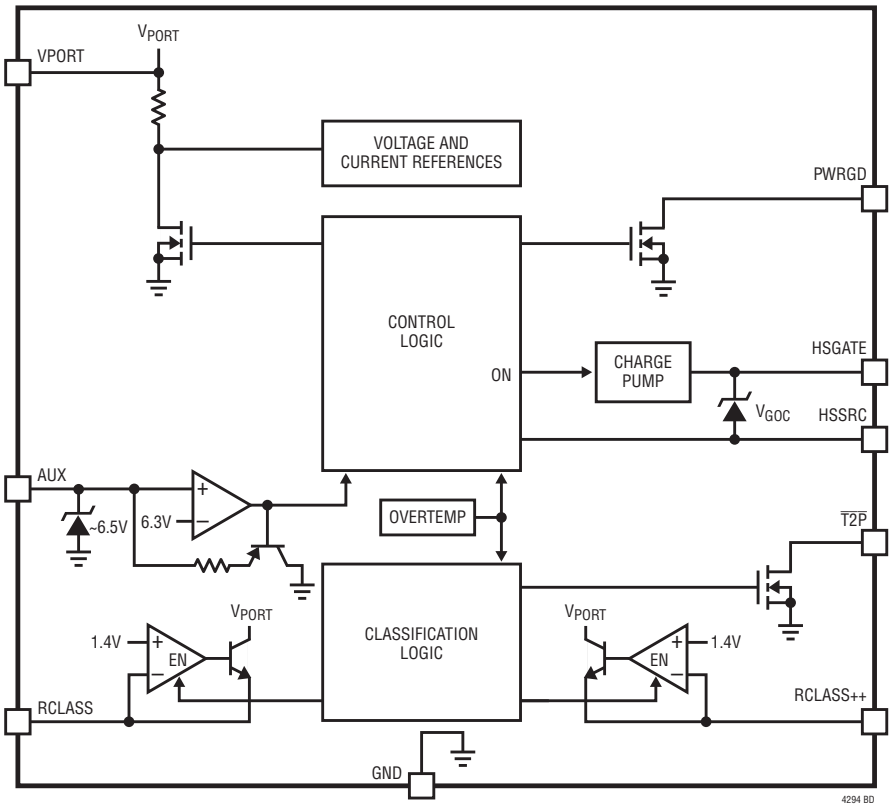
PWRGD (Pin 7): Power Good Indicator, Open-Drain Output. Pulls to GND during V_{CLASS} and inrush.

HSSRC (Pin 8): External Hot Swap MOSFET Source. Connect to source of the external MOSFET.

HSGATE (Pin 9): External Hot Swap MOSFET Gate Control, Output. Connect to gate of the external MOSFET.

VPORT (Pin 10): PD interface upper power rail and external Hot Swap MOSFET drain connection.

BLOCK DIAGRAM



APPLICATIONS INFORMATION

OVERVIEW

Power over Ethernet (PoE) continues to gain popularity as products take advantage of DC power and high speed data available from a single RJ45 connector. Powered device (PD) equipment vendors are running into the 25.5W power limit established by the IEEE 802.3at standard.

The LT4294 is an IEEE 802.3bt-compliant PD interface controller, and allows up to 71.3W operation while maintaining backwards compatibility with existing PSE systems. The $\overline{T2P}$ output indicates the number of classification events received during IEEE 802.3bt-compliant mutual identification and negotiation of available power. The LT4294 controls a low $R_{DS(ON)}$ N-channel MOSFET to maximize efficiency and delivered power.

Analog Devices also provides the LT4295, an IEEE 802.3bt-compliant PD with an integrated switching regulator to service applications that require a more compact and integrated solution.

IEEE 802.3bt vs LTPoE++ Available Power

The LT4294 supports IEEE 802.3bt PD power levels up to 71.3W.

The LT4275 and LT4276 are available to support PD power levels up to 90W under the LTPoE++ standard. See the Related Parts section for a list of LTPoE++ products.

MODES OF OPERATION

Detection Signature

During detection, the PSE looks for a 25k signature resistor which identifies the device as a PD. The PSE will apply two voltages in the range of 2.7V to 10.1V and measure the corresponding currents. Figure 1 shows the detection voltages. The PSE calculates the signature resistance using a $\Delta V/\Delta I$ measurement technique.

The LT4294 presents its precision, temperature-compensated 24.4k resistor between the VPORT and GND pins, allowing the PSE to recognize a PD is present and requesting power to be applied. The LT4294 signature resistor is smaller than 25k to compensate for the additional series resistance introduced by the IEEE required bridge or the LT4321-based ideal diode bridge.

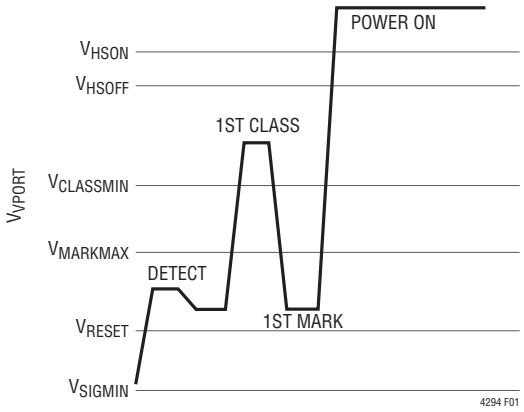


Figure 1. Type 3 or 4 PSE, 1-Event Class Sequence

IEEE 802.3bt Single-Signature vs Dual-Signature PDs

IEEE 802.3bt defines two PD topologies: single-signature and dual-signature. The LT4294 primarily targets single-signature PD topologies, eliminating the need for a second PD controller. All PD descriptions and IEEE 802.3 standard references in this data sheet are limited in scope to single-signature PDs.

The LT4294 may be deployed in dual-signature PD applications. For more information, contact Analog Devices Applications.

Classification Signature and Mark

The classification/mark process varies depending on the PSE type. A PSE, after a successful detection, may apply a classification probe voltage of 14.5V to 20.5V and measure the PD classification signature current. Once the PSE applies a classification probe voltage, the PSE returns the PD voltage to the mark voltage range before applying another classification probe voltage, or powering up the PD.

An example of 1-Event classification is shown in Figure 1. In 2-Event classification, a PSE probes for power classification twice as shown in Figure 2. An IEEE 802.3bt PSE may apply as many as 5 events before powering up the PD.

APPLICATIONS INFORMATION

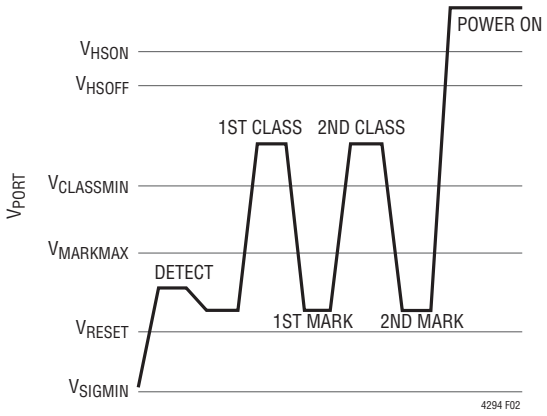


Figure 2. Type 2 PSE, 2-Event Class Sequence

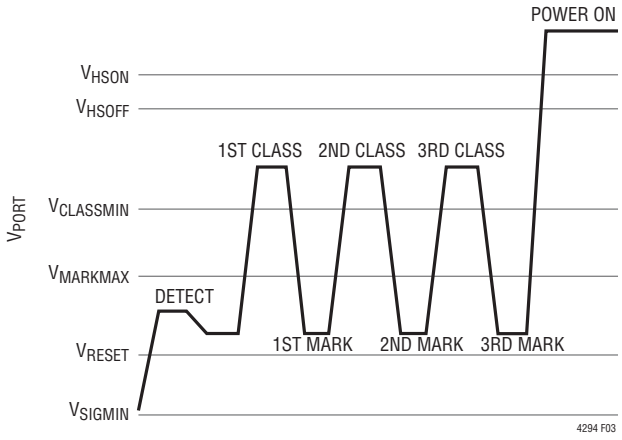


Figure 3. Type 3 or 4 PSE, 3-Event Class Sequence

IEEE 802.3bt Physical Classification and Demotion

IEEE 802.3bt defines physical classification to allow a PD to request a power allocation from the connected PSE and to allow the PSE to inform the PD of the PSE's available power. Demotion is provided if the PD Requested Power level is not available at the PSE. If demoted, the PD must operate in a lower power state.

The number of class/mark events issued by the PSE directly indicates the power allocated to the PD and is summarized in Table 1.

IEEE 802.3bt provides nine PD classes and four PD types, as shown in Table 2. The LT4294 class is configured by setting the R_{CLS} and R_{CLS++} resistor values.

Table 1. PSE Allocated Power

PD REQUESTED CLASS	NUMBER OF PSE CLASS/MARK EVENTS				
	1	2	3	4	5
0	13W				
1	3.84W				
2	6.49W				
3	13W				
4	**13W**	25.5W			
5	**13W**	**25.5W**		40W	
6	**13W**	**25.5W**		51W	
7	**13W**	**25.5W**		**51W**	62W
8	**13W**	**25.5W**		**51W**	71.3W

Note: Bold indicates the PD has been demoted.

Table 2. Single-Signature Classification, Power Levels and Resistor Selection

PD REQUESTED CLASS	PD REQUESTED POWER	PD TYPE	NOMINAL CLASS CURRENT	RESISTOR (1%)	
				R_{CLS}	R_{CLS}++
0	13W	Type 1	2.5mA	1.00kΩ	Open
1	3.84W	Type 1 or 3	10.5mA	140Ω	Open
2	6.49W	Type 1 or 3	18.5mA	76.8Ω	Open
3	13W	Type 1 or 3	28mA	49.9Ω	Open
4	25.5W	Type 2 or 3	40mA	34.8Ω	Open
5	40W	Type 3	40mA/2.5mA	1.00kΩ	37.4Ω
6	51W	Type 3	40mA/10.5mA	140Ω	46.4Ω
7	62W	Type 4	40mA/18.5mA	76.8Ω	64.9Ω
8	71.3W	Type 4	40mA/28mA	49.9Ω	118Ω

APPLICATIONS INFORMATION

IEEE 802.3bt PSEs present a single classification event (see Figure 1) to Class 0 through 3 PDs. A Class 0 through 3 PD presents its class signature to the PSE and is then powered on if sufficient power is available. Power limited IEEE 802.3bt PSEs may issue a single event to Class 4 and higher PDs in order to demote those PDs to Class 3 (13W).

IEEE 802.3bt PSEs present up to three classification events, depending on PSE Type, to Class 4 PDs (see Figure 3). Class 4 PDs present a class signature 4 on all events. The third event differentiates a Class 4 PD from a higher Class PD. Power-limited IEEE 802.3bt PSEs may issue three events to Class 5 and higher PDs in order to demote those PDs to Class 4 (25.5W).

IEEE 802.3bt PSEs present four classification events (see Figure 4) to Class 5 and 6 PDs. Class 5 and 6 PDs present a class signature 4 on the first two events, then present a class signature 0 or 1, respectively, on the remaining events. Power limited IEEE 802.3bt PSEs may issue four events to Class 7 and higher PDs in order to demote those PDs to Class 6 (51W).

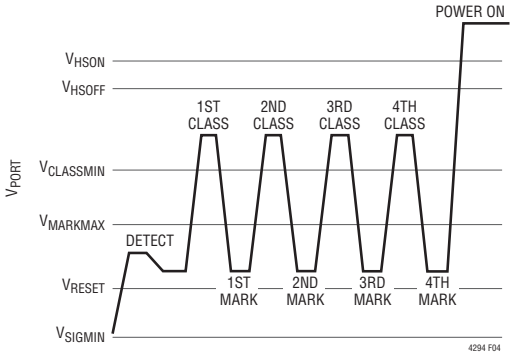


Figure 4. Type 3 or 4 PSE, 4-Event Class Sequence

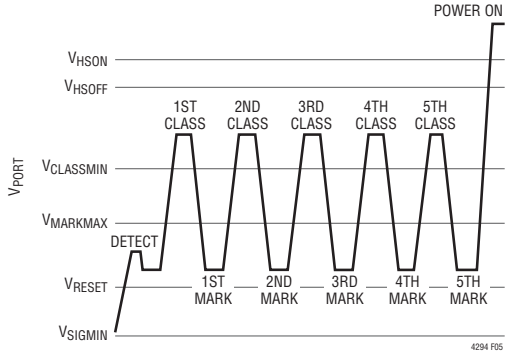


Figure 5. Type 4 PSE, 5-Event Class Sequence

IEEE 802.3bt PSEs present five classification events (see Figure 5) to Class 7 and 8 PDs. Class 7 and 8 PDs present a class signature 4 on the first two events, then present a class signature 2 or 3, respectively, on the remaining events.

The number of class/mark events is communicated through the LT4294 $\overline{T2P}$ pin. See $\overline{T2P}$ Output section for more details.

Classification Resistors (R_{CLS} and R_{CLS++})

The R_{CLS} and R_{CLS++} resistors set the classification currents corresponding to the PD power classification. Select the value of R_{CLS} and R_{CLS++} from Table 2 and connect each 1% resistor between the RCLASS, RCLASS++ pins and GND.

Detection Signature Corrupt During Mark Event

During the mark event, the LT4294 presents <11kΩ to the port as required by the IEEE 802.3 specification.

Inrush and Power On

Once the PSE detects and classifies the PD, the PSE then powers on the PD. When the port voltage rises above the V_{HSON} threshold, it begins to source I_{GPU} out of the HSGATE pin. This current flows into an external capacitor, C_{GATE} in Figure 6, that causes a voltage to ramp up the gate of the external MOSFET. The external MOSFET acts as a source follower and ramps the voltage up on the output bulk capacitor, C_{PORT}, thereby determining the inrush current, I_{INRUSH}. Design I_{INRUSH} to be approximately ~100mA. See equation below:

$$I_{INRUSH} = I_{GPU} \bullet \frac{C_{PORT}}{C_{GATE}}$$

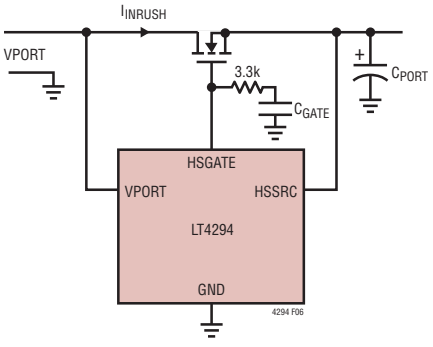


Figure 6. Configuring I_{INRUSH}

APPLICATIONS INFORMATION

The LT4294 internal charge pump provides an N-channel MOSFET solution, eliminating a larger and more costly P-channel MOSFET. The low $R_{DS(ON)}$ MOSFET also maximizes power delivery and efficiency, reduces power and heat dissipation, and eases thermal design.

Power Good

The PWRGD pin is held low by its open drain output until HSGATE charges up to approximately 7V above HSSRC. The PWRGD pin is used to hold off the downstream circuitry until inrush is complete and the external MOSFET is fully enhanced. The HSGATE pin remains high and the PWRGD pin remains open-drain until the port voltage falls below V_{HSOFF}.

Delay Start

When the PSE powers up the port, the PD application should not draw more than 350mA for 80ms to comply with the IEEE 802.3 standard.

Auxiliary Supply Override

If the AUX pin is held above V_{AUXT}, the LT4294 enters auxiliary power supply override mode. In this mode the signature resistor disconnects, classification is disabled, HSGATE pulls down, the PWRGD pin is open drain and $\overline{T2P}$ pin indicates max available power.

The AUX pin allows for setting the auxiliary supply turn on and turn off voltage thresholds, V_{AUXON}, and V_{AUXOFF} respectively. The auxiliary supply hysteresis voltage, V_{AUXHYS}, is generated with sinking current, I_{AUXH}, and is active only when the AUX pin voltage is less than V_{AUXT}. Use the following equations to set V_{AUXON} and V_{AUXOFF} via R1 and R2 in Figure 7. Note that an internal 6.5V Zener limits the voltage on the AUX pin.

$$R1 = \frac{V_{AUXON} - V_{AUXOFF}}{I_{AUXH}} = \frac{V_{AUXHYS}}{I_{AUXH}}$$

$$R2 = \frac{R1}{\left(\frac{V_{AUXOFF}}{V_{AUXT}} - 1\right)}$$

$$R1 \geq \frac{V_{AUX(MAX)} - V_{AUXT}}{1.4mA}$$

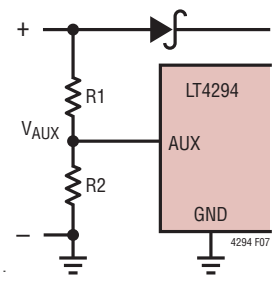


Figure 7. AUX Threshold and Hysteresis Calculation

A capacitor up to 1000pF may be placed between the AUX pin and GND to improve noise immunity. V_{AUXON} must be lower than V_{HSOFF}.

$\overline{T2P}$ Output

The LT4294 communicates the PSE allocated power to the PD application via the $\overline{T2P}$ pin. The $\overline{T2P}$ pin state is determined by the AUX pin, the RCLASS^{++} pin, and the number of classification events. The LT4294 uses a 4-state encoding for the $\overline{T2P}$ output. $\overline{T2P}$ state and the associated PSE allocated power are shown in Table 3.

Table 3. $\overline{T2P}$ Response to Determine PSE Allocated Power

STATE	PD REQUESTED CLASS	NUMBER OF CLASSIFICATION EVENTS	$\overline{T2P}$*	PSE ALLOCATED POWER
Auxiliary	0-4	N/A	Low-Z	AUX Power
	5-8	N/A	25%	AUX Power
PoE	0-4	1	Hi-Z	Min (PD Requested Power, 13W)
		≥ 2	Low-Z	25.5W
	5-8	1	Hi-Z	13W
		2 or 3	Low-Z	25.5W
		4	50%	Min (PD Requested Power, 51W)
		5	25%	Min (PD Requested Power, 71.3W)

*Specified as the percentage of the period which $\overline{T2P}$ is low impedance with respect to GND.

The highest priority input is the AUX pin. AUX is asserted to enter the auxiliary power state and deasserted to enter the PoE state. In the auxiliary power state, the $\overline{T2P}$ pin indicates the highest available power, based on

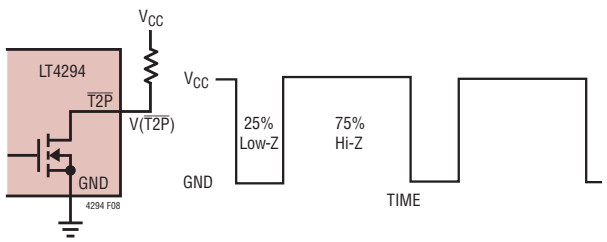


Figure 8. Response Example for 25% Low-Z, 75% Hi-Z

APPLICATIONS INFORMATION

PD Requested Class. The auxiliary power supply must be sized to provide at least the PD Requested Power.

Second, PD Requested Class and PD Requested Power are configured using the RCLASS and RCLASS++ pins. The RCLASS++ pin alone can be used to determine if the PD Class is 0-4 or 5-8, as shown in Table 2.

Last, the number of classification events determines the amount of power allocated by the PSE as described in Table 1.

Interoperability Across Various PSEs and Auxiliary Power Source

Table 4 summarizes the expected $\overline{T2P}$ response, the PSE allocated power, and the number of classification events. The result is a function of PD Requested Class and power source—Auxiliary or PoE.

Overtemperature Protection

The IEEE 802.3 specification requires a PD to withstand any applied voltage from 0V to 57V indefinitely. During classification, however, the power dissipation in the LT4294 may be as high as 1.5W. The LT4294 can easily tolerate this power for the maximum IEEE classification timing but overheats if this condition persists abnormally.

The LT4294 includes an overtemperature protection feature which is intended to protect the device during momentary overload conditions. If the junction temperature exceeds the overtemperature threshold, the LT4294 pulls down HSGATE pin, and disables classification.

EXTERNAL INTERFACE AND COMPONENT SELECTION

PoE Input Bridge

A PD is required to polarity-correct its input voltage. There are several different options available for bridge rectifiers;

Table 4. LT4294 Interoperability ($\overline{T2P}$ Response*, PSE Allocated Power, Number of Classification Events)

	PSE TYPE, CLASS (POWER)							
	IEEE 802.3 TYPE 1	IEEE 802.3 TYPE 2	IEEE 802.3 TYPE 3			IEEE 802.3 TYPE 4		AUXILIARY POWER SOURCE**
PD REQUESTED CLASS (PD REQUESTED POWER)	CLASS 3 (13W)	CLASS 4 (25.5W)	CLASS 4 (25.5W)	CLASS 5 (40W)	CLASS 6 (51W)	CLASS 7 (62W)	CLASS 8 (71.3W)	
CLASS 0–3 (Up to 13W)	Hi-Z Up to 13W 1-Event	Hi-Z Up to 13W 1-Event	Hi-Z Up to 13W 1-Event	Hi-Z Up to 13W 1-Event	Hi-Z Up to 13W 1-Event	Hi-Z Up to 13W 1-Event	Hi-Z Up to 13W 1-Event	Low-Z Aux. Power N/A
CLASS 4 (25.5W)	Hi-Z 13W 1-Event	Low-Z 25.5W 2-Event	Low-Z 25.5W 3-Event	Low-Z 25.5W 3-Event	Low-Z 25.5W 3-Event	Low-Z 25.5W 3-Event	Low-Z 25.5W 3-Event	Low-Z Aux. Power N/A
CLASS 5 (40W)	Hi-Z 13W 1-Event	Low-Z 25.5W 2-Event	Low-Z 25.5W 3-Event	50% 40W 4-Event	50% 40W 4-Event	50% 40W 4-Event	50% 40W 4-Event	25% Aux. Power N/A
CLASS 6 (51W)	Hi-Z 13W 1-Event	Low-Z 25.5W 2-Event	Low-Z 25.5W 3-Event	Low-Z 25.5W 3-Event	50% 51W 4-Event	50% 51W 4-Event	50% 51W 4-Event	25% Aux. Power N/A
CLASS 7 (62W)	Hi-Z 13W 1-Event	Low-Z 25.5W 2-Event	Low-Z 25.5W 3-Event	Low-Z 25.5W 3-Event	50% 51W 4-Event	25% 62W 5-Event	25% 62W 5-Event	25% Aux. Power N/A
CLASS 8 (71.3W)	Hi-Z 13W 1-Event	Low-Z 25.5W 2-Event	Low-Z 25.5W 3-Event	Low-Z 25.5W 3-Event	50% 51W 4-Event	50% 51W 4-Event	25% 71.3W 5-Event	25% Aux. Power N/A

↓

$\overline{T2P}$ Response* →	25%
PSE Allocated Power →	71.3W
Number of Classification Events →	5-Event

Note 1. Shade of blue indicates the PD has been demoted or denied power.

* Specified as the percentage of the period which $\overline{T2P}$ is low impedance with respect to GND.

** Auxiliary Power Supply must be sized to provide PD Requested Power.

APPLICATIONS INFORMATION

silicon diodes, Schottky diodes, and ideal diodes. When silicon or Schottky diode bridges are used, the diode forward voltage drops affect the voltage at the VPORT pin. The LT4294 is designed to tolerate these voltage drops. Note, the voltage parameters shown in the Electrical Characteristics are specified at the LT4294 package pins.

A silicon diode bridge consumes up to 4% of the available power. In addition, silicon diode bridges exhibit poor pairset-to-pairset unbalance performance. Each branch of a silicon diode bridge shares source/return current, and thermal runaway can cause large, non-compliant current unbalances between pairsets.

While using Schottky diodes can help reduce the power loss with a lower forward voltage, the Schottky bridge may not be suitable for high temperature PD applications. Schottky diode bridges exhibit temperature induced leakage currents. The leakage current has a voltage dependency that can invalidate the measured detection signature. In addition, these leakage currents can back-feed through the unpowered branch and the unused bridge, violating IEEE 802.3 specifications.

For high efficiency applications, the LT4294 supports an LT4321-based PoE ideal diode bridge that reduces the forward voltage drop from 0.7V to 20mV per diode while maintaining IEEE 802.3 compliance. The LT4321 simplifies thermal design, eliminates costly heatsinks, and can operate in space-constrained applications.

Auxiliary Input Diode Bridge

Some PDs are required to receive AC or DC power from an auxiliary power source. A diode bridge is typically required to handle the voltage rectification and polarity correction.

In high efficiency applications, or in low auxiliary input voltage applications, the voltage drop across the rectifier cannot be tolerated. The LT4294 can be configured with an LT4320-based ideal diode bridge to recover the diode voltage drop and ease thermal design.

For applications with auxiliary input voltages below 10V, the LT4294 must be configured with an LT4320-based ideal diode bridge to recover the voltage drop and guarantee the minimum VPORT voltage is within the VPORT AUX Mode Range as specified in the Electrical Characteristics table.

An example of a high efficiency typical application circuit is show in the Typical Application section.

Input Capacitor

A 0.1µF capacitor is needed from V_{PORT} to GND to meet the input impedance requirement in IEEE 802.3 and to properly bypass the LT4294. When operating with the LT4321, locally bypass each with a 0.047µF capacitor, thus keeping the total port capacitance within specification.

Transient Voltage Suppressor

The LT4294 specifies an absolute maximum voltage of 100V and is designed to tolerate brief overvoltage events due to Ethernet cable surges. To protect the LT4294 from an overvoltage event, install a unidirectional transient voltage suppressor (TVS) such as an SMAJ58A between the V_{PORT} and GND pins. For PD applications that require an auxiliary power input, install a TVS between V_{IN} and GND. See Layout Considerations for TVS placement.

For extremely high cable discharge and surge protection, contact Analog Devices Applications.

Exposed Pad

The LT4294 DFN package has an exposed pad that is internally electrically connected to GND. The exposed pad may only be connected to GND on the printed circuit board.

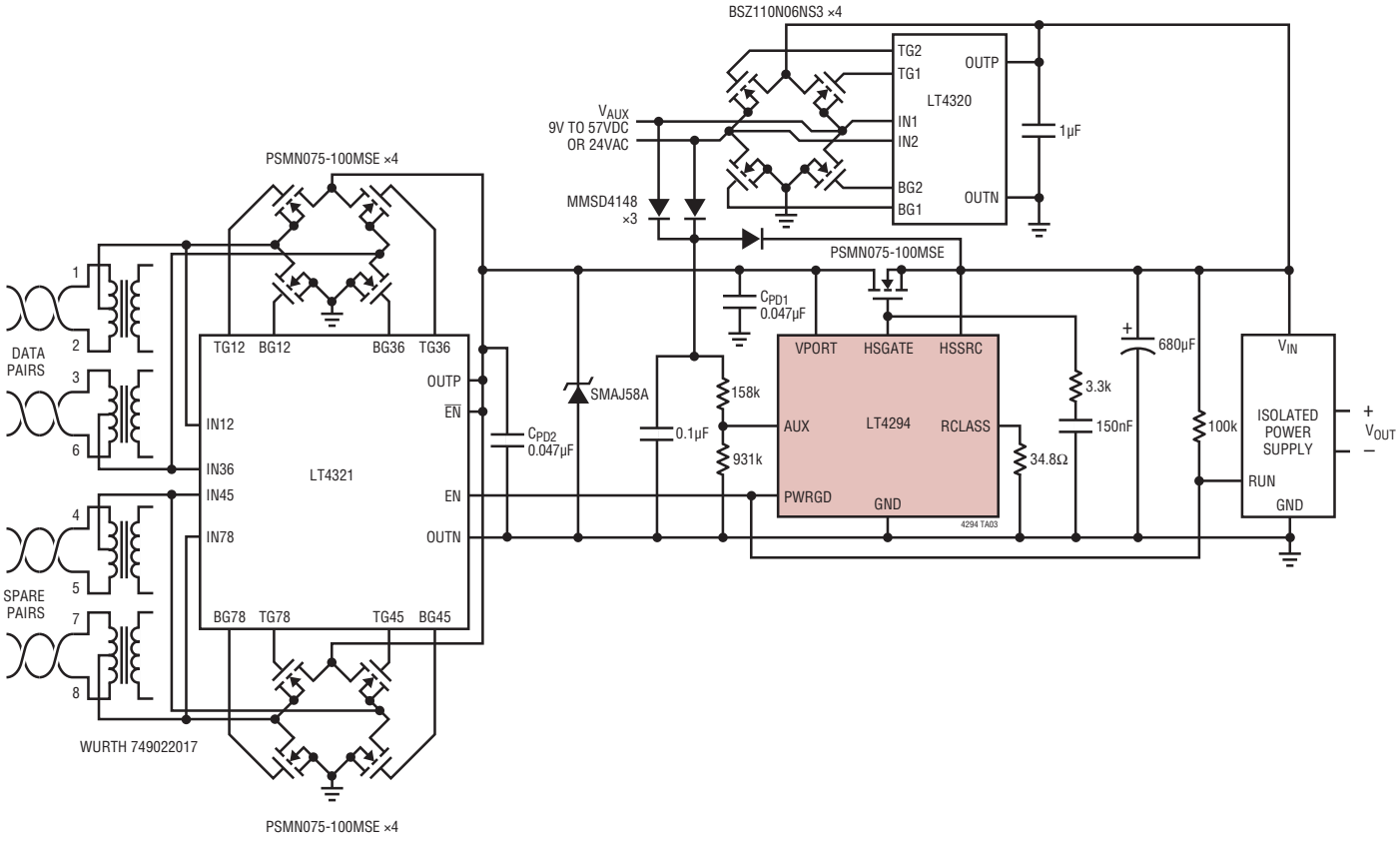
LAYOUT CONSIDERATIONS

Avoid excessive parasitic capacitance on the RCLASS and RCLASS++ pins and place resistors R_{CLS} and R_{CLS++} close to the LT4294.

It is strictly required for maximum protection to place the 0.1µF input capacitor, C_{PD}, and transient voltage suppressor as close to the LT4294 as possible. When operating the LT4294 with the LT4321, place a 0.047µF capacitor, C_{PD1}, as close as possible to the LT4294 VPORT and GND pins (pin 10 and pin 5, respectively), and a 0.047µF capacitor, C_{PD2}, as close as possible to the LT4321 OUTP and OUTN pins.

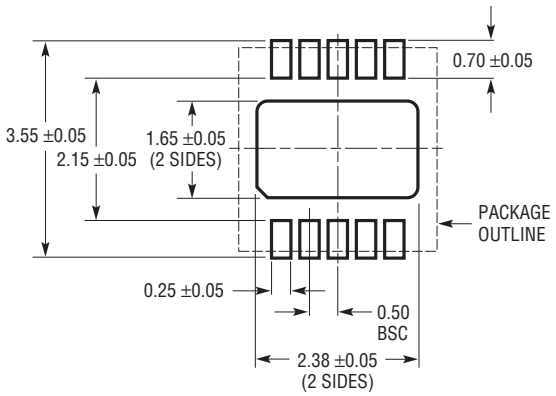
TYPICAL APPLICATIONS

High Efficiency 25.5W PD Solution with $12V_{DC}$ and $24V_{AC}$ Auxiliary Input

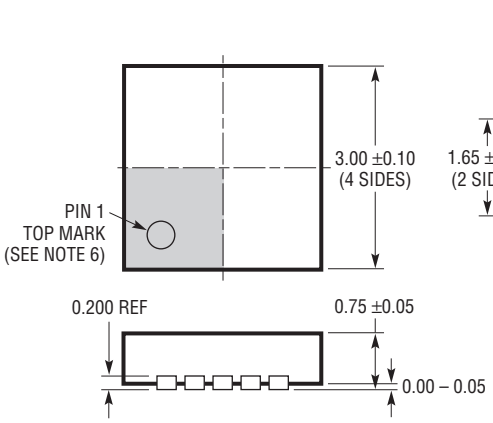


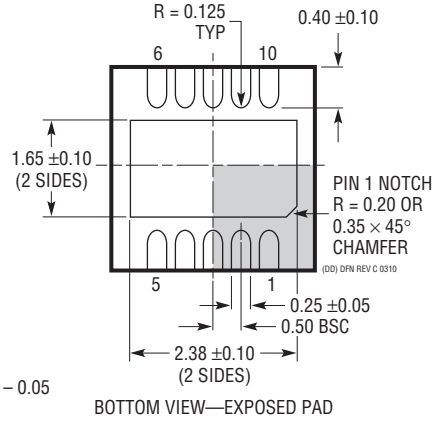
PACKAGE DESCRIPTION

DD Package
10-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1699 Rev C)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



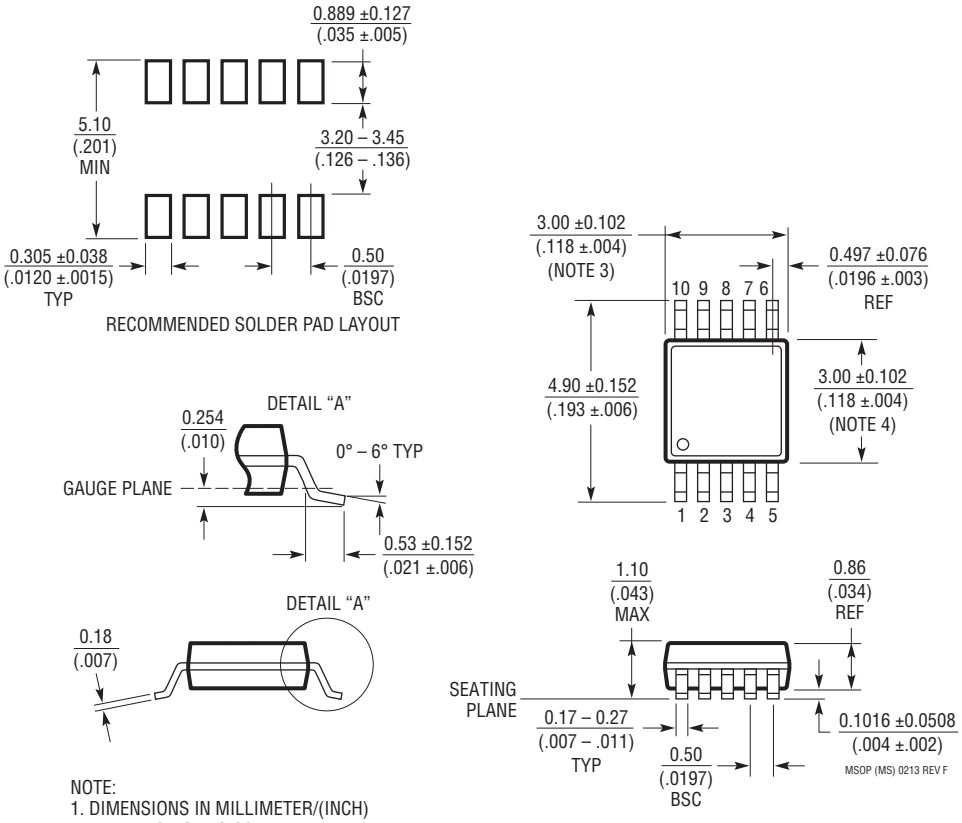


BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-2). CHECK THE LTC WEBSITE DATA SHEET FOR CURRENT STATUS OF VARIATION ASSIGNMENT
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

MS Package
10-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1661 Rev F)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	09/18	Updated to IEEE 802.3af/at/bt (Draft 3.5) Revised $\overline{T2P}$ Output Applications Information Revised External Interface and Component Selection Applications Information	1-16 10, 11 11, 12
B	04/19	Removed Draft Number Added Table 4 – Interoperability	1-16 11