PoE Ideal Diode Bridge Controller

FEATURES

- Reduces Heat, Eliminates Thermal Design Problems
- Maximizes Power Efficiency
- Less than 800µA Quiescent Operating Current
- Fully Compatible with IEEE 802.3af/at/bt Detection and Classification
- IEEE 802.3af/at/bt Compliant When Paired with a Powered Device (PD) Controller
- Works with 2-Pair and 4-Pair PoE Applications
- Compatible with PoE, PoE+, PoE++, and LTPoE++®
- 100V Absolute Maximum Voltage
- H-Grade Version Operates Up to 125°C
- 16-Lead 4mm × 4mm QFN Package

APPLICATIONS

- PoE/PoE+/PoE++/LTPoE++ Powered Devices
- DC Polarity Correction and Ideal Diode-ORing of Telecom Supplies

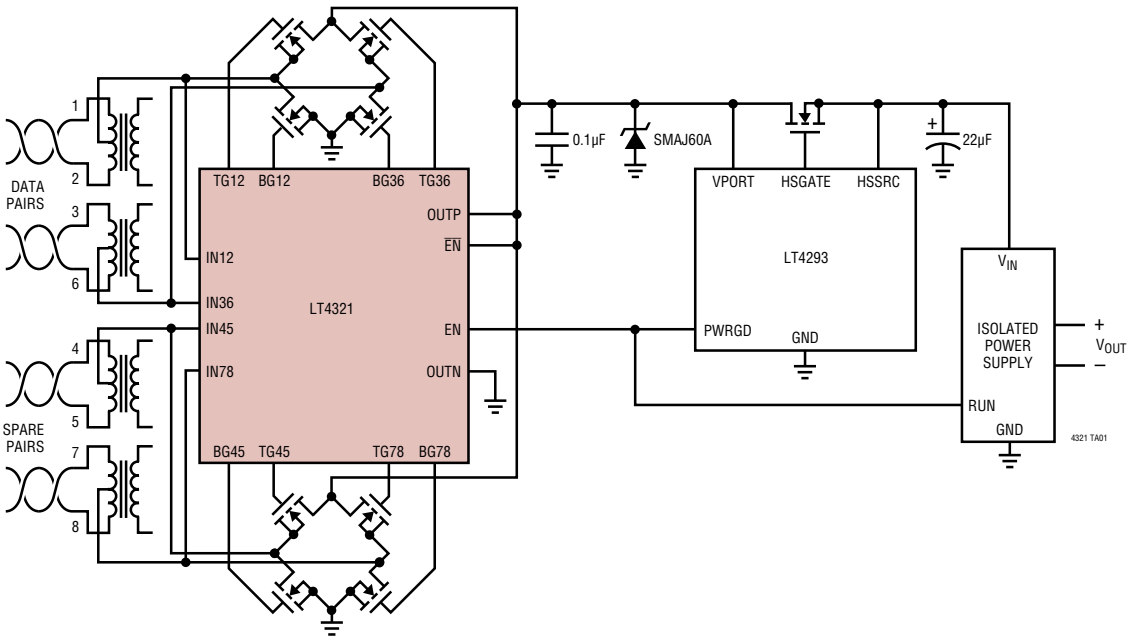
DESCRIPTION

The LT®4321 is a dual ideal diode bridge controller that enables a Power over Ethernet (PoE) powered device (PD) to receive power in either voltage polarity from RJ-45 data pairs, spare pairs, or both. The LT4321 and eight N-channel MOSFETs replace the eight diodes in a passive PoE rectifier bridge. The LT4321 eases thermal design and increases delivered power.

An internal charge pump allows an all-NMOS bridge eliminating larger and more costly PMOS switches. The LT4321 works with 2-pair and 4-pair applications. High impedance input sense pins prevent reverse current on unused pairs. If the power source fails or is shorted, a fast turn-off minimizes reverse current transients. Unlike discrete ideal bridge solutions, the LT4321 will operate through transients without enabling the MOSFETs on unpowered pairs.

TYPICAL APPLICATION

Powered Device for PoE (to 13W), PoE+ (to 25.5W), PoE++ (to 71.3W) or LTPoE++ (to 90W) Systems



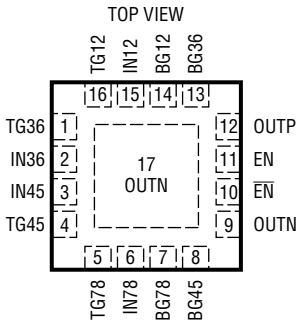
Rev. A

ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

OUTP – OUTN ..... –0.3V to 100V
IN12, IN36, IN45, IN78 ..... –2V to OUTP + 2V
BG12, BG36, BG45, BG78 Voltages ..... –0.3V to 100V
TG12, TG36, TG45, TG78
Voltages ..... –0.3V to OUTP + 12V
TG12 – IN12 Voltage ..... –0.3V to 12V
TG36 – IN36 Voltage ..... –0.3V to 12V
TG45 – IN45 Voltage ..... –0.3V to 12V
TG78 – IN78 Voltage ..... –0.3V to 12V
EN, $\overline{EN}$, ... –0.3V to 100V
Operating Ambient Temperature Range
LT4321I ..... –40°C to 85°C
LT4321H ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



UF PACKAGE
16-LEAD (4mm × 4mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JC} = 4.5°C/W
EXPOSED PAD (PIN 17) IS OUTN, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT4321IUF#PBF	LT4321IUF#TRPBF	4321	16-Lead 4mm × 4mm Plastic QFN	–40°C to 85°C
LT4321HUF#PBF	LT4321HUF#TRPBF	4321	16-Lead 4mm × 4mm Plastic QFN	–40°C to 125°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, OUTP = 20V to 80V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Operating Supply Range	|IN12 – IN36|, |IN45 – IN78|, OUTP	●	20		80	V
V_{UVLO}	Undervoltage Lockout	OUTP – OUTN	●	15	17	18	V
I_S(DET)	Total Supply Current in Detect Region	OUTP < 10V	●		0.8	5	µA
I_S(OFF)	Total Supply Current in Shutdown	OUTP > 12V, EN < V_{IL} and $\overline{EN}$ > V_{IH}	●		32	60	µA
I_S(ON)	Total Operating Supply Current	EN > V_{IH} or $\overline{EN}$ < V_{IL}, OUTP > 20V	●		0.5	0.8	mA
	Top Gate Drive	INn = OUTP + $\Delta V_{SD(MAX)}$ + 5mV, 10µA Out of TGn (Note 3)	●	7.7	9.5	11	V
V_{BG}	Bottom Gate Drive	10µA Out of BGn (Note 3)	●	10	11.5	13	V
	Top Gate Pull-Up Current	TGn = INn (Note 3)	●	50	120	250	µA
	Top Gate Pull-Down Current	INn = OUTP – 0.25V; TGn – INn = 5V	●	1.25			mA
	Bottom Gate Pull-Up Current	BGn < V_{BG} (Note 3)	●	15	30	45	µA
	Bottom Gate Pull-Down Current	BGn = 5V	●	3			mA
	$\overline{EN}$ Pull-Up Resistance (Active Low)	OUTP = 55V	●	160	250	310	kΩ
	EN Pull-Down Resistance (Active High)	OUTP = 55V	●	160	250	310	kΩ
V_{IH}	Digital Input High	EN, $\overline{EN}$	●			2.6	V
V_{IL}	Digital Input Low	EN, $\overline{EN}$	●	0.5			V
$V_{\overline{ENOC}}$	$\overline{EN}$ Open Circuit Voltage	OUTP = 55V	●	2	2.5	3	V
ΔV_{SD}	Topside Forward Regulation Voltage	INn – OUTP	●	2	10	18	mV
	Bottom Comparator Turn-On Threshold	INn – OUTN	●	–30	–15	0	mV
	Bottom Comparator Turn-Off Threshold	INn – OUTN	●	2	15	30	mV

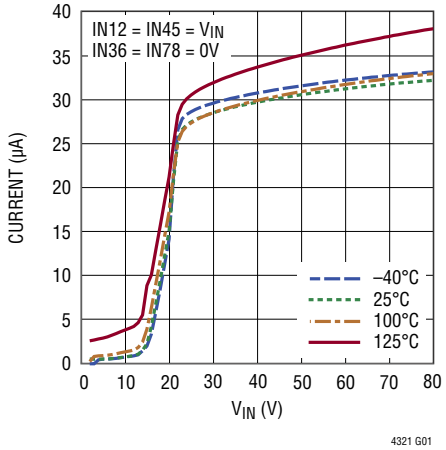
Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Referenced with respect to OUTN unless otherwise specified.

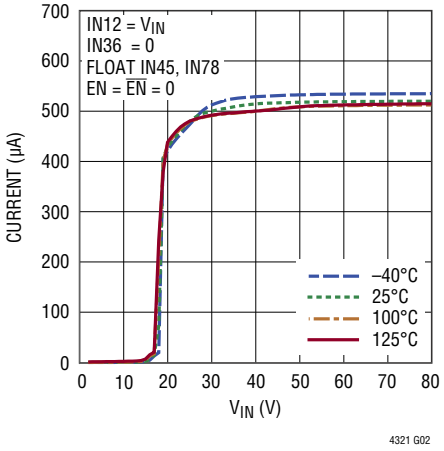
Note 3: All conditions for external MOSFET turn on must be met. See Table 1 and Table 2.

TYPICAL PERFORMANCE CHARACTERISTICS

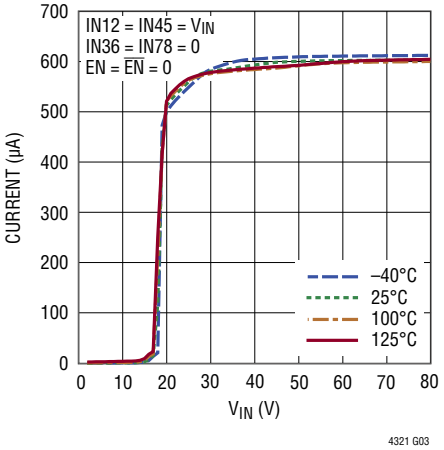
Total Supply Current in Shutdown



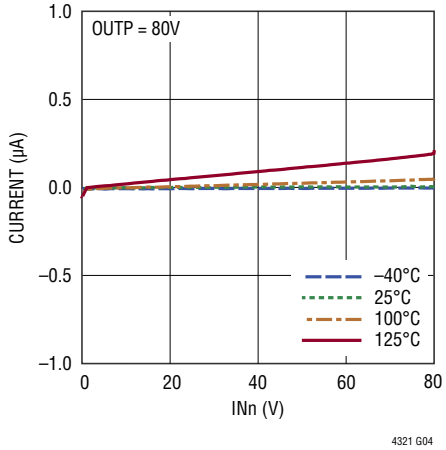
Total Supply Current in Ideal Bridge Mode, 2-Pair



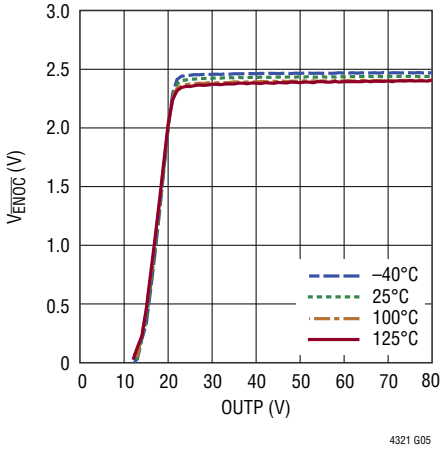
Total Supply Current in Ideal Bridge Mode, 4-Pair



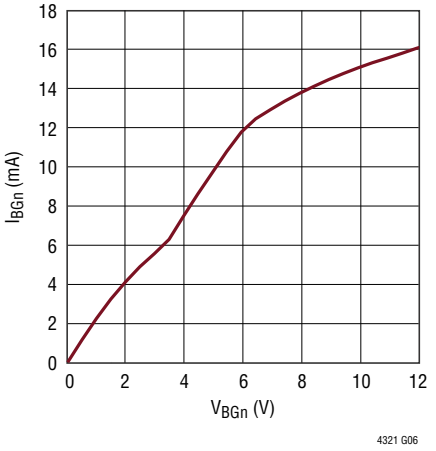
Input Pin Current



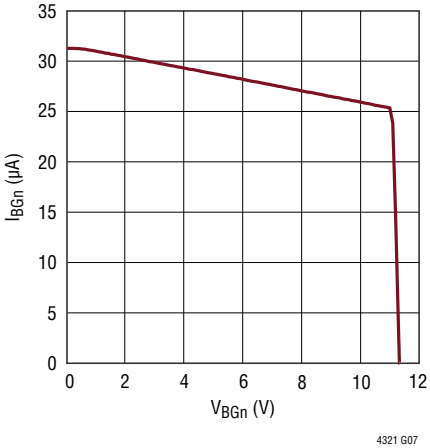
EN Open Circuit Voltage



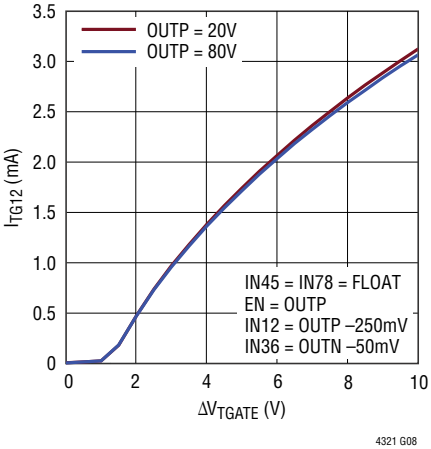
BGn Pull-Down Strength



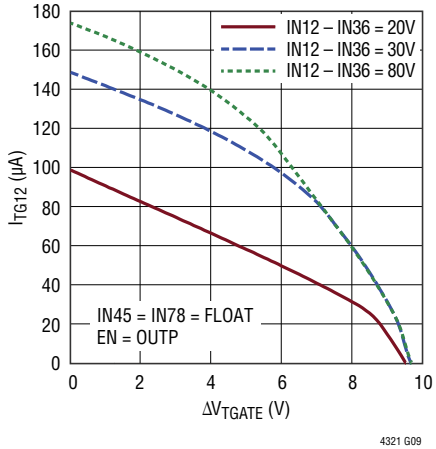
BGn Pull-Up Strength



TG Pull-Down Strength



TG Pull-Up Strength



PIN FUNCTIONS

IN12: Data Pair Input 1. In a PoE system, IN12 connects to the center tap of the transformer connected to pins 1 and 2 on an RJ45 connector.

IN36: Data Pair Input 2. In a PoE system, IN36 connects to the center tap of the transformer connected to pins 3 and 6 on an RJ45 connector.

IN45: Spare Pair Input 1. In a PoE system, IN45 connects to the center tap of the transformer connected to pins 4 and 5 on an RJ45 connector.

IN78: Spare Pair Input 2. In a PoE system, IN78 connects to the center tap of the transformer connected to pins 7 and 8 on an RJ45 connector.

TG12: Top-Side Gate Driver Output. TG12 pin pulls high with respect to IN12 when IN12 is greater than OUTP and IN36 is less than OUTN.

TG36: Top-Side Gate Driver Output. TG36 pin pulls high with respect to IN36 when IN36 is greater than OUTP and IN12 is less than OUTN.

TG45: Top-Side Gate Driver Output. TG45 pin pulls high with respect to IN45 when IN45 is greater than OUTP and IN78 is less than OUTN.

TG78: Top-Side Gate Driver Output. TG78 pin pulls high with respect to IN78 when IN78 is greater than OUTP and IN45 is less than OUTN.

BG12: Bottom-Side Gate Driver Output. BG12 pin pulls high with respect to OUTN when IN36 is greater than OUTP and IN12 is less than OUTN.

BG36: Bottom-Side Gate Driver Output. BG36 pin pulls high with respect to OUTN when IN12 is greater than OUTP and IN36 is less than OUTN.

BG45: Bottom-Side Gate Driver Output. BG45 pin pulls high with respect to OUTN when IN78 is greater than OUTP and IN45 is less than OUTN.

BG78: Bottom-Side Gate Driver Output. BG78 pin pulls high with respect to OUTN when IN45 is greater than OUTP and IN78 is less than OUTN.

$\overline{\text{EN}}$: Enable, Active Low. Pull down to OUTN to enable ideal diode bridge mode. EN is internally pulled up to $V_{\overline{ENOC}}$. Tie to OUTP if the application circuit uses the EN pin to enable ideal bridge mode.

EN: Enable, Active High. Pull up to enable ideal diode bridge mode. EN is internally pulled down to OUTN. Tie to OUTN if the application circuit uses the $\overline{\text{EN}}$ pin to enable ideal bridge mode.

OUTP: Positive Output Voltage. OUTP is the rectified voltage from which the LT4321 draws power.

OUTN: Negative Output Voltage. OUTN is the negative rectified voltage.

EXPOSED PAD: The exposed pad must be electrically connected to the OUTN pin.

APPLICATIONS INFORMATION

OVERVIEW

The LT4321 is a dual ideal diode bridge controller designed to rectify two independent DC channels into a single output. An LT4321-based solution meets IEEE 802.3 PoE requirements for a PD diode bridge and rectifies both 2-pair and 4-pair power from an Ethernet cable into a common output. The LT4321 senses the greater of the two input channels, |IN12-IN36| or |IN45-IN78|, and connects them to the output with the correct polarity. Smooth crossover between channels is guaranteed by the enforced dropout voltage, ΔV_{SD}.

A very common application is an IEEE 802.3 powered device, which is required to accept voltage in either polarity at its RJ-45 input. Polarity correction devices allow the PD to work equally well with standard or cross-over cables and endspan or midspan PSEs. They also prevent the PD from back feeding current into the Ethernet cable. There are several different options available for bridge rectifiers; silicon diodes, Schottky diodes, and ideal diodes. Traditional diode bridges lower efficiency due to the forward drop generated across two conducting diodes. This voltage drop reduces the available supply voltage and dissipates significant power.

A silicon diode bridge can consume up to 4% of the available PD power. In addition, silicon diode bridges exhibit poor pairset-to-pairset unbalance performance in 4-pair PoE++. Each branch of a silicon diode bridge shares source/return current, and thermal runaway can cause large, non-compliant current unbalances between pairsets.

While using Schottky diodes can help reduce the power loss with a lower forward voltage, the Schottky bridge may not be suitable for high temperature applications. Schottky diode bridges exhibit temperature induced leakage currents. The leakage current has a voltage dependency that can invalidate the measured detection signature. In addition, these leakage currents can back-feed through the unpowered branch and the unused bridge, violating IEEE 802.3 specifications.

The LT4321 uses actively driven MOSFETs to nearly elimi-nate the forward voltage drop. By maximizing available voltage and reducing power dissipation (Figure 1), the LT4321 simplifies PD design and reduces power supply cost. It can also eliminate thermal design problems, costly heat sinks, and reduce PC board area.

Some designs use ideal diode bridge circuits implemented with discrete components. These bridges often suffer from a trade-off between quiescent current and tolerance to transients and leakage. With quiescent current properly tuned for PoE, stray PCB leakage between bridge components can be enough to cause accidental turn-on, latchup, and destruction of the circuit.

The LT4321 offers significant improvements over discrete solutions. The integrated bridge controller allows for sophisticated sensing and control of the PowerPath™ MOSFETs, ensuring that MOSFETs that are supposed to be off, stay off. An ideal bridge controlled by the LT4321 is tolerant to hot-plugs, input shortcircuits, common mode shift, and PCB leakage in the application circuit.

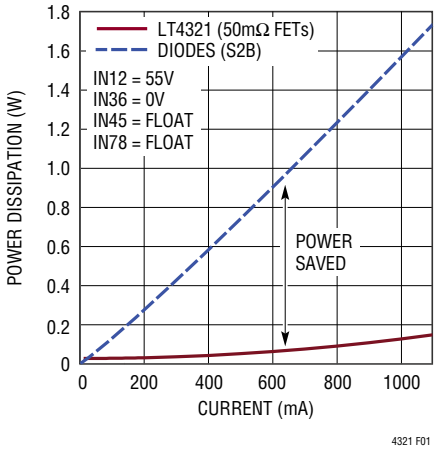


Figure 1. Power Dissipation vs Load Current

OPERATING MODES

Ideal Diode Bridge Mode

In ideal bridge mode the LT4321 saves power by activating MOSFETs in place of power path diodes. The LT4321 enters ideal bridge mode when OUTP is greater than V_{UVLO} and either EN or $\overline{EN}$ is asserted.

When the LT4321 is enabled, it senses the inputs with respect to the output to decide which external MOSFETs to turn on. Inputs are grouped into pairs, IN12/IN36 and

APPLICATIONS INFORMATION

Table 1. Conditions for Ideal Bridge Mode on IN12/IN36

PoE MODE	OUTP	EN | $\overline{EN}$	IN12	IN36	IN45	IN78	TG12	TG36	BG12	BG36
Detect/Class	< V_{UVLO}	X	X	X	X	X	OFF			
Class/Inrush	> V_{UVLO}	0								
Power ON		1	> OUTP	< OUTN	X	X	**ON**	OFF	OFF	**ON**
			< OUTN	> OUTP			OFF	**ON**	**ON**	OFF
|IN12 – IN36| < OUTP – OUTN			> OUTN				OFF			
			< OUTP							

Table 2. Conditions for Ideal Bridge Mode on IN45/IN78

PoE MODE	OUTP	EN | $\overline{EN}$	IN12	IN36	IN45	IN78	TG45	TG78	BG45	BG78
Detect/Class	< V_{UVLO}	X	X	X	X	X	OFF			
Class/Inrush	> V_{UVLO}	0								
Power ON		1	X	X	> OUTP	< OUTN	**ON**	OFF	OFF	**ON**
					< OUTN	> OUTP	OFF	**ON**	**ON**	OFF
|IN45 – IN78| < OUTP – OUTN					> OUTN		OFF			
					< OUTP					

IN45/IN78. Within each pair, one input voltage must be greater than OUTP and one must be less than OUTN before the external MOSFETs related to that pair are enabled. For example, if IN36 is greater than OUTP and IN12 is less than OUTN, TG36 and BG12 will turn on. Table 1 and Table 2 outline the conditions that activate the ideal diode bridge.

Shutdown Mode

Shutdown mode is intended to keep the LT4321 quiescent current from interfering with detection and classification in a PoE system (Figure 2). The LT4321 is always in shutdown mode when OUTP < V_{UVLO}. It can be held in shutdown mode over the full operating voltage range by deasserting both the EN and $\overline{EN}$ pins.

Shutting down the LT4321 does not disconnect the load. The external MOSFETs are shorted gate to source and bridge current is carried by the MOSFETs' body diodes. The eight body diodes will act like two traditional diode bridges. At light load, the power dissipated in the forward drop of the body diodes will be less than the power dissipated by the LT4321 quiescent current. In applications with a low power sleep mode, the LT4321 can optionally be shut down to save power if the load current is less than 20mA.

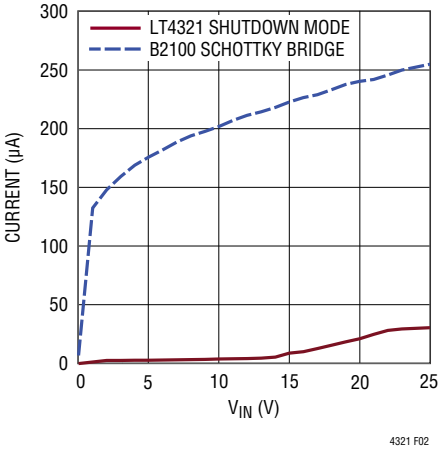


Figure 2. Leakage Current at 125°C

APPLICATIONS INFORMATION

EXTERNAL INTERFACE AND COMPONENT SELECTION

Bypass Capacitance

A 0.1µF ceramic capacitor must be placed across the OUTP and OUTN pins.

In PD applications, the IEEE 802.3 standard limits the port capacitance at the PD interface (C_{PD}) to 0.12µF. The LT4321 and the PD interface controller both need local bypass capacitance, but they can share the same 0.1µF capacitor. If the LT4321 and the PD interface controller cannot both be positioned next to a shared bypass capacitor, split the C_{PD} capacitance between the two chips by placing a 0.047µF ceramic close to the LT4321 and another 0.047µF ceramic close to the PD interface controller.

A 10µF or greater capacitance must be connected across OUTP and OUTN pins when the LT4321 is enabled. In PoE applications it is sufficient for the C_{PORT} capacitor to be connected by the PD interface controller's hot swap FET. In non-PoE applications the C_{PORT} capacitor may be permanently connected between OUTP and OUTN.

Transient Voltage Suppressor

The LT4321 specifies an absolute maximum voltage of 100V and is designed to tolerate brief overvoltage events. However, pins that interface to Ethernet cables or remote telecom supplies can routinely see excessive peak voltages. To protect the LT4321, install a unidirectional transient voltage suppressor (TVS) such as an SMAJ60A between OUTP and OUTN. This TVS must be mounted as close as possible to the LT4321.

For extremely high cable discharge and surge protection contact Analog Devices Applications.

MOSFET Selection

Select external MOSFETs that have a drain-source breakdown voltage higher than the maximum input voltage. For PoE systems the drain-source breakdown should be at least 100V. For all applications the gate threshold must be a minimum of 2V.

The amount of power saved by the LT4321 depends on the channel resistance, $R_{DS(ON)}$, of the external MOSFETs. To maximize performance and power savings select $R_{DS(ON)}$ such that the forward voltage drop, V_F, is between 20mV and 70mV. Given the average output load current, I_{AVG}:

$$R_{DS(ON)} = V_F/I_{AVG}$$

For example, a PoE+ class 4 PD's maximum average current, I_{AVG}, is 600mA. Choosing a MOSFET forward voltage drop of 40mV reduces power consumption to $1/15^{th}$ that of a B2100 Schottky diode bridge.

$$R_{DS(ON)} = 40mV/600mA = 66m\Omega$$

Enable Pins

When OUTP is greater than V_{UVLO}, the enable pins EN and $\overline{EN}$ will control whether the LT4321 is in shutdown mode or ideal bridge mode (Table 1 and Table 2). EN and $\overline{EN}$ may be driven by a 3.3V or 5V logic signal, or with an open drain or collector.

The $\overline{EN}$ pin is pulled up to the internally generated voltage $V_{\overline{ENOC}}$ by an internal 250kΩ resistor. The EN pin is pulled down to OUTN by an internal 250kΩ resistor. When OUTP is less than 12V the enable pins are high impedance to prevent these resistors from corrupting PoE detection.

The enable pins tolerate 100V (absolute maximum) and may be tied directly to the OUTP or OUTN pins as needed.

Figure 3 and Figure 4 show how to interface the enable pins to a PD interface controller. In these configurations, the LT4321 PoE ideal bridge will be enabled after detection and classification are complete and before the PD is consuming a significant amount of current.

Figure 5 shows how to configure the enable pins if the LT4321 and PD ground planes are separated by a Common Mode Choke (CMC). Connecting a 24V Zener from VPORTP to EN pins enables the LT4321 at power on while drawing minimal current during detection and classification.

APPLICATIONS INFORMATION

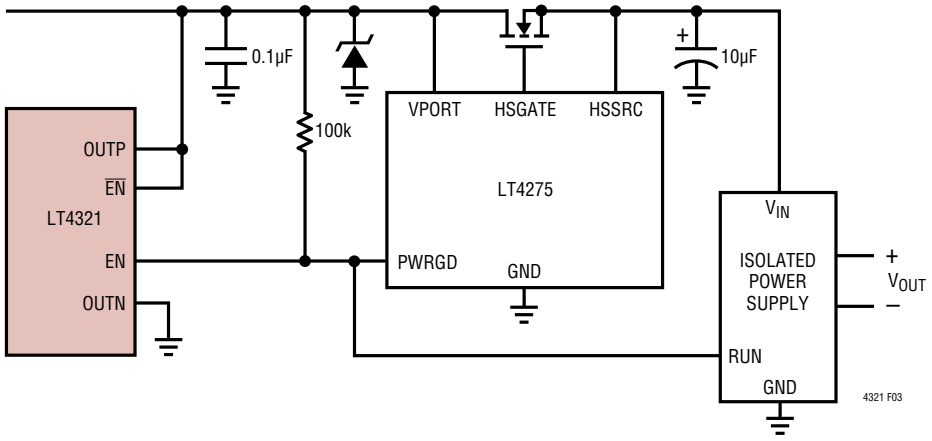


Figure 3. PD Interface Using the EN Pin

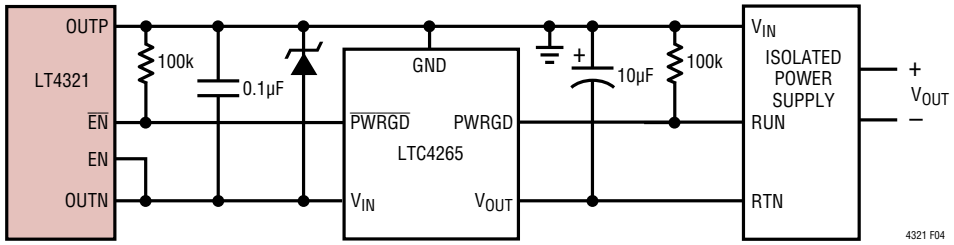


Figure 4. PD Interface Using the $\overline{EN}$ Pin

APPLICATIONS INFORMATION

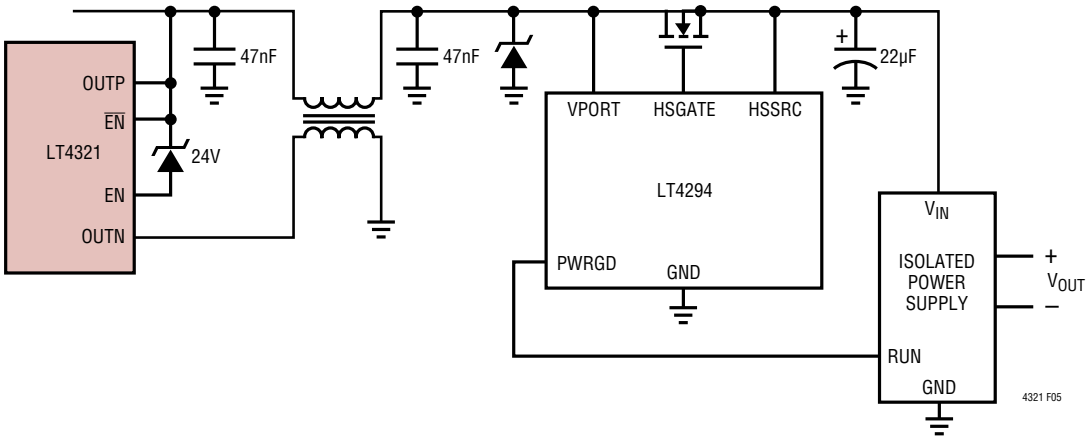
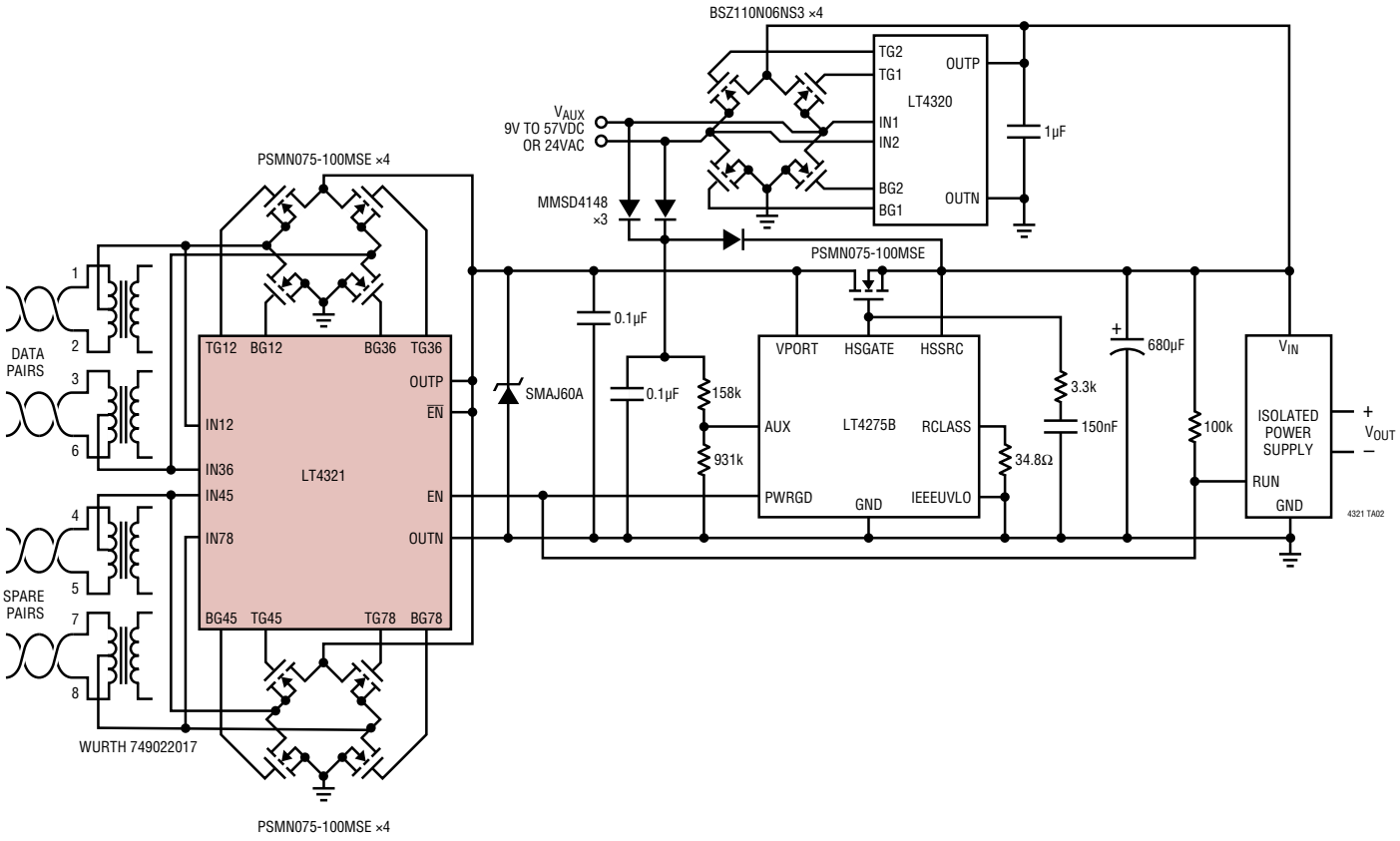


Figure 5. Using Zener Diode with EN Pin

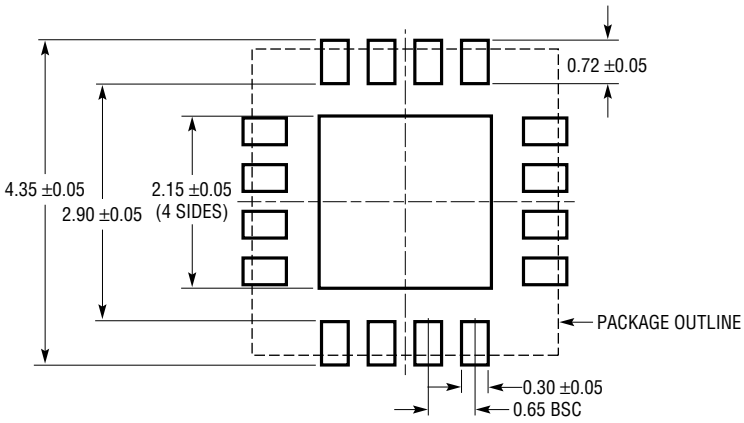
TYPICAL APPLICATIONS

High Efficiency 25W PD Solution with 12VDC and 24VAC Auxiliary Input

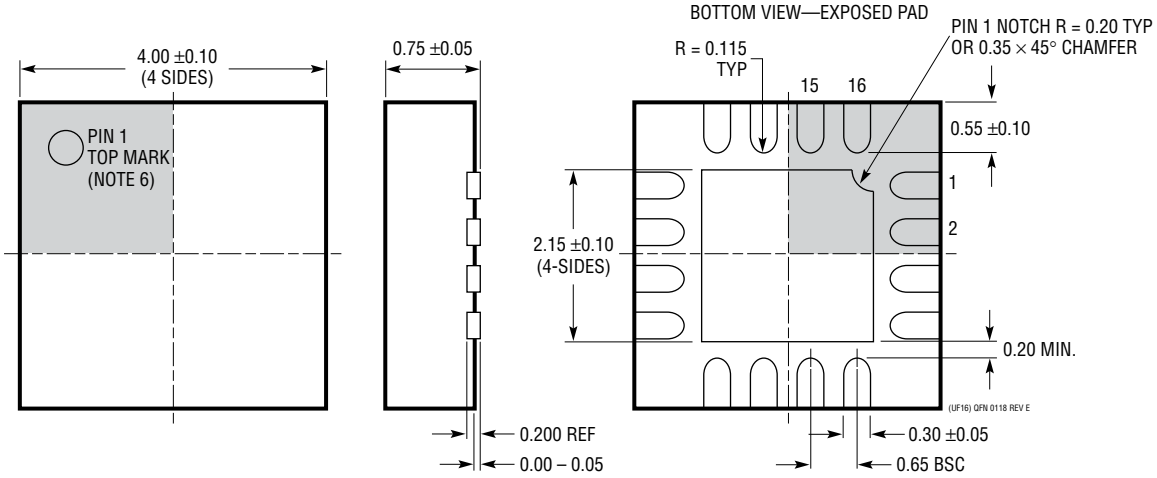


PACKAGE DESCRIPTION

UF Package
16-Lead Plastic QFN (4mm × 4mm)
(Reference LTC DWG # 05-08-1692 Rev E)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGGC)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	07/22	Typical Application Diagram revised. Correction to unit scale from mA to µA on BGn Pull-Up Strength. Updated Overview Section. Added Figure 5 and associated text. Minor update to Typical Applications Diagrams.	1 4 6 8, 10 11, 14