MOSFET Diode-OR Controller

FEATURES

- **Low Loss Replacement for ORing Diode in Multiple Sourced Power Supplies**
- **External N-Channel MOSFETs for High Current Capability**
- **Internal Boost Regulator Supply for MOSFET Gate Drive**
- **Wide Input Range: 1.2V to 18V**
- Fast Switching MOSFET Gate Control
- Input Under and Overvoltage Detection
- STATUS and $\overline{\text{FAULT}}$ Outputs for Monitoring
- Internal MOSFET Gate Clamp
- Available in a 10-pin MSOP Package

APPLICATIONS

- Paralleled Power Supplies
- Uninterrupted Supplies
- High Availability Systems
- N + 1 Redundant Power Supplies

DESCRIPTION

The LT®4351 creates a near ideal diode using external single or back-to-back N-channel MOSFETs. This ideal diode function permits low loss ORing of multiple power sources. Power sources can easily be ORed together to increase total system power and reliability with minimal effect on supply voltage or efficiency. Disparate power supplies can be efficiently ORed together.

The IC monitors the input supply with respect to the load and turns on the MOSFET(s) when the input supply is higher. If the MOSFET's $R_{DS(ON)}$ is sufficiently small, the LT4351 will regulate the voltage across the MOSFET(s) to 15mV. A STATUS pin indicates the MOSFET on-state.

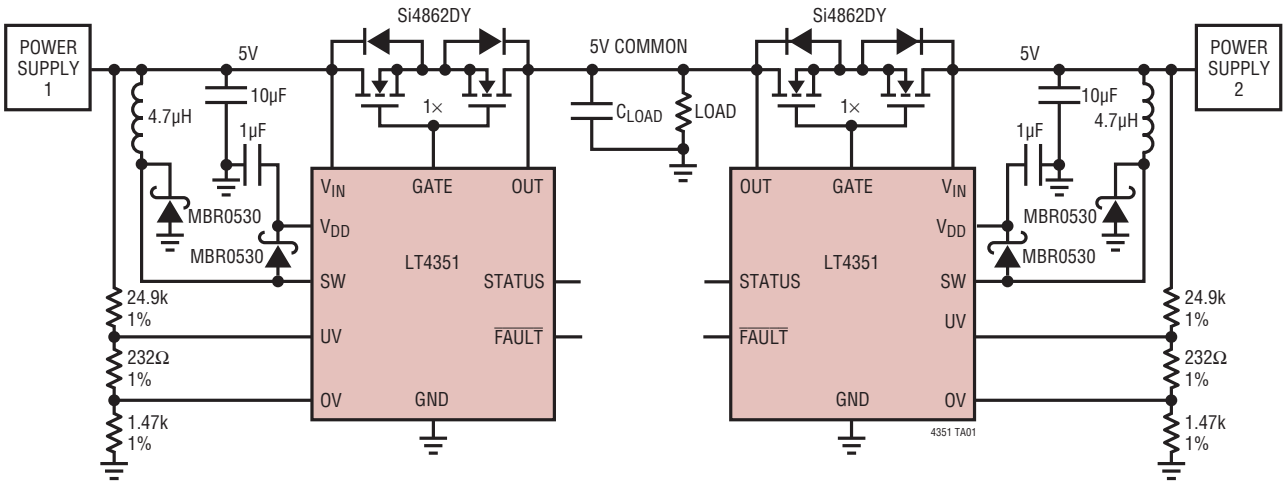
An internal boost regulator generates the MOSFET gate drive voltage. Low operating voltage allows for ORing of supplies as low as 1.2V.

The LT4351 will disable power passage during undervoltage or overvoltage conditions. These voltages are set by resistive dividers on the UV and OV pins. The undervoltage threshold has user programmable hysteresis. Overvoltage detection is filtered to reduce false triggering.

The LT4351 is available in a 10-pin MSOP package.

TYPICAL APPLICATION

Dual 5V Redundant Supply

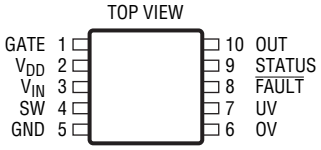


ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN} Voltage ..... –0.3V to 19V
OUT Voltage ..... –0.3V to 19V
V_{DD} Voltage ..... –0.3V to 30V
$\overline{FAULT}$, STATUS Voltages ..... –0.3V to 30V
$\overline{FAULT}$, STATUS Current 8mA
UV, OV Voltages ..... –0.3V to 9V
SW Voltage ..... –0.3V to 32V
Operating Temperature Range
LT4351C ..... 0°C to 70°C
LT4351I ..... –40°C to 85°C
Junction Temperature (Note 2) ..... 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PIN CONFIGURATION



MS PACKAGE
10-LEAD PLASTIC MSOP

T_{JMAX} = 125°C, θ_{JA} = 120°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT4351CMS#PBF	LT4351CMS#TRPBF	LTZZ	10-Lead Plastic MSOP	0°C to 70°C
LT4351IMS#PBF	LT4351IMS#TRPBF	LTA1	10-Lead Plastic MSOP	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = V_{OUT} = 5V, V_{DD} = 16.1V, V_{UV} = 0.4V, V_{OV} = 0.2V, GATE Open, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supply and Protection							
V_{IN}	Operating Range		●	1.2		18	V
I_{VIN}	V_{IN} Supply Current	V_{IN} = 1.2V, V_{OUT} = 1.1V, V_{DD} = 12.3V V_{IN} = 18V, V_{OUT} = 17.9V, V_{DD} = 29.1V	● ●		1.41 1.71	2 2.1	mA mA
$V_{UV(TH)}$	Undervoltage Turn-Off Voltage Threshold	UV Falling	●	290	300	310	mV
$I_{UV(HYST)}$	I_{UV} Hysteresis	Difference Between I_{UV} at $V_{UV(TH)}$ + 10mV and $V_{UV(TH)}$ – 10mV	●	7	10	13	µA
I_{UV}	UV Input Bias Current	V_{UV} = $V_{UV(TH)}$ + 10mV	●		–100	–400	nA
$V_{OV(TH)}$	Overvoltage Threshold	OV Rising	●	290	300	310	mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = V_{OUT} = 5V, V_{DD} = 16.1V, V_{UV} = 0.4V, V_{OV} = 0.2V, GATE Open, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{OV}	OV Input Bias Current	V_{OV} = $V_{OV(TH)}$ – 10mV	●		–100	–400	V
$V_{F(ON)}$	$\overline{FAULT}$ Pin On-Voltage	I_F = 5mA in Fault Condition	●		0.14	0.25	V
$I_{F(OFF)}$	$\overline{FAULT}$ Pin Leakage Current	V_F = 30V, V_{IN} = 4.9V	●		0.04	1	µA
Boost Supply							
V_{BR}	Boost Regulation Trip Voltage	Measured as V_{DD} to V_{IN}, Rising Edge	●	10.2	10.7	11.4	V
t_{OFF}	Boost Supply Off-Time				600		ns
I_{SWLIM}	Boost Supply Switch Current Limit		●	350	450	650	mA
Gate Drive							
V_{IOR}	Input-to-Output Regulated Voltage		●	4	15	25	mV
ΔV_{GL}	Gate Voltage Limit	V_{IN} = 5V, V_{OUT} = 4.9V, V_{DD} = 13V Measured with Respect to V_{DD}	●		–2.3	–3	V
$\Delta V_{G(MAX)}$	Maximum Gate Voltage	V_{IN} = 5V, V_{OUT} = 4.9V, V_{DD} = 16.1V Measured with Respect to V_{OUT}	●	7	7.4	7.8	V
$V_{G(OFF)}$	Gate Off-Voltage	V_{OUT} = 5.1V	●		0.16	0.30	V
I_{GSO}	Gate Source Current	V_{OUT} = 4.9V, V_{GATE} = 9V			0.670		A
I_{GSK}	Gate Sink Current	V_{OUT} = 5.1V, V_{GATE} = 9V			0.670		A
V_{DD}	Operating Range		●			30	V
I_{VDD}	V_{DD} Supply Current	V_{IN} = 1.2V, V_{OUT} = 1.1V, V_{DD} = 12.3V, GATE Open V_{IN} = 18V, V_{OUT} = 17.9V, V_{DD} = 29.1V, GATE Open	● ●		3 3.6	4 5.6	mA mA
Status Functions							
ΔV_{GIS}	Minimum Gate Voltage for Turning On Status	V_{OUT} = 4.9V, I_{STATUS} = 1mA	●		0.75	1	V
V_{IOGF}	V_{IN} to V_{OUT} Fault Voltage with Open Gate	V_{OUT} Falling, Measured with Respect to V_{IN}		185	210	230	mV
$V_{ST(ON)}$	Status Pin On-Voltage	I_{ST} = 5mA, V_{OUT} = 4.9V, Status On	●		0.13	0.25	V
$I_{ST(OFF)}$	Status Pin Leakage Current	V_{ST} = 30V, Status Off, V_{IN} = 4.9V	●		0.04	1	µA

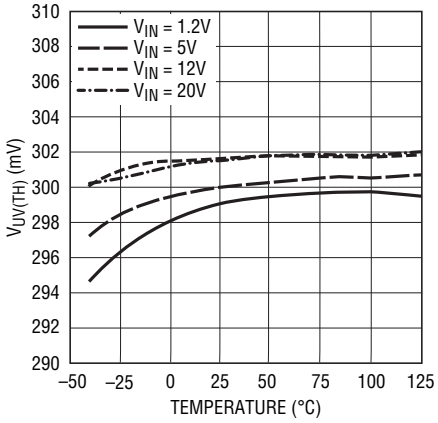
Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula:

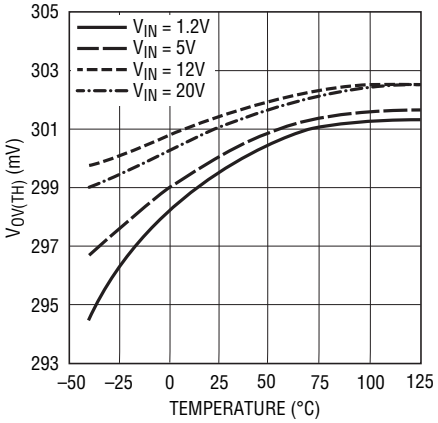
$T_J = T_A + (P_D \bullet 120°C/W)$

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

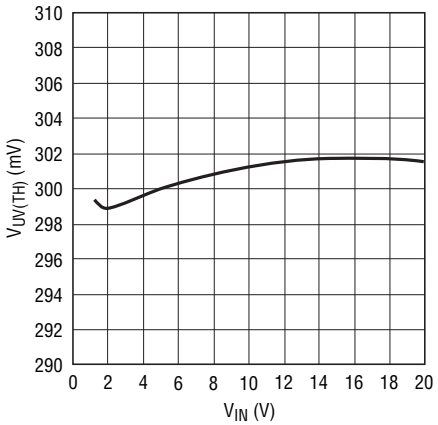
Undervoltage Threshold vs Temperature



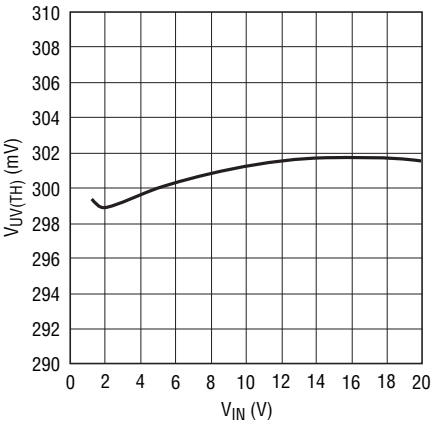
Overvoltage Threshold vs Temperature



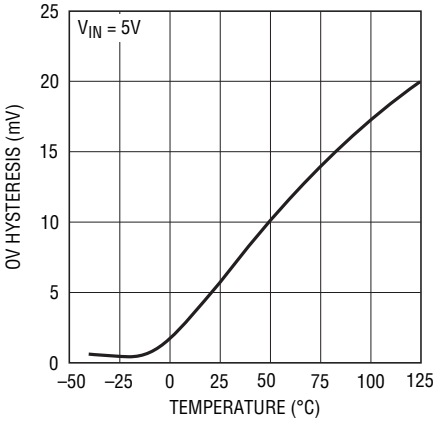
Undervoltage Threshold vs V_{IN}



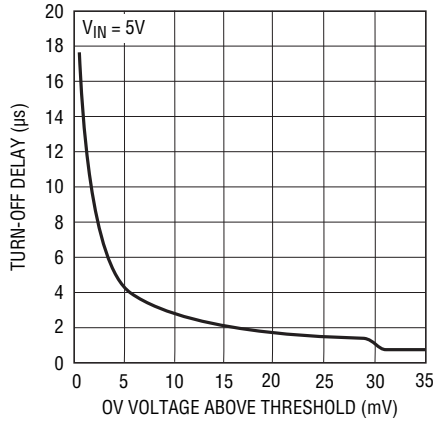
Overvoltage Threshold vs V_{IN}



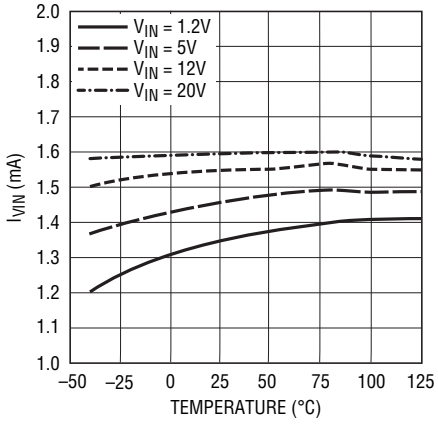
Overvoltage Hysteresis vs Temperature



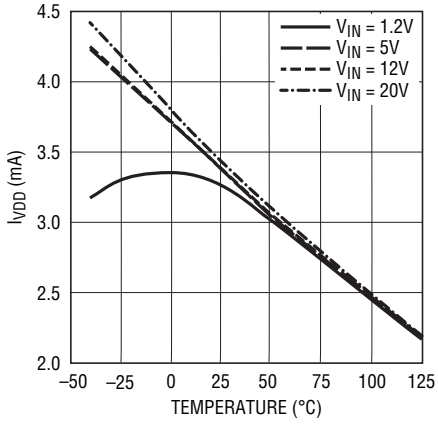
Overvoltage Turn-Off Delay vs Overvoltage Overdrive



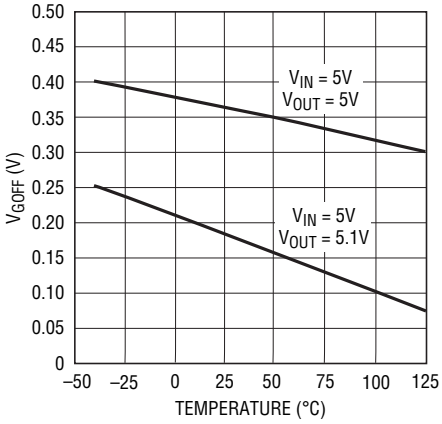
I_{VIN} vs Temperature



I_{VDD} vs Temperature

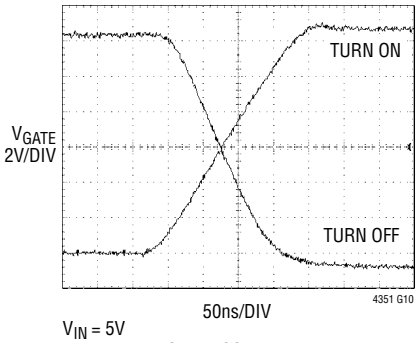


Gate Off-Voltage vs Temperature



TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

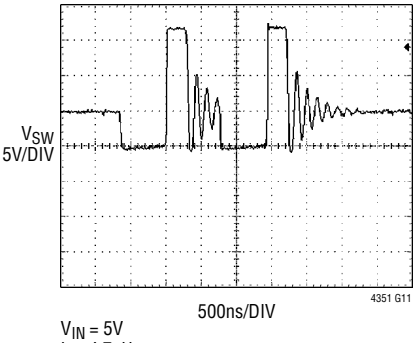
GATE Pin Turn On and Off Waveform with 10nF Capacitor Load



50ns/DIV

V_{IN} = 5V
V_{OUT} = 4.9V TO 5.1V SQUARE WAVE

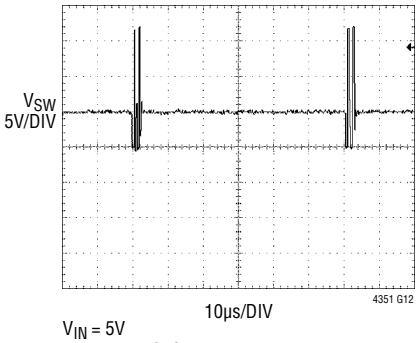
Typical SW Pin Waveform



500ns/DIV

V_{IN} = 5V
L = 4.7µH

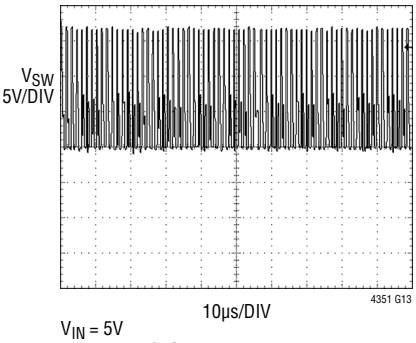
Typical SW Pin Waveform



10µs/DIV

V_{IN} = 5V
4.7µH INDUCTOR

SW Pin Waveform at Maximum Boost Regulator Output



10µs/DIV

V_{IN} = 5V
4.7µH INDUCTOR

PIN FUNCTIONS

GATE (Pin 1): MOSFET Gate Drive Pin. This pin is tied to the gate(s) of the external N-channel MOSFET(s). The GATE pin drives high when UV is above the $V_{UV(TH)}$ threshold, OV is below the $V_{OV(TH)}$ threshold and V_{IN} is greater than OUT by 15mV. When not driven high, GATE actively pulls to GND. GATE can sink or source up to 600mA.

V_{DD} (Pin 2): Gate Drive Supply Pin. This is the supply pin for the gate drive amplifier. It is either generated by the onboard boost regulator or supplied externally. When turning on the MOSFET(s), a large high current pulse flows through this pin. Bypass the pin with a 1µF capacitor placed in close proximity to the part. The voltage on this pin is also the feedback for the boost regulator. If the V_{DD} voltage exceeds the V_{IN} voltage by 10.7V, the boost switch is held off.

V_{IN} (Pin 3): Input Supply Pin. This pin is the supply pin for the control circuitry and the boost regulator. It is also one input in conjunction with OUT for controlling the MOSFET(s). Bypassing should include a low ESR/ESL capacitor placed in close proximity to the part.

SW (Pin 4): Boost Regulator Switch Pin. This pin is the boost regulator switch output. It is connected to the boost inductor and the boost diode. Peak switch current is limited internally to 450mA. A Schottky diode between GND and SW is required. If an external V_{DD} supply is used, leave this pin open.

GND (Pin 5): Device Ground Pin. This pin is ground for the boost switch, gate driver as well as the control circuitry. Tie the V_{IN} and V_{DD} bypass capacitors and ground plane close to this pin to minimize the effects of switching currents on part performance.

OV (Pin 6): Overvoltage Shutdown Pin. This pin is used for input overvoltage detection. It is connected to a resistive divider from V_{IN}. When the voltage exceeds the OV threshold (0.3V), GATE is pulled to GND disabling power transfer. In addition, the $\overline{FAULT}$ pin pulls low indicating a fault. Overvoltage detection has filtering on it to prevent false triggering. The filtering depends on the level of overdrive. Filtered tripping will occur when OV exceeds 0.3V. If OV exceeds 0.33V, the gate immediately turns off (no filtering). If overvoltage detection is not required, ground the OV pin. See the Applications Information section for further information.

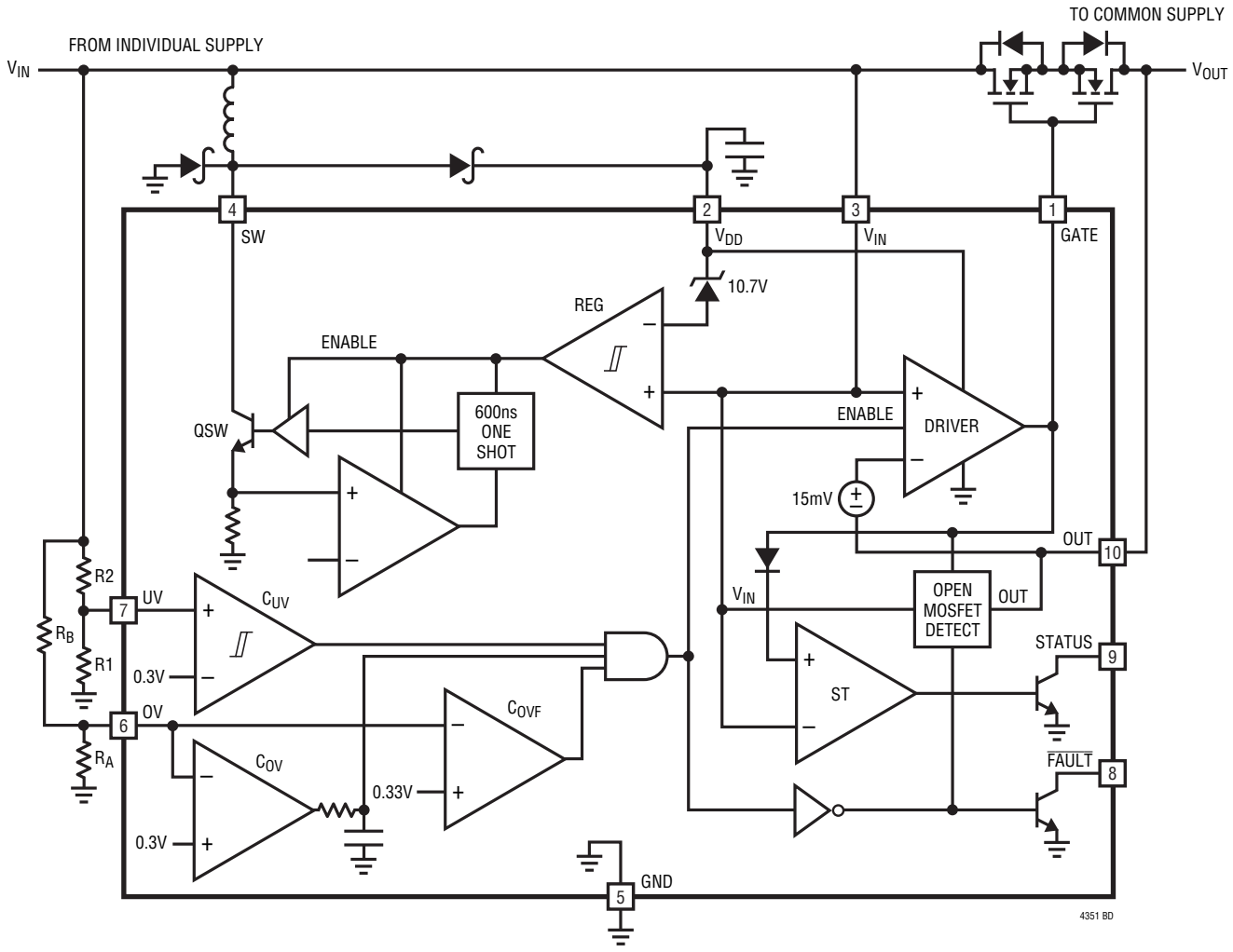
UV (Pin 7): Undervoltage Shutdown Pin. This pin is used for the undervoltage detect function. It is connected to a resistive divider from V_{IN}. When the voltage is below the UV threshold, GATE pulls to GND disabling power transfer. In addition, the $\overline{FAULT}$ pin pulls low indicating a fault. When the UV pin voltage drops below the threshold, a 10µA current is pulled from the divider to provide hysteresis. If undervoltage detection is not required, tie the UV pin to a voltage greater than 320mV and not greater than V_{IN}. Do not force more than 9V on UV due to an internal clamp. See the Applications Information section for further information.

$\overline{FAULT}$ (Pin 8): Fault Comparator Status Pin. This pin pulls low when a fault occurs. A fault has occurred if the UV pin is below threshold or the OV pin is above threshold. The $\overline{FAULT}$ pin low indicates that there is a problem with the V_{IN} (source) supply. GATE is pulled to GND during a fault, disabling the MOSFET(s) and prohibits common supply contamination. If the GATE pin goes to compliance (GATE equals the lesser of V_{DD} – 2.3V or OUT + 7.4V) and V_{IN} is greater than OUT by more than 0.21V, $\overline{FAULT}$ turns on as an indicator that the MOSFETs are probably not functioning. Leave this pin open if not used.

STATUS (Pin 9): MOSFET Status Pin. This pin pulls low when GATE is above V_{IN} by more than 0.7V and V_{IN} is greater than OUT by 15mV. This indicates the MOSFET is on. Leave this pin open if not used.

OUT (Pin 10): Common Supply Pin. This pin is connected to the supply common and is used in conjunction with V_{IN} as one input controlling the MOSFET(s).

BLOCK DIAGRAM



OPERATION

Increasingly, system designers have to deal with multiple supply sources. The multiplicity may provide parallel, redundant supplies for increased reliability or provide a means of connecting disparate supplies. In all cases the desire is for behavior like a diode but with no loss or voltage drop.

ORing diodes have been the conventional means of connecting these supplies. The disadvantage of this approach is that diodes introduce efficiency loss because of their forward voltage drop. This variable voltage drop also degenerates supply tolerance. Additionally, diodes provide no information concerning the status of the sourcing supply. Separate control must also be added to ensure that a supply that is out of range is not allowed to affect the common supply.

The LT4351 eliminates these problems by using N-channel MOSFETs as the pass elements. The MOSFET is turned on when power is being passed, allowing for a low voltage drop from the supply to the load. When the input source voltage drops below the output common supply voltage it turns off the MOSFET, thereby matching the function and performance of an ideal diode.

The LT4351 drives either a single MOSFET or dual back-to-back MOSFETs. Dual MOSFETs are chosen to eliminate current flow from the input supply to the output supply when the V_{IN} voltage is greater than OUT.

A driver amplifier monitors the input (V_{IN}) and output (OUT) and controls the MOSFETs. If V_{IN} exceeds OUT by 15mV, GATE goes high and turns on the MOSFET(s) allowing for power passage.

Undervoltage and overvoltage comparators C_{UV}, C_{OV} and C_{OVF} also control power passage. A resistive divider in conjunction with the UV and OV pins sets appropriate thresholds such that the MOSFET(s) is off when the UV pin is below 300mV or OV pin is above 300mV.

To help deal with the transients on the supply lines, the UV input has current hysteresis. When the UV voltage drops below the 300mV threshold, a 10µA current is pulled from the pin. Thus the user can set the hysteresis level through appropriate values in the divider.

Overvoltage shutdown occurs in two stages. The first occurs when the OV pin exceeds the 300mV reference. When OV just exceeds the reference, an internal capacitor starts charging, delaying the signal to turn off the MOSFET(s).

The second occurs when the OV pin exceeds 330mV. The OVF comparator will immediately trip pulling GATE to GND. This affords a delay inversely proportional to the amount of overdrive. This also provides for glitch immunity without compromising response time in the event of a serious overvoltage condition.

The $\overline{FAULT}$ output indicates the status of the C_{OV}, C_{OVF} and C_{UV} comparators. It pulls low during a fault condition. It also pulls low when GATE is at compliance and V_{IN} > OUT by more than 0.21V indicating a probable nonfunctioning MOSFET. Compliance occurs when GATE is at the lesser of OUT + 7.4V or V_{DD} – 2.3V. $\overline{FAULT}$ derives its drive from the greater of V_{IN} or OUT. It is active if V_{IN} or OUT is greater than 0.9V. If V_{IN} or OUT is below this level, the output state is not guaranteed.

The gate drive consists of a high current, wide bandwidth amplifier (driver). When the amplifier is enabled, it attempts to regulate the GATE voltage such that the voltage across the MOSFET(s) is approximately 15mV. If the MOSFET(s) on resistance is so high as to prevent regulation, then GATE goes to compliance and the MOSFET(s) fully turns on. The inputs to the amplifier are V_{IN} and OUT. The GATE pin sources current from V_{DD} and sinks current to GND. The maximum GATE to V_{IN} voltage is the lesser of V_{DD} – 2.3V or 7.4V above V_{OUT} or V_{IN} (internal clamp voltage).

The STATUS comparator, ST, pulls low when GATE exceeds V_{IN} by 0.7V. This occurs when V_{IN} > OUT + 15mV. The STATUS pin pulls low as an indication that power is passing through the MOSFET(s).

If V_{IN} is greater than OUT by 0.21V and GATE > V_{IN} + 7.4V or at compliance (GATE = V_{DD} – 2.3V), STATUS will go high as an indication of a likely open MOSFET. $\overline{FAULT}$ will pull low in this state indicating the probable fault.

The gate drive amplifier and STATUS function derive power from V_{DD}. The circuit requires V_{DD} > 2.5V. If V_{DD} is present, the gate drive amplifier and STATUS are active independent of the state of V_{IN}. If in a fault, GATE pulls actively low. In the event of V_{DD} collapse there still is an active pull-down (though of lesser strength) of GATE powered from OUT, guaranteeing turn off.

OPERATION

The on-chip boost regulator uses a constant off-time control scheme. When V_{DD} is below the regulation trip voltage, the switch turns on after a 600ns off-time. When the switch turns on current ramps up in the inductor until the current limit is reached (450mA). The switch turns off and the inductor's current flows through the external diode to charge up the V_{DD} capacitor. If V_{DD} is still too low, the switch turns on again after a fixed off-time of 600ns.

The boost regulator regulates V_{DD} to approximately 10.7V above V_{IN} When V_{DD} is above this level, the SW transistor turn-on is disabled. When V_{DD} falls below this level by the hysteresis level, the SW transistor is allowed to turn on. There is approximately 0.15V of hysteresis.

APPLICATIONS INFORMATION

Setting Fault Thresholds

The gate drive amplifier implements the ideal diode function. The fault comparators (UV and OV) prevent out of range input voltages from affecting the output by disabling the amplifier during these conditions. Think of the UV and OV as gating the ideal diode function, something a regular diode cannot do.

A resistive divider from V_{IN} to UV and one from V_{IN} to OV are the usual way of setting the $\overline{FAULT}$ thresholds. For UV the resistor values are set by:

$$R2 = \frac{UV_{HYST}}{I_{UVHYST}}$$

$$R1 = \frac{V_{UV}}{UV_{FAULT} - V_{UV}} \bullet R2$$

where UV_{HYST} is the desired undervoltage hysteresis at the input. UV_{FAULT} is the desired undervoltage trip voltage at the input. V_{UV} is the part undervoltage trip point (0.3V) and I_{HYSTUV} is the undervoltage hysteresis current (10µA). See Figure 1.

The divider on the OV pin is a straightforward resistive divider (Figure 2):

$$R_B = \left(\frac{OV_{FAULT}}{V_{OV}} - 1\right) R_A$$

$$R_A = \frac{0.3V}{R_A, R_B \text{ Divider Current}}$$

where OV_{FAULT} is the desired overvoltage trip point at the input and V_{OV} is the OV pin threshold (0.3V). The OV pin has 7mV of voltage hysteresis at room.

It is possible to do both dividers together using only three resistors though with more interdependence in components (Figure 3). The input bias current for UV and OV is less than 200nA, so keep resistor values less than 10k.

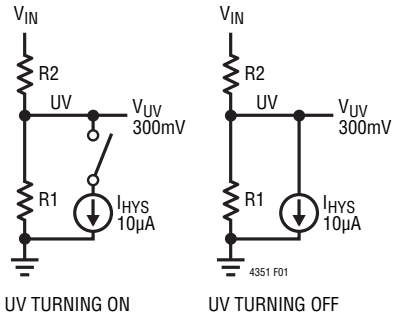


Figure 1

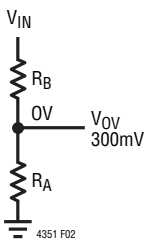


Figure 2

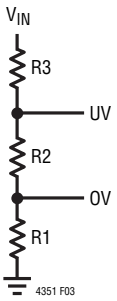


Figure 3

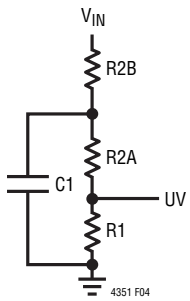


Figure 4

APPLICATIONS INFORMATION

In that case, the resistor values are set by:

$$R3 = \frac{UV_{HYST}}{I_{UVHYST}}$$

$$R2 = \frac{V_{UV} - \frac{UV_{FAULT}}{OV_{FAULT}} \bullet V_{OV}}{UV_{FAULT} - V_{UV}} \bullet R3$$

$$R1 = \frac{V_{OV} \bullet UV_{FAULT}}{OV_{FAULT} \bullet \left(UV_{FAULT} - V_{UV}\right)} \bullet R3$$

Hysteresis helps prevent erratic behavior due to the noise on V_{IN}. Two of the most common noise sources are: V_{IN} dipping when the MOSFETs first turn on and draw down the voltage on the V_{IN} capacitors, and the boost regulator switch turning on and drawing current from the V_{IN} capacitors. Use low ESR capacitors for V_{IN} and OUT filtering.

Note that because the UV pin uses current hysteresis, placing a capacitor on UV to ground to filter noise will reduce the effective hysteresis. Filtering can be achieved by splitting the R2 resistor, as shown in Figure 4.

To defeat undervoltage fault detection, the UV pin should be tied higher than 0.33V. UV can be tied to V_{IN} provided V_{IN} < 9V. Overvoltage fault detection can be defeated by grounding the OV pin. Do not exceed V_{IN}.

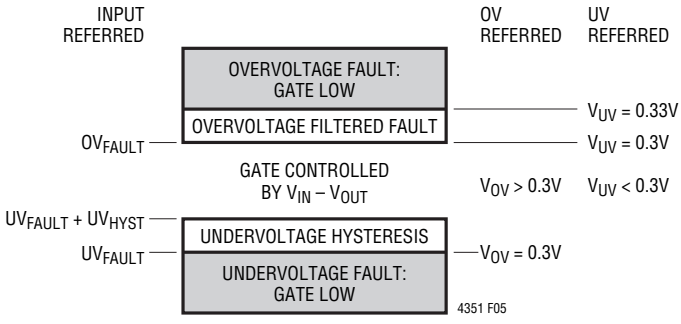


Figure 5. Graphical Representation of the UV and OV Functions

External Shutdown

To externally turn off the MOSFETs, such as to disable the supply, use an open-collector transistor pulling down on the UV pin. Note this will not turn off the boost regulator which will continue to operate.

Boost Regulator

The boost regulator will start working as soon as V_{IN} is greater than 0.85V. The regulator will supply all the current for the gate drive amplifier. While the amplifier itself requires only about 3mA, larger current pulses are required when charging the MOSFET gate. The reservoir capacitor on V_{DD} will provide this current (Figure 6).

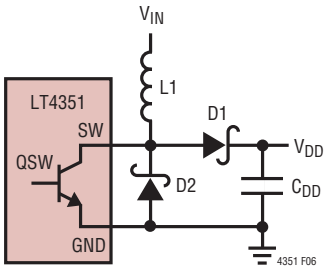


Figure 6

The regulator performance is relatively insensitive to the inductor value. The inductor value does control the frequency of operation. A 4.7µH inductor is recommended for V_{IN} voltages less than 10V and 10µH for V_{IN} voltages greater than 10V. Several inductors that work well with the LT4351 are listed in Table 1. Many different sizes and shapes are available. Consult each manufacturer for more detailed information and for their entire selection of related parts. The switching frequency for the boost regulator is around 1MHz so ferrite core inductors should be used to obtain the best efficiency. The inductor must handle a peak current of 0.7A minimum and have a DC resistance of 0.5Ω or less. Shielded inductors are recommended to reduce the noise due to inductive switching.

Table 1. Recommended Inductors

PART NUMBER	IND (µH)	DCR (mΩ)	VENDOR
LPS3314-472ML LPS4012-103ML	4.7 10	175 350	Coilcraft 847-639-6400 www.coilcraft.com
744029004 744042100	4.7 10	200 150	Würth Elektronik www.we-online.com
SD3112-4R7-R SD3118-100-R	4.7 10	246 295	Coiltronics www.coiltronics.com

APPLICATIONS INFORMATION

For V_{IN} less than 2V, choose a DC resistance less than 0.2Ω.

Note that V_{DD} current referred to the input supply is higher. A first order approximation of the input current is:

$$I_{VINVDD} = \left(1 + \frac{10.6}{V_{IN}}\right) \bullet \frac{I_{VDD}}{80\%}$$

Under normal operation, the V_{DD} current is under 10mA and the boost regulator operates in Burst Mode® operation. If any additional load is added, ensure that the regulator is capable of supplying that load. As the load is increased, the boost regulator will switch into continuous mode operation. Further increases in load will collapse the boost regulator voltage.

Operating the regulator with increased load will cause increased IC power dissipation and temperature, which must be taken into consideration.

A 100ns delay from detecting the switch current limit to turning off the power switch produces an overshoot of the inductor current from the 0.45A switch limit. The amount of overshoot depends on the boost regulator inductance. Choosing an inductor that can handle 0.75A peak current will be sufficient for the recommended inductors.

Diode Selection

Schottky diodes, with their low forward voltage drop and fast switching speed, are the best match for the LT4351 boost regulator. Select a diode that can handle 0.75A peak current and a reverse breakdown of 15V greater than the maximum V_{IN}.

V_{DD} Capacitor Selection

Low ESR (Equivalent Series Resistance) capacitors should be used on V_{DD} to minimize the output ripple voltage. Multilayer ceramic capacitors are the best choice, as they have a very low ESR and are available in very small packages. Always use a capacitor with a voltage rating at least 12V greater than V_{IN}.

Capacitors

Two types of input capacitors are generally needed for the LT4351. The first is a large bulk capacitor that takes care of ringing associated with inductance of the input supply lines and provides charge for the load when switching the MOSFET. The input parasitic inductance in conjunction with C_B and its ESR create an LCR network. The input LCR can be stimulated by the boost regulator switch current or load current transients when the MOSFETs are on. To reduce ringing associated with input inductance, C_B should be:

$$C_B \geq \frac{4 \bullet L_{IN}}{R_{ESR}^2}$$

where C_B is the capacitor value, R_{ESR} is the capacitor's ESR and L_{IN} is the inductance of the input lines.

While damped ringing is not necessarily bad, it may produce unexpected results as the LT4351 ideal diode reacts to the varying V_{IN} to OUT voltage. Typically an electrolytic or tantalum low ESR capacitor would be used. Figure 7a illustrates V_{IN} for a low value of C_B and Figure 7b shows it with a correctly sized value.

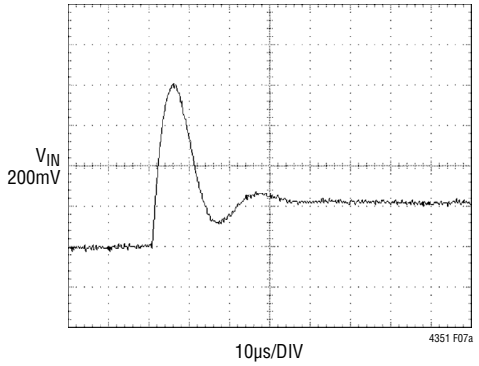


Figure 7a. Example of Input Voltage Ringing with Low C_{IN} Capacitor at MOSFET Turn Off

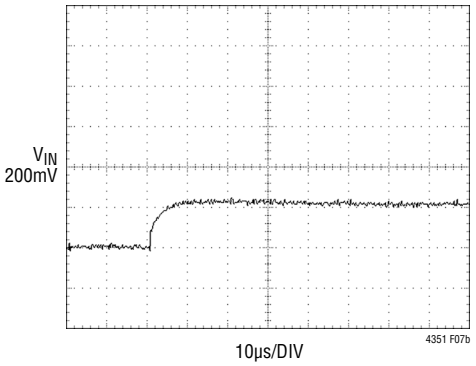


Figure 7b. Example of Input Voltage with Sufficient C_{IN} Capacitor at MOSFET Turn Off

APPLICATIONS INFORMATION

As an example, for 500nH of inductance and R_{ESR} of about 100mΩ, then:

$$C \geq \frac{4 \bullet 500nF}{0.1^2} = 200\mu F$$

Check vendor data for ESR and iterate to get the best value. Additional C_B capacitance may be required for load concerns.

If the boost regulator is being used, place a 10µF low ESR ceramic capacitor from V_{IN} to GND. Place a 10µF and a 0.1µF ceramic capacitor close to V_{IN} and GND. These capacitors should have low ESR (less than 10mΩ for the 10µF and 40mΩ for the 0.1µF). These capacitors help to eliminate problems associated with noise produced by the boost regulator. They are decoupled from the V_{IN} supply by a small 1Ω resistor, as shown in Figure 8. The LT4351 will perform better with a small ceramic capacitor (10µF) on OUT to GND.

External Boost Supply

The V_{DD} pin may be powered by an external supply. In this case, simply omit the boost regulator inductor and diode and leave the SW pin open. Suitable V_{DD} capacitance (minimum of a 1µF ceramic) should remain due to the current pulses required for the gate driver.

The V_{DD} current consists of 3.5mA of DC current with the current required to charge the MOSFET's gate which is dependent on the gate charge required and frequency of switching. Typically the average current will be under 10mA.

MOSFET Selection

The LT4351 uses either a single N-channel MOSFET or back-to-back N-channel MOSFETs as the pass element. Back-to-back MOSFETs prevent the MOSFET body diode from passing current.

Use a single MOSFET if current flow is allowable from input to output when the input supply is above the output (limited overvoltage protection). In this case the MOSFET should have a source on the input side so the body diode conducts current to the load. Back-to-back MOSFETs are normally connected with their sources tied together to provide added protection against exceeding maximum gate to source voltage.

Selection of MOSFETs should be based on $R_{DS(ON)}$, BV_{DSS} and BV_{GSS}. BV_{DSS} should be high enough to prevent breakdown when V_{IN} or OUT are at their maximum value. $R_{DS(ON)}$ should be selected to keep within the MOSFET power rating at the maximum load current ($I^2 \bullet R_{DS(ON)}$) BV_{GSS} should be at least 8V. The LT4351 will clamp the GATE to 7.5V above the lesser of V_{IN} or OUT. For back-to-back MOSFETs where sources are tied together, this allows the use of MOSFETs with a VGS max rating of 8V or more. If a single MOSFET is used, care must be taken to ensure the VGS max rating is not exceeded. When the MOSFET is turned off, the GATE voltage is near ground, the source at V_{IN}. Thus, MOSFET VGS max must be greater than $V_{IN(MAX)}$.

If a single MOSFET is used with source to V_{IN}, then BV_{GSS} should be greater than the maximum V_{IN} since the MOSFET gate is at 0.2V when off.

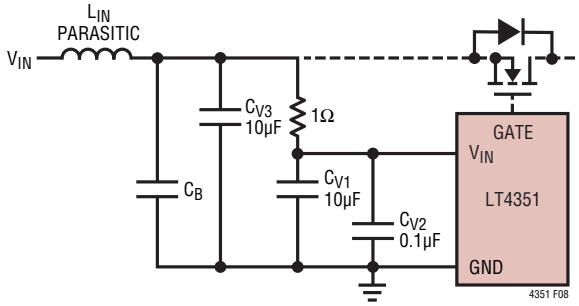


Figure 8. V_{IN} Capacitors

APPLICATIONS INFORMATION

The gate drive amplifier will attempt to regulate the voltage across the MOSFETs to 15mV. Regulation will be achieved if:

$$R_{DS} < \frac{15mV}{2 \bullet I_{LOAD}} \text{ for two MOSFETs and}$$

$$R_{DS} < \frac{15mV}{I_{LOAD}} \text{ for a single MOSFET}$$

This requires very low R_{DS} values. This may be achieved by paralleling MOSFETs, but be careful to keep interconnection trace resistance low. In the event that regulation cannot be achieved, the gate drive amplifier will drive GATE to its clamp and achieve the best R_{DS} possible at that level.

STATUS

The STATUS pin sinks current when the input (V_{IN}) is above output (OUT) by 15mV and GATE is above V_{IN} by 0.7V. This will normally indicate that power is being passed though the MOSFETs.

In the event of a nonfunctional MOSFET, the GATE voltage will be driven high (to the GATE clamp voltage). If V_{IN} is greater than OUT by more than 0.21V, the $\overline{FAULT}$ pin will sink current to signal the potential problem.

There is no direct measurement or confirmation of current flowing in the MOSFETs. Current is shared between sources based on their voltage and series resistance. If precision load sharing is desired, the LTC4350 may be a more suitable part.

Redundant Supplies

The LT4351 is an improved solution for ORing redundant supplies because of its lower forward drop versus conventional diodes. The lower forward drop significantly improves overall efficiency, improves the voltage tolerance at the load and provides for a more accurate transition from supply to supply and more accurate load sharing between supplies.

ORing can be done either at the load or at the source. Figure 9 shows some examples. ORing at the load is usually the safest method since it protects against shorts in interconnects.

The LT4351 tighter forward-voltage tolerance makes it easier to balance current between similar supplies using the droop method. The droop method uses the supply voltage and series resistance in the power path to provide load sharing. In this case, size the MOSFET's $R_{DS(ON)}$ low to allow for regulation.

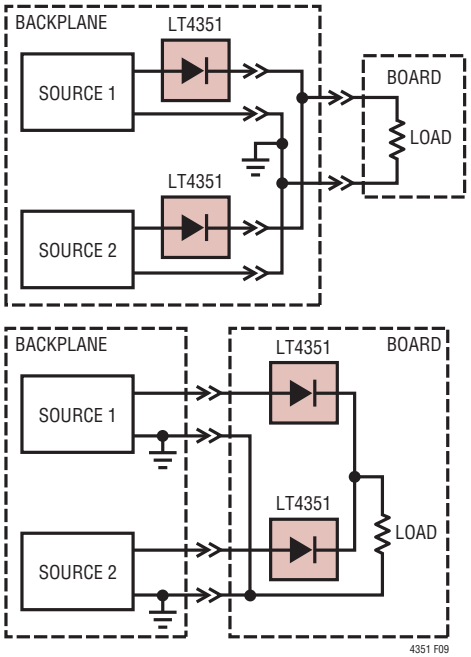


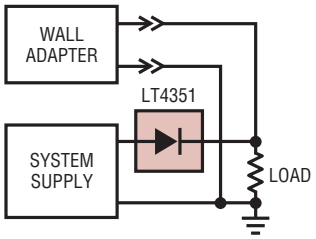
Figure 9. Redundant Backplane Supplies

APPLICATIONS INFORMATION

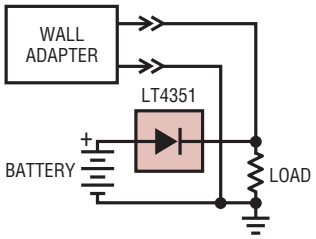
ORing Disparate Supplies

The LT4351 provides an easy solution for connecting together different types of power sources. Again, because of the low forward drop, the efficiency of the system is improved and the voltage transition between supplies is more accurate. In addition, the undervoltage and overvoltage features of the LT4351 provide options for enabling and disabling the supplies that are not available from a common diode. Figure 10 shows some examples of connecting disparate supplies.

Isolated System Supply from Wall Adapter



Isolated Battery Backup



Three Source ORing Provides Protection Against Out of Range Supplies

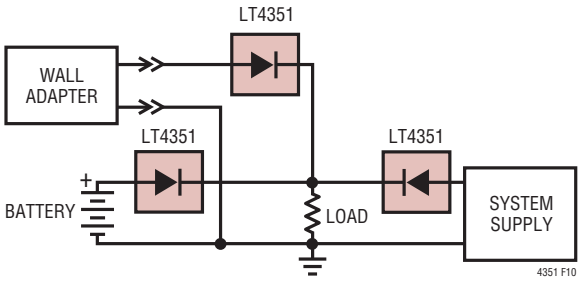


Figure 10

Start-Up Considerations

There is no inherent shutdown in the part. As V_{IN} ramps up, the boost regulator starts at about 0.85V and becomes fully operational by 1.1V. The undervoltage and overvoltage comparators become accurate by 1.2V. The gate drive amplifier keeps GATE low during this period with either a passive pull-down, a weak active pull-down if OUT is greater than 0.8V or with the full gate drive sink if V_{DD} is above 2.2V.

Once V_{IN} is greater than 1.2V and V_{DD} is up, the part then operates normally. The UV and OV pins will control the enabling of the gate driver and once enabled, the V_{IN} to OUT voltage controls MOSFET turn on.

If V_{DD} is still being charged when the gate driver turns on the MOSFET, the GATE pin tracks with the V_{DD} increase until it reaches either the gate clamp voltage or the compliance of the gate driver. If V_{DD} is present without V_{IN} or OUT, the GATE pin actively sinks low.

Power Dissipation

The internal power dissipation of the LT4351 is comprised of the following four major components: DC power dissipation from V_{IN}, DC power dissipation from V_{DD}, the dissipation in the boost switch including the base drive, and dynamic power dissipation due to current used to charge and discharge the MOSFETs. The DC components are:

$$P_{DCVIN} = I_{VIN} \bullet V_{IN}$$

$$P_{DCVDD} = I_{VDD} \bullet V_{DD}$$

Figure 11 shows the internal dissipation of the boost regulator as a function of V_{IN} and inductor value. Figure 11 represents the worst-case condition with the regulator on all the time, which does not occur in normal practice.

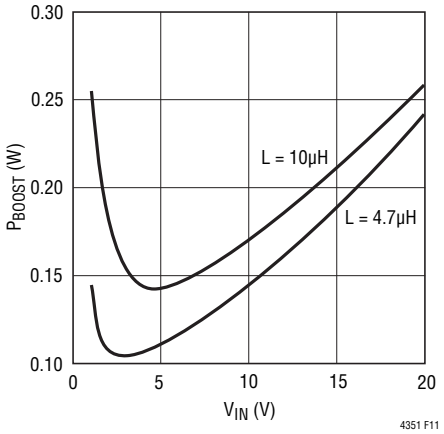


Figure 11. $P_{BOOST(MAX)}$

APPLICATIONS INFORMATION

Since the boost regulator supplies current for V_{DD}, the current is the V_{DD} supply current (3.5mA) plus the average current to charge the gate. For a gate charge of 50nC at a 10kHz rate, this adds 0.5mA of current. The power dissipated by the boost regulator to supply the 4mA is shown in Figure 12, representing a more typical situation.

Finally, the gate driver dissipates power internally when charging and discharging the gate of the MOSFETs. This power depends on the input capacitance of the MOSFETs and the frequency of charge and discharge. The power associated with this can be approximated by:

$$P_{GATE} = f_G \bullet V_{DD} \bullet Q_G \bullet \left(1 - \frac{V_{IN}}{16}\right)$$

where Q_G is the required gate charge to charge the MOSFET to the clamp voltage (7.4V) and f_G is the frequency at which the gate is charged and discharged. Normally f_G is low and the resulting power would be very low. Figure 13 shows P_{GATE} for a 50nC gate charge at a 1kHz rate.

Total power dissipation is the sum of all of P_{DCVIN}, P_{DCVDD}, P_{BOOST} and P_{GATE}. Figure 14 is representative of the total power dissipation of a typical application at steady state.

The die junction temperature is then computed as:

$$T_J = T_A + \theta_{JA} \bullet P_{TOTAL}$$

where T_J is the die junction temperature, T_A is the ambient temperature, θ_{JA} is the thermal resistance of the part (120°C/W) and P_{TOTAL} is ascertained from the above. Therefore, a 0.1W power dissipation causes a 12° temperature rise above ambient.

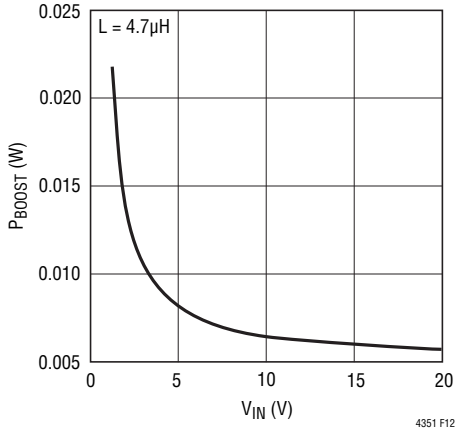


Figure 12. $P_{BOOST(TYP)}$

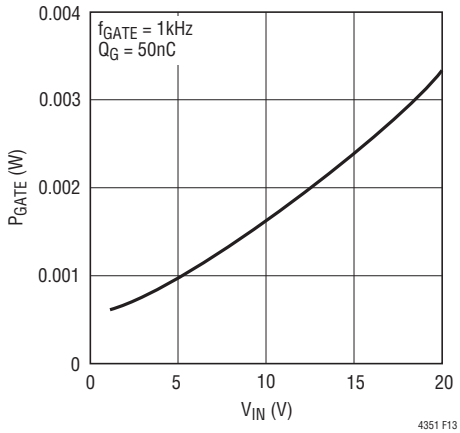


Figure 13. P_{GATE} vs V_{IN} (V_{DD} = V_{IN} + 10.7)

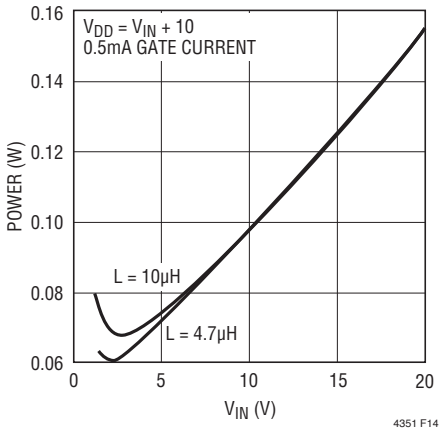


Figure 14. Total Power (Typical)

APPLICATIONS INFORMATION

Design Example

The following demonstrates the calculations involved for setting design components for a 5V system that requires 5A. Two supplies are used to do this. The V_{IN} supply will be deemed in spec when it is within ±5% of nominal. Allow 5% of hysteresis for UV.

So,

UV_{FAULT} = 4.75V, UV_{HYST} = 0.25V

OV_{FAULT} = 5.5

Two separate resistive dividers are used.

For the UV divider:

$$R2 = \frac{UV_{HYST}}{I_{UVHYST}} = \frac{0.25V}{10\mu A} = 25k \ \ (\text{Use } 24.9k)$$

$$R1 = \frac{R2 \bullet V_{UV}}{UV_{FAULT} - V_{UV}} = \frac{24.9k \bullet 0.3V}{4.75V - 0.3V}$$

R1 = 1.68k. The closest 1% value is 1.69k

The OV resistors are set as a straight resistive divider.

If the current in the R_A, R_B divider is 200µA, then:

$$R_A = \frac{0.3V}{200mA} = 1.5k \text{ use } 1.47k \ (1\%)$$

then

$$R_B = \left(\frac{OV_{FAULT}}{V_{OV}} - 1\right) R_A = \left(\frac{5.5}{0.3} - 1\right) 1.47k$$

R_B = 25.48, use 25.5k

For regulation, the MOSFETs must have:

$$R_{DS} < \frac{15mV}{2 \bullet 5A} = 1.5m\Omega$$

This very low value cannot be accomplished with a single set of MOSFETs so a decision must be made whether to use multiple MOSFETs or to live with an unregulated offset. Since low mΩ $R_{DS(ON)}$ is available, the IR drop using a single MOSFET would still be acceptable. For $R_{DS(ON)}$ = 4mΩ the drop is 2 • 5A • 4mΩ = 40mV. The finished schematic is shown in Figure 15.

Layout Considerations

There are two considerations for board layout. The first is that V_{IN} and V_{DD} bypass capacitors should be as close to the part as possible. The GND pin should represent the common tie point. The resistive dividers for UV and OV should tie here as well.

Take care that current flow to the load (both through V_{IN} and GND), does not inadvertently produce errors due to IR drops in PCB traces.

Keep the traces to the MOSFETs wide and short and close to the part. The PCB traces associated with the power path through the MOSFETs should have low resistance.

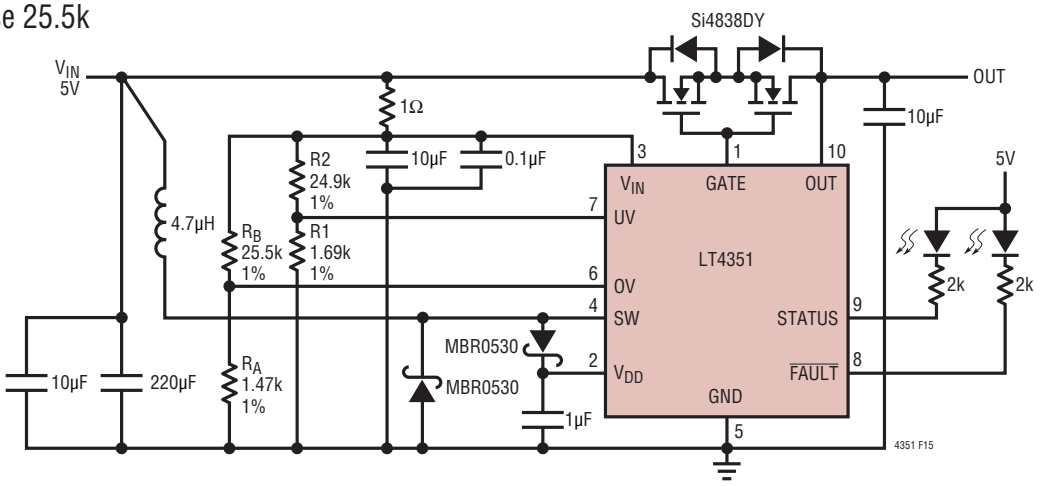
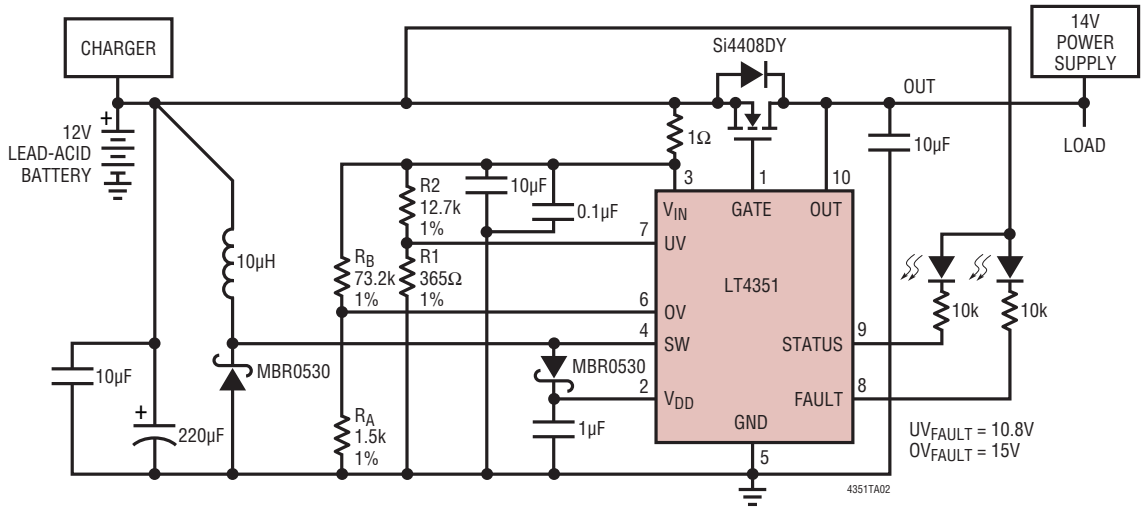


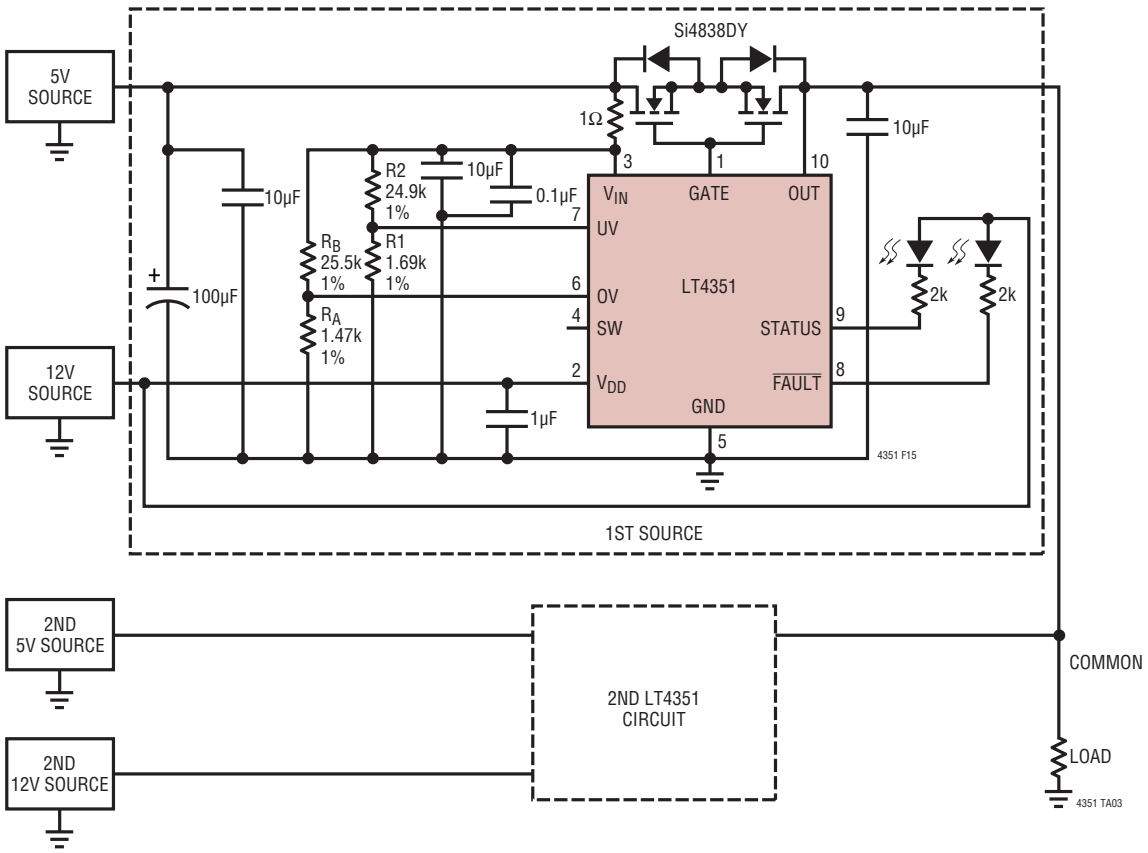
Figure 15. 5V/5A Design Example

TYPICAL APPLICATIONS

Lead Acid Battery Backup



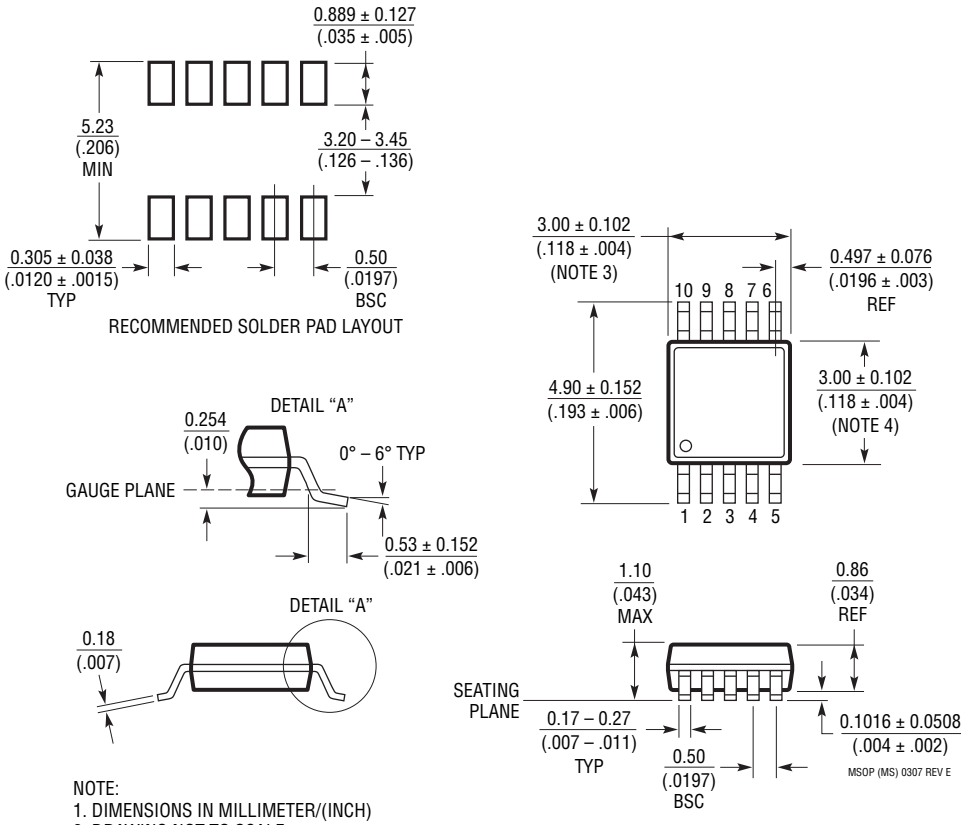
5V Redundant Supply with External V_{DD}



PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

MS Package
10-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1661 Rev E)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

REVISION HISTORY (Revision history begins at Rev C)

REV	DATE	DESCRIPTION	PAGE NUMBER
C	12/10	Reversed orientation of N-channel MOSFETs in Typical Application drawing.	1
D	12/11	Revised V_{BR} Maximum value in Electrical Characteristics section	3