40MHz to 900MHz Quadrature Demodulator

FEATURES

- **RF Input Frequency Range: 40MHz to 900MHz**
- **High IIP3: 21dBm at 800MHz**
- **High IIP2: 58dBm at 800MHz**
- **I/Q Gain Mismatch: 0.3dB Max**
- **I/Q Phase Mismatch: 0.7°**
- Noise Figure: 12.4dB at 800MHz
- Conversion Gain: 3.3dB at 800MHz
- Baseband Bandwidth: 130MHz
- Single Ended, 50Ω Matched 2XLO Input
- Shutdown Mode
- 16-Lead QFN (4mm × 4mm) Package with Exposed Pad

APPLICATIONS

- Wireless Infrastructure
- High Linearity Direct Conversion I/Q Receiver
- High Linearity I/Q Demodulator

DESCRIPTION

The LT®5517 is a 40MHz to 900MHz quadrature demodulator optimized for high linearity receiver applications where high dynamic range is important. It is suitable for communications receivers where an RF or IF signal is directly converted into I and Q baseband signals with a bandwidth up to 130MHz. The LT5517 incorporates balanced I and Q mixers, LO buffer amplifiers and a precision, broadband quadrature generator derived from an on-chip divide-by-two circuit.

The superior linearity and low noise performance of the LT5517 is achieved across its full frequency range. A well-balanced divide-by-two circuit generates precision quadrature LO carriers to drive the I mixer and the Q mixer. Consequently, the outputs of the I-channel and the Q-channel are well matched in amplitude, and their phases are 90° apart. The LT5517 also provides excellent 50Ω impedance matching at the 2XLO port across its entire frequency range.

TYPICAL APPLICATION

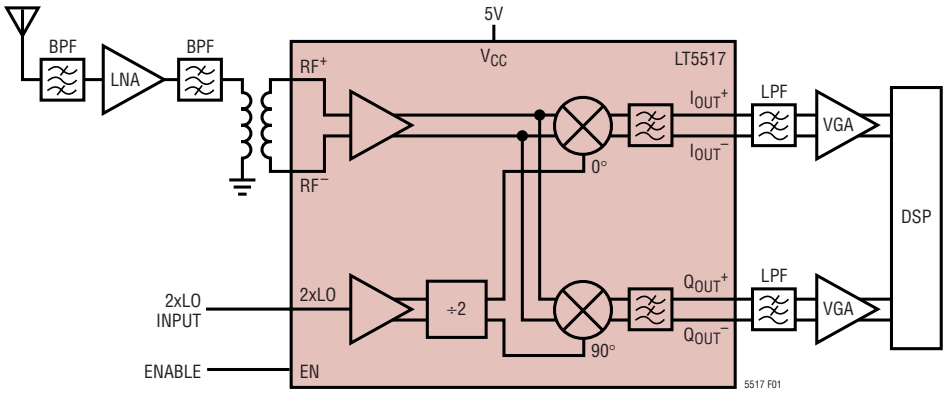
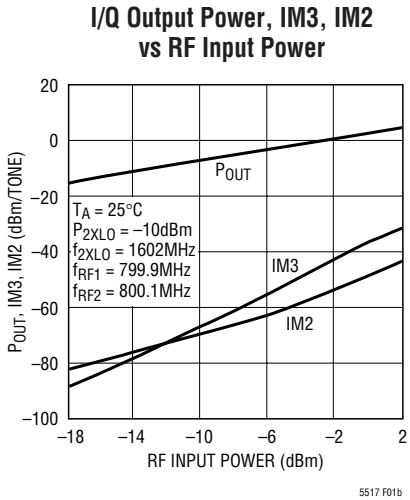


Figure 1. High Signal-Level I/Q Demodulator for 450MHz Infrastructure Receiver

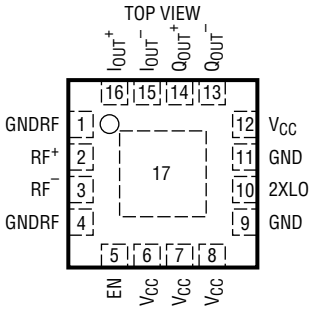


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Power Supply Voltage 5.5V
Enable Voltage ..... 0V, V_{CC}
2XLO Voltage (10dBm Equivalent) ..... ±1V
RF^+ to RF^- Differential Voltage
(10dBm Equivalent) ..... ±2V
Operating Ambient Temperature ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 125°C
Maximum Junction Temperature ..... 125°C

PACKAGE/ORDER INFORMATION



UF PACKAGE
16-LEAD (4mm × 4mm) PLASTIC QFN
EXPOSED PAD (PIN 17) IS GND,
MUST BE SOLDERED TO PCB

T_{JMAX} = 125°C, θ_{JA} = 37°C/W

ORDER PART NUMBER
LT5517EUF
UF PART MARKING
5517

Consult LTC Marketing for parts specified with wider operating temperature ranges.

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C. V_{CC} = 5V, EN = V_{CC}, f_{RF1} = 799.9MHz, f_{RF2} = 800.1MHz, f_{2XLO} = 1602MHz, P_{2XLO} = –10dBm, unless otherwise noted. (Notes 2, 3) (Test circuit shown in Figure 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
RF Frequency Range			40 to 900		MHz
2XLO Frequency Range			80 to 1800		MHz
2XLO Power			–15 to 0		dBm
2XLO Port Return Loss	Internally Matched to a 50Ω Source		20		dB
Conversion Gain	Voltage Gain, Load Impedance = 1kΩ	0	3.3		dB
Gain Variation vs Temperature	–40°C to 85°C		0.01		dB/°C
Noise Figure			12.4		dB
Input 3rd Order Intercept	2-Tone, –10dBm/Tone, Δf = 200kHz		21		dBm
Input 2nd Order Intercept	2-Tone, –10dBm/Tone, Δf = 200kHz		58		dBm
Input 1dB Compression			10		dBm
Baseband Bandwidth			130		MHz
I/Q Gain Mismatch	(Note 4)	–0.3	0.03	0.3	dB
I/Q Phase Mismatch	(Note 4)	–3.5	0.7	3.5	deg
Output Impedance	Differential		120		Ω
2XLO to RF Leakage			–69		dBm
LO to RF Leakage			–80		dBm
RF to 2XLO Isolation			63		dB

DC ELECTRICAL CHARACTERISTICS

T_A = 25°C. V_{CC} = 5V unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage		4.5		5.25	V
Supply Current		70	90	110	mA
Shutdown Current	EN = LOW		0.1	20	µA
Turn-On Time	(Note 5)		200		ns
Turn-Off Time	(Note 5)		300		ns
EN = HIGH (On)		1.6			V
EN = LOW (Off)				1.3	V
EN Input Current	V_{ENABLE} = 5V		2		µA
Output DC Offset Voltage ($\lvert I_{OUT}^+ - I_{OUT}^- \rvert$, $\lvert Q_{OUT}^+ - Q_{OUT}^- \rvert$)	f_{LO} = 1602MHz, P_{LO} = –10dBm		0.5	30	mV
Output DC Offset Variation vs Temperature	–40°C to 85°C		7		µV/°C

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: Tests are performed as shown in the configuration of Figure 2.

Note 3: Specifications over the –40°C to 85°C temperature range are assured by design, characterization and correlation with statistical process control.

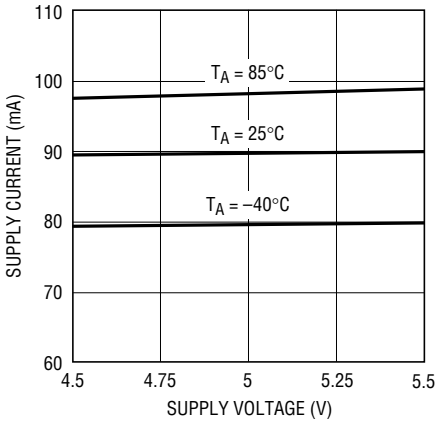
Note 4: Measured at P_{2XLO} = –10dBm and output frequency = 1MHz.

Note 5: Turn ON and Turn OFF times are based on rise and fall times of the output baseband voltage with RF input power of –10dBm.

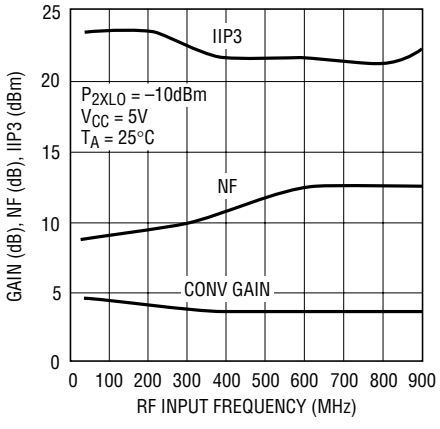
TYPICAL PERFORMANCE CHARACTERISTICS

f_{RF} = 800MHz, P_{2XLO} = –10dBm, unless otherwise noted. (Test circuit shown in Figure 2)

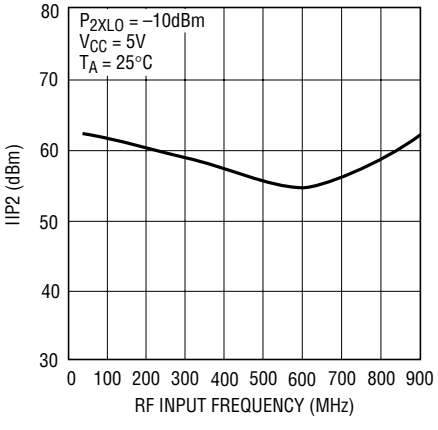
Supply Current vs Supply Voltage



Conv Gain, NF, IIP3 vs RF Input Frequency



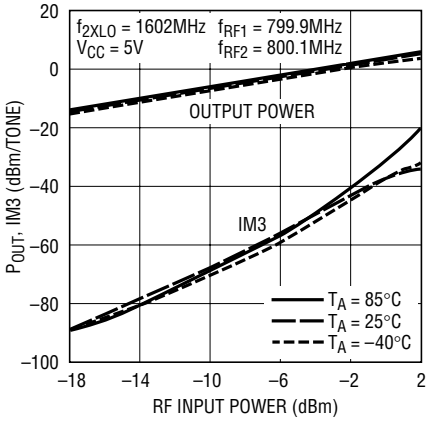
IIP2 vs RF Input Frequency



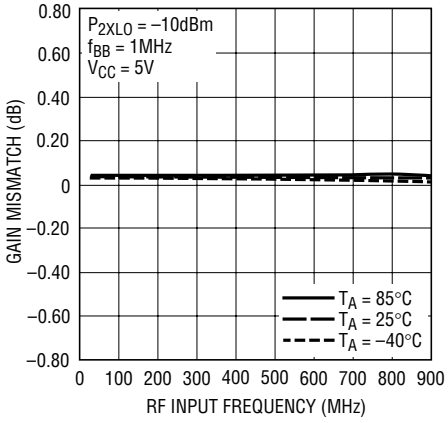
TYPICAL PERFORMANCE CHARACTERISTICS

f_{RF} = 800MHz, P_{2XLO} = –10dBm, unless otherwise noted. (Test circuit shown in Figure 2)

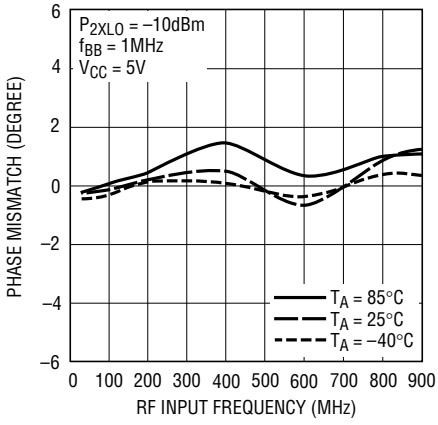
I/Q Output Power, IM3 vs RF Input Power



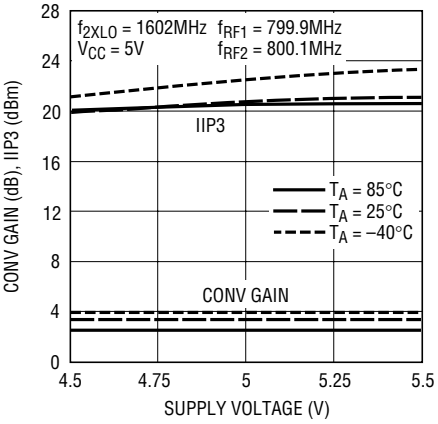
I/Q Gain Mismatch vs RF Input Frequency



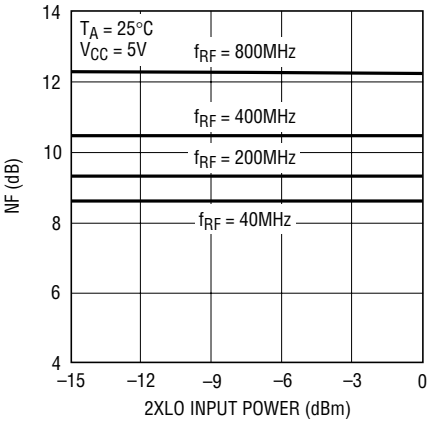
I/Q Phase Mismatch vs RF Input Frequency



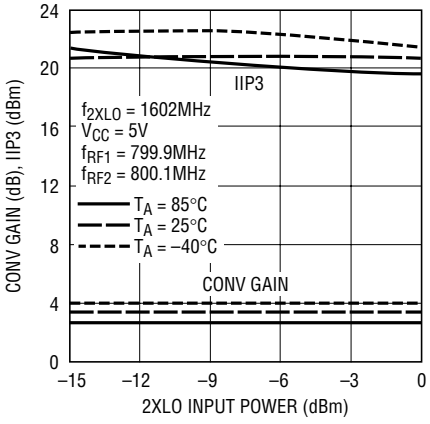
Conv Gain, IIP3 vs Supply Voltage



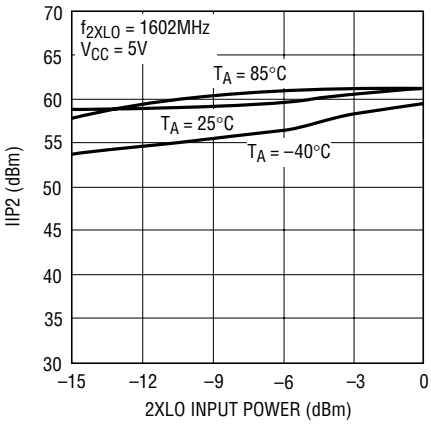
NF vs 2XLO Input Power



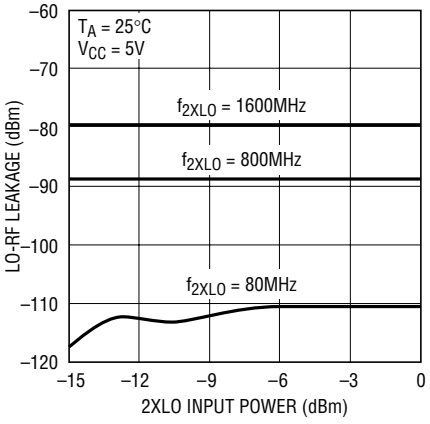
Conv Gain, IIP3 vs 2XLO Input Power



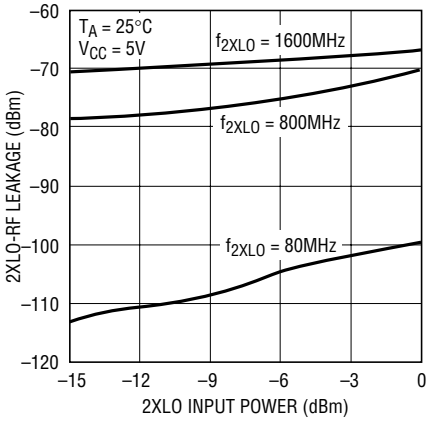
IIP2 vs 2XLO Input Power



LO-RF Leakage vs 2XLO Input Power



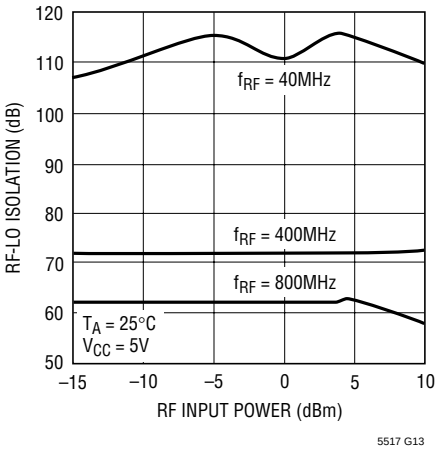
2XLO-RF Leakage vs 2XLO Input Power



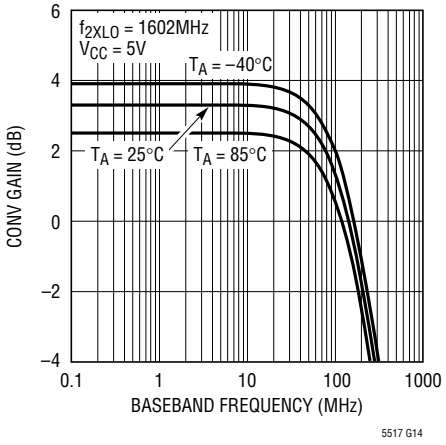
TYPICAL PERFORMANCE CHARACTERISTICS

f_{RF} = 800MHz, P_{2XLO} = –10dBm, unless otherwise noted. (Test circuit shown in Figure 2)

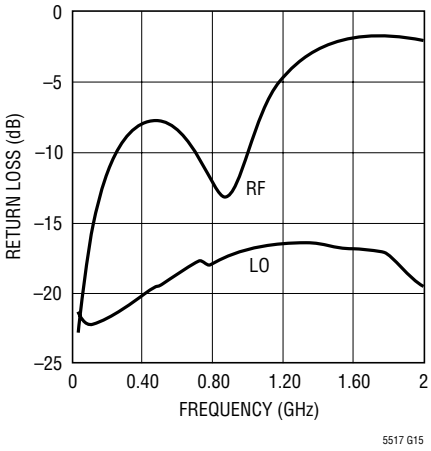
RF-LO Isolation vs RF Input Power



Conv Gain vs Baseband Frequency



RF, 2XLO Port Return Loss vs Frequency



PIN FUNCTIONS

GNDRF (Pins 1, 4): Ground Pins for RF Termination. These pins are not internally connected, and should be connected to the PCB ground plane for best RF isolation.

RF^+, RF^- (Pins 2, 3): Differential RF Input Pins. These pins are internally biased to 2.30V. These two pins should be DC blocked when connected to ground or other matching components. The inputs can be terminated in a single-ended configuration, but differential input drive is preferred for best performance. An external matching network is required for impedance transformation.

EN (Pin 5): Enable Pin. When the input voltage is higher than 1.6V, the circuit is completely turned on. When the input voltage is less than 1.3V, the circuit is turned off.

V_{CC} (Pins 6, 7, 8, 12): Power Supply Pins. These pins should be decoupled using 1000pF and 0.1µF capacitors.

GND (Pins 9, 11): Ground Pins. These pins are internally tied together and to the Exposed Pad. They should be connected to the PCB ground plane.

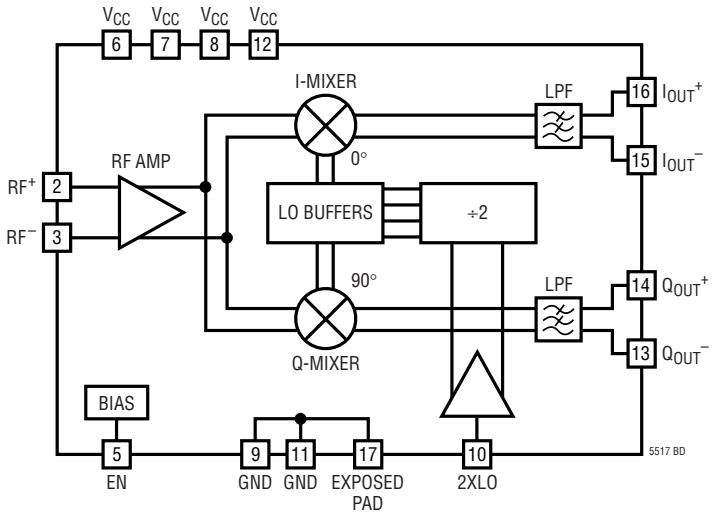
2XLO (Pin 10): 2XLO Input Pin. This pin is internally biased to 1V. The input signal's frequency should be twice that of the desired demodulator LO frequency. The pin should be AC coupled with an external DC blocking capacitor.

Q_{OUT}^-, Q_{OUT}^+ (Pins 13, 14): Differential Baseband Output Pins of the Q-Channel. The internal DC bias voltage is V_{CC} – 0.78V for each pin.

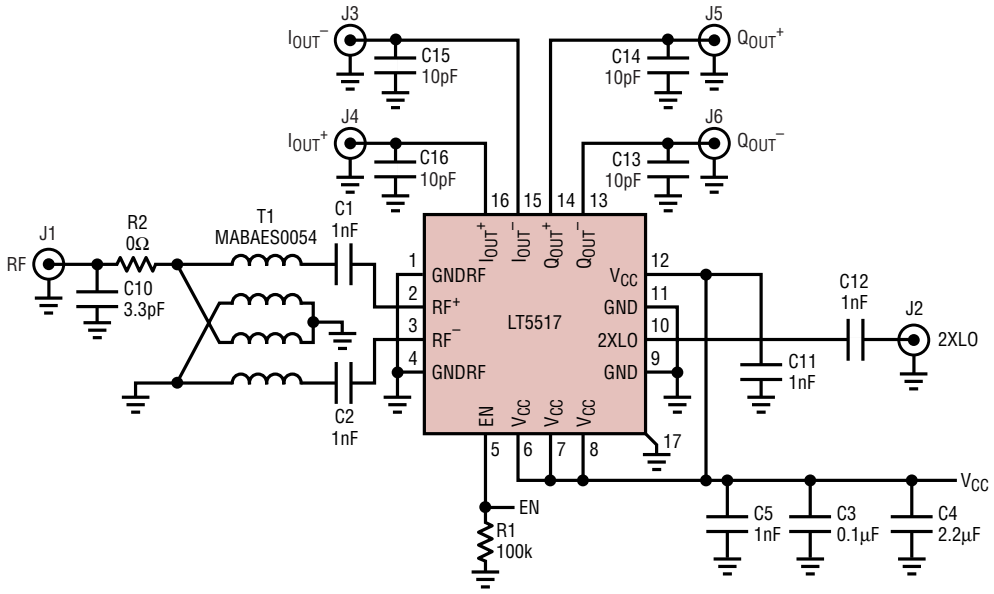
I_{OUT}^-, I_{OUT}^+ (Pins 15, 16): Differential Baseband Output Pins of the I-Channel. The internal DC bias voltage is V_{CC} – 0.78V for each pin.

Exposed Pad (Pin 17): Ground Return for the Entire IC. This pin must be soldered to the printed circuit board ground plane.

BLOCK DIAGRAM



TEST CIRCUIT



REFERENCE DESIGNATION	VALUE	SIZE	PART NUMBER
C1,C2,C5,C11,C12	1nF	0603	AVX 06033A102JAT1A
C3	0.1µF	0603	TAIYO YUDEN EMK107B
C4	2.2µF	0603	TAIYO YUDEN JMK107B
C10	3.3pF	0603	AVX 06033A3R3KAT2A
C13 TO C16	10pF	0805	AVX 08055A100ZAT1A
R1	100k	0603	OPTIONAL
R2	0Ω	0603	JUMPER, OPTIONAL
T1	1:4		M/A COM MABAES0054

5517 F02

Figure 2. Evaluation Circuit Schematic

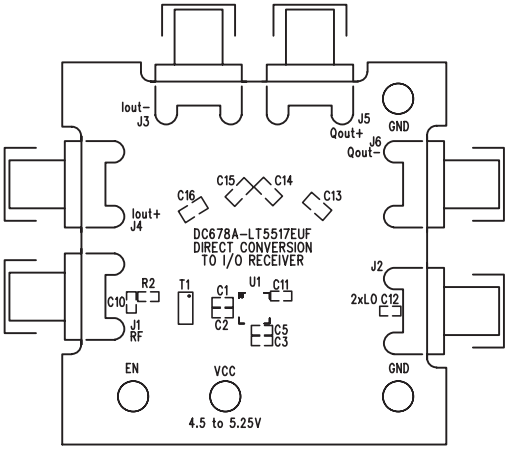


Figure 3. Component Side Silkscreen of Evaluation Board

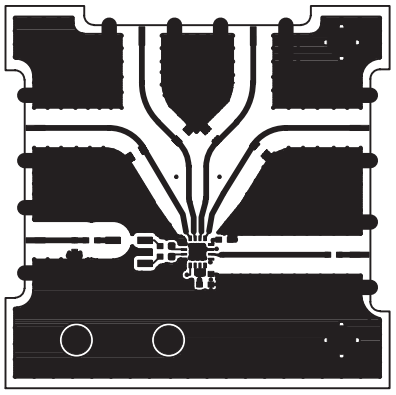


Figure 4. Component Side Layout of Evaluation Board

APPLICATIONS INFORMATION

The LT5517 is a direct I/Q demodulator targeting high linearity receiver applications. It consists of an RF amplifier, I/Q mixers, a quadrature LO carrier generator and bias circuitry.

The RF signal is applied to the inputs of the RF amplifier, and is then demodulated into I-channel and Q-channel baseband signals using precision quadrature LO signals, which are internally generated using a divide-by-two circuit. The demodulated I/Q signals are lowpass filtered internally with a –3dB bandwidth of 130MHz. The differential outputs of the I-channel and Q-channel are well matched in amplitude and their phases are 90° apart across the full frequency range from 40MHz to 900MHz.

RF Input Port

Differential drive is recommended for the RF inputs as shown in Figure 2. A low loss 1:4 transformer is used on the demonstration board for a wide bandwidth input impedance match and to assure good noise figure and maximum demodulator gain. Single-ended to differential conversion can also be implemented using narrowband L-C circuits to produce the required balanced waveforms at the RF^+ and RF^- inputs using three discrete elements as shown in Figure 5. Nominal values are listed in Table 1. (In practice, these values should be compensated according to the parasitics of the PCB.) The conversion gain and NF of the receiver are similar to those of the transformer-coupled demo board, because the single-ended to differential conversion has a 1:4 impedance transformation, similar to the transformer.

Table 1. The Component Values of Matching Network L_{SH}, C_{S1} and C_{S2}

FREQUENCY (MHz)	L_{SH} (nH)	C_{S1}, C_{S2} (pF)
40	437	71.1
100	169	28.6
200	80.8	14.3
300	51.5	9.6
400	37	7.2
500	28.3	5.8
600	22.6	4.9
700	18.5	4.2
800	15.6	3.7
900	13.5	3.3

The differential impedance of the RF inputs is listed in Table 2. The RF inputs may also be terminated in a single-ended configuration. In this case either the RF^+ or the RF^- input can be simply AC coupled to a 50Ω source, while the other RF input is connected to ground with a 1nF capacitor. Note, however, that this will result in degraded conversion gain and noise figure in most cases.

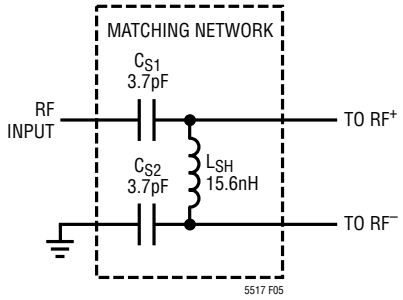


Figure 5. RF Input Matching Network at 800MHz

APPLICATIONS INFORMATION

Table 2. RF Input Differential Impedance

FREQUENCY (MHz)	DIFFERENTIAL INPUT IMPEDANCE (Ω)	DIFFERENTIAL S11	
		MAG	ANGLE(°)
40	240.1-j10.3	0.665	–0.8
100	245.5-j25.9	0.664	–2.5
200	236.8-j50.0	0.664	–5.1
300	223.6-j70.5	0.663	–7.6
400	207.9-j86.3	0.662	–10.2
500	190.6-j98.1	0.660	–12.7
600	173.2-j105.8	0.657	–15.3
700	156.2-j110.2	0.655	–17.9
800	141.2-j111.8	0.651	–20.4
900	129.5-j114.5	0.650	–22.9

2XLO Input Port

To ease the interface of the receiver with the external 2XLO input, the 2XLO port is designed with on-chip 50Ω impedance matching up to 2GHz. The input is internally biased at 1V. A 1nF DC blocking capacitor is required when connected to the external 2XLO source.

The 2XLO frequency is required to be twice the desired operating frequency in order for the chip to generate the quadrature Local Oscillator (LO) signals for the demodulator. The on-chip divide-by-two circuit delivers well-matched, quadrature LO carriers to the I mixer and the Q mixer.

I-Channel and Q-Channel Outputs

Each of the I-channel and Q-channel outputs is internally connected to V_{CC} though a 60Ω resistor. The output DC bias voltage is V_{CC} – 0.78V. The outputs can be DC coupled or AC coupled to the external loads. The differential output impedance of the demodulator is 120Ω in parallel with a 10pF internal capacitor, forming a lowpass filter with a –3dB corner frequency at 130MHz. The load impedance, R_{LOAD}, should be larger than 600Ω to assure full gain. The gain is reduced by $20 \bullet \log(1 + 120\Omega/R_{LOAD})$ in dB when the differential output is terminated by R_{LOAD}. For example, the gain is reduced by 6.85dB when each output pin is connected to a 50Ω load (or 100Ω differential loads). The output should be taken differentially (or by using differential-to-single-ended conversion) for best RF performance, including NF and IM2. Proper filtering of the unwanted high frequency mixing product is also important to maintain the highest linearity. A convenient

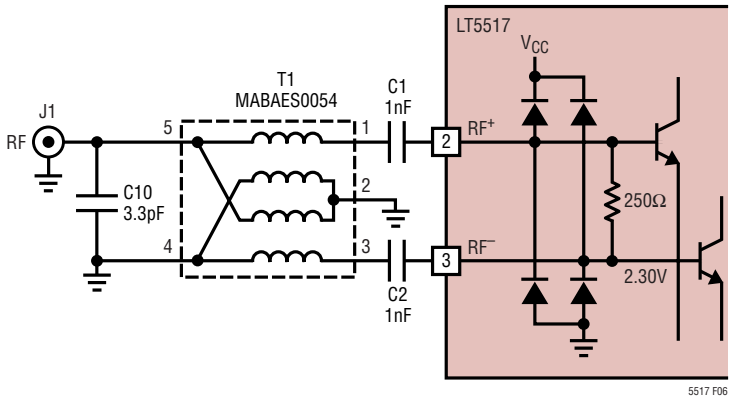


Figure 6. RF Input Equivalent Circuit with External Broadband Matching

APPLICATIONS INFORMATION

approach is to terminate each output with a shunt capacitor. The capacitor value can be optimized depending upon the operating frequency and the specific PCB layout.

The phase relationship between the I-channel output signal and the Q-channel output signal is fixed. When the LO input frequency is higher than the RF input frequency, then the Q-channel outputs (Q_{OUT}^+, Q_{OUT}^-) lead the I-channel outputs (I_{OUT}^+, I_{OUT}^-) by 90°.

When the LO input frequency is lower than the RF input frequency, then the Q-channel outputs lag the I-channel outputs by 90°. Note that the phase relationship of the I- and Q-channel outputs relative to the LO can vary by 180°, depending on start-up conditions. This is the nature of a frequency divider-based quadrature phase generator.

When AC output coupling is used, the resulting highpass filter's –3dB roll-off frequency is defined by the R-C constant of the blocking capacitor and R_{LOAD}, assuming $R_{LOAD} > 600\Omega$.

Care should be taken when the demodulator's outputs are DC coupled to the external load to make sure that the I/Q mixers are biased properly. If the current drain from the outputs exceeds 6mA, there can be significant degradation of the linearity performance. Each output can sink no more than 13mA when connected to an external load with a DC voltage higher than V_{CC} – 0.78V.

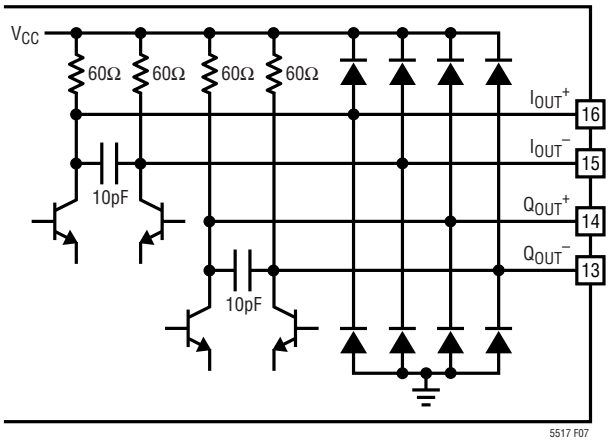
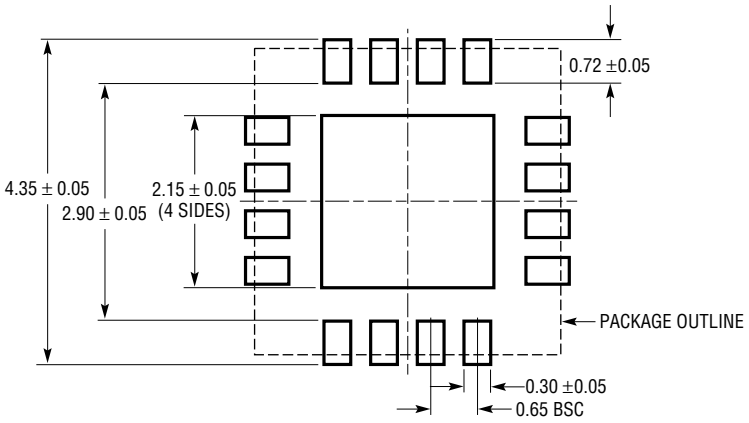


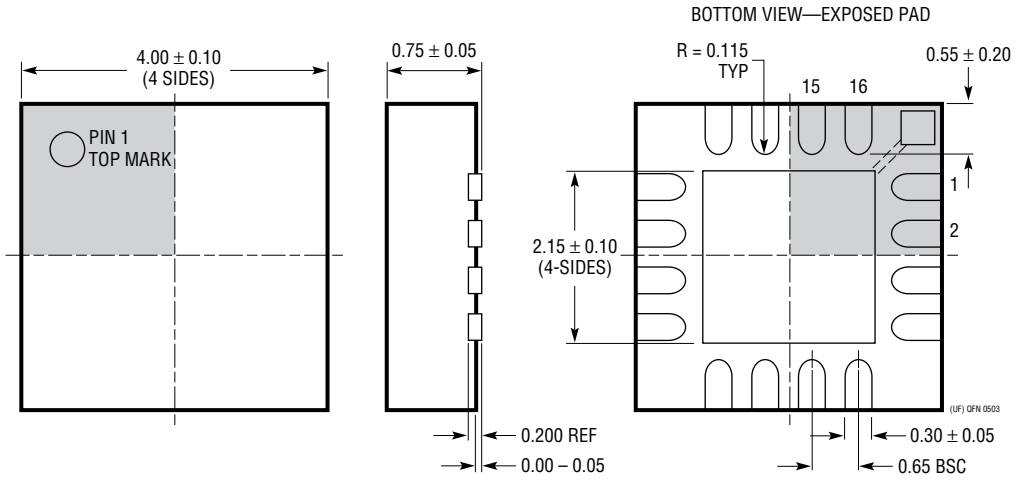
Figure 7. I/Q Output Equivalent Circuit

PACKAGE DESCRIPTION

UF Package
16-Lead Plastic QFN (4mm × 4mm)
(Reference LTC DWG # 05-08-1692)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGGC)
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
4. EXPOSED PAD SHALL BE SOLDER PLATED