1.3GHz to 2.3GHz High Linearity Upconverting Mixer

FEATURES

- **Wide RF Output Frequency Range: 1.3GHz to 2.3GHz**
- **15.9dBm Typical Input IP3 at 1.9GHz**
- **On-Chip RF Output Transformer**
- **No External LO or RF Matching Required**
- **Single-Ended LO and RF Operation**
- **Integrated LO Buffer: –5dBm Drive Level**
- **Low LO to RF Leakage: – 41dBm Typical**
- Wide IF Frequency Range: DC to 400MHz
- Enable Function with Low Off-State Leakage Current
- Single 5V Supply
- Small 16-Lead QFN Plastic Package

APPLICATIONS

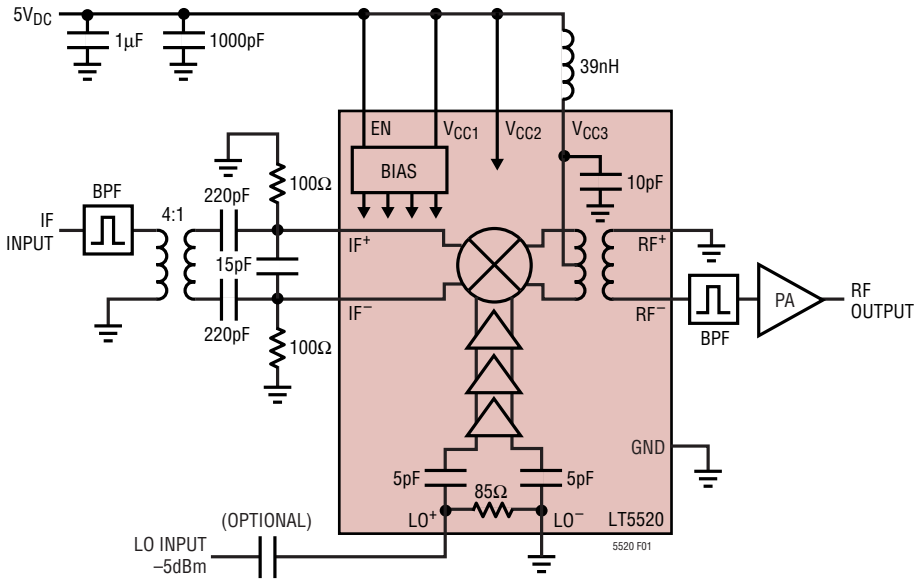
- Wireless Infrastructure
- Cable Downlink Infrastructure
- Point-to-Point Data Communications
- High Linearity Frequency Conversion

DESCRIPTION

The LT®5520 mixer is designed to meet the high linearity requirements of wireless and cable infrastructure transmission applications. A high-speed, internally matched, LO amplifier drives a double-balanced mixer core, allowing the use of a low power, single-ended LO source. An RF output transformer is integrated, thus eliminating the need for external matching components at the RF output, while reducing system cost, component count, board area and system-level variations. The IF port can be easily matched to a broad range of frequencies for use in many different applications.

The LT5520 mixer delivers 15.9dBm typical input 3rd order intercept point at 1.9GHz with IF input signal levels of –10dBm. The input 1dB compression point is typically 4dBm. The IC requires only a single 5V supply.

TYPICAL APPLICATION



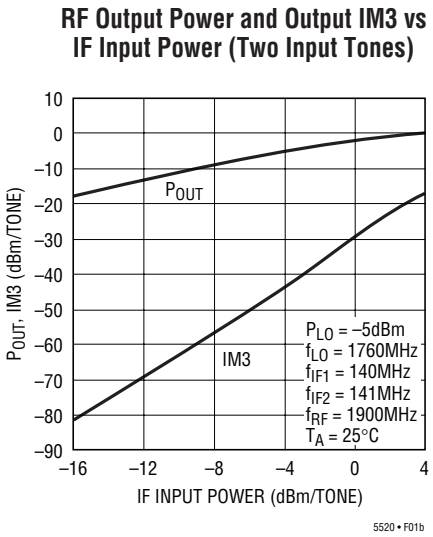


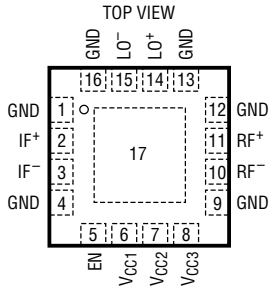
Figure 1. Frequency Conversion in Wireless Infrastructure Transmitter

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage 5.5V
Enable Voltage ..... –0.3V to (V_{CC} + 0.3V)
LO Input Power (Differential) 10dBm
RF^+ to RF^- Differential DC Voltage ..... ±0.13V
RF Output DC Common Mode Voltage ..... –1V to V_{CC}
IF Input Power (Differential) 10dBm
IF^+, IF^- DC Currents 25mA
LO^+ to LO^- Differential DC Voltage ..... ±1V
LO Input DC Common Mode Voltage ..... –1V to V_{CC}
Operating Temperature Range ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 125°C
Junction Temperature (T_J) ..... 125°C

PACKAGE/ORDER INFORMATION



UF PACKAGE
16-LEAD (4mm × 4mm) PLASTIC QFN
EXPOSED PAD IS GND (PIN 17),
MUST BE SOLDERED TO PCB

T_{JMAX} = 125°C, θ_{JA} = 37°C/W

ORDER PART NUMBER
LT5520EUF
UF PART MARKING
5520

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
IF Input Frequency Range			DC to 400		MHz
LO Input Frequency Range			900 to 2700		MHz
RF Output Frequency Range			1300 to 2300		MHz

1900MHz Application: V_{CC} = 5V_{DC}, EN = High, T_A = 25°C, IF input = 140MHz at –10dBm, LO input = 1.76GHz at –5dBm, RF output measured at 1900MHz, unless otherwise noted. Test circuit shown in Figure 2. (Notes 2, 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
IF Input Return Loss	Z_O = 50Ω, with External Matching		20		dB
LO Input Return Loss	Z_O = 50Ω		16		dB
RF Output Return Loss	Z_O = 50Ω		20		dB
LO Input Power			–10 to 0		dBm
Conversion Gain			–1		dB
Input 3rd Order Intercept	–10dBm/Tone, Δf = 1MHz		15.9		dBm
Input 2nd Order Intercept	–10dBm, Single-Tone		45		dBm
LO to RF Leakage			–41		dBm
LO to IF Leakage			–35		dBm
Input 1dB Compression			4		dBm
IF Common Mode Voltage	Internally Biased		1.77		V_{DC}
Noise Figure	Single Side Band		15		dB

DC ELECTRICAL CHARACTERISTICS

(Test Circuit Shown in Figure 2) V_{CC} = 5V_{DC}, EN = High , T_A = 25°C (Note 3), unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Enable (EN) Low = Off, High = On					
Turn-On Time (Note 4)			2		µs
Turn-Off Time (Note 4)			6		µs
Input Current	V_{ENABLE} = 5V_{DC}		1	10	µA

DC ELECTRICAL CHARACTERISTICS

(Test Circuit Shown in Figure 2) V_{CC} = 5V_{DC}, EN = High , T_A = 25°C (Note 3), unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Enable = High (On)		3			V_{DC}
Enable = Low (Off)				0.5	V_{DC}
Power Supply Requirements (V_{CC})					
Supply Voltage			4.5 to 5.25		V_{DC}
Supply Current	V_{CC} = 5V_{DC}		60	70	mA
Shutdown Current	EN = Low		1	100	µA

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

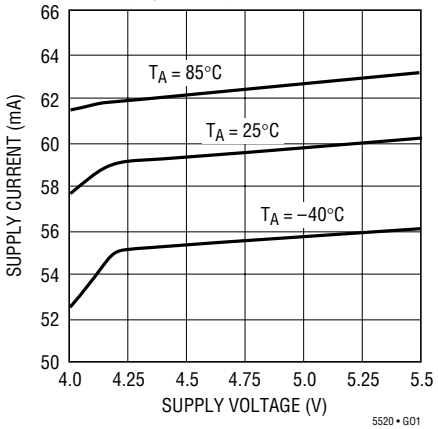
Note 2: External components on the final test circuit are optimized for operation at f_{RF} = 1900MHz, f_{LO} = 1.76GHz and f_{IF} = 140MHz.

Note 3: Specifications over the –40°C to 85°C temperature range are assured by design, characterization and correlation with statistical process controls.

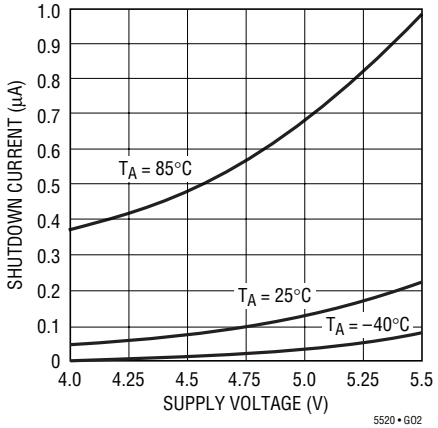
Note 4: Turn-On and Turn-Off times are based on the rise and fall times of the RF output envelope from full power to –40dBm with an IF input power of –10dBm.

TYPICAL PERFORMANCE CHARACTERISTICS (Test Circuit Shown in Figure 2)

Supply Current vs Supply Voltage

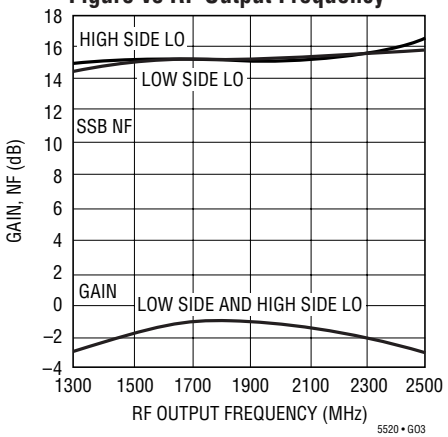


Shutdown Current vs Supply Voltage

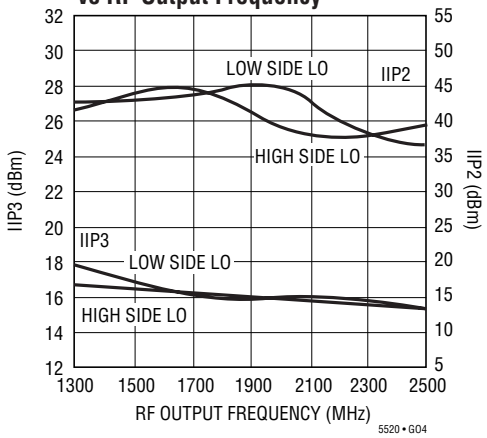


V_{CC} = 5V_{DC}, EN = High, T_A = 25°C, IF input = 140MHz at –10dBm, LO input = 1.76GHz at –5dBm, RF output measured at 1900MHz, unless otherwise noted. For 2-tone inputs: 2nd IF input = 141MHz at –10dBm. (Test Circuit Shown in Figure 2.)

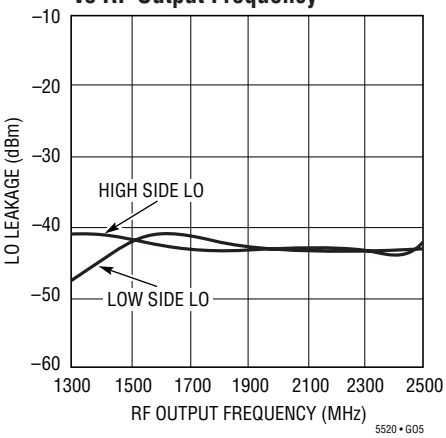
Conversion Gain and SSB Noise Figure vs RF Output Frequency



IIP3 and IIP2 vs RF Output Frequency



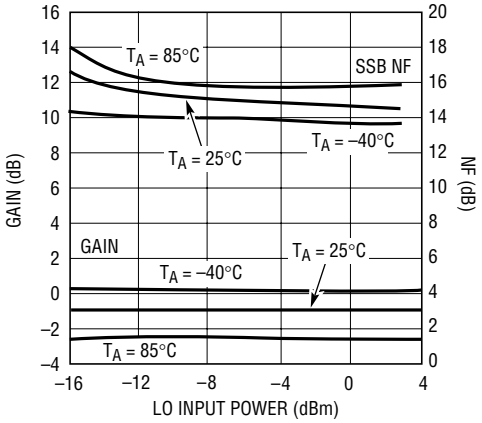
LO-RF Leakage vs RF Output Frequency



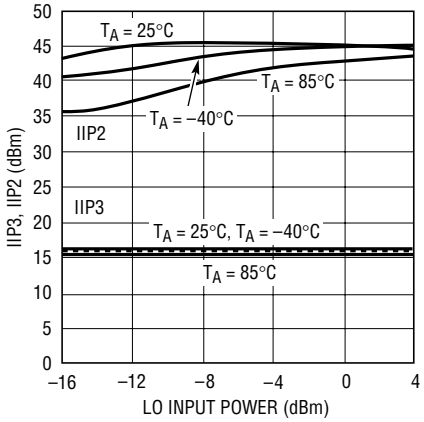
TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 5V_{DC}, EN = High , T_A = 25°C, IF input = 140MHz at –10dBm, LO input = 1.76GHz at –5dBm, RF output measured at 1900MHz, unless otherwise noted. For 2-tone inputs: 2nd IF Input = 141MHz at –10dBm. (Test Circuit Shown in Figure 2.)

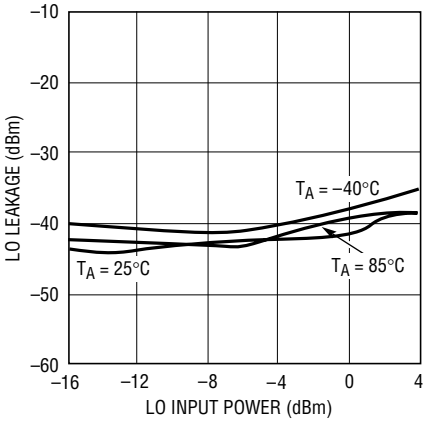
Conversion Gain and SSB Noise Figure vs LO Input Power



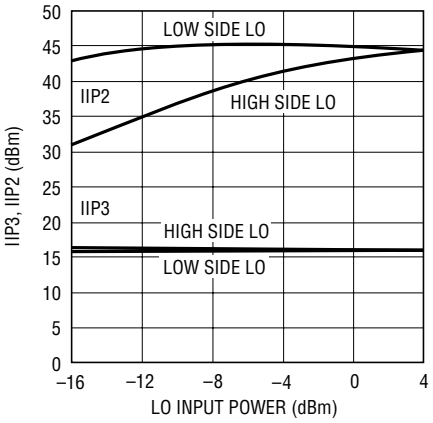
IIP3 and IIP2 vs LO Input Power



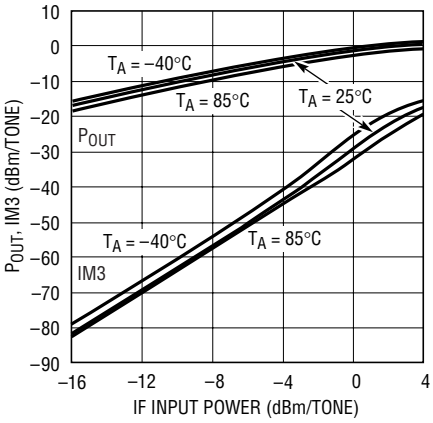
LO-RF Leakage vs LO Input Power



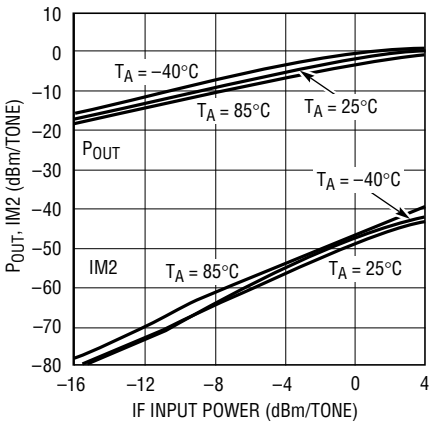
IIP3 and IIP2 vs LO Input Power



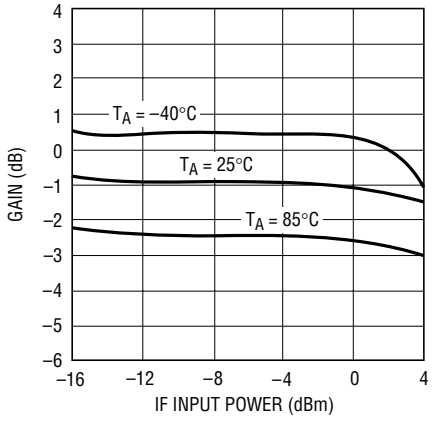
RF Output Power and Output IM3 vs IF Input Power (Two Input Tones)



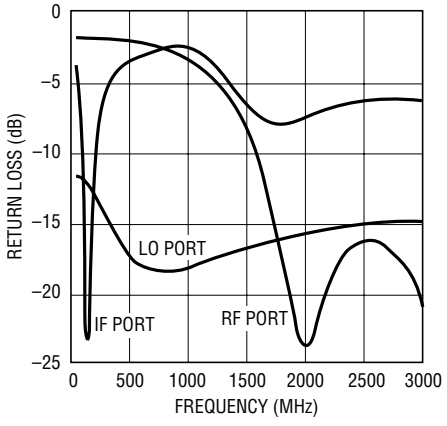
RF Output Power and Output IM2 vs IF Input Power (Two Input Tones)



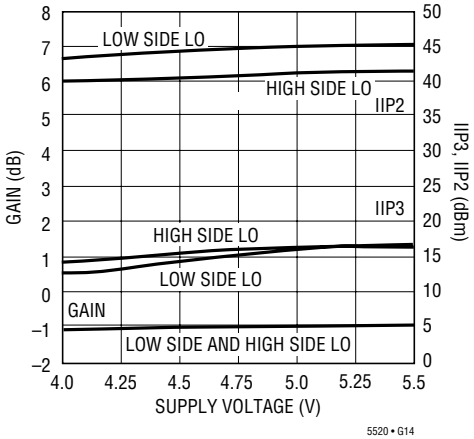
Conversion Gain vs IF Input Power (One Input Tone)



IF, LO and RF Port Return Loss vs Frequency



Conversion Gain, IIP3 and IIP2 vs Supply Voltage



PIN FUNCTIONS

GND (Pins 1, 4, 9, 12, 13, 16): Internal Grounds. These pins are used to improve isolation and are not intended as DC or RF grounds for the IC. Connect these pins to low impedance grounds for best performance.

IF+, IF– (Pins 2, 3): Differential IF Signal Inputs. A differential signal must be applied to these pins through DC blocking capacitors. The pins must be connected to ground with 100Ω resistors (the grounds must each be capable of sinking about 18mA). For best LO leakage performance, these pins should be DC isolated from each other. An impedance transformation is required to match the IF input to the desired source impedance (typically 50Ω or 75Ω).

EN (Pin 5): Enable Pin. When the applied voltage is greater than 3V, the IC is enabled. When the applied voltage is less than 0.5V, the IC is disabled and the DC current drops to about 1μA.

V_{CC1} (Pin 6): Power Supply Pin for the Bias Circuits. Typical current consumption is about 2mA. This pin should be externally connected to V_{CC} and have appropriate RF bypass capacitors.

V_{CC2} (Pin 7): Power Supply Pin for the LO Buffer Circuits. Typical current consumption is about 22mA. This pin should have appropriate RF bypass capacitors as shown in Figure 2. The 1000pF capacitor should be located as close to the pins as possible.

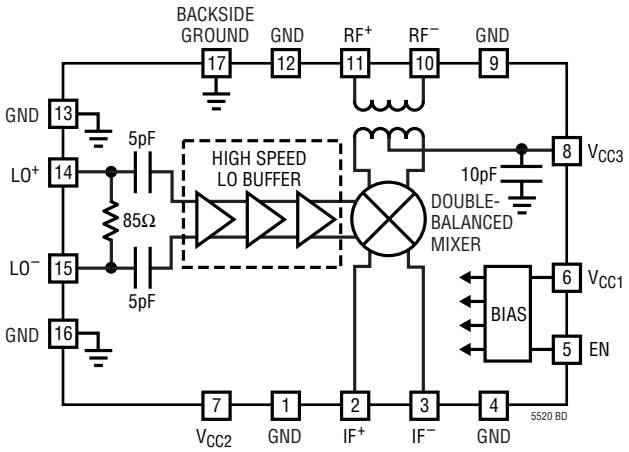
V_{CC3} (Pin 8): Power Supply Pin for the Internal Mixer. Typical current consumption is about 36mA. This pin should be externally connected to V_{CC} through an inductor. A 39nH inductor is used in Figure 2, though the value is not critical.

RF–, RF+ (Pins 10, 11): Differential RF Outputs. One pin may be DC connected to a low impedance ground to realize a 50Ω single-ended output. No external matching components are required. A DC voltage should not be applied across these pins, as they are internally connected through a transformer winding.

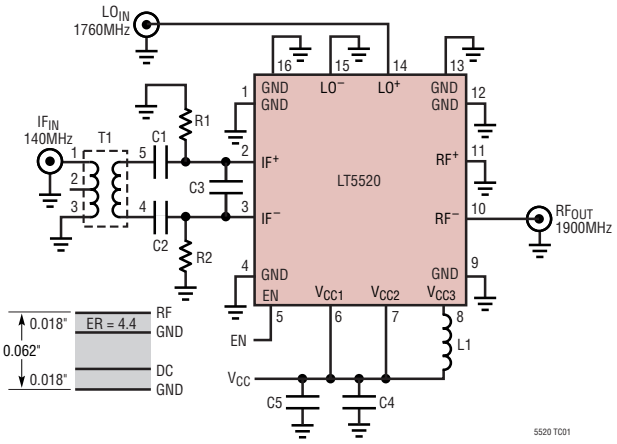
LO+, LO– (Pins 14, 15): Differential Local Oscillator Inputs. The LT5520 works well with a single-ended source driving the LO+ pin and the LO– pin connected to a low impedance ground. No external matching components are required. An internal resistor is connected across these pins; therefore, a DC voltage should not be applied across the inputs.

GROUND (Pin 17, Exposed Pad): DC and RF ground return for the entire IC. This must be soldered to the printed circuit board low impedance ground plane.

BLOCK DIAGRAM



TEST CIRCUIT



REF DES	VALUE	SIZE	PART NUMBER
C1, C2	220pF	0402	AVX 04023C221KAT2A
C3	15pF	0402	AVX 04023A150KAT2A
C4	1000pF	0402	AVX 04023A102KAT2A
C5	1µF	0603	Taiyo Yuden LMK107BJ105MA
L1	39nH	0402	Toko LL1005-FH39NJ
R1, R2	100Ω, 0.1%	0603	IRC PFC-W0603R-03-10R1-B
T1	4:1	SM-22	M/A-COM ETC4-1-2

Figure 2. Test Schematic for the LT5520

APPLICATIONS INFORMATION

The LT5520 consists of a double-balanced mixer, a high-performance LO buffer, and bias/enable circuits. The RF and LO ports may be driven differentially; however, they are intended to be used in single-ended mode by connecting one input of each pair to ground. The IF input ports must be DC-isolated from the source and driven differentially. The IF input should be impedance-matched for the desired input frequency. The LO input has an internal broadband 50Ω match with return loss better than 10dB at frequencies up to 3000MHz. The RF output band ranges from 1300MHz to 2300MHz, with an internal RF transformer providing a 50Ω impedance match across the band. Low side or high side LO injection can be used.

IF Input Port

The IF inputs are connected to the emitters of the double-balanced mixer transistors, as shown in Figure 3. These pins are internally biased and an external resistor must be connected from each IF pin to ground to set the current through the mixer core. The circuit has been optimized to work with 100Ω resistors, which will result in approximately 18mA of DC current per side. For best LO leakage performance, the resistors should be well matched; thus resistors with 0.1%, tolerance are recommended. If LO leakage is not a concern, then lesser tolerance resistors can be used. The symmetry of the layout is also important for achieving optimum LO isolation.

The capacitors shown in Figure 3, C1 and C2, serve two purposes. They provide DC isolation between the IF^+ and IF^- ports, thus preventing DC interactions that could cause unpredictable variations in LO leakage. They also improve the impedance match by canceling excess inductance in the package and transformer. The input capacitor value required to realize an impedance match at desired frequency, f, can be estimated as follows:

$$C_1 = C_2 = \frac{1}{(2\pi f)^2 (L_{IN} + L_{EXT})}$$

where; f is in units of Hz, L_{IN} and L_{EXT} are in H, and C1, C2 are in farad. L_{IN} is the differential input inductance of the LT5520, and is approximately 1.67nH. L_{EXT} represents the combined inductances of differential external components and transmission lines. For the evaluation board shown in Figure 10, L_{EXT} = 4.21nH. Thus, for f = 140MHz, the above formula gives C1 = C2 = 220pF.

APPLICATIONS INFORMATION

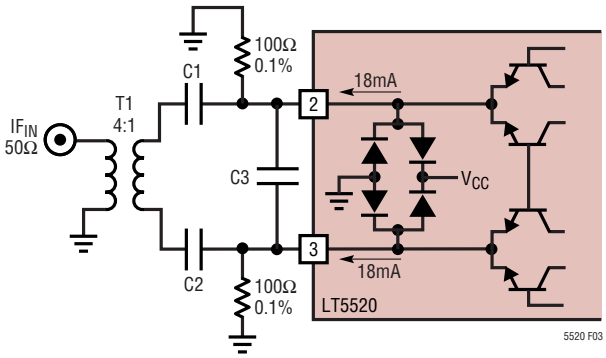


Figure 3. IF Input with External Matching

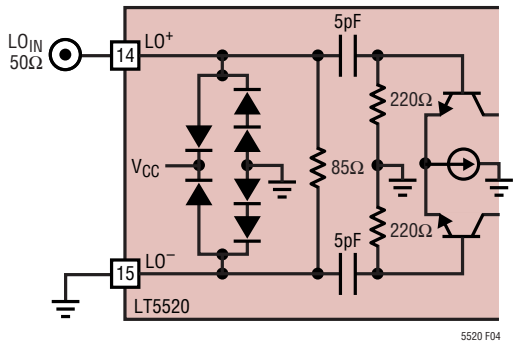


Figure 4. LO Input Circuit

Table 1 lists the differential IF input impedance and reflection coefficient for several frequencies. A 4:1 balun can be used to transform the impedance up to about 50Ω.

Table 1. IF Input Differential Impedance

Frequency (MHz)	Differential Input Impedance	Differential S11	
		Mag	Angle
10	10.1 + j0.117	0.663	180
44	10.1 + j0.476	0.663	179
70	10.1 + j0.751	0.663	178
140	10.2 + j1.47	0.663	177
170	10.2 + j1.78	0.663	176
240	10.2 + j2.53	0.663	174
360	10.2 + j3.81	0.663	171
500	10.2 + j5.31	0.663	167

LO Input Port

The simplified circuit for the LO buffer input is shown in Figure 4. The LO buffer amplifier consists of high-speed limiting differential amplifiers, optimized to drive the mixer quad for high linearity. The LO^+ and LO^- ports can be driven differentially; however, they are intended to be driven by a single-ended source. An internal resistor connected across the LO^+ and LO^- inputs provides a broadband 50Ω impedance match. Because of the resistive match, a DC voltage at the LO input is not recommended. If the LO signal source output is not AC coupled, then a DC blocking capacitor should be used at the LO input.

Though the LO input is internally 50Ω matched, there may be some cases, particularly at higher frequencies or with different source impedances, where a further optimized match is desired. Table 2 includes the single -ended input impedance and reflection coefficient vs frequency for the LO input for use in such cases.

Table 2. Single-Ended LO Input Impedance

Frequency (MHz)	Input Impedance	S11	
		Mag	Angle
1300	62.8 – j9.14	0.139	–30.9
1500	62.2 – j11.4	0.148	–37.1
1700	61.5 – j13.4	0.157	–42.4
1900	60.0 – j15.2	0.164	–48.9
2100	58.4 – j16.9	0.172	–54.7
2300	56.5 – j17.9	0.176	–60.4
2500	54.9 – j18.8	0.182	–65.1
2700	53.7 – j18.8	0.182	–68.5

RF Output Port

An internal RF transformer, shown in Figure 5, reduces the mixer-core impedance to provide an impedance of 50Ω across the RF^+ and RF^- pins. The LT5520 is designed and tested with the outputs configured for single-ended operation, as shown in the Figure 5; however, the outputs can be used differentially as well. A center-tap in the transformer provides the DC connection to the mixer core and the transformer provides DC isolation at the RF output. The RF^+ and RF^- pins are connected together through the secondary windings of the transformer, thus a DC voltage should not be applied across these pins.

APPLICATIONS INFORMATION

The impedance data for the RF output, listed in Table 3, can be used to develop matching networks for different load impedances.

Table 3. Single-Ended RF Output Impedance

Frequency (MHz)	Input Impedance	S11	
		Mag	Angle
1300	26.9 + j38.2	0.520	94.7
1500	44.2 + j35.7	0.359	78.4
1700	53.9 + j20.6	0.198	68.0
1900	49.5 + j7.97	0.080	88.9
2100	42.8 + j4.14	0.089	148
2300	38.9 + j5.41	0.139	151
2500	38.7 + j7.78	0.154	140
2700	41.1 – j9.51	0.142	127

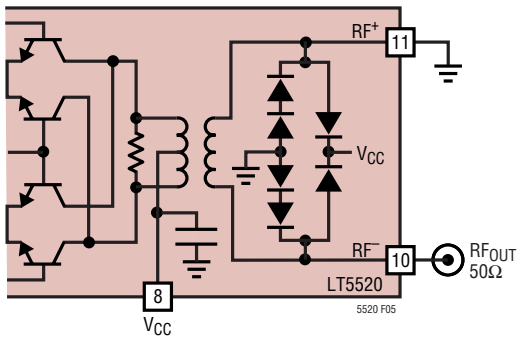


Figure 5. RF Output Circuit

Operation at Different Input Frequencies

On the evaluation board shown in Figure 10, the input of the LT5520 can be easily matched for different frequencies by changing the input capacitors, C1 and C2. Table 4 lists some actual values used at selected frequencies.

Table 4. Input Capacitor Values vs Frequency

Frequency (MHz)	Capacitance (C1, C2) (pF)
70	820
140	220
240	68
480	18
650	12

The performance was evaluated with the input tuned for each of these frequencies and the results are summarized in Figures 6-8. The same IF input balun transformer was used for all measurements. In each case, the LO input frequency was adjusted to maintain an RF output frequency of 1900 MHz.

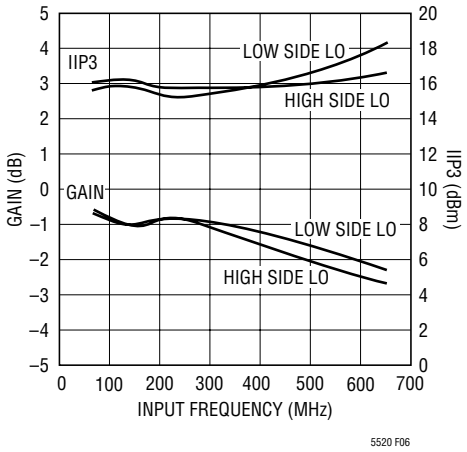


Figure 6. Conversion Gain and IIP3 vs Tuned IF Input Frequency

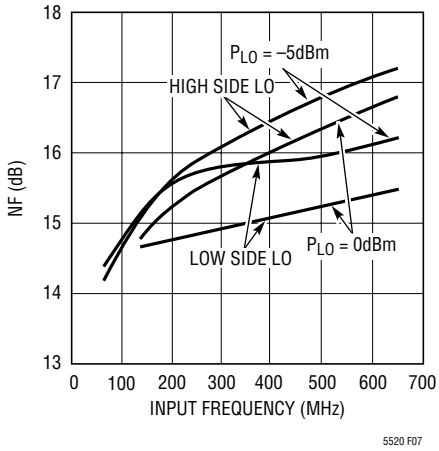


Figure 7. SSB Noise Figure vs Tuned IF Input Frequency

APPLICATIONS INFORMATION

Figures 6-8 illustrate the performance versus tuned IF input frequency with both high side and low side LO injection. Figure 6 shows the measured conversion gain and IIP3. The noise figure is plotted in Figure 7 for LO power levels of –5dBm and 0dBm. At lower input frequencies, the LO power level has little impact on noise figure. However, for higher frequencies, an increased LO drive level may be utilized to achieve better noise figure. The single-tone IIP2 behavior is illustrated in Figure 8.

Low Frequency Matching of the RF Output Port

Without any external components on the RF output, the internal transformer of the LT5520 provides a good 50Ω impedance match for RF frequencies above approximately 1600MHz. At frequencies lower than this, the return loss drops below 10dB and degrades the conversion gain. The addition of a single 3.3pF capacitor in series with the RF output improves the match at lower RF frequencies, shifting the 10dB return loss point to about 1300MHz, as demonstrated in Figure 9. This change also results in an improvement of the conversion gain, as shown in Figure 9.

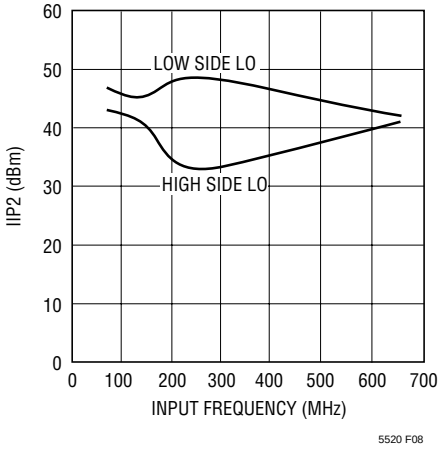


Figure 8. IIP2 vs Tuned IF Input Frequency

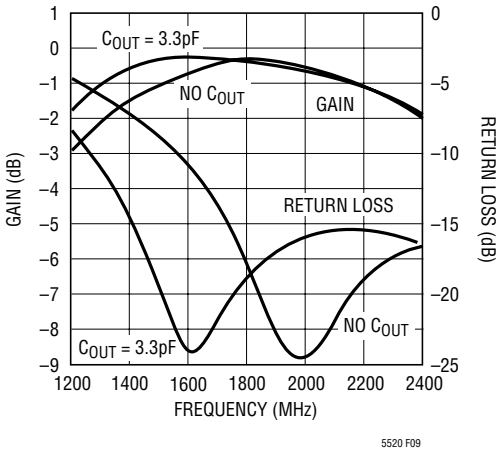
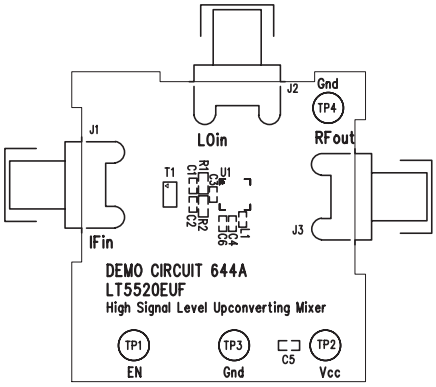
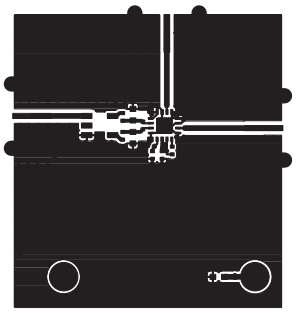


Figure 9. Conversion Gain and Return Loss vs Output Frequency

APPLICATIONS INFORMATION



(10a) Top Layer Silkscreen

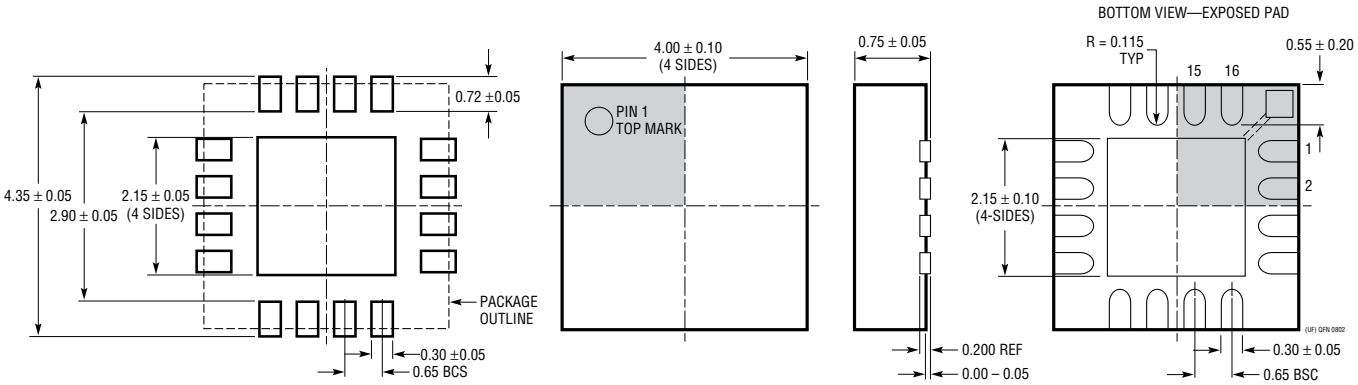


(10b) Top Layer Metal

Figure 10. Evaluation Board Layout

PACKAGE DESCRIPTION

UF Package
16-Lead Plastic QFN (4mm × 4mm)
(Reference LTC DWG # 05-08-1692)



NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGGC)
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
4. EXPOSED PAD SHALL BE SOLDER PLATED