Low Distortion IF Amplifier/ADC Driver with Digitally Controlled Gain

FEATURES

- **Output IP3 at 100MHz: 40dBm**
- **Maximum Output Power: 16dBm**
- **Bandwidth: LF to 540MHz**
- **Propagation Delay: 0.8ns**
- **Maximum Gain: 27dB**
- **Gain Control Range: 22.5dB**
- **Gain Control Step: 1.5dB**
- Gain Control Settling Time: 500ns
- Noise Figure: 8.6dB at 100MHz (Max Gain)
- Output Noise Floor: –138dBm/Hz (Max Gain)
- Reverse Isolation: –92dB
- Single Supply: 4.75V to 5.25V
- Shutdown Mode
- Enable/Disable Time: 1µs
- Differential I/O Interface
- 20-Lead TSSOP Package

APPLICATIONS

- High Linearity ADC Driver
- IF Sampling Receivers
- VGA IF Power Amplifier
- 50Ω Driver
- Instrumentation Applications

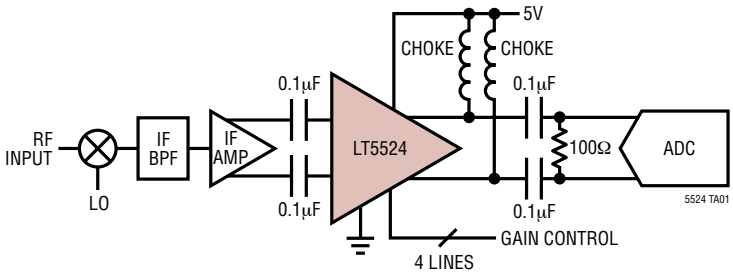
DESCRIPTION

The LT®5524 is a programmable gain amplifier (PGA) with bandwidth extending from low frequency (LF) to 540MHz. It consists of a digitally controlled variable attenuator, followed by a high linearity amplifier. Four parallel digital inputs control the gain over a 22.5dB range with 1.5dB step resolution. An on-chip power supply regulator/filter helps isolate the amplifier signal path from external noise sources.

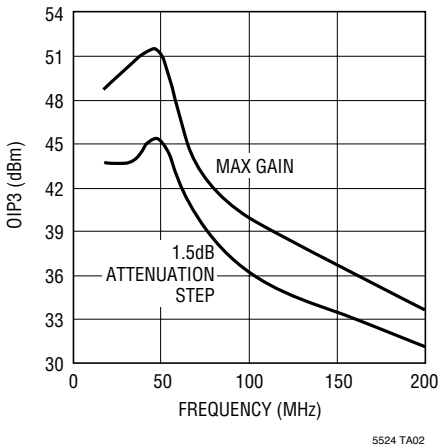
The LT5524's open-loop architecture offers stable operation for any practical load conditions, including peaking-free AC response when driving capacitive loads, and excellent reverse isolation.

The LT5524 may be operated broadband, where the output differential RC time constant sets the bandwidth, or it may be used as a narrowband driver with the appropriate output filter.

TYPICAL APPLICATION



Output IP3 vs Frequency, R_{OUT} = 200Ω

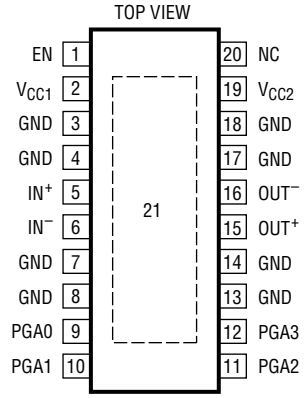


ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Power Supply Voltage (V_{CC1}, V_{CC2}) 6V
Output DC Voltage (OUT^+, OUT^-) 7V
Control Input Voltage (EN, PGAx) ..... –0.5V to V_{CC}
Signal Input Voltage (IN^+, IN^-) ..... –0.5V to 3V
Operating Ambient Temperature Range .. –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)..... 300°C

PACKAGE/ORDER INFORMATION



FE PACKAGE
20-LEAD PLASTIC TSSOP

T_{JMAX} = 150°C, θ_{JA} = 38°C/W
EXPOSED PAD (PIN 21) IS GND
MUST BE SOLDERED TO PCB

ORDER PART NUMBER
LT5524EFE

Consult LTC Marketing for parts specified with wider operating temperature ranges.

PROGRAMMABLE GAIN SETTINGS

	ATTENUATION STEP RELATIVE TO MAX GAIN	PGA0	PGA1	PGA2	PGA3	POWER GAIN*
1	0dB	High	High	High	High	27.0dB
2	–1.5dB	Low	High	High	High	25.5dB
3	–3.0dB	High	Low	High	High	24.0dB
4	–4.5dB	Low	Low	High	High	22.5dB
5	–6.0dB	High	High	Low	High	21.0dB
6	–7.5dB	Low	High	Low	High	19.5dB
7	–9.0dB	High	Low	Low	High	18.0dB
8	–10.5dB	Low	Low	Low	High	16.5dB
9	–12.0dB	High	High	High	Low	15.0dB
10	–13.5dB	Low	High	High	Low	13.5dB
11	–15.0dB	High	Low	High	Low	12.0dB
12	–16.5dB	Low	Low	High	Low	10.5dB
13	–18.0dB	High	High	Low	Low	9.0dB
14	–19.5dB	Low	High	Low	Low	7.5dB
15	–21.0dB	High	Low	Low	Low	6.0dB
16	–22.5dB	Low	Low	Low	Low	4.5dB (Note 3)

*R_{OUT} = 200Ω

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5V, V_{CCO} = 5V, EN = 3V, T_A = 25°C, unless otherwise noted. (Note 7) (Test circuits shown in Figures 9 and 10)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Normal Operating Conditions						
V_{CC}	Supply Voltage (Pins 2, 19)	(Note 4)	4.75	5	5.25	V
V_{CCO}	OUT^+, OUT^- Output Pin DC Common Mode Voltage	OUT^+, OUT^- Connected to V_{OSUP} via Choke Inductors or Resistors (Note 5)	3	5	5.5	V
Shutdown DC Characteristics, EN = 0.6V						
$V_{IN(BIAS)}$	IN^+, IN^- Bias Voltage	Max Gain (Note 6)	1.15	1.3	1.5	V
$I_{IL(PGA)}$	PGAO, PGA1, PGA2, PGA3 Input Current	V_{IN} = 0.6V			20	µA
$I_{IH(PGA)}$	PGAO, PGA1, PGA2, PGA3 Input Current	V_{IN} = 5V			20	µA
I_{OUT}	OUT^+, OUT^- Current	All Gain Settings			20	µA
I_{CC}	V_{CC} Supply Current	All Gain Settings (Note 4)		44	100	µA
Enable and PGA Inputs DC Characteristics						
V_{IL}	EN and PGAx Input Low Voltage	x = 0, 1, 2, 3			0.6	V
V_{IH}	EN and PGAx Input High Voltage	x = 0, 1, 2, 3	3			V
$I_{IL(PGA)}$	PGAO, PGA1, PGA2, PGA3 Input Current	V_{IN} = 0.6V			20	µA
$I_{IH(PGA)}$	PGAO, PGA1, PGA2, PGA3 Input Current	V_{IN} = 3V and 5V		15	30	µA
$I_{IL(EN)}$	EN Input Current	V_{IN} = 0.6V		4	20	µA
$I_{IH(EN)}$	EN Input Current	V_{IN} = 3V V_{IN} = 5V		18 38	 100	µA µA
DC Characteristics, EN = 3V						
$V_{IN(BIAS)}$	IN^+, IN^- Bias Voltage	Max Gain (Note 6)	1.34	1.48	1.65	V
R_{IN}	Input Differential Resistance	All Gain Settings (DC)		122		Ω
g_m	Amplifier Transconductance	Max Gain		0.15		S
I_{OUT}	OUT^+, OUT^- Quiescent Current	All Gain Settings, V_{OUT} = 5V	17	20	24	mA
$I_{OUT(OFFSET)}$	Output Current Mismatch	All Gain Settings, IN^+, IN^- Open		100		µA
I_{CC}	V_{CC1} + V_{CC2} Supply Current	Max Gain (Note 4) Min Gain (Note 4)		34 36	40 43	mA mA
$I_{CC(TOTAL)}$	Total Supply Current	I_{CC} + 2 • I_{OUT} (Max Gain)		75	91	mA

AC ELECTRICAL CHARACTERISTICS

V_{CC} = 5V, V_{CCO} = 5V, EN = 3V, T_A = 25°C, R_{OUT} = 200Ω. Maximum gain specifications are with respect to differential inputs and differential outputs, unless otherwise noted. (Note 7) (Test circuits shown in Figures 9 and 10)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Dynamic Performance						
BW	Large-Signal –3dB Bandwidth	All Gain Settings (Note 8), R_{OUT} = 100Ω		LF to 540		MHz
$V_{OUT(CLIP)}$	Output Voltage Clipping Levels	Each OUT+, OUT– with Respect to Ground (Note 11)	2		8	V
$P_{OUT(MAX)}$	Clipping Limited Maximum Sinusoidal Output Power	All Gain Settings, Single Tone, f_{IN} = 100MHz (Note 10)		16		dBm
g_m	Amplifier Transconductance	Max Gain, f_{IN} = 100MHz		0.15		S
S12	Reverse Isolation	f_{IN} = 100MHz (Note 9)		–92		dB
Distortion and Noise						
OIP3	Output Third Order Intercept Point for PGA0 = High (PGA1, PGA2, PGA3 Any State)	P_{OUT} = 4dBm (Each Tone), 200kHz Tone Spacing, f_{IN} = 100MHz		+40		dBm
	Output Third Order Intercept Point for PGA0 = Low (PGA1, PGA2, PGA3 Any State)	P_{OUT} = 4dBm (Each Tone), 200kHz Tone Spacing, f_{IN} = 100MHz		+36		dBm
HD2	Second Harmonic Distortion	P_{OUT} = 5dBm (Single Tone), f_{IN} = 50MHz		–76		dBc
HD3	Third Harmonic Distortion	P_{OUT} = 5dBm (Single Tone), f_{IN} = 50MHz		–72		dBc
N_{FLOOR}	Output Noise Floor (PGA0, PGA2, PGA3 Any State)	PGA1 = High, f_{IN} = 100MHz PGA1 = Low, f_{IN} = 100MHz		–138 –140		dBm/Hz dBm/Hz
NF	Noise Figure	Max Gain Setting, f_{IN} = 100MHz		8.6		dB
	PGA Settling Time	Output Settles within 10% of Final Value		500		ns
	Enable/Disable Time	Output Settles within 10% of Final Value		600		ns
Amplifier Power Gain and Gain Step						
G_{MAX}	Maximum Gain	f_{IN} = 20MHz and 200MHz		27		dB
G_{MIN}	Minimum Gain	f_{IN} = 20MHz and 200MHz		4.5		dB
G_{STEP}	Gain Step Size	f_{IN} = 20MHz and 200MHz	0.8	1.5	2.2	dB
	Gain Step Accuracy	f_{IN} = 20MHz and 200MHz		±0.2		dB
Amplifier I/O Impedance (Parallel Values, Specified Differentially)						
R_{IN}	Input Resistance	f_{IN} = 100MHz		122		Ω
C_{IN}	Input Capacitance	f_{IN} = 100MHz		2		pF
R_O	Output Resistance	f_{IN} = 100MHz		5		kΩ
C_O	Output Capacitance	f_{IN} = 100MHz		1.7		pF

Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

Note 2: All voltage values are with respect to ground.

Note 3: Default state for open PGA inputs.

Note 4: V_{CC1} and V_{CC2} (Pins 2 and 19) are internally connected.

Note 5: External V_{OSUP} is adjusted such that V_{CCO} output pin common mode voltage is as specified when resistors are used. For choke inductors or transformer, V_{OSUP} = V_{CCO} = 5V typ.

Note 6: Internally generated common mode input bias voltage requires capacitive or transformer coupling to the signal source.

Note 7: Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls. Gain always refers to power gain. Input matching is assumed. P_{IN} is the available input power. P_{OUT} is the power into the external load, R_{OUT}, as seen by the LT5524 differential outputs. All dBm figures are with respect to 50Ω.

Note 8: High frequency operation is limited by the RC time constants at the input and output ports. The low frequency (LF) roll-off is set by I/O interface choice.

Note 9: Limited by package and board isolation.

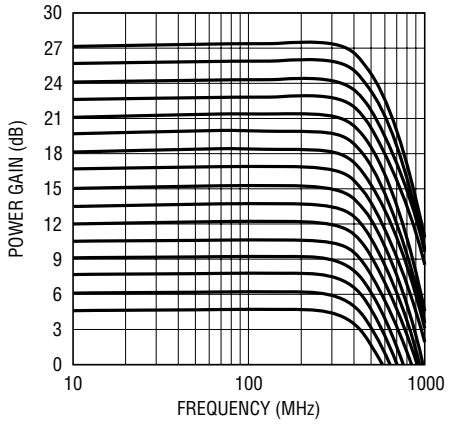
Note 10: See "Clipping Free Operation" in the Applications Information section. Refer to Figure 7.

Note 11: Although the instantaneous AC voltage on the OUT+ or OUT– pins may in some situations safely exceed 8V (with respect to ground), in no case should the DC voltage on these pins be allowed to exceed the ABSMAX tested limit of 7V.

TYPICAL PERFORMANCE CHARACTERISTICS

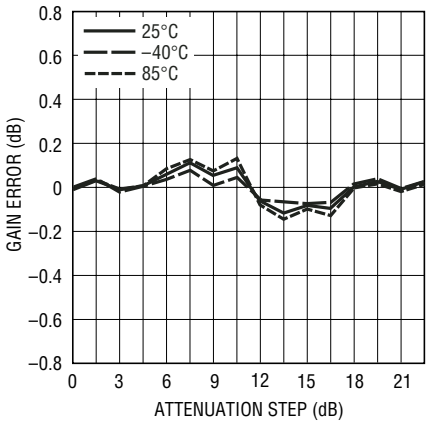
T_A = 25°C, V_{CC} = 5V, V_{CCO} = 5V, EN = 3V, control input levels V_{IL} = 0.6V, V_{IH} = 3V unless otherwise noted. (Test circuit shown in Figure 9)

Frequency Response for All Gain Steps, R_{OUT} = 200Ω



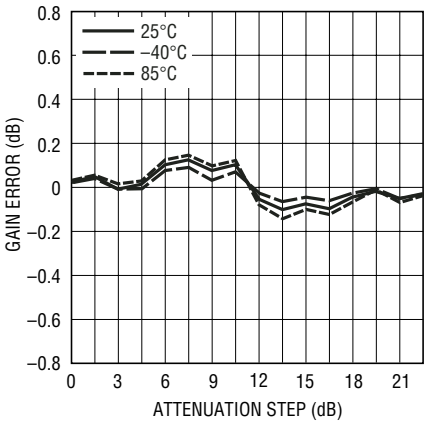
5524 G01

Gain Error vs Attenuation Step at 25MHz, R_{OUT} = 200Ω



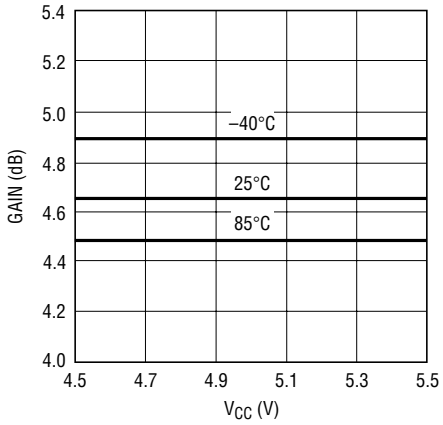
5524 G02

Gain Error vs Attenuation Step at 100MHz, R_{OUT} = 200Ω



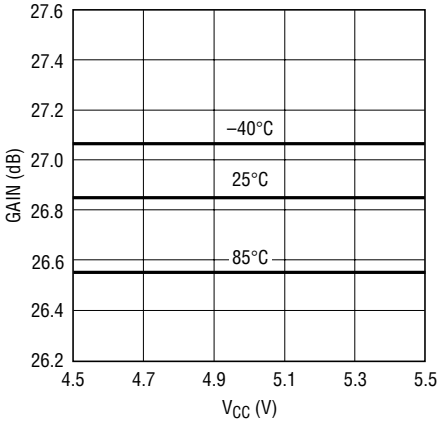
5524 G03

Minimum Gain vs V_{CC} at 120MHz, R_{OUT} = 200Ω



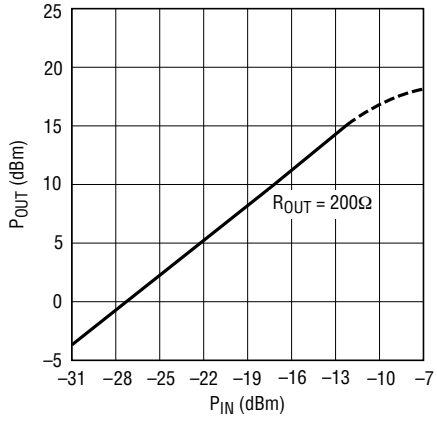
5524 G04

Maximum Gain vs V_{CC} at 120MHz, R_{OUT} = 200Ω



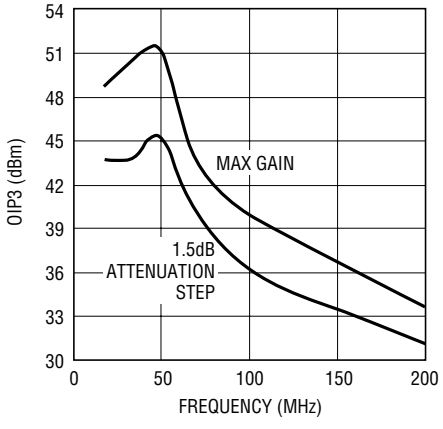
5524 G05

P_{OUT} vs P_{IN} at 50MHz, Max Gain



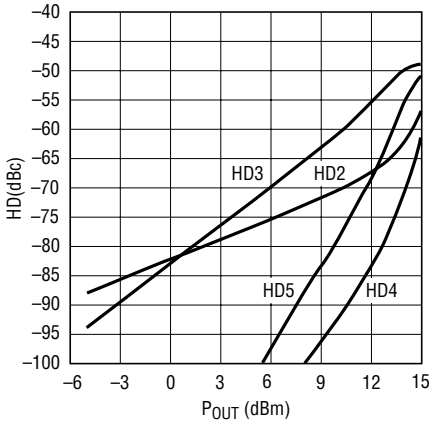
5524 G06

OIP3 vs Frequency at Pin = –23dBm, Max Gain and 1.5dB Attenuation Step, R_{OUT} = 200Ω



5524 G07

Harmonic Distortion vs P_{OUT} at 50MHz, Max Gain, R_{OUT} = 200Ω

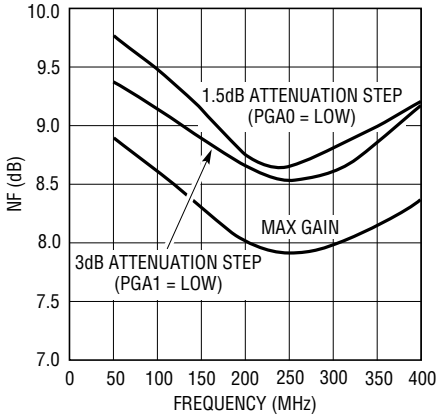


5524 G08

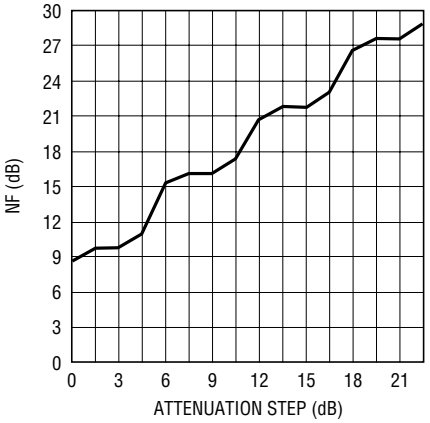
TYPICAL PERFORMANCE CHARACTERISTICS

Two tones, 200kHz spacing, T_A = 25°C, EN = 3V, V_{CC} = 5V, V_{CCO} = 5V, control input levels V_{IL} = 0.6V, V_{IH} = 3V unless otherwise noted. (Test circuit shown in Figure 10)

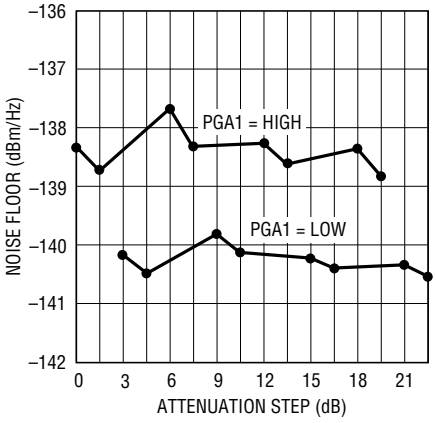
Noise Figure vs Frequency



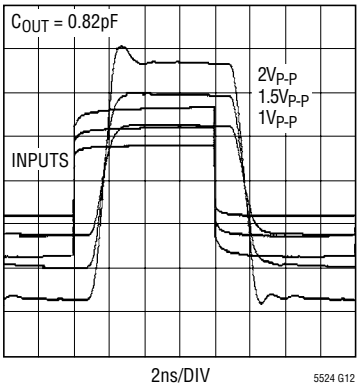
NF vs Attenuation Step at Freq = 100MHz



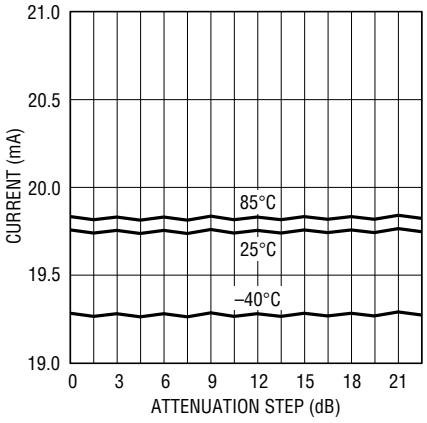
Output Noise Floor vs Attenuation Step, Freq = 100MHz, R_{OUT} = 200Ω



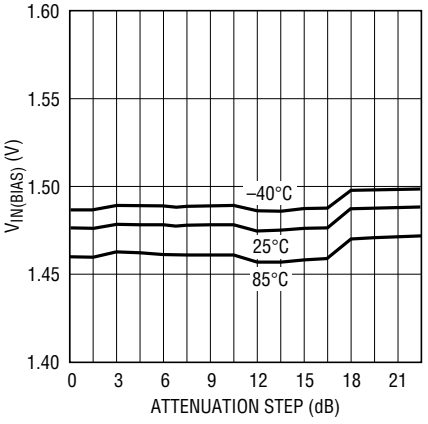
Pulse Response vs Output Level at Max Gain. Indicated Voltage Levels are into 50Ω External Load



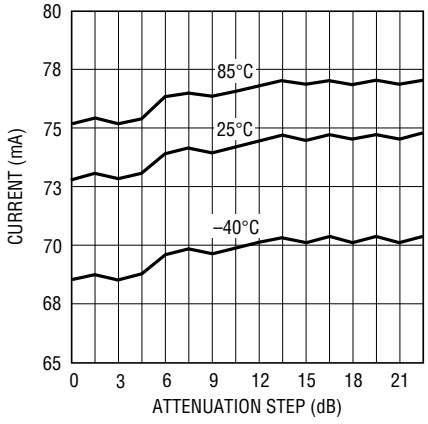
Single-Ended Output Current vs Attenuation Step



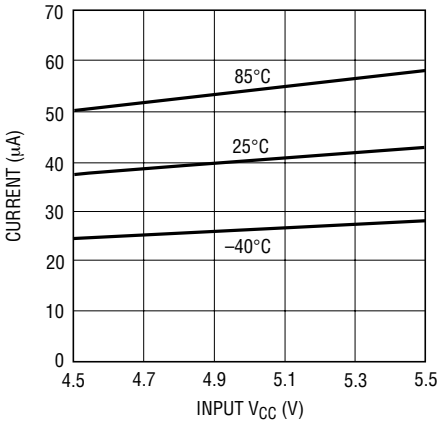
$V_{IN(BIAS)}$ vs Attenuation Step



Total I_{CC} vs Attenuation Step



I_{CC} Shutdown Current vs V_{CC}, EN = 0.6V



PIN FUNCTIONS

EN (Pin 1): Enable Pin for Amplifier. When the input voltage is higher than 3V, the amplifier is turned on. When the input voltage is less than or equal to 0.6V, the amplifier is turned off. This pin is internally pulled to ground if not connected.

V_{CC1} (Pin 2): Power Supply. This pin is internally connected to V_{CC2} (Pin 19). Decoupling capacitors (1000pF and 0.1µF for example) may be required in some applications.

GND (Pins 3, 4, 7, 8, 13, 14, 17, 18): Ground.

IN^+ (Pin 5): Positive Signal Input Pin with Internal DC Bias.

IN^- (Pin 6): Negative Signal Input Pin with Internal DC Bias.

PGA0 (Pin 9): Amplifier PGA Control Input Pin for the 1.5dB Attenuation Step (see Programmable Gain table). Input is high when the input voltage is greater than 3V. Input is low when the input voltage is less than or equal to 0.6V. This pin is internally pulled to ground if not connected.

PGA1 (Pin 10): Amplifier PGA Control Input Pin for the 3dB Attenuation Step (see Programmable Gain table). Input is high when the input voltage is greater than 3V. Input is low when the input voltage is less than or equal to 0.6V. This pin is internally pulled to ground if not connected.

PGA2 (Pin 11): Amplifier PGA Control Input Pin for the 6dB Attenuation Step (see Programmable Gain table). Input is high when the input voltage is greater than 3V. Input is low when the input voltage is less than or equal to 0.6V. This pin is internally pulled to ground if not connected.

PGA3 (Pin 12): Amplifier PGA Control Input Pin for 12dB Attenuation Step (see Programmable Gain table). Input is high when the input voltage is greater than 3V. Input is low when the input voltage is less than or equal to 0.6V. This pin is internally pulled to ground if not connected.

OUT^+ (Pin 15): Positive Amplifier Output. A transformer with center tap tied to V_{CC} or a choke inductor is recommended to source the DC quiescent current.

OUT^- (Pin 16): Negative Amplifier Output. A transformer with center tap tied to V_{CC} or a choke inductor is recommended to source the DC quiescent current.

V_{CC2} (Pin 19): Power Supply. This pin is internally connected to V_{CC1} (Pin 2).

NC (Pin 20): Not Connected.

Exposed Pad (Pin 21): Ground. This pin must be soldered to the printed circuit board ground plane for good heat transfer.

BLOCK DIAGRAM

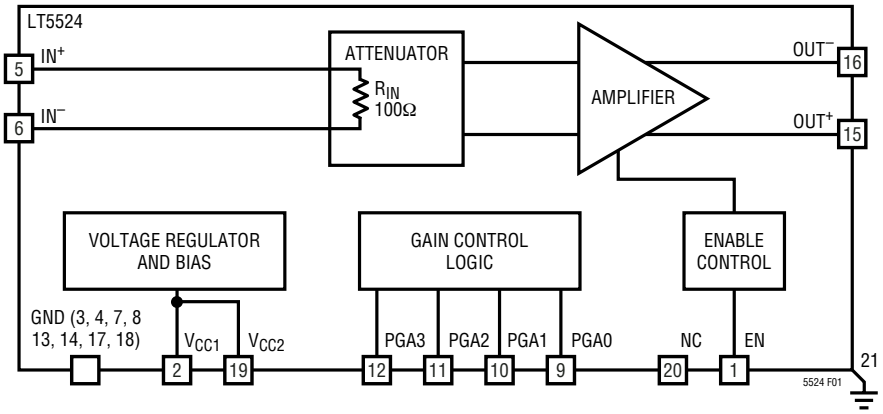


Figure 1. Functional Block Diagram

APPLICATIONS INFORMATION

Circuit Operation

The LT5524 is a high linearity amplifier with high impedance output (Figure 1). It consists of the following sections:

- An input variable attenuator "gain-control" block with 122Ω input impedance
- A differential transconductance amplifier, with enable input
- An internal bias block with internal voltage regulator
- A gain control logic block

The LT5524 amplifier provides amplification with very low distortion using a linearized open-loop architecture. In contrast with high linearity amplifiers employing negative feedback, the LT5524 offers:

- Stable operation for any practical load
- A capacitive output reactance (not inductive) that provides peaking free AC response to capacitive loads
- Exceptional reverse isolation of –100dB at 50MHz and –78dB at 300MHz (package and board leakage limited)

The LT5524 is a transconductance amplifier and its operation can be understood conceptually as consisting of two steps: First, the input signal voltage is converted to an output current. The intermodulation distortion (in dBc) of the LT5524 output current is determined by the input signal level, and is almost independent of the output load conditions. Thus, the LT5524's input IP3 is also nearly independent of the output load.

Next, the external output load (R_{OUT}) converts the output current to output voltage (or power). The LT5524's voltage and power gain both increase with increasing R_{OUT}. Accordingly, the output power and output IP3 also increase with increasing R_{OUT}. The actual output linearity performance in the application will thus be set by the choice of output load, as well as by the output network.

Maximum Gain Calculation

The maximum power gain (with the 0dB attenuation step) is:

$$G_{PWR}(dB) = 10 \bullet \log(g_m^2 \bullet R_{IN} \bullet R_{OUT})$$

where:

g_m is the LT5524 transconductance = 0.15S.

R_{IN} is the LT5524 differential input impedance ≅ 122Ω. Input impedance matching is assumed.

R_{OUT} is the external differential output impedance as seen by the LT5524's differential outputs. R_{OUT} should be distinguished from the actual load impedance, R_{LOAD}, which will typically be coupled to the LT5524 output by an impedance transformation network.

The power gain as a function of R_{OUT} is plotted in Figure 2. The ideal relationship is linear. The curved line indicates the roll-off due to the finite (noninfinite) output resistance of the LT5524.

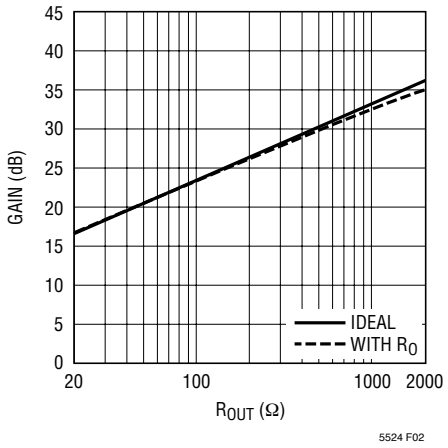


Figure 2. Power Gain as a Function of R_{OUT}

The actual available output power (as well as power gain and OIP3) will be reduced by losses in the output interface, consisting of:

- The insertion loss of the output impedance transformation network (for example the transformer insertion loss in Figure 6)
- About –3dB loss if a matching resistor (R_{MATCH} in Figure 6) is used to provide output load impedance back-matching (for example when driving transmission lines)

APPLICATIONS INFORMATION

Input Interface

For the lowest noise and highest linearity, the LT5524 should be driven with a differential input signal. Single-ended drive will severely degrade linearity and noise performance.

Example input matching networks are shown in Figures 3 and 4.

Input matching network design criteria are:

- DC block the LT5524 internal bias voltage (see Input Bias Voltage section for DC coupling information)
- Match the source impedance to the LT5524, $R_{IN} \cong 122\Omega$
- Provide well balanced differential input drive (capacitor C2 in Figure 4)
- Minimize insertion loss to avoid degrading the noise figure (NF)

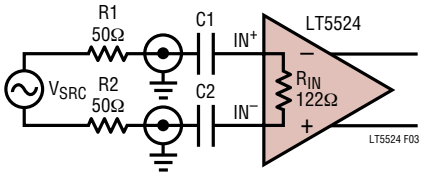


Figure 3. Input Capacitively-Coupled to a Differential Source

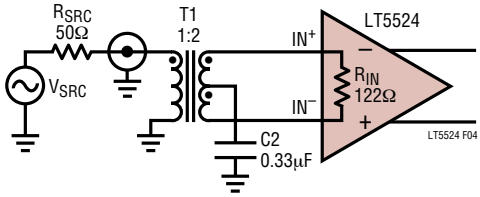


Figure 4. Input Transformer-Coupled to a Single-Ended Source

Output Interface

The output interface network provides an impedance transformation between the actual load impedance, R_{LOAD}, and the LT5524 output loading, R_{OUT}, chosen to maximize power or linearity, or to minimize output noise, or for some other criteria as explained in the following sections.

Two examples of output matching networks are shown in Figures 5 and 6 (as implemented in the LT5524 demo boards).

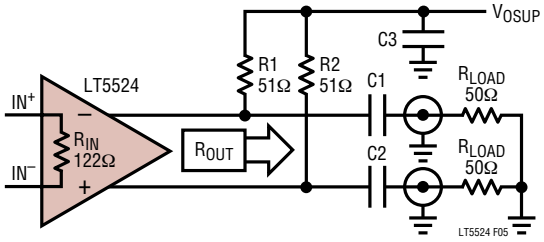


Figure 5. Output Impedance-Matched and Capacitively Coupled to a Differential Load

Note: In Figure 5, (choke) inductors may be placed in parallel with or used to replace resistors R1 and R2, thus eliminating the DC voltage drop across these resistors.

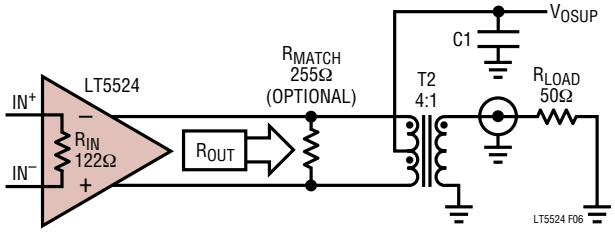


Figure 6. Output Impedance-Matched and Transformer-Coupled to a Single-Ended Load

Output network design criteria are:

- Provide DC isolation between the LT5524 DC output voltage and R_{LOAD}.
- Provide a path for the output DC current from the output voltage source V_{OSUP}.
- Provide an impedance transformation, if required, between the load impedance, R_{LOAD}, and the optimum R_{OUT} loading.
- Set the bandwidth of the output network.
- Optional: Provide board output impedance matching using resistor R_{MATCH} (when driving a transmission line).
- Use high linearity passive parts to avoid introducing nonlinearity.

Note that there is a noise penalty of up to 6dB when using power delivered by only one output in Figure 5.

APPLICATIONS INFORMATION

Clipping Free Operation

The LT5524 is a class A amplifier. To avoid signal distortion, the user must ensure that the LT5524 outputs do not enter into current or voltage limiting. The following discussion applies to maximum gain operation.

To avoid current clipping, the output signal current should not exceed the DC quiescent current, I_{OUT} = 20mA (typical). Correspondingly, the maximum input voltage, $V_{IN(MAX)}$, is I_{OUT}/g_m = 133mV (peak). In power terms, $P_{IN(MAX)}$ = –11.5dBm (assuming R_{IN} = 122Ω).

To avoid output voltage clipping (due to LT5524 output stage saturation or breakdown), the single-ended output voltage swing should stay within the specified limits; i.e., 2V ≤ V_{OUT} ≤ 8V. For a DC output bias of 5V, the maximum single ended swing will be 3Vpeak and the maximum differential swing will be 6Vpeak. The simultaneous onset of both current and voltage limiting occurs when R_{OUT} = 6Vpeak/20mA = 300Ω (typ) for a maximum P_{OUT} = 17.8dBm. This calculation applies for a sinusoidal signal. For nonsinusoidal signals, use the appropriate crest factor to calculate the actual maximum power that avoids output clipping.

Although the instantaneous AC voltage on the OUT^+ or OUT^- pins may in some situations safely exceed 8V (with respect to ground), in no case should the DC voltage on these pins be allowed to exceed the ABSMAX tested limit of 7V.

For nonoptimal R_{OUT} values, the maximum available output power will be lower and can be calculated (considering current limiting for R_{OUT} < 300Ω, and voltage limiting for R_{OUT} > 300Ω). The result of this calculation is shown in Figure 7.

The LT5524 input should not be overdriven (P_{IN} > –11.5dBm at maximum gain). The consequences of overdrive are reduced bandwidth and, when the frequency is greater than 50MHz, reduced output power. At reduced gain settings, the maximum P_{IN} is increased by an amount equal to the gain reduction.

Input Bias Voltage

The LT5524 IN^+, IN^- signal inputs are internally biased to 1.48V common mode when enabled, and to 1.26V in shutdown mode. These inputs are typically coupled by means of a capacitor or a transformer to a signal source, and impedance matching is assumed. In shutdown mode, the internal bias can handle up to 1μA leakage on the input coupling capacitors. This reduces the turn-on delay due to the input coupling RC time constant when exiting shutdown mode.

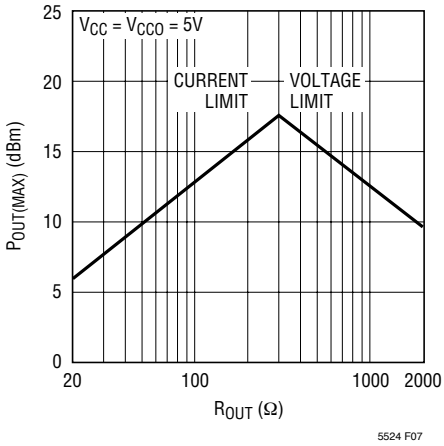


Figure 7. Maximum Output Power as a Function of R_{OUT}

If DC coupling to the input is required, the external common mode bias should track the LT5524's internal common mode level. The DC current from the LT5524 inputs should not exceed $I_{IN(SINK)}$ = –200μA and $I_{IN(SOURCE)}$ = 400μA.

Stability Considerations

The LT5524's open-loop architecture allows it to drive any practical load. Note that LT5524 gain is proportional to the load impedance, and may exceed the reverse isolation at frequencies above 1GHz if the LT5524's outputs are left unloaded, with instability as the undesirable consequence. In such cases, placing a resistive differential load (e.g., 4k) or a small capacitor at the LT5524 outputs can be used to limit the maximum gain.

The LT5524 has about 20GHz gain-bandwidth product. Hence, attention must be paid to the printed circuit board layout to avoid output pin to input pin signal coupling (the evaluation board layout is a good example). Due to the LT5524's internal power supply regulator, external supply decoupling capacitors typically are not required. Likewise, decoupling capacitors on the LT5524 control inputs typically are not needed. Note, however, that the Exposed Pad

APPLICATIONS INFORMATION

on the LT5524 package must be soldered to a good ground plane on the PCB.

PGA Function, Linearity and NF

As described in the Circuit Operation section, the LT5524 consists of a variable (step) attenuator followed by a high gain output amplifier. The overall gain of the LT5524 is digitally controlled by means of four gain control pins with internal pull-down. Minimum gain is programmed when the gain control pins are set low or left floating. In shutdown mode, these PGA inputs draw <10μA leakage current, regardless of the applied voltage.

The 6dB and 12dB attenuation steps (PGA2 and PGA3) are implemented by switching the amplifier inputs to an input attenuator tap. The 3dB attenuation step (PGA1) changes the amplifier transconductance. The output IP3 is approximately independent of the PGA1, PGA2 and PGA3 gain settings. However, the 1.5dB attenuation step utilizes a current steering technique that disables the internal linearity compensation circuit, and the OIP3 can be reduced by as much as 6dB when PGA0 is low. Therefore, to achieve the LT5524's highest linearity performance, the PGA0 pin should be set high.

The LT5524 noise figure is 8.6dB at 100MHz in the maximum gain state. For the –3dB attenuation setting, the NF is 9.2dB. The noise figure increases in direct proportion to the amount of programmed gain reduction for the 1.5dB, 6dB and 12dB steps.

The output noise floor is proportional to the output load impedance, R_{OUT}. It is almost constant for PGA1 = high and for any PGA0, PGA2, PGA3 state. When PGA1 = low, the output noise floor is 2dB lower (see Typical Performance Characteristics).

Other Linearity Considerations

LT5524 linearity is a strong function of signal frequency. OIP3 decreases about 13dB for every octave of frequency increase above 100MHz.

As noted in the Circuit Operation section, at any given frequency and input level, the LT5524 provides a current output with fairly constant intermodulation distortion figure in dBc, regardless of the output load value. For higher R_{OUT} values, more gain and output power is available, and better OIP3 figures can be achieved. However, high R_{OUT} values are not easily implemented in practice, limited by the availability of high ratio output impedance transformation networks.

Linearity can also be limited by the output RC time constant (bandwidth limitations), particularly for high R_{OUT} values. A solution is outlined in the Bandpass Applications section.

The LT5524 linearity degrades when common mode signal is present. The input transformer center tap should be decoupled to ground to provide a balanced input differential signal and to avoid linearity degradation for high attenuation steps. When the signal frequency is lower than 50MHz, and there is significant common mode signal, then high attenuation settings may result in degraded linearity.

At signal frequencies below 100MHz, the LT5524's internal linearity compensation circuitry may provide "sweet spots" with very high OIP3, in excess of +52dBm. This almost perfect distortion correction cannot be sustained over the full operating temperature range and with variations of the LT5524 output load (complex impedance Z_{OUT}). Users are advised to rely on data shown in the Typical Performance Characteristics curves to estimate the dependable linearity performance.

Wideband Applications

At low frequencies, the value of the decoupling capacitors, choke inductors and choice of transformer will set the minimum frequency of operation. Output DC coupling is possible, but this typically reduces the LT5524's output DC bias voltage, and thus the output swing and available power.

At high frequencies, the output RC time constants set an upper limit to the maximum frequency of operation in the case of the wideband output networks presented so far. For example the LT5524 output capacitance, C_{OUT} = 1.7pF, and a pure resistive load, R_{OUT} = 200Ω, will set the –3dB bandwidth to about 400MHz. In an actual application, the $R_{LOAD} \bullet C_{LOAD}$ product may be even more restrictive. The use of wideband output networks will not only limit the

APPLICATIONS INFORMATION

bandwidth, but will also degrade linearity because part of the available power is wasted driving the capacitive load.

The LT5524's output reactance is capacitive. Therefore improved AC response is possible by using external series output inductors. When driving purely resistive loads, an inductor in series with the LT5524 output may help to achieve maximally flat AC response as exemplified in the characterization setup schematic (Figure 9).

The series inductor can extend the application bandwidth, but it provides no improvement in linearity performance.

Series inductance may also produce peaking in the AC response. This can be the case when (high Q) choke inductors are used in an output interface such as in Figure 5, and the PCB trace (connection) to the load is too long. Since the LT5524's output impedance is relatively high, the PCB trace acts as a series inductor. The most direct solution is to shorten the connection lines by placing the driver closer to the load. Another solution to flatten the AC response is to place resistance close to the LT5524 outputs. In this way the connection line behaves more like a terminated transmission line, and the AC peaking due to the capacitive load can be removed.

Bandpass Applications

For narrow band IF applications, the LT5524's output capacitance and the application load capacitance can be incorporated as part of an LC impedance transformation network, giving improved linearity performance for signal frequencies greater than 100MHz. Figure 8 is an example of such a network.

The network consists of two parallel resonant LC tank circuits critically coupled by capacitors C1 and C2. The R_{OUT} to R_{LOAD} transformation ratio in this particular implementation is 2. The choice of impedance transformation ratio is more flexible than in the wideband case. The LC network is a bandpass filter, a useful feature in many applications.

A variety of bandpass matching network configurations are conceivable, depending on the requirements of the particular application. The design of these networks is facilitated by the fact that the LT5524 outputs are not destabilized by reactive loading.

Note that these LC networks may distort the output signal if their amplitude and phase response exhibit nonlinear behavior. For example, if resistors R1 and R2 in Figure 5 are replaced with LC resonant tank circuits, then severe OIP3 degradation may occur.

Low Output Noise Floor Applications

In some applications the maximum output noise floor is specified. The LT5524 output noise floor is elevated above the available noise power (–174dBm/Hz into 50Ω) by the NF + Gain. Consequently, reduction of the LT5524's power gain is the only way to reduce the output noise floor.

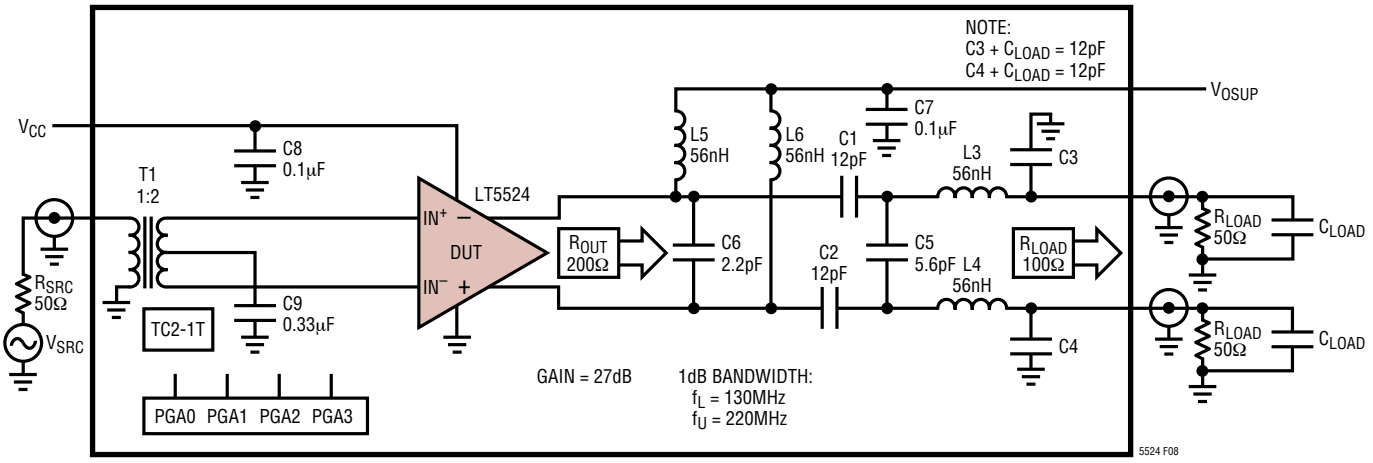


Figure 8. Bandpass Output Transformation Network Example

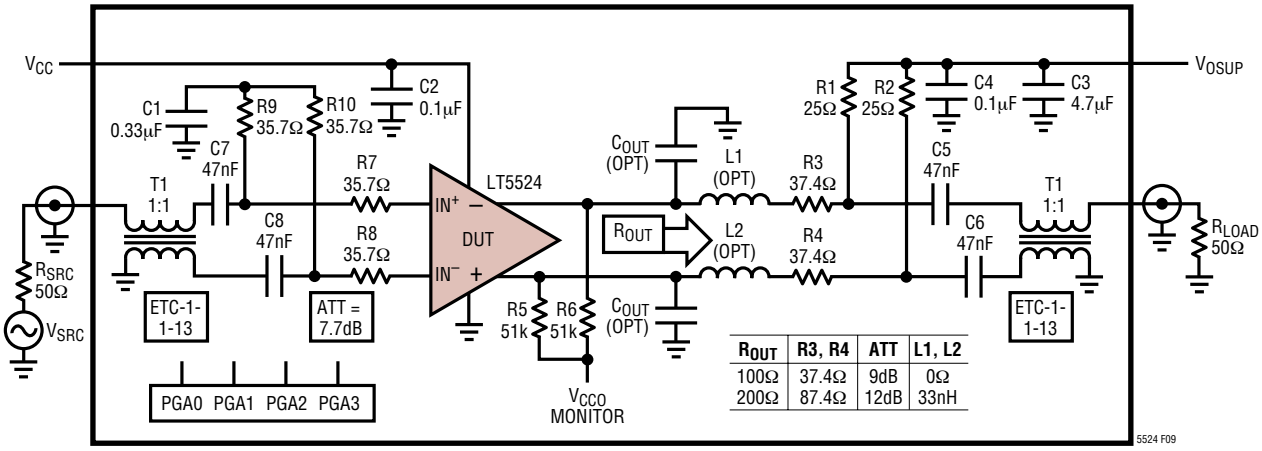
APPLICATIONS INFORMATION

In fixed gain applications, the LT5524 can be set to 3dB attenuation relative to maximum gain. As shown in the Typical Performance Characteristics, this gives a 2dB reduction in the output noise floor with no loss of linearity.

In general, the output noise floor can be reduced by decreasing R_{OUT} (and hence power gain), at the cost of reduced OIP3.

LT5524 Characterization

The LT5524's typical performance data are based on the test circuits shown in Figures 9 and 10. Figure 9 does not necessarily reflect the use of the LT5524 in an actual application. (For that, see the Application Boards section.) Rather, it represents a compromise that most accurately measures the actual operation of the part by itself, undistorted by the artifacts of the impedance transformation network, or by external bandwidth limiting factors. Balun transformers are used to interface with single-ended test equipment. Input and output resistive attenuators (not shown) provide broadband I/O impedance control. The L1, L2 inductors are selected for maximally flat AC output response. C_{OUT} (normally open) shows the placement of capacitive loading when this is specified as a characterization variable. The V_{CCO} monitor pin allows setting the output DC level (5V typical) by adjusting voltage V_{OSUP}.



ROUT	R3, R4	ATT	L1, L2
100Ω	37.4Ω	9dB	0Ω
200Ω	87.4Ω	12dB	33nH

Figure 9. Characterization Board (Simplified Schematic)

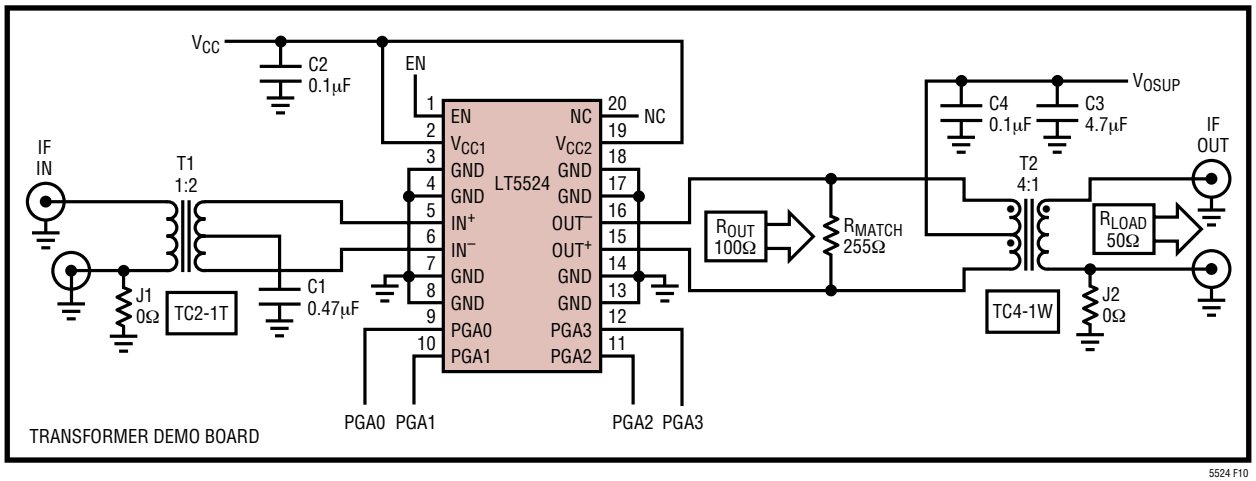


Figure 10. Output Transformer Application Board (Simplified Schematic)

APPLICATIONS INFORMATION

Application (Demo) Boards

The LT5524 demo boards are provided in the versions shown in Figure 10 (with output transformer) and Figure 11 (without output transformer). All I/O signal ports are matched to 50Ω. Moreover, 40k resistors (not shown) connect all five control pins (EN, PGA0, PGA1, PGA2, PGA3) to V_{CC}, such that the LT5524 is shipped in maximum gain state.

The gain setting can be changed by connecting the control pins to ground. Test points (TP1, TP2, TP3) are provided to monitor the input and output DC bias voltage. Jumper J1 can be removed when differential input is desired, but in that case, T1 should be changed to a 1:1 center-tap transformer to preserve 50Ω input matching. The demo board is shipped with optional output back-matching resistor R_{MATCH} = 255Ω. This results in a net output load, R_{OUT} = 100Ω, presented to the LT5524.

The Output Transformer Application Board (Figure 10) is one example of an output impedance transformation (T2 transformer). For the Typical Performance Characteristics curves, all linearity tests are performed on this board. By removing R_{MATCH}, the performance with R_{OUT} = 200Ω can be evaluated (provided the lack of impedance back-matching is suitably remedied).

The transformer board can provide a differential output when Jumper J2 is removed.

The Wideband Differential Output Application Board (Figure 11) is an example of direct coupling (no transformer) to the load, and has wider output bandwidth. This board gives direct access to the LT5524's output pins, and was used for stability tests. Higher V_{OSUP} (6.5V) is required to compensate for the DC voltage drop on R1 and R2. Use TP2, TP3 to monitor the actual LT5524 output bias voltage. By replacing R1 and R2 with inductors, this board can operate with a 5V supply. However, this may limit the minimum signal frequency. For example, an 820nH choke inductor will limit the lowest signal frequency to 40MHz.

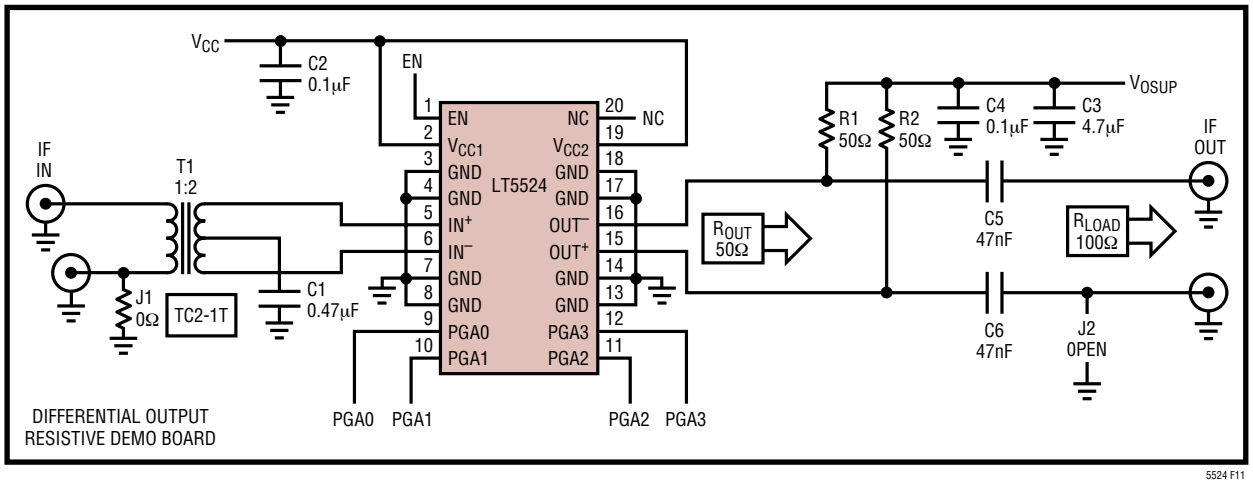
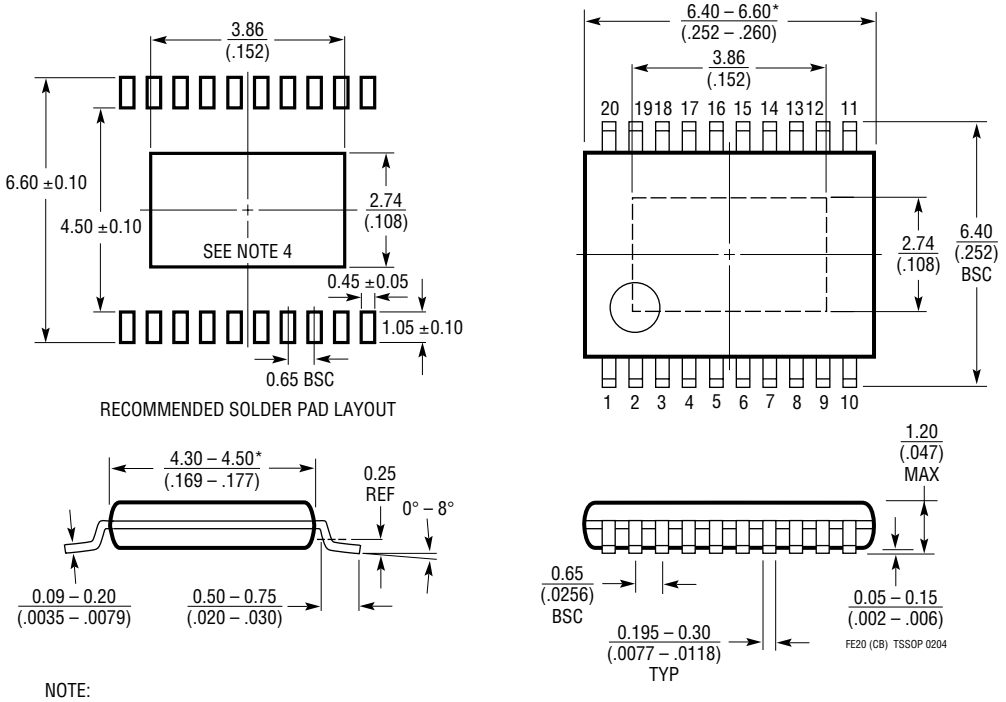


Figure 11. Wideband Differential Output Application Board (Simplified Schematic)

PACKAGE DESCRIPTION

FE Package
20-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1663)
Exposed Pad Variation CB



NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{(\text{INCHES})}$
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT

*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE