High Linearity, Low Power Downconverting Mixer

FEATURES

- **Operation up to 2GHz**
- **Broadband RF, LO and IF Operation**
- **High Input IP3: +16.5dBm at 900MHz**
- **Typical Conversion Gain: 0.6dB at 900MHz**
- **SSB Noise Figure: 11dB at 900MHz**
- **On-Chip 50Ω LO Match**
- **Integrated LO Buffer: –5dBm Drive Level**
- **High LO-RF and LO-IF Isolation**
- Low Supply Current: 28mA Typ
- Enable Function
- Single 5V Supply
- 16-Lead QFN (4mm × 4mm) Package

APPLICATIONS

- Point-to-Point Data Communication Systems
- Wireless Infrastructure
- Cable Downlink Infrastructure
- High Linearity Receiver Applications

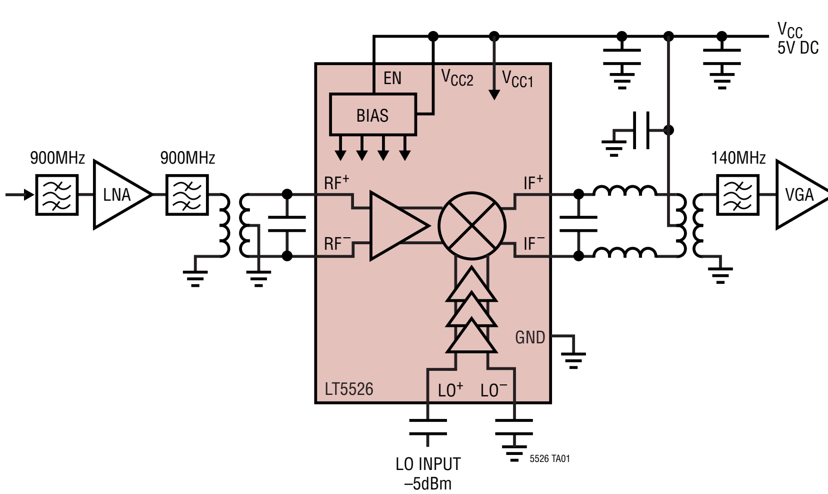
DESCRIPTION

The LT®5526 is a low power broadband mixer optimized for high linearity applications such as point-to-point data transmission, cable infrastructure and wireless infrastructure systems. The device includes an internally matched high speed LO amplifier driving a double-balanced active mixer core. An integrated RF buffer amplifier provides excellent LO-RF isolation. The RF and IF ports can be easily matched across a broad range of frequencies for use in a wide variety of applications.

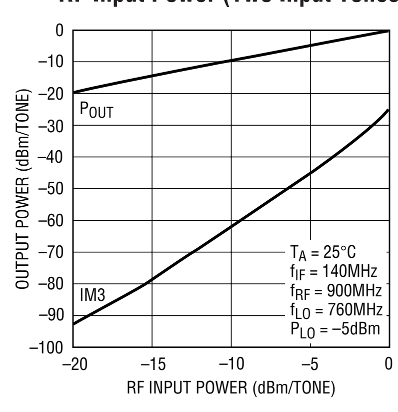
The LT5526 offers a high performance alternative to passive mixers. Unlike passive mixers which have conversion loss and require high LO drive levels, the LT5526 delivers conversion gain at significantly lower LO input levels and is much less sensitive to LO power level variations.

TYPICAL APPLICATION

High Signal Level Frequency Downconversion



IF Output Power and IM3 vs RF Input Power (Two Input Tones)



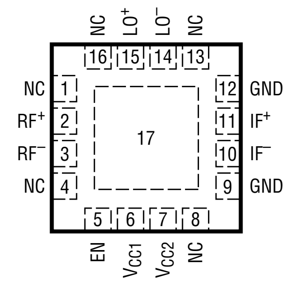
ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage 5.5V
Enable Voltage .... –0.3V to V_{CC} + 0.3V
LO Input Power .... +10dBm
LO+ to LO– Differential DC Voltage .... ±1V
RF Input Power .... +10dBm
RF+ to RF– Differential DC Voltage .... ±0.7V
Operating Temperature Range .... –40°C to 85°C
Storage Temperature Range .... –65°C to 125°C
Junction Temperature (T_J) .... 125°C

PACKAGE/ORDER INFORMATION

TOP VIEW



UF PACKAGE
16-LEAD (4mm × 4mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JA} = 37°C/W
EXPOSED PAD (PIN 17) IS GND,
MUST BE SOLDERED TO PCB.
NC PINS SHOULD BE GROUNDED

ORDER PART NUMBER	UF PART MARKING
LT5526EUF	5526

Consult LTC Marketing for parts specified with wider operating temperature ranges.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5V, EN = 3V, T_A = 25°C (Note 3), unless otherwise noted. Test circuit shown in Figure 1.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Requirements (V_{CC})					
Supply Voltage		3.6	5	5.3	V
Supply Current	V_{CC} = 5V		28	33	mA
Shutdown Current	EN = Low			100	μA
Enable (EN) Low = Off, High = On					
EN Input High Voltage (On)		3			V
EN Input Low Voltage (Off)				0.3	V
Enable Pin Input Current	EN = 5V EN = 0V		55 0.01		μA μA
Turn-On Time (Note 5)			3		μs
Turn-Off Time (Note 5)			6		μs

AC ELECTRICAL CHARACTERISTICS (Notes 2, 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
RF Input Frequency Range (Note 4)	Requires RF Matching		0.1 to 2000		MHz
LO Input Frequency Range (Note 4)	Requires DC Blocks		0.1 to 2500		MHz
IF Output Frequency Range (Note 4)	Requires IF Matching		0.1 to 1000		MHz

V_{CC} = 5V, EN = 3V, T_A = 25°C. Test circuits shown in Figures 1 and 2. (Notes 2, 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
RF Input Return Loss	Z_0 = 50Ω, External Match		15		dB
LO Input Return Loss	Z_0 = 50Ω, External DC Blocks		15		dB
IF Output Return Loss	Z_0 = 50Ω, External Match		15		dB
LO Input Power			–10 to 0		dBm

AC ELECTRICAL CHARACTERISTICS

V_{CC} = 5V, EN = 3V, T_A = 25°C, P_{RF} = –15dBm (–15dBm/tone for 2-tone IIP3 tests, ∆f = 1MHz), P_{LO} = –5dBm, unless otherwise noted. Test circuits shown in Figures 1 and 2. (Notes 2, 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
RF to LO Isolation	f_{RF} = 350MHz, f_{IF} = 70MHz, f_{LO} = 420MHz f_{RF} = 900MHz, f_{IF} = 140MHz, f_{LO} = 760MHz f_{RF} = 1900MHz, f_{IF} = 140MHz, f_{LO} = 1760MHz		69 55 50		dB dB dB
Conversion Gain	f_{RF} = 350MHz, f_{IF} = 70MHz, f_{LO} = 420MHz f_{RF} = 900MHz, f_{IF} = 140MHz, f_{LO} = 760MHz f_{RF} = 1900MHz, f_{IF} = 140MHz, f_{LO} = 1760MHz		0.6 0.6 0.4		dB dB dB
Conversion Gain vs Temperature	T_A = –40°C to 85°C		–0.013		dB/°C
Input 3rd Order Intercept	f_{RF} = 350MHz, f_{IF} = 70MHz, f_{LO} = 420MHz f_{RF} = 900MHz, f_{IF} = 140MHz, f_{LO} = 760MHz f_{RF} = 1900MHz, f_{IF} = 140MHz, f_{LO} = 1760MHz		15.2 16.5 14.1		dBm dBm dBm
Single Sideband Noise Figure	f_{RF} = 350MHz, f_{IF} = 70MHz, f_{LO} = 420MHz f_{RF} = 900MHz, f_{IF} = 140MHz, f_{LO} = 760MHz f_{RF} = 1900MHz, f_{IF} = 140MHz, f_{LO} = 1760MHz		12.7 11.0 13.7		dB dB dB
LO to RF Leakage	f_{RF} = 350MHz, f_{IF} = 70MHz, f_{LO} = 420MHz f_{RF} = 900MHz, f_{IF} = 140MHz, f_{LO} = 760MHz f_{RF} = 1900MHz, f_{IF} = 140MHz, f_{LO} = 1760MHz		–65 –65 –55		dBm dBm dBm
LO to IF Leakage	f_{RF} = 350MHz, f_{IF} = 70MHz, f_{LO} = 420MHz f_{RF} = 900MHz, f_{IF} = 140MHz, f_{LO} = 760MHz f_{RF} = 1900MHz, f_{IF} = 140MHz, f_{LO} = 1760MHz		–56 –74 –37		dBm dBm dBm
2RF-2LO Output Spurious Product (f_{RF} = f_{LO} ± f_{IF}/2)	350MHz: f_{RF} = 385MHz at –15dBm, f_{LO} = 420MHz 900MHZ: f_{RF} = 830MHz at –15dBm, f_{LO} = 760MHz 1900MHz: f_{RF} = 1830MHz at –15dBm, f_{LO} = 1760MHz		–75 –72 –48		dBc dBc dBc
3RF-3LO Output Spurious Product (f_{RF} = f_{LO} ± f_{IF}/3)	350MHz: f_{RF} = 396.67MHz at –15dBm, f_{LO} = 420MHz 900MHZ: f_{RF} = 806.67MHz at –15dBm, f_{LO} = 760MHz 1900MHz: f_{RF} = 1806.67MHz at –15dBm, f_{LO} = 1760MHz		–65 –68 –56		dBc dBc dBc
Input 1dB Compression	f_{RF} = 350MHz, f_{IF} = 70MHz, f_{LO} = 420MHz f_{RF} = 900MHz, f_{IF} = 140MHz, f_{LO} = 760MHz f_{RF} = 1900MHz, f_{IF} = 140MHz, f_{LO} = 1760MHz		5 5 1		dBm dBm dBm

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: The 900MHz and 1900MHz performance is measured with the test circuit shown in Figure 1. The 350MHz performance is measured using the test circuit in Figure 2.

Note 3: Specifications over the –40°C to 85°C temperature range are assured by design, characterization and correlation with statistical process controls.

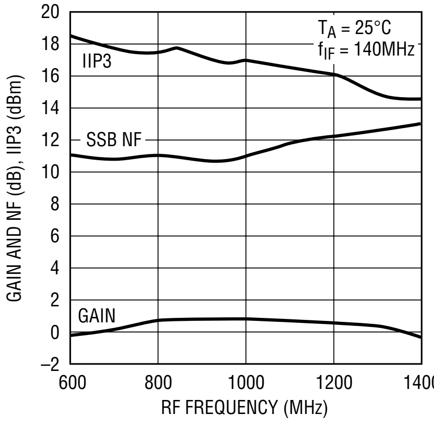
Note 4: Operation over a wider frequency range is possible with reduced performance. Consult the factory for information and assistance.

Note 5: Turn-on and turn-off times correspond to a change in the output level by 40dB.

TYPICAL AC PERFORMANCE CHARACTERISTICS

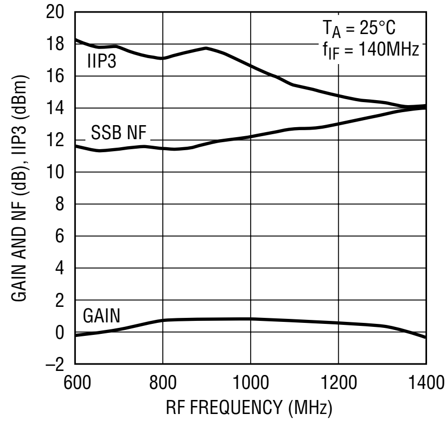
900MHz Application. V_{CC} = 5V, EN = 3V, T_A = 25°C, P_{RF} = –15dB (–15dBm/tone for 2-tone IIP3 tests, Δf = 1MHz), f_{LO} = f_{RF} – 140MHz, P_{LO} = –5dBm, IF output measured at 140MHz, unless otherwise noted. Test circuit shown in Figure 1.

Conversion Gain, IIP3 and SSB NF vs RF Frequency (Low Side LO)



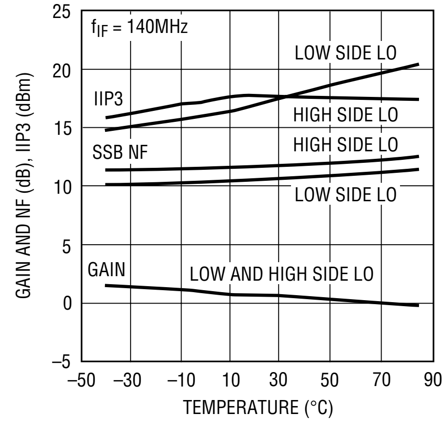
5526 G01

Conversion Gain, IIP3 and SSB NF vs RF Frequency (High Side LO)



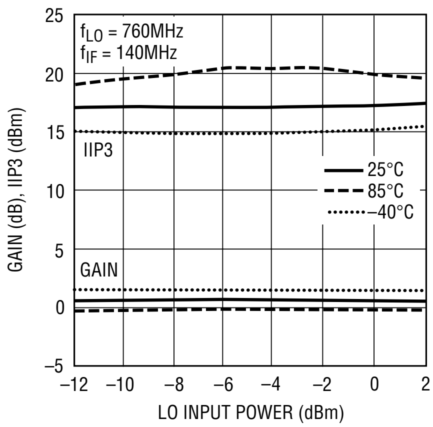
5526 G02

Conversion Gain, IIP3 and SSB NF vs Temperature



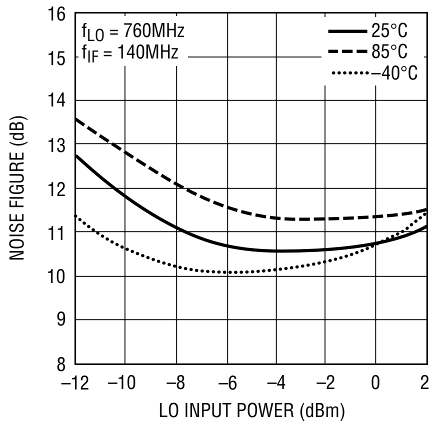
5526 G03

Conversion Gain and IIP3 vs LO Input Power



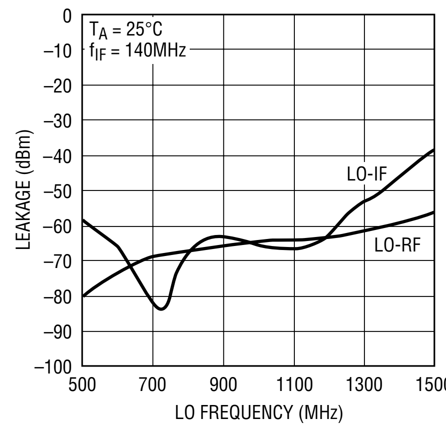
5526 G04

SSB Noise Figure vs LO Input Power



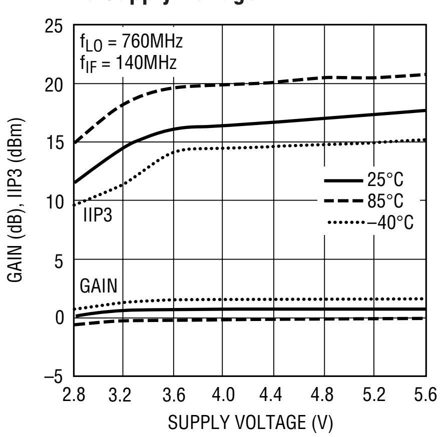
5526 G05

LO-IF and LO-RF Leakage vs LO Input Frequency



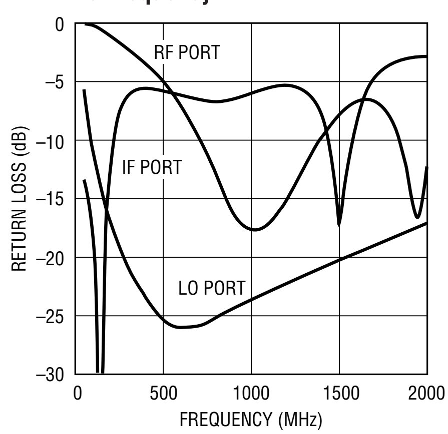
5526 G06

Conversion Gain and IIP3 vs Supply Voltage



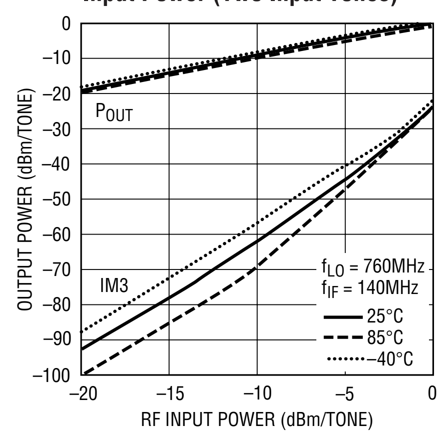
5526 G07

RF, LO and IF Port Return Loss vs Frequency



5526 G08

IF Output Power and IM3 vs RF Input Power (Two Input Tones)

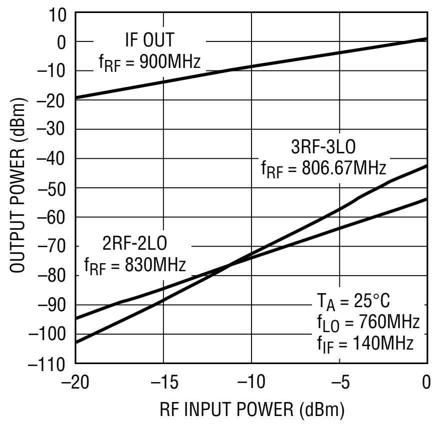


5526 G09

TYPICAL AC PERFORMANCE CHARACTERISTICS

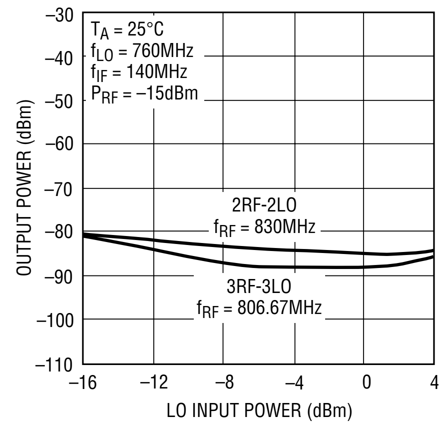
900MHz Application. V_{CC} = 5V, EN = 3V, T_A = 25°C, P_{RF} = –15dB (–15dBm/tone for 2-tone IIP3 tests, Δf = 1MHz), f_{LO} = f_{RF} – 140MHz, P_{LO} = –5dBm, IF output measured at 140MHz, unless otherwise noted. Test circuit shown in Figure 1.

IF_{OUT}, 2 × 2 and 3 × 3 Spurs vs RF Input Power



5526 G10

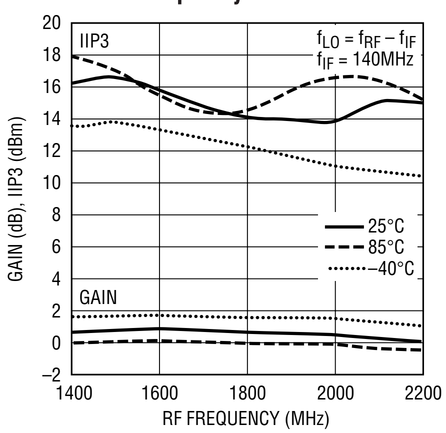
2 × 2 and 3 × 3 Spurs vs LO Input Power



5526 G11

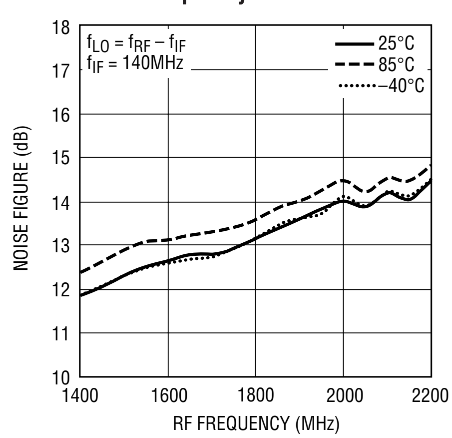
1900MHz Application. V_{CC} = 5V, EN = 3V, T_A = 25°C, P_{RF} = –15dB (–15dBm/tone for 2-tone IIP3 tests, Δf = 1MHz), f_{LO} = f_{RF} – 140MHz, P_{LO} = –5dBm, IF output measured at 140MHz, unless otherwise noted. Test circuit shown in Figure 1.

Conversion Gain and IIP3 vs RF Frequency



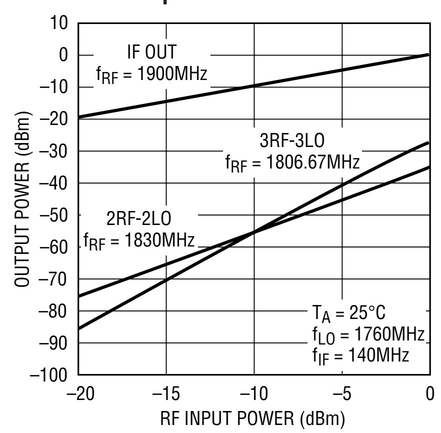
5526 G12

SSB Noise Figure vs RF Frequency



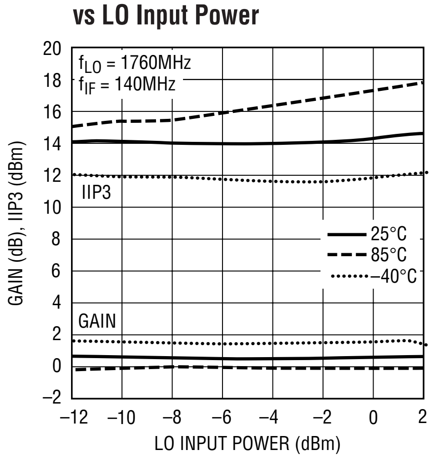
5526 G13

IF_{OUT}, 2 × 2 and 3 × 3 Spurs vs RF Input Power



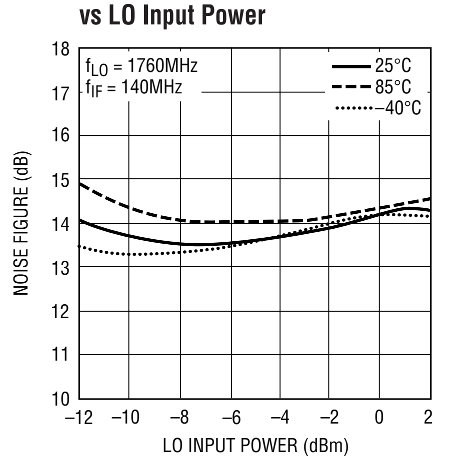
5526 G14

Conversion Gain and IIP3 vs LO Input Power



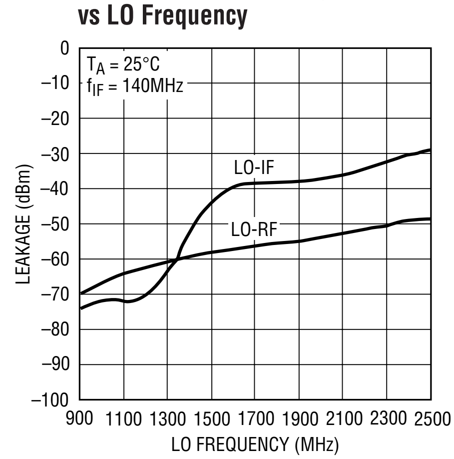
5526 G15

SSB Noise Figure vs LO Input Power



5526 G16

LO-IF and LO-RF Leakage vs LO Frequency

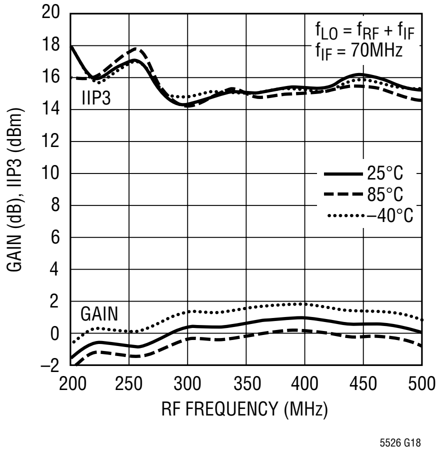


5526 G17

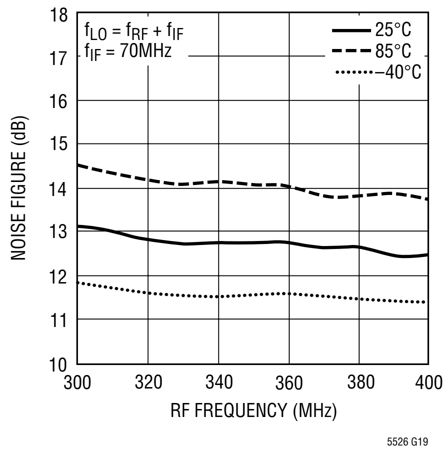
TYPICAL AC PERFORMANCE CHARACTERISTICS

350MHz Application. V_{CC} = 5V, EN = 3V, T_A = 25°C, P_{RF} = –15dB (–15dBm/tone for 2-tone IIP3 tests, Δf = 1MHz), f_{LO} = f_{RF} + 70MHz, P_{LO} = –5dBm, IF output measured at 70MHz, unless otherwise noted. Test circuit shown in Figure 2.

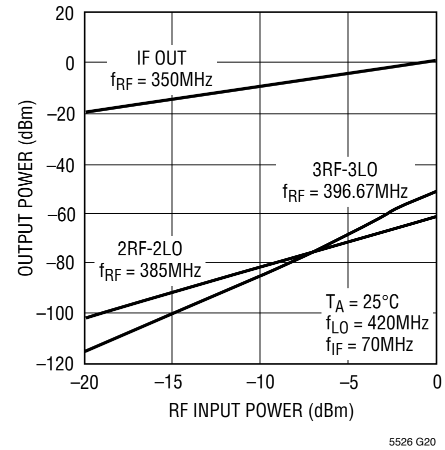
Conversion Gain and IIP3 vs RF Frequency



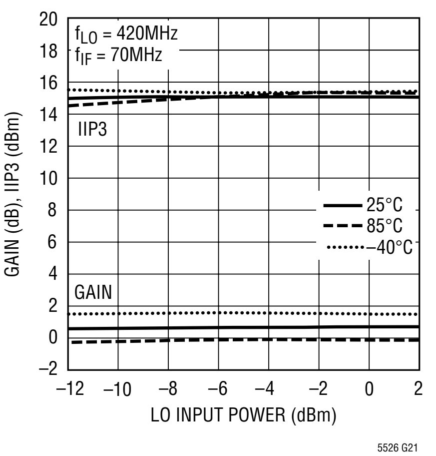
SSB Noise Figure vs RF Frequency



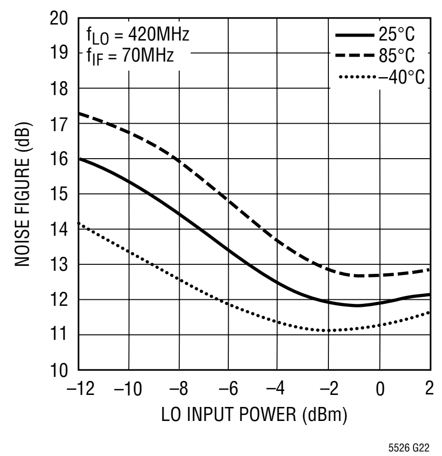
IF_{OUT}, 2 × 2 and 3 × 3 Spurs vs RF Input Power



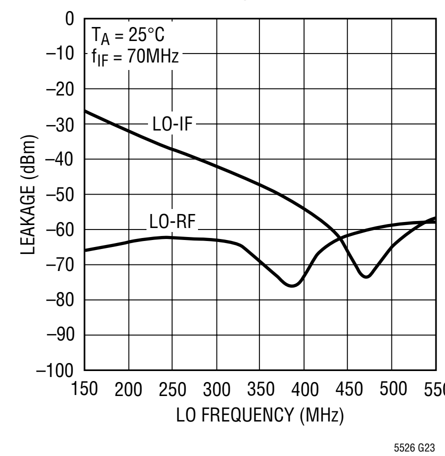
Conversion Gain and IIP3 vs LO Input Power



SSB Noise Figure vs LO Input Power



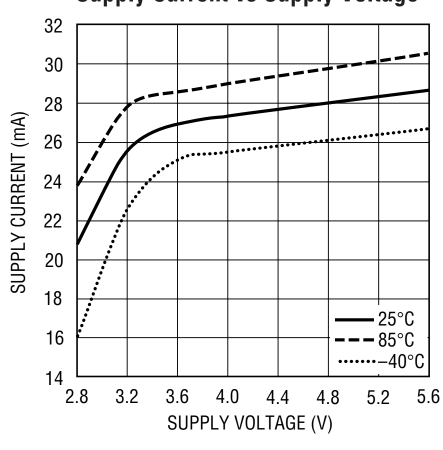
LO-IF and LO-RF Leakage vs LO Frequency



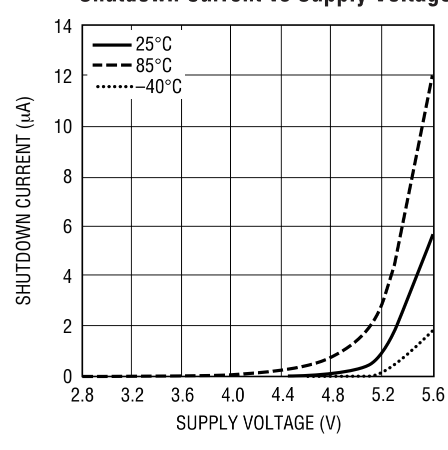
TYPICAL DC PERFORMANCE CHARACTERISTICS

Test circuit shown in Figure 1.

Supply Current vs Supply Voltage



Shutdown Current vs Supply Voltage



PIN FUNCTIONS

NC (Pins 1, 4, 8, 13, 16): Not Connected Internally. These pins should be grounded on the circuit board for improved LO-to-RF and LO-to-IF isolation.

RF$^+$, RF$^-$ (Pins 2, 3): Differential Inputs for the RF Signal. These pins must be driven with a differential signal. Each pin must also be connected to a DC ground capable of sinking 7.5mA (15mA total). This DC bias return can be accomplished through the center-tap of a balun or with shunt inductors. An impedance transformation is required to match the RF input to 50Ω (or 75Ω).

EN (Pin 5): Enable Pin. When the input voltage is higher than 3V, the mixer circuits supplied through Pins 6, 7, 10 and 11 are enabled. When the input voltage is less than 0.3V, all circuits are disabled. Typical enable pin input current is 55μA for EN = 5V and 0.01μA when EN = 0V.

V_{CC1} (Pin 6): Power Supply Pin for the LO Buffer Circuits. Typical current consumption is 11mA. This pin should be externally connected to the other V_{CC} pins and decoupled with 100pF and 0.01μF capacitors.

V_{CC2} (Pin 7): Power Supply Pin for the Bias Circuits. Typical current consumption is 2.5mA. This pin should be externally connected to the other V_{CC} pins and decoupled with 100pF and 0.01μF capacitors.

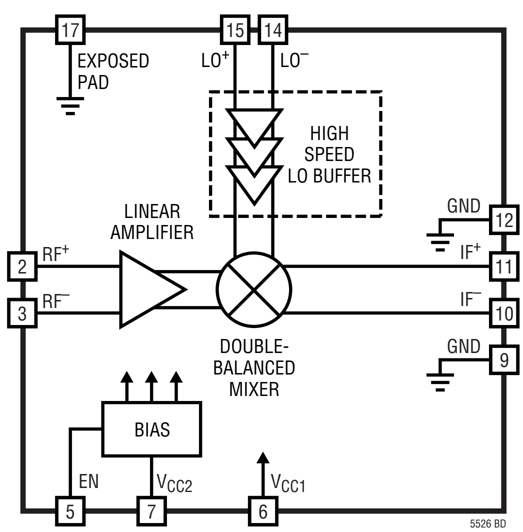
GND (Pins 9, 12): Ground. These pins are internally connected to the Exposed Pad for better isolation. They should be connected to ground on the circuit board, though they are not intended to replace the primary grounding through the Exposed Pad of the package.

IF$^-$ and IF$^+$ (Pins 10, 11): Differential Outputs for the IF Signal. An impedance transformation may be required to match the outputs. These pins must be connected to V_{CC} through impedance matching inductors, RF chokes or a transformer center-tap.

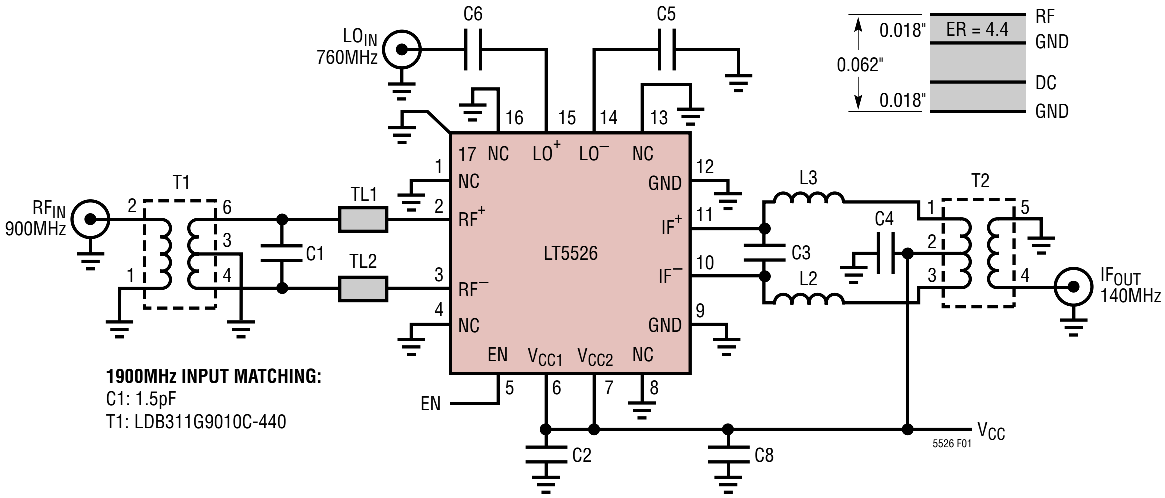
LO$^-$, LO$^+$ (Pins 14, 15): Differential Inputs for the Local Oscillator Signal. The LO input is internally matched to 50Ω; however, external DC blocking capacitors are required because these pins are internally biased to approximately 1.7V DC. Either LO input can be driven with a single-ended source while connecting the unused input to ground through a DC blocking capacitor.

Exposed Pad (Pin 17): Circuit Ground Return for the Entire IC. This must be soldered to the printed circuit board ground plane.

BLOCK DIAGRAM

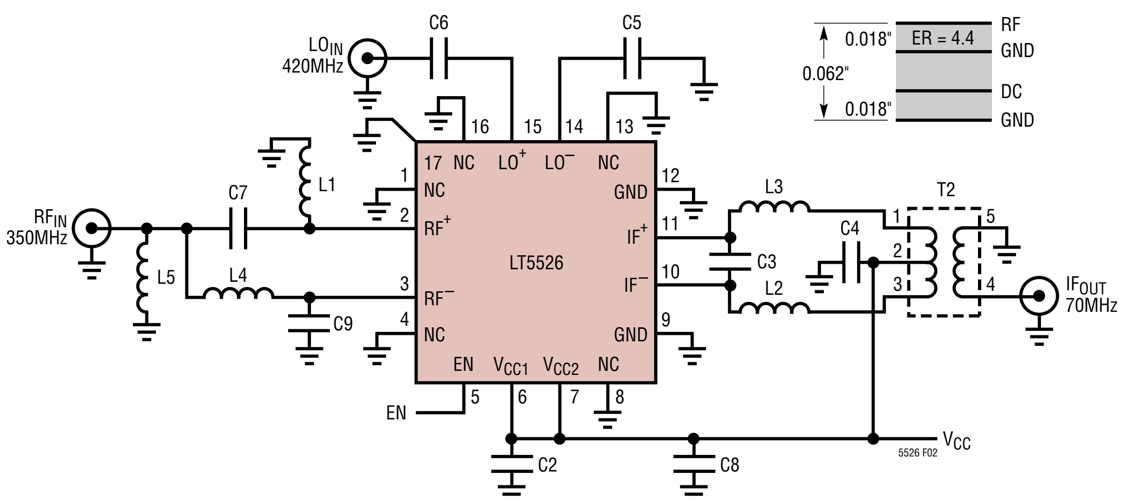


TEST CIRCUITS



REF DES	VALUE	SIZE	PART NUMBER	REF DES	VALUE	SIZE	PART NUMBER
C1	2.7pF	0402	AVX 04025A2R7CAT	L2, L3	150nH	1608	Toko LL1608-FSR15J
C2	0.01µF	0402	AVX 04023C103JAT	T1	1:1	1206	Murata LDB31900M05C-417
C3	1.2pF	0402	AVX 04025A1R2BAT	T2	4:1	SM-22	M/A-COM ETC4-1-2
C4, C5, C6	100pF	0402	AVX 04025A101JAT	TL1, TL2	Z_0 = 80	L = 1.25mm	
C8	1µF	0603	Taiyo Yuden LMK107BJ105MA				

Figure 1. Test Schematic for 900MHz Application. For 1900MHz or Other Applications, Component Values Are as Indicated in Figure 1 and in Applications Section



REF DES	VALUE	SIZE	PART NUMBER	REF DES	VALUE	SIZE	PART NUMBER
C2	0.01pF	0402	AVX 04023C103JAT	L1, L4	15nH	1005	Toko LL1005-FH15NJ
C3	3.9pF	0402	AVX 04025A3R9BAT	L2, L3	270nH	1608	Toko LL1608-FSR27J
C4, C5, C6	100pF	0402	AVX 04025A101JAT	L5	100nH	1005	Toko LL1005-FHR10J
C8	1µF	0603	Taiyo Yuden LMK107BJ105MA	T2	4:1	SM-22	M/A-COM ETC4-1-2
C7, C9	10pF	0402	AVX 04025A100JAT				

Figure 2. Test Schematic for 350MHz Applications

APPLICATIONS INFORMATION

The LT5526 consists of a double-balanced mixer, RF buffer amplifier, high speed limiting LO buffer and bias/enable circuits. The IC has been optimized for downconverter applications with RF input signals to 2GHz and LO signals to 2.5GHz. With proper matching, the IF output can be tuned for operation at frequencies from 0.1MHz to 1GHz. Operation over a wider input frequency range is possible, though with reduced performance.

The RF, LO and IF ports are all differential, though the LO port is internally matched for single-ended drive (with external DC blocking capacitors). The LT5526 is characterized and production tested using single-ended LO drive. Low side or high side LO injection can be used.

RF Input Port

Figure 3 shows a simplified schematic of the internal RF input circuit and example external impedance matching components for a 900MHz application. Each RF input pin requires a low resistance DC return to ground capable of handling 7.5mA. The DC ground can be realized using the center-tap of an input transformer (T1), as shown, or through matching inductors or bias chokes connected from Pins 2 and 3 to ground.

A lowpass impedance matching network is used to transform the differential input impedance at Pins 2 and 3 to the optimum value for the balun output, as illustrated in Figures 3 and 4. To assist in matching, Table 1 lists the differential input impedance and reflection coefficient at Pins 2 and 3 for several RF frequencies. The following example demonstrates how to design a lowpass impedance transformation network for the RF input.

From Table 1, the differential input impedance at 900MHz is: $R_{RF} + jX_{RF} = 31.3 + j8.41\Omega$. The 8.41Ω reactance is divided into two halves, with one half on each side of the 31.3Ω internal load resistor, as shown in Figure 4. The matching network consists of additional external series inductance and a capacitor (C1) in parallel with the desired source impedance (50Ω in this example). The external capacitance and inductance are calculated as follows:

$$n = R_S/R_{RF} = 50/31.3 = 1.597$$

$$Q = \sqrt{(n-1)} = 0.773$$

$$X_C = R_S/Q = 64.7\Omega$$

$$C1 = 1/(\omega \bullet X_C) = 2.74pF$$

$$X_L = R_{RF} \bullet Q = 24.2\Omega$$

$$X_{EXT} = X_L - X_{RF} = 15.8\Omega$$

$$L_{EXT} = X_{EXT}/\omega = 2.79nH$$

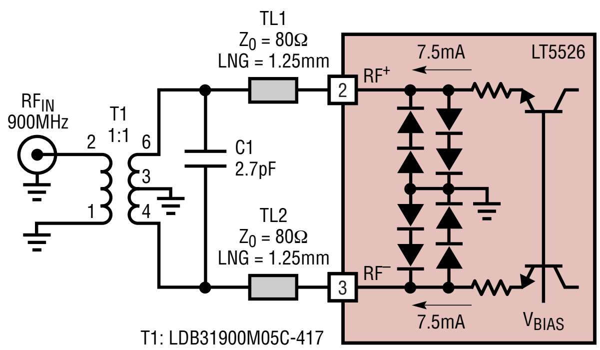


Figure 3. RF Input with External Matching for 900MHz Application

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The external inductance is split in half (1.4nH), with each half connected between the pin and C1 as shown in Figure 4. The inductance may be realized with short, high impedance printed transmission lines, as in Figure 3, which provides a compact board layout and reduced component count. A 1:1 transformer (T1 in Figure 3) converts the 50Ω differential impedance to a 50Ω single-ended input.

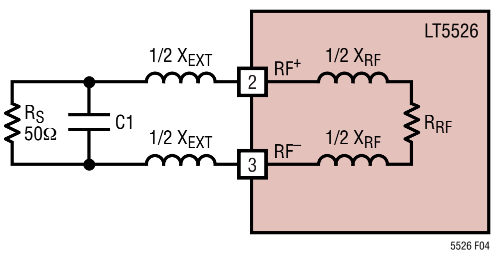

Figure 4. RF Input Impedance Matching Topology

Table 1. RF Input Differential Impedance

FREQUENCY (MHz)	INPUT IMPEDANCE	REFLECTION COEFFICIENT	
		MAG	ANGLE
70	28.0 + j1.34	0.282	176
140	28.2 + j2.46	0.280	172
240	28.4 + j3.30	0.278	169
360	28.4 + j4.75	0.282	164
450	28.6 + j5.42	0.280	162
750	29.9 + j7.39	0.268	155
900	31.3 + j8.41	0.251	150
1500	38.3 + j17.9	0.237	112
1900	42.5 + j24.6	0.269	92.2

An alternative method of driving the RF input is to use a lumped-element balun configuration, as shown in Figure 5. This type of network may provide a more cost-effective solution for narrow band applications (fractional bandwidths < 30%). The actual balun is composed of components C7, C9, L1 and L4, and their values may be estimated as follows:

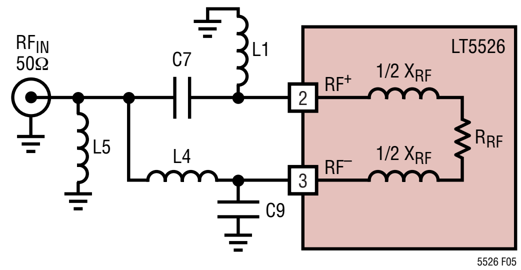

Figure 5. Schematic of Lumped Element Input Balun

$$L1 = L4 = \frac{\sqrt{R_S \cdot R_{RF}}}{\omega}$$

$$C7 = C9 = \frac{1}{\omega\sqrt{R_S \cdot R_{RF}}}$$

Where R_S is the source resistance (50Ω) and R_{RF} is the mixer input resistance from Table 1.

The computed values are only approximate, as they don't factor in the effects of X_{RF} or the parasitics of the external components. Actual component values for several frequencies are listed in Table 2, and measured return loss vs. frequency is plotted for each example in Figure 6.

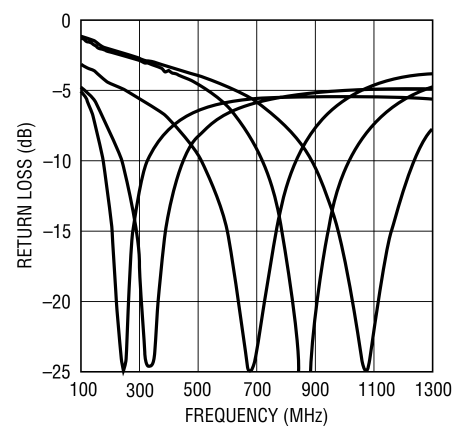

Figure 6. Input Return Loss with Lumped Element Baluns Using Values from Table 2

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The purpose of L5 is to provide a DC return path for Pin 3. (Another possible placement for L5 would be across Pins 2 and 3, thus using L1 as part of the DC return path.) The inductance and resonant frequency of L5 should be large enough that they don't significantly affect the input impedance and performance of the balun. Either multilayer or wire-wound inductors may be used.

The impact of L5 on input matching can be reduced by adding a capacitor in parallel with it. In this case, the capacitor value should be the same as C7 and C9, while L5 should have the same value as L1 and L4.

Table 2. Component Values for Lumped Balun on RF Input

FREQUENCY (MHz)	L (nH)	C (pF)	L5 (nH)	BANDWIDTH (MHz)
240	27	18	100	100
380	15	10	100	130
680	6.8	4.7	47	215
900	6.8	3.9	18	230
1100	3.9	2.7	15	230

LO Input Port

The LO buffer amplifier consists of high speed limiting differential amplifiers designed to drive the mixer core for high linearity. The LO^+ and LO^- pins are designed for single-ended drive, though differential drive can be used if desired. The LO input is internally matched to 50Ω; however, external DC blocking capacitors are required because the LO pins are internally biased to approximately 1.7V DC. A simplified schematic for the LO input is shown in Figure 7.

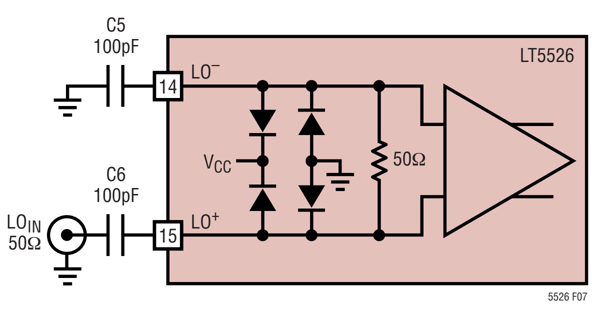

Figure 7. LO Input Schematic

External 100pF DC blocking capacitors provide a broadband match from about 110MHz to 2.7GHz, as shown in the plot of return loss vs frequency in Figure 8. The LO input match can be improved at lower frequencies by increasing the values of C5 and C6.

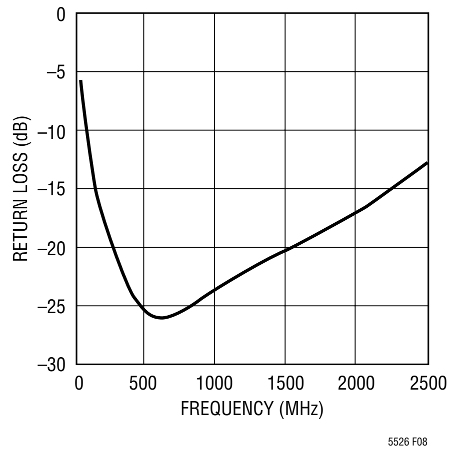

Figure 8. Typical LO Input Return Loss with 100pF DC Blocking Capacitors

Table 3. Single-Ended LO Input Impedance

FREQUENCY (MHz)	INPUT IMPEDANCE	REFLECTION COEFFICIENT MAG	ANGLE
400	63.4 – j12.0	0.158	–35.8
600	61.6 – j8.38	0.128	–31.5
800	61.8 – j6.86	0.122	–26.6
1000	62.4 – j7.09	0.127	–26.1
1200	62.8 – j8.32	0.135	–28.8
1400	62.6 – j10.3	0.144	–34.0
1600	61.9 – j12.6	0.154	–40.3
1800	60.5 – j14.4	0.160	–46.2

IF Output Port

A simplified schematic of the IF output circuit is shown in Figure 9. The output pins, IF^+ and IF^-, are internally connected to the collectors of the mixer switching transistors. Both pins must be biased at the supply voltage, which can be applied through the center-tap of a transformer or

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through impedance-matching inductors. Each IF pin draws about 7.5mA of supply current (15mA total). For optimum single-ended performance, these differential outputs must be combined externally through an IF transformer or balun.

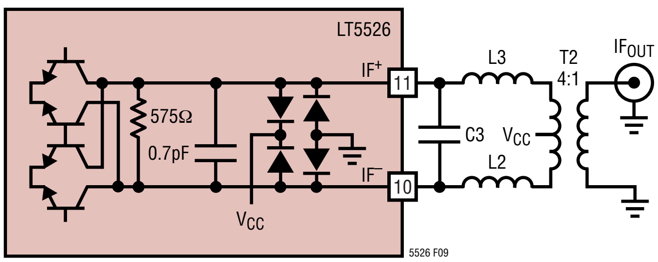

Figure 9. IF Output with External Matching

An equivalent small-signal model for the output is shown in Figure 10. The output impedance can be modeled as a 575Ω resistor in parallel with a 0.7pF capacitor. For most applications, the bond-wire inductance (0.7nH per side) can be ignored.

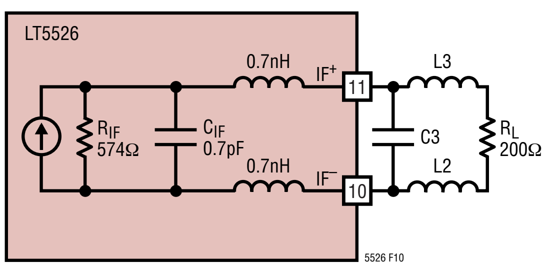

Figure 10. IF Output Small-Signal Model

The external components, C3, L2 and L3 form an impedance transformation network to match the mixer output impedance to the input impedance of transformer T2. The values for these components can be estimated using the same equations that were used for the input matching network, along with the impedance values listed in Table 4. As an example, at an IF frequency of 140MHz and R_L = 200Ω (using a 4:1 transformer for T2),

$$n = R_{IF}/R_L = 574/200 = 2.87$$
$$Q = \sqrt{(n - 1)} = 1.368$$
$$X_C = R_{IF}/Q = 420\Omega$$
$$C = 1/(\omega \bullet X_C) = 2.71pF$$
$$C3 = C - C_{IF} = 2.01pF$$
$$X_L = R_L \bullet Q = 274\Omega$$
$$L2 = L3 = X_L/2\omega = 156nH$$

Table 4. IF Differential Impedance (Parallel Equivalent)

FREQUENCY (MHz)	OUTPUT IMPEDANCE	REFLECTION COEFFICIENT	
		MAG	ANGLE
70	575‖ – j3.39k	0.840	–1.8
140	574‖ – j1.67k	0.840	–3.5
240	572‖ – j977	0.840	–5.9
450	561‖ – j519	0.838	–11.1
750	537‖ – j309	0.834	–18.6
860	525‖ – j267	0.831	–21.3
1000	509‖ – j229	0.829	–24.8
1250	474‖ – j181	0.822	–31.3
1500	435‖ – j147	0.814	–38.0

Low Cost Output Match

For low cost applications in which the required fractional bandwidth of the IF output is less than 25%, it may be possible to replace the output transformer with a lumped-element network similar to that discussed earlier for the RF input. This circuit is shown in Figure 11, where L11, L12, C11 and C12 form a narrowband bridge balun. These element values are selected to realize a 180° phase shift at the desired IF frequency and can be estimated by using the equations below. In this case, R_{IF} is the mixer output resistance and R_L is the load resistance (50Ω).

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$$L11 = L12 = \frac{\sqrt{R_{IF} \bullet R_L}}{\omega}$$

$$C11 = C12 = \frac{1}{\omega\sqrt{R_{IF} \bullet R_L}}$$

Inductors L13 and L14 provide a DC path between V_{CC} and the IF^+ pin. Only one of these inductors is required. Low cost multilayer chip inductors are adequate for L11, L12 and L13. If L14 is used instead of L13, a larger value is usually required, which may require the use of a wire-wound inductor. Capacitor C13 is a DC block which can also be used to adjust the impedance match. Capacitor C14 is a bypass capacitor.

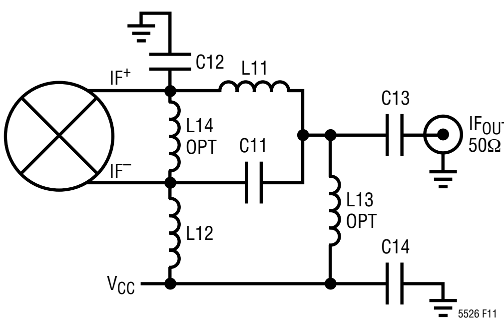


Figure 11. Narrowband Bridge IF Balun

Typical return loss of the IF output port is plotted versus frequency in Figure 12 for a 240MHz balun design. For this example, L11 = L12 = 100nH, C11 = C12 = 3.9pF, L14 = 560nH and C13 = 100pF. Performance versus IF output frequency is shown in Figure 13 in the case of a 1900MHz RF input. These results show that the usable IF bandwidth is greater than 60MHz, assuming tight tolerance matching components. Contact the factory for applications assistance with this circuit.

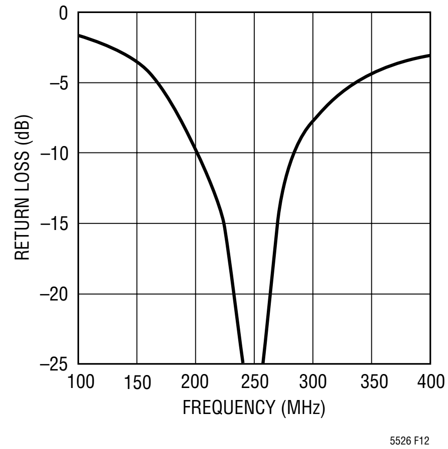


Figure 12. Typical Return Loss Performance with a 240MHz Narrowband Bridge IF Balun (Swept IF)

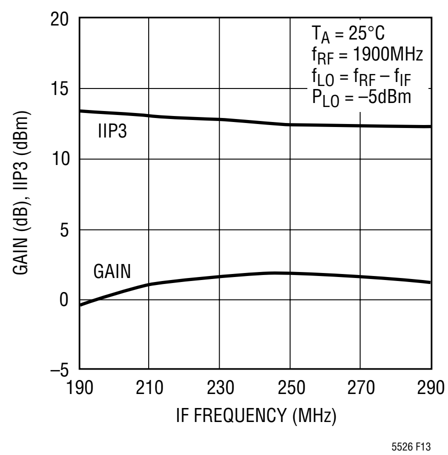
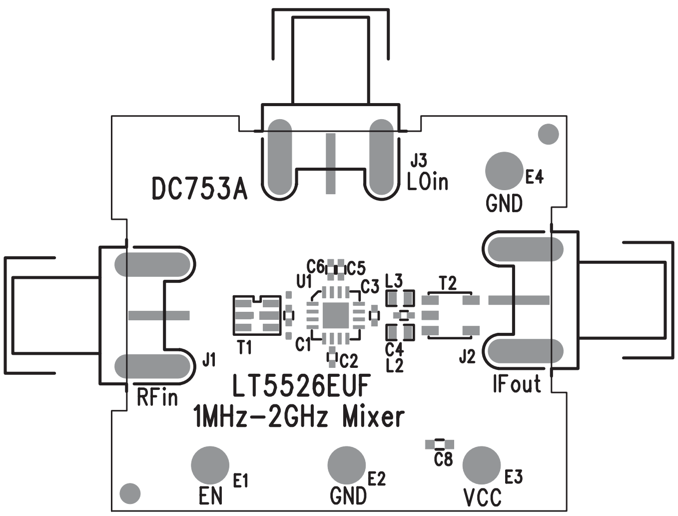


Figure 13. Typical Gain and IIP3 Performance with a 240MHz Narrowband Bridge IF Balun (Swept IF)

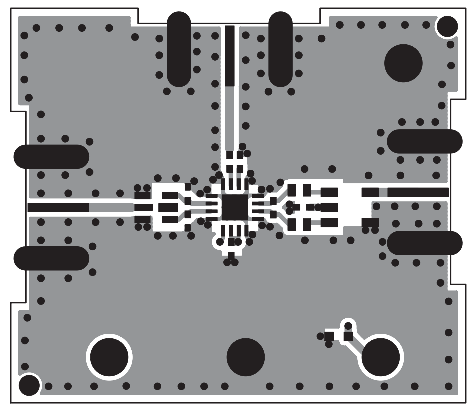
TYPICAL APPLICATIONS

Evaluation Board Layouts

Top Layer Silkscreen

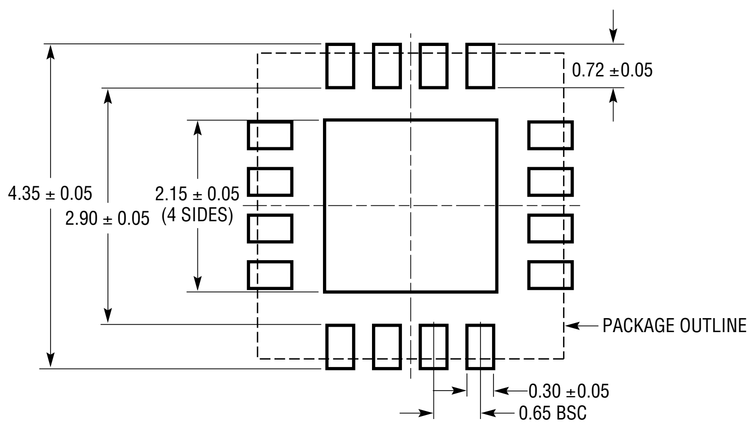


Top Layer Metal

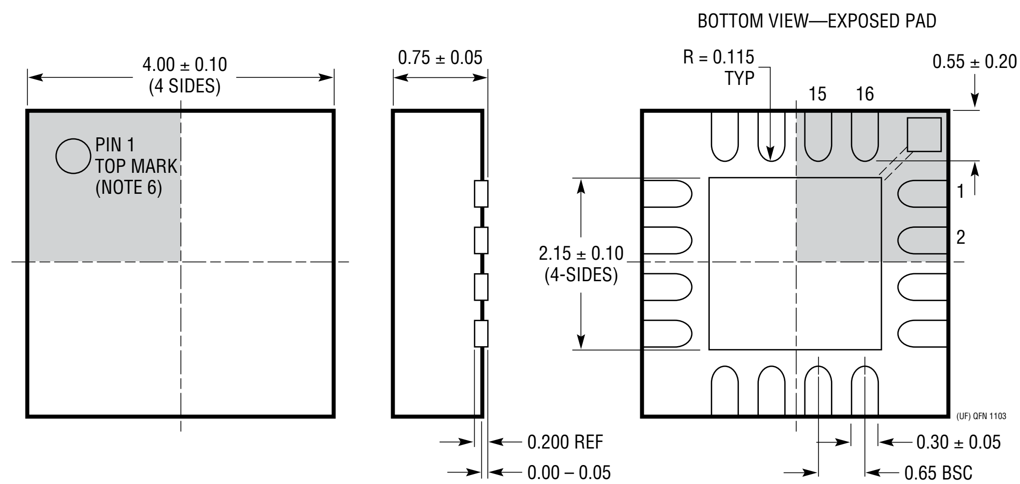


PACKAGE DESCRIPTION

UF Package
16-Lead Plastic QFN (4mm × 4mm)
(Reference LTC DWG # 05-08-1692)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGGC)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE