

Wide Dynamic Range RF/IF Log Detector

FEATURES

- Low Frequency to 1000MHz Operation
- 83dB Dynamic Range with ± 1 dB Nonlinearity at 200MHz
- Sensitivity -76 dBm or Better at 200MHz
- Log-Linear Transfer Slope of 20mV/dB
- Supply Voltage Range: 2.7V to 5.25V
- Supply Current: 13.5mA at 3V
- Tiny 8-Lead (3mm \times 2mm) DFN Package

DESCRIPTION

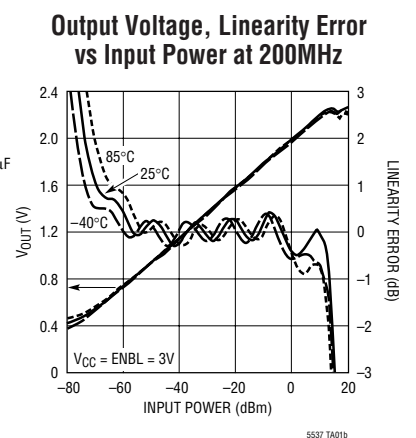
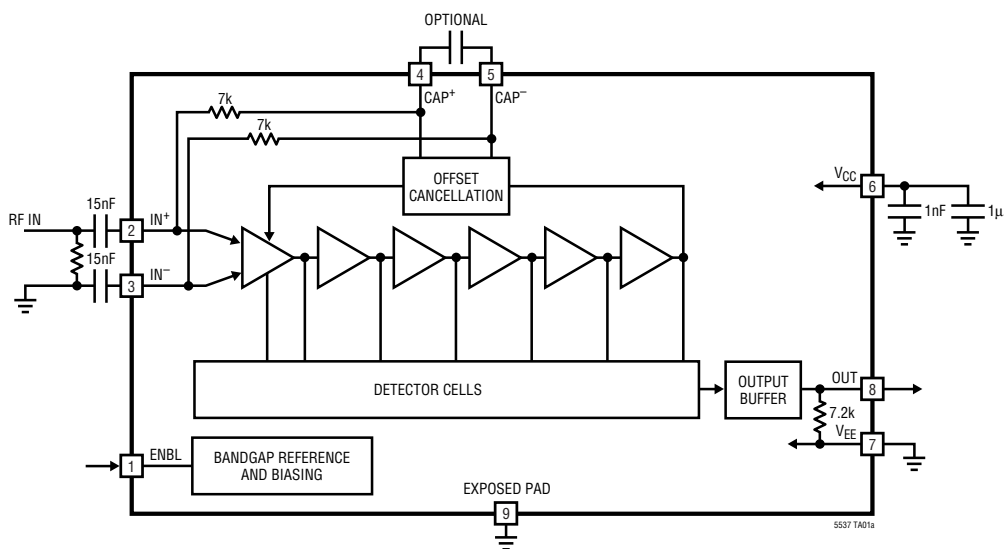
The LT[®]5537 is a wide dynamic range RF/IF detector, operational from below 10MHz to 1000MHz. The lower limit of the operating frequency range can be extended to near DC by the use of an external capacitor. The input dynamic range at 200MHz with ± 3 dB nonlinearity is 90dB (from -76 dBm to 14dBm, single-ended 50 Ω input). The detector output voltage slope is nominally 20mV/dB, and the typical temperature coefficient is 0.01dB/ $^{\circ}$ C at 200MHz.

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APPLICATIONS

- Linear-to-Log Signal Level Conversion
- Received Signal Strength Indication (RSSI)
- RF Power Control
- RF/IF Power Detection
- Receiver RF/IF Gain Control
- Envelope Detection
- ASK Receiver

TYPICAL APPLICATION



ABSOLUTE MAXIMUM RATINGS

(Note 1)

Power Supply Voltage	5.5V
Enable Voltage	-0.2V, $V_{CC} + 0.2V$
Input Power (Note 2)	22dBm
Operating Ambient Temperature Range ..	-40°C to 85°C
Storage Temperature Range	-65°C to 125°C
Maximum Junction Temperature	125°C

PACKAGE/ORDER INFORMATION

TOP VIEW

DDB PACKAGE
8-LEAD (3mm × 2mm) PLASTIC DFN
 $\theta_{JA} = 76^{\circ}\text{C/W}$
EXPOSED PAD (PIN 9) SHOULD BE SOLDERED TO PCB

ORDER PART NUMBER	DDB PART MARKING
LT5537EDDB	LBJR

Order Options Tape and Reel: Add #TR
Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: <http://www.linear.com/leadfree/>

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS $V_{CC} = 3V$, $ENBL = 3V$, $T_A = 25^{\circ}\text{C}$, unless otherwise specified. (Notes 3, 4)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Signal Input					
Input Frequency Range	(Note 5)		10 to 1000		MHz
Maximum Input Power for Monotonic Output	50Ω Termination				
	200MHz		14.0		dBm
	600MHz		11.6		dBm
	1GHz		9.4		dBm
DC Common Mode Voltage			$V_{CC} - 0.4$		V
Small-Signal Impedance	Measured at 200MHz		1.73kΩ //1.45pF		
f = 10MHz					
Linear Dynamic Range	±3dB Error		88.8		dB
	±1dB Error		72.5		dB
Slope	R1 = 33k (Note 8)		19.6		mV/dB
Intercept	$V_{OUT} = 0V$, Extrapolated		-97		dBm
Sensitivity	(Notes 3, 7)		-76.7		dBm
Temperature Coefficient	$P_{IN} = -20\text{dBm}$		-0.007		dB/°C
f = 50MHz					
Linear Dynamic Range	±3dB Error		90.6		dB
	±1dB Error		81.0		dB
Slope	R1 = 33k (Note 8)		20		mV/dB
Intercept	$V_{OUT} = 0V$, Extrapolated		-96		dBm
Sensitivity	(Notes 3, 7)		-77.2		dBm
Temperature Coefficient	$P_{IN} = -20\text{dBm}$		-0.005		dB/°C

ELECTRICAL CHARACTERISTICS $V_{CC} = 3V$, $ENBL = 3V$, $T_A = 25^\circ C$, unless otherwise specified. (Notes 3, 4)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
f = 100MHz					
Linear Dynamic Range	$\pm 3dB$ Error		90.5		dB
	$\pm 1dB$ Error		82.8		dB
Slope	$R1 = 33k$ (Note 8)		20.3		mV/dB
Intercept	$V_{OUT} = 0V$, Extrapolated		-95		dBm
Sensitivity	(Notes 3, 7)		-77		dBm
Temperature Coefficient	$P_{IN} = -20dBm$		-0.004		dB/ $^\circ C$
f = 200MHz					
Linear Dynamic Range	$\pm 3dB$ Error		90.3		dB
	$\pm 1dB$ Error		83.5		dB
Slope	$R1 = 33k$ (Note 8)		21.2		mV/dB
Intercept	$V_{OUT} = 0V$, Extrapolated		-94		dBm
Sensitivity	(Notes 3, 7)		-76.4		dBm
Temperature Coefficient	$P_{IN} = -20dBm$		0.010		dB/ $^\circ C$
f = 400MHz					
Linear Dynamic Range	$\pm 3dB$ Error		88.2		dB
	$\pm 1dB$ Error		70.8		dB
Slope	$R1 = 33k$ (Note 8)		23.1		mV/dB
Intercept	$V_{OUT} = 0V$, Extrapolated		-91		dBm
Sensitivity	(Notes 3, 7)		-75.3		dBm
Temperature Coefficient	$P_{IN} = -20dBm$		0.019		dB/ $^\circ C$
f = 600MHz					
Linear Dynamic Range	$\pm 3dB$ Error		85.8		dB
	$\pm 1dB$ Error		72.5		dB
Slope	$R1 = 33k$ (Note 8)		25.2		mV/dB
Intercept	$V_{OUT} = 0V$, Extrapolated		-89		dBm
Sensitivity	(Notes 3, 7)		-74.1		dBm
Temperature Coefficient	$P_{IN} = -20dBm$		0.026		dB/ $^\circ C$
f = 1GHz					
Linear Dynamic Range	$\pm 3dB$ Error		63.5		dB
	$\pm 1dB$ Error		51.7		dB
Slope	$R1 = 33k$ (Note 8)		31.4		mV/dB
Intercept	$V_{OUT} = 0V$, Extrapolated		-80		dBm
Sensitivity	(Notes 3, 7)		-69.2		dBm
Temperature Coefficient	$P_{IN} = -20dBm$		0.031		dB/ $^\circ C$
Output					
Starting Voltage	No RF Signal Present		0.4		V
Response Time	Input from -30dBm to 0dBm, $C_{LOAD} = 2.5pF$		110		ns
Baseband Modulation Bandwidth	Output Load Capacitance = 2.5pF		6		MHz
Shutdown Mode					
ENBL = High (On)		1			V
ENBL = Low (Off)				0.3	V
ENBL Input Current	$V_{ENBL} = 3V$		100		μA
	$V_{ENBL} = 0V$		0		μA
Turn-On Time			100		μs
Turn-Off Time			100		μs

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ELECTRICAL CHARACTERISTICS $V_{CC} = 3V$, $ENBL = 3V$, $T_A = 25^\circ C$, unless otherwise specified. (Notes 3, 4)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply					
Supply Voltage	(Note 6)	2.7		5.25	V
Supply Current	$V_{CC} = 3V$	10	13.5	15	mA
Shutdown Current	$ENBL = Low$		500		μA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Maximum differential AC input voltage between IN^+ and IN^- is 4V peak. Equivalent to 22dBm with 50Ω input impedance or 16dBm with 200Ω input impedance (1:4 transformer used).

Note 3: Tests are performed as shown in the configuration of Figure 13.

Note 4: Specifications over the $-40^\circ C$ to $85^\circ C$ temperature range are assured by design, characterization and correlation with statistical process control.

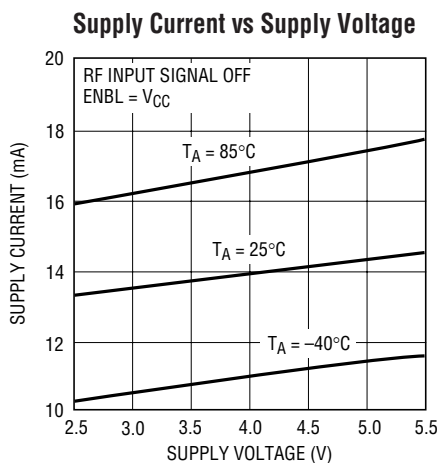
Note 5: Operation at lower frequency is possible as described in the “Low Frequency Operation” section in Applications Information.

Note 6: The maximum output voltage is limited to approximately $V_{CC} - 0.6V$. Either the output slope should be reduced or input power level should be limited in order to avoid saturating the output circuit when $V_{CC} < 3V$. See discussion in “Dynamic Range” section.

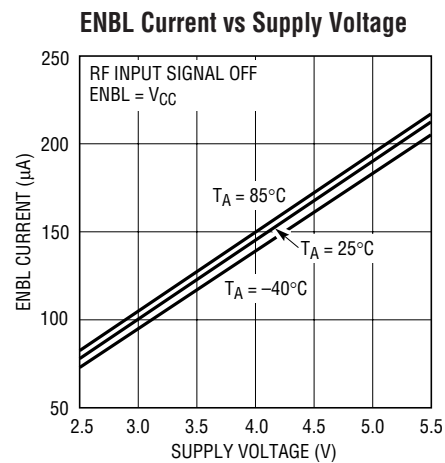
Note 7: Sensitivity is defined as the minimum input power required for the output voltage to be within 3dB of the ideal log-linear transfer curve. Sensitivity can be improved by as much as 10dB by using a narrowband input impedance transformation network. See discussion in “Input Matching” section.

Note 8: The output slope is adjustable using an external pull-down resistor (R1). See Applications Information for description of the output circuit.

TYPICAL PERFORMANCE CHARACTERISTICS



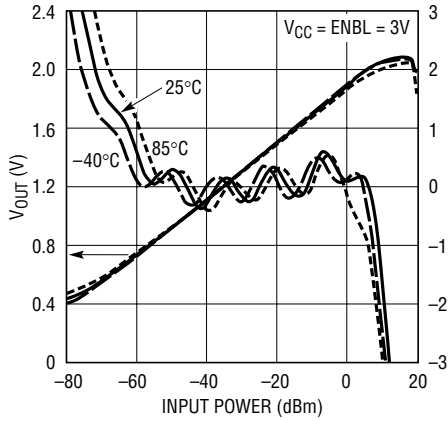
5537 G02



5537 G03

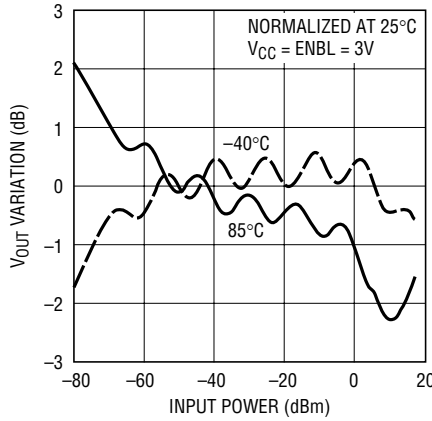
TYPICAL PERFORMANCE CHARACTERISTICS

Output Voltage, Linearity Error vs Input Power at 10MHz



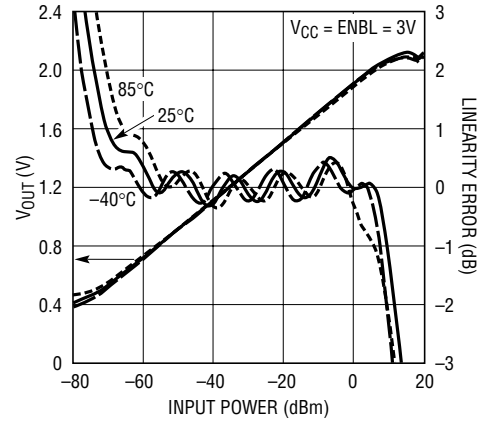
5537 G04

V_{OUT} Variation vs Input Power at 10MHz



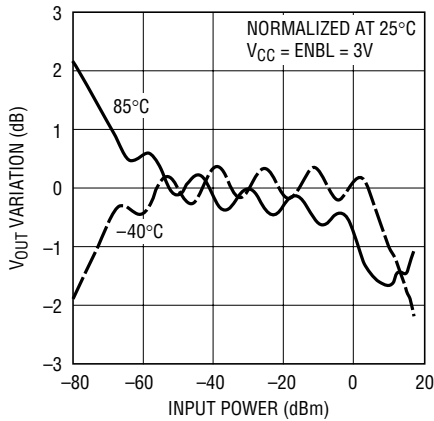
5537 G05

Output Voltage, Linearity Error vs Input Power at 50MHz



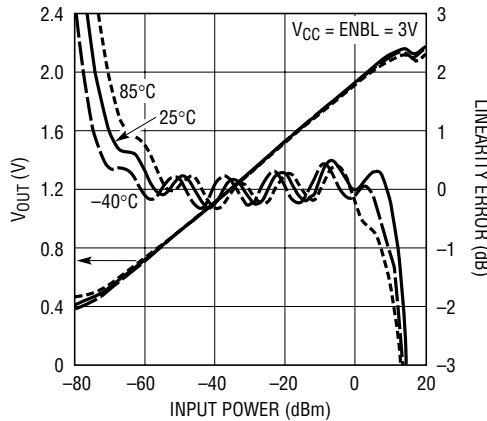
5537 G06

V_{OUT} Variation vs Input Power at 50MHz



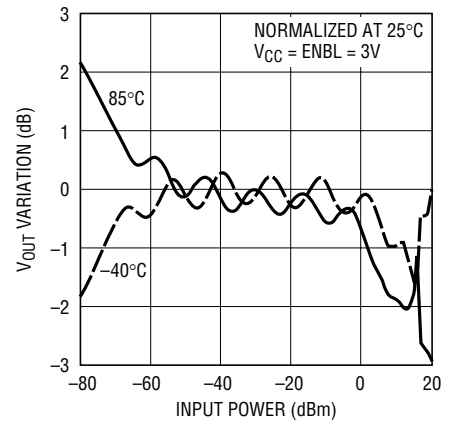
5537 G07

Output Voltage, Linearity Error vs Input Power at 100MHz



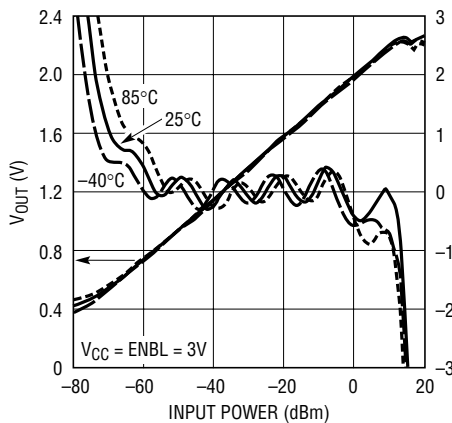
5537 G08

V_{OUT} Variation vs Input Power at 100MHz



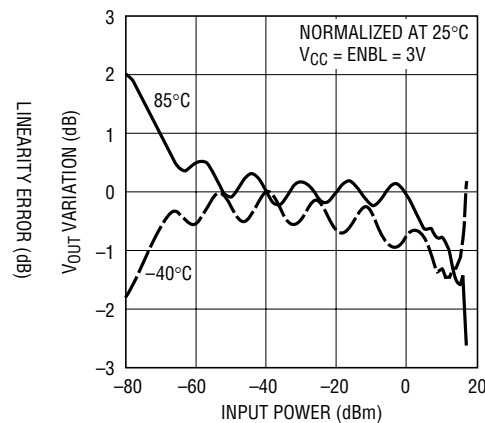
5537 G09

Output Voltage, Linearity Error vs Input Power at 200MHz



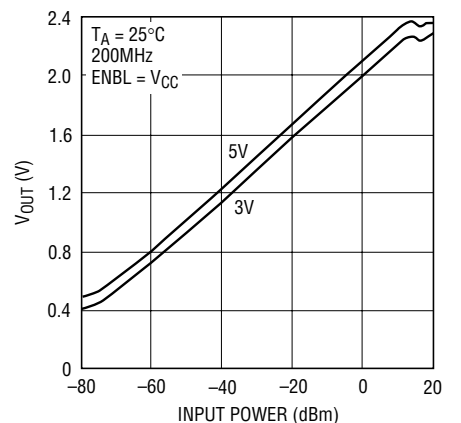
5537 G10

V_{OUT} Variation vs Input Power at 200MHz



5537 G11

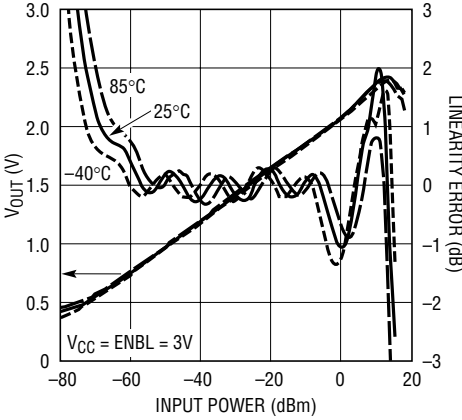
Typical Detector Characteristics



5537 G12

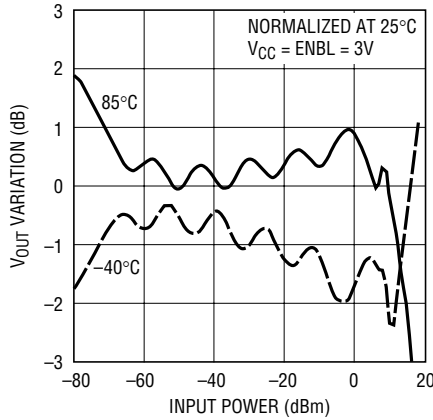
TYPICAL PERFORMANCE CHARACTERISTICS

Output Voltage, Linearity Error vs Input Power at 400MHz



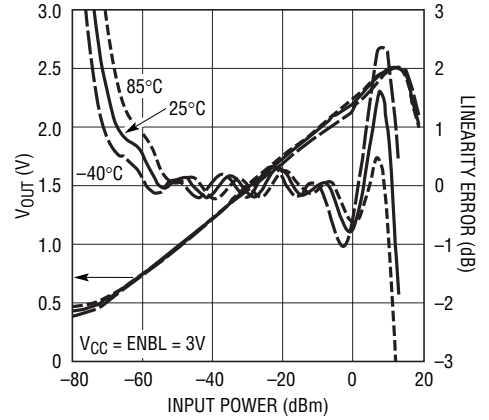
5537 G13

V_{OUT} Variation vs Input Power at 400MHz



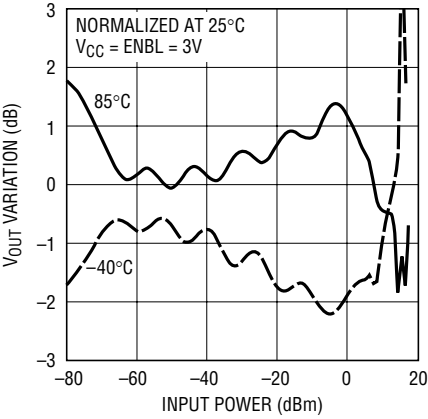
5537 G11

Output Voltage, Linearity Error vs Input Power at 600MHz



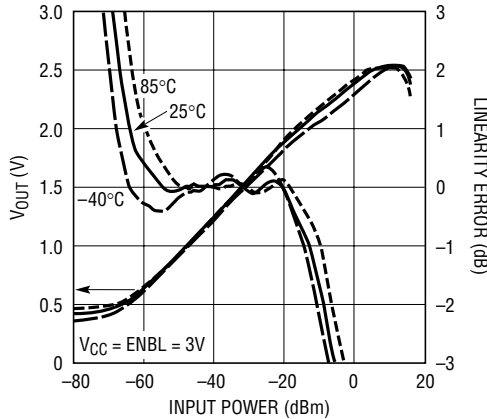
5537 G15

V_{OUT} Variation vs Input Power at 600MHz



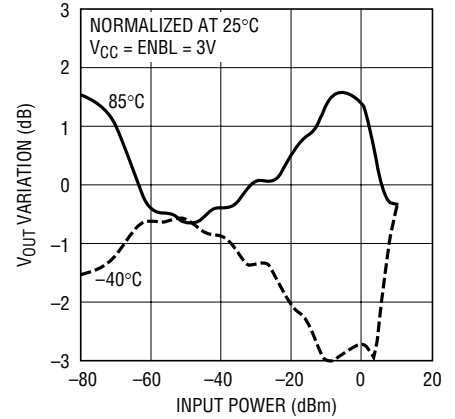
5537 G16

Output Voltage, Linearity Error vs Input Power at 1GHz



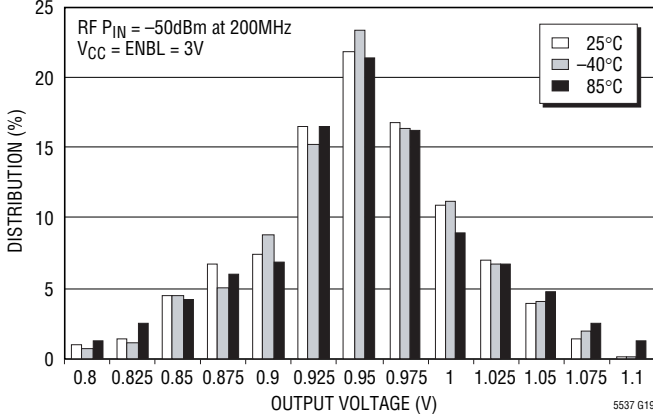
5537 G17

V_{OUT} Variation vs Input Power at 1GHz



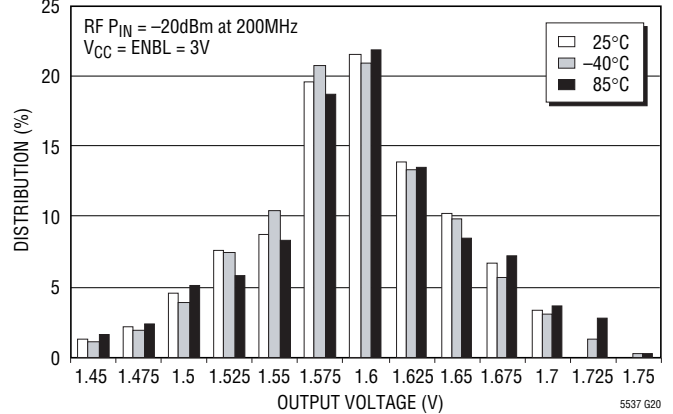
5537 G18

Output Voltage Distribution vs Temperature at -50dBm



5537 G19

Output Voltage Distribution vs Temperature at -20dBm



5537 G20

PIN FUNCTIONS

ENBL (Pin 1): Enable Pin. When the input voltage is higher than 1V, the circuit is ON. When the input voltage is less than 0.3V, or this pin is not connected, the chip is disabled (OFF).

IN⁺, IN⁻ (Pins 2, 3): Differential Signal Input Pins. These pins are internally biased to $V_{CC} - 0.4V$. The impedance between IN⁺ and IN⁻ is approximately $1.73k\Omega/1.45pF$ at 200MHz. The input pins should be AC coupled.

CAP⁺, CAP⁻ (Pins 4, 5): External Filter Capacitor Pins. The minimum RF input frequency can be lowered by adding an optional external capacitor between CAP⁺ and CAP⁻.

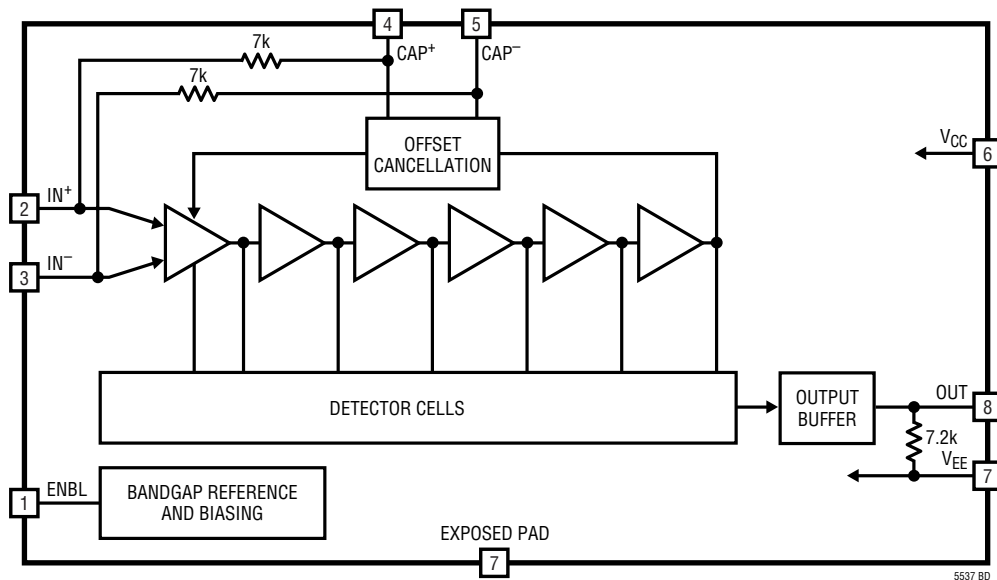
V_{CC} (Pin 6): Power Supply Pin. This pin should be decoupled using 1000pF and 0.1μF capacitors.

V_{EE} (Pin 7): Ground pin.

OUT (Pin 8): Output pin.

Exposed Pad (Pin 9): Should be connected to PCB ground.

BLOCK DIAGRAM



5537 BD

APPLICATIONS INFORMATION

The LT5537 provides a log-linear relationship between an RF/IF input voltage and its output. The input signal is amplified successively by limiting amplifier stages. A series of detector cells rectify the signals and produce an output current which is log-linearly related to the input power with a coefficient (I_{SLOPE}) of $3.4\mu A/dB$ at 200MHz (independent of the input termination impedance). This coefficient is almost constant below 200MHz, but rises at higher frequency. The normalized slope variation plot in Figure 1 can be used to determine the log-linear coefficient at any frequency. The slope of the output voltage curve is determined by the total load resistance at the output terminal.

$$V_{SLOPE} = I_{SLOPE} \cdot R_{LOAD}$$

The on-chip pull-down resistor is 7.2k. The total load resistance (R_{LOAD}) can be adjusted by adding external load resistance to change the output slope. For example, to achieve a log-linear rate of 20mV/dB, a 33k resistor is connected between the output pin and ground.

$$\text{Slope} = 3.4\mu A/dB \cdot (7.2/33)k\Omega = 20.1mV/dB$$

Additionally, an off-chip capacitor may be used to reduce the output time domain voltage ripple.

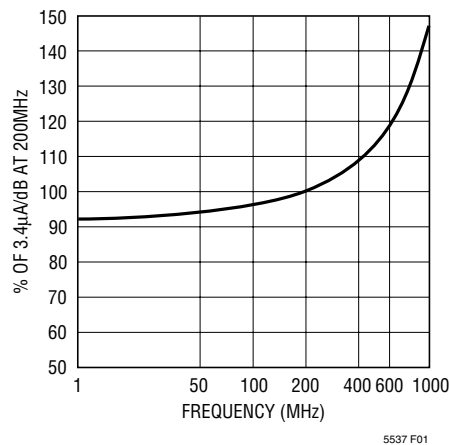


Figure 1. Slope Variation over Frequency

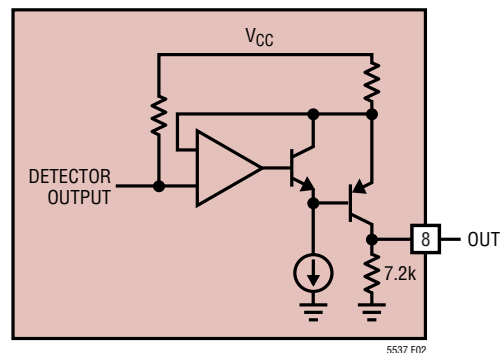


Figure 2. Simplified Output Circuit

APPLICATIONS INFORMATION

Dynamic Range

The LT5537 is capable of detecting and log-converting an input signal over a wide dynamic range. The range of the output voltage may be limited, however, and the monotonicity of the output versus input at high input level may be affected if the supply voltage is low and the log-linear slope is set too high. The minimum V_{CC} to support 90dB dynamic range with 20mV/dB slope is 2.8V under nominal conditions at 25°C. The data shown in the Typical Performance Characteristics plots was taken with $V_{CC} = 3V$. If there is difficulty encountered in achieving the desired dynamic range, then the user is advised to increase the supply voltage or else to decrease the output slope by connecting a smaller valued resistor between the output and ground.

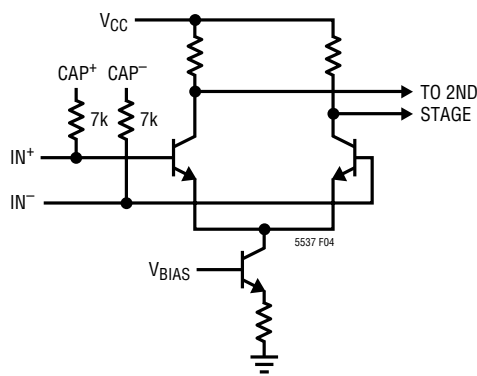


Figure 3. Simplified Input Circuit

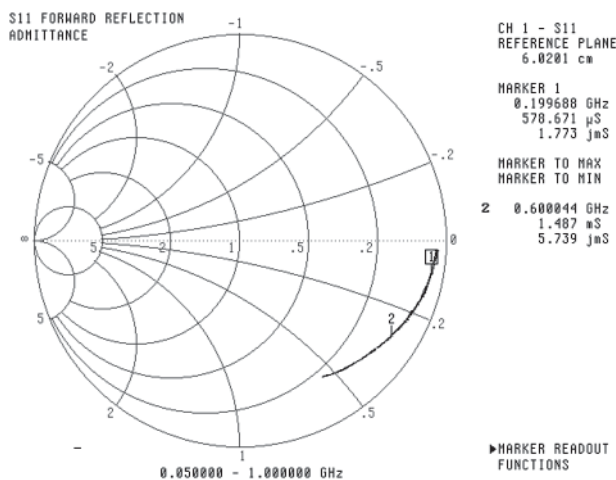


Figure 4. Input Admittance

Input Matching

The LT5537 has a high impedance input (Figure 3). The differential input impedance is derived from S11 measurement with one of the input pins AC grounded (Figure 4). At 200MHz, the input is equivalent to 1.73k/1.45pF (Table 1).

The input dynamic range is constant in voltage terms, ranging from approximately -89dBVrms to 1dBVrms at 200MHz. The dynamic range expressed in power is dependent on the actual impedance selected in the application design.

Table 1. Parallel Equivalent RC of the LT5537 Input

FREQUENCY	R	C
100MHz	1.85kΩ	1.51pF
200MHz	1.73kΩ	1.45pF
400MHz	1.07kΩ	1.48pF
600MHz	673Ω	1.52pF
800MHz	435Ω	1.65pF
1000MHz	303Ω	1.78pF

The simplest way of input matching the LT5537 is to terminate the input signal with a 50Ω resistor and AC couple it to one of the input pins while AC grounding the other input pin (Figure 13). The sensitivity (defined as the minimum input power required for the output to be within 3dB of the ideal log-linear response) is -76.4dBm at 200MHz in this case.

To achieve the best sensitivity, the input termination impedance should be increased and the input pins should be differentially driven. An example application circuit is shown in Figure 5 which uses a transformer to step up the impedance and perform the balun function. The 240Ω resistor (R2) sets the impedance at the input of the chip to 200Ω. A 1:4 transformer is used to match the 50Ω signal source impedance to the circuit input impedance. C1 and C2 are DC blocking capacitors. This application circuit has a (3dB error) sensitivity of -82.4dBm at 200MHz.

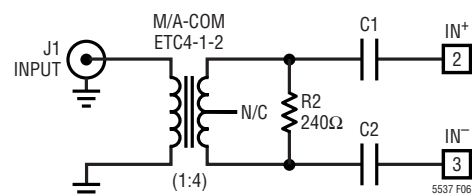


Figure 5. Differential Input Matching to 200Ω

APPLICATIONS INFORMATION

The 1:4 input transformer can also be replaced with a narrow band discrete balun circuit using three components as shown in Figure 6. Capacitors C11, C12 and inductor L1 form a tank circuit having a transformer-like function over a narrow bandwidth. The increased power-to-voltage transformation and the narrower input passband serve to improve the sensitivity of the logarithmic detector.

The resonant balun circuit using discrete components can be custom designed for a range of different input impedance or sensitivity requirements.

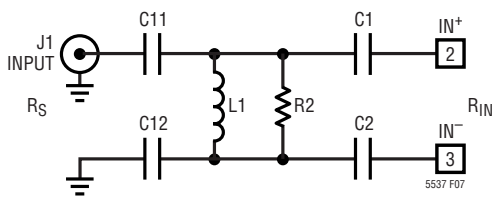


Figure 6. Input Matching Network

Table 2. Matching Network Component Values for 200MHz Center Frequency

SENSITIVITY (dBm)	10dB RETURN LOSS BW (MHz)	L1 (nH)	C11, C12 (pF)	R2 (Ω)	Q	EFFECTIVE INPUT RESISTANCE (Ω)
-82.4	55	82	15	330	2.1	264
-86.1	18	120	7.5	2k	3.9	828

The examples given in Table 2 cover two different transformation ratios. The first one transforms single-ended 50Ω to differential 264Ω. The V_{OUT} vs P_{IN} transfer curves in Figure 7 indicate that the input power range for linear logarithmic detection is shifted downward by 7dB with a sensitivity improvement of 6dB compared with a simple 50Ω termination. The input return loss is 30dB at the design frequency of 200MHz. Bandwidth for better than 10dB return loss is 55MHz. The second example has a higher Q of 3.9 and a corresponding transformed impedance of 828Ω. The input power range for linear operation is shifted downward by 12dB with a sensitivity improvement of 10dB compared with a simple 50Ω termination. The input return loss is 25dB at the design frequency. Bandwidth for better than 10dB return loss is 18MHz.

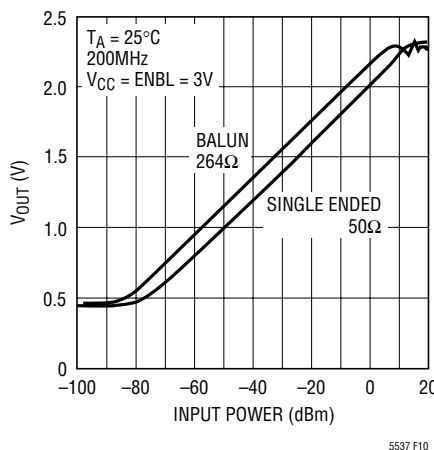


Figure 7. Measured Output with $R_{IN} = 264\Omega$

APPLICATIONS INFORMATION

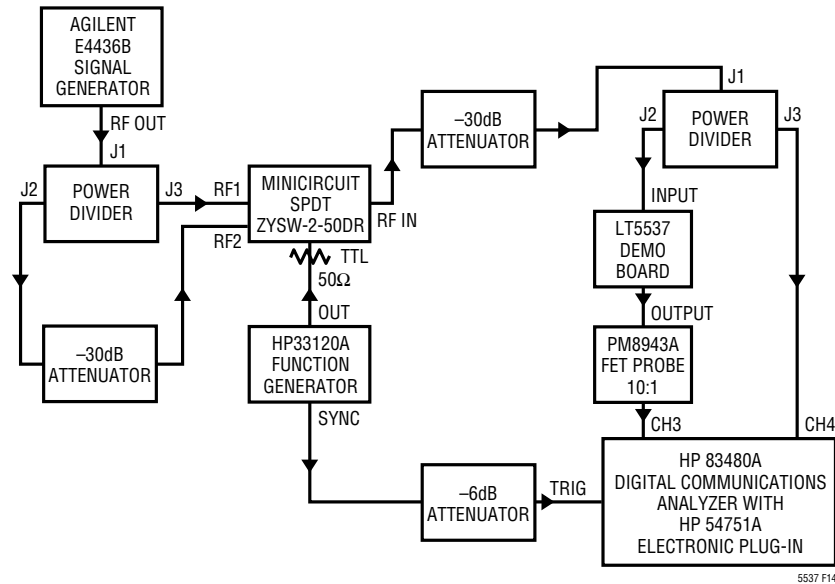


Figure 8. Timing Test Setup

Baseband Response

The unloaded bandwidth of the LT5537 output buffer is 10MHz. With 2.5pF loading, the output bandwidth is approximately 6MHz. The baseband response of the LT5537 was characterized with a pulsed RF input using the setup shown in Figure 8. The input to the LT5537 is a 200MHz CW RF signal switched between -30dBm and -60dBm at a rate of 600kHz. The output was connected to a FET probe (Fluke PM8943A, 10:1 tip) which has a capacitive loading of 2.5pF. The 10% to 90% rise and fall times are 109ns and 115ns, respectively. The input signal and output response are shown in Figure 9.

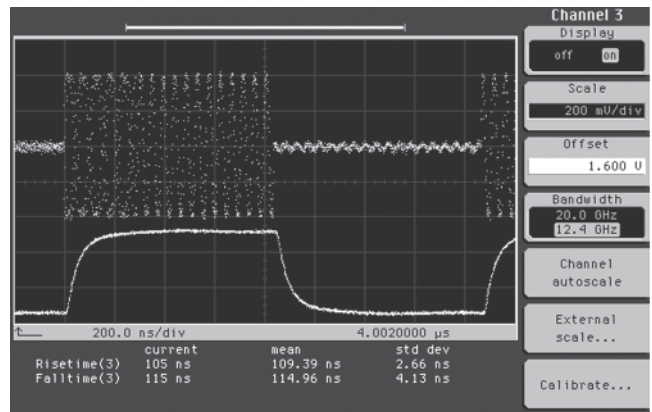


Figure 9. Response Time (-30dBm to -60dBm)

APPLICATIONS INFORMATION

Table 3. Application Design Examples

DESIGN NUMBER	C1, C2	C6	INPUT POLE	INTERNAL POLE	DC REJECTION BW	DC LOOP PM	LOWEST OPERATING FREQUENCY	APPLICATIONS
1	15nF	Open	8.5kHz	414kHz	1.13MHz	75°	1.13MHz	Minimal Component Count
2	100pF	33nF	1.3MHz	740Hz	160kHz	84°	1.3MHz	General Purpose
3	5pF	390pF	20MHz	50kHz	10MHz	60°	20MHz	HF, Fast Settling
4	47nF	2.2μF	2.8kHz	10Hz	2kHz	57°	2.8kHz	Very Low Frequency

Bold = dominant pole

Low Frequency Operation

Because the limiting amplifier stages of the LT5537 are DC coupled, the high overall gain requires DC offset control. The LT5537 has internal DC offset cancellation circuitry. The voltage at the output of the limiting amplifier is low-pass filtered, inverted and fed back to the input of the limiting amplifier. The DC cancellation also reduces the gain of the amplifier at low frequency. As a result, the LT5537 has a bandpass frequency response with a lower end determined by the bandwidth of the offset cancellation feedback loop.

The equivalent circuit of the loop filter is shown in Figure 10. C1 and C2 are the external DC blocking capacitors of the differential inputs; C6 is an optional external filter capacitor which is in parallel with an on-chip filter capacitor ($C_{INT} = 60\text{pF}$). For analysis purposes only, the values for C6 and the on-chip filter capacitor are doubled when a single-ended equivalent circuit is derived from a differential implementation.

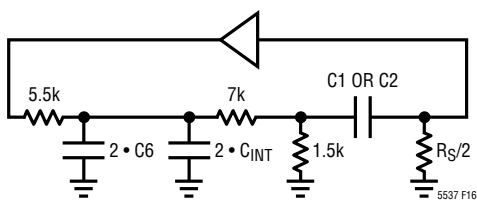


Figure 10. Offset Cancellation Loop Filter

The optional capacitance (C6) placed between CAP+ (Pin 4) and CAP- (Pin 5) together with the input DC blocking capacitors C1 and C2 are used to adjust the operating frequency range. The DC offset cancellation loop contains two poles and one zero (in the low frequency region for the purpose of this analysis). The loop filter capacitance ($C6 + C_{INT}$) generates one of the two poles, the input AC coupling capacitors (C1 and C2) determine the other pole and the input termination resistance leads to the zero. (The pole associated with the input AC coupling capacitor also sets the lower corner frequency of the signal path). The presence of the two poles in the circuit enables two approaches to the design of the application circuit for a desired frequency response. But stability margin has to be ensured in order to avoid ringing in response to any input transient. Table 3 lists four low frequency loop designs suitable for different applications.

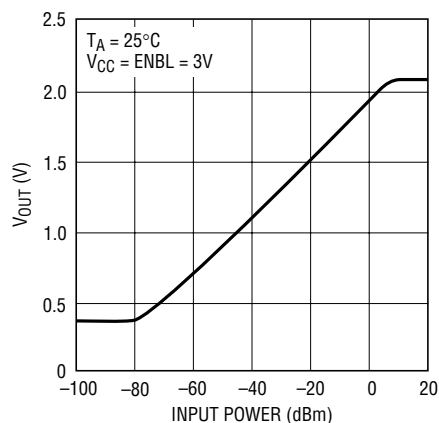
Design 1 is the simplest application circuit. The external capacitor C6 is not used. The input pole is set by the AC coupling capacitors (C1, C2) and is the dominant pole at 8.5kHz. The zero generated by the input coupling capacitor and the termination resistor is at 60 times the input pole frequency. The second pole set by the on-chip filter capacitor (C_{INT}) should be at approximately the same frequency as that of the zero. This design has a stability phase margin (PM) of 75 degrees.

APPLICATIONS INFORMATION

Design 2 is the application circuit (Figure 13) used for characterization in this data sheet. This is a robust general purpose design which can operate as low as 1.3MHz. Optional filter capacitor ($C6 = 33\text{nF}$) together with the on-chip capacitor set the dominant pole at 740Hz. The input pole associated with the AC coupling capacitors ($C1, C2 = 100\text{pF}$) is at 1.3MHz which is beyond the loop cut-off frequency of 160kHz. The zero is at an even higher frequency and can be safely ignored. This design has a stability phase margin of 84 degrees, resulting in a very well damped response to any input biasing transients.

Design 3 features fast settling. This design is appropriate when fast response in the presence of input biasing transients is required, and very low frequency operation is not needed.

Design 4 demonstrates the possibility of operating the LT5537 at very low frequency ($<10\text{kHz}$) by configuring the offset cancellation loop for very low bandwidth. The response of this circuit at 10kHz is plotted in Figure 11.



5537 F17

Figure 11. 10kHz Operation

Offset Cancellation Loop and the Timing Response

The input of the LT5537 is AC coupled, and the on-chip DC biasing is automatically regulated as described above. But if the DC component of the input signal has any transient step with sufficiently short rise or fall time (for example the output of an active RF switch has a biasing shift between switching states), a transient voltage pulse is induced by the displacement current needed to charge the input AC coupling capacitor. Also, if the pulse frequency or the repetition rate is within the loop bandwidth of the offset cancellation circuit, the LT5537 will respond to the induced voltage pulse in the same way it nulls out its internal DC offset, even though the chip is DC isolated from the input signal.

If the external capacitor ($C6$) is used to extend the low frequency response of the LT5537, then this will also lengthen the response time of the DC offset cancellation circuit. In the presence of DC steps or glitches at the input, the transient response of the slowed offset cancellation loop will be superimposed on the faster logarithmic detector output, degrading the overall response time of the chip.

The sensitivity of the LT5537 is very high. An input biasing step with amplitude of 0.5mV can generate a output voltage response of 400mV before the input voltage transient dissipates or the offset cancellation loop nulls out the transient, whichever occurs first.

One way to prevent the input signal containing a biasing transient from degrading the timing response is to design the offset cancellation loop to have a high bandwidth, allowing faster settling. Design 3 in Table 3 is suitable for this purpose, but will not operate below 20MHz.

APPLICATIONS INFORMATION

Enable Pin Operation

The enable circuit of the LT5537 is shown in a simplified form in Figure 12. When the voltage at the ENBL pin is $\geq 1V$, the enable circuit biases the chip up for normal operation. The current drawn by the ENBL pin is dependent on the voltage on that pin. At $V_{CC} = ENBL = 3V$, the ENBL current is typically $100\mu A$. At $V_{CC} = ENBL = 5V$, the ENBL current increases to about $200\mu A$. When the voltage at the ENBL pin is $\leq 0.3V$, or if the pin is not connected, the chip is disabled and draws a reduced supply current of about $500\mu A$, with $V_{CC} = 3V$.

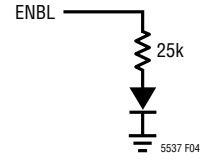


Figure 12. Equivalent ENBL Input Circuit

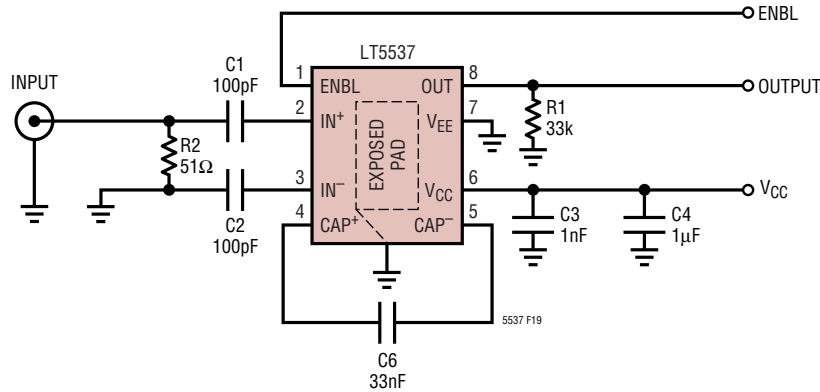


Figure 13. Application Board Schematic

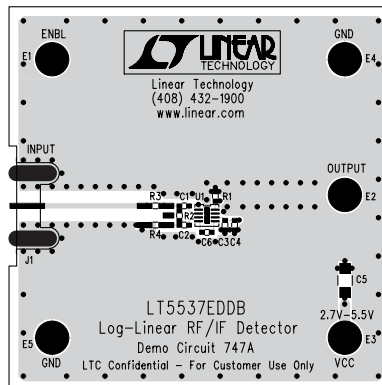
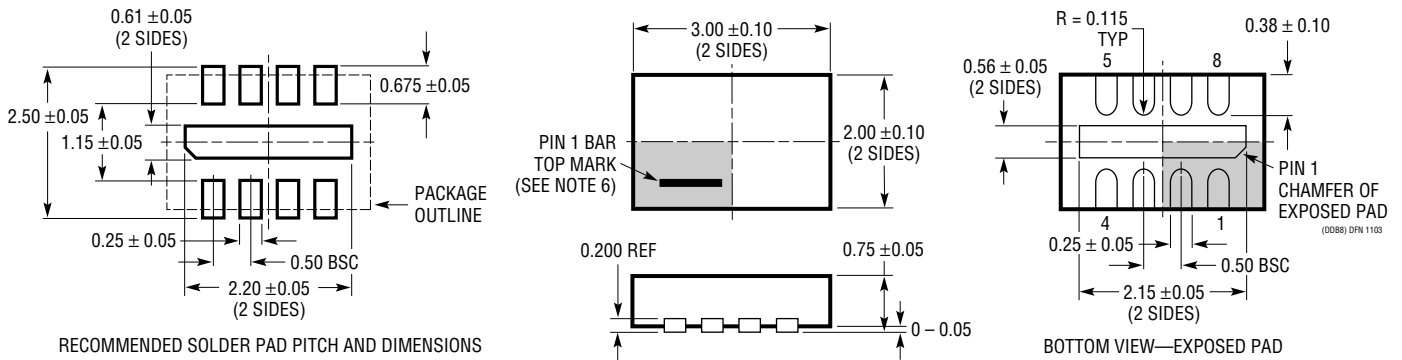


Figure 14. Layout of the Evaluation Board

PACKAGE DESCRIPTION

DDB Package 8-Lead Plastic DFN (3mm × 2mm) (Reference LTC DWG # 05-08-1702)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

NOTE:

1. DRAWING CONFORMS TO VERSION (WECD-1) IN JEDEC PACKAGE OUTLINE M0-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE