GSM/EDGE Optimized, High Linearity Direct Quadrature Modulator

FEATURES

- **Optimized Image Rejection for 850MHz to 965MHz**
- **High OIP3: +22.9dBm at 900MHz**
- **Low Output Noise Floor at 5MHz Offset:**
  No RF: –159.4dBm/Hz
  P_{OUT} = 4dBm: –153dBm/Hz
- **Integrated LO Buffer and LO Quadrature Phase Generator**
- **50Ω AC-Coupled Single-Ended LO and RF Ports**
- **50Ω DC Interface to Baseband Inputs**
- **Low Carrier Leakage: –43dBm at 900MHz**
- **High Image Rejection: –52dBc at 900MHz**
- 16-Lead 4mm × 4mm QFN Package

APPLICATIONS

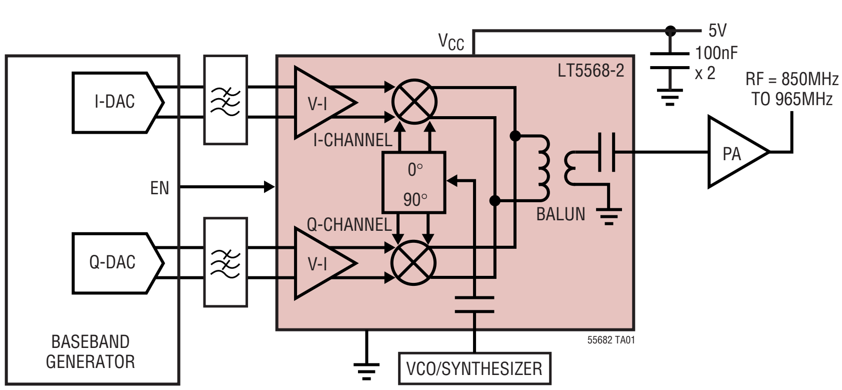
- Infrastructure Tx for GSM/Cellular Bands
- Image Reject Up-Converters for Cellular Bands
- Low-Noise Variable Phase-Shifter for 700MHz to 1050MHz Local Oscillator Signals
- RFID Reader

DESCRIPTION

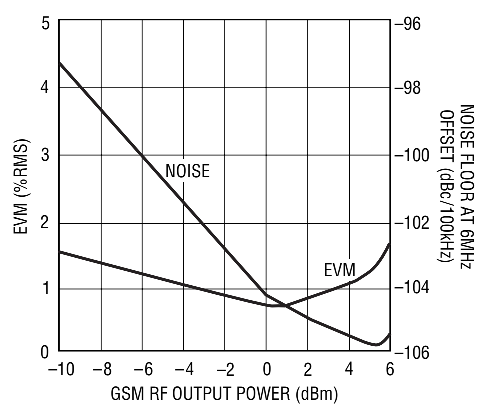
The LT®5568-2 is a direct I/Q modulator designed for high performance wireless applications, including wireless infrastructure. It allows direct modulation of an RF signal using differential baseband I and Q signals. It supports GSM, EDGE, CDMA, CDMA2000 and other systems that operate in the 850MHz to 965MHz band. It may be configured as an image reject upconverting mixer, by applying 90° phase-shifted signals to the I and Q inputs. The I/Q baseband inputs consist of voltage-to-current converters that in turn drive double-balanced mixers. The outputs of these mixers are summed and applied to an on-chip RF transformer, which converts the differential mixer signals to a 50Ω single-ended output. The four balanced I and Q baseband input ports are intended for DC coupling from a source with a common mode voltage level of about 0.5V. The LO path consists of an LO buffer with single-ended input, and precision quadrature generators that produce the LO drive for the mixers. The supply voltage range is 4.5V to 5.25V.

TYPICAL APPLICATION

850MHz to 965MHz Direct Conversion Transmitter Application



GSM EVM and Noise vs RF Output Power at 900MHz



ABSOLUTE MAXIMUM RATINGS

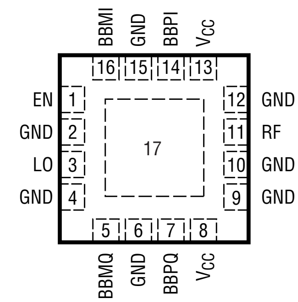
(Note 1)

Supply Voltage 5.5V
Common Mode Level of BBPI, BBMI and
BBPQ, BBMQ 2.5V
Operating Ambient Temperature
(Note 2) .... –40°C to 85°C
Storage Temperature Range................... –65°C to 125°C
Voltage on Any Pin
Not to Exceed...................... –500mV to V_{CC} + 500mV

CAUTION: This part is sensitive to ESD. It is very important that proper ESD precautions be observed when handling the LT5568-2.

PIN CONFIGURATION

TOP VIEW



UF PACKAGE
16-LEAD (4mm × 4mm) PLASTIC QFN
T_{JMAX} = 125°C, θ_{JA} = 37°C/W
EXPOSED PAD (PIN 17) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT5568-2EUF#PBF	LT5568-2EUF#TRPBF	55682	16-Lead (4mm × 4mm) Plastic QFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

V_{CC} = 5V, EN = High, T_A = 25°C, f_{LO} = 900MHz, f_{RF} = 902MHz, P_{LO} = 0dBm. BBPI, BBMI, BBPQ, BBMQ inputs 0.54V_{DC}, Baseband Input Frequency = 2MHz, I&Q 90° shifted (upper side-band selection). $P_{RF, OUT}$ = –10dBm, unless otherwise noted. (Note 3)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
RF Output (RF)						
f_{RF}	RF Frequency Range RF Frequency Range	–3dB Bandwidth –1dB Bandwidth		0.6 to 1.1 0.7 to 1		GHz GHz
$S_{22, ON}$	RF Output Return Loss	EN = High (Note 6)		–16		dB
$S_{22, OFF}$	RF Output Return Loss	EN = Low (Note 6)		–18		dB
NFloor	RF Output Noise Floor	No Input Signal (Note 8) P_{OUT} = 4dBm (Note 9) P_{OUT} = 4dBm (Note 10)		–159.4 –153 –152.6		dBm/Hz dBm/Hz dBm/Hz
G_P	Conversion Power Gain	$P_{OUT}/P_{IN, I\&Q}$	–9	–6.8	–3	dB
G_V	Conversion Voltage Gain	20 • Log ($V_{OUT, 50\Omega}/V_{IN, DIFF, I\ or\ Q}$)		–6.8		dB
P_{OUT}	Absolute Output Power	$1V_{P-P\ DIFF}$ CW Signal, I and Q		–2.8		dBm
$G_{3LO\ vs\ LO}$	3 • LO Conversion Gain Difference	(Note 17)		–23		dB
OP1dB	Output 1dB Compression	(Note 7)		8.6		dBm
OIP2	Output 2nd Order Intercept	(Notes 13, 14)		59		dBm
OIP3	Output 3rd Order Intercept	(Notes 13, 15)		22.9		dBm

ELECTRICAL CHARACTERISTICS

V_{CC} = 5V, EN = High, T_A = 25°C, f_{LO} = 900MHz, f_{RF} = 902MHz, P_{LO} = 0dBm. BBPI, BBMI, BBPQ, BBMQ inputs 0.54V_{DC}, Baseband Input Frequency = 2MHz, I&Q 90° shifted (upper side-band selection). $P_{RF, OUT}$ = –10dBm, unless otherwise noted. (Note 3)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
IR	Image Rejection	f_{BB} = 100kHz (Note 16)		–52		dBc
LOFT	Carrier Leakage (LO Feedthrough)	EN = High, P_{LO} = 0dBm (Note 16) EN = Low, P_{LO} = 0dBm (Note 16)		–43 –65		dBm dBm
LO Input (LO)						
f_{LO}	LO Frequency Range			0.6 to 1.1		GHz
P_{LO}	LO Input Power		–10	0	5	dBm
$S_{11, ON}$	LO Input Return Loss	EN = High (Note 6)		–15		dB
$S_{11, OFF}$	LO Input Return Loss	EN = Low (Note 6)		–2.5		dB
NF_{LO}	LO Input Referred Noise Figure	(Note 5) at 900MHz		14.7		dB
G_{LO}	LO to RF Small Signal Gain	(Note 5) at 900MHz		14.7		dB
$IIP3_{LO}$	LO Input 3rd Order Intercept	(Note 5) at 900MHz		–3		dBm
Baseband Inputs (BBPI, BBMI, BBPQ, BBMQ)						
BW_{BB}	Baseband Bandwidth	–3dB Bandwidth		380		MHz
V_{CMBB}	DC Common Mode Voltage	(Note 4)		0.54		V
$R_{IN, SE}$	Single-Ended Input Resistance	(Note 4)		47		Ω
P_{LO2BB}	Carrier Feedthrough on BB	P_{OUT} = 0 (Note 4)		–38		dBm
IP1dB	Input 1dB Compression Point	Differential Peak-to-Peak (Notes 7, 18)		4.3		$V_{P-P, DIFF}$
Power Supply (V_{CC})						
V_{CC}	Supply Voltage		4.5	5	5.25	V
$I_{CC, ON}$	Supply Current	EN = High	80	110	145	mA
$I_{CC, OFF}$	Supply Current, Sleep Mode	EN = 0V			100	µA
t_{ON}	Turn-On Time	EN = Low to High (Note 11)		0.3		µs
t_{OFF}	Turn-Off Time	EN = High to Low (Note 12)		1.4		µs
Enable (EN), Low = Off, High = On						
Enable	Input High Voltage Input High Current	EN = High EN = 5V	1.0	 245		V µA
Sleep	Input Low Voltage Input Low Current	EN = Low EN = 0V		 0.01	0.5	V µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Specifications over the –40°C to 85°C temperature range are assured by design, characterization and correlation with statistical process controls.

Note 3: Tests are performed as shown in the configuration of Figure 7.

Note 4: On each of the four baseband inputs BBPI, BBMI, BBPQ and BBMQ.

Note 5: V(BBPI) – V(BBMI) = 1V_{DC}, V(BBPQ) – V(BBMQ) = 1V_{DC}.

Note 6: Maximum value within 850MHz to 965MHz.

Note 7: An external coupling capacitor is used in the RF output line.

Note 8: At 20MHz offset from the LO signal frequency.

Note 9: At 20MHz offset from the CW signal frequency.

Note 10: At 5MHz offset from the CW signal frequency.

Note 11: RF power is within 10% of final value.

Note 12: RF power is at least 30dB lower than in the ON state.

Note 13: Baseband is driven by 2MHz and 2.1MHz tones. Drive level is set in such a way that the two resulting RF tones are –10dBm each.

Note 14: IM2 measured at LO frequency + 4.1MHz.

Note 15: IM3 measured at LO frequency + 1.9MHz and LO frequency + 2.2MHz.

Note 16: Amplitude average of the characterization data set without image or LO feedthrough nulling (unadjusted).

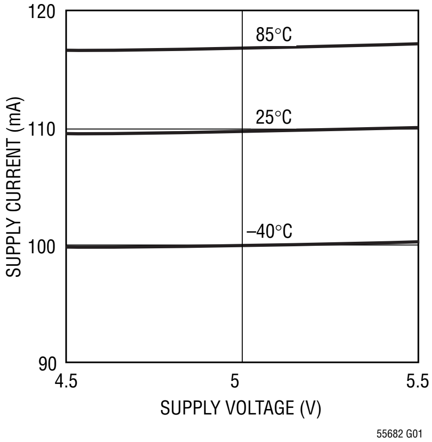
Note 17: The difference in conversion gain between the spurious signal at f = 3 • LO – BB versus the conversion gain at the desired signal at f = LO + BB for BB = 2MHz and LO = 900MHz.

Note 18: The input voltage corresponding to the output P1dB.

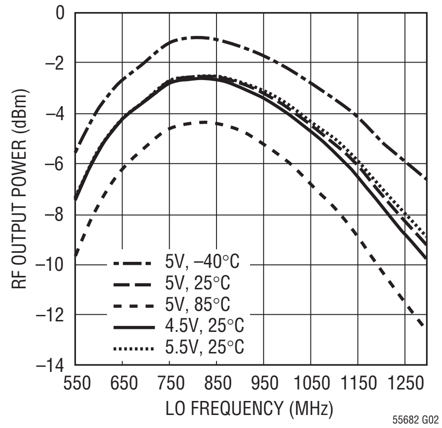
TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 5V, EN = High, T_A = 25°C, f_{LO} = 900MHz, P_{LO} = 0dBm. BBPI, BBMI, BBPQ, BBMQ inputs 0.54V_{DC}, Baseband Input Frequency f_{BB} = 2MHz, I&Q 90° shifted. f_{RF} = f_{BB} + f_{LO} (upper sideband selection). $P_{RF, OUT}$ = –10dBm (–10dBm/tone for 2-tone measurements), unless otherwise noted. (Note 3)

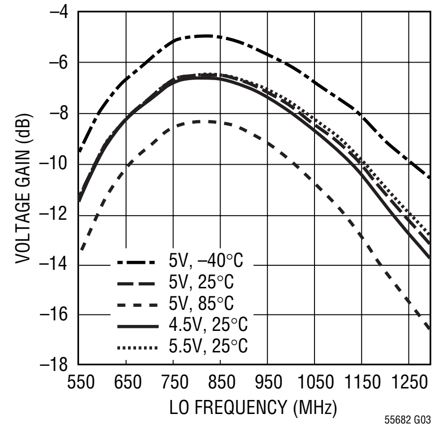
Supply Current vs Supply Voltage



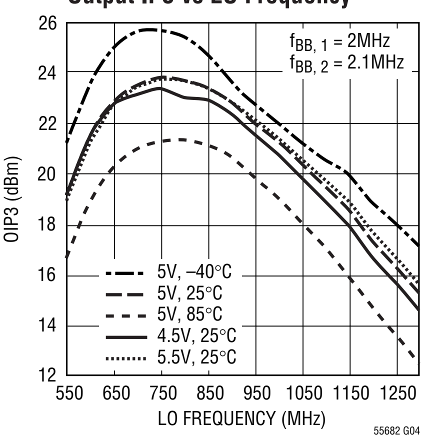
RF Output Power vs LO Frequency at 1V_{P-P} Differential Baseband Drive



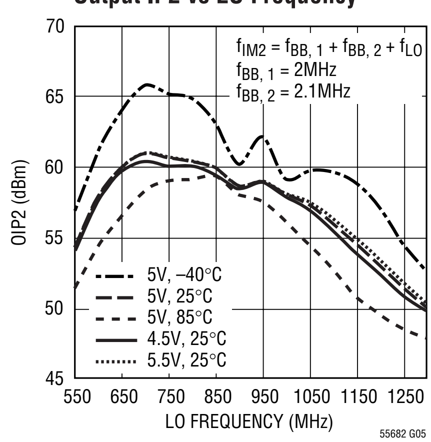
Voltage Gain vs LO Frequency



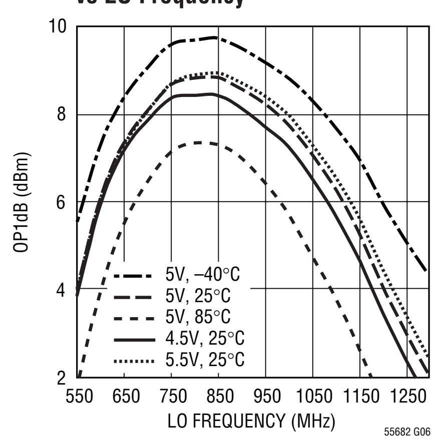
Output IP3 vs LO Frequency



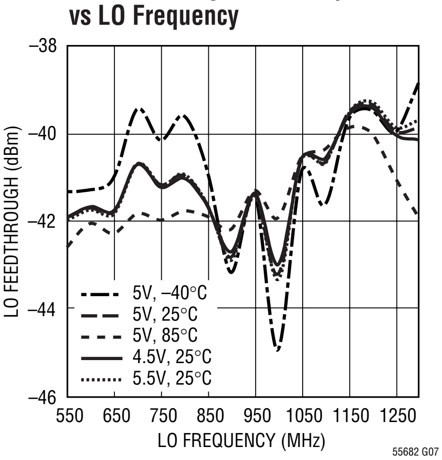
Output IP2 vs LO Frequency



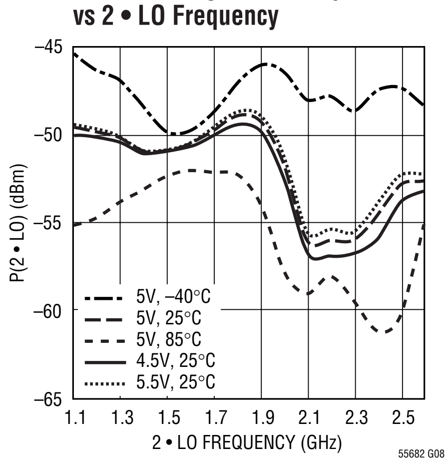
Output 1dB Compression vs LO Frequency



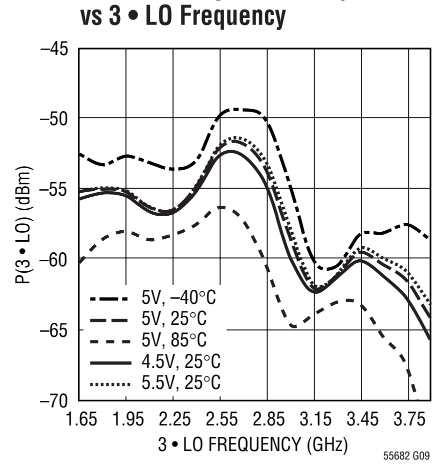
LO Feedthrough to RF Output vs LO Frequency



2 • LO Leakage to RF Output vs 2 • LO Frequency



3 • LO Leakage to RF Output vs 3 • LO Frequency



TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 5V, EN = High, T_A = 25°C, f_{LO} = 900MHz, P_{LO} = 0dBm. BBPI, BBMI, BBPQ, BBMQ inputs 0.54V_{DC}, Baseband Input Frequency f_{BB} = 2MHz, I&Q 90° shifted. f_{RF} = f_{BB} + f_{LO} (upper sideband selection). $P_{RF, OUT}$ = –10dBm (–10dBm/tone for 2-tone measurements), unless otherwise noted. (Note 3)

Noise Floor vs RF Frequency

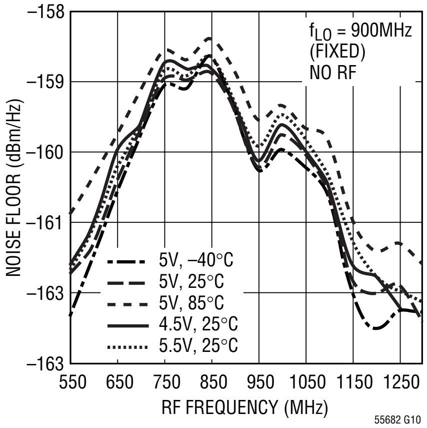
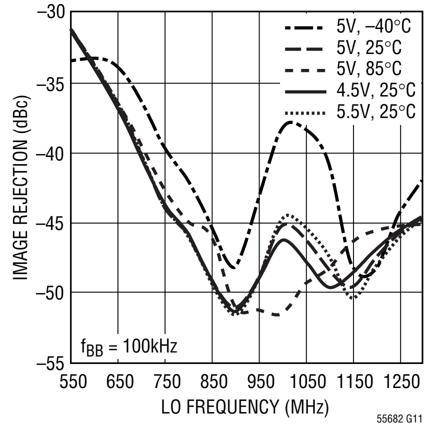
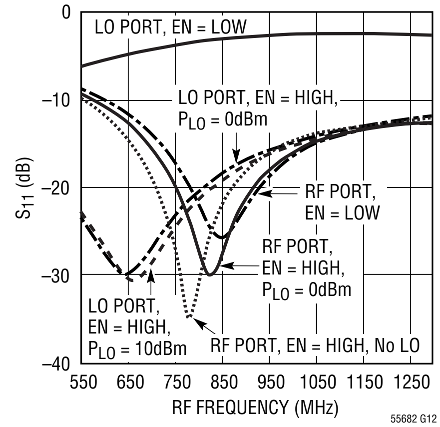


Image Rejection vs LO Frequency



LO and RF Port Return Loss vs RF Frequency



LO Feedthrough to RF Output vs LO Input Power

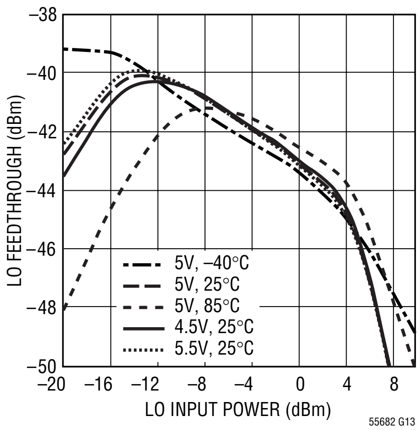
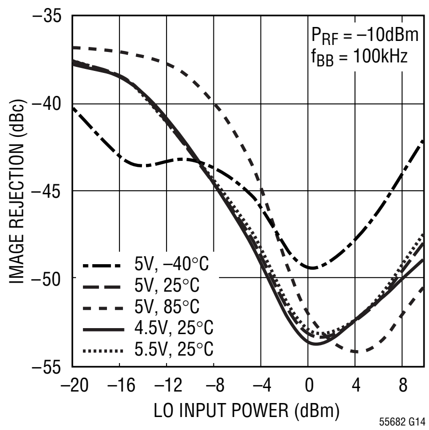
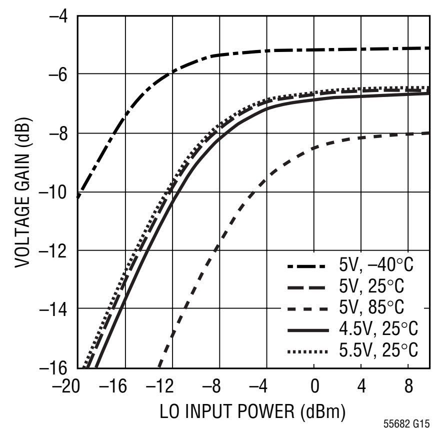


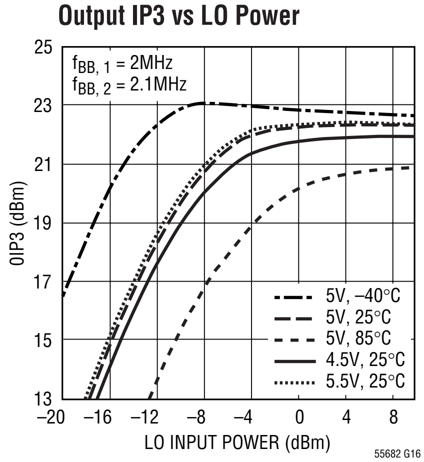
Image Rejection vs LO Input Power



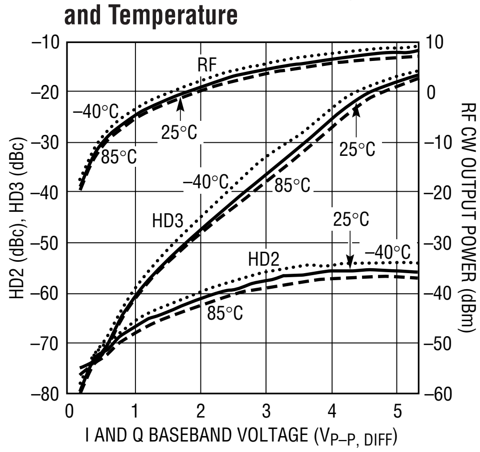
Voltage Gain vs LO Power



Output IP3 vs LO Power



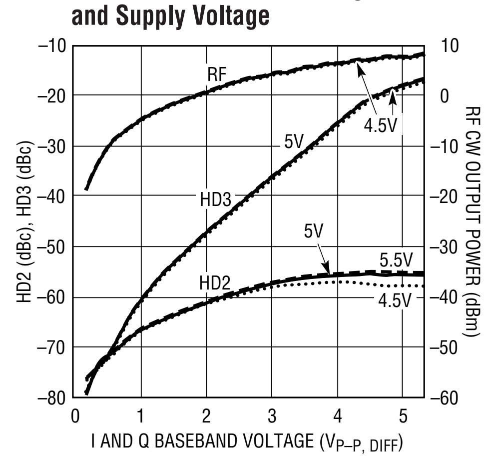
RF CW Output Power, HD2 and HD3 vs CW Baseband Voltage and Temperature



HD2 = MAX POWER AT f_{LO} + 2 • f_{BB} OR f_{LO} – 2 • f_{BB}
HD3 = MAX POWER AT f_{LO} + 3 • f_{BB} OR f_{LO} – 3 • f_{BB}

55682 G17

RF CW Output Power, HD2 and HD3 vs CW Baseband Voltage and Supply Voltage



HD2 = MAX POWER AT f_{LO} + 2 • f_{BB} OR f_{LO} – 2 • f_{BB}
HD3 = MAX POWER AT f_{LO} + 3 • f_{BB} OR f_{LO} – 3 • f_{BB}

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TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 5V, EN = High, T_A = 25°C, f_{LO} = 900MHz, P_{LO} = 0dBm. BBPI, BBMI, BBPQ, BBMQ inputs 0.54V_{DC}, Baseband Input Frequency f_{BB} = 2MHz, I&Q 90° shifted. f_{RF} = f_{BB} + f_{LO} (upper sideband selection). $P_{RF,\ OUT}$ = –10dBm (–10dBm/tone for 2-tone measurements), unless otherwise noted. (Note 3)

LO Feedthrough to RF Output vs CW Baseband Voltage

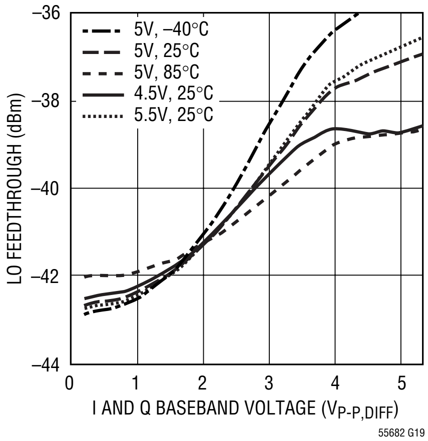
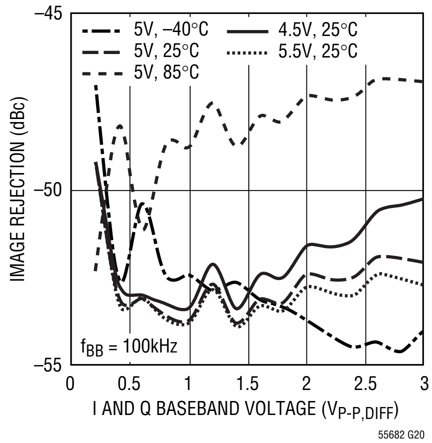
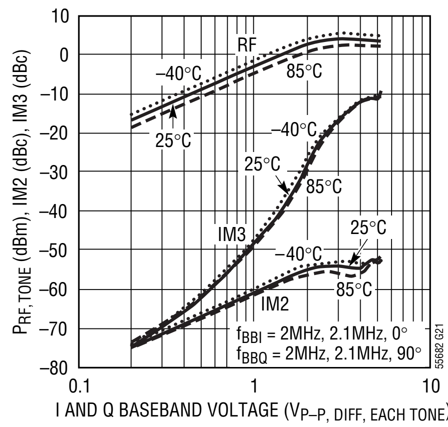


Image Rejection vs CW Baseband Voltage

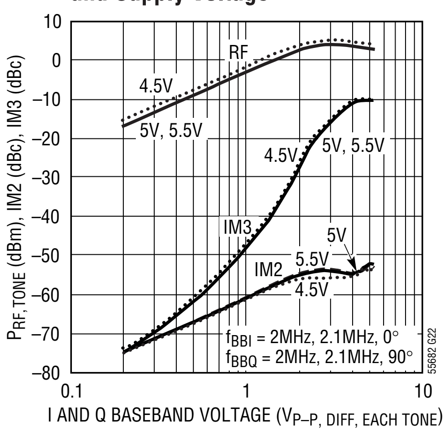


RF Two-Tone Power (Each Tone), IM2 and IM3 vs Baseband Voltage and Temperature



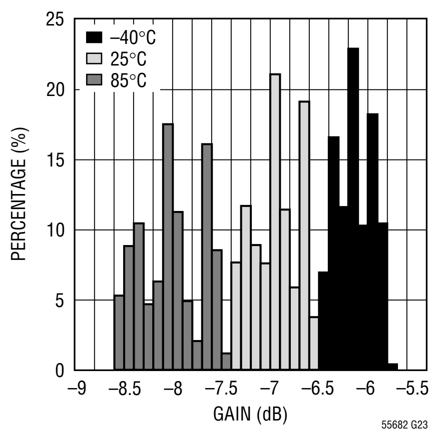
IM2 = POWER AT f_{LO} + 4.1MHz
IM3 = MAX POWER AT f_{LO} + 1.9MHz OR f_{LO} + 2.2MHz

RF Two-Tone Power (Each Tone), IM2 and IM3 vs Baseband Voltage and Supply Voltage

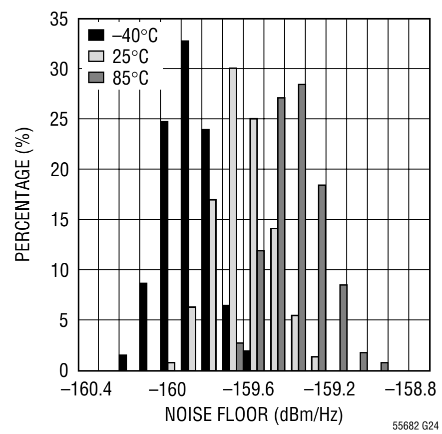


IM2 = POWER AT f_{LO} + 4.1MHz
IM3 = MAX POWER AT f_{LO} + 1.9MHz OR f_{LO} + 2.2MHz

Gain Distribution



Noise Floor Distribution



LO Leakage Distribution

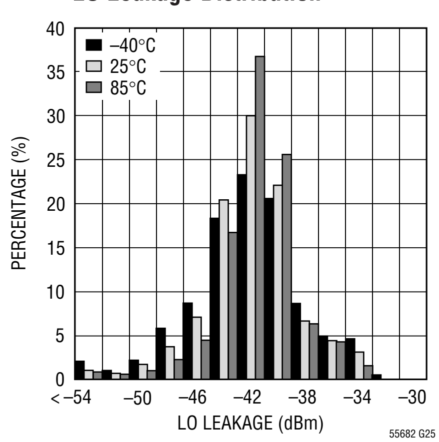
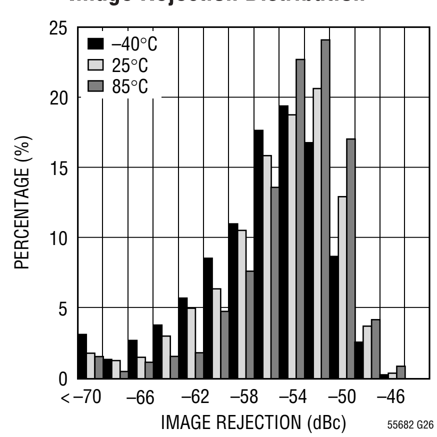


Image Rejection Distribution



PIN FUNCTIONS

EN (Pin 1): Enable Input. When the enable pin voltage is higher than 1V, the IC is turned on. When the input voltage is less than 0.5V, the IC is turned off.

GND (Pins 2, 4, 6, 9, 10, 12, 15): Ground. Pins 6, 9, 15 and 17 (exposed pad) are connected to each other internally. Pins 2 and 4 are connected to each other internally and function as the ground return for the LO signal. Pins 10 and 12 are connected to each other internally and function as the ground return for the on-chip RF balun. For best RF performance, pins 2, 4, 6, 9, 10, 12, 15 and the Exposed Pad 17 should be connected to the printed circuit board ground plane.

LO (Pin 3): LO Input. The LO input is an AC-coupled single-ended input with approximately 50Ω input impedance at RF frequencies. Externally applied DC voltage should be within the range –0.5V to V_{CC} + 0.5V in order to avoid turning on ESD protection diodes.

BBPQ, BBMQ (Pins 7, 5): Baseband Inputs for the Q-channel, each 50Ω input impedance. Internally biased at about 0.54V. Applied voltage must stay below 2.5V.

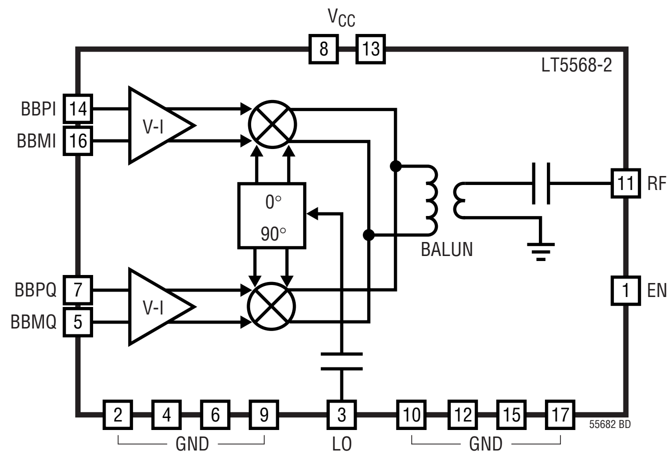
V_{CC} (Pins 8, 13): Power Supply. Pins 8 and 13 are connected to each other internally. It is recommended to use 0.1µF capacitors for decoupling to ground on each of these pins.

RF (Pin 11): RF Output. The RF output is an AC-coupled single-ended output with approximately 50Ω output impedance at RF frequencies. Externally applied DC voltage should be within the range –0.5V to V_{CC} + 0.5V in order to avoid turning on ESD protection diodes.

BBPI, BBMI (Pins 14, 16): Baseband Inputs for the I-channel, each with 50Ω input impedance. Internally biased at about 0.54V. Applied voltage must stay below 2.5V.

Exposed Pad (Pin 17): Ground. This pin must be soldered to the printed circuit board ground plane.

BLOCK DIAGRAM



APPLICATIONS INFORMATION

The LT5568-2 consists of I and Q input differential voltage-to-current converters, I and Q up-conversion mixers, an RF output balun, an LO quadrature phase generator and LO buffers.

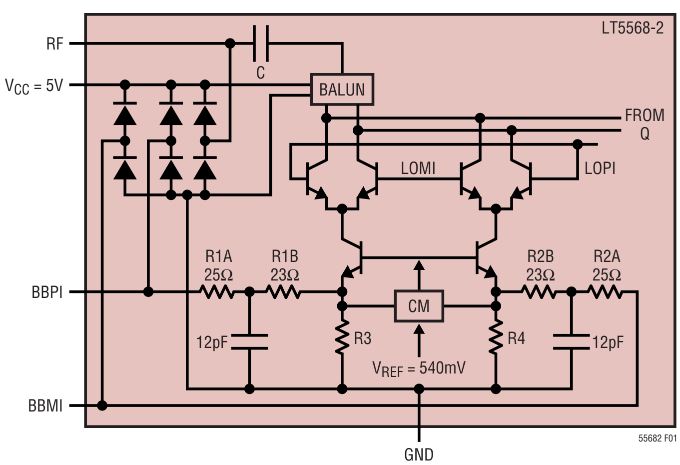


Figure 1. Simplified Circuit Schematic of the LT5568-2 (Only I-Half is Drawn)

External I and Q baseband signals are applied to the differential baseband input pins, BBPI, BBMI, and BBPQ, BBMQ. These voltage signals are converted to currents and translated to RF frequency by means of double-balanced up-converting mixers. The mixer outputs are combined in an RF output balun, which also transforms the output impedance to 50Ω. The center frequency of the resulting RF signal is equal to the LO signal frequency. The LO input drives a phase shifter which splits the LO signal into in-phase and quadrature LO signals. These LO signals are then applied to on-chip buffers which drive the up-conversion mixers. Both the LO input and RF output are single-ended, 50Ω-matched and AC coupled.

Baseband Interface

The baseband inputs (BBPI, BBMI), (BBPQ, BBMQ) present a differential input impedance of about 100Ω. At each of the four baseband inputs, a first-order lowpass filter using 25Ω

APPLICATIONS INFORMATION

and 12pF to ground is incorporated (see Figure 1), which limits the baseband bandwidth to approximately 330MHz (–1dB point). The common mode voltage is about 0.54V and is approximately constant over temperature.

It is important that the applied common mode voltage level of the I and Q inputs is about 0.54V in order to properly bias the LT5568-2. Some I/Q test generators allow setting the common mode voltage independently. In this case, the common mode voltage of those generators must be set to 0.27V to match the LT5568-2 internal bias, because for DC signals, there is no –6dB source-load voltage division (see Figure 2).

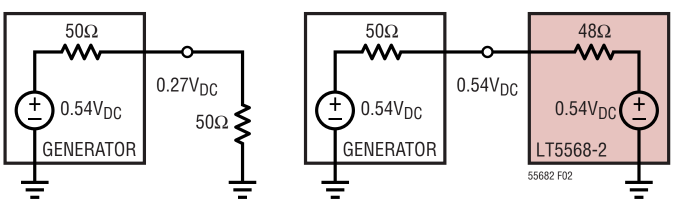


Figure 2. DC Voltage Levels for a Generator Programmed at $0.27V_{DC}$ for a 50Ω Load and the LT5568-2 as a Load

The baseband inputs should be driven differentially; otherwise, the even-order distortion products will degrade the overall linearity severely. Typically, a DAC will be the signal source for the LT5568-2. Reconstruction filters should be placed between the DAC output and the LT5568-2's baseband inputs. In Figure 3, a typical baseband interface schematic for GSM is drawn. It shows a ground referenced DAC output interface followed by a 3rd order active OpAmp RC lowpass filter with a 400kHz cutoff frequency (–3dB). The DAC in this example sources a current from 0mA to 20mA, with a voltage compliance range of at least 0V to 1V. This interface is DC coupled, which allows adjustment of the DAC's differential output current to minimize the LO feedthrough. The voltage swing at the LT5568-2 baseband inputs is about $2V_{P\text{-}P,DIFF}$, which results in a 1.2dBm GSM RF output power at 900MHz with noise floor of –154.3dBm/Hz at 6MHz offset (= –104.3dBm/100kHz). The RMS EVM is about 0.6%. The LT1819, which houses two LT1818s, can be used instead of U2 and U3. The total current in the positive supply is about 157mA and the current in the negative supply is about 40mA.

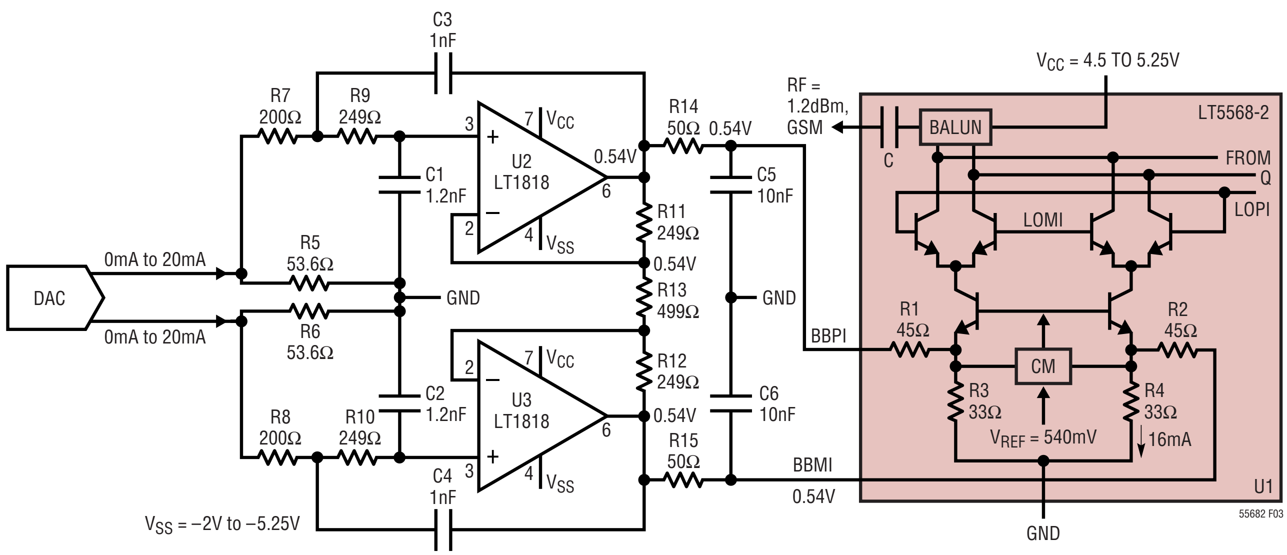


Figure 3. LT5568-2 GSM Baseband Interface with 3rd Order Lowpass Filter and Ground Referenced DAC (Only I-Channel is Shown)

APPLICATIONS INFORMATION

LO Section

The internal LO input amplifier performs single-ended to differential conversion of the LO input signal. Figure 4 shows the equivalent circuit schematic of the LO input.

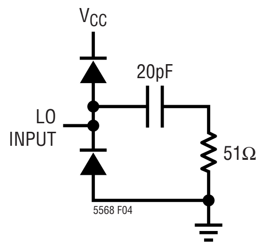


Figure 4. Equivalent Circuit Schematic of the LO Input

The internal, differential LO signal is then split into in-phase and quadrature (90° phase shifted) signals that drive LO buffer sections. These buffers drive the double balanced I and Q mixers. The phase relationship between the LO input and the internal in-phase LO and quadrature LO signals is fixed, and is independent of start-up conditions. The internal phase shifters are designed to deliver accurate quadrature signals. For LO frequencies significantly below 650MHz or above 1.25GHz, however, the quadrature accuracy will diminish, causing the image rejection to degrade. The LO pin input impedance is about 50Ω, and the recommended LO input power is 0dBm. For lower LO input power, the gain, OIP2, OIP3 and noise floor at P_{RF} = 4dBm will degrade, especially for P_{LO} below –2dBm and at T_A = 85°C. For high LO input power (e.g., +5dBm), the image rejection will degrade with no improvement in linearity or gain. Harmonics present on the LO signal can degrade the image rejection because they can introduce a small excess phase shift in the internal phase splitter. For the second (at 1.8GHz) and third harmonics (at 2.7GHz) at –20dBc, the resulting signal at the image frequency is about –61dBc or lower, corresponding to an excess phase shift of much less than 1 degree. For the second and third LO harmonics at –10dBc, the introduced signal at the image frequency is about –51dBc. Higher harmonics than the third will have less impact. The LO return loss typically will be better than 11dB over the 700MHz to 1.05GHz range. Table 1 shows the LO port input impedance vs frequency.

Table 1. LO Port Input Impedance vs Frequency for EN = High and P_{LO} = 0dBm

Frequency MHz	Input Impedance Ω	S_{11} Mag	S_{11} Angle
500	47.5 + j12.1	0.126	95.0
600	59.4 + j8.4	0.115	37.8
700	66.2 – j1.14	0.140	–3.41
800	67.2 – j13.4	0.185	–31.7
900	61.1 – j23.9	0.232	–53.2
1000	53.3 – j26.8	0.252	–68.7
1100	48.2 – j26.1	0.258	–79.4
1200	42.0 – j27.4	0.297	–90.0

If the part is in shutdown mode, the input impedance of the LO port will be different. The LO input impedance for EN = Low is given in Table 2.

Table 2. LO Port Input Impedance vs Frequency for EN = Low and P_{LO} = 0dBm

Frequency MHz	Input Impedance Ω	S_{11} Mag	S_{11} Angle
500	33.6 + j41.3	0.477	85.4
600	59.8 + j69.1	0.539	49.8
700	140 + j89.8	0.606	19.6
800	225 – j62.6	0.659	–6.8
900	92.9 – j128	0.704	–29.6
1000	39.8 – j95.9	0.735	–45.5
1100	22.8 – j72.7	0.755	–65.6
1200	16.0 – j57.3	0.763	–79.7

RF Section

After up-conversion, the RF outputs of the I and Q mixers are combined. An on-chip balun performs internal differential to single-ended output conversion, while transforming the output signal impedance to 50Ω. Table 3 shows the RF port output impedance vs frequency.

Table 3. RF Port Output Impedance vs Frequency for EN = High and P_{LO} = 0dBm

Frequency MHz	Input Impedance Ω	S_{22} Mag	S_{22} Angle
500	22.0 + j5.7	0.395	164.2
600	28.2 + j12.5	0.317	141.3
700	38.8 + j14.8	0.206	117.5
800	49.4 + j7.2	0.072	90.6
900	49.3 – j5.1	0.051	–94.7
1000	42.5 – j11.1	0.143	–117.0
1100	36.7 – j11.7	0.202	–130.7
1200	33.0 – j10.3	0.238	–141.6

APPLICATIONS INFORMATION

The RF output S_{22} with no LO power applied is given in Table 4.

Table 4. RF Port Output Impedance vs Frequency for EN = High and No LO Power Applied

Frequency MHz	Input Impedance Ω	S_{22} Mag	S_{22} Angle
500	22.7 + j5.6	0.381	164.0
600	29.7 + j11.6	0.290	142.0
700	40.5 + j11.6	0.164	121.9
800	47.3 + j2.2	0.037	139.6
900	44.1 – j6.7	0.094	–126.9
1000	38.2 – j9.8	0.171	–133.9
1100	34.0 – j9.4	0.218	–143.1
1200	31.5 – j7.8	0.245	–151.6

For EN = Low the S_{22} is given in Table 5.

Table 5. RF Port Output Impedance vs Frequency for EN = Low

Frequency MHz	Input Impedance Ω	S_{22} Mag	S_{22} Angle
500	21.2 + j5.4	0.409	164.9
600	26.6 + j12.5	0.340	142.5
700	36.6 + j16.6	0.241	118.1
800	49.2 + j11.6	0.116	87.4
900	52.9 – j2.0	0.034	–33.1
1000	46.4 – j11.2	0.121	–101.1
1100	39.3 – j13.2	0.188	–120.6
1200	34.4 – j12.1	0.231	–133.8

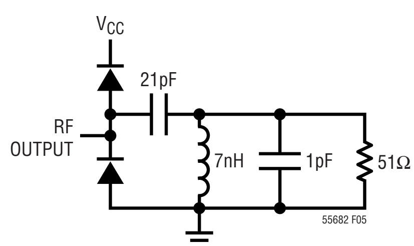


Figure 5. Equivalent Circuit Schematic of the RF Output

Note that an ESD diode is connected internally from the RF output to ground (see Figure 5). For strong output RF signal levels (higher than 3dBm), this ESD diode can degrade the linearity performance if the 50Ω termination impedance is connected directly to ground. To prevent this, a coupling capacitor can be inserted in the RF output line. This is strongly recommended during a 1dB compression measurement.

Enable Interface

Figure 6 shows a simplified schematic of the EN pin interface. The voltage necessary to turn on the LT5568-2 is 1V. To disable (shut down) the chip, the enable voltage must be below 0.5V. If the EN pin is not connected, the chip is disabled. This EN = Low condition is assured by the 75k on-chip pull-down resistor. It is important that the voltage at the EN pin does not exceed V_{CC} by more than 0.5V. If this should occur, the supply current could be sourced through the EN pin ESD protection diodes, which are not designed to carry the full supply current, and damage may result.

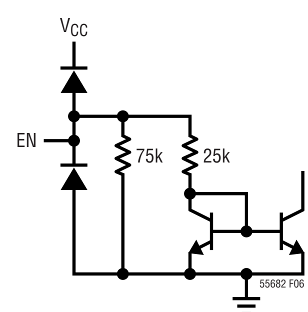


Figure 6. EN Pin Interface

APPLICATIONS INFORMATION

Evaluation Board

Figure 7 shows the evaluation board schematic. A good ground connection is required for the exposed pad. If this is not done properly, the RF performance will degrade. Additionally, the exposed pad provides heat sinking for the part and minimizes the possibility of the chip overheating.

R1 (optional) limits the EN pin current in the event that the EN pin is pulled high while the V_{CC} inputs are low. In Figures 8 and 9 the silk screens and the PCB board layout are shown.

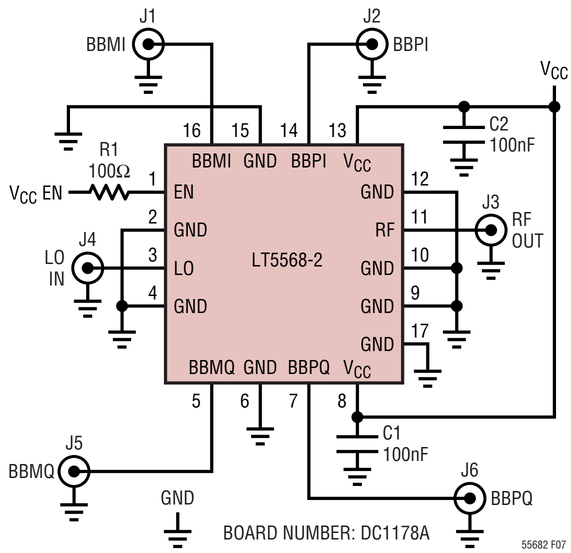


Figure 7. Evaluation Circuit Schematic

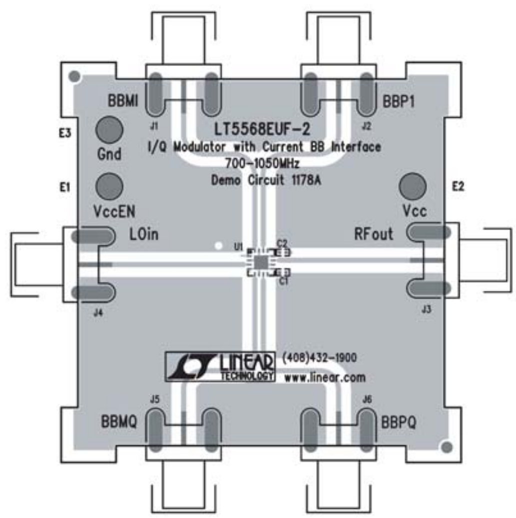


Figure 8. Component Side of Evaluation Board

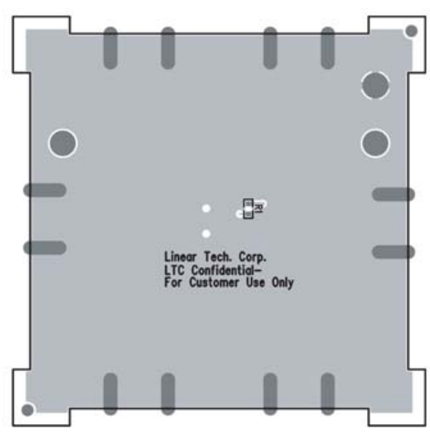


Figure 9. Bottom Side of Evaluation Board

APPLICATIONS INFORMATION

Application Measurements

The LT5568-2 is recommended for base-station applications using various modulation formats. Figure 10 shows a typical application. Figure 11 shows the ACPR performance for CDMA2000 using 1- and 3-carrier modulation. Figures 12 and 13 illustrate the 1- and 3-carrier CDMA2000 RF spectrum. To calculate ACPR, a correction is made for the spectrum analyzer noise floor. If the output power is high, the ACPR will be limited by the linearity performance of the part. If the output power is low, the ACPR will be limited by the noise performance of the part. In the middle, an optimum ACPR is observed.

Because of the LT5568-2's very high dynamic range, the test equipment can limit the accuracy of the ACPR measurement. See Application Note 99. Consult the factory for advice on the ACPR measurement, if needed.

The ACPR performance is sensitive to the amplitude match of the BBPI and BBMI (or BBPQ and BBMQ) inputs. This is because a difference in AC current amplitude will give rise to a difference in amplitude between the even-order harmonic products generated in the internal V-I converter. As a result, they will not cancel out entirely. Therefore, it is important to keep the currents in those pins exactly

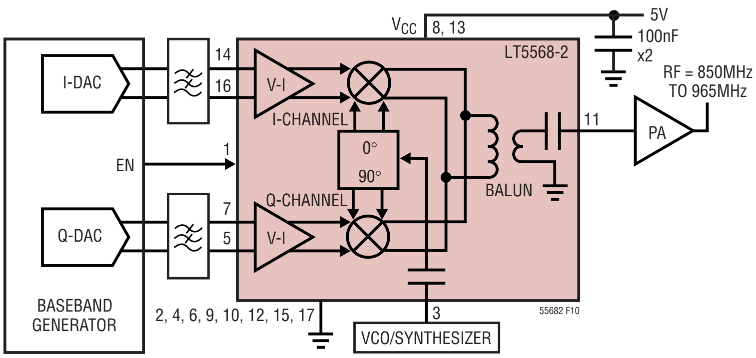


Figure 10. 850MHz to 965MHz Direct Conversion Transmitter Application

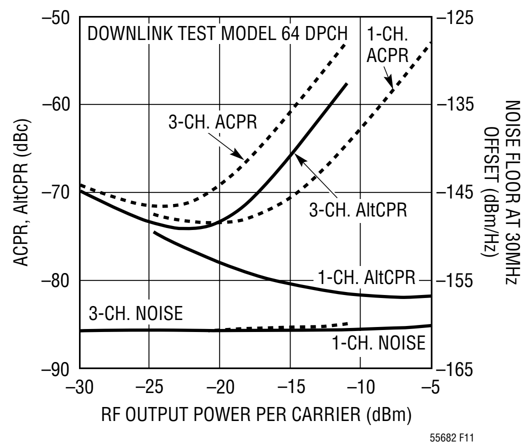


Figure 11. ACPR, AltCPR and Noise CDMA2000 Modulation

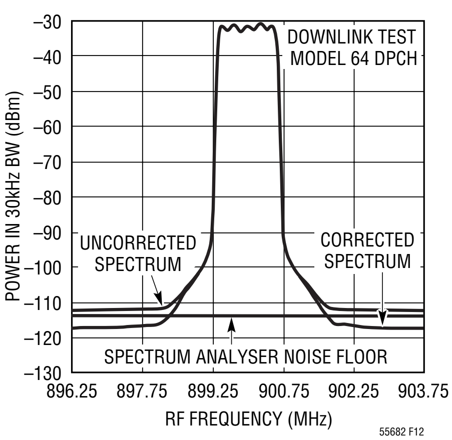


Figure 12. 1-Carrier CDMA2000 Spectrum

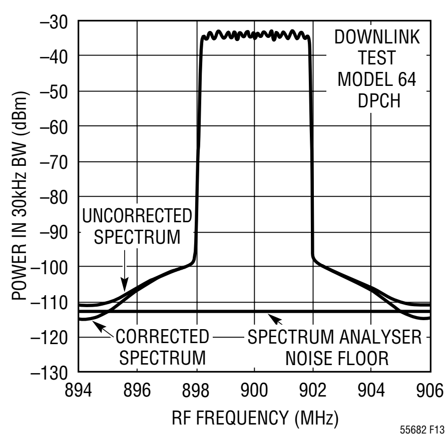


Figure 13. 3-Carrier CDMA2000 Spectrum

APPLICATIONS INFORMATION

the same (but of opposite sign). The current will enter the LT5568-2's common-base stage, and will flow to the mixer upper switches. This can be seen in Figure 1 where the internal circuit of the LT5568-2 is drawn.

After calibration when the temperature changes, the LO feedthrough and the image rejection performance will change. This is illustrated in Figure 14. The LO feedthrough and image rejection can also change as a function of the baseband drive level, as is depicted in Figure 15. In Figure 16 the GSM EVM and noise performance vs RF output power is drawn.

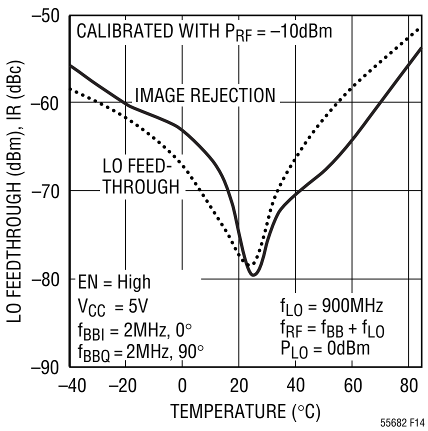


Figure 14. LO Feedthrough and Image Rejection vs Temperature after Calibration at 25°C

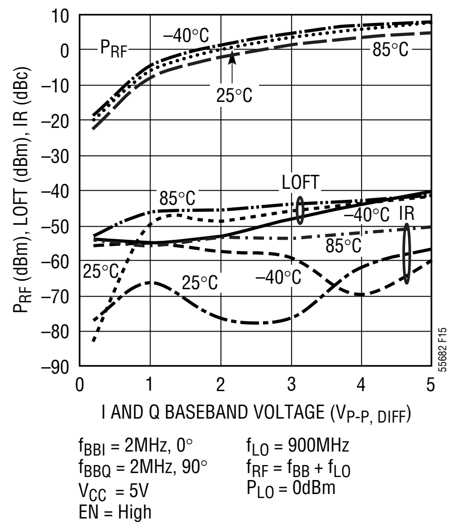


Figure 15. LO Feedthrough and Image Rejection vs Baseband Drive Voltage after Calibration at 25°C

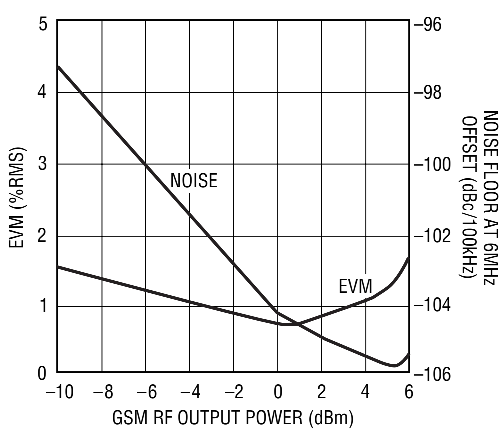
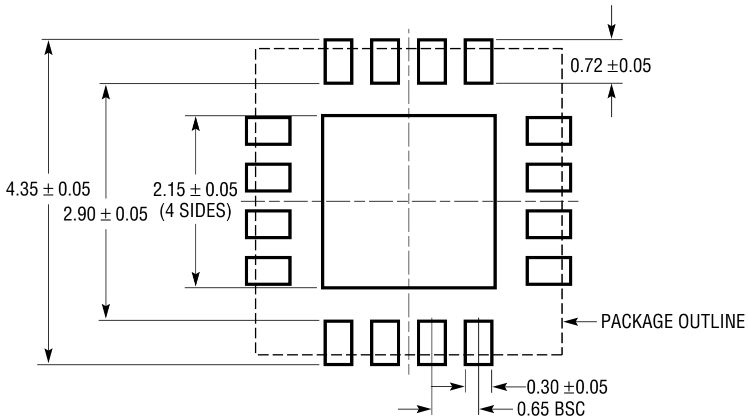


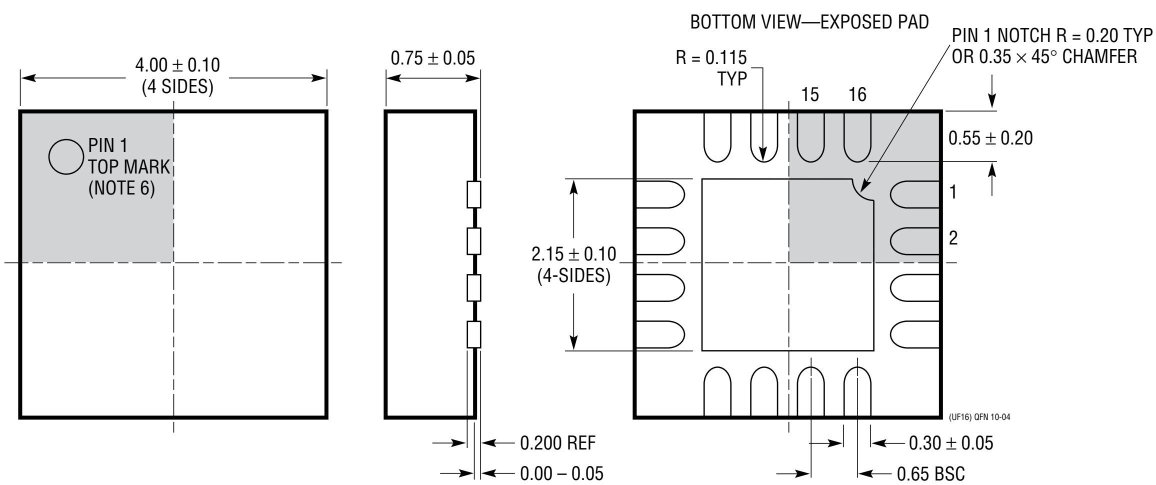
Figure 16. GSM EVM and Noise vs RF Output Power at 900MHz

PACKAGE DESCRIPTION

UF Package
16-Lead Plastic QFN (4mm × 4mm)
(Reference LTC DWG # 05-08-1692)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGGC)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE