

High Linearity Direct Conversion Quadrature Demodulator

FEATURES

- **Input Frequency Range: 0.8GHz to 2.7GHz***
- **50Ω Single-Ended RF and LO Ports**
- **High IIP3: 28dBm at 900MHz, 22.6dBm at 1.9GHz**
- **High IIP2: 54.1dBm at 900MHz, 60dBm at 1.9GHz**
- **Input P1dB: 13.2dBm at 900MHz**
- **I/Q Gain Mismatch: 0.04dB Typical**
- **I/Q Phase Mismatch: 0.4° Typical**
- **Low Output DC Offsets**
- **Noise Figure: 12.8dB at 900MHz, 12.7dB at 1.9GHz**
- **Conversion Gain: 3dB at 900MHz, 4.2dB at 1.9GHz**
- **Very Few External Components**
- **Shutdown Mode**
- **16-Lead QFN 4mm × 4mm Package with Exposed Pad**

APPLICATIONS

- Cellular/PCS/UMTS Infrastructure
- RFID Reader
- High Linearity Direct Conversion I/Q Receiver

DESCRIPTION

The LT[®]5575 is an 800MHz to 2.7GHz direct conversion quadrature demodulator optimized for high linearity receiver applications. It is suitable for communications receivers where an RF signal is directly converted into I and Q baseband signals with bandwidth up to 490MHz. The LT5575 incorporates balanced I and Q mixers, LO buffer amplifiers and a precision, high frequency quadrature phase shifter. The integrated on-chip broadband transformers provide 50Ω single-ended interfaces at the RF and LO inputs. Only a few external capacitors are needed for its application in an RF receiver system.

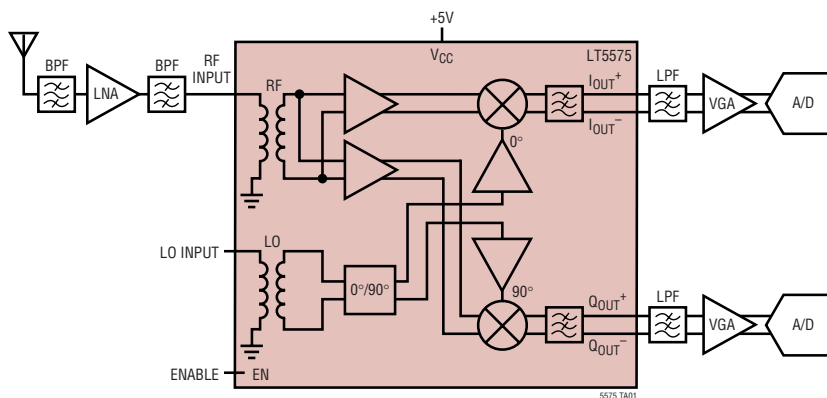
The high linearity of the LT5575 provides excellent spur-free dynamic range for the receiver. This direct conversion demodulator can eliminate the need for intermediate frequency (IF) signal processing, as well as the corresponding requirements for image filtering and IF filtering. Channel filtering can be performed directly at the outputs of the I and Q channels. These outputs can interface directly to channel-select filters (LPFs) or to baseband amplifiers.

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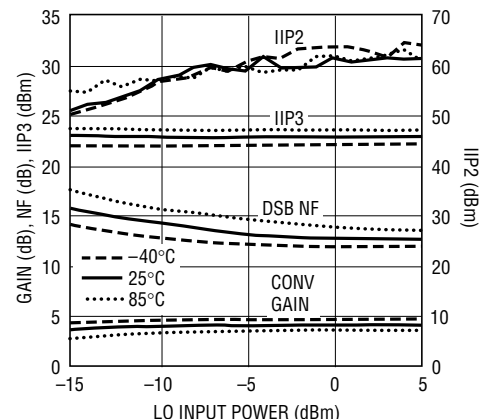
*Operation over a wider frequency range is possible with reduced performance. Consult the factory.

TYPICAL APPLICATION

High Signal-Level I/Q Demodulator for Wireless Infrastructure



Conversion Gain, NF, IIP3 and IIP2 vs LO Input Power at 1900MHz



5575 TA01b

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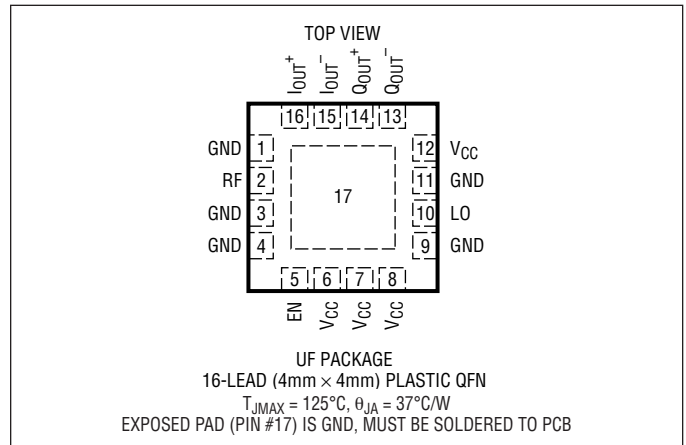
ABSOLUTE MAXIMUM RATINGS

(Note 1)

| | |
|-------------------------------------|--------------------------|
| Power Supply Voltage | 5.5V |
| Enable Voltage | -0.3V to $V_{CC} + 0.3V$ |
| LO Input Power | 10dBm |
| RF Input Power | 20dBm |
| RF Input DC Voltage..... | $\pm 0.1V$ |
| LO Input DC Voltage | $\pm 0.1V$ |
| Operating Ambient Temperature | -40°C to 85°C |
| Storage Temperature Range..... | -65°C to 125°C |
| Maximum Junction Temperature | 125°C |

CAUTION: This part is sensitive to electrostatic discharge (ESD). It is very important that proper ESD precautions be observed when handling the LT5575.

PIN CONFIGURATION



ORDER INFORMATION

| LEAD FREE FINISH | TAPE AND REEL | PART MARKING | PACKAGE DESCRIPTION | TEMPERATURE RANGE |
|------------------|-----------------|--------------|-------------------------|-------------------|
| LT5575EUF#PBF | LT5575EUF#TRPBF | 5575 | 16-Lead (4mm x 4mm) QFN | -40°C to 85°C |

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on nonstandard lead based finish parts.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>
For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandreel/>

DC ELECTRICAL CHARACTERISTICS $V_{CC} = +5V, T_A = 25^\circ C$, unless otherwise noted. (Note 3)

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|-----------------------------------|-----|-----|------|------------------|
| Supply Voltage | | 4.5 | | 5.25 | V |
| Supply Current | | | 132 | 155 | mA |
| Shutdown Current | EN = Low | | < 1 | 100 | μA |
| Turn On Time | | | 120 | | ns |
| Turn Off Time | | | 750 | | ns |
| EN = High (On) | | 2 | | | V |
| EN = Low (Off) | | | | 1 | V |
| EN Input Current | $V_{ENABLE} = 5V$ | | 120 | | μA |
| Output DC Offset Voltage ($ I_{OUT+} - I_{OUT-} , Q_{OUT+} - Q_{OUT-} $) | $f_{LO} = 1900MHz, P_{LO} = 0dBm$ | | < 9 | | mV |
| Output DC Offset Variation vs Temperature | -40°C to 85°C | | 38 | | $\mu V/^\circ C$ |

AC ELECTRICAL CHARACTERISTICS Test circuit shown in Figure 1. (Notes 2, 3)

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|-------------------------------|--|-----|------------|-----|-------|
| RF Input Frequency Range | No External Matching (High Band) | | 1.5 to 2.7 | | GHz |
| | With External Matching (Low Band, Mid Band) | | 0.8 to 1.5 | | GHz |
| LO Input Frequency Range | No External Matching (High Band) | | 1.5 to 2.7 | | GHz |
| | With External Matching (Low Band, Mid Band) | | 0.8 to 1.5 | | GHz |
| Baseband Frequency Range | | | DC to 490 | | MHz |
| Baseband I/Q Output Impedance | Single-Ended | | 65Ω// 5pF | | |
| RF Input Return Loss | $Z_0 = 50\Omega$, 1.5GHz to 2.7GHz, Internally Matched | | >10 | | dB |
| LO Input Return Loss | $Z_0 = 50\Omega$, 1.5GHz to 2.7GHz, Internally Matched | | >10 | | dB |
| LO Input Power | | | -13 to 5 | | dBm |

AC ELECTRICAL CHARACTERISTICS $V_{CC} = +5V$, EN = High, $T_A = 25^\circ C$, $P_{RF} = -10dBm$ (-10dBm/tone for 2-tone IIP2 and IIP3 tests), Baseband Frequency = 1MHz (0.9MHz and 1.1MHz for 2-tone tests), $P_{LO} = 0dBm$, unless otherwise noted. (Notes 2, 3, 6)

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|-------------------------------------|-------------------------|-------|-------|-------|
| Conversion Gain | Voltage Gain, $R_{LOAD} = 1k\Omega$ | | | | |
| | $R_F = 900MHz$ (Note 5) | | 3 | | dB |
| | $R_F = 1900MHz$ | | 4.2 | | dB |
| | $R_F = 2100MHz$ | | 3.5 | | dB |
| | $R_F = 2500MHz$ | | 2 | | dB |
| Noise Figure (Double-Side Band, Note 4) | $R_F = 900MHz$ (Note 5) | | 12.8 | | dB |
| | $R_F = 1900MHz$ | | 12.7 | | dB |
| | $R_F = 2100MHz$ | | 13.6 | | dB |
| | $R_F = 2500MHz$ | | 15.7 | | dB |
| | Input 3rd-Order Intercept | $R_F = 900MHz$ (Note 5) | | 28 | |
| $R_F = 1900MHz$ | | | 22.6 | | dBm |
| $R_F = 2100MHz$ | | | 22.7 | | dBm |
| $R_F = 2500MHz$ | | | 23.3 | | dBm |
| Input 2nd-Order Intercept | | $R_F = 900MHz$ (Note 5) | | 54.1 | |
| | $R_F = 1900MHz$ | | 60 | | dBm |
| | $R_F = 2100MHz$ | | 56 | | dBm |
| | $R_F = 2500MHz$ | | 52.3 | | dBm |
| | Input 1dB Compression | $R_F = 900MHz$ (Note 5) | | 13.2 | |
| $R_F = 1900MHz$ | | | 11.2 | | dBm |
| $R_F = 2100MHz$ | | | 11 | | dBm |
| $R_F = 2500MHz$ | | | 12.3 | | dBm |
| I/Q Gain Mismatch | | $R_F = 900MHz$ (Note 5) | | 0.03 | |
| | $R_F = 1900MHz$ | | 0.01 | | dB |
| | $R_F = 2100MHz$ | | 0.04 | | dB |
| | $R_F = 2500MHz$ | | 0.04 | | dB |
| | I/Q Phase Mismatch | $R_F = 900MHz$ (Note 5) | | 0.5 | |
| $R_F = 1900MHz$ | | | 0.4 | | ° |
| $R_F = 2100MHz$ | | | 0.6 | | ° |
| $R_F = 2500MHz$ | | | 0.2 | | ° |
| LO to RF Leakage | | $R_F = 900MHz$ (Note 5) | | -60.8 | |
| | $R_F = 1900MHz$ | | -64.6 | | dBm |
| | $R_F = 2100MHz$ | | -60.2 | | dBm |
| | $R_F = 2500MHz$ | | -51.2 | | dBm |

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AC ELECTRICAL CHARACTERISTICS $V_{CC} = +5V$, $EN = High$, $T_A = 25^\circ C$, $P_{RF} = -10dBm$ ($-10dBm/$ tone for 2-tone IIP2 and IIP3 tests), Baseband Frequency = 1MHz (0.9MHz and 1.1MHz for 2-tone tests), $P_{LO} = 0dBm$, unless otherwise noted. (Notes 2, 3, 6)

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|--------------------|-------------------------|-----|------|-----|-------|
| RF to LO Isolation | $R_F = 900MHz$ (Note 5) | | 59.7 | | dBc |
| | $R_F = 1900MHz$ | | 57.1 | | dBc |
| | $R_F = 2100MHz$ | | 59.5 | | dBc |
| | $R_F = 2500MHz$ | | 53.1 | | dBc |

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Tests are performed as shown in the configuration of Figure 1.

Note 3: Specifications over the $-40^\circ C$ to $85^\circ C$ temperature range are assured by design, characterization and correlation with statistical process control.

Note 4: DSB Noise Figure is measured with a small-signal noise source at the baseband frequency of 15MHz without any filtering on the RF input and no other RF signal applied.

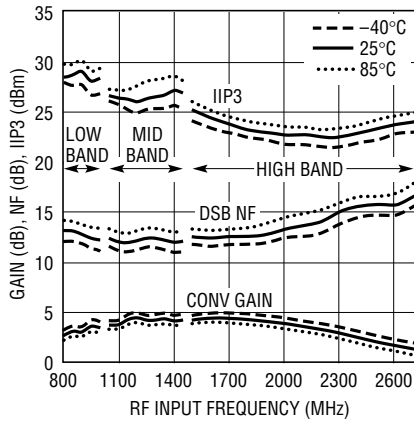
Note 5: 900MHz performance is measured with external RF and LO matching. The optional output capacitors C1-C4 (10pF) are also used for best IIP2 performance.

Note 6: For these measurements, the complementary outputs (e.g., I_{OUT+} , I_{OUT-}) were combined using a 180° phase shift combiner.

Note 7: Large-signal noise figure is measured at an output frequency of 198.7MHz with RF input signal at $f_{LO} - 1MHz$. Both RF and LO input signals are appropriately bandpass filtered, as well as baseband output.

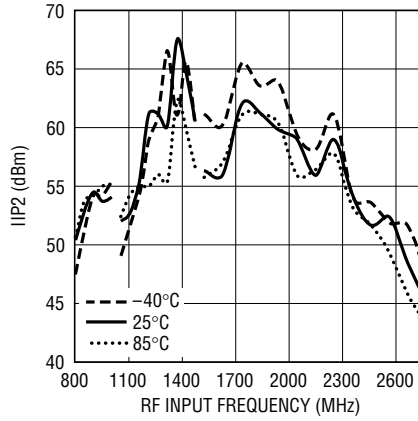
TYPICAL AC PERFORMANCE CHARACTERISTICS $V_{CC} = 5V$, $EN = High$, $T_A = 25^\circ C$, $P_{RF} = -10dBm$ (-10dBm/tone for 2-tone IIP2 and IIP3 tests), $f_{BB} = 1MHz$ (0.9MHz and 1.1MHz for 2-tone tests), $P_{LO} = 0dBm$, unless otherwise noted. Test Circuit Shown in Figure 1 (Note 6).

Conversion Gain, NF and IIP3 vs Frequency



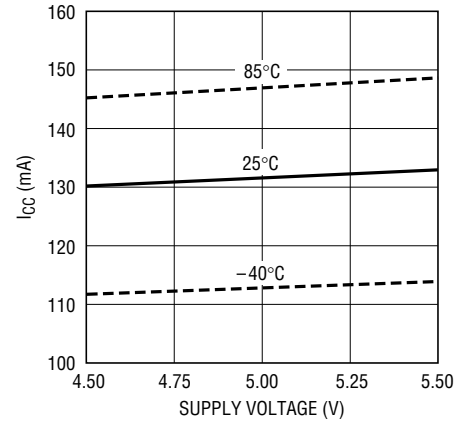
5575 G01

IIP2 vs Frequency



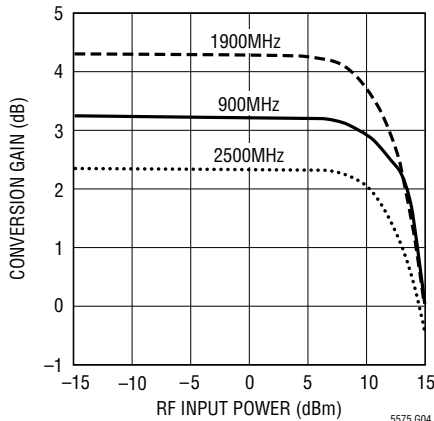
5575 G02

Supply Current vs Supply Voltage



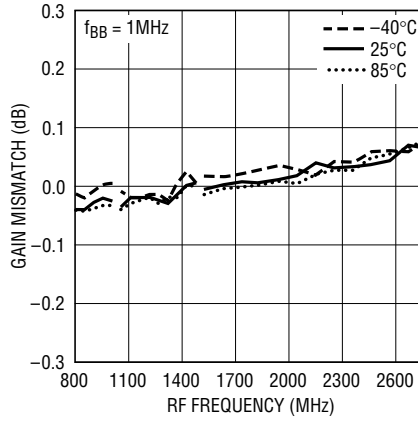
5575 G03

Conversion Gain vs RF Input Power



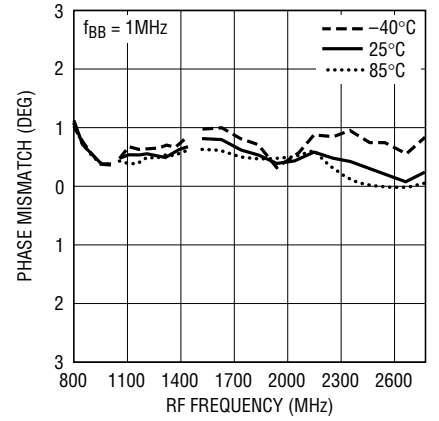
5575 G04

I/Q Gain Mismatch vs RF Input Frequency



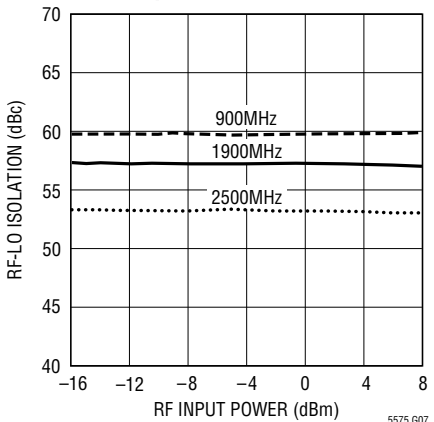
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I/Q Phase Mismatch vs RF Input Frequency



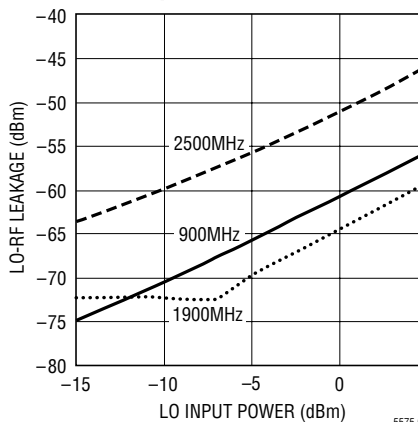
5575 G06

RF-LO Isolation vs RF Input Power



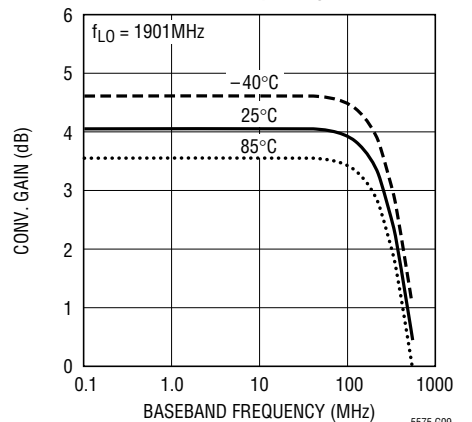
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LO-RF Leakage vs LO Input Power



5575 G08

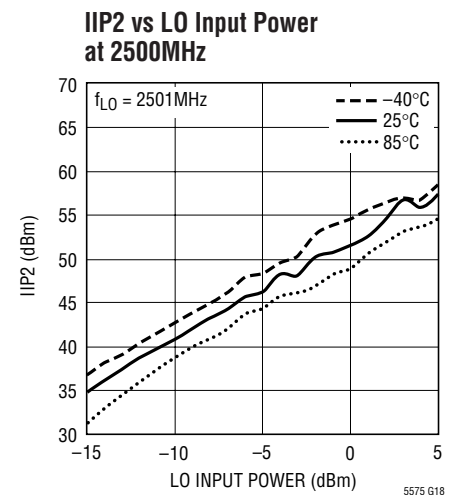
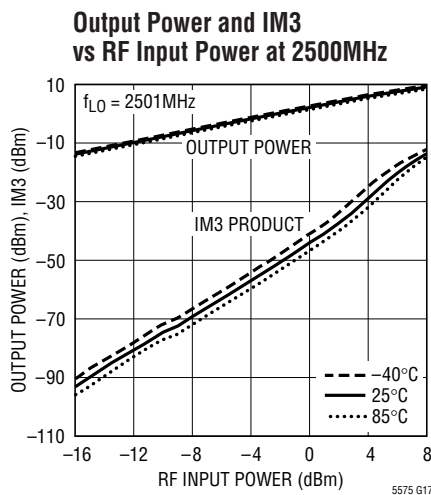
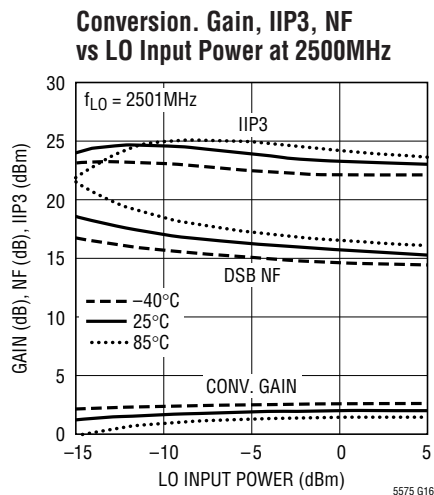
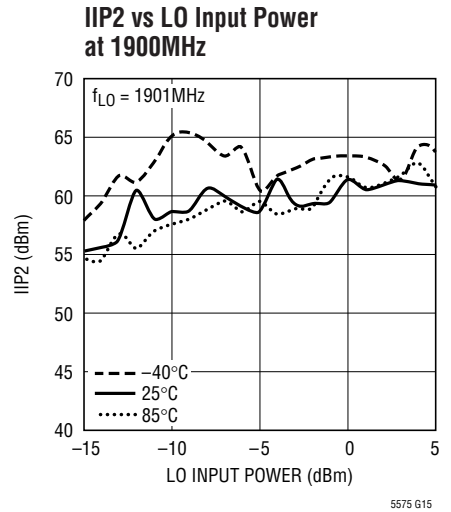
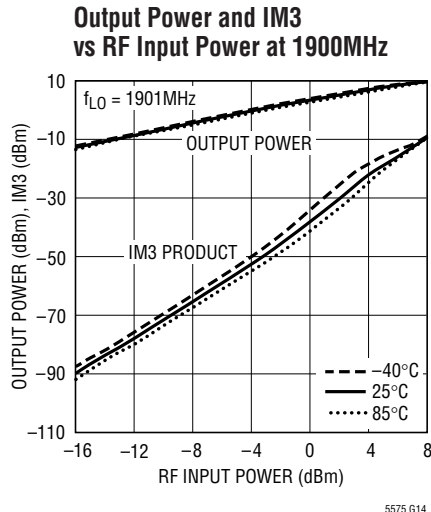
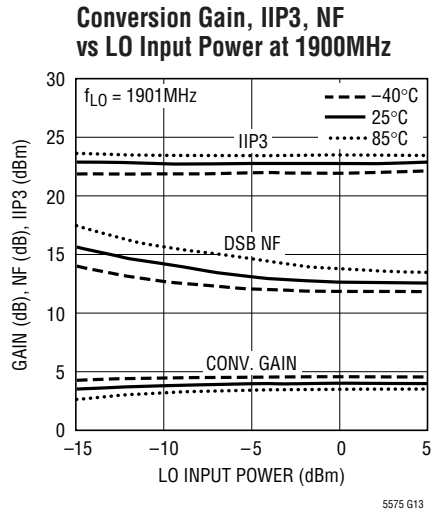
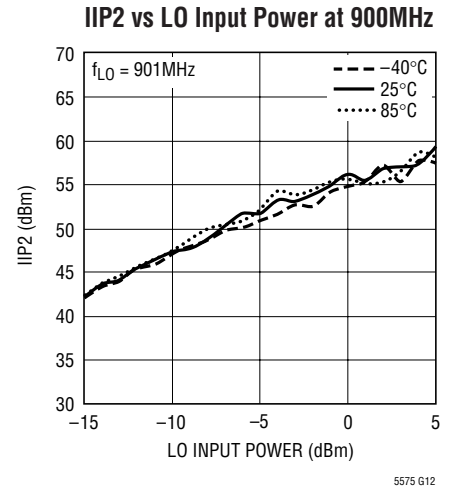
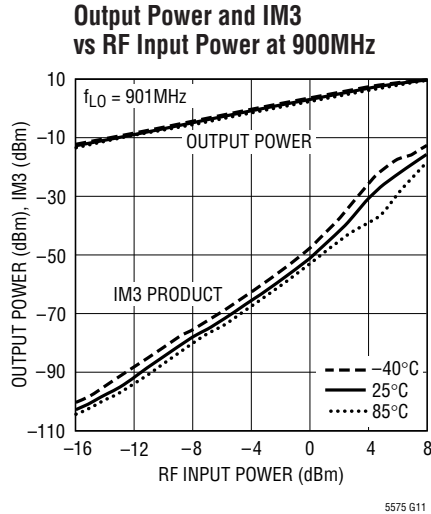
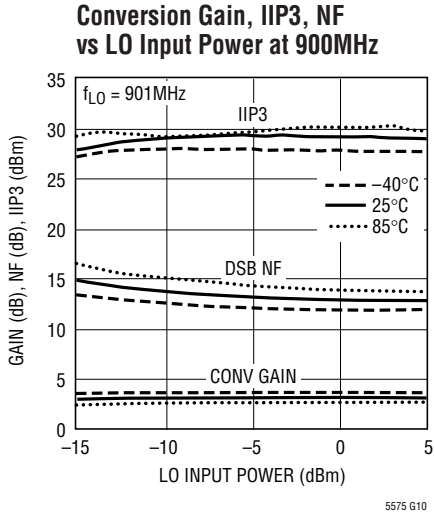
Conversion Gain vs Baseband Frequency



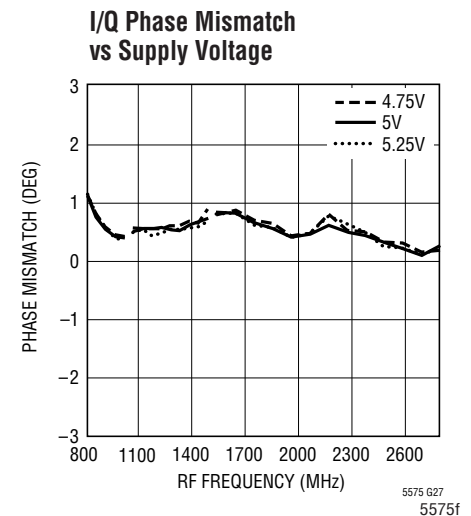
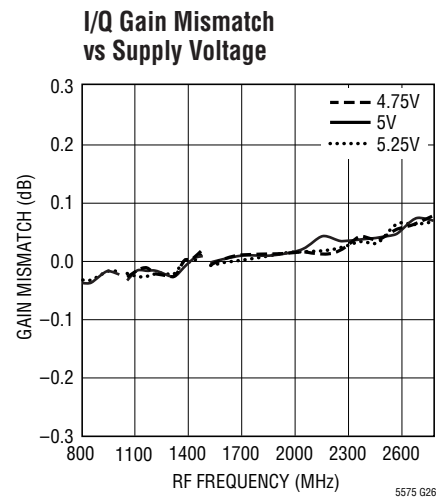
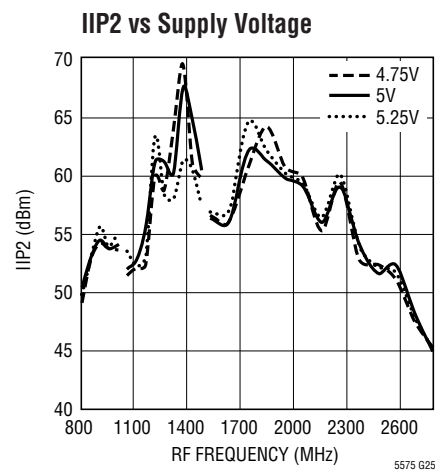
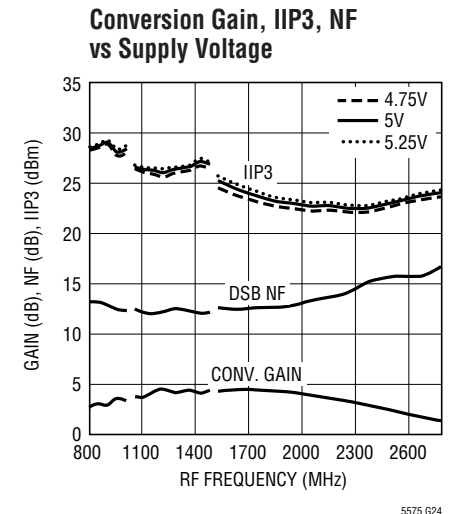
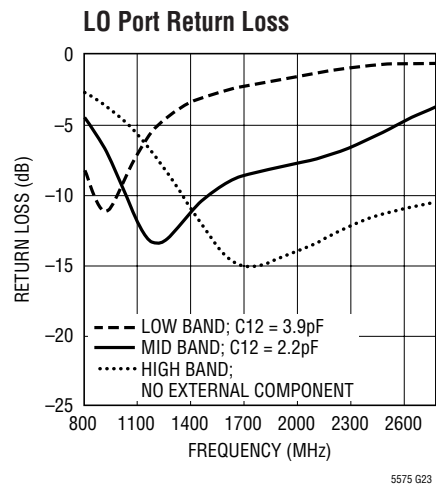
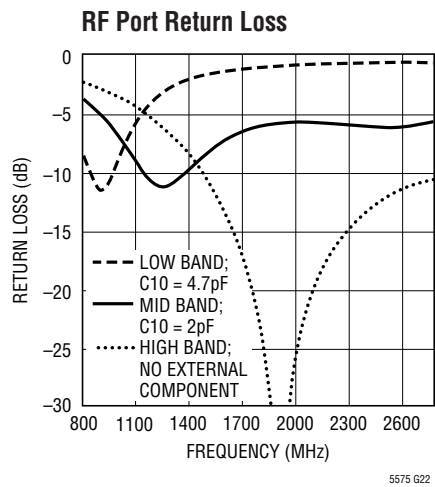
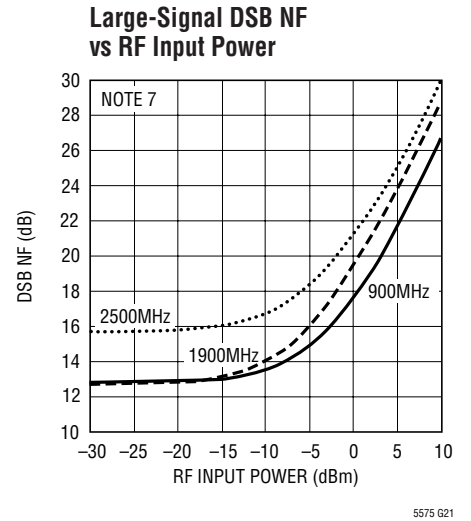
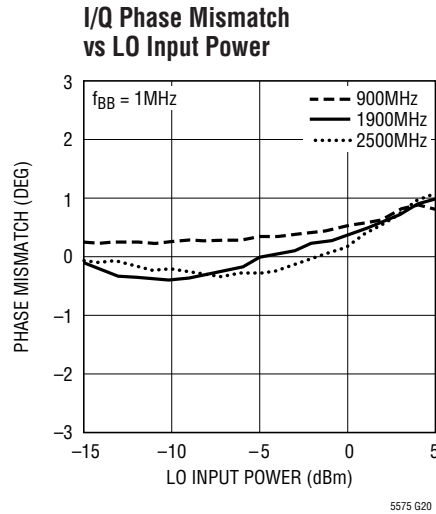
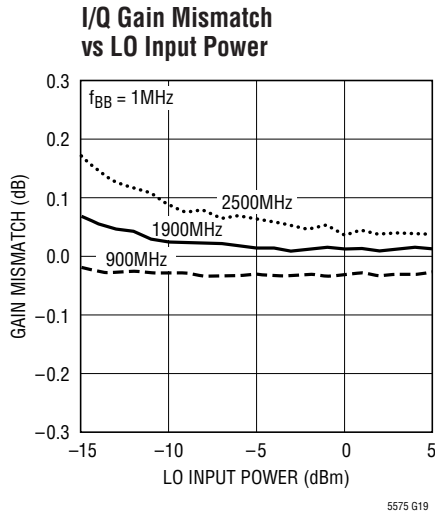
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TYPICAL AC PERFORMANCE CHARACTERISTICS $V_{CC} = 5V$, $EN = High$, $T_A = 25^\circ C$, $P_{RF} = -10dBm$ (-10dBm/tone for 2-tone IIP2 and IIP3 tests), $f_{BB} = 1MHz$ (0.9MHz and 1.1MHz for 2-tone tests), $P_{LO} = 0dBm$, unless otherwise noted. Test Circuit Shown in Figure 1 (Note 6).

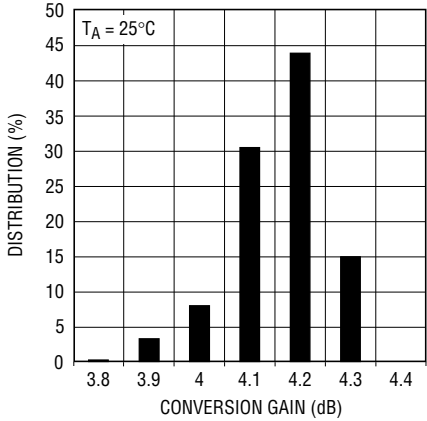


TYPICAL AC PERFORMANCE CHARACTERISTICS $V_{CC} = 5V$, $EN = High$, $T_A = 25^\circ C$, $P_{RF} = -10dBm$ ($-10dBm/$ tone for 2-tone IIP2 and IIP3 tests), $f_{BB} = 1MHz$ (0.9MHz and 1.1MHz for 2-tone tests), $P_{LO} = 0dBm$, unless otherwise noted. Test Circuit Shown in Figure 1 (Notes 6, 7).



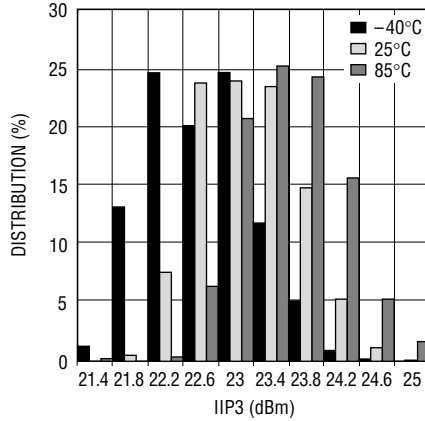
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Conversion Gain Distribution at 1900MHz



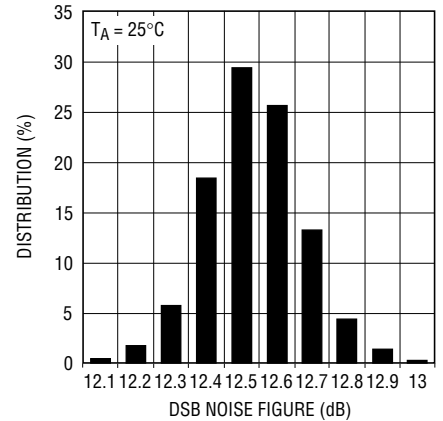
5575 G28

IIP3 Distribution at 1900MHz vs Temperature



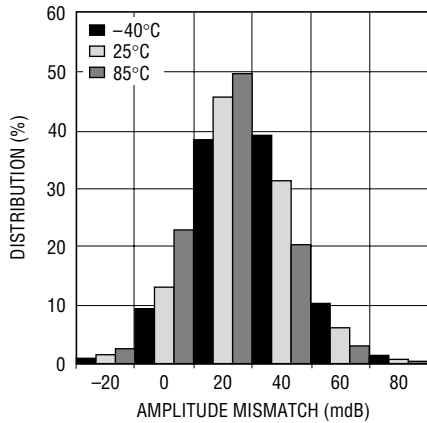
5575 G29

Noise Figure Distribution at 1900MHz



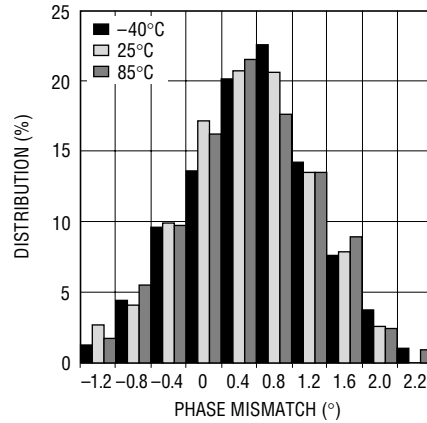
5575 G30

I/Q Amplitude Mismatch Distribution at 1900MHz vs Temperature



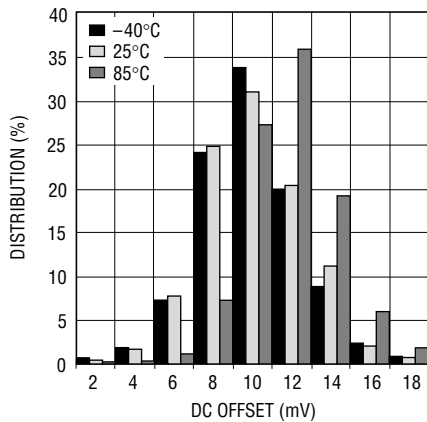
5575 G31

I/Q Phase Mismatch Distribution at 1900MHz vs Temperature



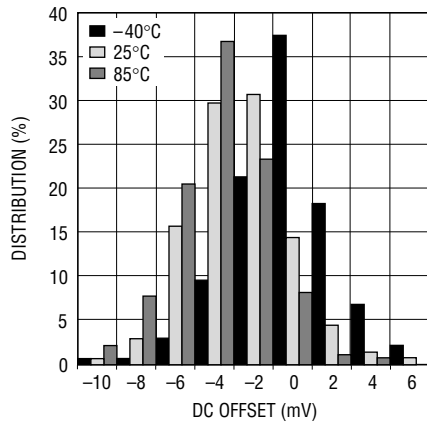
5575 G32

I-Output DC Offset Voltage Distribution vs Temperature



5575 G33

Q-Output DC Offset Voltage Distribution vs Temperature



5575 G34

PIN FUNCTIONS

GND (Pins 1, 3, 4, 9, 11): Ground pin.

RF (Pin 2): RF Input Pin. This is a single-ended 50Ω terminated input. No external matching network is required for the high frequency band. An external series capacitor (and/or shunt capacitor) may be required for impedance transformation to 50Ω in the low frequency band from 800MHz to 1.5GHz (see Figure 4). If the RF source is not DC blocked, a series blocking capacitor should be used. Otherwise, damage to the IC may result.

V_{CC} (Pins 6, 7, 8, 12): Power Supply Pins. These pins should be decoupled using 1000pF and 0.1μF capacitors.

EN (Pin 5): Enable Pin. When the input voltage is higher than 2.0V, the circuit is completely turned on. When the enable pin voltage is less than 1.0V, the circuit is turned off. Under no conditions should the voltage at the EN pin exceed V_{CC} + 0.3V. Otherwise, damage to the IC may result. If the Enable function is not needed, then the EN pin should be tied to V_{CC}.

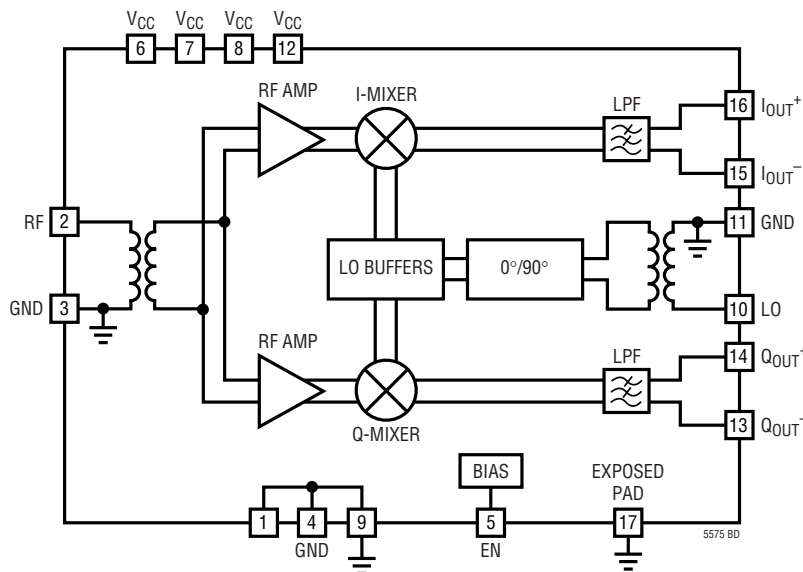
LO (Pin 10): Local Oscillator Input Pin. This is a single-ended 50Ω terminated input. No external matching network is required in the high frequency band. An external shunt capacitor (and/or series capacitor) may be required for impedance transformation to 50Ω for the low frequency band from 800MHz to 1.5GHz (see Figure 6). If the LO source is not DC blocked, a series blocking capacitor must be used. Otherwise, damage to the IC may result.

Q_{OUT}⁻, Q_{OUT}⁺ (Pins 13, 14): Differential Baseband Output Pins of the Q Channel. The internal DC bias voltage is V_{CC} – 1.1V for each pin.

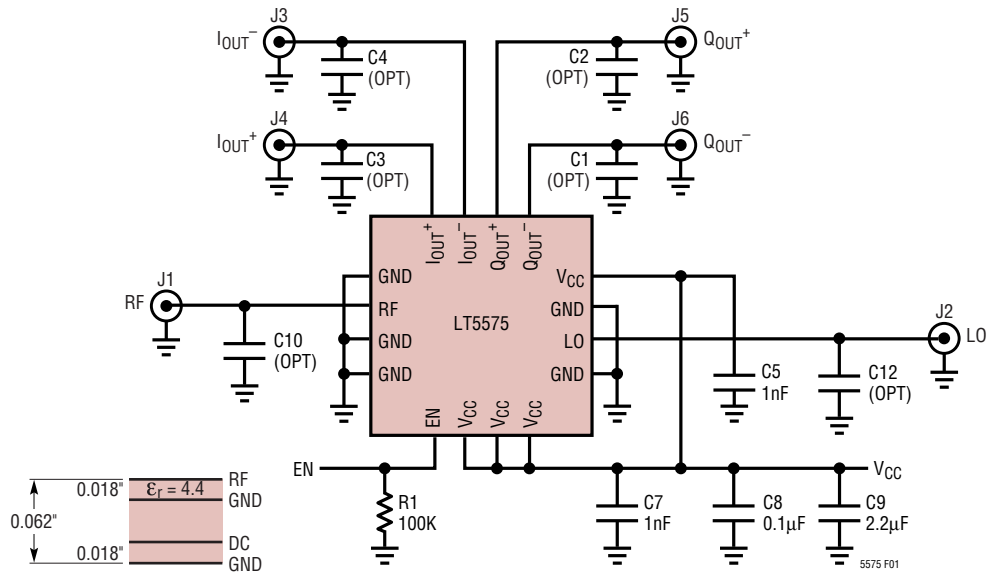
I_{OUT}⁻, I_{OUT}⁺ (Pins 15, 16): Differential Baseband Output Pins of the I Channel. The internal DC bias voltage is V_{CC} – 1.1V for each pin.

Exposed Pad (Pin 17): Ground Return for the Entire IC. This pin must be soldered to the printed circuit board ground plane.

BLOCK DIAGRAM



TEST CIRCUIT



| REF DES | VALUE | SIZE | PART NUMBER |
|---------|--------|------|----------------------|
| C5, C7 | 1000pF | 0402 | AVX 04025C102JAT |
| C8 | 0.1μF | 0402 | AVX 0402ZD104KAT |
| C9 | 2.2μF | 3216 | AVX TPSA225M010R1800 |
| R1 | 100kΩ | 0402 | |

| FREQUENCY RANGE | RF MATCH | LO MATCH | BASEBAND |
|-------------------------------|----------|----------|----------|
| | | C10 | C12 |
| LOW BAND: 800 TO 1000MHz | 4.7pF | 3.9pF | 10pF |
| MID BAND: 1000 TO 1500MHz | 2pF | 2pF | 2.2pF |
| HIGH BAND: 1500 TO 2700MHz | - | - | - |

Figure 1. Evaluation Circuit Schematic

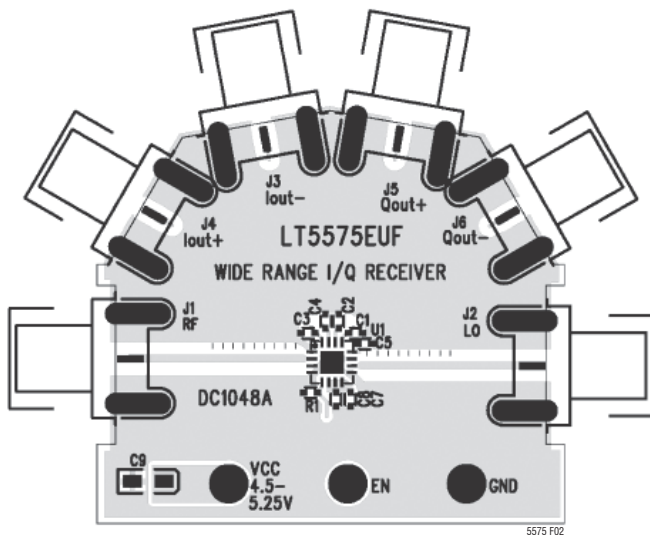


Figure 2. Top Side of Evaluation Board

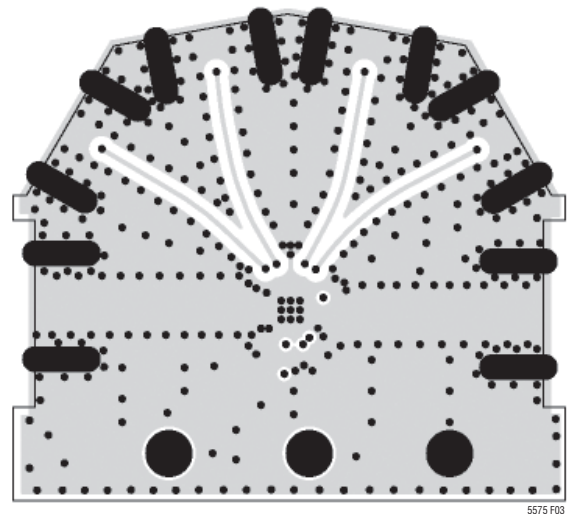


Figure 3. Bottom Side of Evaluation Board

APPLICATIONS INFORMATION

The LT5575 is a direct I/Q demodulator targeting high linearity receiver applications, such as RFID readers and wireless infrastructure. It consists of RF transconductance amplifiers, I/Q mixers, a quadrature LO phase shifter, and bias circuitry.

The RF signal is applied to the inputs of the RF transconductance amplifiers and is then demodulated into I/Q baseband signals using quadrature LO signals which are internally generated from an external LO source by precision 90° phase-shifters. The demodulated I/Q signals are single-pole low-pass filtered on-chip with a -3dB bandwidth of 490MHz. The differential outputs of the I-channel and Q-channel are well matched in amplitude; their phases are 90° apart.

Broadband transformers are integrated on-chip at both the RF and LO inputs to enable single-ended RF and LO interfaces. In the high frequency band (1.5GHz to 2.7GHz), both RF and LO ports are internally matched to 50Ω. No external matching components are needed. For the lower frequency bands (800MHz to 1.5GHz), a simple network with series and/or shunt capacitors can be used as the impedance matching network.

RF Input Port

Figure 4 shows the demodulator's RF input which consists of an integrated transformer and high linearity transconductance amplifiers. The primary side of the transformer is connected to the RF input pin. The secondary side of the transformer is connected to the differential inputs of the transconductance amplifiers. Under no circumstances should an external DC voltage be applied to the RF input pin. DC current flowing into the primary side of the transformer may cause damage to the integrated transformer. A series blocking capacitor should be used to AC-couple the RF input port to the RF signal source.

The RF input port is internally matched over a wide frequency range from 1.5GHz to 2.7GHz with input return loss typically better than 10dB. No external matching network is needed for this frequency range. When the part is operated at lower frequencies, however, the input return loss can be improved with the matching network shown in Figure 4. Shunt capacitor C10 and series capacitor C11 can be selected for optimum input impedance matching at the

desired frequency as illustrated in Figure 5. For lower frequency band operation, the external matching component C11 can serve as a series DC blocking capacitor.

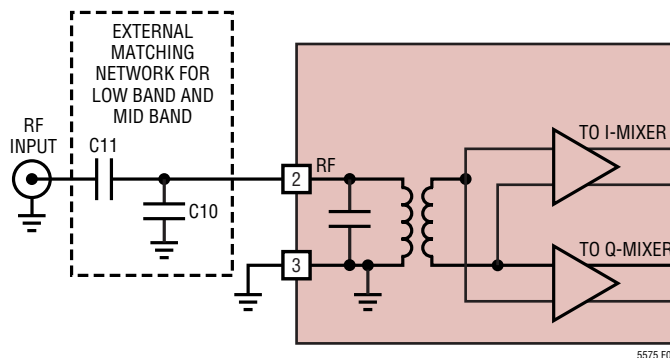


Figure 4. RF Input Interface

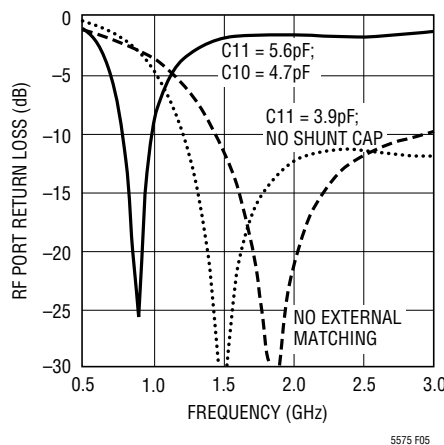


Figure 5. RF Input Return Loss with External Matching

APPLICATIONS INFORMATION

The RF input impedance and S11 parameters (without external matching components) are listed in Table 1.

Table 1. RF Input Impedance

| FREQUENCY (GHz) | INPUT IMPEDANCE (Ω) | S11 | |
|-----------------|------------------------------|-------|----------------------|
| | | MAG | ANGLE ($^{\circ}$) |
| 0.8 | 8.1 +j 21.3 | 0.760 | 133.0 |
| 0.9 | 10.5 +j 24.9 | 0.715 | 125.4 |
| 1.0 | 13.8 +j 28.8 | 0.660 | 117.2 |
| 1.1 | 18.6 +j 32.5 | 0.595 | 108.6 |
| 1.2 | 25.2 +j 35.5 | 0.521 | 99.6 |
| 1.3 | 33.6 +j 36.8 | 0.441 | 90.3 |
| 1.4 | 43.1 +j 34.6 | 0.355 | 80.8 |
| 1.5 | 51.4 +j 28.4 | 0.270 | 71.6 |
| 1.6 | 55.8 +j 19.3 | 0.188 | 63 |
| 1.7 | 55.4 +j 10.4 | 0.110 | 56.9 |
| 1.8 | 51.8 +j 3.9 | 0.042 | 63 |
| 1.9 | 46.9 +j 0.4 | 0.032 | 172.7 |
| 2.0 | 42.3 +j -0.8 | 0.084 | -173.9 |
| 2.1 | 38.4 +j -0.3 | 0.131 | -178.2 |
| 2.2 | 35.4 +j 1 | 0.172 | 175.3 |
| 2.3 | 33 +j 2.9 | 0.207 | 168.4 |
| 2.4 | 31.5 +j 4.9 | 0.235 | 161.9 |
| 2.5 | 30.4 +j 7 | 0.258 | 155.4 |
| 2.6 | 29.9 +j 9.1 | 0.274 | 149.2 |
| 2.7 | 29.7 +j 11.1 | 0.287 | 143.4 |

LO Input Port

The demodulator’s LO input interface is shown in Figure 6. The input consists of an integrated transformer and a precision quadrature phase shifter which generates 0° and 90° phase-shifted LO signals for the LO buffer amplifiers driving the I/Q mixers. The primary side of the transformer is connected to the LO input pin. The secondary side of the transformer is connected to the differential inputs of the LO quadrature generator. Under no circumstances should an external DC voltage be applied to the input pin. DC current flowing into the primary side of the transformer may damage the transformer. A series blocking capacitor should be used to AC-couple the LO input port to the LO signal source.

The LO input port is internally matched over a wide frequency range from 1.5GHz to 2.7GHz with input return loss typically better than 10dB. No external matching network is needed for this frequency range. When the part is operated at a lower frequency, the input return loss can be improved with the matching network shown in Figure 6. Shunt capacitor C12 and series capacitor C13 can be selected for optimum input impedance matching at the desired frequency as illustrated in Figure 7. For lower frequency operation, external matching component C13 can serve as the series DC blocking capacitor.

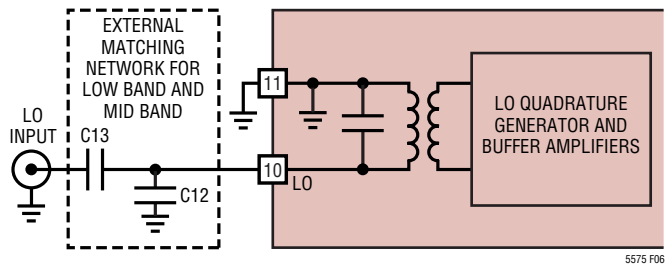


Figure 6. LO Input Interface

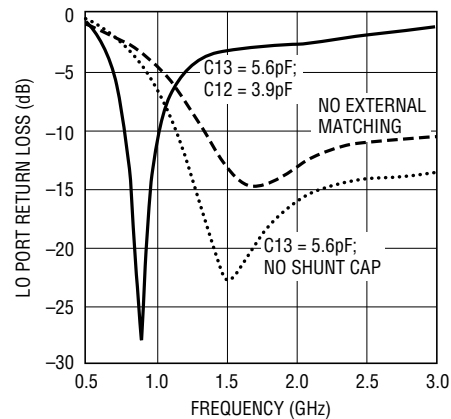


Figure 7. LO Input Return Loss with External Matching

APPLICATIONS INFORMATION

The LO input impedance and S11 parameters (without external matching components) are listed in Table 2.

Table 2. LO Input Impedance

| FREQUENCY (GHz) | INPUT IMPEDANCE (Ω) | S11 | |
|-----------------|------------------------------|-------|----------------------|
| | | MAG | ANGLE ($^{\circ}$) |
| 0.8 | 9.6 +j 23.7 | 0.731 | 127.9 |
| 0.9 | 13 +j 27.1 | 0.669 | 120.4 |
| 1.0 | 17.9 +j 30 | 0.592 | 113.2 |
| 1.1 | 24.1 +j 31.7 | 0.508 | 106.1 |
| 1.2 | 31.2 +j 31.4 | 0.421 | 99.8 |
| 1.3 | 37.5 +j 28.9 | 0.341 | 95.1 |
| 1.4 | 41.9 +j 24.6 | 0.272 | 93.4 |
| 1.5 | 43.4 +j 20 | 0.221 | 96.2 |
| 1.6 | 42.9 +j 16.4 | 0.189 | 103.5 |
| 1.7 | 41.2 +j 14.1 | 0.18 | 113.1 |
| 1.8 | 39.5 +j 13.1 | 0.186 | 120.3 |
| 1.9 | 37.8 +j 13.1 | 0.201 | 124.5 |
| 2.0 | 36.6 +j 13.6 | 0.217 | 125.6 |
| 2.1 | 35.6 +j 14.6 | 0.236 | 125 |
| 2.2 | 35.1 +j 15.7 | 0.25 | 123.1 |
| 2.3 | 34.9 +j 17.1 | 0.264 | 120.1 |
| 2.4 | 35.1 +j 18.5 | 0.272 | 116.6 |
| 2.5 | 35.5 +j 19.9 | 0.281 | 113 |
| 2.6 | 36.3 +j 21.2 | 0.284 | 109 |
| 2.7 | 37.2 +j 22.5 | 0.287 | 105.1 |

I-Channel and Q-Channel Outputs

Each of the I-channel and Q-channel outputs is internally connected to V_{CC} through a 65Ω resistor. The output DC bias voltage is $V_{CC} - 1.1V$. The outputs can be DC-coupled or AC-coupled to the external loads. Each single-ended output has an impedance of 65Ω in parallel with a $5pF$ internal capacitor, forming a low-pass filter with a $-3dB$ corner frequency at $490MHz$. The loading resistance on each output, R_{LOAD} (single-ended), should be larger than 300Ω to assure full gain. The gain is reduced by $20 \cdot \log_{10}(1 + 65\Omega/R_{LOAD})$ in dB when the output port is terminated by R_{LOAD} . For instance, the gain is reduced by $7.23dB$ when each output pin is connected to a 50Ω load (or 100Ω differentially). The output should be taken differentially (or by using differential-to-single-ended conversion) for best RF performance, including NF and IM2.

The phase relationship between the I-channel output signal and the Q-channel output signal is fixed. When the LO input frequency is larger (or smaller) than the RF input frequency, the Q-channel outputs (Q_{OUT}^+ , Q_{OUT}^-) lead (or lag) the I-channel outputs (I_{OUT}^+ , I_{OUT}^-) by 90° .

When AC output coupling is used, the resulting high-pass filter's $-3dB$ roll-off frequency is defined by the RC constant of the blocking capacitor and R_{LOAD} , assuming $R_{LOAD} \gg 65\Omega$.

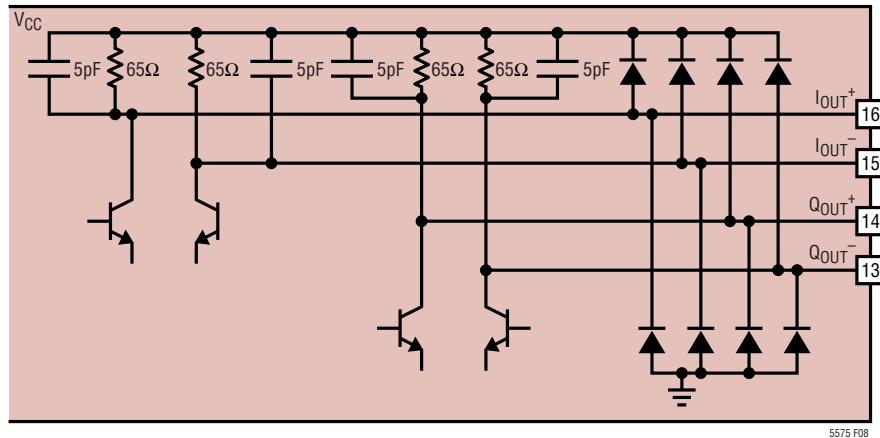


Figure 8. I/Q Output Equivalent Circuit

APPLICATIONS INFORMATION

Care should be taken when the demodulator's outputs are DC-coupled to the external load to make sure that the I/Q mixers are biased properly. If the current drain from the outputs exceeds 6mA, there can be significant degradation of the linearity performance. Each output can sink no more than 16.8mA when the outputs are connected to an external load with a DC voltage higher than $V_{CC} - 1.1V$. The I/Q output equivalent circuit is shown in Figure 8.

In order to achieve best IIP2 performance, it is important to minimize high frequency coupling among the baseband outputs, RF port and LO port. For a multilayer PCB layout design, the metal lines of the baseband outputs should be placed on the backside of the PCB as shown in Figures 2 and 3. Typically, output shunt capacitors C1-C4 are not required for the application near 1900MHz. However, for other frequency bands, these capacitors can be optimized for best IIP2 performance. For example, when the operating frequency is 900MHz, the IIP2 can be improved to 54dBm or better when 10pF shunt capacitors are placed at each output.

Enable Interface

A simplified schematic of the EN pin is shown in Figure 9. The enable voltage necessary to turn on the LT5575 is 2V. To disable or turn off the chip, this voltage should be below 1V. If the EN pin is not connected, the chip is disabled. However, it is not recommended that the pin be left floating for normal operation.

It is important that the voltage applied to the EN pin should never exceed V_{CC} by more than 0.3V. Otherwise, the supply current may be sourced through the upper ESD protection diode connected at the EN pin. Under no circumstances should voltage be applied to the EN pin before the supply voltage is applied to the V_{CC} pin. If this occurs, damage to the IC may result.

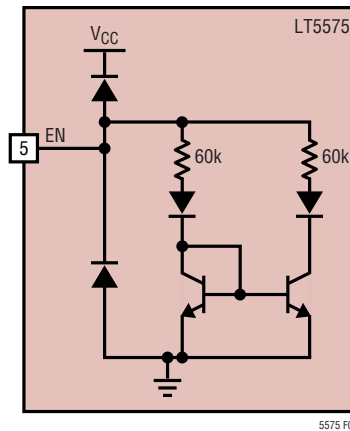
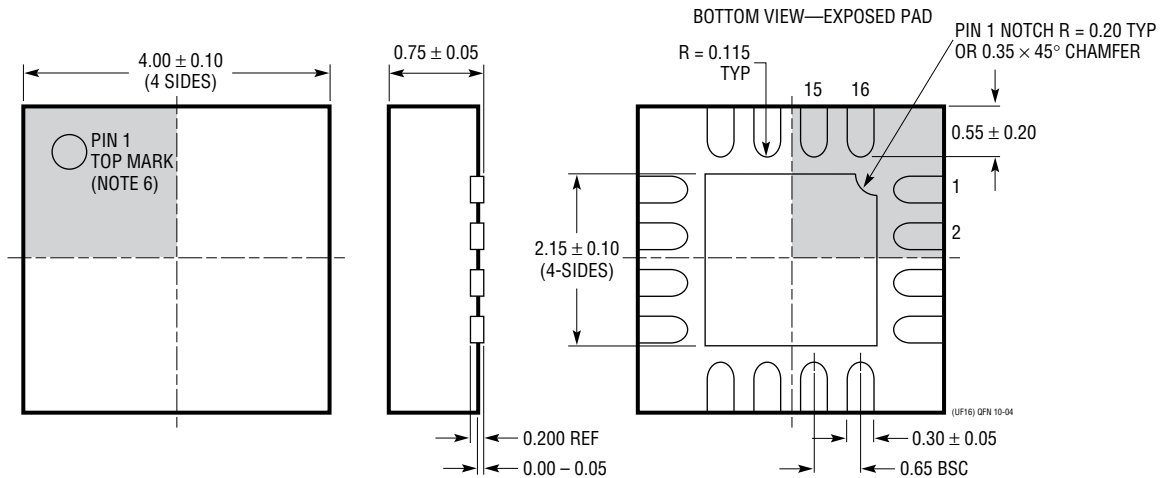
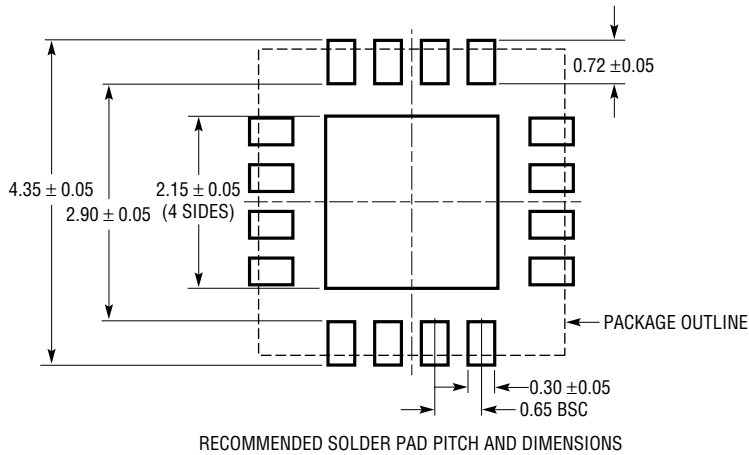


Figure 9. Enable Pin Simplified Circuit

PACKAGE DESCRIPTION

UF Package
16-Lead Plastic QFN (4mm × 4mm)
 (Reference LTC DWG # 05-08-1692)



- NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGFC)
 2. DRAWING NOT TO SCALE
 3. ALL DIMENSIONS ARE IN MILLIMETERS
 4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
 5. EXPOSED PAD SHALL BE SOLDER PLATED
 6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE