6GHz RMS Power Detector with 40dB Dynamic Range

FEATURES

- **Frequency Range: 10MHz to 6GHz**
- **Accurate Power Measurement of High Crest Factor (Up to 12dB) Waveforms**
- **40dB Log Linear Dynamic Range**
- **Exceptional Accuracy Over Temperature**
- **Fast Response Time: 1µs Rise, 8µs Fall**
- **Low Power: 1.4mA at 3.3V**
- **Log-Linear DC Output vs Input RF Power in dBm**
- Small 3mm × 2mm 8-Pin DFN Package
- Single-Ended RF Input

APPLICATIONS

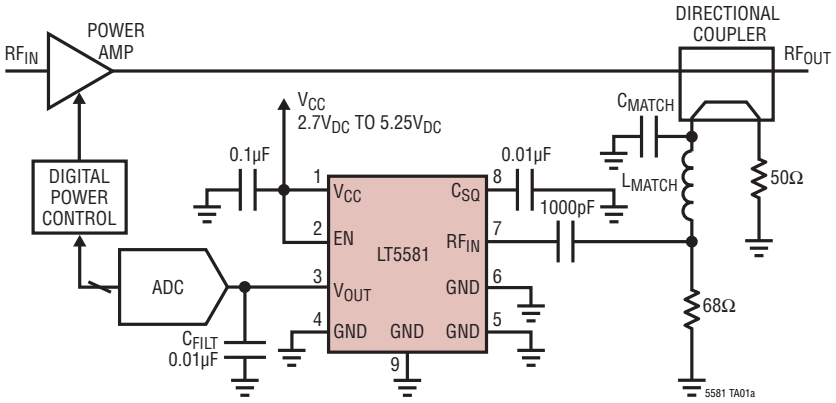
- GSM/EDGE, CMDA, CDMA2000, W-CDMA, LTE, WiMAX RF Power Control
- Pico-Cells, Femto-Cells RF Power Control
- Wireless Repeaters
- CATV/DVB Transmitters
- MIMO Wireless Access Points
- Portable RMS Power Measurement Instrumentation

DESCRIPTION

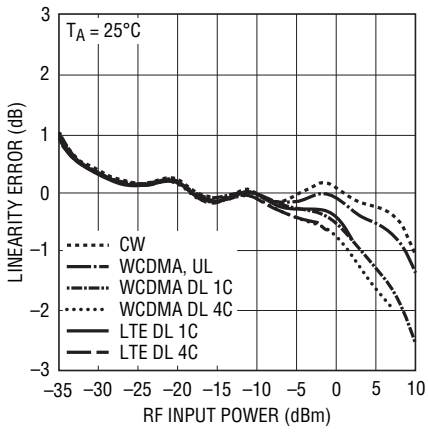
The LT®5581 is a 10MHz to 6GHz, low power monolithic precision RMS power detector. The RMS detector uses a proprietary technique to accurately measure the RF power from –34dBm to +6dBm (at 2.14GHz) of modulated signals with a crest factor as high as 12dB. It outputs a DC voltage in linear scale proportional to an RF input signal power in dBm. The LT5581 is suitable for precision power measurement and control for a wide variety of RF standards, including GSM/EDGE, CDMA, CDMA2000, W-CDMA, TD-SCDMA, UMTS, LTE and WiMAX, etc. The final DC output is connected in series with an on-chip 300Ω resistor, which enables further filtering of the output modulation ripple with just a single off-chip capacitor.

TYPICAL APPLICATION

10MHz to 6GHz Infrastructure Power Amplifier Level Control



Linearity Error vs RF Input Power, 2140MHz Modulated Waveforms



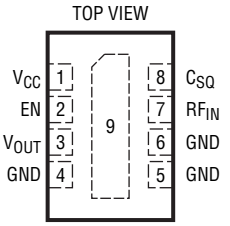
ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage 5.5V
Maximum Input Signal Power—Average 15dBm
Maximum Input Signal Power—Peak (Note 7) 25dBm
DC Voltage at RF_{IN} ..... –0.3V to 2V
V_{OUT} Voltage ..... –0.3V to V_{CC} + 0.3V
Maximum Junction Temperature, T_{JMAX} ..... 150°C
Operating Temperature Range ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C

CAUTION: This part is sensitive to electrostatic discharge. It is very important that proper ESD precautions be observed when handling the LT5581.

PIN CONFIGURATION



DDB PACKAGE
8-LEAD (3mm × 2mm) PLASTIC DFN
T_{JMAX} = 150°C, θ_{JA} = 76°C/W
EXPOSED PAD (PIN 9) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT5581IDDB#PBF	LT5581IDDB#TRPBF	LDKM	8-Lead (3mm × 2mm) Plastic DFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, V_{CC} = 3.3V, EN = 3.3V, unless otherwise noted (Note 2). Test circuit is shown in Figure 1.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
AC Input						
Input Frequency Range (Note 4)				10-6000		MHz
Input Impedance				205||1.6		Ω||pF
f_{RF} = 450MHz						
RF Input Power Range	Externally Matched to 50Ω Source			–34 to 6		dBm
Linear Dynamic Range, CW (Note 3)	±1dB Linearity Error			40		dB
Linear Dynamic Range, CDMA (Note 3)	±1dB Linearity Error; CDMA 4-Carrier			40		dB
Output Slope				31		mV/dB
Logarithmic Intercept (Note 5)				–42		dBm
Output Variation vs Temperature	Normalized to Output at 25°C, –40°C < T_A < 85°C; P_{IN} = –34 to +6dBm			±1		dB
Output Variation vs Temperature	Normalized to Output at 25°C, –40°C < T_A < 85°C; P_{IN} = –27 to –10dBm			±0.5		dB
Deviation from CW Response; P_{IN} = –34dBm to 0dBm	TETRA π/4 DQPSK CDMA 4-Carrier 64-Channel Fwd 1.23Mcps			±0.1 ±0.5		dB dB

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, V_{CC} = 3.3V, EN = 3.3V, unless otherwise noted (Note 2). Test circuit is shown in Figure 1.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
2nd Order Harmonic Distortion	At RF Input; CW Input; P_{IN} = 0dBm			–57		dBc
3rd Order Harmonic Distortion	At RF Input; CW Input; P_{IN} = 0dBm			–52		dBc
f_{RF} = 880MHz						
RF Input Power Range	Externally Matched to 50Ω Source			–34 to 6		dBm
Linear Dynamic Range, CW (Note 3)	±1dB Linearity Error			40		dB
Linear Dynamic Range, EDGE (Note 3)	±1dB Linearity Error; EDGE 3π/8-Shifted 8PSK			40		dB
Output Slope				31		mV/dB
Logarithmic Intercept (Note 5)				–42		dBm
Output Variation vs Temperature	Normalized to Output at 25°C, –40°C < T_A < 85°C; P_{IN} = –34 to +6dBm			±1		dB
Output Variation vs Temperature	Normalized to Output at 25°C, –40°C < T_A < 85°C; P_{IN} = –27 to –10dBm			±0.5		dB
Deviation from CW Response, Pin = –34 to +6dBm	EDGE 3π/8 Shifted 8PSK			±0.1		dB
f_{RF} = 2140MHz						
RF Input Power Range	Externally Matched to 50Ω Source			–34 to 6		dBm
Linear Dynamic Range, CW (Note 3)	±1dB Linearity Error			43		dB
Linear Dynamic Range, WCDMA (Note 3)	±1dB Linearity Error; 4-Carrier WCDMA			37		dB
Output Slope				31		mV/dB
Logarithmic Intercept (Note 5)				–42		dBm
Output Variation vs Temperature	Normalized to Output at 25°C, –40°C < T_A < 85°C; P_{IN} = –34 to 6dBm			±1		dB
Output Variation vs Temperature	Normalized to Output at 25°C, –40°C < T_A < 85°C; P_{IN} = –27 to –10dBm			±0.5		dB
Maximum Deviation from CW Response P_{IN} = –34 to –4dBm	WCDMA 1-Carrier Uplink WCDMA 64-Channel 4-Carrier Downlink			±0.1 ±0.5		dB dB
f_{RF} = 2600MHz						
RF Input Power Range	Externally Matched to 50Ω Source			–34 to 6		dBm
Linear Dynamic Range, CW (Note 3)	±1dB Linearity Error			40		dB
Output Slope				31		mV/dB
Logarithmic Intercept (Note 5)				–42		dBm
Output Variation vs Temperature	Normalized to Output at 25°C, –40°C < T_A < 85°C; P_{IN} = –34 to +6dBm			±1		dB
Output Variation vs Temperature	Normalized to Output at 25°C, –40°C < T_A < 85°C; P_{IN} = –27 to –10dBm			±0.5		dB
Maximum Deviation from CW Response P_{IN} = –34 to 2dBm	WiMAX OFDMA Preamble WiMAX OFDM Burst			±0.1 ±0.5		dB dB
f_{RF} = 3500MHz						
RF Input Power Range	Externally Matched to 50Ω Source			–30 to 6		dBm
Linear Dynamic Range, CW (Note 3)	±1dB Linearity Error			36		dB
Output Slope				31		mV/dB
Logarithmic Intercept (Note 5)				–41		dBm
Output Variation vs Temperature	Normalized to Output at 25°C, –40°C < T_A < 85°C; P_{IN} = –30 to +6dBm			±1		dB

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, V_{CC} = 3.3V, EN = 3.3V, unless otherwise noted (Note 2). Test circuit is shown in Figure 1.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Output Variation vs Temperature	Normalized to Output at 25°C, –40°C < T_A < 85°C; P_{IN} = –27 to –10dBm			±0.5		dB
Deviation from CW Response P_{IN} = –34 to –4dBm	WiMAX OFDMA Preamble WiMAX OFDM Burst			±0.1 ±0.5		dB dB
f_{RF} = 5800MHz						
RF Input Power Range	Externally Matched to 50Ω Source			–25 to 6		dBm
Linear Dynamic Range, CW (Note 3)	±1dB Linearity Error			31		dB
Output Slope				31		mV/dB
Logarithmic Intercept (Note 5)				–33		dBm
Output Variation vs Temperature	Normalized to Output at 25°C, –40°C < T_A < 85°C; P_{IN} = –25 to +6dBm			±1		dB
Output Variation vs Temperature	Normalized to Output at 25°C, –40°C < T_A < 85°C; P_{IN} = –20 to +6dBm			±0.5		dB
Deviation from CW Response	WiMAX OFDM Burst; P_{IN} = –25 to 6dBm			±0.2		dB
Output						
Output DC Voltage	No Signal Applied to RF Input			180		mV
Output Impedance	Internal Series Resistor Allows for Off-Chip Filter Cap			300		Ω
Output Current Sourcing/Sinking				5/5		mA
Rise Time	0.2V to 1.6V, 10% to 90%, f_{RF} = 2140MHz			1		µs
Fall Time	1.6V to 0.2V, 10% to 90%, f_{RF} = 2140MHz			8		µs
Power Supply Rejection Ratio (Note 6)	For Over Operating Input Power Range			49		dB
Integrated Output Voltage Noise	1kHz to 6.5kHz Integration BW, P_{IN} = 0dBm CW			150		μV_{RMS}
Enable (EN) Low = Off, High = On						
EN Input High Voltage (On)		●	2			V
EN Input Low Voltage (Off)		●			0.3	V
Enable Pin Input Current	EN = 3.3V			20		µA
Turn-On Time; CW RF input	V_{OUT} Within 10% of Final Value; P_{IN} = 0dBm			1		µs
Settling Time; RF Pulse	V_{OUT} Within 10% of Final Value; P_{IN} = 0dBm			1		µs
Power Supply						
Supply Voltage		●	2.7	3.3	5.25	V
Supply Current	No RF Input Signal			1.4		mA
Shutdown Current	EN = 0.3V, V_{CC} = 3.3V			0.2	6	µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LT5581 is guaranteed functional over the operating temperature range from –40°C to 85°C.

Note 3: The linearity error is calculated by the difference between the incremental slope of the output and the average output slope from –20dBm to 0dBm. The dynamic range is defined as the range over which the linearity error is within ±1dB.

Note 4: An external capacitor at the C_{SQ} pin should be used for input frequencies below 250MHz. Lower frequency operation results in excessive RF ripple in the output voltage.

Note 5: Logarithmic intercept is an extrapolated input power level from the best fitted log-linear straight line, where the output voltage is 0V.

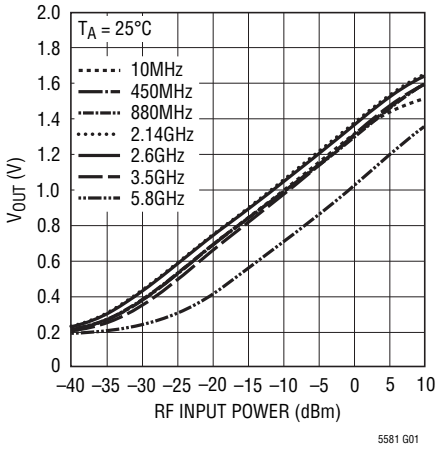
Note 6: PSRR is determined as the dB value of the change in V_{OUT} voltage over the change in V_{CC} supply voltage.

Note 7: Not production tested. Guaranteed by design and correlation to production tested parameters.

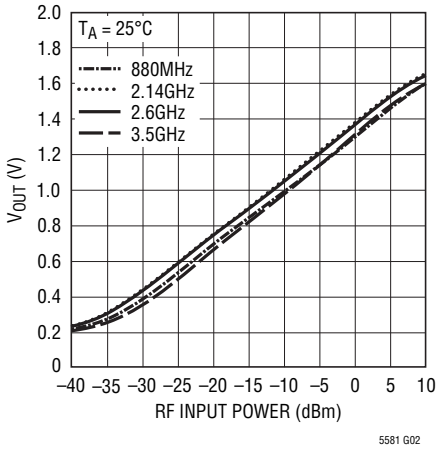
TYPICAL PERFORMANCE CHARACTERISTICS

Performance characteristics taken at V_{CC} = 3.3V, EN = 3.3V and T_A = 25°C, unless otherwise noted. (Test circuit shown in Figure 1)

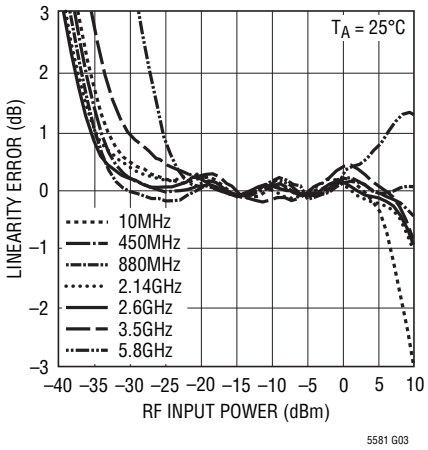
Output Voltage vs Frequency



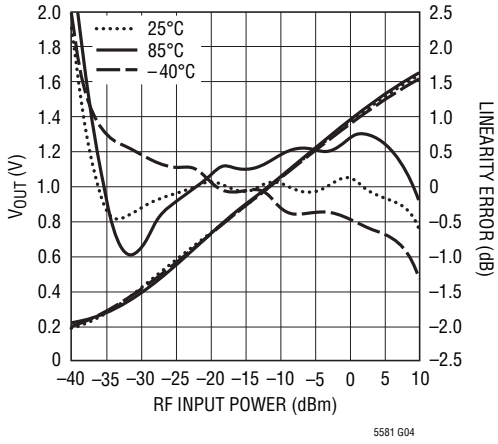
Output Voltage vs Frequency



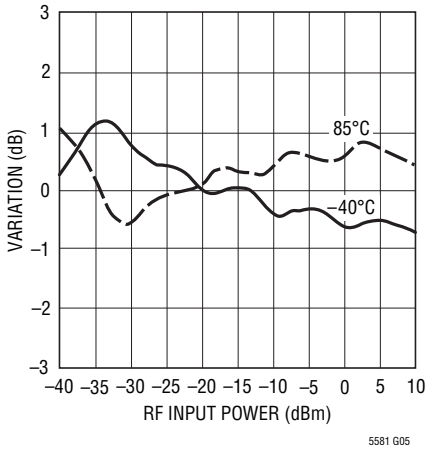
Linearity Error vs Frequency



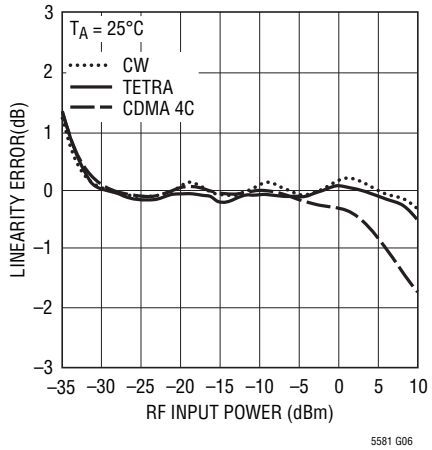
Output Voltage and Linearity Error at 450MHz



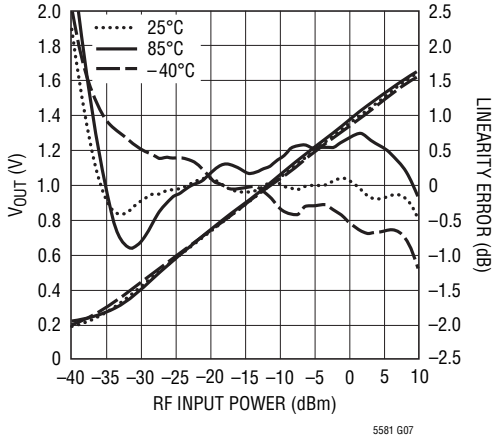
Linearity Error Temperature Variation from 25°C at 450MHz



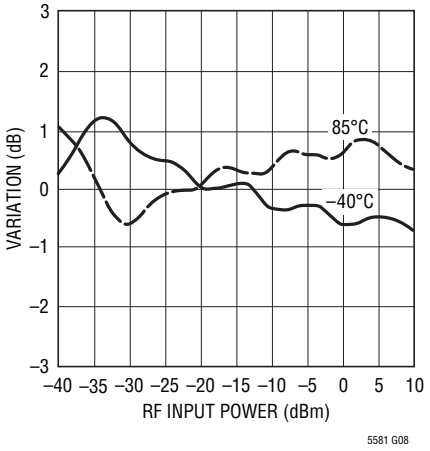
Linearity Error vs RF Input Power, 450MHz Modulated Waveforms



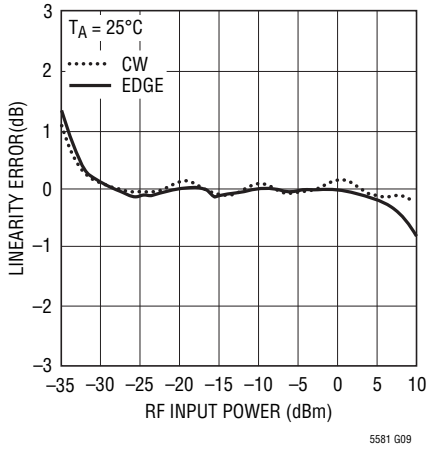
Output Voltage and Linearity Error at 880MHz



Linearity Error Temperature Variation from 25°C at 880MHz

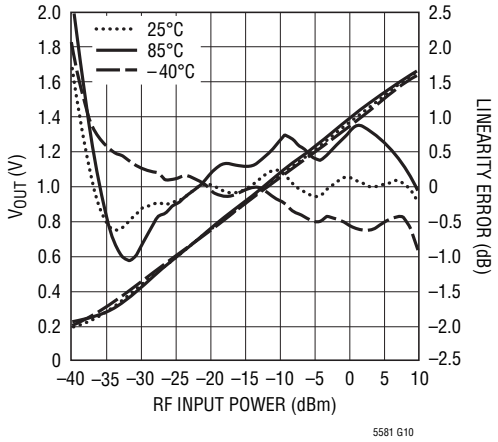


Linearity Error vs RF Input Power, 880MHz Modulated Waveforms

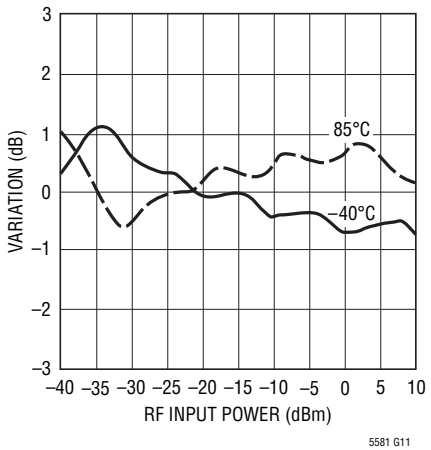


TYPICAL PERFORMANCE CHARACTERISTICS

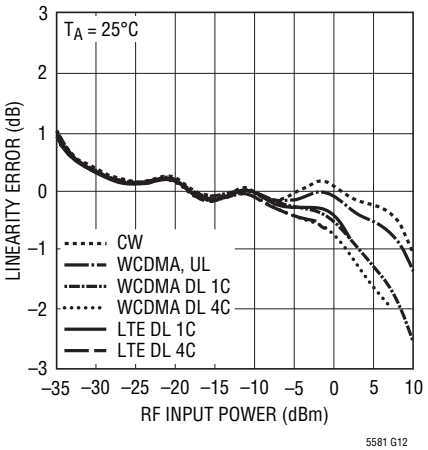
Output Voltage and Linearity Error at 2140MHz



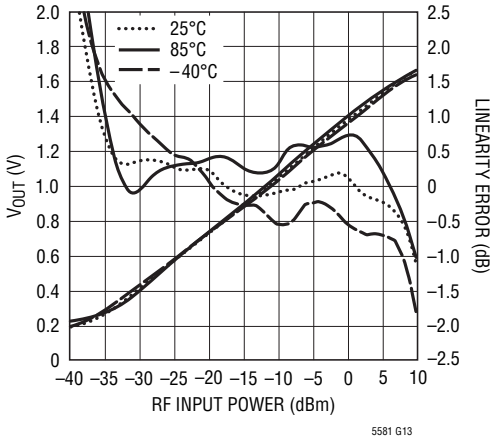
Linearity Error Temperature Variation from 25°C at 2140MHz



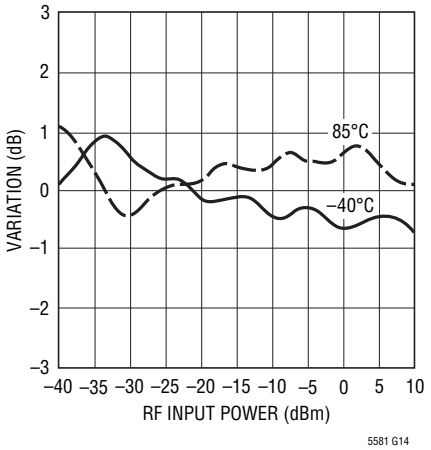
Linearity Error vs RF Input Power, 2140MHz Modulated Waveforms



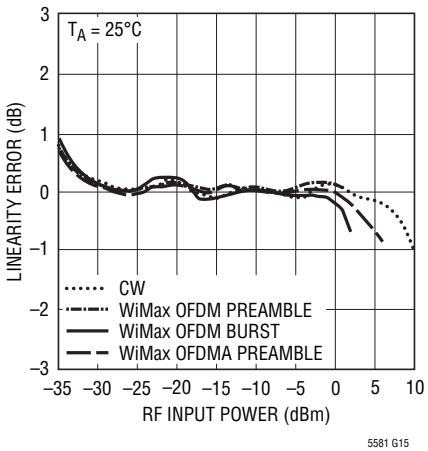
Output Voltage and Linearity Error at 2600MHz



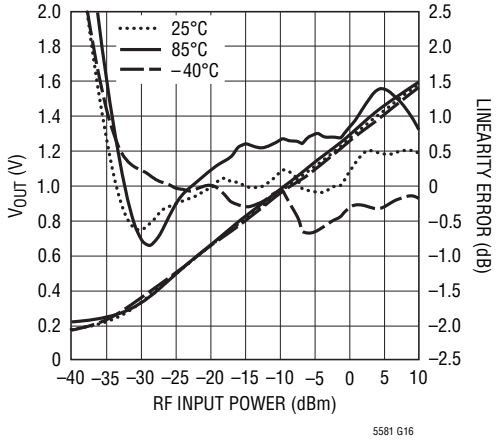
Linearity Error Temperature Variation from 25°C at 2600MHz



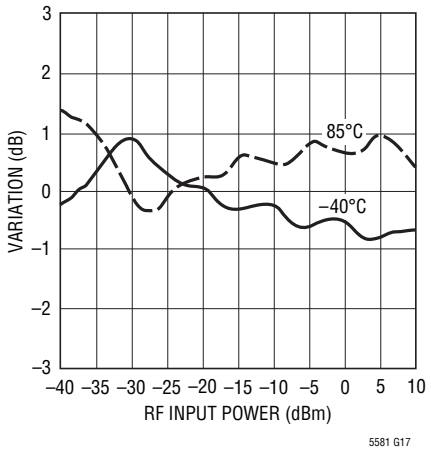
Linearity Error vs RF Input Power, 2.6GHz Modulated Waveforms



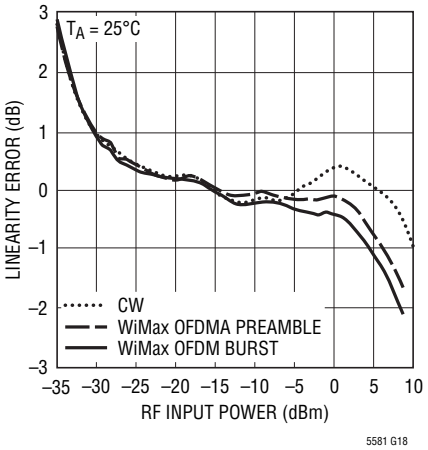
Output Voltage and Linearity Error at 3500MHz



Linearity Error Temperature Variation from 25°C at 3500MHz

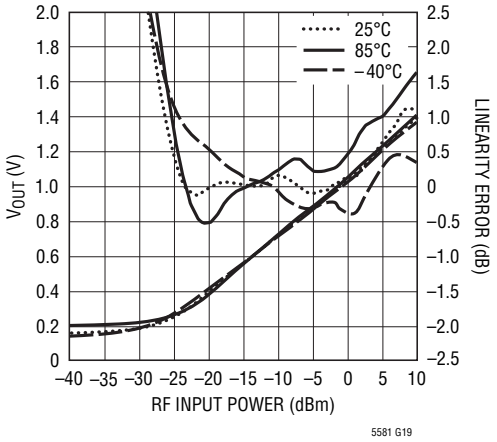


Linearity Error vs RF Input Power, 3.5GHz Modulated Waveforms

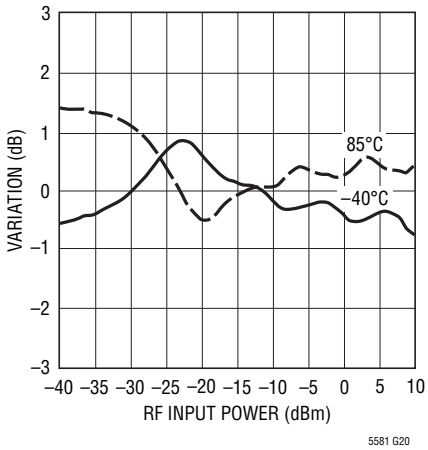


TYPICAL PERFORMANCE CHARACTERISTICS

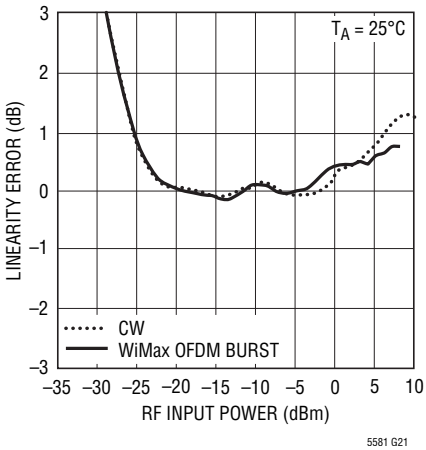
Output Voltage and Linearity Error at 5800MHz



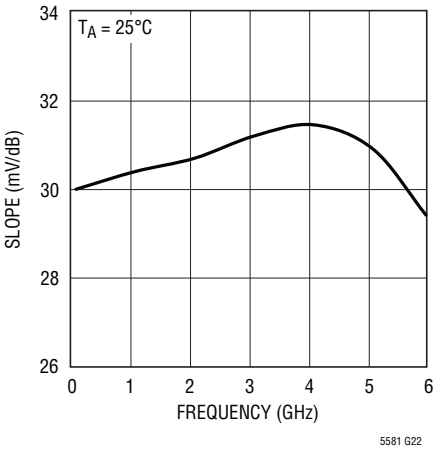
Linearity Error Temperature Variation from 25°C at 5800MHz



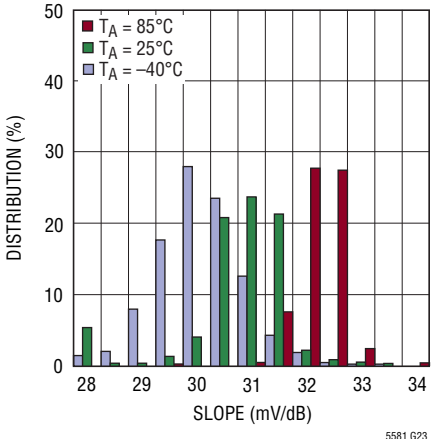
Linearity Error vs RF Input Power, 5.8GHz Modulated Waveforms



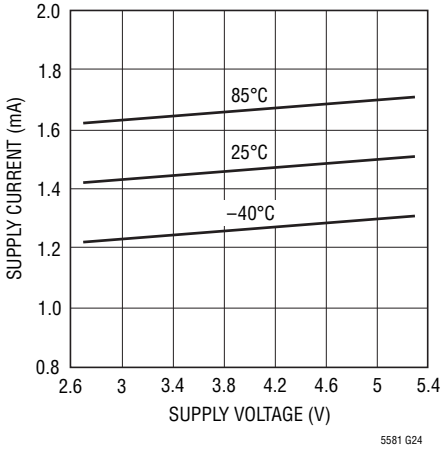
Slope vs Frequency



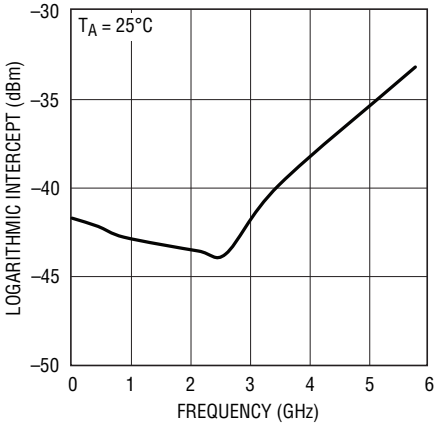
Slope Distribution vs Temperature



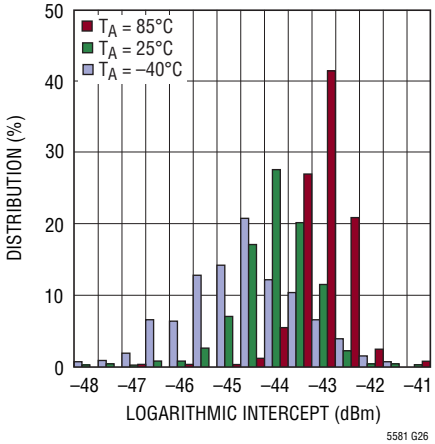
Supply Current vs Supply Voltage



Logarithmic Intercept vs Frequency

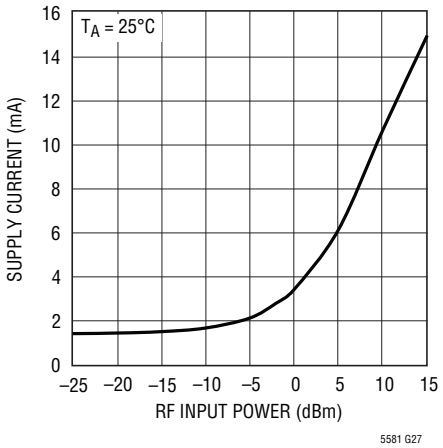


Logarithmic Intercept Distribution vs Temperature

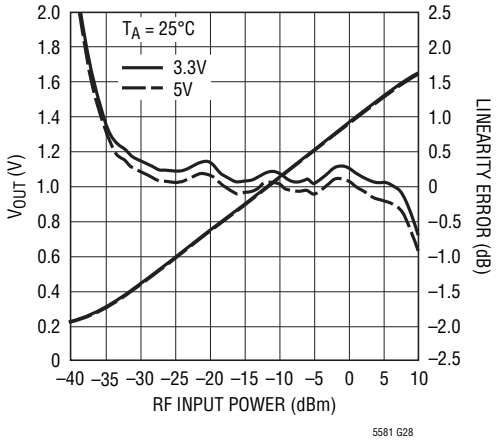


TYPICAL PERFORMANCE CHARACTERISTICS

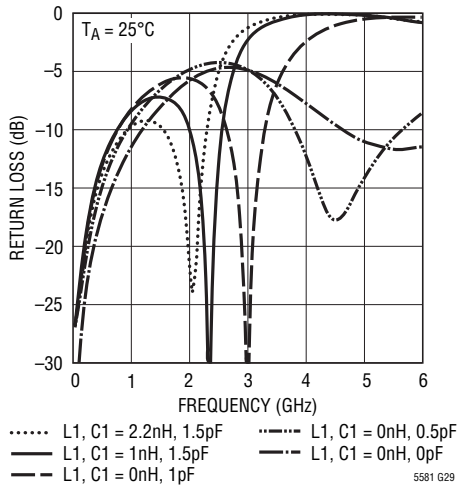
Supply Current vs RF Input Power



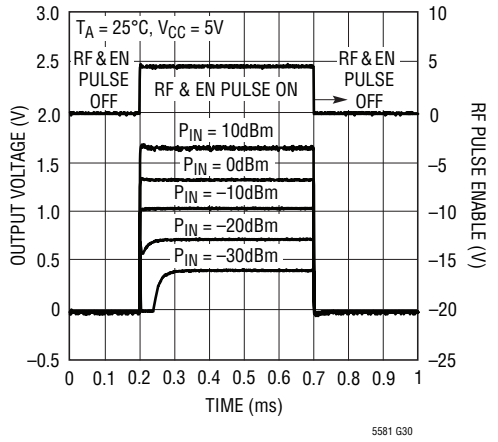
Output Voltage and Linearity Error vs V_{CC} at 2140MHz



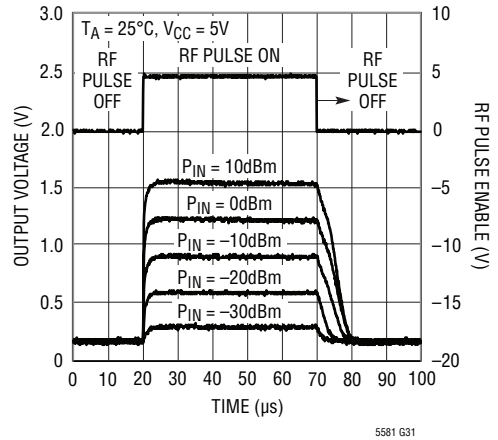
Return Loss vs Frequency Reference in Figure 1 Test Circuit



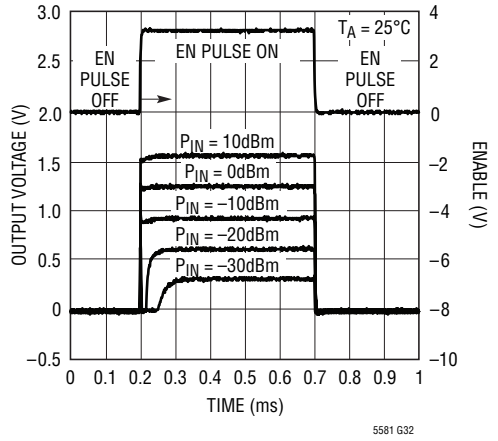
Output Transient Response with RF and EN Pulse



Output Transient Response



Output Transient Response with CW RF and EN Pulse



PIN FUNCTIONS

V_{CC} (Pin 1): Power Supply, 2.7V to 5.25V. V_{CC} should be bypassed with a 0.1µF ceramic capacitor.

EN (Pin 2): Chip Enable. A logic low or no-connect on the enable pin shuts down the part. A logic high enables the part. An internal 500k pull-down resistor ensures the part is off when the enable driver is in a three-state condition.

V_{OUT} (Pin 3): Detector Output.

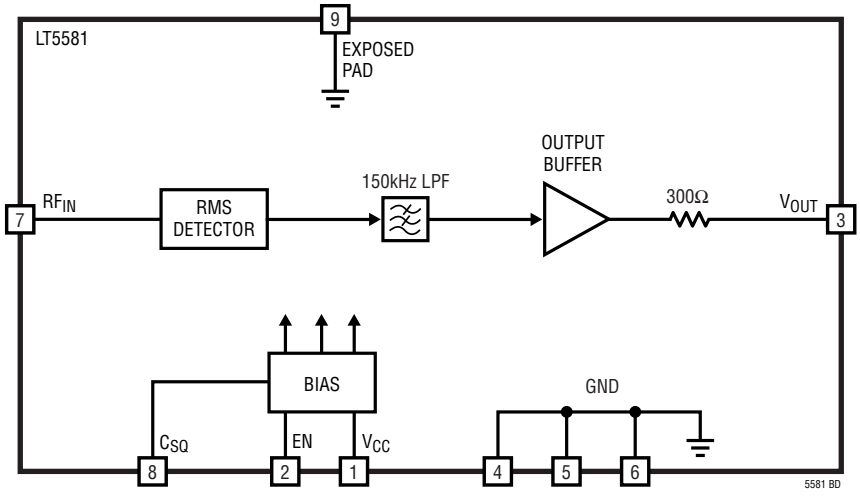
GND (Pins 4, 5, 6): Ground.

RF_{IN} (Pin 7): RF Input. Should be DC-blocked with coupling capacitor; 1000pF recommended. This pin has an internal 200Ω termination.

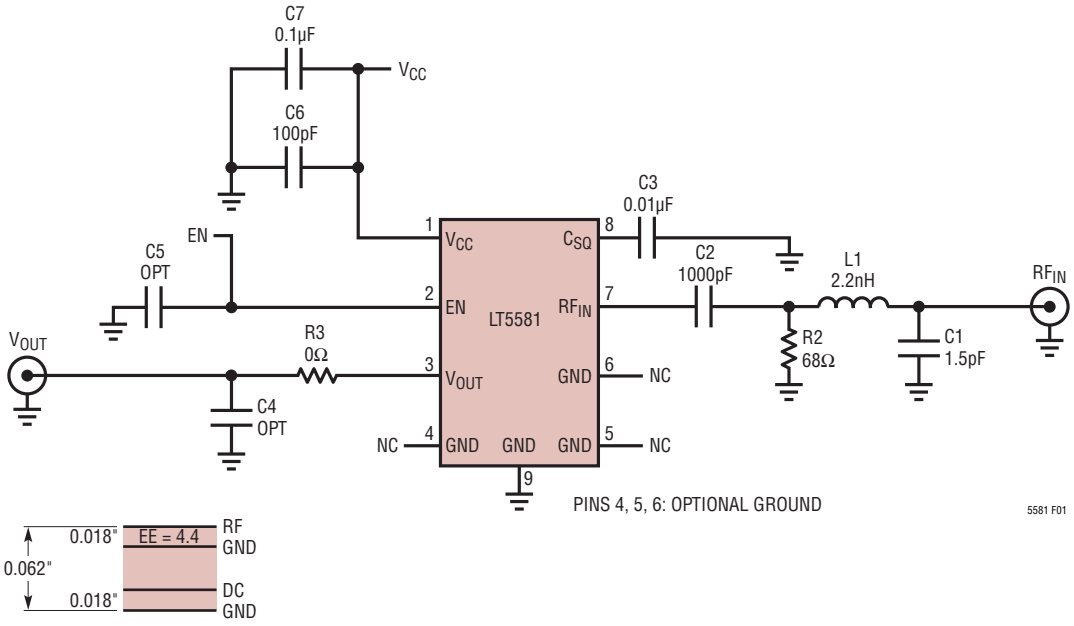
C_{SQ} (Pin 8): Optional Low Frequency Range Extension Capacitor. This pin is for frequencies below 250MHz. Use 0.01µF from pin to ground for 10MHz operation.

Exposed Pad (Pin 9): Ground. The Exposed Pad must be soldered to the PCB. For high frequency operation, the backside ground connection should have a low inductance connection to the PCB ground, using many through-hole vias. See the layout information in the Applications Information section.

BLOCK DIAGRAM



TEST CIRCUIT



REF DES	VALUE	SIZE	PART NUMBER
C6	100pF	0603	AVX 06033A101KAT2A
C7	0.1µF	0603	AVX 06033C104KAT2A
C3	0.01µF	0603	AVX 06033C103KAT2A
C2	1000pF	0603	AVX 06033C102KAT2A
R2	68Ω	0603	

FREQUENCY RANGE	RF_{IN} MATCH	
	L1	C1
1GHz to 2.2GHz	2.2nH	1.5pF
2GHz to 2.6GHz	1.2nH	1.5pF
2.6GHz to 3.4GHz	0	1pF
3.8GHz to 5.5GHz	0	0.5pF
4.6GHz to 6GHz	0	0

Figure 1. Evaluation Circuit Schematic

APPLICATIONS INFORMATION

OPERATION

To achieve an accurate average power measurement of the high crest factor modulated RF signals, the LT5581 combines a proprietary high speed power measurement subsystem with an internal 150kHz low pass averaging filter and an output voltage buffer in a completely integrated solution with minimal off-chip components. The resulting output voltage is directly proportional to the average RF input power in dBm. Figure 1 shows the evaluation circuit schematic, and Figures 2 and 3 show the associated board artwork. For best high frequency performance, it is important to place many ground vias directly under the package.

RF Input Matching

The input resistance is about 205Ω. Input capacitance is 1.6pF. The impedance vs frequency of the RF input is detailed in Table 1.

Table 1. RF Input Impedance

FREQUENCY (MHz)	INPUT IMPEDANCE (Ω)	S11	
		MAG	ANGLE (°)
10	203.6-j5.5	0.606	–0.8
50	199.5-j22.4	0.603	–3.4
100	191.7-j40.3	0.601	–6.4
200	171.1-j68.5	0.601	–12.3
400	121.8-j95.4	0.608	–24
500	100.2-j97.5	0.613	–29.8
800	56.8-j86.5	0.631	–46.5
900	48-j81.2	0.638	–51.8
1000	41.1-j76	0.645	–56.8
1500	22.2-j55	0.679	–79.5
2000	14.6-j41.4	0.710	–97.9
2100	13.6-j39.2	0.716	–101.2
2500	10.8-j32.1	0.737	–112.9
3000	8.6-j25	0.759	–125.7
3500	7.3-j19.4	0.774	–136.9
4000	6.6-j14.5	0.783	–147.1
5000	8.8-j9.6	0.709	–157.6
6000	6.4-j0	0.774	–179.9

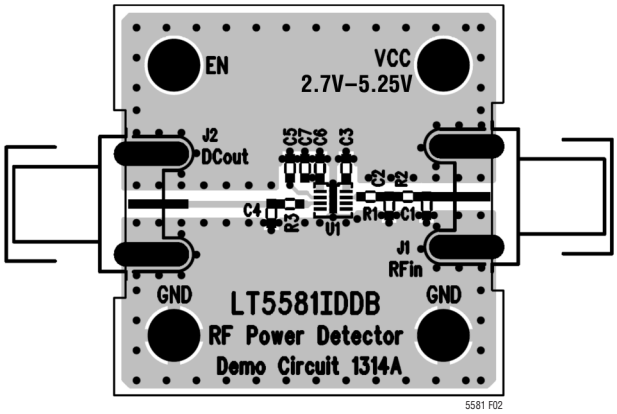


Figure 2. Top Side of Evaluation Board

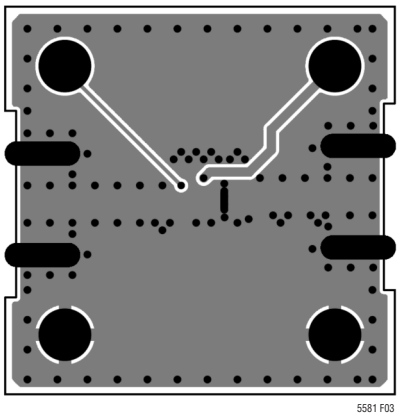


Figure 3. Bottom Side of Evaluation Board

APPLICATIONS INFORMATION

A shunt 68Ω resistor can be used to provide a broadband impedance match at low frequencies up to 1.3GHz, and from 4.5GHz to 6GHz. As shown in Figure 4, a nominal broadband input match can be achieved up to 2.2GHz by using an LC matching circuit consisting of a series 2.2nH inductor (L1) and a shunt 1.5pF capacitor (C1). This match will maintain a return loss of about 10dB across the band. For matching at higher frequencies, values for L1 and C1 are listed in the table of Figure 1. The input reflection coefficient referenced to the RF input pin (with no external components) is shown on the Smith Chart in Figure 5. Alternatively, it is possible to match using an impedance transformation network by omitting R1 and transforming the 205Ω load to 50Ω. The resulting match, over a narrow band of frequencies, will improve sensitivity up to about 6dB maximum; the dynamic range remains the same. For example, by omitting R1 and setting L1 = 1.8nH and C1 = 3pF, a 2:1 VSWR match can be obtained from 1.95GHz to 2.36GHz, with a sensitivity improvement of 5dB.

The RF_{IN} input DC blocking capacitor (C2) and the C_{SQ} bias decoupling capacitor (C3), can be adjusted for low frequency operation. For input frequencies down to 10MHz, 0.01µF is needed at C_{SQ}. For frequencies above 250MHz, the on-chip 20pF decoupling capacitor is sufficient, and C_{SQ} may be eliminated as desired. The DC-blocking capacitor can be as large as 2200pF for 10MHz operation, or 100pF for 2GHz operation. A DC-blocking capacitor larger than 2200pF results in an undesirable RF pulse response on the falling edge. Therefore, for general applications, the recommended value for C2, is conservatively set at 1000pF.

Output Interface

The output buffer of the LT5581 is shown in Figure 6. It includes a push-pull stage with a series 300Ω resistor. The output stage is capable of sourcing and sinking 5mA of current. The output pin can be shorted to GND or V_{CC} without damage, but going beyond V_{CC} + 0.5V or GND – 0.5V may result in damage, as the internal ESD protection diodes will start to conduct excessive current.

The residual ripple, due to RF modulation, can be reduced by adding external components R_{SS} and C_{LOAD} (R3 and C4 on the Evaluation Circuit Schematic in Figure 1) to

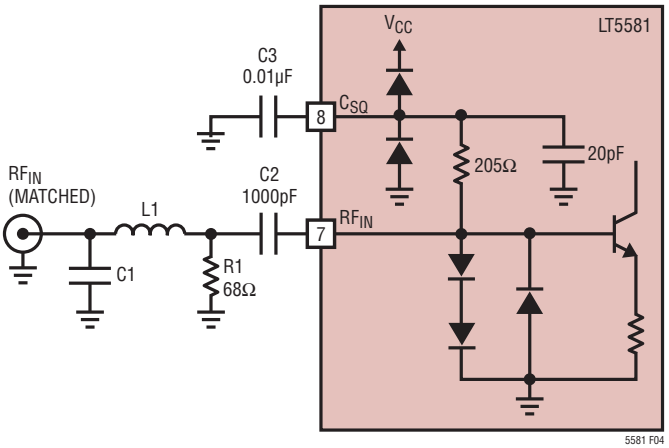


Figure 4. Simplified Circuit Schematic of the RF Input Interface

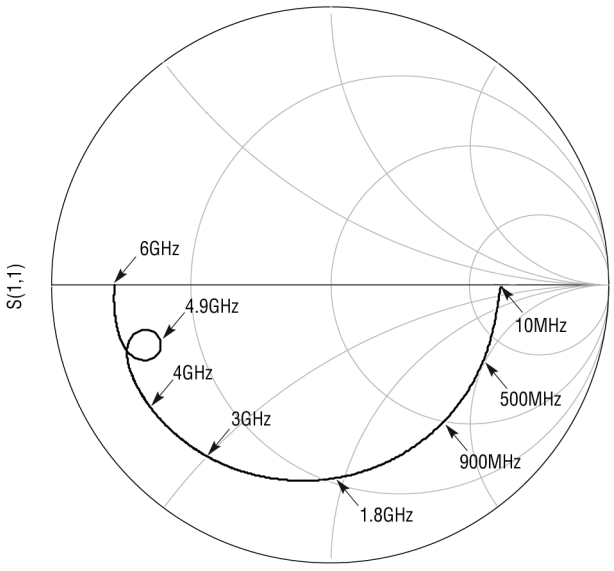


Figure 5. Input Reflection Coefficient

APPLICATIONS INFORMATION

the output pin, to form an RC lowpass filter. The internal 300Ω resistor in series with the output pin enables filtering of the output signal with just the addition of C_{LOAD}. Figure 7 shows the effect of the external filter capacitor on the residual ripple level for a 4-carrier WCDMA signal at 2.14GHz with –10dBm. Adding a 10nF capacitor to the output decreases the peak-to-peak output ripple from $135mV_{P-P}$ to $50mV_{P-P}$. The filter –3dB corner frequency can be calculated with the following equation:

$$f_C = \frac{1}{2\pi C_{LOAD}(300+R_{SS})}$$

Figure 8 shows the transient response for a 2.6GHz WiMAX signal, with preamble and burst ripple reduced by a factor of 3, using a 0.047µF external filter capacitor. The average power in the preamble section is –10dBm, while the burst section has a 3dB lower average power. With the capacitor, the ripple in the preamble section is about 0.5dB peak-to-peak. The modulation used was OFDM (WiMAX 802.16-2004) MMDS band, 1.5MHz BW, with 256 size FFT and 1 burst at QPSK 3/4.

Figure 9 shows how the peak-to-peak ripple decreases with increasing external filter capacitance value. Also shown is how the RF pulse response will have longer rise and fall times with the addition of this lowpass filter cap.

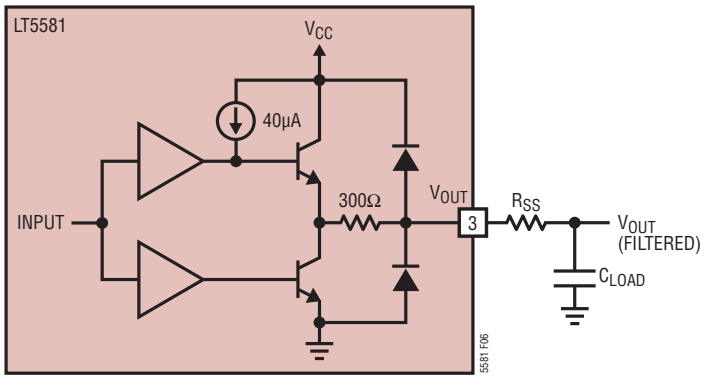


Figure 6. Simplified Circuit Schematic of the Output Interface

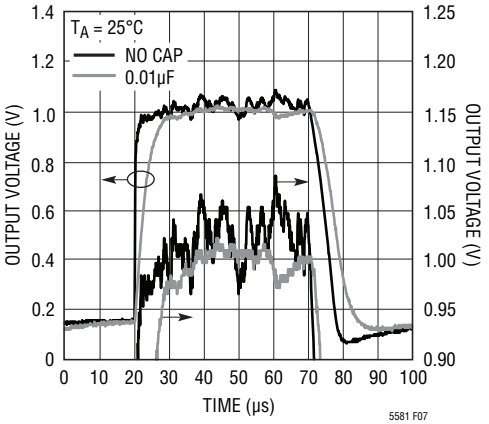


Figure 7. Residual Ripple, Output Transient Response for RF Pulse with WCDMA 4-Carrier Modulation

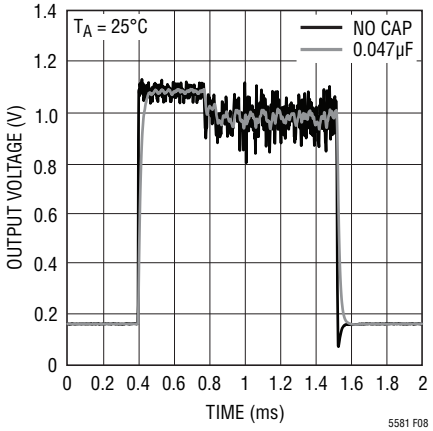


Figure 8. Residual Ripple for 2.6GHz WiMAX OFDM 802.16-2004

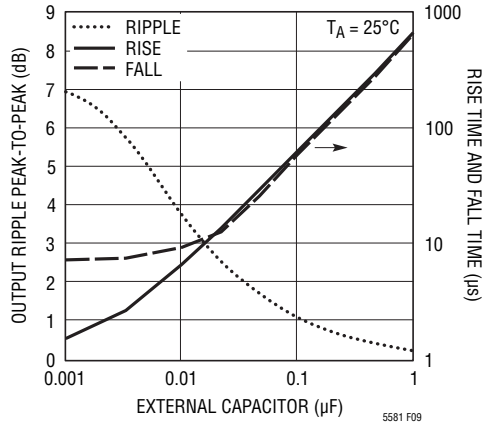


Figure 9. Residual Ripple, Output Transient Times for RF Pulse with WCDMA 4-Carrier Modulation vs External Filter Capacitor C4

APPLICATIONS INFORMATION

Figure 10 shows that rise time and fall time are strong functions of RF input power. Data is taken without the output filter capacitor.

For a given RF modulation type—WCDMA, for example—the internal 150kHz filter provides nominal filtering of the residual ripple level. Additional external filtering occurs in the log domain, which introduces a systematic log error in relation to the signal's crest factor, as shown in the following equation in dB.[1]

$$Error|dB = 10 \bullet \log_{10}(r + (1 - r)10^{-CF/10}) - CF \bullet (r\text{-}1)$$

Where CF is the crest factor and r is the duty cycle of the measurement (or number of measurements made at the peak envelope, divided by the total number of periodic measurements in the measurement period). It is important to note that the CF refers to the 150kHz low pass filtered envelope of the signal. The error will depend on the statistics and bandwidth of the modulation signal in relation to the internal 150kHz filter. For example, in the case of WCDMA, simulations prove that it is possible to set the external filter capacitor corner frequency at 15kHz and only introduce an error less than 0.1dB.

Figure 11 depicts the output AM modulation ripple as a function of modulation difference frequency for a 2-tone input signal at 2140MHz with –10dBm input power. The resulting deviation in the output voltage of the detector shows the effect of the internal 150kHz filter.

[1] Steve Murray, "Beware of Spectrum Analyzer Power Averaging Techniques," Microwaves & RF, Dec. 2006.

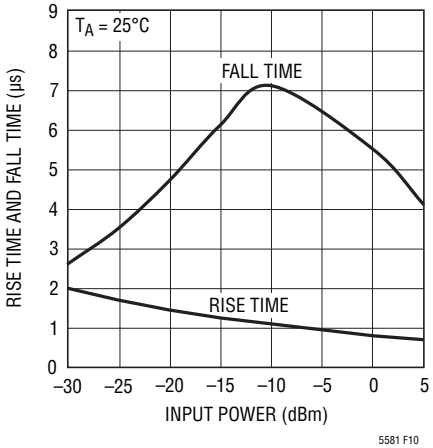


Figure 10. RF Pulse Response Rise Time and Fall Time vs RF Input Power

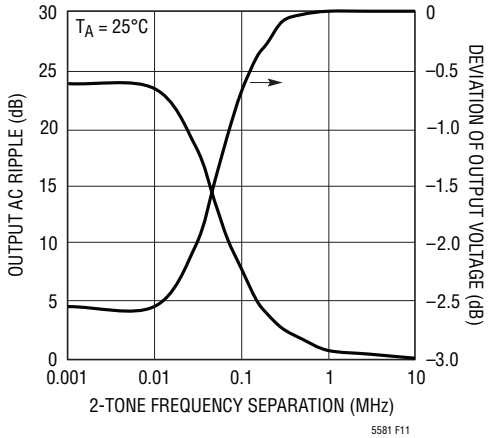


Figure 11. Output DC Voltage Deviation and Residual Ripple vs 2-Tone Separation Frequency

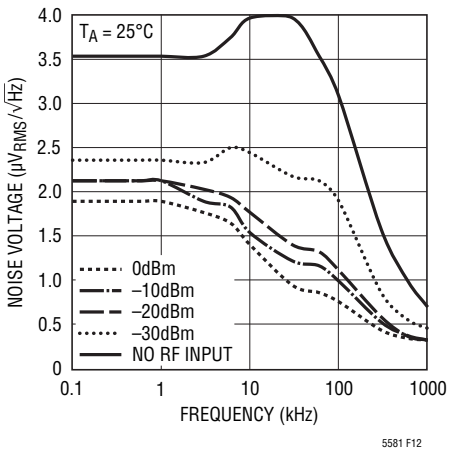


Figure 12. Output Voltage Noise Density

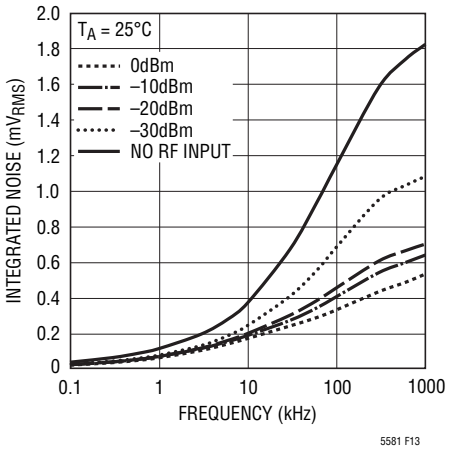


Figure 13. Integrated Output Voltage Noise

APPLICATIONS INFORMATION

The output voltage noise density and integrated noise are shown in Figures 12 and 13, respectively, for various input power levels. Noise is a strong function of input level. There is roughly a 10dB reduction in the output noise level for an input level of 0dBm versus no input.

Enable Pin

A simplified schematic of the EN pin is shown in Figure 14. To enable the LT5581, it is necessary to put greater than 2V on this pin. To disable or turn off the chip, this voltage should be below 0.3V. At an enable voltage of 3.3V, the pin draws roughly 20µA. If the EN pin is not connected, the chip is disabled through an internal 500k pull-down resistor.

It is important that the voltage applied to the EN pin never exceeds V_{CC} by more than 0.5V, otherwise, the supply current may be sourced through the upper ESD protection diode connected at the EN pin.

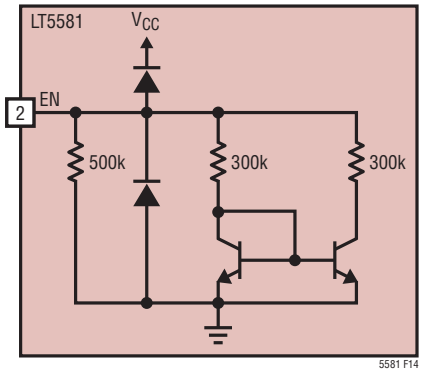
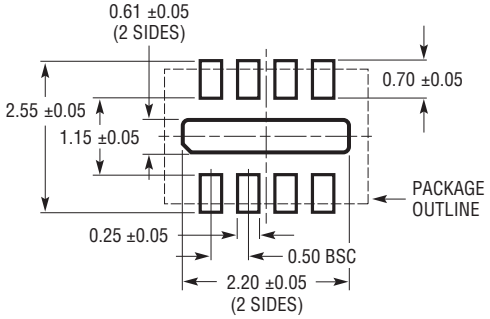


Figure 14. Enable Pin Simplified Schematic

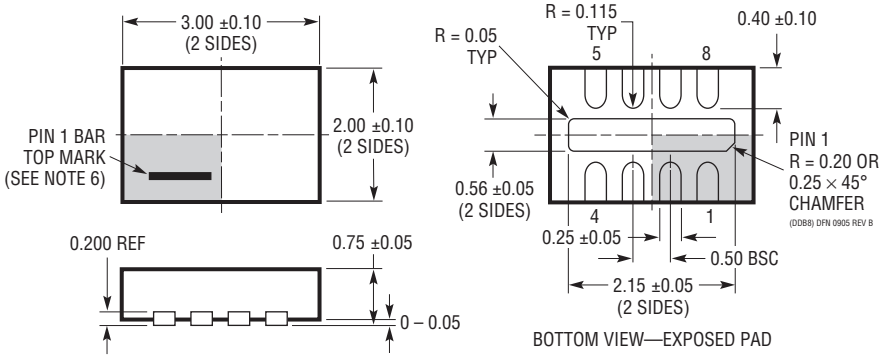
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

DDB Package
8-Lead Plastic DFN (3mm × 2mm)
(Reference LTC DWG # 05-08-1702 Rev B)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING CONFORMS TO VERSION (WECD-1) IN JEDEC PACKAGE OUTLINE M0-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	4/10	Updated Note 2 in Electrical Characteristics Section	4
B	8/15	Changed Enable Pin input voltage to 2V	15