

FEATURES

- **Wide Supply Range: 1.6V to 16V**
- **Low Supply Current: 1 μ A/Amplifier Max**
- **Low Input Bias Current: 90pA Max**
- Low Input Offset Voltage: 500 μ V Max
- Low Input Offset Voltage Drift: 2 μ V/ $^{\circ}$ C
- CMRR: 100dB
- PSRR: 95dB
- A_{VOL} Driving 20k Ω Load: 100,000 Min
- Capacitive Load Handling: 500pF
- Specified from -40° C to 125 $^{\circ}$ C
- Available in Tiny 2mm \times 2mm DFN and Low Profile (1mm) ThinSOTTM Packages

APPLICATIONS

- Portable Gas Monitors
- Battery- or Solar-Powered Systems
- Low Voltage Signal Processing
- Micropower Active Filters

DESCRIPTION

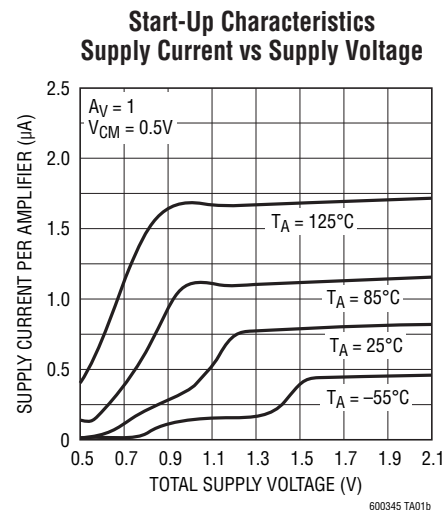
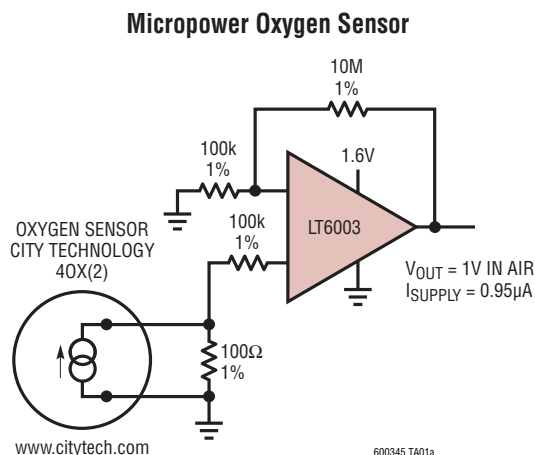
The LT[®]6003/LT6004/LT6005 are single/dual/quad op amps designed to maximize battery life and performance for portable applications. These amplifiers operate on supplies as low as 1.6V and are fully specified and guaranteed over temperature on 1.8V, 5V and \pm 8V supplies while only drawing 1 μ A maximum quiescent current.

The ultralow supply current and low operating voltage are combined with excellent amplifier specifications; input offset voltage of 500 μ V maximum with a typical drift of only 2 μ V/ $^{\circ}$ C, input bias current of 90pA maximum, open loop gain of 100,000 and the ability to drive 500pF capacitive loads, making the LT6003/LT6004/LT6005 amplifiers ideal when excellent performance is required in battery powered applications.

The single LT6003 is available in the 5-pin TSOT-23 and tiny 2mm \times 2mm DFN packages. The dual LT6004 is available in the 8-pin MSOP and 3mm \times 3mm DFN packages. The quad LT6005 is available in the 16-pin SSOP and 5mm \times 3mm DFN packages. These devices are specified over the commercial, industrial and automotive temperature ranges.

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TYPICAL APPLICATION



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LT6003/LT6004/LT6005

ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage (V^+ to V^-).....	18V	Specified Temperature Range (Note 4)	
Differential Input Voltage.....	18V	LT6003C, LT6004C, LT6005C.....	0°C to 70°C
Input Voltage Below V^-	9V	LT6003I, LT6004I, LT6005I.....	-40°C to 85°C
Input Current.....	10mA	LT6003H, LT6004H, LT6005H.....	-40°C to 125°C
Output Short Circuit Duration (Note 2).....	Indefinite	Junction Temperature	
Operating Temperature Range (Note 3)		DFN Packages.....	125°C
LT6003C, LT6004C, LT6005C.....	-40°C to 85°C	All Other Packages.....	150°C
LT6003I, LT6004I, LT6005I.....	-40°C to 85°C	Storage Temperature Range	
LT6003H, LT6004H, LT6005H.....	-40°C to 125°C	DFN Packages.....	-65°C to 125°C
		All Other Packages.....	-65°C to 150°C
		Lead Temperature (Soldering, 10 sec)	
		TSOT, MSOP, SSOP Packages.....	300°C

PIN CONFIGURATION

<p>LT6003</p> <p>TOP VIEW</p> <p>DC PACKAGE 4-LEAD (2mm × 2mm) PLASTIC DFN</p> <p>$T_{JMAX} = 125^\circ\text{C}$, $\theta_{JA} = 102^\circ\text{C/W}$ (NOTE 2) EXPOSED PAD (PIN 5) IS V^-. MUST BE SOLDERED TO PCB</p>	<p>LT6003</p> <p>TOP VIEW</p> <p>S5 PACKAGE 5-LEAD PLASTIC TSOT-23</p> <p>$T_{JMAX} = 150^\circ\text{C}$, $\theta_{JA} = 250^\circ\text{C/W}$</p>	<p>LT6004</p> <p>TOP VIEW</p> <p>DD PACKAGE 8-LEAD (3mm × 3mm) PLASTIC DFN</p> <p>$T_{JMAX} = 125^\circ\text{C}$, $\theta_{JA} = 160^\circ\text{C/W}$ (NOTE 2) EXPOSED PAD (PIN 9) CONNECTED TO V^-. (PCB CONNECTION OPTIONAL)</p>
<p>LT6004</p> <p>TOP VIEW</p> <p>MS8 PACKAGE 8-LEAD PLASTIC MSOP</p> <p>$T_{JMAX} = 150^\circ\text{C}$, $\theta_{JA} = 250^\circ\text{C/W}$</p>	<p>LT6005</p> <p>TOP VIEW</p> <p>DHC PACKAGE 16-LEAD (5mm × 3mm) PLASTIC DFN</p> <p>$T_{JMAX} = 125^\circ\text{C}$, $\theta_{JA} = 160^\circ\text{C/W}$ (NOTE 2) EXPOSED PAD (PIN 17) CONNECTED TO V^-. (PCB CONNECTION OPTIONAL)</p>	<p>LT6005</p> <p>TOP VIEW</p> <p>GN PACKAGE 16-LEAD PLASTIC SSOP</p> <p>$T_{JMAX} = 150^\circ\text{C}$, $\theta_{JA} = 135^\circ\text{C/W}$</p>

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LT6003CDC#PBF	LT6003CDC#TRPBF	LCKF	4-Lead (2mm × 2mm) Plastic DFN	0°C to 70°C
LT6003IDC#PBF	LT6003IDC#TRPBF	LCKF	4-Lead (2mm × 2mm) Plastic DFN	-40°C to 85°C
LT6003HDC#PBF	LT6003HDC#TRPBF	LCKF	4-Lead (2mm × 2mm) Plastic DFN	-40°C to 125°C
LT6003CS5#PBF	LT6003CS5#TRPBF	LTCKG	5-Lead Plastic TSOT-23	0°C to 70°C
LT6003IS5#PBF	LT6003IS5#TRPBF	LTCKG	5-Lead Plastic TSOT-23	-40°C to 85°C
LT6003HS5#PBF	LT6003HS5#TRPBF	LTCKG	5-Lead Plastic TSOT-23	-40°C to 125°C
LT6004CDD#PBF	LT6004CDD#TRPBF	LCCB	8-Lead (3mm × 3mm) Plastic DFN	0°C to 70°C
LT6004IDD#PBF	LT6004IDD#TRPBF	LCCB	8-Lead (3mm × 3mm) Plastic DFN	-40°C to 85°C
LT6004HDD#PBF	LT6004HDD#TRPBF	LCCB	8-Lead (3mm × 3mm) Plastic DFN	-40°C to 125°C
LT6004CMS8#PBF	LT6004CMS8#TRPBF	LTCBZ	8-Lead Plastic MSOP	0°C to 70°C
LT6004IMS8#PBF	LT6004IMS8#TRPBF	LTCBZ	8-Lead Plastic MSOP	-40°C to 85°C
LT6004HMS8#PBF	LT6004HMS8#TRPBF	LTCBZ	8-Lead Plastic MSOP	-40°C to 125°C
LT6005CDHC#PBF	LT6005CDHC#TRPBF	6005	16-Lead (5mm × 3mm) Plastic DFN	0°C to 70°C
LT6005IDHC#PBF	LT6005IDHC#TRPBF	6005	16-Lead (5mm × 3mm) Plastic DFN	-40°C to 85°C
LT6005HDHC#PBF	LT6005HDHC#TRPBF	6005	16-Lead (5mm × 3mm) Plastic DFN	-40°C to 125°C
LT6005CGN#PBF	LT6005CGN#TRPBF	6005	16-Lead Plastic SSOP	0°C to 70°C
LT6005IGN#PBF	LT6005IGN#TRPBF	6005I	16-Lead Plastic SSOP	-40°C to 85°C
LT6005HGN#PBF	LT6005HGN#TRPBF	6005H	16-Lead Plastic SSOP	-40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container. Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandree/>

ELECTRICAL CHARACTERISTICS (LT6003C/I, LT6004C/I, LT6005C/I) The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_S = 1.8V, 0V, V_{CM} = 0.5V; V_S = 5V, 0V, V_{CM} = 2.5V, V_{OUT} = half supply, R_L to ground, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V _{OS}	Input Offset Voltage	LT6003S5, LT6004MS8 0°C ≤ T _A ≤ 70°C	●	175	500	μV
		-40°C ≤ T _A ≤ 85°C	●		725	μV
					950	μV
		LT6005GN 0°C ≤ T _A ≤ 70°C	●	190	650	μV
				925	μV	
		-40°C ≤ T _A ≤ 85°C	●		1.15	mV
		LT6004DD, LT6005DHC 0°C ≤ T _A ≤ 70°C	●	290	850	μV
		-40°C ≤ T _A ≤ 85°C	●		1.15	mV
					1.4	mV
		LT6003DC 0°C ≤ T _A ≤ 70°C	●	290	950	μV
		-40°C ≤ T _A ≤ 85°C	●		1.3	mV
					1.6	mV
ΔV _{OS} /ΔT	Input Offset Voltage Drift (Note 5)	S5, MS8, GN	●	2	5	μV/°C
		DC, DD, DHC	●	2	7	μV/°C

LT6003/LT6004/LT6005

ELECTRICAL CHARACTERISTICS (LT6003C/I, LT6004C/I, LT6005C/I) The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $V_S = 1.8\text{V}, 0\text{V}$, $V_{CM} = 0.5\text{V}$; $V_S = 5\text{V}, 0\text{V}$, $V_{CM} = 2.5\text{V}$, $V_{OUT} = \text{half supply}$, R_L to ground, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_B	Input Bias Current (Note 7)	$V_{CM} = 0.3\text{V}, 0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$	●	5	90	pA
		$V_{CM} = V^+ - 0.3\text{V}, 0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$	●	40	140	pA
		$V_{CM} = 0.3\text{V}, -40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	●	5	120	pA
		$V_{CM} = V^+ - 0.3\text{V}, -40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	●	40	170	pA
		$V_{CM} = 0\text{V}$	●	0.13	1.4	nA
I_{OS}	Input Offset Current (Note 7)	$V_{CM} = 0.3\text{V}$	●	5	80	pA
		$V_{CM} = V^+ - 0.3\text{V}$	●	7	80	pA
		$V_{CM} = 0\text{V}$	●	5	100	pA
	Input Noise Voltage	0.1Hz to 10Hz		3		μV_{P-P}
e_n	Input Noise Voltage Density	$f = 100\text{Hz}$		325		$\text{nV}/\sqrt{\text{Hz}}$
i_n	Input Noise Current Density	$f = 100\text{Hz}$		12		$\text{fA}/\sqrt{\text{Hz}}$
R_{IN}	Input Resistance	Differential		10		$\text{G}\Omega$
		Common Mode		2000		$\text{G}\Omega$
C_{IN}	Input Capacitance			6		pF
CMRR	Common Mode Rejection Ratio (Note 7)	$V_S = 1.8\text{V}$				
		$V_{CM} = 0\text{V to } 0.7\text{V}$	●	73	100	dB
		$V_{CM} = 0\text{V to } 1.8\text{V}, \text{S5, MS8, GN}$	●	63	80	dB
		$V_{CM} = 0\text{V to } 1.8\text{V}, \text{DC, DD, DHC}$	●	60	78	dB
	$V_S = 5\text{V}$					
	$V_{CM} = 0\text{V to } 3.9\text{V}$	●	88	115	dB	
	$V_{CM} = 0\text{V to } 5\text{V}, \text{S5, MS8, GN}$	●	72	90	dB	
	$V_{CM} = 0\text{V to } 5\text{V}, \text{DC, DD, DHC}$	●	69	86	dB	
	Input Offset Voltage Shift (Note 7)	$V_{CM} = 0\text{V to } V^+ - 1.1\text{V}$	●	7	155	μV
		$V_{CM} = 0\text{V to } V^+, \text{S5, MS8, GN}$	●	0.16	1.3	mV
		$V_{CM} = 0\text{V to } V^+, \text{DC, DD, DHC}$	●	0.23	1.8	mV
	Input Voltage Range	Guaranteed by CMRR	●	0	V^+	V
PSRR	Power Supply Rejection Ratio	$V_S = 1.6\text{V to } 6\text{V}, V_{CM} = 0.5\text{V}, 0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$	●	80	95	dB
		$V_S = 1.7\text{V to } 6\text{V}, V_{CM} = 0.5\text{V}, -40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	●	78	95	dB
	Minimum Supply Voltage	Guaranteed by PSRR, $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$	●	1.6		V
		$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	●	1.7		V
A_{VOL}	Large Signal Voltage Gain (Note 7)	$V_S = 1.8\text{V}$		25	150	V/mV
		$R_L = 20\text{k}\Omega, V_{OUT} = 0.25\text{V to } 1.25\text{V}$	●	15		V/mV
	$V_S = 5\text{V}$		100	500	V/mV	
	$R_L = 20\text{k}\Omega, V_{OUT} = 0.25\text{V to } 4.25\text{V}$	●	60		V/mV	
V_{OL}	Output Swing Low (Notes 6, 8)	No Load	●	15	50	mV
		$I_{SINK} = 100\mu\text{A}$	●	110	240	mV
V_{OH}	Output Swing High (Notes 6, 9)	No Load	●	45	100	mV
		$I_{SOURCE} = 100\mu\text{A}$	●	200	350	mV
I_{SC}	Short Circuit Current (Note 8)	Short to GND		2	5	mA
		$0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$	●	1.5		mA
		$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	●	0.5		mA
		Short to V^+		2	7	mA
	$0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$	●	1.5		mA	
	$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	●	0.5		mA	
I_S	Supply Current per Amplifier	$V_S = 1.8\text{V}$		0.85	1	μA
		$0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$	●		1.4	μA
		$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	●		1.6	μA
		$V_S = 5\text{V}$		1	1.2	μA
	$0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$	●		1.6	μA	
	$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	●		1.9	μA	

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ELECTRICAL CHARACTERISTICS (LT6003C/I, LT6004C/I, LT6005C/I) The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $V_S = 1.8\text{V}$, 0V , $V_{CM} = 0.5\text{V}$; $V_S = 5\text{V}$, 0V , $V_{CM} = 2.5\text{V}$, $V_{OUT} = \text{half supply}$, R_L to ground, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
GBW	Gain Bandwidth Product	$f = 100\text{Hz}$		2		kHz
SR	Slew Rate (Note 11)	$A_V = -1$, $R_F = R_G = 1\text{M}\Omega$ $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	● ●	0.55 0.4 0.2	0.8	V/ms V/ms V/ms
FPBW	Full Power Bandwidth	$V_{OUT} = 1.5V_{P-P}$ (Note 10)		170		Hz

(LT6003H, LT6004H, LT6005H) The ● denotes the specifications which apply over the full specified temperature range of $-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$. $V_S = 1.8\text{V}$, 0V , $V_{CM} = 0.5\text{V}$; $V_S = 5\text{V}$, 0V , $V_{CM} = 2.5\text{V}$, $V_{OUT} = \text{half supply}$, R_L to ground, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	LT6003S5, LT6004MS8 LT6005GN LT6004DD, LT6005DHC LT6003DC	● ● ●		1.5 1.7 1.9 2.1	mV mV mV mV
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift (Note 5)	S5, MS8, GN DC, DD, DHC	● ●	2 3	6 8	$\mu\text{V}/^\circ\text{C}$ $\mu\text{V}/^\circ\text{C}$
I_B	Input Bias Current (Note 7)	LT6003, $V_{CM} = 0.3\text{V}$, $V^+ - 0.3\text{V}$ LT6004, LT6005, $V_{CM} = 0.3\text{V}$, $V^+ - 0.3\text{V}$	● ●		6 12	nA nA
I_{OS}	Input Offset Current (Note 7)	LT6003, $V_{CM} = 0.3\text{V}$, $V^+ - 0.3\text{V}$ LT6004, LT6005, $V_{CM} = 0.3\text{V}$, $V^+ - 0.3\text{V}$	● ●		2 4	nA nA
CMRR	Common Mode Rejection Ratio (Note 7)	$V_S = 1.8\text{V}$ $V_{CM} = 0.3\text{V}$ to 0.7V $V_{CM} = 0.3\text{V}$ to 1.5V , S5, MS8, GN $V_{CM} = 0.3\text{V}$ to 1.5V , DC, DD, DHC	● ● ●	67 57 55		dB dB dB
		$V_S = 5\text{V}$ $V_{CM} = 0.3\text{V}$ to 3.9V $V_{CM} = 0.3\text{V}$ to 4.7V , S5, MS8, GN $V_{CM} = 0.3\text{V}$ to 4.7V , DC, DD, DHC	● ● ●	86 68 66		dB dB dB
	Input Offset Voltage Shift (Note 7)	$V_{CM} = 0.3\text{V}$ to $V^+ - 1.1\text{V}$ $V_{CM} = 0.3\text{V}$ to $V^+ - 0.3\text{V}$, S5, MS8, GN $V_{CM} = 0.3\text{V}$ to $V^+ - 0.3\text{V}$, DC, DD, DHC	● ● ●		180 1.7 2.2	μV mV mV
	Input Voltage Range	Guaranteed by CMRR	●	0.3	$V^+ - 0.3\text{V}$	V
PSRR	Power Supply Rejection Ratio	$V_S = 1.7\text{V}$ to 6V , $V_{CM} = 0.5\text{V}$	●	76		dB
	Minimum Supply	Guaranteed by PSRR	●	1.7		V
A_{VOL}	Large Signal Voltage Gain (Note 7)	$V_S = 1.8\text{V}$, $R_L = 20\text{k}\Omega$, $V_{OUT} = 0.4\text{V}$ to 1.25V $V_S = 5\text{V}$, $R_L = 20\text{k}\Omega$, $V_{OUT} = 0.4\text{V}$ to 4.25V	● ●	4 20		V/mV V/mV
V_{OL}	Output Swing Low (Notes 6, 8)	No Load $I_{SINK} = 100\mu\text{A}$	● ●		60 275	mV mV
V_{OH}	Output Swing High (Notes 6, 9)	No Load $I_{SOURCE} = 100\mu\text{A}$	● ●		120 400	mV mV
I_{SC}	Short Circuit Current (Note 8)	Short to GND Short to V^+	● ●	0.5 0.5		mA mA
I_S	Supply Current per Amplifier	$V_S = 1.8\text{V}$ $V_S = 5\text{V}$	● ●		2.2 2.5	μA μA
SR	Slew Rate (Note 11)	$A_V = -1$, $R_F = R_G = 1\text{M}\Omega$	●	0.2		V/ms

LT6003/LT6004/LT6005

ELECTRICAL CHARACTERISTICS (LT6003C/I, LT6004C/I, LT6005C/I) The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $V_S = \pm 8\text{V}$, $V_{CM} = V_{OUT} = \text{half supply}$, R_L to ground, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	LT6003S5, LT6004MS8 $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	●	185	600	μV
			●		825	μV
			●		1.05	mV
			●			
	LT6005GN $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	●	200	750	μV	
		●		1.05	mV	
		●		1.25	mV	
	LT6004DD, LT6005DHC $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	●	300	950	μV	
		●		1.25	mV	
		●		1.5	mV	
	LT6003DC $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	●	0.3	1.05	mV	
		●		1.4	mV	
		●		1.65	mV	
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift (Note 5)	S5, MS8, GN	●	2	5	$\mu\text{V}/^\circ\text{C}$
		DC, DD, DHC	●	2	7	$\mu\text{V}/^\circ\text{C}$
I_B	Input Bias Current	$0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$	●	7	100	pA
		$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	●	7	150	pA
I_{OS}	Input Offset Current		●	7	90	pA
		Input Noise Voltage		3		μV_{P-P}
e_n	Input Noise Voltage Density	$f = 100\text{Hz}$		325		$\text{nV}/\sqrt{\text{Hz}}$
i_n	Input Noise Current Density	$f = 100\text{Hz}$		12		$\text{fA}/\sqrt{\text{Hz}}$
R_{IN}	Input Resistance	Differential		10		$\text{G}\Omega$
		Common Mode		2000		$\text{G}\Omega$
C_{IN}	Input Capacitance			6		pF
CMRR	Common Mode Rejection Ratio	$V_{CM} = -8\text{V to } 6.9\text{V}$	●	92	120	dB
		$V_{CM} = -8\text{V to } 8\text{V}$, S5, MS8, GN	●	82	100	dB
		$V_{CM} = -8\text{V to } 8\text{V}$, DC, DD, DHC	●	78	96	dB
	Input Offset Voltage Shift	$V_{CM} = -8\text{V to } 6.9\text{V}$	●	15	375	μV
		$V_{CM} = -8\text{V to } 8\text{V}$, S5, MS8, GN	●	0.16	1.3	mV
		$V_{CM} = -8\text{V to } 8\text{V}$, DC, DD, DHC	●	0.25	2	mV
	Input Voltage Range	Guaranteed by CMRR	●	-8	8	V
PSRR	Power Supply Rejection Ratio	$V_S = \pm 1.1\text{V to } \pm 8\text{V}$	●	86	105	dB
A_{VOL}	Large Signal Voltage Gain	$R_L = 100\text{k}\Omega$, $V_{OUT} = -7.3\text{V to } 7.3\text{V}$		350		V/mV
V_{OL}	Output Swing Low (Notes 6, 8)	No Load	●	10	50	mV
		$I_{SINK} = 100\mu\text{A}$	●	105	240	mV
V_{OH}	Output Swing High (Notes 6, 9)	No Load	●	50	120	mV
		$I_{SOURCE} = 100\mu\text{A}$	●	195	350	mV
I_{SC}	Short Circuit Current	Short to GND	●	4	9	mA
		$0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$	●	3		mA
		$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	●	1		mA
I_S	Supply Current per Amplifier	$0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$	●	1.25	1.5	μA
		$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	●		1.9	μA
			●		2.2	μA
GBW	Gain Bandwidth Product	$f = 100\text{Hz}$		3		kHz
SR	Slew Rate (Note 11)	$A_V = -1$, $R_F = R_G = 1\text{M}\Omega$	●	0.55	1.3	V/ms
		$0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$	●	0.4		V/ms
		$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	●	0.2		V/ms
FPBW	Full Power Bandwidth	$V_{OUT} = 14\text{V}_{P-P}$ (Note 10)		30		Hz

ELECTRICAL CHARACTERISTICS (LT6003H, LT6004H, LT6005H) The ● denotes the specifications which apply over the full specified temperature range of $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$. $V_S = \pm 8\text{V}$, $V_{\text{CM}} = V_{\text{OUT}} = \text{half supply}$, R_L to ground, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	LT6003S5, LT6004MS8	●		1.6	mV
		LT6005GN	●		1.8	mV
		LT6004DD, LT6005DHC	●		2	mV
		LT6003DC	●		2.2	mV
$\Delta V_{\text{OS}}/\Delta T$	Input Offset Voltage Drift (Note 5)	S5, MS8, GN	●	2	6	$\mu\text{V}/^{\circ}\text{C}$
		DC, DD, DHC	●	3	8	$\mu\text{V}/^{\circ}\text{C}$
I_B	Input Bias Current	LT6003	●		6	nA
		LT6004, LT6005	●		12	nA
I_{OS}	Input Offset Current	LT6003	●		2	nA
		LT6004, LT6005	●		4	nA
CMRR	Common Mode Rejection Ratio	$V_{\text{CM}} = -7.7\text{V}$ to 6.9V	●	90		dB
		$V_{\text{CM}} = -7.7\text{V}$ to 7.7V , S5, MS8, GN	●	78		dB
		$V_{\text{CM}} = -7.7\text{V}$ to 7.7V , DC, DD, DHC	●	76		dB
	Input Offset Voltage Shift	$V_{\text{CM}} = -7.7\text{V}$ to 6.9V	●		460	μV
		$V_{\text{CM}} = -7.7\text{V}$ to 7.7V , S5, MS8, GN	●		1.9	mV
		$V_{\text{CM}} = -7.7\text{V}$ to 7.7V , DC, DD, DHC	●		2.5	mV
	Input Voltage Range	Guaranteed by CMRR	●	-7.7	7.7	V
PSRR	Power Supply Rejection Ratio	$V_S = \pm 1.1\text{V}$ to $\pm 8\text{V}$	●	84		dB
V_{OL}	Output Swing Low (Notes 6, 8)	No Load	●		60	mV
		$I_{\text{SINK}} = 100\mu\text{A}$	●		275	mV
V_{OH}	Output Swing High (Note 6)	No Load	●		140	mV
		$I_{\text{SOURCE}} = 100\mu\text{A}$	●		400	mV
I_{SC}	Short Circuit Current	Short to GND	●	1		mA
I_S	Supply Current per Amplifier		●		3	μA
SR	Slew Rate (Note 11)	$A_V = -1$, $R_F = R_G = 1\text{M}\Omega$	●	0.2		V/ms

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: A heat sink may be required to keep the junction temperature below absolute maximum. This depends on the power supply voltage and how many amplifiers are shorted. The θ_{JA} specified for the DC, DD and DHC packages is with minimal PCB heat spreading metal. Using expanded metal area on all layers of a board reduces this value.

Note 3: The LT6003C/LT6004C/LT6005C and LT6003I/LT6004I/LT6005I are guaranteed functional over the temperature range of -40°C to 85°C . The LT6003H/LT6004H/LT6005H are guaranteed functional over the operating temperature range of -40°C to 125°C .

Note 4: The LT6003C/LT6004C/LT6005C are guaranteed to meet specified performance from 0°C to 70°C . The LT6003I/LT6004I/LT6005I are designed, characterized and expected to meet specified performance from

-40°C to 85°C but are not tested or QA sampled at these temperatures. The LT6003I/LT6004I/LT6005I are guaranteed to meet specified performance from -40°C to 85°C . The LT6003H/LT6004H/LT6005H are guaranteed to meet specified performance from -40°C to 125°C .

Note 5: This parameter is not 100% tested.

Note 6: Output voltage swings are measured between the output and power supply rails.

Note 7: Limits are guaranteed by correlation to $V_S = 5\text{V}$ tests.

Note 8: Limits are guaranteed by correlation to $V_S = 1.8\text{V}$ tests

Note 9: Limits are guaranteed by correlation to $V_S = \pm 8\text{V}$ tests

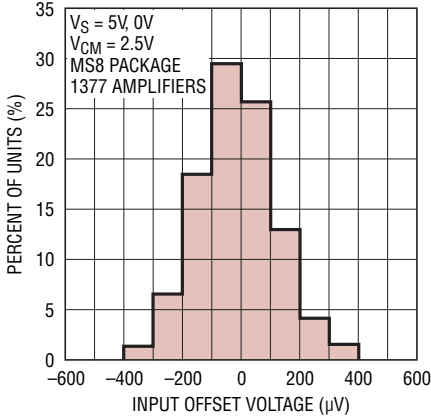
Note 10: Full-power bandwidth is calculated from the slew rate:

$$\text{FPBW} = \text{SR}/\pi V_{\text{P-P}}$$

Note 11: Slew rate measured at $V_S = 1.8\text{V}$, $V_{\text{OUT}} = 0.4\text{V}$ to 1.4V is used to guarantee by correlation the slew rate at $V_S = 5\text{V}$, $V_{\text{OUT}} = 1\text{V}$ to 4V and the slew rate at $V_S = \pm 8\text{V}$, $V_{\text{OUT}} = -5\text{V}$ to 5V .

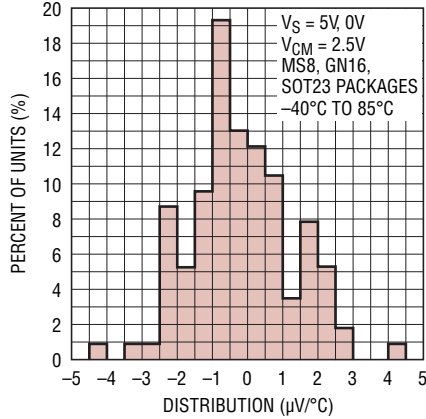
TYPICAL PERFORMANCE CHARACTERISTICS

V_{OS} Distribution



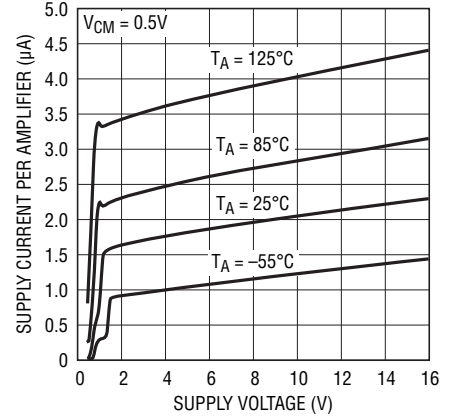
600345 G01

TC V_{OS} Distribution



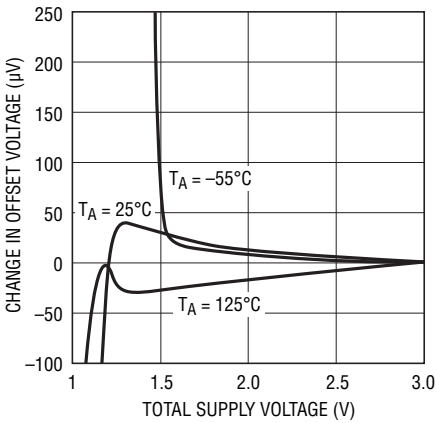
600345 G02

Supply Current vs Supply Voltage



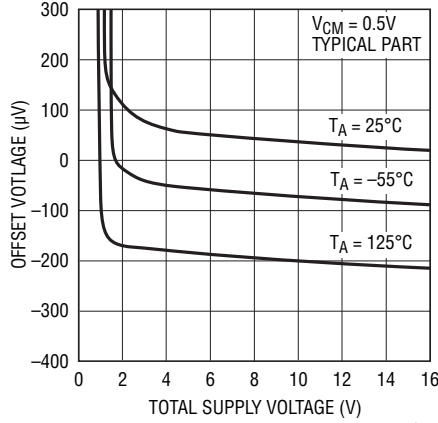
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Change in Input Offset Voltage vs Total Supply Voltage



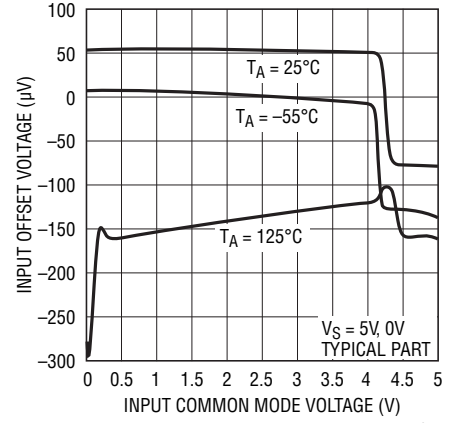
600345 G04

Input Offset Voltage vs Total Supply Voltage



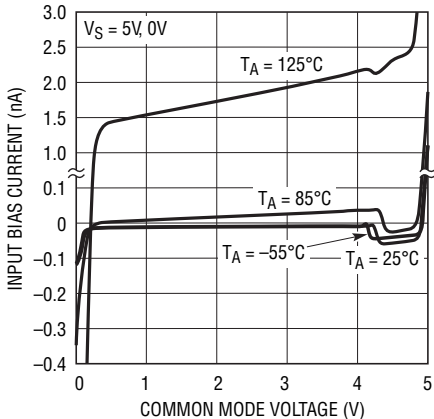
60012 G05

Input Offset Voltage vs Input Common Mode Voltage



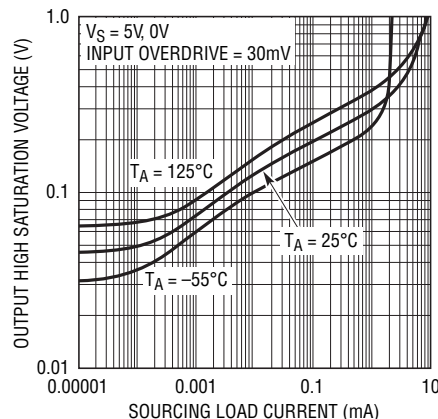
600345 G06

Input Bias Current vs Common Mode Voltage



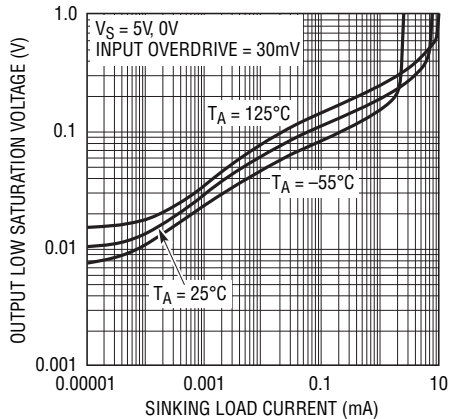
600345 G07

Output Saturation Voltage vs Load Current (Output High)



600345 G08

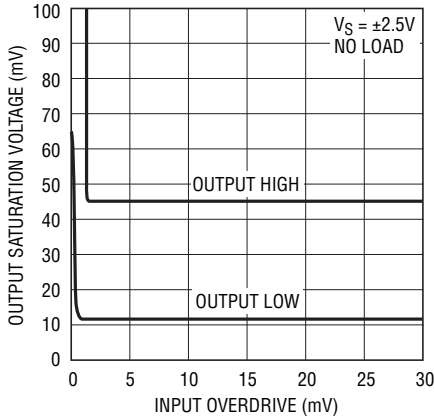
Output Saturation Voltage vs Load Current (Output Low)



600345 G09

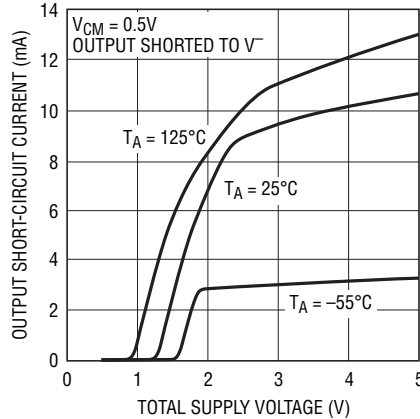
TYPICAL PERFORMANCE CHARACTERISTICS

Output Saturation Voltage vs Input Overdrive



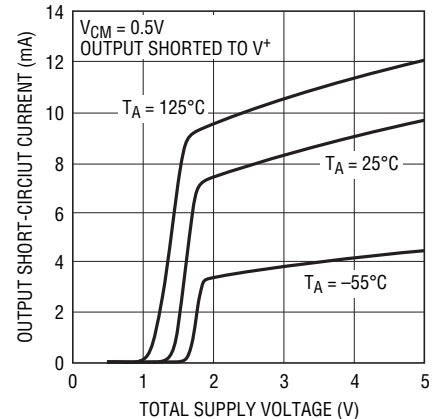
600345 G10

Output Short-Circuit Current vs Total Supply Voltage (Sourcing)



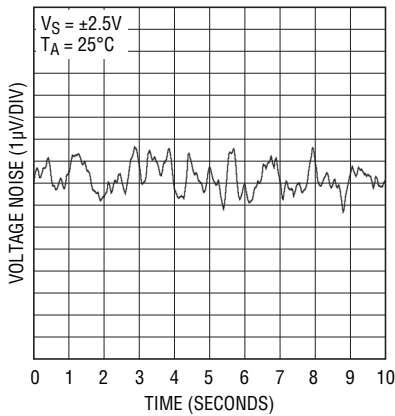
600345 G11

Output Short-Circuit Current vs Total Supply Voltage (Sinking)



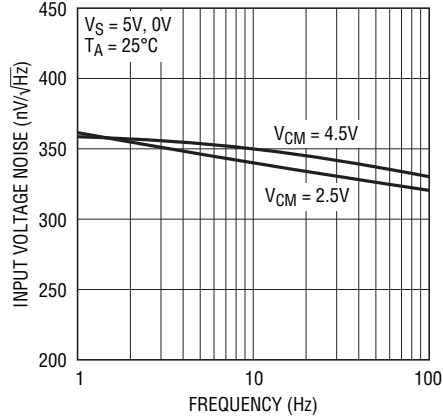
600345 G12

0.1Hz to 10Hz Voltage Noise



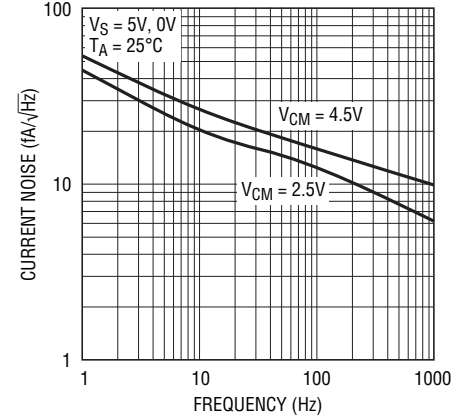
600345 G13

Voltage Noise vs Frequency



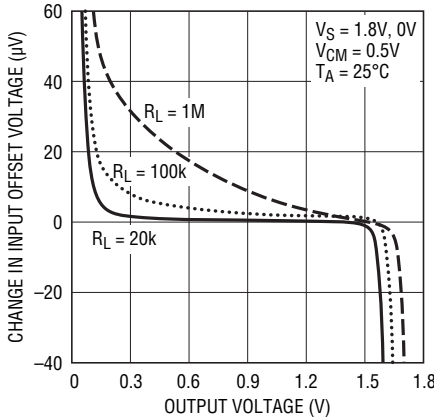
600345 G14

Current Noise vs Frequency



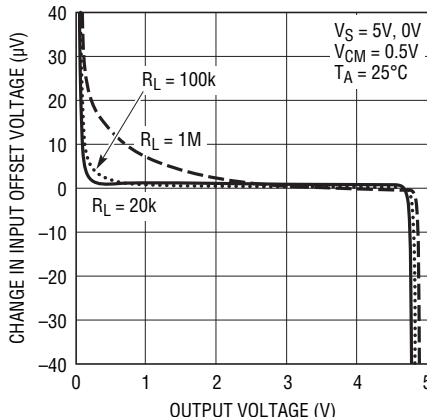
600345 G15

Open-Loop Gain



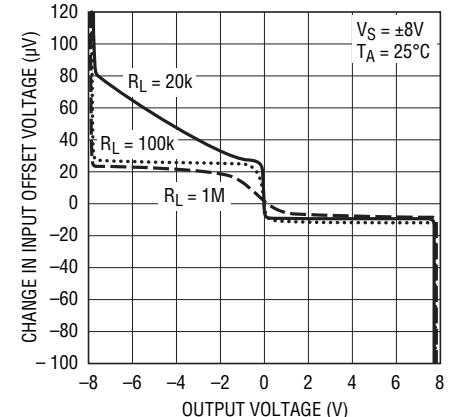
600345 G16

Open-Loop Gain



600345 G17

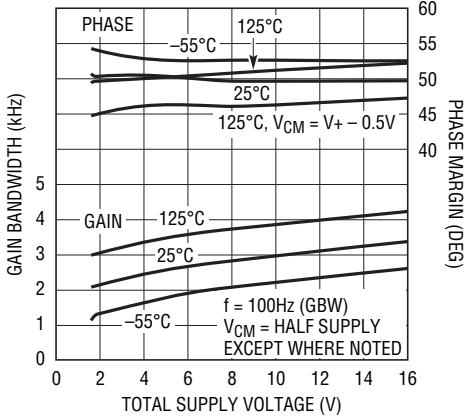
Open-Loop Gain



600345 G18

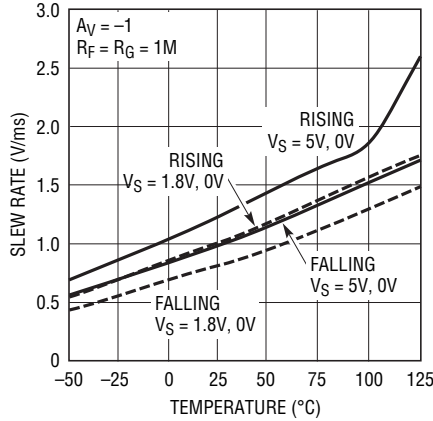
TYPICAL PERFORMANCE CHARACTERISTICS

Gain Bandwidth and Phase Margin vs Total Supply Voltage



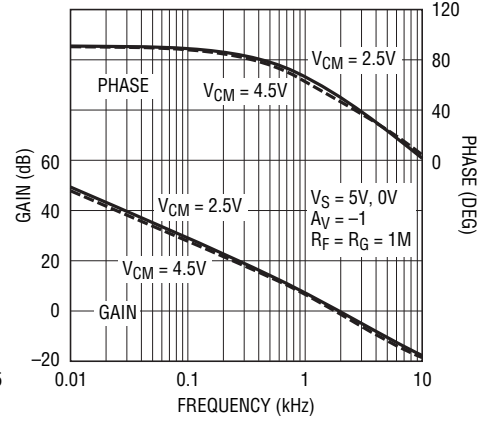
600345 G19

Slew Rate vs Temperature



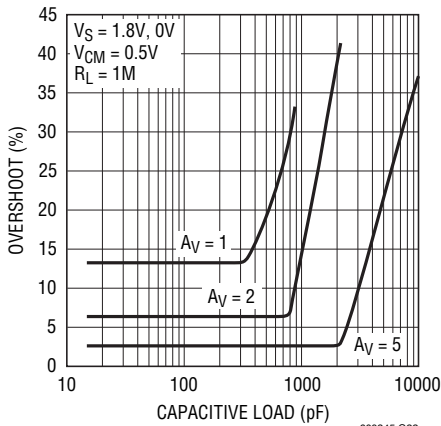
600345 G20

Gain and Phase vs Frequency



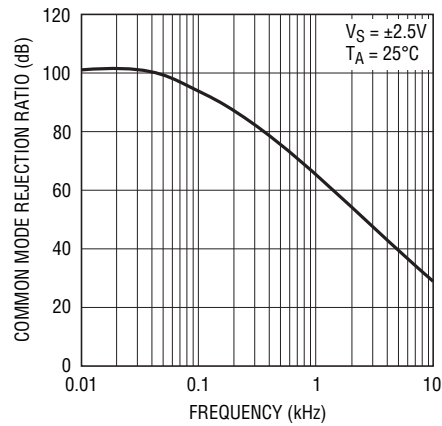
600345 G21

Capacitive Load Handling
Overshoot vs Capacitive Load



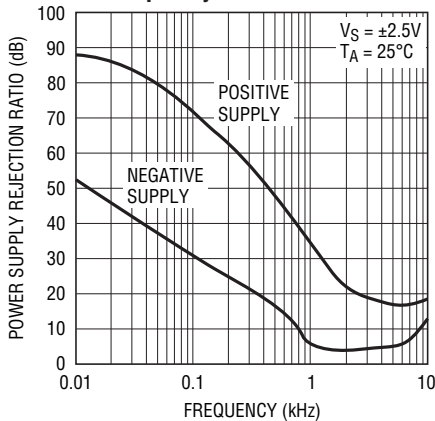
600345 G22

Common Mode Rejection Ratio
vs Frequency



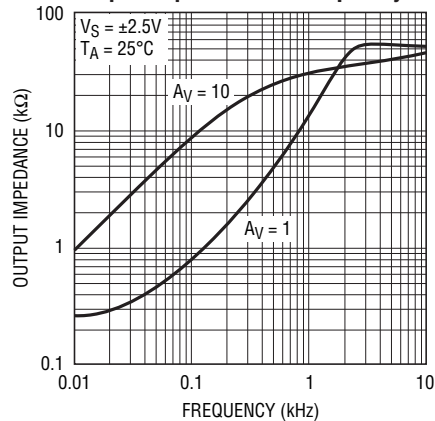
600345 G23

Power Supply Rejection Ratio
vs Frequency



600345 G24

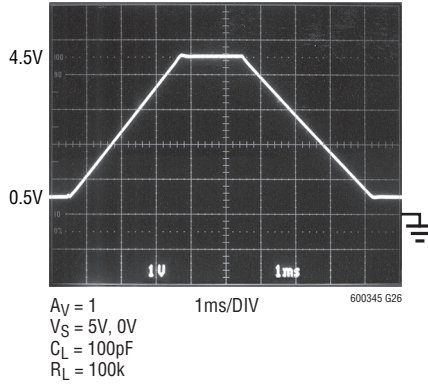
Output Impedance vs Frequency



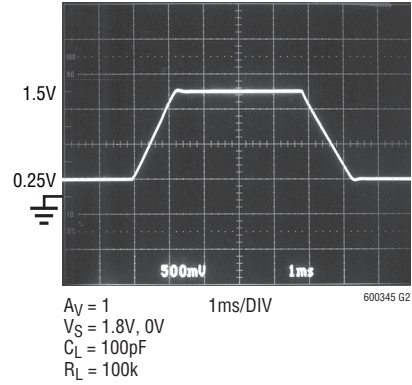
600345 G25

TYPICAL PERFORMANCE CHARACTERISTICS

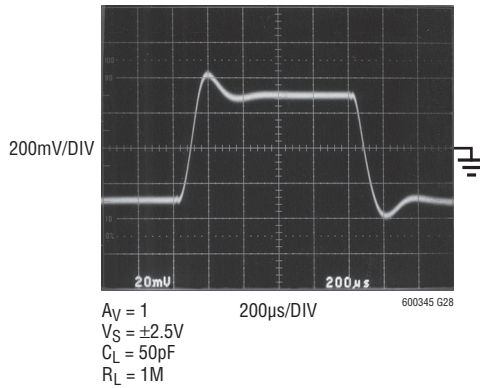
Large-Signal Response



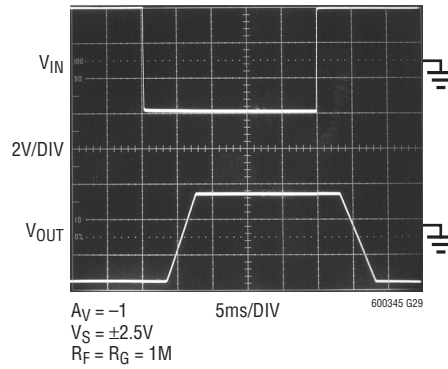
Large-Signal Response



Small-Signal Response



Output Saturation Recovery



SIMPLIFIED SCHEMATIC

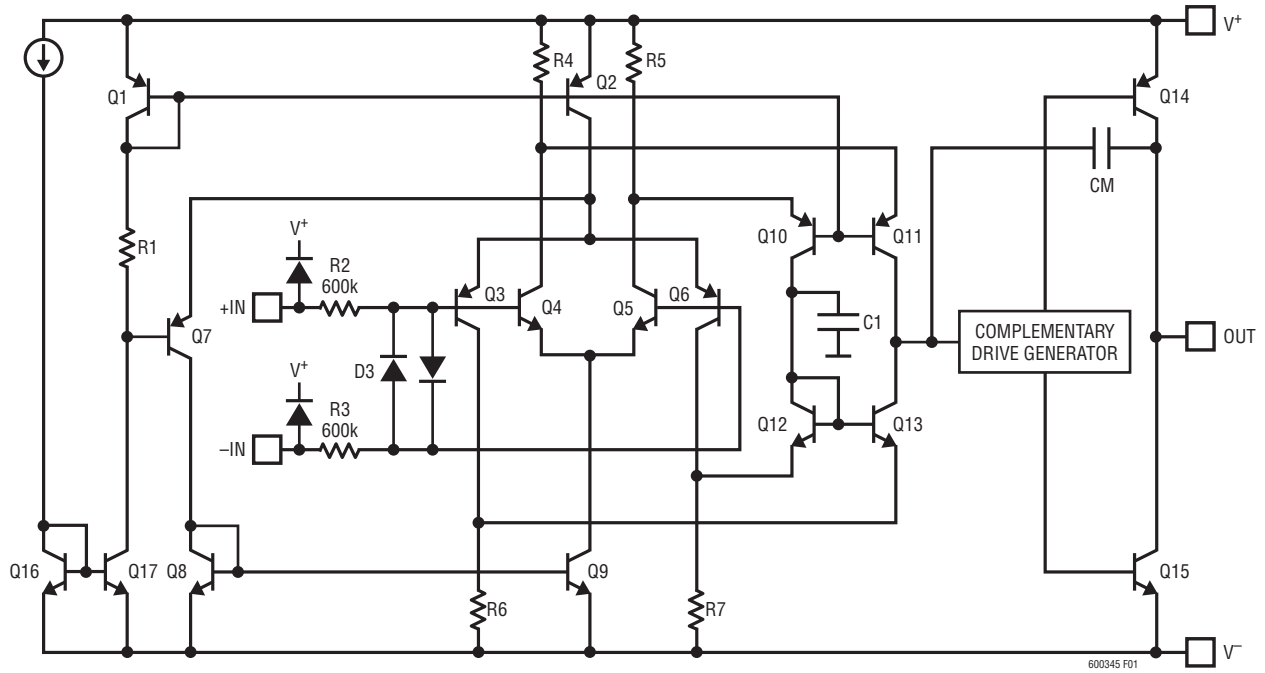


Figure 1

APPLICATIONS INFORMATION

Supply Voltage

The positive supply of the LT6003/LT6004/LT6005 should be bypassed with a small capacitor (about 0.01 μ F) within an inch of the pin. When driving heavy loads, an additional 4.7 μ F electrolytic capacitor should be used. When using split supplies, the same is true for the negative supply pin.

Rail-to-Rail Characteristics

The LT6003/LT6004/LT6005 are fully functional for an input signal range from the negative supply to the positive supply. Figure 1 shows a simplified schematic of the amplifier. The input stage consists of two differential amplifiers, a PNP stage Q3/Q6 and an NPN stage Q4/Q5 that are active over different ranges of the input common mode voltage. The PNP stage is active for common mode voltages, V_{CM} , between the negative supply to approximately 0.9V below the positive supply. As V_{CM} moves closer towards the positive supply, the transistor Q7 will steer Q2's tail current to the current mirror Q8/Q9, activating the NPN differential pair. The PNP pair becomes inactive for the rest of the input common mode voltage range up to the positive supply.

The second stage is a folded cascode and current mirror that converts the input stage differential signals into a single ended output. Capacitor C1 reduces the unity cross frequency and improves the frequency stability without degrading the gain bandwidth of the amplifier. The complementary drive generator supplies current to the output transistors that swing from rail to rail.

Input

Input bias current (I_B) is minimized with cancellation circuitry on both input stages. The cancellation circuitry remains active when V_{CM} is more than 300mV from either rail. As V_{CM} approaches V^- the cancellation circuitry turns off and I_B is determined by the tail current of Q2 and the

beta of the PNP input transistors. As V_{CM} approaches V^+ devices in the cancellation circuitry saturate causing I_B to increase (in the nanoamp range). Input offset voltage errors due to I_B can be minimized by equalizing the noninverting and inverting source impedances.

The input offset voltage changes depending on which input stage is active; input offset voltage is trimmed on both input stages, and is guaranteed to be 500 μ V max in the PNP stage. By trimming the input offset voltage of both input stages, the input offset voltage shift over the entire common mode range (CMRR) is typically 160 μ V, maintaining the precision characteristics of the amplifier.

The input stage of the LT6003/LT6004/LT6005 incorporates phase reversal protection to prevent wrong polarity outputs from occurring when the inputs are driven up to 9V below the negative rail. 600k protective resistors are included in the input leads so that current does not become excessive when the inputs are forced below V^- or when a large differential signal is applied. Input current should be limited to 10mA when the inputs are driven above the positive rail.

Output

The output of the LT6003/LT6004/LT6005 is guaranteed to swing within 100mV of the positive rail and 50mV of the negative rail with no load, over the industrial temperature range. The LT6003/LT6004/LT6005 can typically source 8mA on a single 5V supply. Sourcing current is reduced to 5mA on a single 1.8V supply as noted in the electrical characteristics. However, when sourcing more than 250 μ A with an output load impedance greater than 20k Ω , a 1 μ F capacitor in series with a 2k resistor should be placed from the output to ground to insure stability.

The normally reverse-biased substrate diode from the output to V^- will cause unlimited currents to flow when the output is forced below V^- . If the current is transient and limited to 100mA, no damage will occur.

APPLICATIONS INFORMATION

Gain

The open-loop gain is almost independent of load when the output is sourcing current. This optimizes performance in single supply applications where the load is returned to ground. The Typical Performance Characteristics curve of Open-Loop Gain for various loads shows the details.

Start-Up and Output Saturation Characteristics

Micropower op amps are often not micropower during start-up or during output saturation. This can wreak havoc on limited current supplies. In the worst case there may not be enough supply current available to take the system up to nominal voltages. Unlike the LT6003/LT6004/LT6005, when the output saturates, some op amps may draw excessive current and pull down the supplies, compromising rail-to-rail performance. Figure 2 shows the start-up characteristics of the LT6003/LT6004/LT6005 for three limiting cases. The circuits are shown in Figure 3. One circuit creates a positive offset forcing the output to come up saturated high. Another circuit creates a negative offset forcing the output to come up saturated low, while the last circuit brings the output up at 1/2 supply. In all cases, the supply current is well controlled and is not excessive when the output is on either rail.

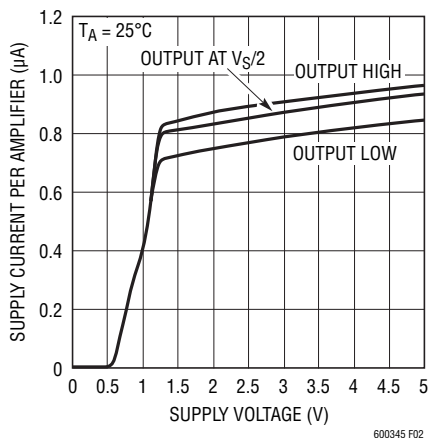


Figure 2. Start-Up Characteristics

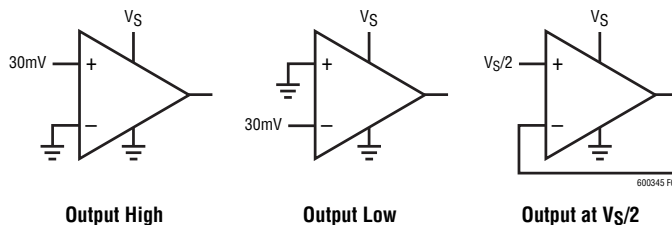
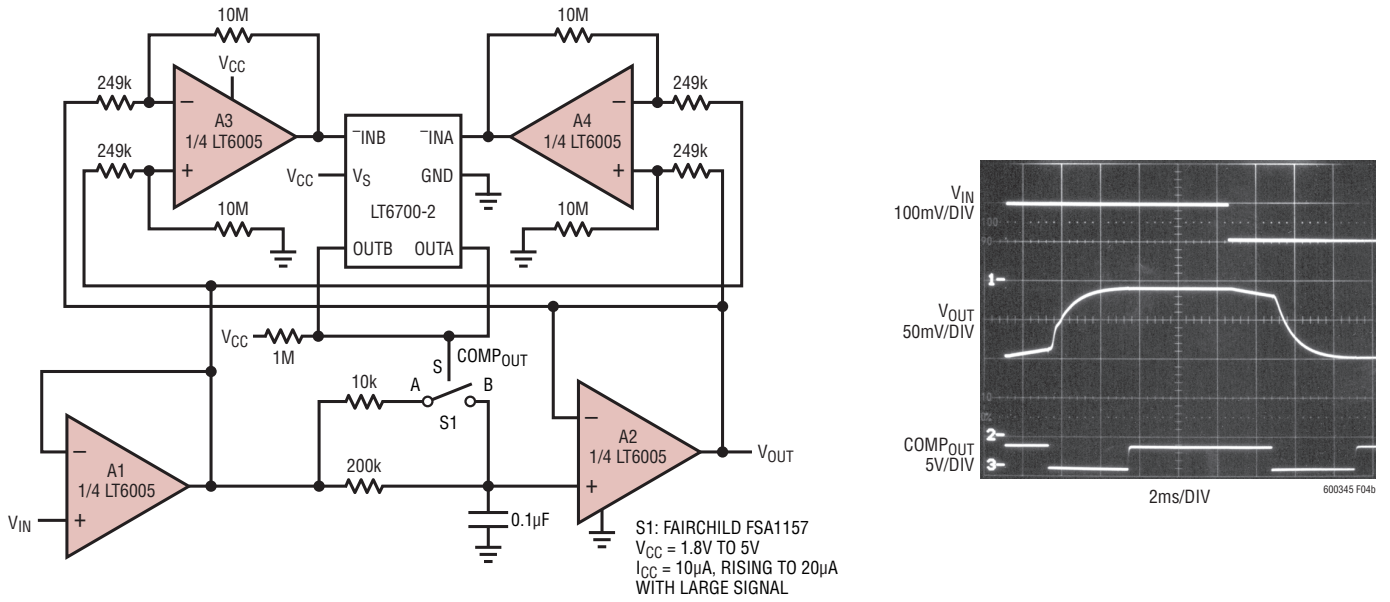


Figure 3. Circuits for Start-Up Characteristics

Adaptive Filter

The circuit of Figure 4 shows the LT6005 applied as a micropower adaptive filter, which automatically adjusts the time constant depending on the signal level. Op amp A1 buffers the input onto the RC which has either a 1ms or 20ms time constant depending on the state of switch S1. The signal is then buffered to the output by op amp A2. Op amps A3 and A4 are configured as gain-of-40 difference amplifiers, gaining up the difference between the buffered input voltage and the output. When there is no difference, the outputs of A3 and A4 will be near zero. When a positive signal step is applied to the input, the output of A3 rises. When a negative signal step is applied to the input, the output of A4 rises. These voltages are fed to the LT6700-2 comparator which has a built in 400mV reference. If the input step exceeds 10mV, the output of the difference amplifiers will exceed 400mV and the comparator output (wired in OR gate fashion) falls low. This turns on S1, reducing the time constant and speeding up the settling. The overall effect is that the circuit provides “slow filtering” with “fast settling.” Waveforms for a 100mV input step are shown in the accompanying photo. The fast 1ms time constant is obvious in the output waveform, while the slow time constant is discernible as the slow ramping sections. That the slow time constant is discernible at all is due to delay time in the difference amplifier and comparator functions.

APPLICATIONS INFORMATION



ADAPTIVE FILTER IMPROVES INHERENT TRADE-OFF OF SETTLING TIME VS NOISE FILTERING. SMALL SIGNAL DC STEPS SETTLE WITH A 20ms TIME CONSTANT FOR AN 8Hz NOISE BANDWIDTH. LARGE STEP SIGNALS (>10mV) CAUSE S1 TO TURN ON, SPEEDING UP THE TIME CONSTANT TO 1ms, FOR IMPROVED SETTLING. AS THE OUTPUT SETTLES BACK TO WITHIN 10mV, S1 TURNS OFF AGAIN, RESTORING THE 20ms TIME CONSTANT, FOR IMPROVED FILTERING.

600345 F04

Figure 4. Adaptive Filter

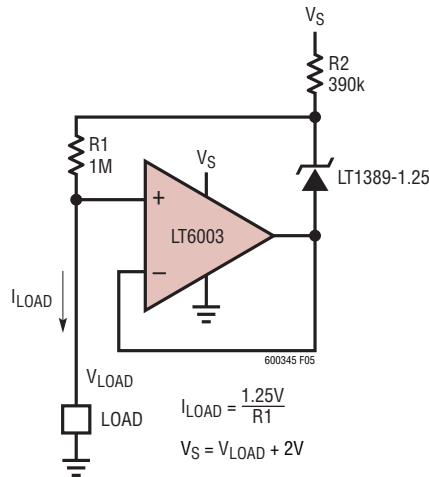
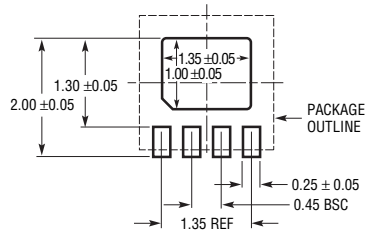


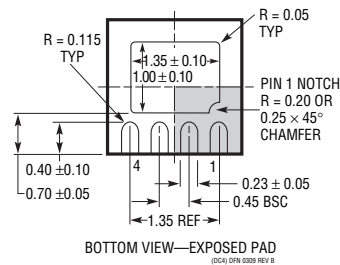
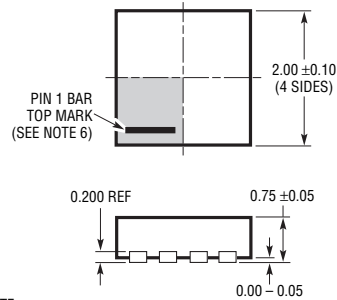
Figure 5. Precision 1.25μA Current Source

PACKAGE DESCRIPTION

DC Package 4-Lead Plastic DFN (2mm × 2mm) (Reference LTC DWG # 05-08-1724 Rev B)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDED

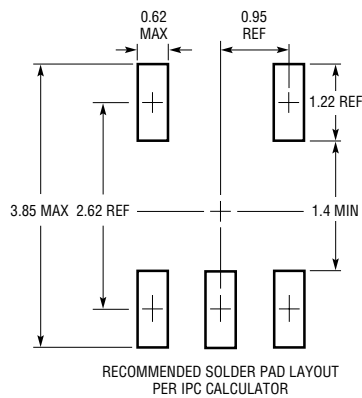


NOTE:

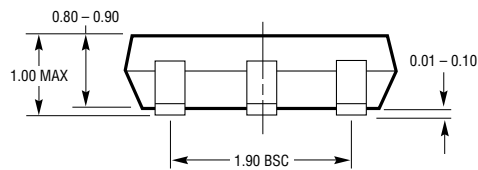
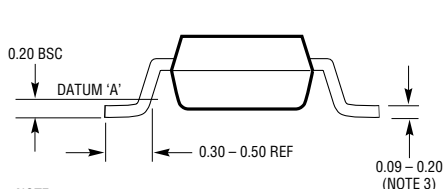
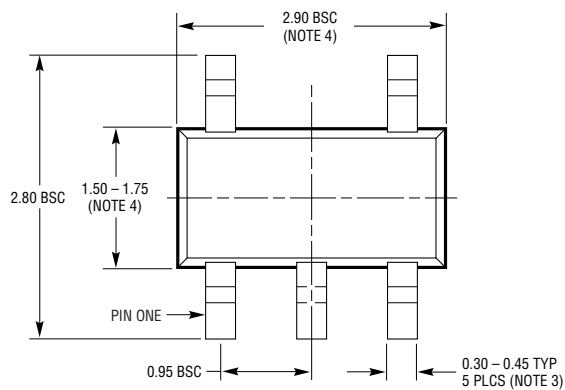
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE

5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

S5 Package 5-Lead Plastic TSOT-23 (Reference LTC DWG # 05-08-1635)



RECOMMENDED SOLDER PAD LAYOUT
PER IPC CALCULATOR



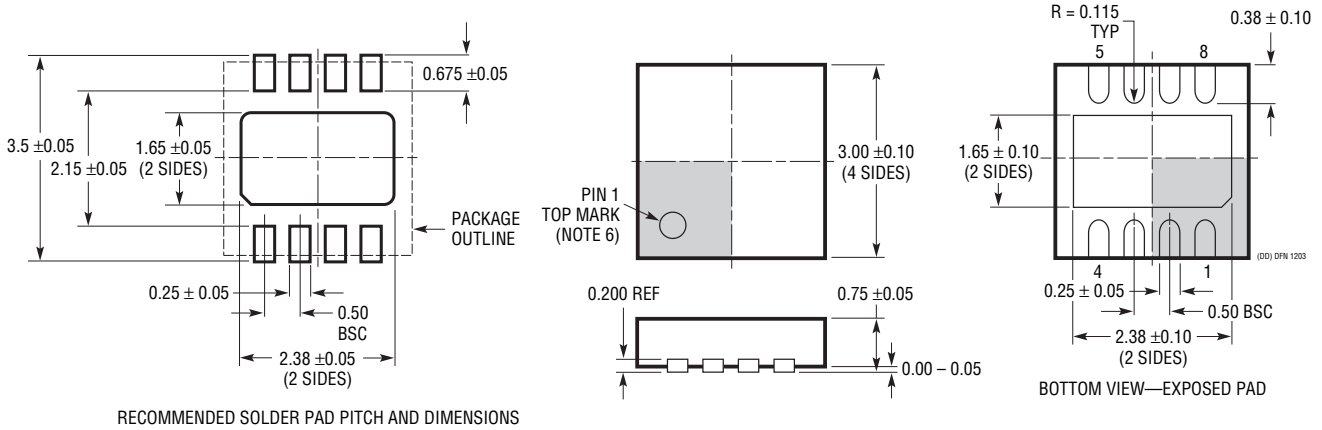
NOTE:

1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE INCLUSIVE OF PLATING
4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
5. MOLD FLASH SHALL NOT EXCEED 0.254mm
6. JEDEC PACKAGE REFERENCE IS MO-193

S5 TSOT-23 0302 REV B

PACKAGE DESCRIPTION

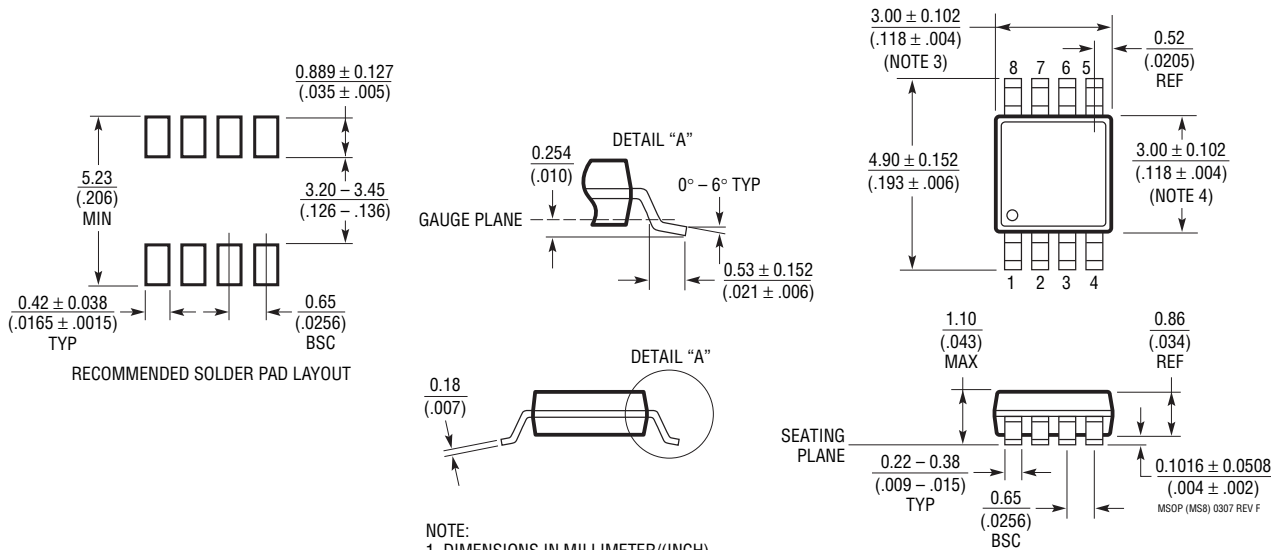
DD Package 8-Lead Plastic DFN (3mm x 3mm) (Reference LTC DWG # 05-08-1698)



NOTE:

1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-1)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON TOP AND BOTTOM OF PACKAGE

MS8 Package 8-Lead Plastic MSOP (Reference LTC DWG # 05-08-1660 Rev F)

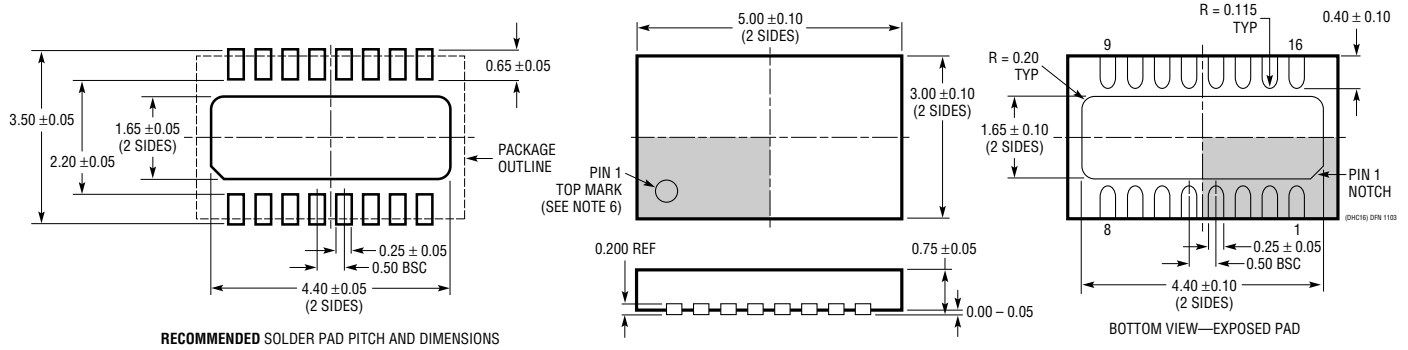


NOTE:

1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

PACKAGE DESCRIPTION

DHC Package 16-Lead Plastic DFN (5mm × 3mm) (Reference LTC DWG # 05-08-1706)

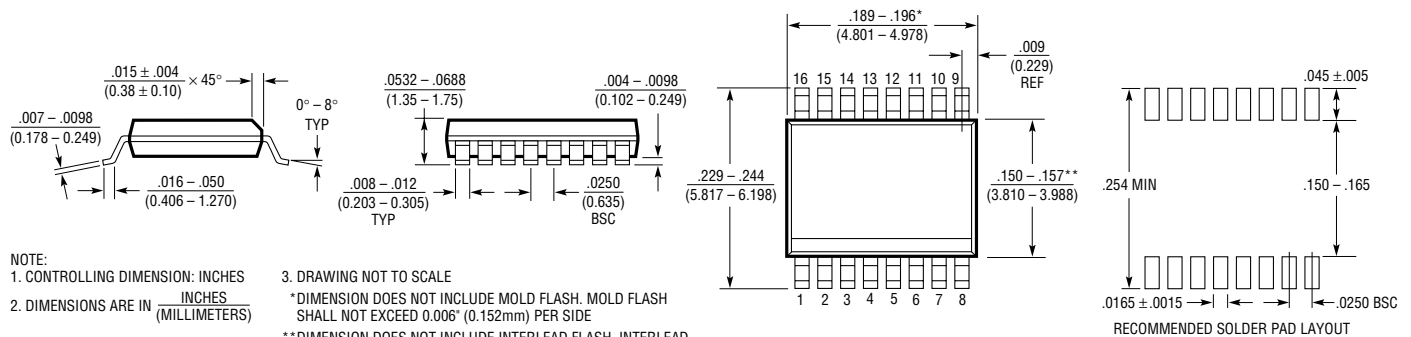


NOTE:

1. DRAWING PROPOSED TO BE MADE VARIATION OF VERSION (WJED-1) IN JEDEC PACKAGE OUTLINE MO-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS

4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

GN Package 16-Lead Plastic SSOP (Narrow .150 Inch) (Reference LTC DWG # 05-08-1641)



NOTE:

1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN $\frac{\text{INCHES}}{\text{MILLIMETERS}}$

3. DRAWING NOT TO SCALE

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

REVISION HISTORY (Revision history begins at Rev D)

REV	DATE	DESCRIPTION	PAGE NUMBER
D	3/11	Changed package description from TSSOP to SSOP in Description, Absolute Maximum Ratings, Pin Configuration, and Order Information	1 to 3