

Current Sense Amplifier, Reference and Comparator with POR

FEATURES

- Current Sense Amplifier
 - Fast Step Response: 500ns
 - Low Offset Voltage: 200 μ V Maximum
 - Low Gain Error: 0.2% Maximum
- Internal 400mV Precision Reference
- Internal Comparator
 - Power-On Reset Capability
 - Fast Response Time: 500ns
 - Total Threshold Error: \pm 1.25% Maximum
- Wide Supply Range: 2.7V to 60V
- Supply Current: 450 μ A
- Specified for -40°C to 125°C Temperature Range
- Available in 8-Lead MSOP and 8-Lead (2mm \times 3mm) DFN Packages

APPLICATIONS

- Overcurrent and Fault Detection
- Current Shunt Measurement
- Battery Monitoring
- Motor Control
- Automotive Monitoring and Control
- Industrial Control

DESCRIPTION

The **LT[®]6118** is a complete high side current sense device that incorporates a precision current sense amplifier, an integrated voltage reference and a latching comparator. The comparator latch functionality can be enabled or disabled and the comparator can be configured to reset upon power-on. The input and the open-drain output of the comparator are independent from the current sense amplifier. The comparator trip point and amplifier gain are configured with external resistors.

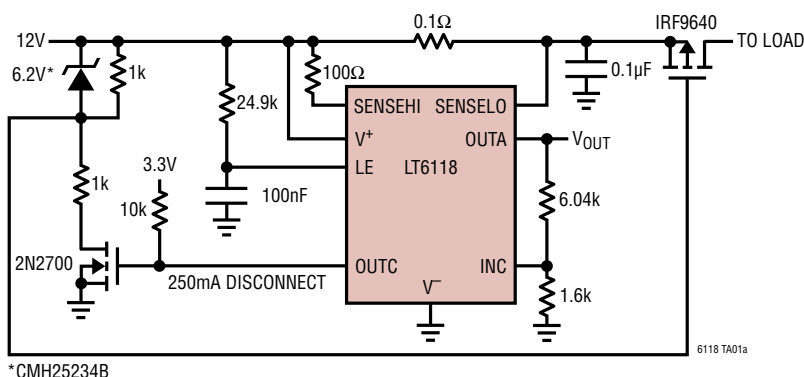
The overall propagation delay of the LT6118 is typically only 1.4 μ s, allowing for quick reaction to overcurrent conditions. The 1MHz bandwidth allows the LT6118 to be used for error detection in critical applications such as motor control. The high threshold accuracy of the comparator, combined with the ability to latch the comparator, ensures the LT6118 can capture high speed events.

The LT6118 is fully specified for operation from -40°C to 125°C , making it suitable for industrial and automotive applications. The LT6118 is available in the small 8-lead MSOP and 8-lead DFN packages.

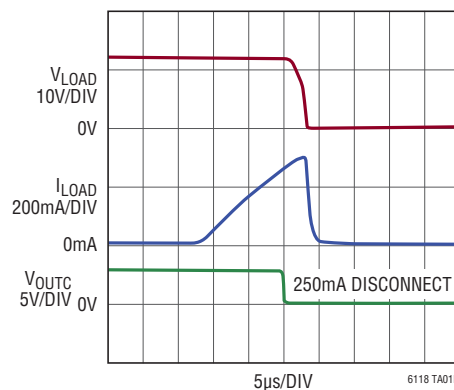
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TYPICAL APPLICATION

Fast Acting Fault Protection with Power-On Reset



Response to Overcurrent Event

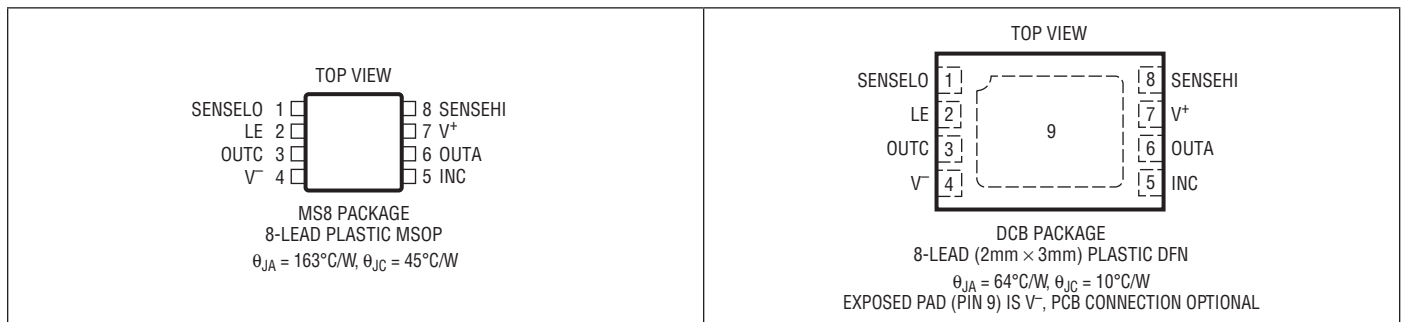


LT6118

ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage (V^+ to V^-)	60V	Amplifier Output Short-Circuit Duration (to V^-)..	Indefinite
Maximum Voltage (SENSELO, SENSEHI, OUTA).....	$V^+ + 1V$	Operating Temperature Range (Note 3)	
Maximum $V^+ - (SENSELO \text{ or } SENSEHI)$	33V	LT6118I.....	-40°C to 85°C
Maximum LE Voltage.....	60V	LT6118H.....	-40°C to 125°C
Maximum Comparator Input Voltage	60V	Specified Temperature Range (Note 3)	
Maximum Comparator Output Voltage.....	60V	LT6118I.....	-40°C to 85°C
Input Current (Note 2).....	-10mA	LT6118H.....	-40°C to 125°C
SENSEHI, SENSELO Input Current	$\pm 10\text{mA}$	Maximum Junction Temperature	150°C
Differential SENSEHI or SENSELO Input Current ..	$\pm 2.5\text{mA}$	Storage Temperature Range	-65°C to 150°C
		MSOP Lead Temperature (Soldering, 10 sec).....	300°C

PIN CONFIGURATION



ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
	LT6118IMS8#PBF	LTGNS	8-Lead Plastic MSOP	-40°C to 85°C
	LT6118HMS8#PBF	LTGNS	8-Lead Plastic MSOP	-40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container. Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandreeel/>

Lead Free Finish

TAPE AND REEL (MINI)	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
	LT6118IDCB#PBF	LGNT	8-Lead (2mm \times 3mm) Plastic DFN	-40°C to 85°C
	LT6118HDCB#PBF	LGNT	8-Lead (2mm \times 3mm) Plastic DFN	-40°C to 125°C

TRM = 500 pieces. *Temperature grades are identified by a label on the shipping container.

Consult LTC Marketing for parts specified with wider operating temperature ranges.

Consult LTC Marketing for information on lead based finish parts.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandreeel/>

ELECTRICAL CHARACTERISTICS The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $V^+ = 12\text{V}$, $V_{\text{PULLUP}} = V^+$, $V_{\text{LE}} = 2.7\text{V}$, $R_{\text{IN}} = 100\Omega$, $R_{\text{OUT}} = R_1 + R_2 = 10\text{k}$, gain = 100, $R_C = 25.5\text{k}$, $C_L = C_{\text{LC}} = 2\text{pF}$, unless otherwise noted. (See Figure 2)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V^+	Supply Voltage Range		● 2.7		60	V
I_S	Supply Current (Note 4)	$V^+ = 2.7\text{V}$, $R_{\text{IN}} = 1\text{k}$, $V_{\text{SENSE}} = 5\text{mV}$		450		μA
		$V^+ = 60\text{V}$, $R_{\text{IN}} = 1\text{k}$, $V_{\text{SENSE}} = 5\text{mV}$	●	550	650 950	μA μA
	LE Pin Current	$V_{\text{LE}} = 0\text{V}$, $V^+ = 60\text{V}$		-100		nA
V_{IH}	LE Pin Input High	$V^+ = 2.7\text{V}$ to 60V	● 1.5			V
V_{IL}	LE Pin Input Low	$V^+ = 2.7\text{V}$ to 60V	●		0.5	V

Current Sense Amplifier

V_{OS}	Input Offset Voltage	$V_{\text{SENSE}} = 5\text{mV}$	●	-200	200	μV
		$V_{\text{SENSE}} = 5\text{mV}$	●	-300	300	μV
$\Delta V_{\text{OS}}/\Delta T$	Input Offset Voltage Drift	$V_{\text{SENSE}} = 5\text{mV}$	●	± 0.8		$\mu\text{V}/^\circ\text{C}$
I_B	Input Bias Current (SENSELO, SENSEHI)	$V^+ = 2.7\text{V}$ to 60V	●	60	300	nA
			●		350	nA
I_{OS}	Input Offset Current	$V^+ = 2.7\text{V}$ to 60V		± 5		nA
I_{OUTA}	Output Current (Note 5)		●	1		mA
PSRR	Power Supply Rejection Ratio (Note 6)	$V^+ = 2.7\text{V}$ to 60V	●	120	127	dB
			●	114		dB
CMRR	Common Mode Rejection Ratio	$V^+ = 36\text{V}$, $V_{\text{SENSE}} = 5\text{mV}$, $V_{\text{ICM}} = 2.7\text{V}$ to 36V		125		dB
		$V^+ = 60\text{V}$, $V_{\text{SENSE}} = 5\text{mV}$, $V_{\text{ICM}} = 27\text{V}$ to 60V	●	110	125	dB
$V_{\text{SENSE(MAX)}}$	Full-Scale Input Sense Voltage (Note 5)	$R_{\text{IN}} = 500\Omega$	●	500		mV
	Gain Error (Note 7)	$V^+ = 2.7\text{V}$ to 12V	●		-0.08	%
		$V^+ = 12\text{V}$ to 60V, $V_{\text{SENSE}} = 5\text{mV}$ to 100mV, MS8 Package	●	-0.2	0	%
		$V^+ = 12\text{V}$ to 60V, $V_{\text{SENSE}} = 5\text{mV}$ to 100mV, DFN Package	●	-0.3	0	%
	SENSELO Voltage (Note 8)	$V^+ = 2.7\text{V}$, $V_{\text{SENSE}} = 100\text{mV}$, $R_{\text{OUT}} = 2\text{k}$	●	2.5		V
		$V^+ = 60\text{V}$, $V_{\text{SENSE}} = 100\text{mV}$	●	27		V
	Output Swing High (V^+ to V_{OUTA})	$V^+ = 2.7\text{V}$, $V_{\text{SENSE}} = 27\text{mV}$	●		0.2	V
		$V^+ = 12\text{V}$, $V_{\text{SENSE}} = 120\text{mV}$	●		0.5	V
BW	Signal Bandwidth	$I_{\text{OUT}} = 1\text{mA}$		1		MHz
		$I_{\text{OUT}} = 100\mu\text{A}$		140		kHz
t_r	Input Step Response (to 50% of Final Output Voltage)	$V^+ = 2.7\text{V}$, $V_{\text{SENSE}} = 24\text{mV}$ Step, Output Rising Edge		500		ns
		$V^+ = 12\text{V}$ to 60V, $V_{\text{SENSE}} = 100\text{mV}$ Step, Output Rising Edge		500		ns
t_{SETTLE}	Settling Time to 1%	$V_{\text{SENSE}} = 10\text{mV}$ to 100mV, $R_{\text{OUT}} = 2\text{k}$		2		μs

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $V^+ = 12\text{V}$, $V_{\text{PULLUP}} = V^+$, $V_{\text{LE}} = 2.7\text{V}$, $R_{\text{IN}} = 100\Omega$, $R_{\text{OUT}} = R_1 + R_2 = 10\text{k}$, gain = 100, $R_C = 25.5\text{k}$, $C_L = C_{\text{LC}} = 2\text{pF}$, unless otherwise noted. (See Figure 2)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Reference and Comparator						
$V_{\text{TH(R)}}$ (Note 9)	Rising Input Threshold Voltage	$V^+ = 2.7\text{V to } 60\text{V}$	● 395	400	405	mV
V_{HYS}	$V_{\text{HYS}} = V_{\text{TH(R)}} - V_{\text{TH(F)}}$	$V^+ = 2.7\text{V to } 60\text{V}$	3	10	15	mV
	Comparator Input Bias Current	$V_{\text{INC}} = 0\text{V}$, $V^+ = 60\text{V}$	● -50			nA
V_{OL}	Output Low Voltage	$I_{\text{OUTC}} = 500\mu\text{A}$, $V^+ = 2.7\text{V}$	●	60	150 220	mV mV
	High to Low Propagation Delay	5mV Overdrive 100mV Overdrive		3 0.5		μs μs
	Output Fall Time			0.08		μs
t_{RESET}	Reset Time			0.5		μs
t_{RPW}	Minimum LE Reset Pulse Width		● 2			μs

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Input and output pins have ESD diodes connected to ground. The SENSEHI and SENSELO pins have additional current handling capability specified as SENSEHI, SENSELO Input Current.

Note 3: The LT6118I is guaranteed to meet specified performance from -40°C to 85°C . LT6118H is guaranteed to meet specified performance from -40°C to 125°C .

Note 4: Supply current is specified with the comparator output high. When the comparator output goes low the supply current will increase by $75\mu\text{A}$ typically.

Note 5: The full-scale input sense voltage and the maximum output current must be considered to achieve the specified performance.

Note 6: Supply voltage and input common mode voltage are varied while amplifier input offset voltage is monitored.

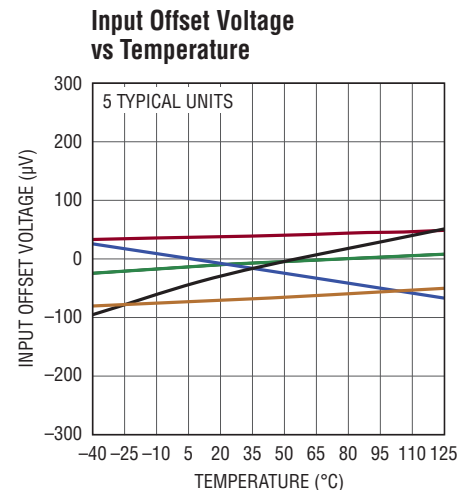
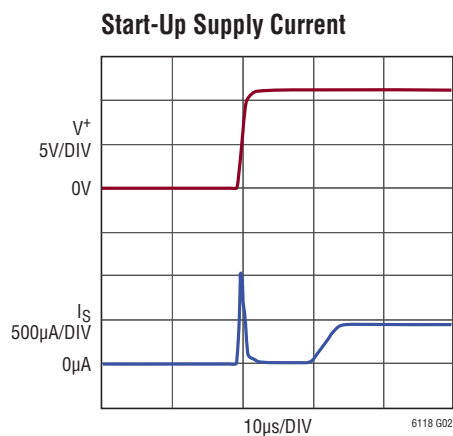
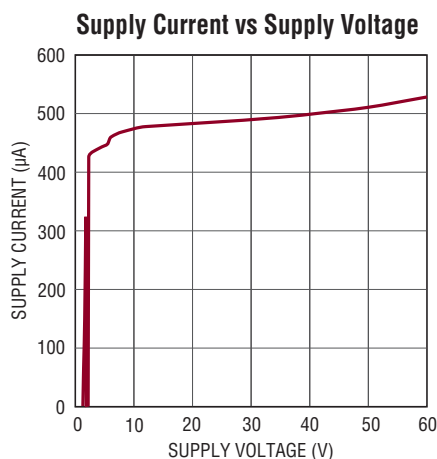
Note 7: The specified gain error does not include the effect of external resistors R_{IN} and R_{OUT} . Although gain error is only guaranteed between 12V and 60V, similar performance is expected for $V^+ < 12\text{V}$, as well.

Note 8: Refer to SENSELO, SENSEHI Range in the Applications Information section for more information.

Note 9: The input threshold voltage which causes the output voltage of the comparator to transition from high to low is specified. The input voltage which causes the comparator output to transition from low to high is the magnitude of the difference between the specified threshold and the hysteresis.

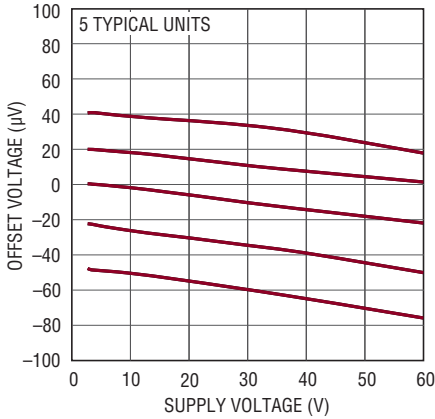
TYPICAL PERFORMANCE CHARACTERISTICS

Performance characteristics taken at $T_A = 25^\circ\text{C}$, $V^+ = 12\text{V}$, $V_{\text{PULLUP}} = V^+$, $V_{\text{LE}} = 2.7\text{V}$, $R_{\text{IN}} = 100\Omega$, $R_{\text{OUT}} = R_1 + R_2 = 10\text{k}$, gain = 100, $R_C = 25.5\text{k}$, $C_L = C_{\text{LC}} = 2\text{pF}$, unless otherwise noted. (See Figure 2)



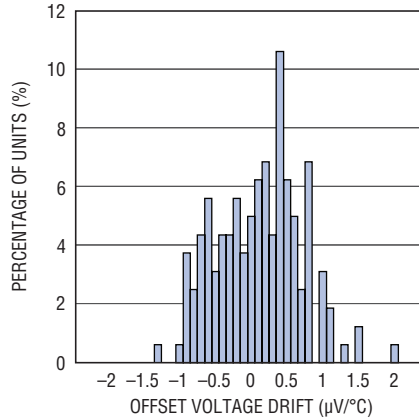
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Amplifier Offset Voltage vs Supply Voltage



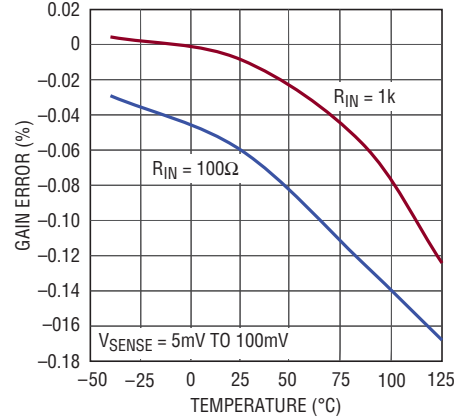
6118 G04

Offset Voltage Drift Distribution



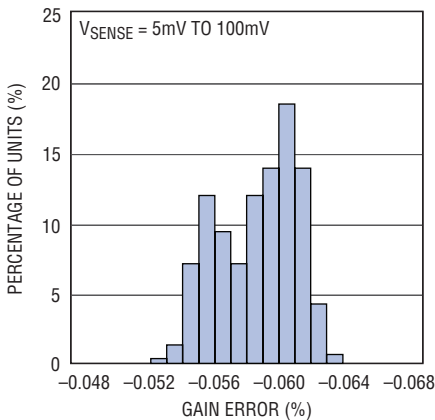
6118 G05

Amplifier Gain Error vs Temperature



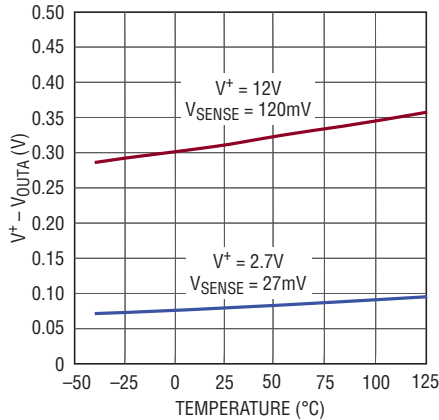
6118 G06

Amplifier Gain Error Distribution



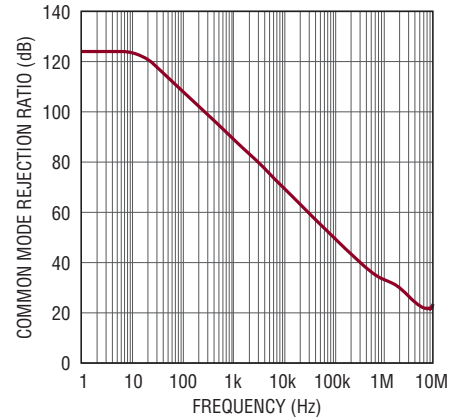
6118 G07

Amplifier Output Swing vs Temperature



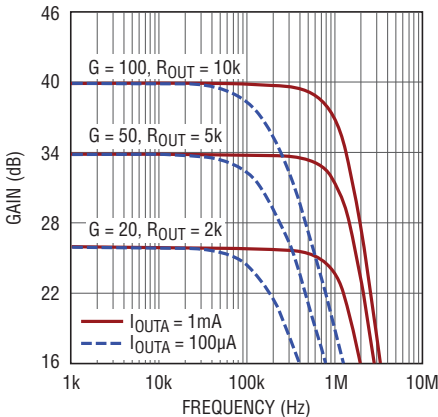
6118 G08

Common Mode Rejection Ratio vs Frequency



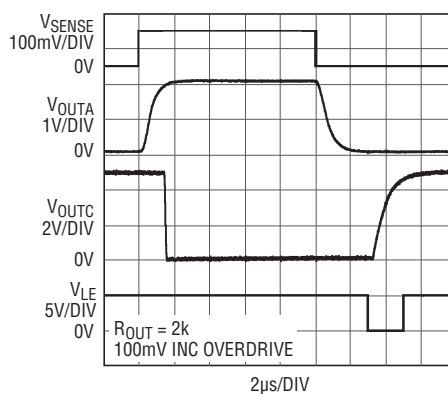
6118 G09

Amplifier Gain vs Frequency



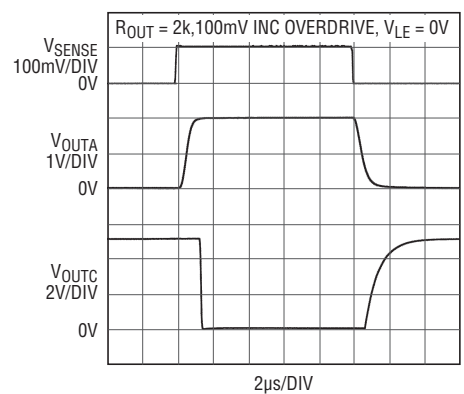
6118 G10

Step Response



6118 G11

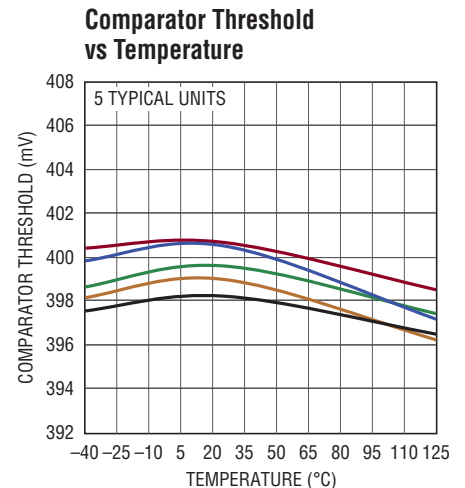
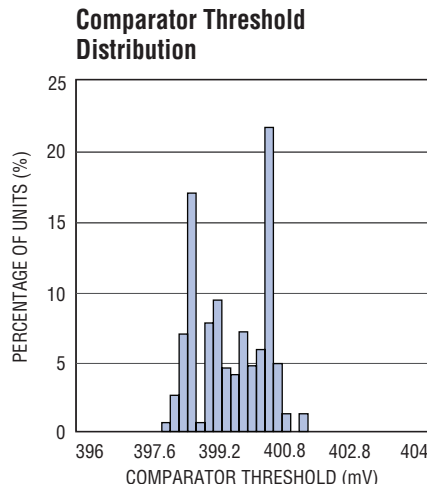
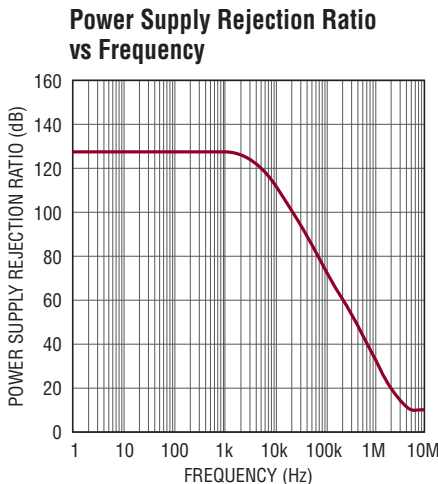
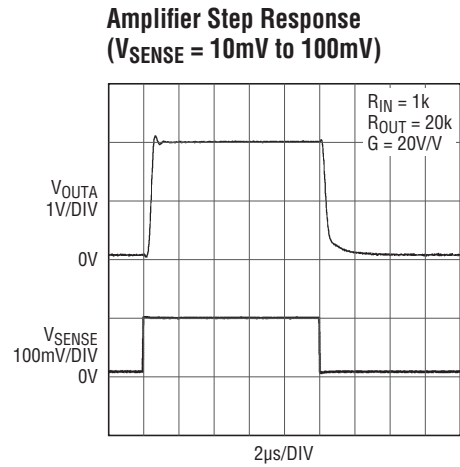
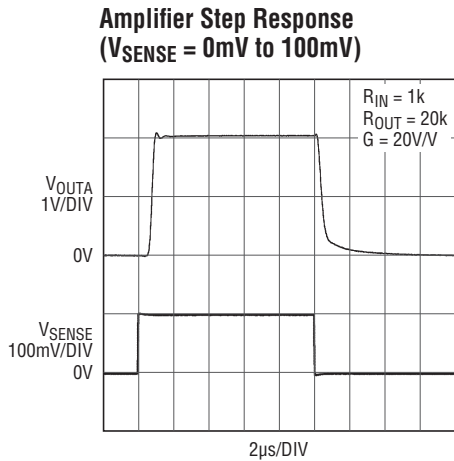
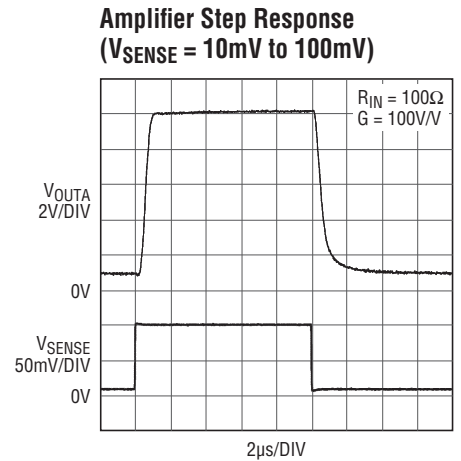
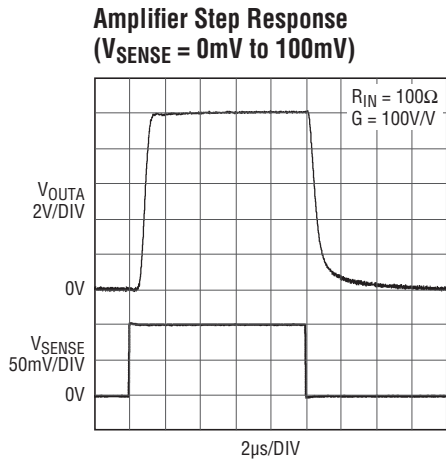
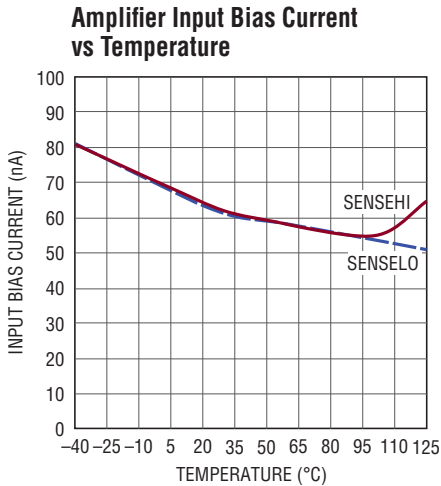
Step Response



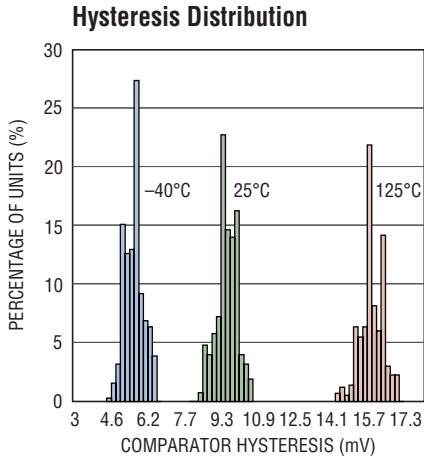
6118 G12

TYPICAL PERFORMANCE CHARACTERISTICS

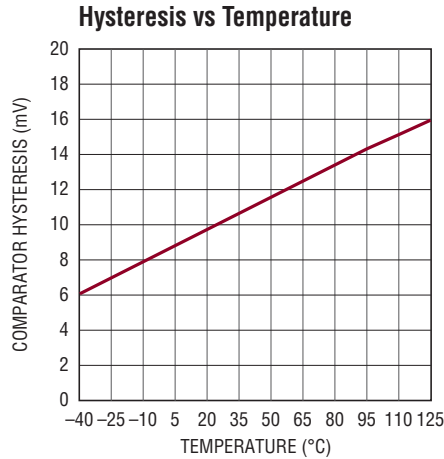
Performance characteristics taken at $T_A = 25^\circ\text{C}$, $V^+ = 12\text{V}$, $V_{\text{PULLUP}} = V^+$, $V_{\text{LE}} = 2.7\text{V}$, $R_{\text{IN}} = 100\Omega$, $R_{\text{OUT}} = R_1 + R_2 = 10\text{k}$, gain = 100, $R_C = 25.5\text{k}$, $C_L = C_{\text{LC}} = 2\text{pF}$, unless otherwise noted. (See Figure 2)



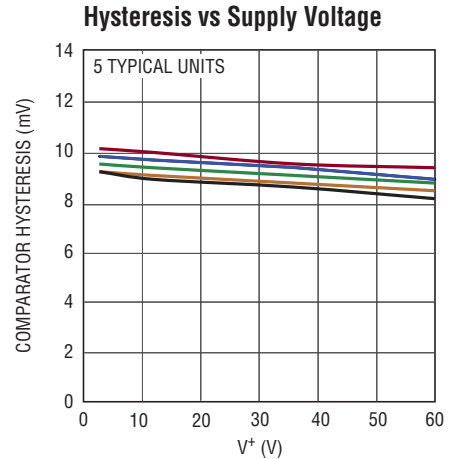
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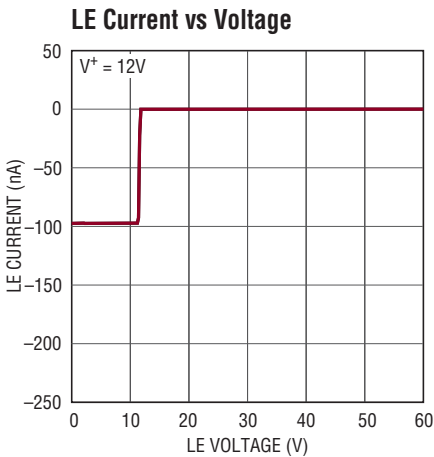
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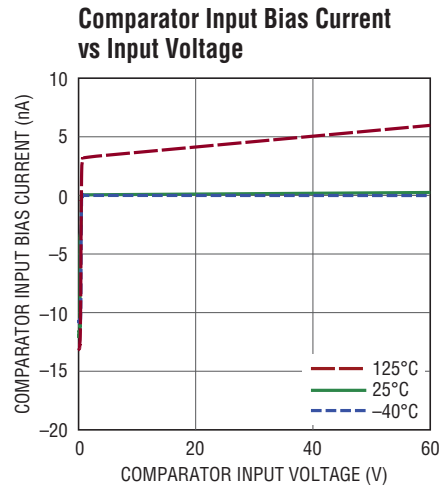
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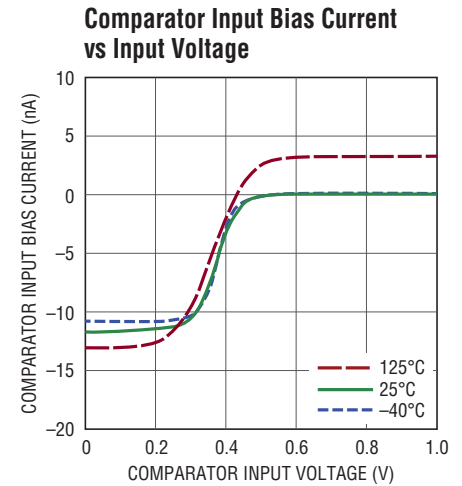
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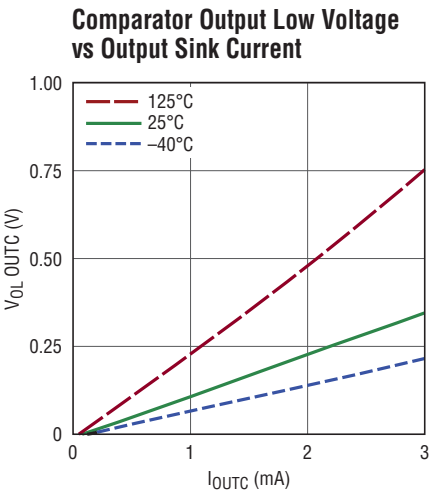
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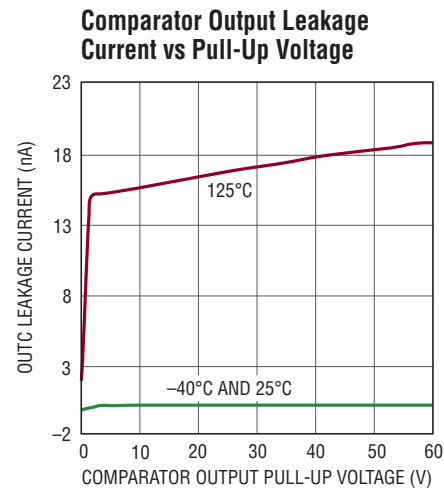
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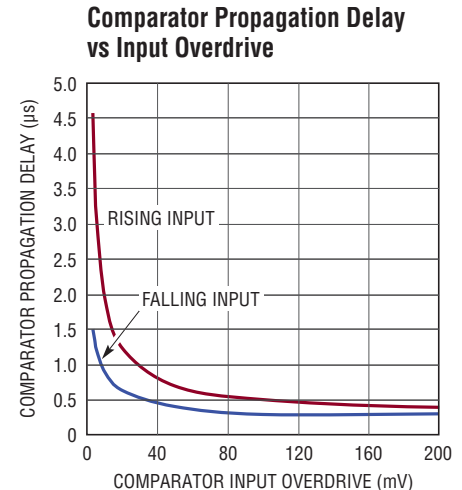
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6118 G27



6118 G28



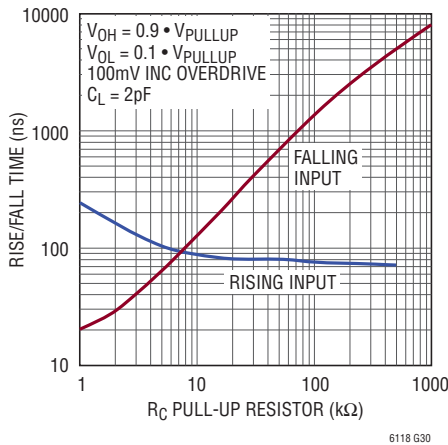
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6118f

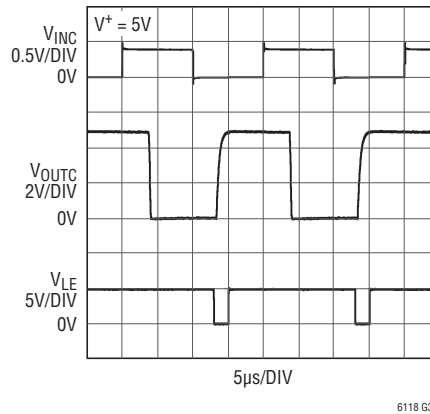
TYPICAL PERFORMANCE CHARACTERISTICS

Performance characteristics taken at $T_A = 25^\circ\text{C}$, $V^+ = 12\text{V}$, $V_{\text{PULLUP}} = V^+$, $V_{\text{LE}} = 2.7\text{V}$, $R_{\text{IN}} = 100\Omega$, $R_{\text{OUT}} = R_1 + R_2 = 10\text{k}$, gain = 100, $R_C = 25.5\text{k}$, $C_L = C_{\text{LC}} = 2\text{pF}$, unless otherwise noted. (See Figure 2)

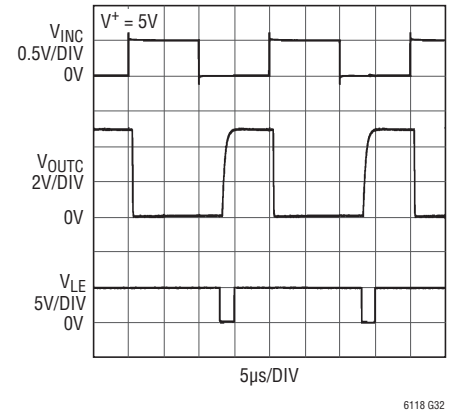
Comparator Rise/Fall Time vs Pull-Up Resistor



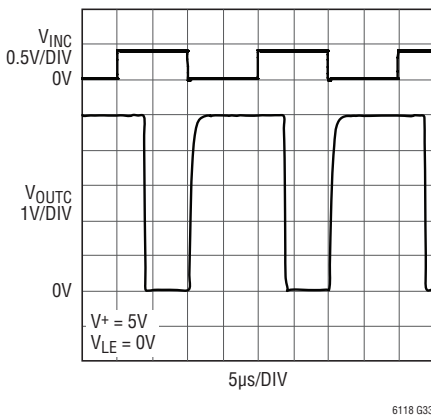
Comparator Step Response (5mV INC Overdrive)



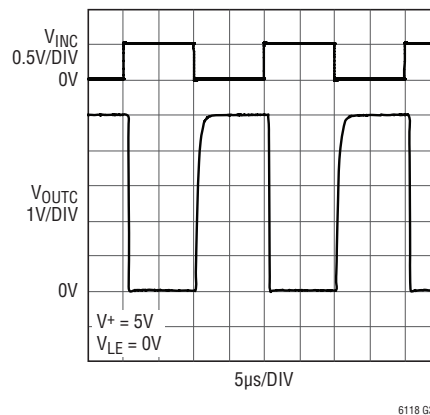
Comparator Step Response (100mV INC Overdrive)



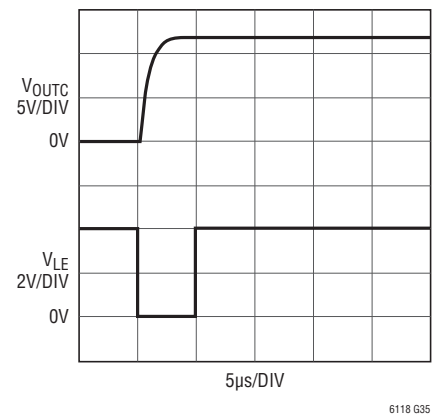
Comparator Step Response (5mV INC Overdrive)



Comparator Step Response (100mV INC Overdrive)



Comparator Reset Response



PIN FUNCTIONS

SENSELO (Pin 1): Sense Amplifier Input. This pin must be tied to the load end of the sense resistor.

LE (Pin 2): Latch Control Pin. When high, the comparator latch is enabled. With the comparator latch enabled, the comparator output will latch at a low level once tripped. When the LE input is low, the comparator latch is disabled and the comparator functions transparently.

OUTC (Pin 3): Open-Drain Comparator Output. Off-state voltage may be as high as 60V above V^- , regardless of V^+ used.

V^- (Pin 4): Negative Supply Pin. This pin is normally connected to ground.

INC (Pin 5): This is the inverting input of the comparator. The other comparator input is internally connected to the 400mV reference.

PIN FUNCTIONS

OUTA (Pin 6): Current Output of the Sense Amplifier. This pin will source a current that is equal to the sense voltage divided by the external gain setting resistor, R_{IN} .

V⁺ (Pin 7): Positive Supply Pin. The V⁺ pin can be connected directly to either side of the sense resistor, R_{SENSE} . When V⁺ is tied to the load end of the sense resistor, the SENSEHI pin can go up to 0.2V above V⁺. Supply current is drawn through this pin.

SENSEHI (Pin 8): Sense Amplifier Input. The internal sense amplifier will drive SENSEHI to the same potential as SENSELO. A resistor (typically R_{IN}) tied from supply to SENSEHI sets the output current, $I_{OUT} = V_{SENSE}/R_{IN}$, where V_{SENSE} is the voltage developed across R_{SENSE} .

Exposed Pad (Pin 9, DCB Package Only): V⁻. The exposed pad may be left open or connected to device V⁻. Connecting the exposed pad to a V⁻ plane will improve thermal management in high voltage applications. The exposed pad should not be used as the primary connection for V⁻.

BLOCK DIAGRAM

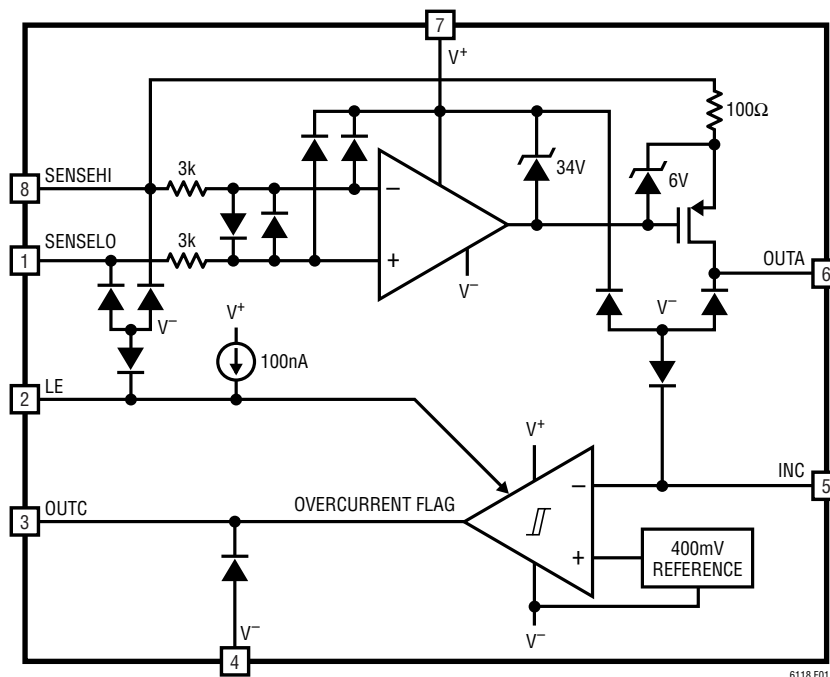


Figure 1. Block Diagram

APPLICATIONS INFORMATION

The LT6118 high side current sense amplifier provides accurate monitoring of currents through an external sense resistor. The input sense voltage is level-shifted from the sensed power supply to a ground referenced output and is amplified by a user-selected gain to the output. The output voltage is directly proportional to the current flowing through the sense resistor.

The LT6118 comparator has a threshold set with a built-in 400mV precision reference and has 10mV of hysteresis. The open-drain output can be easily used to level shift to digital supplies.

Amplifier Theory of Operation

An internal sense amplifier loop forces SENSEHI to have the same potential as SENSELO as shown in Figure 2.

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Connecting an external resistor, R_{IN} , between SENSEHI and V_{SUPPLY} forces a potential, V_{SENSE} , across R_{IN} . A corresponding current, I_{OUTA} , equal to V_{SENSE}/R_{IN} , will flow through R_{IN} . The high impedance inputs of the sense amplifier do not load this current, so it will flow through an internal MOSFET to the output pin, OUTA.

The output current can be transformed back into a voltage by adding a resistor from OUTA to V^- (typically ground). The output voltage is then:

$$V_{OUT} = V^- + I_{OUTA} \cdot R_{OUT}$$

where $R_{OUT} = R1 + R2$ as shown in Figure 2.

Table 1. Example Gain Configurations

GAIN	R_{IN}	R_{OUT}	V_{SENSE} FOR $V_{OUT} = 5V$	I_{OUTA} AT $V_{OUT} = 5V$
20	499 Ω	10k	250mV	500 μA
50	200 Ω	10k	100mV	500 μA
100	100 Ω	10k	50mV	500 μA

Useful Equations

Input Voltage: $V_{SENSE} = I_{SENSE} \cdot R_{SENSE}$

Voltage Gain: $\frac{V_{OUT}}{V_{SENSE}} = \frac{R_{OUT}}{R_{IN}}$

Current Gain: $\frac{I_{OUTA}}{I_{SENSE}} = \frac{R_{SENSE}}{R_{IN}}$

Note that $V_{SENSE(MAX)}$ can be exceeded without damaging the amplifier, however, output accuracy will degrade as V_{SENSE} exceeds $V_{SENSE(MAX)}$, resulting in increased output current, I_{OUTA} .

Selection of External Current Sense Resistor

The external sense resistor, R_{SENSE} , has a significant effect on the function of a current sensing system and must be chosen with care.

First, the power dissipation in the resistor should be considered. The measured load current will cause power dissipation as well as a voltage drop in R_{SENSE} . As a result, the sense resistor should be as small as possible while still providing the input dynamic range required by the measurement. Note that the input dynamic range is the difference between the maximum input signal and the minimum accurately reproduced signal, and is limited primarily by input DC offset of the internal sense amplifier of the LT6118. To ensure the specified performance, R_{SENSE} should be small enough that V_{SENSE} does not exceed $V_{SENSE(MAX)}$ under peak load conditions. As an example, an application may require the maximum sense voltage be 100mV. If this application is expected to draw 2A at peak load, R_{SENSE} should be set to 50m Ω .

Once the maximum R_{SENSE} value is determined, the minimum sense resistor value will be set by the resolution or dynamic range required. The minimum signal that can be

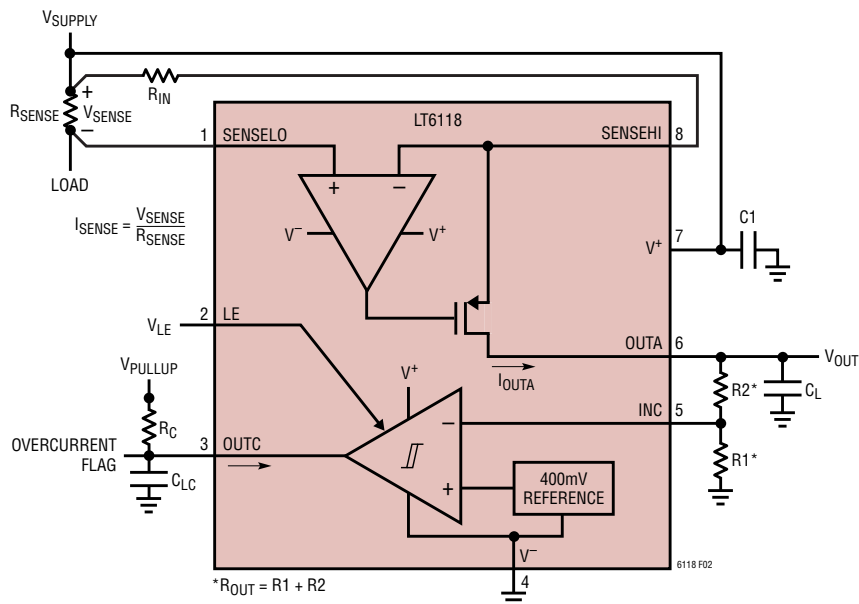


Figure 2. Typical Connection

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accurately represented by this sense amplifier is limited by the input offset. As an example, the LT6118 has a maximum input offset of 200 μ V. If the minimum current is 20mA, a sense resistor of 10m Ω will set V_{SENSE} to 200 μ V. This is the same value as the input offset. A larger sense resistor will reduce the error due to offset by increasing the sense voltage for a given load current. Choosing a 50m Ω R_{SENSE} will maximize the dynamic range and provide a system that has 100mV across the sense resistor at peak load (2A), while input offset causes an error equivalent to only 4mA of load current.

In the previous example, the peak dissipation in R_{SENSE} is 200mW. If a 5m Ω sense resistor is employed, then the effective current error is 40mA, while the peak sense voltage is reduced to 10mV at 2A, dissipating only 20mW.

The low offset and corresponding large dynamic range of the LT6118 make it more flexible than other solutions in this respect. The 200 μ V maximum offset gives 68dB of dynamic range for a sense voltage that is limited to 500mV max.

Sense Resistor Connection

Kelvin connection of the SENSEHI and SENSELO inputs to the sense resistor should be used in all but the lowest power applications. Solder connections and PC board interconnections that carry high currents can cause significant error in measurement due to their relatively large resistances. One 10mm \times 10mm square trace of 1oz copper is approximately 0.5m Ω . A 1mV error can be caused by as little as 2A flowing through this small interconnect. This will cause a 1% error for a full-scale V_{SENSE} of 100mV. A 10A load current in the same interconnect will cause a 5% error for the same 100mV signal. By isolating the sense traces from the high current paths, this error can be reduced by orders of magnitude. A sense resistor with integrated Kelvin sense terminals will give the best results. Figure 2 illustrates the recommended method for connecting the SENSEHI and SENSELO pins to the sense resistor.

Selection of External Input Gain Resistor, R_{IN}

R_{IN} should be chosen to allow the required speed and resolution while limiting the output current to 1mA. The maximum value for R_{IN} is 1k to maintain good loop stability. For a given V_{SENSE} , larger values of R_{IN} will lower power

dissipation in the LT6118 due to the reduction in I_{OUT} while smaller values of R_{IN} will result in faster response time due to the increase in I_{OUT} . If low sense currents must be resolved accurately in a system that has a very wide dynamic range, a smaller R_{IN} may be used if the maximum I_{OUTA} current is limited in another way, such as with a Schottky diode across R_{SENSE} (Figure 3). This will reduce the high current measurement accuracy by limiting the result, while increasing the low current measurement resolution.

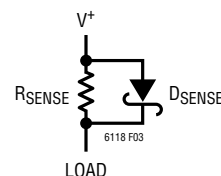


Figure 3. Shunt Diode Limits Maximum Input Voltage to Allow Better Low Input Resolution Without Overranging

This approach can be helpful in cases where occasional bursts of high currents can be ignored.

Care should be taken when designing the board layout for R_{IN} , especially for small R_{IN} values. All trace and interconnect resistances will increase the effective R_{IN} value, causing a gain error.

The power dissipated in the sense resistor can create a thermal gradient across a printed circuit board and consequently a gain error if R_{IN} and R_{OUT} are placed such that they operate at different temperatures. If significant power is being dissipated in the sense resistor then care should be taken to place R_{IN} and R_{OUT} such that the gain error due to the thermal gradient is minimized.

Selection of External Output Gain Resistor, R_{OUT}

The output resistor, R_{OUT} , determines how the output current is converted to voltage. V_{OUT} is simply $I_{OUTA} \cdot R_{OUT}$. Typically, R_{OUT} is a combination of resistors configured as a resistor divider which has a voltage tap going to the comparator input to set the comparator threshold.

In choosing an output resistor, the maximum output voltage must first be considered. If the subsequent circuit is a buffer or ADC with limited input range, then R_{OUT} must be chosen so that $I_{OUTA(MAX)} \cdot R_{OUT}$ is less than the allowed maximum input range of this circuit.

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In addition, the output impedance is determined by R_{OUT} . If another circuit is being driven, then the input impedance of that circuit must be considered. If the subsequent circuit has high enough input impedance, then almost any useful output impedance will be acceptable. However, if the subsequent circuit has relatively low input impedance, or draws spikes of current such as an ADC load, then a lower output impedance may be required to preserve the accuracy of the output. More information can be found in the Output Filtering section. As an example, if the input impedance of the driven circuit, $R_{IN(DRIVEN)}$, is 100 times R_{OUT} , then the accuracy of V_{OUT} will be reduced by 1% since:

$$\begin{aligned} V_{OUT} &= I_{OUTA} \cdot \frac{R_{OUT} \cdot R_{IN(DRIVEN)}}{R_{OUT} + R_{IN(DRIVEN)}} \\ &= I_{OUTA} \cdot R_{OUT} \cdot \frac{100}{101} = 0.99 \cdot I_{OUTA} \cdot R_{OUT} \end{aligned}$$

Amplifier Error Sources

The current sense system uses an amplifier and resistors to apply gain and level-shift the result. Consequently, the output is dependent on the characteristics of the amplifier, such as gain error and input offset, as well as the matching of the external resistors.

Ideally, the circuit output is:

$$V_{OUT} = V_{SENSE} \cdot \frac{R_{OUT}}{R_{IN}}; \quad V_{SENSE} = R_{SENSE} \cdot I_{SENSE}$$

In this case, the only error is due to external resistor mismatch, which provides an error in gain only. However, offset voltage, input bias current and finite gain in the amplifier can cause additional errors:

Output Voltage Error, $\Delta V_{OUT(VOS)}$, Due to the Amplifier DC Offset Voltage, V_{OS}

$$\Delta V_{OUT(VOS)} = V_{OS} \cdot \frac{R_{OUT}}{R_{IN}}$$

The DC offset voltage of the amplifier adds directly to the value of the sense voltage, V_{SENSE} . As V_{SENSE} is increased, accuracy improves. This is the dominant error of the system and it limits the available dynamic range.

Output Voltage Error, $\Delta V_{OUT(IBIAS)}$, Due to the Bias Currents I_B^+ and I_B^-

The amplifier bias current I_B^+ flows into the SENSELO pin while I_B^- flows into the SENSEHI pin. The error due to I_B is the following:

$$\Delta V_{OUT(IBIAS)} = R_{OUT} \left(I_B^+ \cdot \frac{R_{SENSE}}{R_{IN}} - I_B^- \right)$$

Since $I_B^+ \approx I_B^- = I_{BIAS}$, if $R_{SENSE} \ll R_{IN}$ then,

$$\Delta V_{OUT(IBIAS)} = -R_{OUT} (I_{BIAS})$$

It is useful to refer the error to the input:

$$\Delta V_{VIN(IBIAS)} = -R_{IN} (I_{BIAS})$$

For instance, if I_{BIAS} is 100nA and R_{IN} is 1k, the input referred error is 100 μ V. This error becomes less significant as the value of R_{IN} decreases. The bias current error can be reduced if an external resistor, R_{IN}^+ , is connected as shown in Figure 4, the error is then reduced to:

$$V_{OUT(IBIAS)} = \pm R_{OUT} \cdot I_{OS}; \quad I_{OS} = I_B^+ - I_B^-$$

Minimizing low current errors will maximize the dynamic range of the circuit.

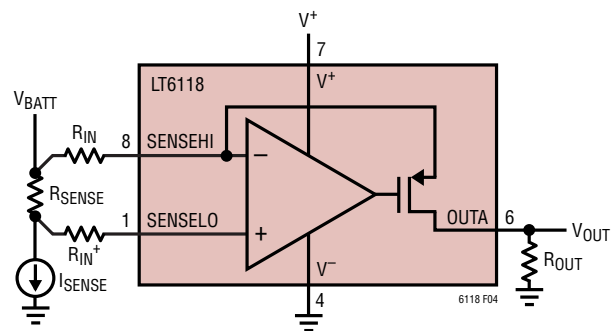


Figure 4. R_{IN}^+ Reduces Error Due to I_B

Output Voltage Error, $\Delta V_{OUT(GAIN ERROR)}$, Due to External Resistors

The LT6118 exhibits a very low gain error. As a result, the gain error is only significant when low tolerance resistors are used to set the gain. Note the gain error is systematically negative. For instance, if 0.1% resistors are used for R_{IN} and R_{OUT} then the resulting worst-case gain error is -0.4% with $R_{IN} = 100\Omega$. Figure 5 is a graph

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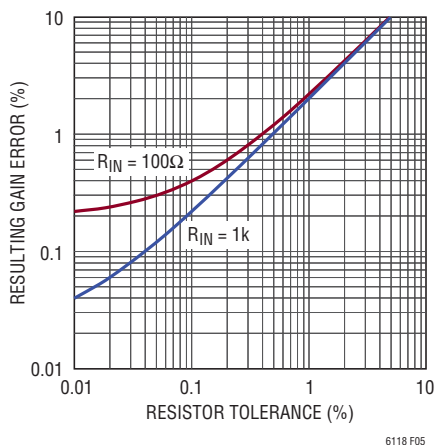


Figure 5. Gain Error vs Resistor Tolerance

of the maximum gain error which can be expected versus the external resistor tolerance.

Output Current Limitations Due to Power Dissipation

The LT6118 can deliver a continuous current of 1mA to the OUTA pin. This current flows through R_{IN} and enters the current sense amplifier via the SENSEHI pin. The power dissipated in the LT6118 due to the output signal is:

$$P_{OUT} = (V_{SENSEHI} - V_{OUTA}) \cdot I_{OUTA}$$

Since $V_{SENSEHI} \approx V^+$, $P_{OUTA} \approx (V^+ - V_{OUTA}) \cdot I_{OUTA}$

There is also power dissipated due to the quiescent power supply current:

$$P_S = I_S \cdot V^+$$

The comparator output current flows into the comparator output pin and out of the V^- pin. The power dissipated in the LT6118 due to the comparator is often insignificant and can be calculated as follows:

$$P_{OUTC} = (V_{OUTC} - V^-) \cdot I_{OUTC}$$

The total power dissipated is the sum of these dissipations:

$$P_{TOTAL} = P_{OUTA} + P_{OUTC} + P_S$$

At maximum supply and maximum output currents, the total power dissipation can exceed 150mW. This will cause significant heating of the LT6118 die. In order to prevent damage to the LT6118, the maximum expected dissipation in each application should be calculated. This number

can be multiplied by the θ_{JA} value, 163°C/W for the MS8 package or 64°C/W for the DFN, to find the maximum expected die temperature. Proper heat sinking and thermal relief should be used to ensure that the die temperature does not exceed the maximum rating.

LE Pin

The LE pin is used to enable the comparator output latch. When the LE pin is high, the output latch is enabled and the comparator output will stay low once it is tripped. When LE is low, the comparator output latch is disabled and the comparator operates transparently. To continuously operate the comparator transparently, the LE pin should be grounded. Do not leave the LE pin floating.

Power-On Reset

During startup the state of the comparator output cannot be guaranteed. To guarantee the correct state of the comparator output on startup, a power-on reset (POR) is required. A POR can be implemented by holding the LE pin low until the LT6118 is in such a state that the comparator output is stable. This can be achieved by using an RC network between the LE, V^+ and GND as shown in Figure 6. When power is applied to the LT6118, the RC network causes the voltage on the LE pin to remain below the V_{IL} (0.5V) threshold long enough for the comparator output to settle into the correct state. The LE pin should remain below 0.5V for at least 100µs after power up in order to guarantee a valid comparator output. The RC value can be determined with the following equation:

$$RC = \frac{t}{\ln\left(\frac{V^+}{V^+ - 0.5V}\right)}; t \geq 100\mu s$$

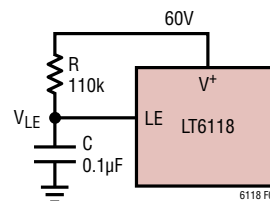


Figure 6. RC Network Achieves Power-On Reset

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The RC will need to be chosen based on the supply voltage of the circuit. Figure 7 can be used to easily determine an appropriate RC combination for an applications supply voltage range.

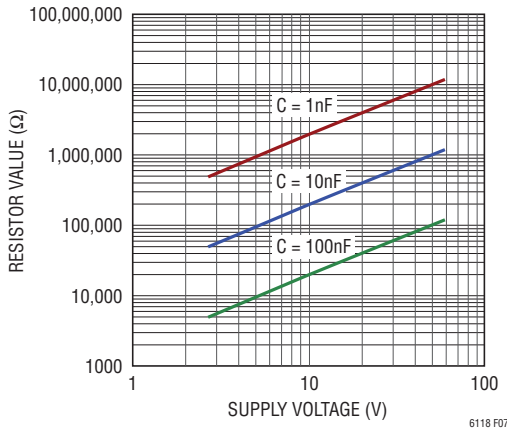


Figure 7. Minimum Resistance for Three Typical Capacitor Values

Output Filtering

The AC output voltage, V_{OUT} , is simply $I_{OUTA} \cdot Z_{OUT}$. This makes filtering straightforward. Any circuit may be used which generates the required Z_{OUT} to get the desired filter response. For example, a capacitor in parallel with R_{OUT} will give a lowpass response. This will reduce noise at the output, and may also be useful as a charge reservoir to keep the output steady while driving a switching circuit such as a MUX or ADC. This output capacitor in parallel with R_{OUT} will create an output pole at:

$$f_{-3dB} = \frac{1}{2 \cdot \pi \cdot R_{OUT} \cdot C_L}$$

SENSELO, SENSEHI Range

The difference between V_{BATT} (see Figure 8) and V^+ , as well as the maximum value of V_{SENSE} , must be considered to ensure that the SENSELO pin doesn't exceed the range listed in the Electrical Characteristics table. The SENSELO and SENSEHI pins of the LT6118 can function from 0.2V above the positive supply to 33V below it. These operating voltages are limited by internal diode clamps shown in Figures 1 and 2. On supplies less than 35.5V, the lower range is limited by $V^- + 2.5V$. This allows the monitored supply, V_{BATT} , to be separate from the LT6118 positive

supply as shown in Figure 8. Figure 9 shows the range of operating voltages for the SENSELO and SENSEHI inputs, for different supply voltage inputs (V^+). The SENSELO and SENSEHI range has been designed to allow the LT6118 to monitor its own supply current (in addition to the load), as long as V_{SENSE} is less than 200mV. This is shown in Figure 10.

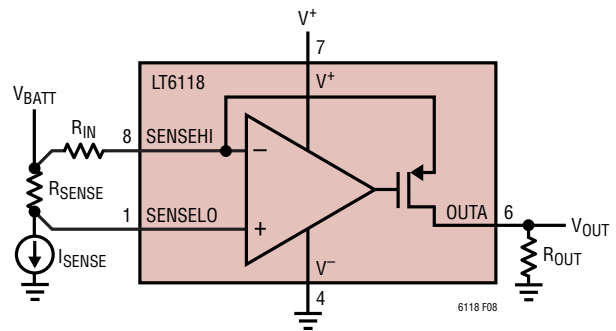


Figure 8. V^+ Powered Separately from Load Supply (V_{BATT})

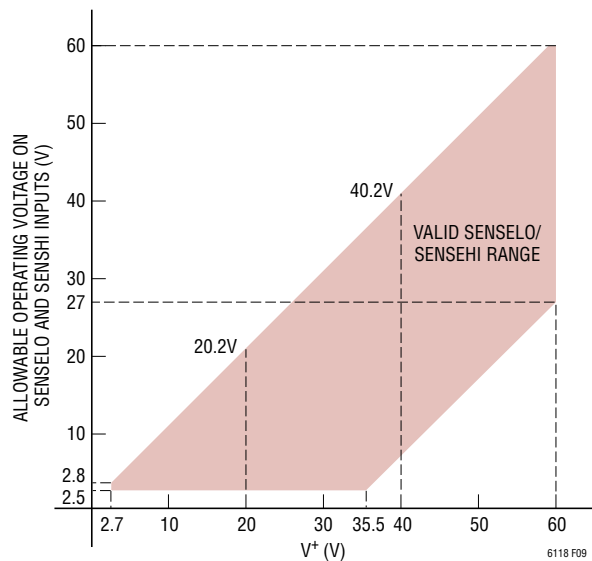


Figure 9. Allowable SENSELO, SENSEHI Voltage Range

Minimum Output Voltage

The output of the LT6118 current sense amplifier can produce a non-zero output voltage when the sense voltage is zero. This is a result of the sense amplifier V_{OS} being forced across R_{IN} as discussed in the Output Voltage Error, $\Delta V_{OUT}(V_{OS})$ section. Figure 11 shows the effect of the input offset voltage on the transfer function for parts at

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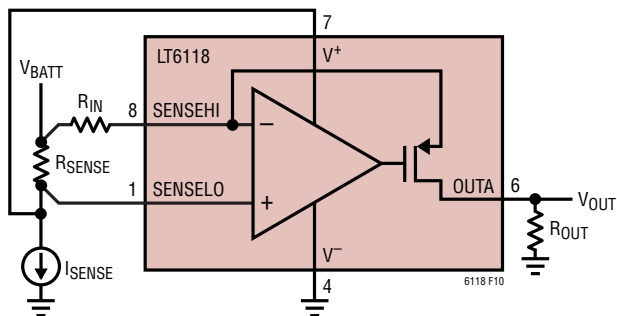


Figure 10. Supply Current Monitored with Load

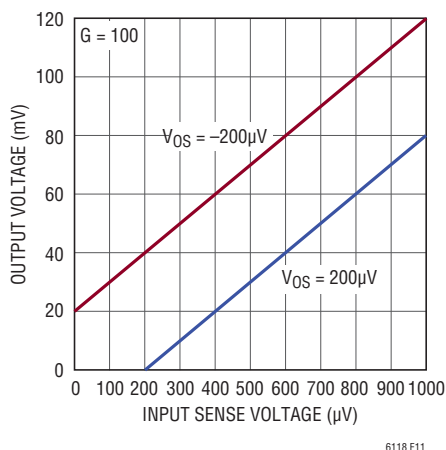


Figure 11. Amplifier Output Voltage vs Input Sense Voltage

the V_{OS} limits. With a negative offset voltage, zero input sense voltage produces an output voltage. With a positive offset voltage, the output voltage is zero until the input sense voltage exceeds the input offset voltage. Neglecting V_{OS} , the output circuit is not limited by saturation of pull-down circuitry and can reach 0V.

Response Time

The LT6118 amplifier is designed to exhibit fast response to inputs for the purpose of circuit protection or current monitoring. This response time will be affected by the external components in two ways, delay and speed.

If the output current is very low and an input transient occurs, there may be an increased delay before the output voltage begins to change. The Typical Performance Characteristics show that this delay is short and it can be improved by increasing the minimum output current, either by increasing R_{SENSE} or decreasing R_{IN} . Note that

the Typical Performance Characteristics are labeled with respect to the initial sense voltage.

The speed is also affected by the external components. Using a larger R_{OUT} will decrease the response time, since $V_{OUT} = I_{OUTA} \cdot Z_{OUT}$ where Z_{OUT} is the parallel combination of R_{OUT} and any parasitic and/or load capacitance. Note that reducing R_{IN} or increasing R_{OUT} will both have the effect of increasing the voltage gain of the circuit. If the output capacitance is limiting the speed of the system, R_{IN} and R_{OUT} can be decreased together in order to maintain the desired gain and provide more current to charge the output capacitance.

The response time of the comparator is the sum of the propagation delay and the fall time. The propagation delay is a function of the overdrive voltage on the input of the comparator. A larger overdrive will result in a lower propagation delay. This helps achieve a fast system response time to fault events. The fall time is affected by the load on the output of the comparator as well as the pull-up voltage.

The LT6118 amplifier has a typical response time of 500ns and the comparators have a typical response time of 500ns. When configured as a system, the amplifier output drives the comparator input causing a total system response time which is typically greater than that implied by the individually specified response times. This is due to the overdrive on the comparator input being determined by the speed of the amplifier output.

Internal Reference and Comparator

The integrated precision reference and comparator combined with the high precision current sense allow for rapid and easy detection of abnormal load currents. This is often critical in systems that require high levels of safety and reliability. The LT6118 comparator is optimized for fault detection and is designed with a latching output. The latching output prevents faults from clearing themselves and requires a separate system or user to reset the output. In applications where the comparator output can intervene and disconnect loads from the supply, a latched output is required to avoid oscillation. The latching output is also useful for detecting problems that are intermittent. In applications where a latching output is not desired the LE pin can be tied low to disable the latch.

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The comparator has one input available externally. The other comparator input is connected internally to the 400mV precision reference. The input threshold (the voltage which causes the output to transition from high to low) is designed to be equal to that of the reference. The reference voltage is established with respect to the device V^- connection.

Comparator Input

The comparator input can swing from V^- to 60V regardless of the supply voltage used. The input current for inputs well above the threshold is just a few pAs. With decreasing input voltage, a small bias current begins to be drawn out of the input near the threshold, reaching 50nA max when at ground potential. Note that this change in input bias current can cause a small nonlinearity in the OUTA transfer function if the comparator input is coupled to the amplifier output with a voltage divider. For example, if the maximum comparator input current is 50nA, and the resistance seen looking out of the comparator input is 1k, then a change in output voltage of 50 μ V will be seen on the analog output when the comparator input voltage passes through its threshold.

Setting Comparator Threshold

The comparator has an internal 400mV precision reference. In order to set the trip point of the LT6118 comparator as configured in Figure 12, the input sense voltage at which the comparator will trip, $V_{SENSE(TRIP)}$ must be calculated:

$$V_{SENSE(TRIP)} = I_{SENSE(TRIP)} \cdot R_{SENSE}$$

The selection of R_{IN} is discussed in the Selection of External Input Gain Resistor R_{IN} section. Once R_{IN} is selected, R_{OUT} can be calculated:

$$R_{OUT} = R_{IN} \frac{400mV}{V_{SENSE(TRIP)}}$$

Since the amplifier output is connected directly to the comparator input, the gain from V_{SENSE} to V_{OUT} is:

$$A_V = \frac{400mV}{V_{SENSE(TRIP)}}$$

As shown in Figure 13, R2 can be used to increase the gain from V_{SENSE} to V_{OUT} without changing $V_{SENSE(TRIP)}$. As before, R1 can be easily calculated:

$$R1 = R_{IN} \frac{400mV}{V_{SENSE(TRIP)}}$$

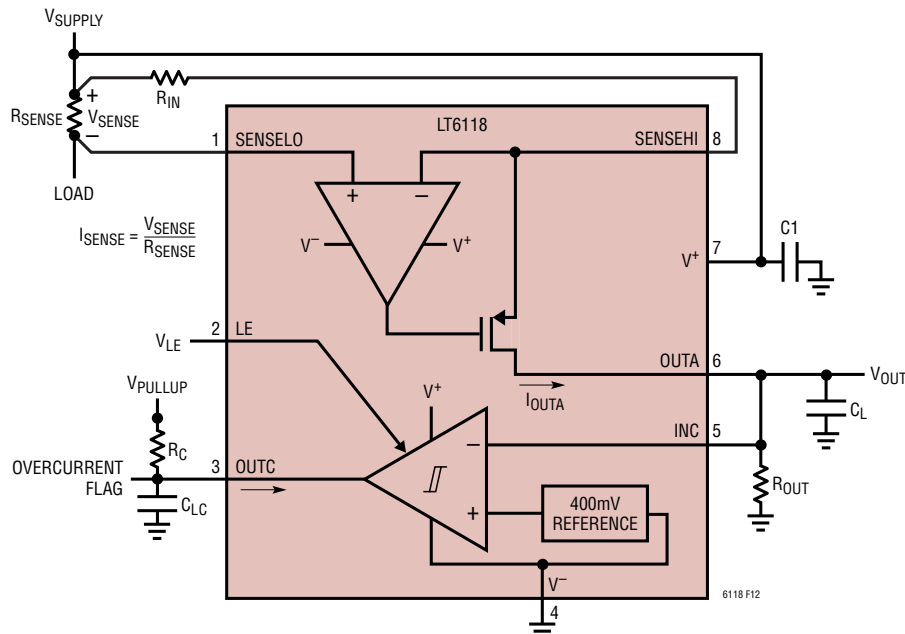


Figure 12. Basic Comparator Configuration

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The gain is now:

$$A_V = \frac{R1+R2}{R_{IN}}$$

This gain equation can be easily solved for R2:

$$R2 = A_V \cdot R_{IN} - R1$$

If the configuration of Figure 10 gives too much gain, R2 can be used to reduce the gain without changing $V_{SENSE(TRIP)}$ as shown in Figure 14. A_V can be easily calculated:

$$A_V = \frac{R1}{R_{IN}}$$

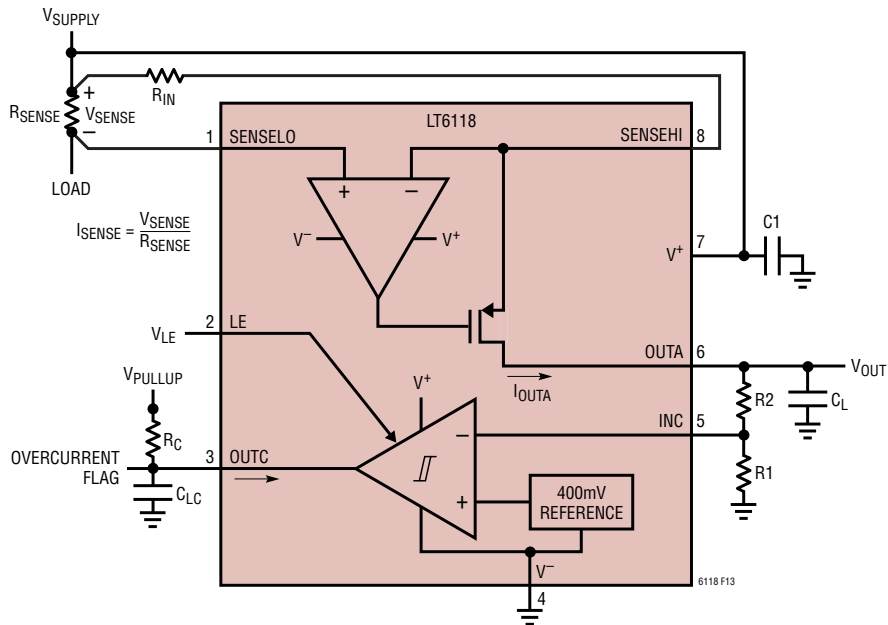


Figure 13: Comparator Configuration with Increased A_V

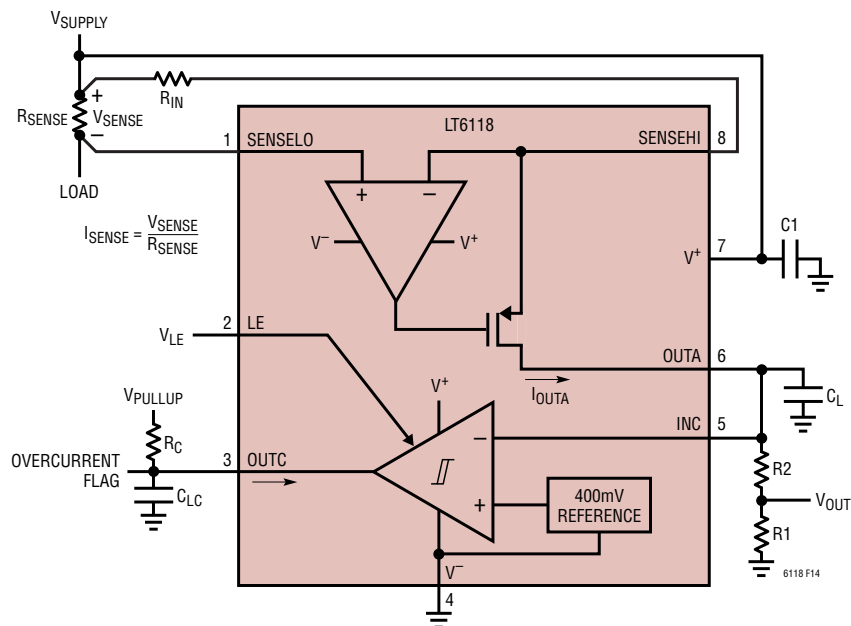


Figure 14: Comparator Configuration with Reduced A_V

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This gain equation can be easily solved for R1:

$$R1 = A_V \cdot R_{IN}$$

The value of R2 can be calculated:

$$R2 = \frac{400\text{mV} \cdot R_{IN} - V_{\text{SENSE(TRIP)}} \cdot R1}{V_{\text{SENSE(TRIP)}}$$

Hysteresis

The comparator has a typical built-in hysteresis of 10mV to simplify design, ensure stable operation in the presence of noise at the input, and to reject supply noise that might be induced by state change load transients. The hysteresis is designed such that the threshold voltage is altered when the output is transitioning from low to high as is shown in Figure 15.

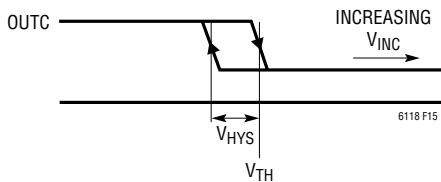


Figure 15. Comparator Output Transfer Characteristics

External positive feedback circuitry can be employed to increase the effective hysteresis if desired, but such circuitry will have an effect on both the rising and falling input thresholds, V_{TH} (the actual internal threshold remains unaffected).

Figure 16 shows how to add additional hysteresis to the comparator.

R5 can be calculated from the amplifier output current which is required to cause the comparator output to trip, I_{OVER} .

$$R5 = \frac{400\text{mV}}{I_{OVER}}, \text{ Assuming } (R1+R2) \gg R5$$

To ensure $(R1 + R2) \gg R5$, R1 should be chosen such that $R1 \gg R5$ so that V_{OUTA} does not change significantly when the comparator trips.

R3 should be chosen to allow sufficient V_{OL} and comparator output rise time due to capacitive loading.

R2 can be calculated:

$$R2 = R1 \cdot \left(\frac{V_{DD} - 390\text{mV}}{V_{\text{HYS(EXTRA)}}} \right)$$

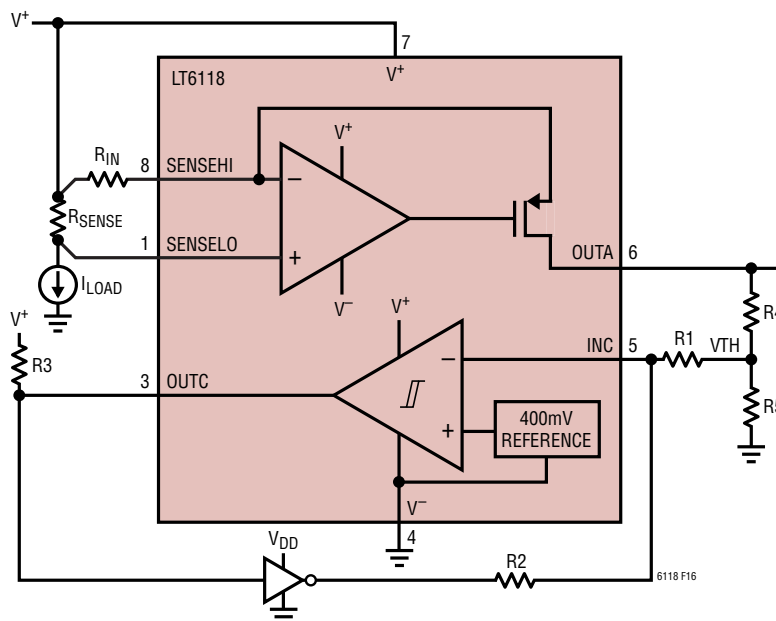


Figure 16. Inverting Comparator with Added Hysteresis

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Note that the hysteresis being added, $V_{\text{HYS(EXTRA)}}$, is in addition to the typical 10mV of built-in hysteresis. For very large values of R2 PCB related leakage may become an issue. A tee network can be implemented to reduce the required resistor values.

The approximate total hysteresis is:

$$V_{\text{HYS}} = 10\text{mV} + R1 \cdot \left(\frac{V_{\text{DD}} - 390\text{mV}}{R2} \right)$$

For example, to achieve $I_{\text{OVER}} = 900\mu\text{A}$ with 50mV of total hysteresis, $R5 = 442\Omega$. Choosing $R1 = 4.42\text{k}$, $R3 = 10\text{k}$ and $V_{\text{DD}} = 5\text{V}$ results in $R2 = 513\text{k}$.

The analog output voltage will also be affected when the comparator trips due to the current injected into R5 by the positive feedback. Because of this, it is desirable to have $(R1 + R2) \gg R5$. The maximum V_{OUTA} error caused by this can be calculated as:

$$\Delta V_{\text{OUTA}} = V_{\text{DD}} \cdot \left(\frac{R5}{R1 + R2 + R5} \right)$$

In the previous example, this is an error of 4.3mV at the output of the amplifier or 43 μV at the input of the amplifier assuming a gain of 100.

Since the comparator can be used independently of the current sense amplifier, it is useful to know the threshold voltage equations with additional hysteresis. The input rising edge threshold which causes the output to transition from high to low is:

$$V_{\text{TH(R)}} = 400\text{mV} \cdot \left(1 + \frac{R1}{R2} \right)$$

The input falling edge threshold which causes the output to transition from low to high is:

$$V_{\text{TH(F)}} = 390\text{mV} \left(1 + \frac{R1}{R2} \right) - V_{\text{DD}} \left(\frac{R1}{R2} \right)$$

Comparator Output

The comparator output can maintain a logic-low level of 150mV while sinking 500 μA . The output can sink higher currents at elevated V_{OL} levels as shown in the Typical Performance Characteristics. Load currents are conducted to the V^- pin. The output off-state voltage may range between 0V and 60V with respect to V^- , regardless of the supply voltage used.

Reverse-Supply Protection

The LT6118 is not protected internally from external reversal of supply polarity. To prevent damage that may occur during this condition, a Schottky diode should be added in series with V^- (Figure 17). This will limit the reverse current through the LT6118. Note that this diode will limit the low voltage operation of the LT6118 by effectively reducing the supply voltage to the part by V_{D} .

Also note that the comparator reference, comparator output and LE input are referenced to the V^- pin. In order to preserve the precision of the reference and to avoid driving the comparator inputs below V^- , R2 must connect to the V^- pin. This will shift the amplifier output voltage up by V_{D} . V_{OUTA} can be accurately measured differentially across R1 and R2. The comparator output low voltage will also be shifted up by V_{D} . The LE pin threshold is referenced to the V^- pin. In order to provide valid input levels to the LT6118 and avoid driving LE below V^- the negative supply of the driving circuit should be tied to V^- of the LT6118.

APPLICATIONS INFORMATION

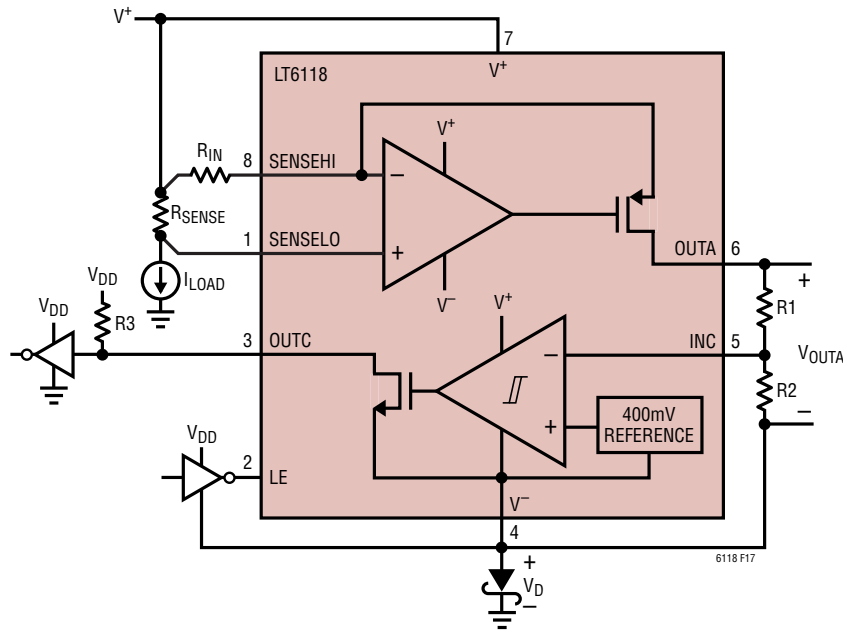
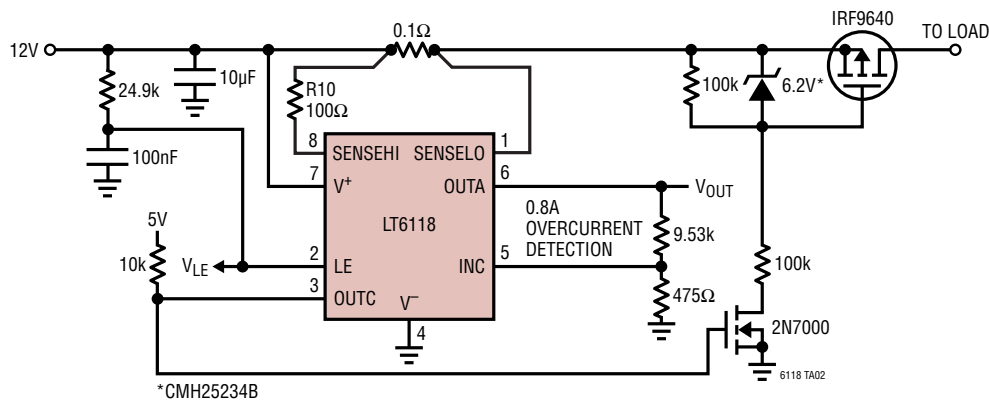


Figure 17. Schottky Prevents Damage During Supply Reversal

TYPICAL APPLICATIONS

Electronic Fuse with Power-On Reset

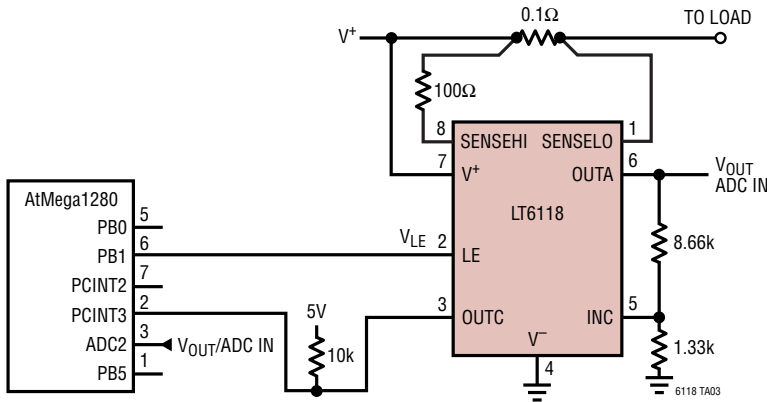


The electronic fuse can be reset either by pulling LE line low or by cycling the power to the system. The circuit is designed to have a 100µs power-on period. After power,

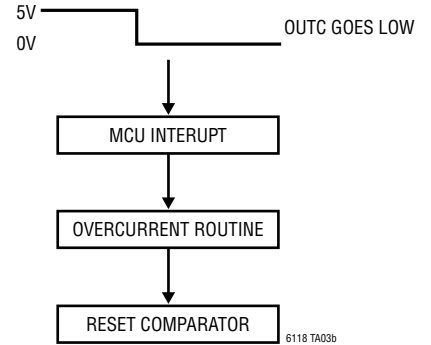
while LE is still below the threshold, the comparator is kept transparent to allow for initial inrush current.

TYPICAL APPLICATIONS

MCU Interfacing with Hardware Interrupts



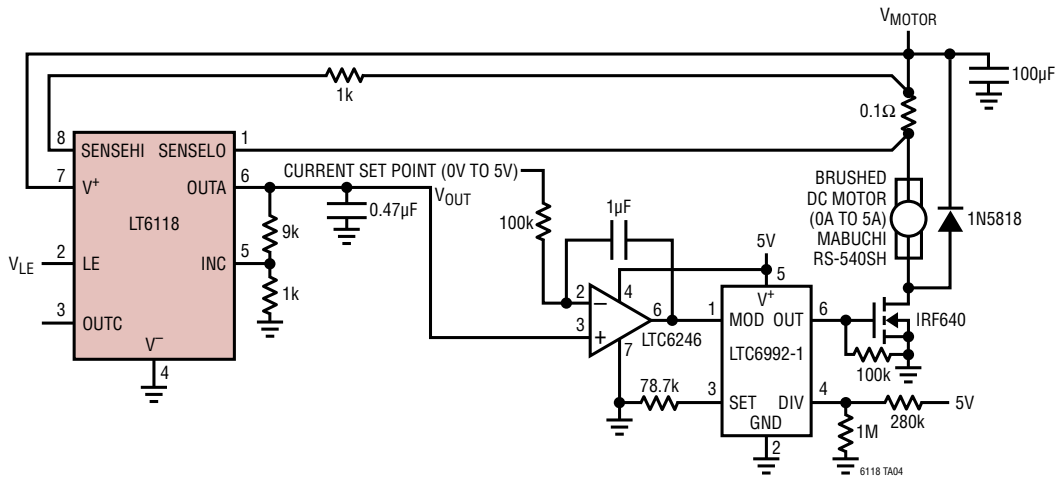
Example:



The comparator is set to have a 300mA overcurrent threshold. The MCU will receive the comparator output as

a hardware interrupt and immediately run an appropriate fault routine.

Simplified DC Motor Torque Control



The figure above shows a simplified DC motor control circuit. The circuit controls motor current, which is proportional to motor torque; the LT6118 is used to provide current feedback to an integrator that servos the motor

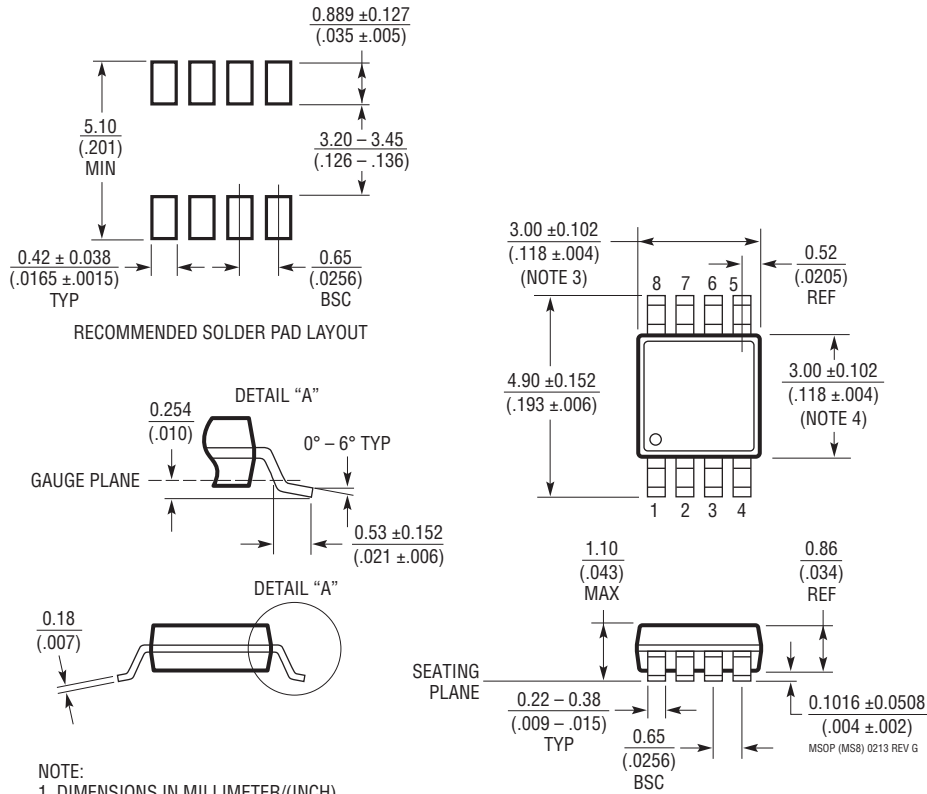
current to the current set point. The LTC®6992 is used to convert the output of the difference amp to the motors PWM control signal.

PACKAGE DESCRIPTION

Please refer to <http://www.linear.com/designtools/packaging/> for the most recent package drawings.

MS8 Package 8-Lead Plastic MSOP

(Reference LTC DWG # 05-08-1660 Rev G)

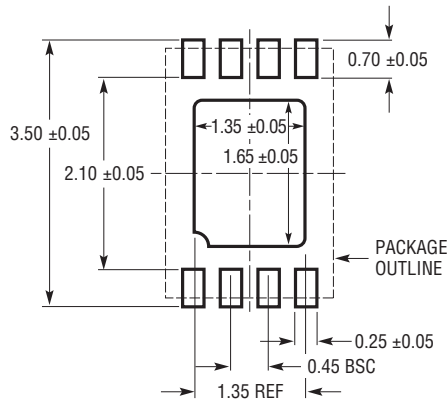


- NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
 2. DRAWING NOT TO SCALE
 3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
 4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
 5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

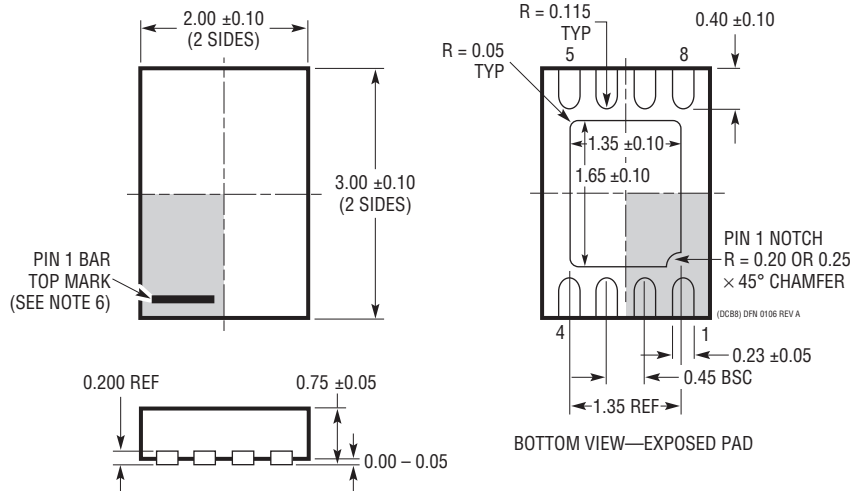
PACKAGE DESCRIPTION

Please refer to <http://www.linear.com/designtools/packaging/> for the most recent package drawings.

DCB Package 8-Lead Plastic DFN (2mm × 3mm) (Reference LTC DWG # 05-08-1718 Rev A)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



NOTE:

1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE