

## FEATURES

- **Low Noise Voltage: 1.9nV/ $\sqrt{\text{Hz}}$**
- **Low Supply Current: 1.2mA/Amp Max**
- **Low Offset Voltage: 350 $\mu\text{V}$  Max**
- **Gain-Bandwidth Product:**
  - LT6233: 60MHz;  $A_V \geq 1$
  - LT6233-10: 375MHz;  $A_V \geq 10$
- **Wide Supply Range: 3V to 12.6V**
- **Output Swings Rail-to-Rail**
- **Common Mode Rejection Ratio: 115dB Typ**
- **Output Current: 30mA**
- **Operating Temperature Range:  $-40^\circ\text{C}$  to  $85^\circ\text{C}$**
- **LT6233 Shutdown to 10 $\mu\text{A}$  Maximum**
- **LT6233/LT6233-10 in a Low Profile (1mm) ThinSOT™ Package**
- **Dual LT6234 in 8-Pin SO and Tiny DFN Packages**
- **LT6235 in a 16-Pin SSOP Package**

## APPLICATIONS

- Ultrasound Amplifiers
- Low Noise, Low Power Signal Processing
- Active Filters
- Driving A/D Converters
- Rail-to-Rail Buffer Amplifiers

## DESCRIPTION

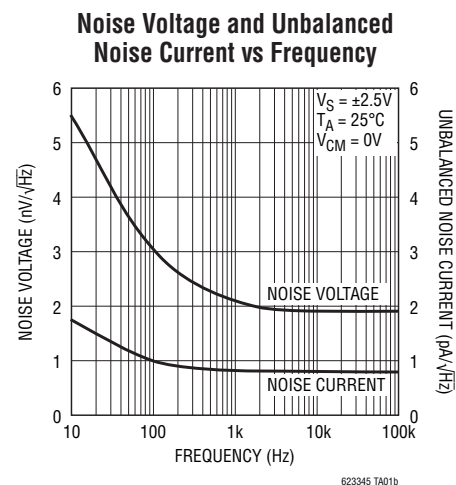
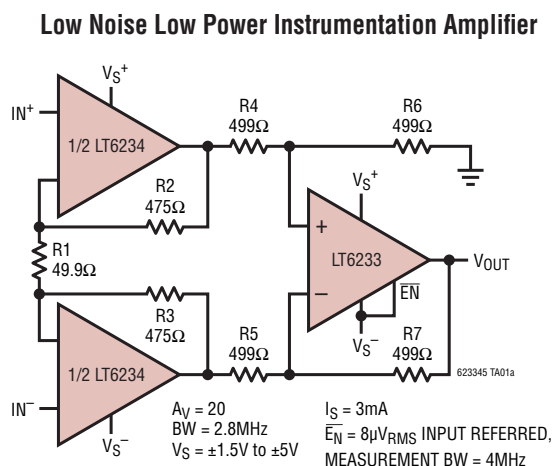
The LT<sup>®</sup>6233/LT6234/LT6235 are single/dual/quad low noise, rail-to-rail output unity-gain stable op amps that feature 1.9nV/ $\sqrt{\text{Hz}}$  noise voltage and draw only 1.2mA of supply current per amplifier. These amplifiers combine very low noise and supply current with a 60MHz gain-bandwidth product, a 17V/ $\mu\text{s}$  slew rate and are optimized for low supply voltage signal conditioning systems. The LT6233-10 is a single amplifier optimized for higher gain applications resulting in higher gain bandwidth and slew rate. The LT6233 and LT6233-10 include an enable pin that can be used to reduce the supply current to less than 10 $\mu\text{A}$ .

The amplifier family has an output that swings within 50mV of either supply rail to maximize the signal dynamic range in low supply applications and is specified on 3.3V, 5V and  $\pm 5\text{V}$  supplies. The  $e_n \cdot \sqrt{I_{\text{SUPPLY}}}$  product of 2.1 per amplifier is among the most noise efficient of any op amp.

The LT6233/LT6233-10 are available in the 6-lead SOT-23 package and the LT6234 dual is available in the 8-pin SO package with standard pinouts. For compact layouts, the dual is also available in a tiny dual fine pitch leadless package (DFN). The LT6235 is available in the 16-pin SSOP package.

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## TYPICAL APPLICATION



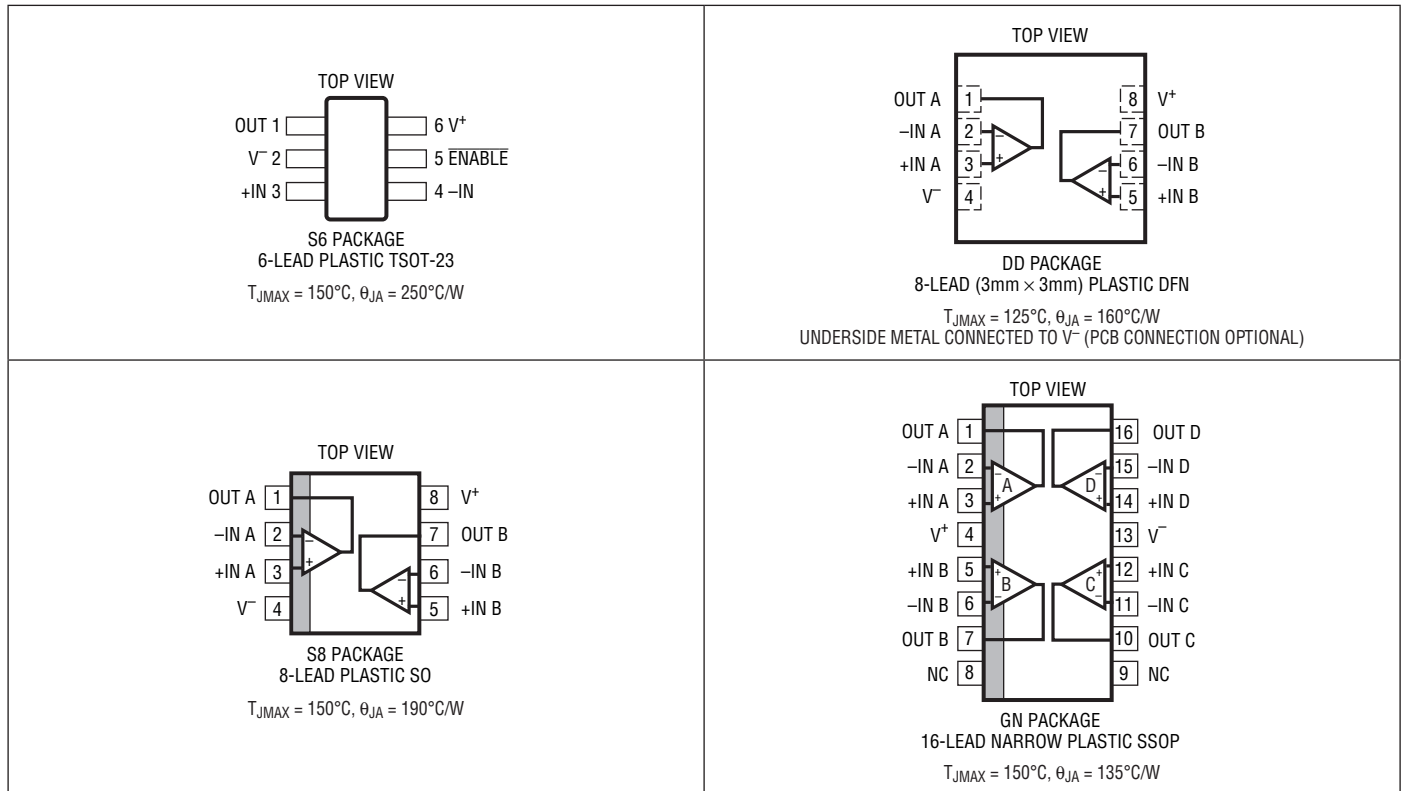
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# LT6233/LT6233-10 LT6234/LT6235

## ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage ( $V^+$ to $V^-$ ) .....	12.6V	Junction Temperature (DD Package).....	125°C
Input Current (Note 2).....	+40mA	Storage Temperature Range .....	-65°C to 150°C
Output Short-Circuit Duration (Note 3) .....	Indefinite	Storage Temperature Range (DD Package).....	-65°C to 125°C
Operating Temperature Range (Note 4)....	-40°C to 85°C	Lead Temperature (Soldering, 10 sec).....	300°C
Specified Temperature Range (Note 5) ....	-40°C to 85°C		
Junction Temperature .....	150°C		

## PIN CONFIGURATION



## ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LT6233CS6#PBF	LT6233CS6#TRPBF	LTAFL	6-Lead Plastic TSOT-23	0°C to 70°C
LT6233IS6#PBF	LT6233IS6#TRPBF	LTAFL	6-Lead Plastic TSOT-23	-40°C to 85°C
LT6233CS6-10#PBF	LT6233CS6-10#TRPBF	LTAFM	6-Lead Plastic TSOT-23	0°C to 70°C
LT6233IS6-10#PBF	LT6233IS6-10#TRPBF	LTAFM	6-Lead Plastic TSOT-23	-40°C to 85°C
LT6234CS8#PBF	LT6234CS8#TRPBF	6234	8-Lead Plastic SO	0°C to 70°C
LT6234IS8#PBF	LT6234IS8#TRPBF	6234I	8-Lead Plastic SO	-40°C to 85°C
LT6234CDD#PBF	LT6234CDD#TRPBF	LAET	8-Lead (3mm × 3mm) Plastic DFN	0°C to 70°C
LT6234IDD#PBF	LT6234IDD#TRPBF	LAET	8-Lead (3mm × 3mm) Plastic DFN	-40°C to 85°C
LT6235CGN#PBF	LT6235CGN#TRPBF	6235	16-Lead Narrow Plastic SSOP	0°C to 70°C
LT6235IGN#PBF	LT6235IGN#TRPBF	6235I	16-Lead Narrow Plastic SSOP	-40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. \*The temperature grade is identified by a label on the shipping container. Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandreel/>

## ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$ , $V_S = 5\text{V}$ , $0\text{V}$ ; $V_S = 3.3\text{V}$ , $0\text{V}$ ; $V_{CM} = V_{OUT} = \text{half supply}$ , ENABLE = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$V_{OS}$	Input Offset Voltage	LT6233S6, LT6233S6-10		100	500	$\mu\text{V}$
		LT6234S8, LT6235GN LT6234DD		50	350	$\mu\text{V}$
	Input Offset Voltage Match (Channel-to-Channel) (Note 6)			80	600	$\mu\text{V}$
$I_B$	Input Bias Current			1.5	3	$\mu\text{A}$
		$I_B$ Match (Channel-to-Channel) (Note 6)		0.04	0.3	$\mu\text{A}$
$I_{OS}$	Input Offset Current			0.04	0.3	$\mu\text{A}$
	Input Noise Voltage	0.1Hz to 10Hz		220		nV <sub>p-p</sub>
$e_n$	Input Noise Voltage Density	$f = 10\text{kHz}$ , $V_S = 5\text{V}$		1.9	3	nV/ $\sqrt{\text{Hz}}$
$i_n$	Input Noise Current Density, Balanced Source Input Noise Current Density, Unbalanced Source	$f = 10\text{kHz}$ , $V_S = 5\text{V}$ , $R_S = 10\text{k}$		0.43		pA/ $\sqrt{\text{Hz}}$
		$f = 10\text{kHz}$ , $V_S = 5\text{V}$ , $R_S = 10\text{k}$		0.78		pA/ $\sqrt{\text{Hz}}$
	Input Resistance	Common Mode		22		M $\Omega$
		Differential Mode		25		k $\Omega$
$C_{IN}$	Input Capacitance	Common Mode		2.5		pF
		Differential Mode		4.2		pF
$A_{VOL}$	Large-Signal Gain	$V_S = 5\text{V}$ , $V_O = 0.5\text{V}$ to $4.5\text{V}$ , $R_L = 10\text{k}$ to $V_S/2$	73	140		V/mV
		$V_S = 5\text{V}$ , $V_O = 0.5\text{V}$ to $4.5\text{V}$ , $R_L = 1\text{k}$ to $V_S/2$	18	35		V/mV
		$V_S = 3.3\text{V}$ , $V_O = 0.65\text{V}$ to $2.65\text{V}$ , $R_L = 10\text{k}$ to $V_S/2$	53	100		V/mV
		$V_S = 3.3\text{V}$ , $V_O = 0.65\text{V}$ to $2.65\text{V}$ , $R_L = 1\text{k}$ to $V_S/2$	11	20		V/mV
$V_{CM}$	Input Voltage Range	Guaranteed by CMRR, $V_S = 5\text{V}$ , $0\text{V}$	1.5		4	V
		Guaranteed by CMRR, $V_S = 3.3\text{V}$ , $0\text{V}$	1.15		2.65	V
CMRR	Common Mode Rejection Ratio	$V_S = 5\text{V}$ , $V_{CM} = 1.5\text{V}$ to $4\text{V}$	90	115		dB
		$V_S = 3.3\text{V}$ , $V_{CM} = 1.15\text{V}$ to $2.65\text{V}$	85	110		dB
	CMRR Match (Channel-to-Channel) (Note 6)	$V_S = 5\text{V}$ , $V_{CM} = 1.5\text{V}$ to $4\text{V}$	84	115		dB

# LT6233/LT6233-10

## LT6234/LT6235

### ELECTRICAL CHARACTERISTICS

$T_A = 25^\circ\text{C}$ ,  $V_S = 5\text{V}$ ,  $0\text{V}$ ;  $V_S = 3.3\text{V}$ ,  $0\text{V}$ ;  $V_{\text{CM}} = V_{\text{OUT}} = \text{half supply}$ ,  
**ENABLE = 0V**, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
PSRR	Power Supply Rejection Ratio	$V_S = 3\text{V to }10\text{V}$	90	115		dB
	PSRR Match (Channel-to-Channel) (Note 6)	$V_S = 3\text{V to }10\text{V}$	84	115		dB
	Minimum Supply Voltage (Note 7)		3			V
$V_{\text{OL}}$	Output Voltage Swing Low (Note 8)	No Load		4	40	mV
		$I_{\text{SINK}} = 5\text{mA}$		75	180	mV
		$V_S = 5\text{V}$ , $I_{\text{SINK}} = 15\text{mA}$		165	320	mV
		$V_S = 3.3\text{V}$ , $I_{\text{SINK}} = 10\text{mA}$		125	240	mV
$V_{\text{OH}}$	Output Voltage Swing High (Note 8)	No Load		5	50	mV
		$I_{\text{SOURCE}} = 5\text{mA}$		85	195	mV
		$V_S = 5\text{V}$ , $I_{\text{SOURCE}} = 15\text{mA}$		220	410	mV
		$V_S = 3.3\text{V}$ , $I_{\text{SOURCE}} = 10\text{mA}$		165	310	mV
$I_{\text{SC}}$	Short-Circuit Current	$V_S = 5\text{V}$	$\pm 40$	$\pm 55$		mA
		$V_S = 3.3\text{V}$	$\pm 35$	$\pm 50$		mA
$I_S$	Supply Current per Amplifier			1.05	1.2	mA
	Disabled Supply Current per Amplifier	ENABLE = $V^+ - 0.35\text{V}$		0.2	10	$\mu\text{A}$
$I_{\text{ENABLE}}$	ENABLE Pin Current	ENABLE = $0.3\text{V}$		-25	-75	$\mu\text{A}$
$V_L$	ENABLE Pin Input Voltage Low				0.3	V
$V_H$	ENABLE Pin Input Voltage High		$V^+ - 0.35$			V
	Output Leakage Current	ENABLE = $V^+ - 0.35\text{V}$ , $V_O = 1.5\text{V to }3.5\text{V}$		0.2	10	$\mu\text{A}$
$t_{\text{ON}}$	Turn-On Time	ENABLE = $5\text{V to }0\text{V}$ , $R_L = 1\text{k}$ , $V_S = 5\text{V}$		500		ns
$t_{\text{OFF}}$	Turn-Off Time	ENABLE = $0\text{V to }5\text{V}$ , $R_L = 1\text{k}$ , $V_S = 5\text{V}$		76		$\mu\text{s}$
GBW	Gain-Bandwidth Product	Frequency = $1\text{MHz}$ , $V_S = 5\text{V}$		55		MHz
		LT6233-10		320		MHz
SR	Slew Rate	$V_S = 5\text{V}$ , $A_V = -1$ , $R_L = 1\text{k}$ , $V_O = 1.5\text{V to }3.5\text{V}$	10	15		$\text{V}/\mu\text{s}$
		LT6233-10, $V_S = 5\text{V}$ , $A_V = -10$ , $R_L = 1\text{k}$ , $V_O = 1.5\text{V to }3.5\text{V}$		80		$\text{V}/\mu\text{s}$
FPBW	Full-Power Bandwidth	$V_S = 5\text{V}$ , $V_{\text{OUT}} = 3V_{\text{P-P}}$ (Note 9)	1.06	1.6		MHz
		LT6233-10, $\text{HD}_2 = \text{HD}_3 \leq 1\%$		2.2		MHz
$t_S$	Settling Time (LT6233, LT6234, LT6235)	$0.1\%$ , $V_S = 5\text{V}$ , $V_{\text{STEP}} = 2\text{V}$ , $A_V = -1$ , $R_L = 1\text{k}$		175		ns

**ELECTRICAL CHARACTERISTICS** The ● denotes the specifications which apply over the  $0^{\circ}\text{C} < T_A < 70^{\circ}\text{C}$  temperature range.  $V_S = 5\text{V}, 0\text{V}$ ;  $V_S = 3.3\text{V}, 0\text{V}$ ;  $V_{CM} = V_{OUT} = \text{half supply}$ ,  $\overline{\text{ENABLE}} = 0\text{V}$ , unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OS}$	Input Offset Voltage	LT6233CS6, LT6233CS6-10	●		600	$\mu\text{V}$
		LT6234CS8, LT6235CGN	●		450	$\mu\text{V}$
		LT6234CDD	●		550	$\mu\text{V}$
	Input Offset Voltage Match (Channel-to-Channel) (Note 6)		●		800	$\mu\text{V}$
$V_{OS\ TC}$	Input Offset Voltage Drift (Note 10)	$V_{CM} = \text{Half Supply}$	●	0.5	3.0	$\mu\text{V}/^{\circ}\text{C}$
$I_B$	Input Bias Current		●		3.5	$\mu\text{A}$
	$I_B$ Match (Channel-to-Channel) (Note 6)		●		0.4	$\mu\text{A}$
$I_{OS}$	Input Offset Current		●		0.4	$\mu\text{A}$
$A_{VOL}$	Large-Signal Gain	$V_S = 5\text{V}, V_O = 0.5\text{V to } 4.5\text{V}, R_L = 10\text{k to } V_S/2$	●	47		$\text{V/mV}$
		$V_S = 5\text{V}, V_O = 0.5\text{V to } 4.5\text{V}, R_L = 1\text{k to } V_S/2$	●	12		$\text{V/mV}$
		$V_S = 3.3\text{V}, V_O = 0.65\text{V to } 2.65\text{V}, R_L = 10\text{k to } V_S/2$	●	40		$\text{V/mV}$
		$V_S = 3.3\text{V}, V_O = 0.65\text{V to } 2.65\text{V}, R_L = 1\text{k to } V_S/2$	●	7.5		$\text{V/mV}$
$V_{CM}$	Input Voltage Range	Guaranteed by CMRR	●			
		$V_S = 5\text{V}, 0\text{V}$ $V_S = 3.3\text{V}, 0\text{V}$	●	1.5 1.15	4 2.65	$\text{V}$ $\text{V}$
CMRR	Common Mode Rejection Ratio	$V_S = 5\text{V}, V_{CM} = 1.5\text{V to } 4\text{V}$ $V_S = 3.3\text{V}, V_{CM} = 1.15\text{V to } 2.65\text{V}$	●	90		$\text{dB}$
	CMRR Match (Channel-to-Channel) (Note 6)	$V_S = 5\text{V}, V_{CM} = 1.5\text{V to } 4\text{V}$	●	85		$\text{dB}$
PSRR	Power Supply Rejection Ratio	$V_S = 3\text{V to } 10\text{V}$	●	90		$\text{dB}$
	PSRR Match (Channel-to-Channel) (Note 6)	$V_S = 3\text{V to } 10\text{V}$	●	84		$\text{dB}$
	Minimum Supply Voltage (Note 7)		●	3		$\text{V}$
$V_{OL}$	Output Voltage Swing Low (Note 8)	No Load	●		50	$\text{mV}$
		$I_{SINK} = 5\text{mA}$	●		195	$\text{mV}$
		$V_S = 5\text{V}, I_{SINK} = 15\text{mA}$	●		360	$\text{mV}$
		$V_S = 3.3\text{V}, I_{SINK} = 10\text{mA}$	●		265	$\text{mV}$
$V_{OH}$	Output Voltage Swing High (Note 8)	No Load	●		60	$\text{mV}$
		$I_{SOURCE} = 5\text{mA}$	●		205	$\text{mV}$
		$V_S = 5\text{V}, I_{SOURCE} = 15\text{mA}$	●		435	$\text{mV}$
		$V_S = 3.3\text{V}, I_{SOURCE} = 10\text{mA}$	●		330	$\text{mV}$
$I_{SC}$	Short-Circuit Current	$V_S = 5\text{V}$	●	$\pm 35$		$\text{mA}$
		$V_S = 3.3\text{V}$	●	$\pm 30$		$\text{mA}$
$I_S$	Supply Current per Amplifier		●		1.45	$\text{mA}$
	Disabled Supply Current per Amplifier	$\overline{\text{ENABLE}} = V^+ - 0.25\text{V}$	●	1		$\mu\text{A}$
$I_{\overline{\text{ENABLE}}}$	ENABLE Pin Current	$\overline{\text{ENABLE}} = 0.3\text{V}$	●		-85	$\mu\text{A}$
$V_L$	ENABLE Pin Input Voltage Low		●		0.3	$\text{V}$
$V_H$	ENABLE Pin Input Voltage High		●	$V^+ - 0.25$		$\text{V}$
	Output Leakage Current	$\overline{\text{ENABLE}} = V^+ - 0.25\text{V}, V_O = 1.5\text{V to } 3.5\text{V}$	●	1		$\mu\text{A}$
$t_{ON}$	Turn-On Time	$\overline{\text{ENABLE}} = 5\text{V to } 0\text{V}, R_L = 1\text{k}, V_S = 5\text{V}$	●	500		$\text{ns}$
$t_{OFF}$	Turn-Off Time	$\overline{\text{ENABLE}} = 0\text{V to } 5\text{V}, R_L = 1\text{k}, V_S = 5\text{V}$	●	120		$\mu\text{s}$
SR	Slew Rate	$V_S = 5\text{V}, A_V = -1, R_L = 1\text{k}, V_O = 1.5\text{V to } 3.5\text{V}$	●	9		$\text{V}/\mu\text{s}$
		LT6233-10, $A_V = -10, R_L = 1\text{k}, V_O = 1.5\text{V to } 3.5\text{V}$	●	75		$\text{V}/\mu\text{s}$
FPBW	Full-Power Bandwidth (Note 9)	$V_S = 5\text{V}, V_{OUT} = 3V_{P-P}$ ; LT6233C, LT6234C, LT6235C	●	955		$\text{kHz}$

# LT6233/LT6233-10

## LT6234/LT6235

**ELECTRICAL CHARACTERISTICS** The ● denotes the specifications which apply over the  $-40^{\circ}\text{C} < T_A < 85^{\circ}\text{C}$  temperature range.  $V_S = 5\text{V}, 0\text{V}$ ;  $V_S = 3.3\text{V}, 0\text{V}$ ;  $V_{\text{CM}} = V_{\text{OUT}} = \text{half supply}$ ,  $\text{ENABLE} = 0\text{V}$ , unless otherwise noted. (Note 5)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$V_{\text{OS}}$	Input Offset Voltage	LT6233IS6, LT6233IS6-10	●		700	$\mu\text{V}$
		LT6234IS8, LT6235IGN	●		550	$\mu\text{V}$
		LT6234IDD	●		650	$\mu\text{V}$
	Input Offset Voltage Match (Channel-to-Channel) (Note 6)		●		1000	$\mu\text{V}$
$V_{\text{OS TC}}$	Input Offset Voltage Drift (Note 10)	$V_{\text{CM}} = \text{Half Supply}$	●	0.5	3	$\mu\text{V}/^{\circ}\text{C}$
$I_{\text{B}}$	Input Bias Current		●		4	$\mu\text{A}$
	$I_{\text{B}}$ Match (Channel-to-Channel) (Note 6)		●		0.4	$\mu\text{A}$
$I_{\text{OS}}$	Input Offset Current		●		0.5	$\mu\text{A}$
$A_{\text{VOL}}$	Large-Signal Gain	$V_S = 5\text{V}, V_0 = 0.5\text{V to } 4.5\text{V}, R_L = 10\text{k to } V_S/2$	●	45		$\text{V/mV}$
		$V_S = 5\text{V}, V_0 = 0.5\text{V to } 4.5\text{V}, R_L = 1\text{k to } V_S/2$	●	11		$\text{V/mV}$
		$V_S = 3.3\text{V}, V_0 = 0.65\text{V to } 2.65\text{V}, R_L = 10\text{k to } V_S/2$	●	38		$\text{V/mV}$
		$V_S = 3.3\text{V}, V_0 = 0.65\text{V to } 2.65\text{V}, R_L = 1\text{k to } V_S/2$	●	7		$\text{V/mV}$
$V_{\text{CM}}$	Input Voltage Range	Guaranteed by CMRR	●			$\text{V}$
		$V_S = 5\text{V}, 0\text{V}$ $V_S = 3.3\text{V}, 0\text{V}$	●	1.5 1.15	4 2.65	$\text{V}$
CMRR	Common Mode Rejection Ratio	$V_S = 5\text{V}, V_{\text{CM}} = 1.5\text{V to } 4\text{V}$ $V_S = 3.3\text{V}, V_{\text{CM}} = 1.15\text{V to } 2.65\text{V}$	●	90		$\text{dB}$
			●	85		$\text{dB}$
	CMRR Match (Channel-to-Channel) (Note 6)	$V_S = 5\text{V}, V_{\text{CM}} = 1.5\text{V to } 4\text{V}$	●	84		$\text{dB}$
PSRR	Power Supply Rejection Ratio	$V_S = 3\text{V to } 10\text{V}$	●	90		$\text{dB}$
	PSRR Match (Channel-to-Channel) (Note 6)	$V_S = 3\text{V to } 10\text{V}$	●	84		$\text{dB}$
	Minimum Supply Voltage (Note 7)		●	3		$\text{V}$
$V_{\text{OL}}$	Output Voltage Swing Low (Note 8)	No Load	●		50	$\text{mV}$
		$I_{\text{SINK}} = 5\text{mA}$	●		195	$\text{mV}$
		$V_S = 5\text{V}, I_{\text{SINK}} = 15\text{mA}$	●		370	$\text{mV}$
		$V_S = 3.3\text{V}, I_{\text{SINK}} = 10\text{mA}$	●		275	$\text{mV}$
$V_{\text{OH}}$	Output Voltage Swing High (Note 6)	No Load	●		60	$\text{mV}$
		$I_{\text{SOURCE}} = 5\text{mA}$	●		210	$\text{mV}$
		$V_S = 5\text{V}, I_{\text{SOURCE}} = 15\text{mA}$	●		445	$\text{mV}$
		$V_S = 3.3\text{V}, I_{\text{SOURCE}} = 10\text{mA}$	●		335	$\text{mV}$
$I_{\text{SC}}$	Short-Circuit Current	$V_S = 5\text{V}$	●	$\pm 30$		$\text{mA}$
		$V_S = 3.3\text{V}$	●	$\pm 20$		$\text{mA}$
$I_{\text{S}}$	Supply Current per Amplifier		●		1.5	$\text{mA}$
	Disabled Supply Current per Amplifier	$\text{ENABLE} = V^+ - 0.2\text{V}$	●	1		$\mu\text{A}$
$I_{\text{ENABLE}}$	ENABLE Pin Current	$\text{ENABLE} = 0.3\text{V}$	●		-100	$\mu\text{A}$
$V_{\text{L}}$	ENABLE Pin Input Voltage Low		●		0.3	$\text{V}$
$V_{\text{H}}$	ENABLE Pin Input Voltage High		●	$V^+ - 0.2$		$\text{V}$
	Output Leakage Current	$\text{ENABLE} = V^+ - 0.2\text{V}, V_0 = 1.5\text{V to } 3.5\text{V}$	●	1		$\mu\text{A}$
$t_{\text{ON}}$	Turn-On Time	$\text{ENABLE} = 5\text{V to } 0\text{V}, R_L = 1\text{k}, V_S = 5\text{V}$	●	500		$\text{ns}$
$t_{\text{OFF}}$	Turn-Off Time	$\text{ENABLE} = 0\text{V to } 5\text{V}, R_L = 1\text{k}, V_S = 5\text{V}$	●	135		$\mu\text{s}$
SR	Slew Rate	$V_S = 5\text{V}, A_V = -1, R_L = 1\text{k}, V_0 = 1.5\text{V to } 3.5\text{V}$	●	8		$\text{V}/\mu\text{s}$
		LT6233-10, $A_V = -10, R_L = 1\text{k}, V_0 = 1.5\text{V to } 3.5\text{V}$	●	70		$\text{V}/\mu\text{s}$
FPBW	Full-Power Bandwidth (Note 9)	$V_S = 5\text{V}, V_{\text{OUT}} = 3\text{V}_{\text{P-P}}$ ; LT6233I, LT6234I, LT6235I	●	848		$\text{kHz}$

**ELECTRICAL CHARACTERISTICS**  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 5\text{V}$ ,  $V_{\text{CM}} = V_{\text{OUT}} = 0\text{V}$ ,  $\overline{\text{ENABLE}} = 0\text{V}$ , unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$V_{\text{OS}}$	Input Offset Voltage	LT6233S6, LT6233S6-10		100	500	$\mu\text{V}$
		LT6234S8, LT6235GN		50	350	$\mu\text{V}$
		LT6234DD		75	450	$\mu\text{V}$
	Input Offset Voltage Match (Channel-to-Channel) (Note 6)			100	600	$\mu\text{V}$
$I_{\text{B}}$	Input Bias Current			1.5	3	$\mu\text{A}$
	$I_{\text{B}}$ Match (Channel-to-Channel) (Note 6)			0.04	0.3	$\mu\text{A}$
$I_{\text{OS}}$	Input Offset Current			0.04	0.3	$\mu\text{A}$
	Input Noise Voltage	0.1Hz to 10Hz		220		$\text{nV}_{\text{P-P}}$
$e_{\text{n}}$	Input Noise Voltage Density	$f = 10\text{kHz}$		1.9	3.0	$\text{nV}/\sqrt{\text{Hz}}$
$i_{\text{n}}$	Input Noise Current Density, Balanced Source	$f = 10\text{kHz}$ , $R_{\text{S}} = 10\text{k}$		0.43		$\text{pA}/\sqrt{\text{Hz}}$
	Input Noise Current Density, Unbalanced Source	$f = 10\text{kHz}$ , $R_{\text{S}} = 10\text{k}$		0.78		$\text{pA}/\sqrt{\text{Hz}}$
	Input Resistance	Common Mode		22		$\text{M}\Omega$
		Differential Mode		25		$\text{k}\Omega$
$C_{\text{IN}}$	Input Capacitance	Common Mode		2.1		$\text{pF}$
		Differential Mode		3.7		$\text{pF}$
$A_{\text{VOL}}$	Large-Signal Gain	$V_{\text{O}} = \pm 4.5\text{V}$ , $R_{\text{L}} = 10\text{k}$	97	180		$\text{V}/\text{mV}$
		$V_{\text{O}} = \pm 4.5\text{V}$ , $R_{\text{L}} = 1\text{k}$	28	55		$\text{V}/\text{mV}$
$V_{\text{CM}}$	Input Voltage Range	Guaranteed by CMRR	-3		4	$\text{V}$
CMRR	Common Mode Rejection Ratio	$V_{\text{CM}} = -3\text{V}$ to $4\text{V}$	90	110		$\text{dB}$
	CMRR Match (Channel-to-Channel) (Note 6)	$V_{\text{CM}} = -3\text{V}$ to $4\text{V}$	84	120		$\text{dB}$
PSRR	Power Supply Rejection Ratio	$V_{\text{S}} = \pm 1.5\text{V}$ to $\pm 5\text{V}$	90	115		$\text{dB}$
	PSRR Match (Channel-to-Channel) (Note 6)	$V_{\text{S}} = \pm 1.5\text{V}$ to $\pm 5\text{V}$	84	115		$\text{dB}$
$V_{\text{OL}}$	Output Voltage Swing Low (Note 8)	No Load		4	40	$\text{mV}$
		$I_{\text{SINK}} = 5\text{mA}$		75	180	$\text{mV}$
		$I_{\text{SINK}} = 15\text{mA}$		165	320	$\text{mV}$
$V_{\text{OH}}$	Output Voltage Swing High (Note 8)	No Load		5	50	$\text{mV}$
		$I_{\text{SOURCE}} = 5\text{mA}$		85	195	$\text{mV}$
		$I_{\text{SOURCE}} = 15\text{mA}$		220	410	$\text{mV}$
$I_{\text{SC}}$	Short-Circuit Current		$\pm 40$	$\pm 55$		$\text{mA}$
$I_{\text{S}}$	Supply Current per Amplifier			1.15	1.4	$\text{mA}$
	Disabled Supply Current per Amplifier	$\overline{\text{ENABLE}} = 4.65\text{V}$		0.2	10	$\mu\text{A}$
$I_{\text{ENABLE}}$	ENABLE Pin Current	$\overline{\text{ENABLE}} = 0.3\text{V}$		-35	-85	$\mu\text{A}$
$V_{\text{L}}$	ENABLE Pin Input Voltage Low				0.3	$\text{V}$
$V_{\text{H}}$	ENABLE Pin Input Voltage High		4.65			$\text{V}$
	Output Leakage Current	$\overline{\text{ENABLE}} = 4.65\text{V}$ , $V_{\text{O}} = \pm 1\text{V}$		0.2	10	$\mu\text{A}$
$t_{\text{ON}}$	Turn-On Time	$\overline{\text{ENABLE}} = 5\text{V}$ to $0\text{V}$ , $R_{\text{L}} = 1\text{k}$		900		$\text{ns}$
$t_{\text{OFF}}$	Turn-Off Time	$\overline{\text{ENABLE}} = 0\text{V}$ to $5\text{V}$ , $R_{\text{L}} = 1\text{k}$		100		$\mu\text{s}$
GBW	Gain-Bandwidth Product	Frequency = $1\text{MHz}$	42	60		$\text{MHz}$
		LT6233-10	260	375		$\text{MHz}$
SR	Slew Rate	$A_{\text{V}} = -1$ , $R_{\text{L}} = 1\text{k}$ , $V_{\text{O}} = -2\text{V}$ to $2\text{V}$	12	17		$\text{V}/\mu\text{s}$
		LT6233-10, $A_{\text{V}} = -10$ , $R_{\text{L}} = 1\text{k}$ , $V_{\text{O}} = -2\text{V}$ to $2\text{V}$		115		$\text{V}/\mu\text{s}$
FPBW	Full-Power Bandwidth	$V_{\text{OUT}} = 3\text{V}_{\text{P-P}}$ (Note 9)	1.27	1.8		$\text{MHz}$
		LT6233-10, $\text{HD2} = \text{HD3} \leq 1\%$		2.2		$\text{MHz}$
$t_{\text{S}}$	Settling Time (LT6233, LT6234, LT6235)	0.1%, $V_{\text{STEP}} = 2\text{V}$ , $A_{\text{V}} = -1$ , $R_{\text{L}} = 1\text{k}$		170		$\text{ns}$

# LT6233/LT6233-10

## LT6234/LT6235

**ELECTRICAL CHARACTERISTICS** The ● denotes the specifications which apply over the  $0^{\circ}\text{C} < T_A < 70^{\circ}\text{C}$  temperature range.  $V_S = \pm 5\text{V}$ ,  $V_{\text{CM}} = V_{\text{OUT}} = 0\text{V}$ ,  $\overline{\text{ENABLE}} = 0\text{V}$ , unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{\text{OS}}$	Input Offset Voltage	LT6233CS6, LT6233CS6-10	●			600	$\mu\text{V}$
		LT6234CS8, LT6235CGN	●			450	$\mu\text{V}$
		LT6234CDD	●			550	$\mu\text{V}$
	Input Offset Voltage Match (Channel-to-Channel) (Note 6)		●			800	$\mu\text{V}$
$V_{\text{OS TC}}$	Input Offset Voltage Drift (Note 10)		●		0.5	3	$\mu\text{V}/^{\circ}\text{C}$
$I_{\text{B}}$	Input Bias Current		●			3.5	$\mu\text{A}$
	$I_{\text{B}}$ Match (Channel-to-Channel) (Note 6)		●			0.4	$\mu\text{A}$
$I_{\text{OS}}$	Input Offset Current		●			0.4	$\mu\text{A}$
$A_{\text{VOL}}$	Large-Signal Gain	$V_0 = \pm 4.5\text{V}$ , $R_{\text{L}} = 10\text{k}$	●	75			$\text{V}/\text{mV}$
		$V_0 = \pm 4.5\text{V}$ , $R_{\text{L}} = 1\text{k}$	●	22			$\text{V}/\text{mV}$
$V_{\text{CM}}$	Input Voltage Range	Guaranteed by CMRR	●	-3		4	V
CMRR	Common Mode Rejection Ratio	$V_{\text{CM}} = -3\text{V}$ to $4\text{V}$	●	90			dB
	CMRR Match (Channel-to-Channel) (Note 6)	$V_{\text{CM}} = -3\text{V}$ to $4\text{V}$	●	84			dB
PSRR	Power Supply Rejection Ratio	$V_{\text{S}} = \pm 1.5\text{V}$ to $\pm 5\text{V}$	●	90			dB
	PSRR Match (Channel-to-Channel) (Note 6)	$V_{\text{S}} = \pm 1.5\text{V}$ to $\pm 5\text{V}$	●	84			dB
$V_{\text{OL}}$	Output Voltage Swing Low (Note 8)	No Load	●			50	mV
		$I_{\text{SINK}} = 5\text{mA}$	●			195	mV
		$I_{\text{SINK}} = 15\text{mA}$	●			360	mV
$V_{\text{OH}}$	Output Voltage Swing High (Note 8)	No Load	●			60	mV
		$I_{\text{SOURCE}} = 5\text{mA}$	●			205	mV
		$I_{\text{SOURCE}} = 15\text{mA}$	●			435	mV
$I_{\text{SC}}$	Short-Circuit Current		●	$\pm 35$			mA
$I_{\text{S}}$	Supply Current per Amplifier Disabled Supply Current per Amplifier	$\overline{\text{ENABLE}} = 4.75\text{V}$	●			1.7	mA
			●		1		$\mu\text{A}$
$I_{\overline{\text{ENABLE}}}$	$\overline{\text{ENABLE}}$ Pin Current	$\overline{\text{ENABLE}} = 0.3\text{V}$	●			-95	$\mu\text{A}$
$V_{\text{L}}$	$\overline{\text{ENABLE}}$ Pin Input Voltage Low		●			0.3	V
$V_{\text{H}}$	$\overline{\text{ENABLE}}$ Pin Input Voltage High		●	4.75			V
	Output Leakage Current	$\overline{\text{ENABLE}} = 4.75\text{V}$ , $V_0 = \pm 1\text{V}$	●		1		$\mu\text{A}$
$t_{\text{ON}}$	Turn-On Time	$\overline{\text{ENABLE}} = 5\text{V}$ to $0\text{V}$ , $R_{\text{L}} = 1\text{k}$	●		900		ns
$t_{\text{OFF}}$	Turn-Off Time	$\overline{\text{ENABLE}} = 0\text{V}$ to $5\text{V}$ , $R_{\text{L}} = 1\text{k}$	●		150		$\mu\text{s}$
SR	Slew Rate	$A_{\text{V}} = -1$ , $R_{\text{L}} = 1\text{k}$ , $V_0 = -2\text{V}$ to $2\text{V}$	●	11			$\text{V}/\mu\text{s}$
		LT6233-10, $A_{\text{V}} = -10$ , $R_{\text{L}} = 1\text{k}$ , $V_0 = -2\text{V}$ to $2\text{V}$	●		105		$\text{V}/\mu\text{s}$
FPBW	Full-Power Bandwidth (Note 9)	$V_{\text{OUT}} = 3\text{V}_{\text{P-P}}$ ; LT6233C, LT6234C, LT6235C	●	1.16			MHz



**ELECTRICAL CHARACTERISTICS** The ● denotes the specifications which apply over the  $-40^{\circ}\text{C} < T_A < 85^{\circ}\text{C}$  temperature range.  $V_S = \pm 5\text{V}$ ,  $V_{\text{CM}} = V_{\text{OUT}} = 0\text{V}$ ,  $\text{ENABLE} = 0\text{V}$ , unless otherwise noted. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{\text{OS}}$	Input Offset Voltage	LT6233IS6, LT6233IS6-10	●			700	$\mu\text{V}$
		LT6234IS8, LT6235IGN	●			550	$\mu\text{V}$
		LT6234IDD	●			650	$\mu\text{V}$
	Input Offset Voltage Match (Channel-to-Channel) (Note 6)		●			1000	$\mu\text{V}$
$V_{\text{OS TC}}$	Input Offset Voltage Drift (Note 10)		●		0.5	3	$\mu\text{V}/^{\circ}\text{C}$
$I_B$	Input Bias Current		●			4	$\mu\text{A}$
	$I_B$ Match (Channel-to-Channel) (Note 6)		●			0.4	$\mu\text{A}$
$I_{\text{OS}}$	Input Offset Current		●			0.5	$\mu\text{A}$
$A_{\text{VOL}}$	Large-Signal Gain	$V_O = \pm 4.5\text{V}$ , $R_L = 10\text{k}$	●	68			$\text{V}/\text{mV}$
		$V_O = \pm 4.5\text{V}$ , $R_L = 1\text{k}$	●	20			$\text{V}/\text{mV}$
$V_{\text{CM}}$	Input Voltage Range	Guaranteed by CMRR	●	-3		4	V
CMRR	Common Mode Rejection Ratio	$V_{\text{CM}} = -3\text{V}$ to $4\text{V}$	●	90			dB
	CMRR Match (Channel-to-Channel) (Note 6)	$V_{\text{CM}} = -3\text{V}$ to $4\text{V}$	●	84			dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 1.5\text{V}$ to $\pm 5\text{V}$	●	90			dB
	PSRR Match (Channel-to-Channel) (Note 6)	$V_S = \pm 1.5\text{V}$ to $\pm 5\text{V}$	●	84			dB
$V_{\text{OL}}$	Output Voltage Swing Low (Note 8)	No Load	●			50	mV
		$I_{\text{SINK}} = 5\text{mA}$	●			195	mV
		$I_{\text{SINK}} = 15\text{mA}$	●			370	mV
$V_{\text{OH}}$	Output Voltage Swing High (Note 8)	No Load	●			70	mV
		$I_{\text{SOURCE}} = 5\text{mA}$	●			210	mV
		$I_{\text{SOURCE}} = 15\text{mA}$	●			445	mV
$I_{\text{SC}}$	Short-Circuit Current		●	$\pm 30$			mA
$I_S$	Supply Current per Amplifier		●			1.75	mA
	Disabled Supply Current per Amplifier	$\text{ENABLE} = 4.8\text{V}$	●		1		$\mu\text{A}$
$I_{\text{ENABLE}}$	ENABLE Pin Current	$\text{ENABLE} = 0.3\text{V}$	●			-110	$\mu\text{A}$
$V_L$	ENABLE Pin Input Voltage Low		●			0.3	V
$V_H$	ENABLE Pin Input Voltage High		●	4.8			V
	Output Leakage Current	$\text{ENABLE} = 4.8\text{V}$ , $V_O = \pm 1\text{V}$	●		1		$\mu\text{A}$
$t_{\text{ON}}$	Turn-On Time	$\text{ENABLE} = 5\text{V}$ to $0\text{V}$ , $R_L = 1\text{k}$	●		900		ns
$t_{\text{OFF}}$	Turn-Off Time	$\text{ENABLE} = 0\text{V}$ to $5\text{V}$ , $R_L = 1\text{k}$	●		160		$\mu\text{s}$
SR	Slew Rate	$A_V = -1$ , $R_L = 1\text{k}$ , $V_O = -2\text{V}$ to $2\text{V}$	●	10			$\text{V}/\mu\text{s}$
		LT6233-10, $A_V = -10$ , $R_L = 1\text{k}$ , $V_O = -2\text{V}$ to $2\text{V}$	●		95		$\text{V}/\mu\text{s}$
FPBW	Full-Power Bandwidth (Note 9)	$V_{\text{OUT}} = 3V_{\text{P-P}}$ ; LT6233I, LT6234I, LT6235I	●	1.06			MHz

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** Inputs are protected by back-to-back diodes. If the differential input voltage exceeds 0.7V, the input current must be limited to less than 40mA.

**Note 3:** A heat sink may be required to keep the junction temperature below the absolute maximum rating when the output is shorted indefinitely.

**Note 4:** The LT6233C/LT6233I, the LT6234C/LT6234I, and LT6235C/LT6235I are guaranteed functional over the temperature range of  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

**Note 5:** The LT6233C/LT6234C/LT6235C are guaranteed to meet specified performance from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ . The LT6233C/LT6234C/LT6235C are designed, characterized and expected to meet specified performance from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ , but are not tested or QA sampled at these temperatures. The LT6233I/LT6234I/LT6235I are guaranteed to meet specified performance from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

**Note 6:** Matching parameters are the difference between the two amplifiers A and D and between B and C of the LT6235; between the two amplifiers of the LT6234. CMRR and PSRR match are defined as follows: CMRR and PSRR are measured in  $\mu\text{V}/\text{V}$  on the matched amplifiers. The difference is calculated between the matching sides in  $\mu\text{V}/\text{V}$ . The result is converted to dB.

## ELECTRICAL CHARACTERISTICS

**Note 7:** Minimum supply voltage is guaranteed by power supply rejection ratio test.

**Note 8:** Output voltage swings are measured between the output and power supply rails.

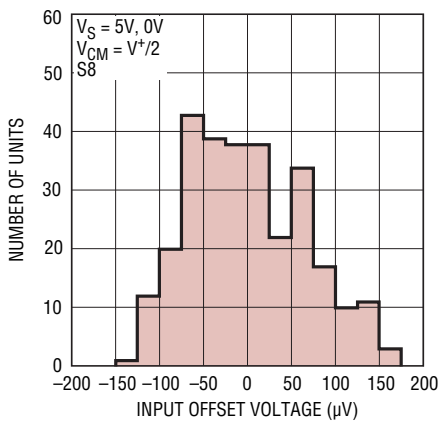
**Note 9:** Full-power bandwidth is calculated from the slew rate:

$$FPBW = SR/2\pi V_P$$

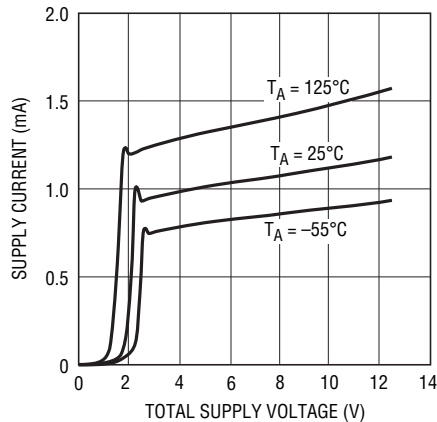
**Note 10:** This parameter is not 100% tested.

## TYPICAL PERFORMANCE CHARACTERISTICS (LT6233/LT6234/LT6235)

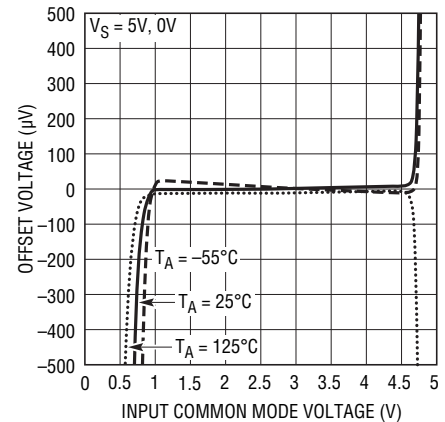
**V<sub>OS</sub> Distribution**



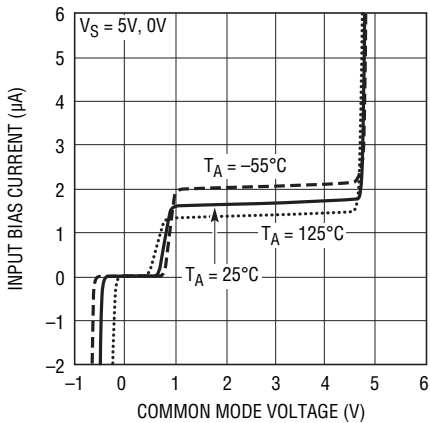
**Supply Current vs Supply Voltage  
(Per Amplifier)**



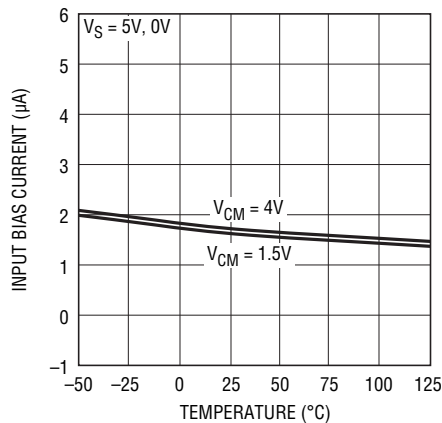
**Offset Voltage vs Input Common Mode Voltage**



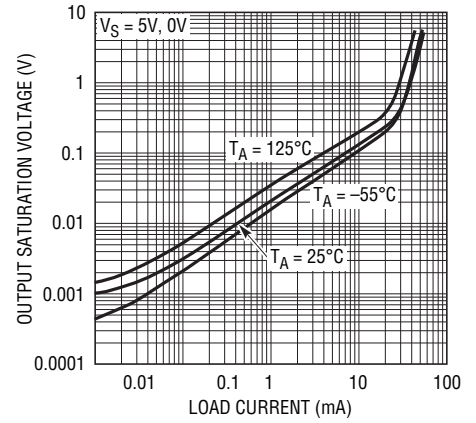
**Input Bias Current  
vs Common Mode Voltage**



**Input Bias Current vs Temperature**



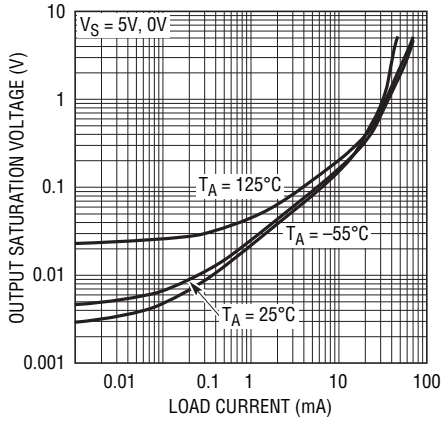
**Output Saturation Voltage  
vs Load Current (Output Low)**



# TYPICAL PERFORMANCE CHARACTERISTICS

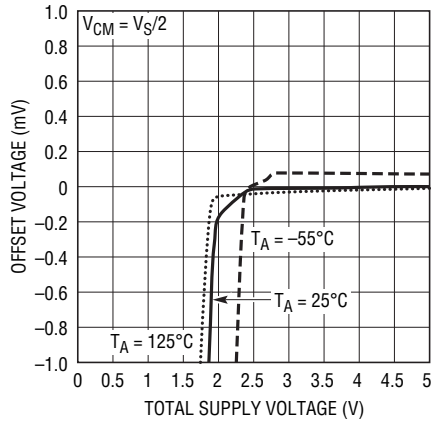
(LT6233/LT6234/LT6235)

**Output Saturation Voltage vs Load Current (Output High)**



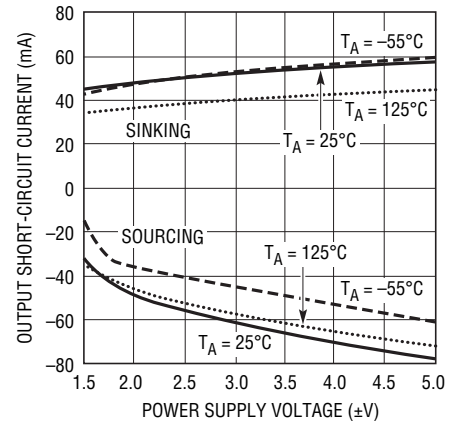
623345 G07

**Minimum Supply Voltage**



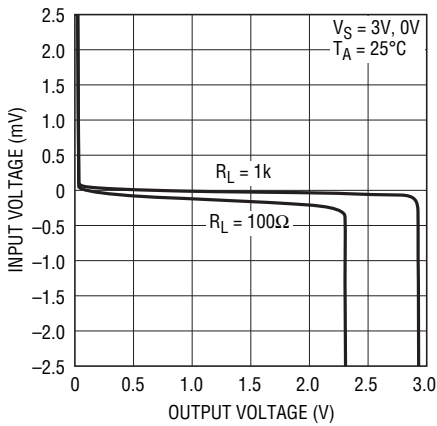
623345 G08

**Output Short-Circuit Current vs Power Supply Voltage**



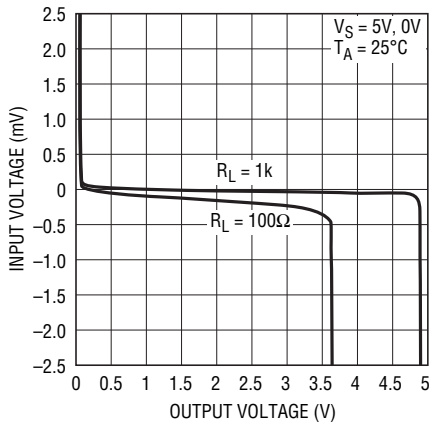
623345 G09

**Open-Loop Gain**



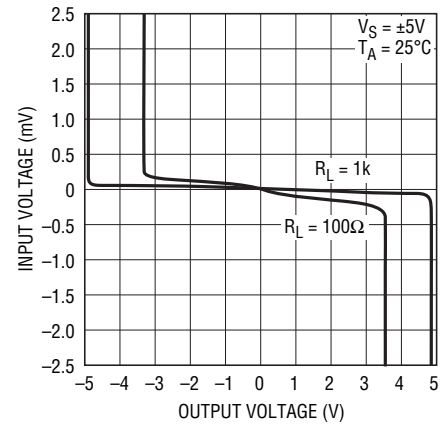
623345 G10

**Open-Loop Gain**



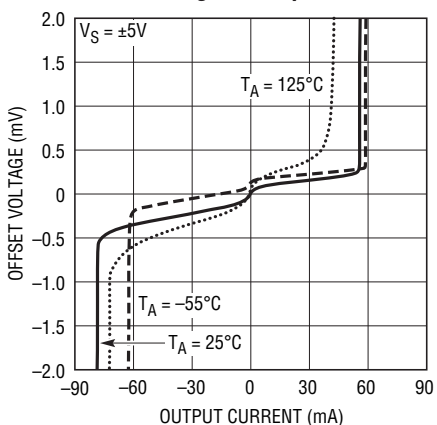
623345 G11

**Open-Loop Gain**



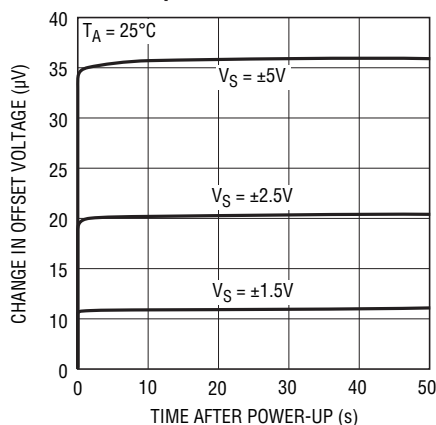
623345 G12

**Offset Voltage vs Output Current**



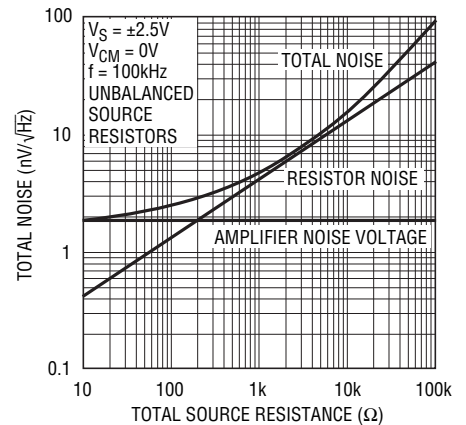
623345 G13

**Warm-Up Drift vs Time**



623345 G14

**Total Noise vs Total Source Resistance**

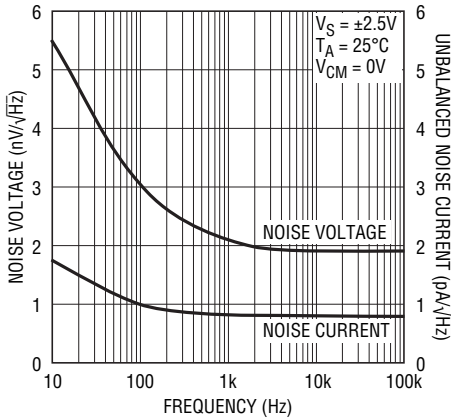


623345 G15

# LT6233/LT6233-10 LT6234/LT6235

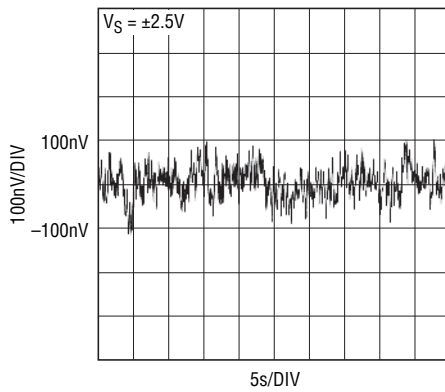
## TYPICAL PERFORMANCE CHARACTERISTICS (LT6233/LT6234/LT6235)

**Noise Voltage and Unbalanced Noise Current vs Frequency**



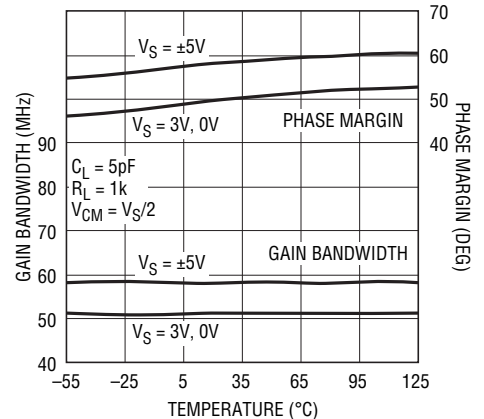
623345 G16

**0.1Hz to 10Hz Output Voltage Noise**



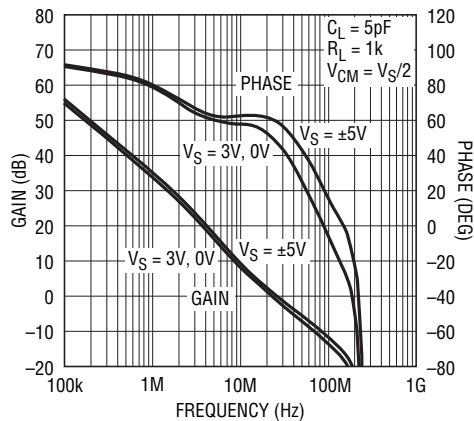
623345 G17

**Gain Bandwidth and Phase Margin vs Temperature**



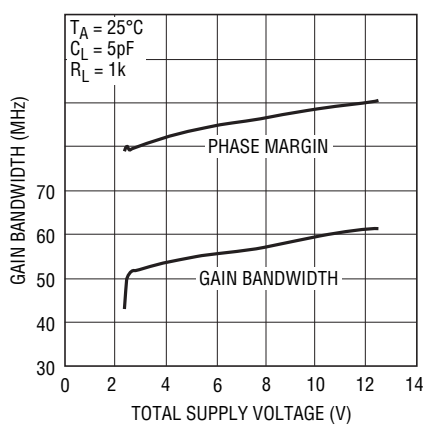
623345 G18

**Open-Loop Gain vs Frequency**



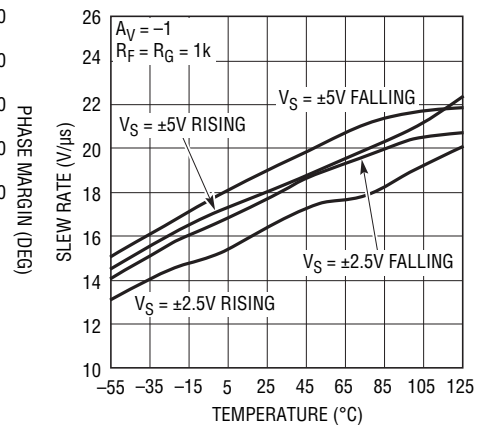
623345 G19

**Gain Bandwidth and Phase Margin vs Supply Voltage**



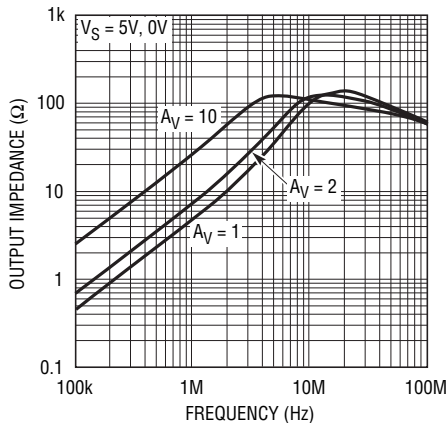
623345 G20

**Slew Rate vs Temperature**



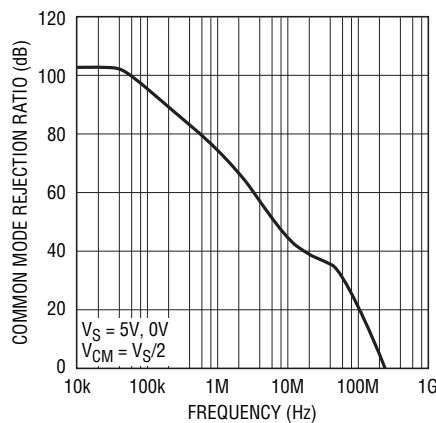
623345 G21

**Output Impedance vs Frequency**



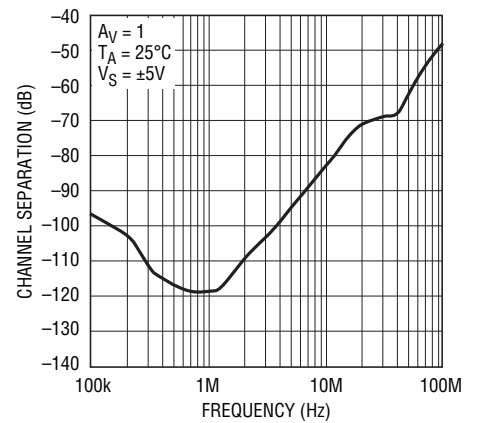
623345 G22

**Common Mode Rejection Ratio vs Frequency**



623345 G23

**Channel Separation vs Frequency**



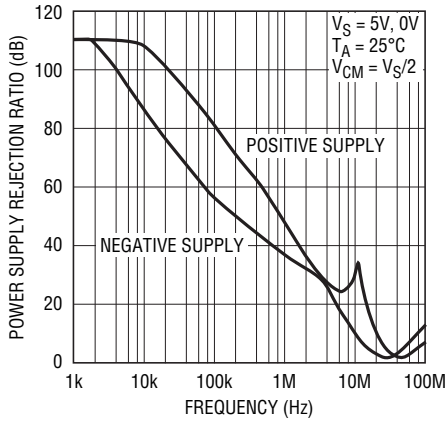
623345 G24

623345fc

# TYPICAL PERFORMANCE CHARACTERISTICS

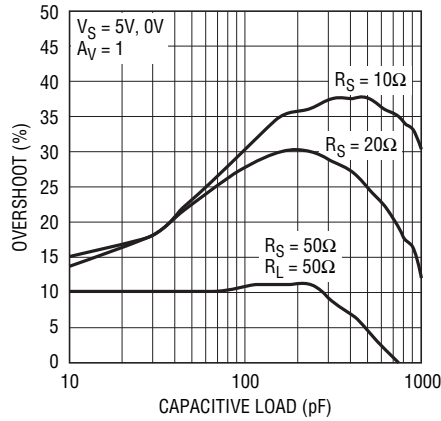
(LT6233/LT6234/LT6235)

**Power Supply Rejection Ratio vs Frequency**



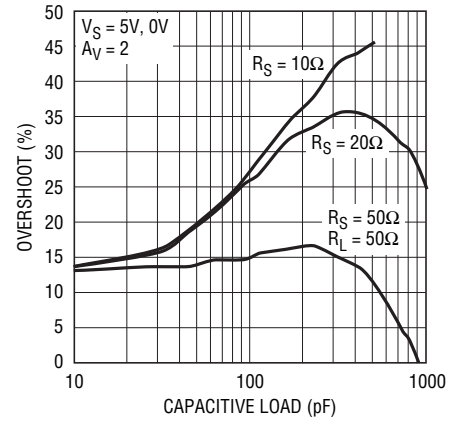
623345 G25

**Series Output Resistance and Overshoot vs Capacitive Load**



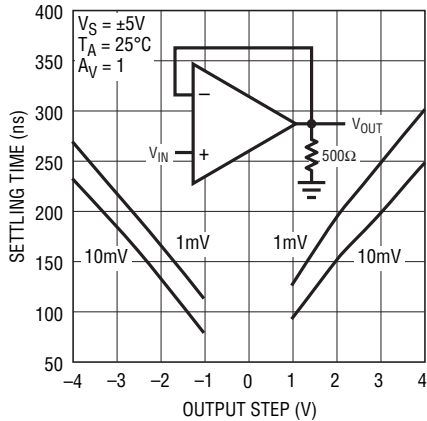
623345 G26

**Series Output Resistance and Overshoot vs Capacitive Load**



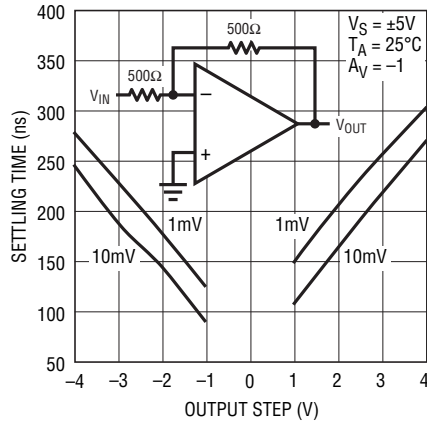
623345 G27

**Settling Time vs Output Step (Noninverting)**



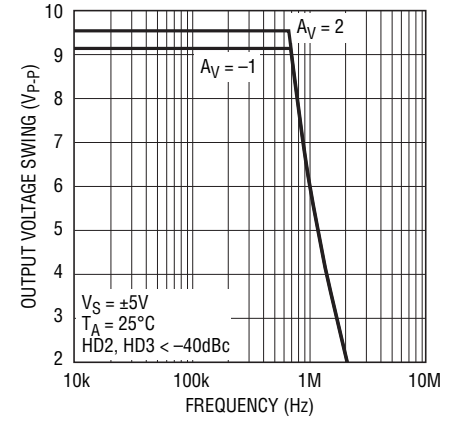
623345 G28

**Settling Time vs Output Step (Inverting)**



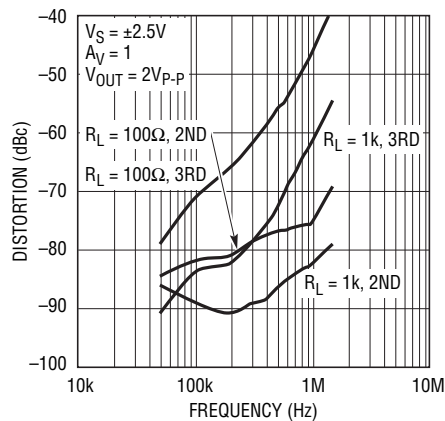
623345 G29

**Maximum Undistorted Output Signal vs Frequency**



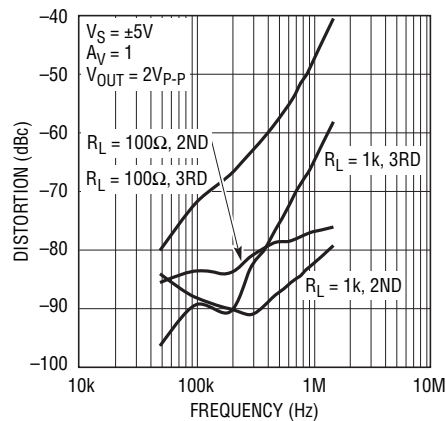
623345 G30

**Distortion vs Frequency**



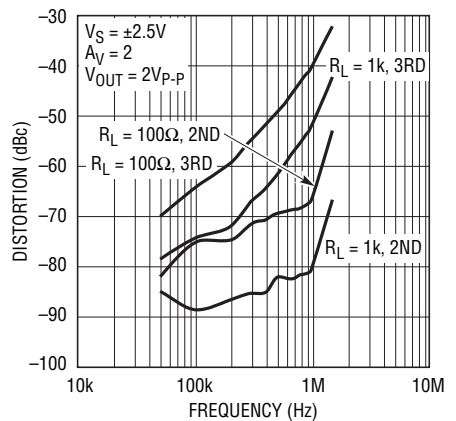
623345 G31

**Distortion vs Frequency**



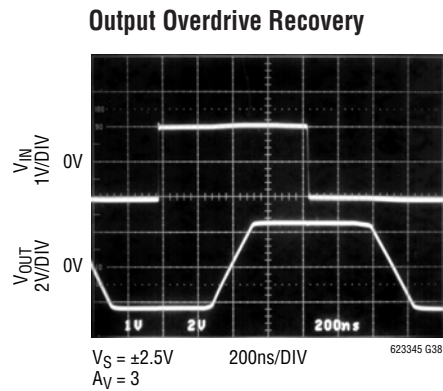
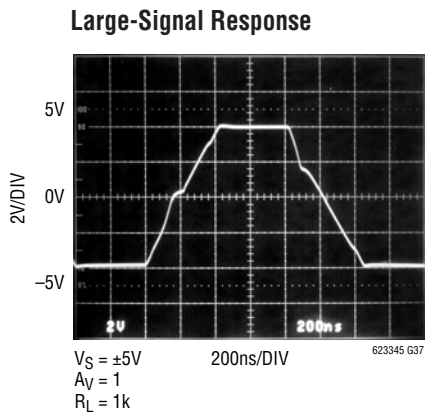
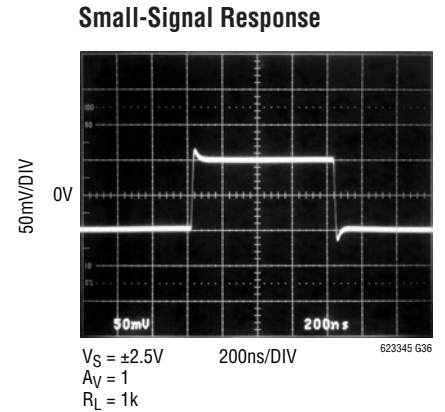
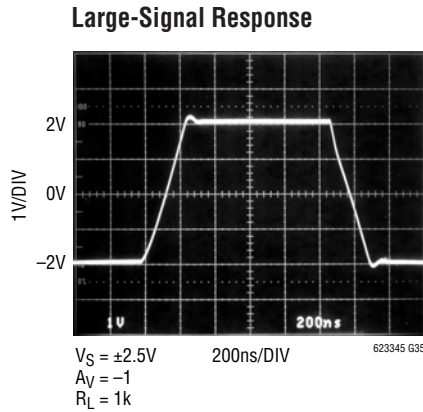
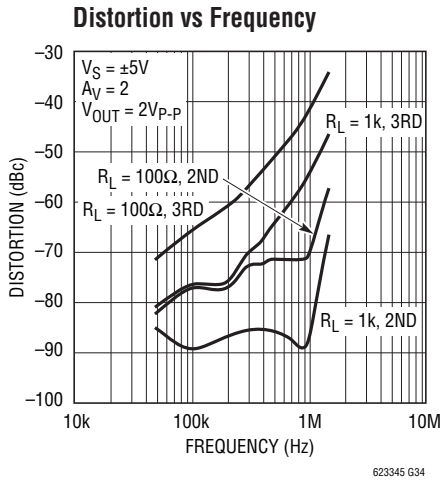
623345 G32

**Distortion vs Frequency**

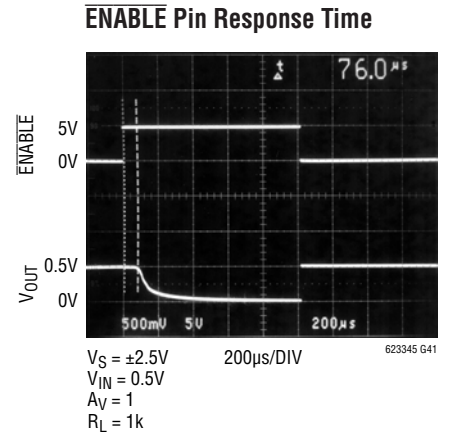
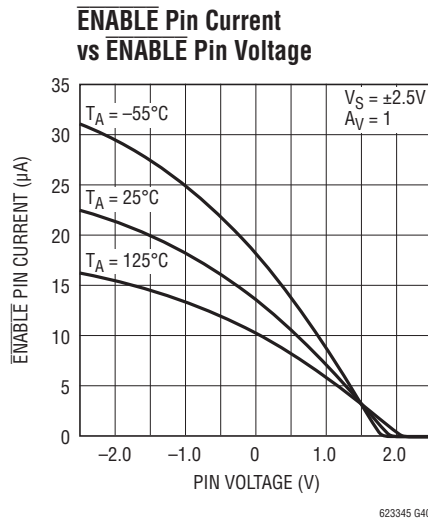
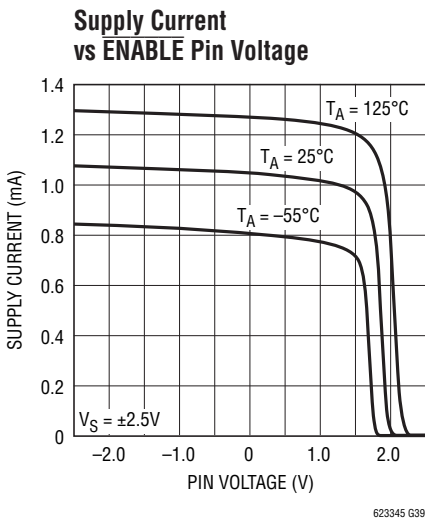


623345 G33

**TYPICAL PERFORMANCE CHARACTERISTICS**  
(LT6233/LT6234/LT6235)



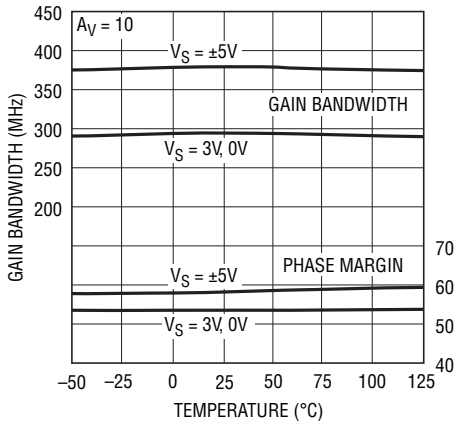
**(LT6233) ENABLE Characteristics**



# TYPICAL PERFORMANCE CHARACTERISTICS

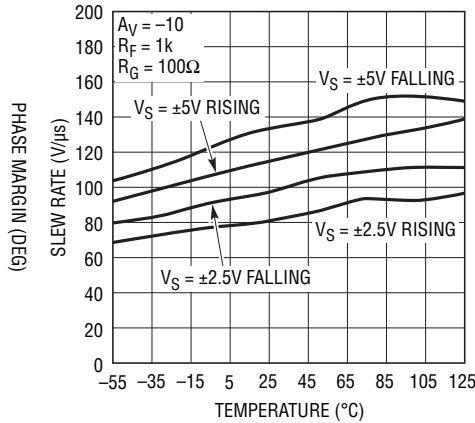
(LT6233-10)

**Gain Bandwidth and Phase Margin vs Temperature**



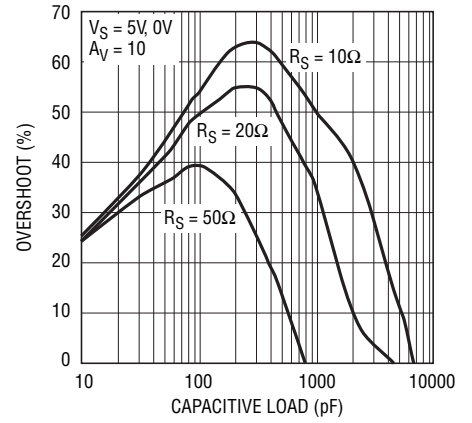
623345 G42

**Slew Rate vs Temperature**



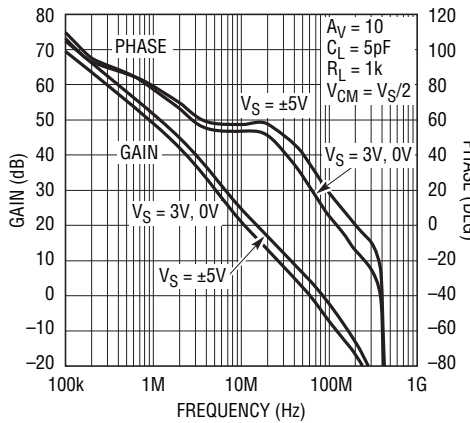
623345 G43

**Series Output Resistor and Overshoot vs Capacitive Load**



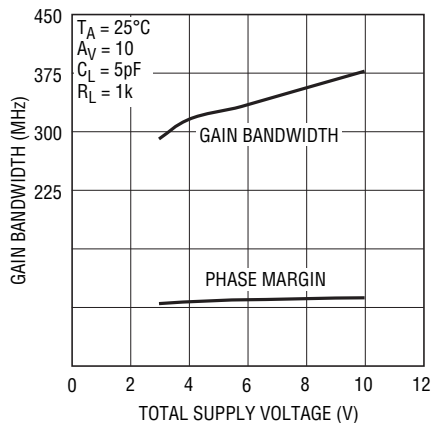
623345 G44

**Open-Loop Gain and Phase vs Frequency**



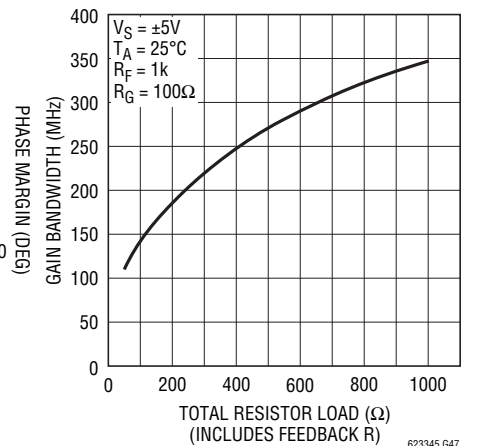
623345 G45

**Gain Bandwidth and Phase Margin vs Supply Voltage**



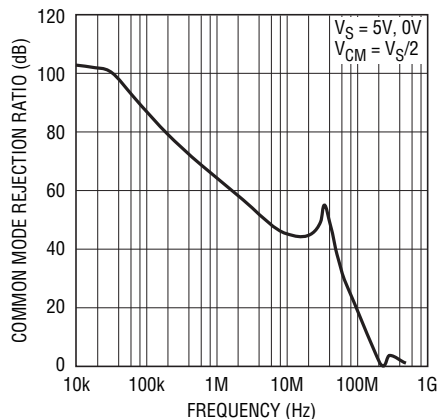
623345 G46

**Gain Bandwidth vs Resistor Load**



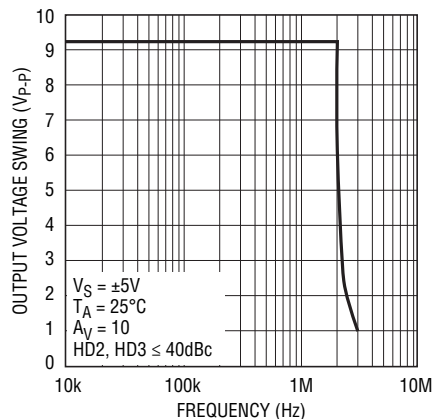
623345 G47

**Common Mode Rejection Ratio vs Frequency**



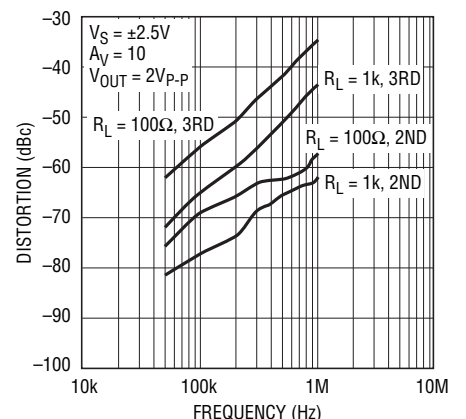
623345 G48

**Maximum Undistorted Output vs Frequency**



623345 G49

**2nd and 3rd Harmonic Distortion vs Frequency**

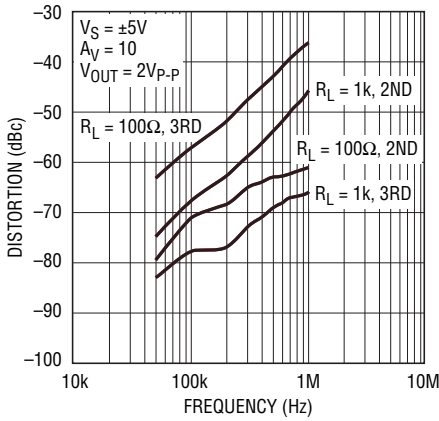


623345 G50  
623345fC

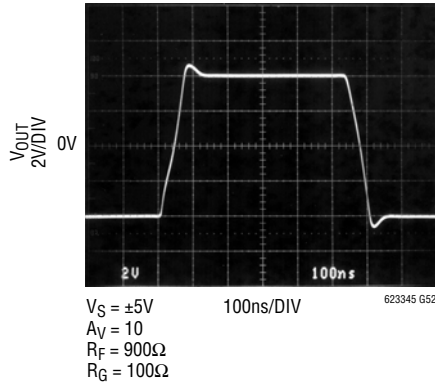
# TYPICAL PERFORMANCE CHARACTERISTICS

(LT6233-10)

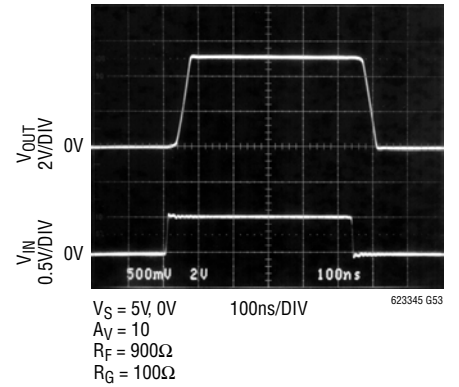
**2nd and 3rd Harmonic Distortion vs Frequency**



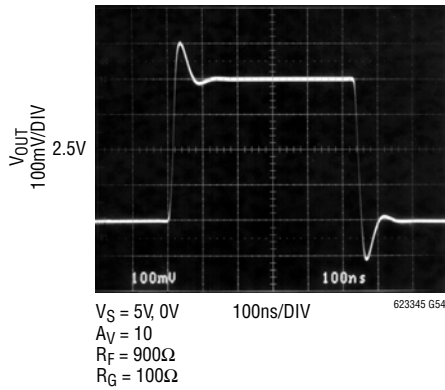
**Large-Signal Response**



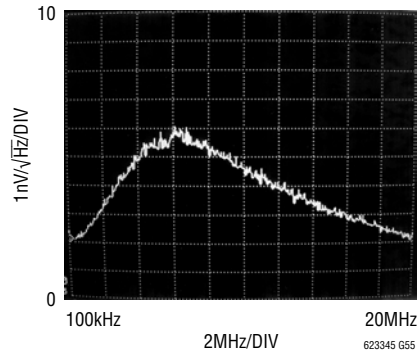
**Output-Overload Recovery**



**Small-Signal Response**



**Input Referred High Frequency Noise Spectrum**





## APPLICATIONS INFORMATION

### Amplifier Characteristics

Figure 1 is a simplified schematic of the LT6233/LT6234/LT6235, which has a pair of low noise input transistors Q1 and Q2. A simple current mirror Q3/Q4 converts the differential signal to a single-ended output, and these transistors are degenerated to reduce their contribution to the overall noise.

Capacitor C1 reduces the unity-cross frequency and improves the frequency stability without degrading the gain bandwidth of the amplifier. Capacitor C<sub>M</sub> sets the overall amplifier gain bandwidth. The differential drive generator supplies current to transistors Q5 and Q6 that swing the output from rail-to-rail.

### Input Protection

There are back-to-back diodes, D1 and D2 across the + and – inputs of these amplifiers to limit the differential input voltage to  $\pm 0.7V$ . The inputs of the LT6233/LT6234/LT6235 do not have internal resistors in series with the input transistors. This technique is often used to protect the input devices from overvoltage that causes excessive current to flow. The addition of these resistors would significantly degrade the low noise voltage of these amplifiers. For instance, a 100 $\Omega$  resistor in series with each input would generate 1.8nV/ $\sqrt{Hz}$  of noise, and the total amplifier noise voltage would rise from 1.9nV/ $\sqrt{Hz}$  to 2.6nV/ $\sqrt{Hz}$ . Once the input differential voltage exceeds  $\pm 0.7V$ , steady-state current conducted through the protection diodes should

be limited to  $\pm 40mA$ . This implies 25 $\Omega$  of protection resistance is necessary per volt of overdrive beyond  $\pm 0.7V$ . These input diodes are rugged enough to handle transient currents due to amplifier slew rate overdrive and clipping without protection resistors.

The photo of Figure 2 shows the output response to an input overdrive with the amplifier connected as a voltage follower. With the input signal low, current source I<sub>1</sub> saturates and the differential drive generator drives Q6 into saturation so the output voltage swings all the way to V<sup>-</sup>. The input can swing positive until transistor Q2 saturates into current mirror Q3/Q4. When saturation occurs, the output tries to phase invert, but diode D2 conducts current from the signal source to the output through the feedback connection. The output is clamped a diode drop below the input. In this photo, the input signal generator is limiting at about 20mA.

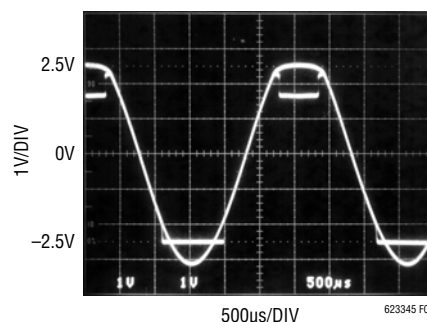


Figure 2. V<sub>S</sub> =  $\pm 2.5V$ , A<sub>V</sub> = 1 with Large Overdrive

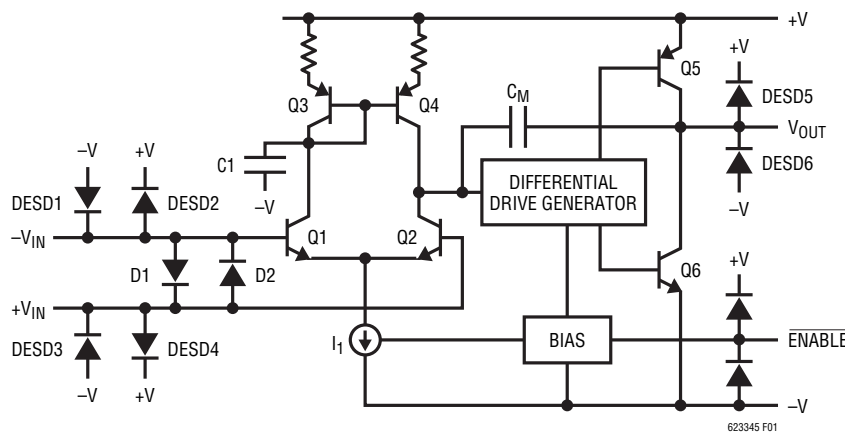


Figure 1. Simplified Schematic

## APPLICATIONS INFORMATION

With the amplifier connected in a gain of  $A_V \geq 2$ , the output can invert with very heavy overdrive. To avoid this inversion, limit the input overdrive to 0.5V beyond the power supply rails.

### ESD

The LT6233/LT6234/LT6235 have reverse-biased ESD protection diodes on all inputs and outputs as shown in Figure 1. If these pins are forced beyond either supply, unlimited current will flow through these diodes. If the current is transient and limited to one hundred milliamps or less, no damage to the device will occur.

### Noise

The noise voltage of the LT6233/LT6234/LT6235 is equivalent to that of a 225Ω resistor, and for the lowest possible noise it is desirable to keep the source and feedback resistance at or below this value, i.e.,  $R_S + R_G || R_{FB} \leq 225\Omega$ . With  $R_S + R_G || R_{FB} = 225\Omega$  the total noise of the amplifier is:

$$e_N = \sqrt{(1.9\text{nV})^2 + (1.9\text{nV})^2} = 2.69\text{nV}/\sqrt{\text{Hz}}$$

Below this resistance value, the amplifier dominates the noise, but in the region between 225Ω and about 30k, the noise is dominated by the resistor thermal noise. As the total resistance is further increased beyond 30k, the amplifier noise current multiplied by the total resistance eventually dominates the noise.

The product of  $e_N \cdot \sqrt{I_{\text{SUPPLY}}}$  is an interesting way to gauge low noise amplifiers. Most low noise amplifiers with low  $e_N$  have high  $I_{\text{SUPPLY}}$  current. In applications that require low noise voltage with the lowest possible supply current, this product can prove to be enlightening. The LT6233/LT6234/LT6235 have an  $e_N \cdot \sqrt{I_{\text{SUPPLY}}}$  product of only 2.1 per amplifier, yet it is common to see amplifiers with similar noise specifications to have  $e_N \cdot \sqrt{I_{\text{SUPPLY}}}$  as high as 13.5.

For a complete discussion of amplifier noise, see the LT1028 data sheet.

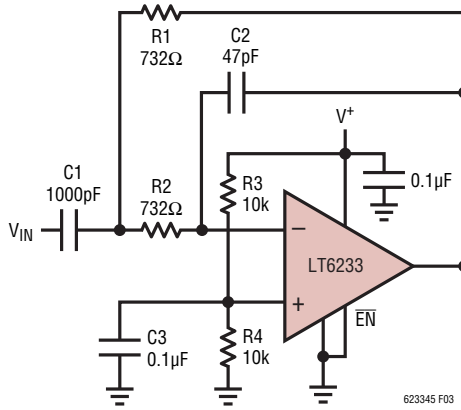
### Enable Pin

The LT6233 and LT6233-10 include an  $\overline{\text{ENABLE}}$  pin that shuts down the amplifier to 10μA maximum supply current. The  $\overline{\text{ENABLE}}$  pin must be driven low to operate the amplifier with normal supply current. The  $\overline{\text{ENABLE}}$  pin must be driven high to within 0.35V of  $V^+$  to shut down the supply current. This can be accomplished with simple gate logic; however care must be taken if the logic and the LT6233 operate from different supplies. If this is the case, then open-drain logic can be used with a pull-up resistor to ensure that the amplifier remains off. See Typical Performance Characteristics.

The output leakage current when disabled is very low; however, current can flow into the input protection diodes D1 and D2 if the output voltage exceeds the input voltage by a diode drop.

## TYPICAL APPLICATIONS

### Single Supply, Low Noise, Low Power, Bandpass Filter with Gain = 10



$$f_0 = \frac{1}{2\pi RC} = 1\text{MHz}$$

$$C = \sqrt{C1 \cdot C2} \quad R = R1 = R2$$

$$f_0 = \left(\frac{732\Omega}{R}\right)\text{MHz, MAXIMUM } f_0 = 1\text{MHz}$$

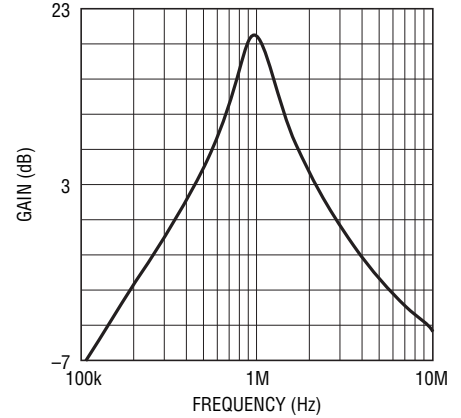
$$f_{-3dB} = \frac{f_0}{2.5}$$

$$A_V = 20\text{dB at } f_0$$

$$E_N = 6\mu\text{VRMS INPUT REFERRED}$$

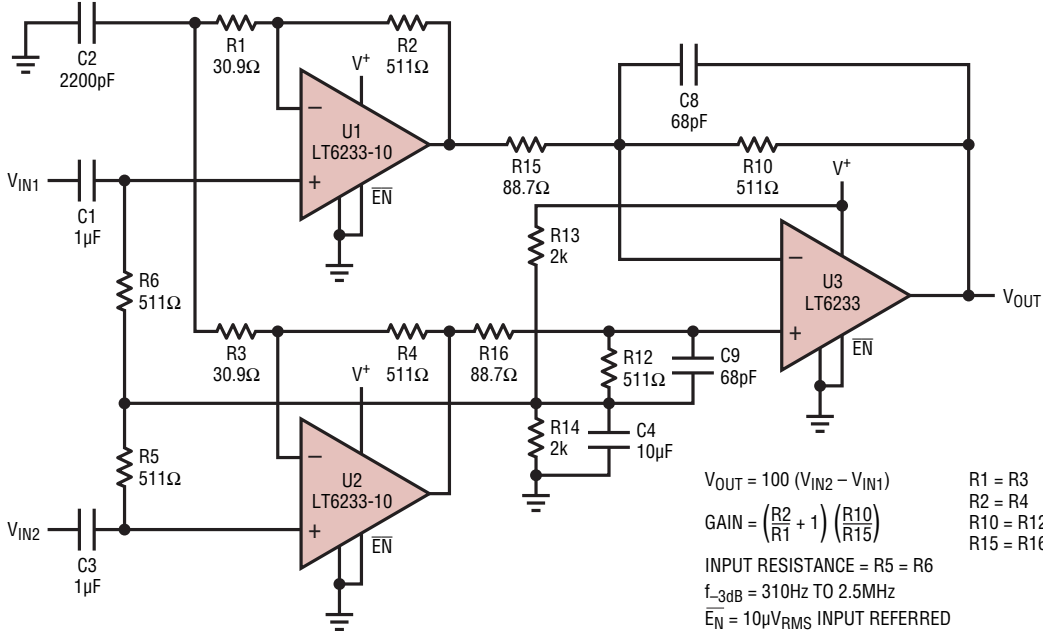
$$I_S = 1.5\text{mA FOR } V^+ = 5\text{V}$$

Frequency Response Plot of Bandpass Filter



623345 F04

### Low Power, Low Noise, Single Supply, Instrumentation Amplifier with Gain = 100



$$V_{OUT} = 100 (V_{IN2} - V_{IN1})$$

$$\text{GAIN} = \left(\frac{R2}{R1} + 1\right) \left(\frac{R10}{R15}\right)$$

$$\text{INPUT RESISTANCE} = R5 = R6$$

$$f_{-3dB} = 310\text{Hz TO } 2.5\text{MHz}$$

$$E_N = 10\mu\text{VRMS INPUT REFERRED}$$

$$I_S = 4.7\text{mA FOR } V_S = 5\text{V, } 0\text{V}$$

$$R1 = R3$$

$$R2 = R4$$

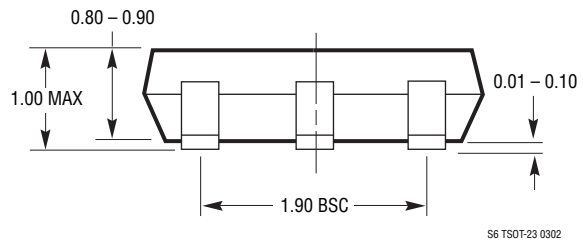
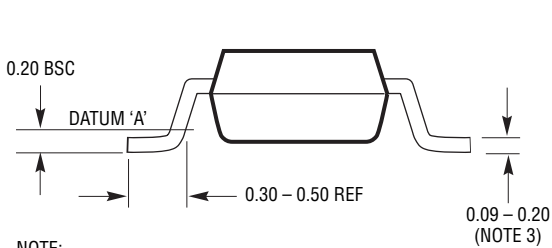
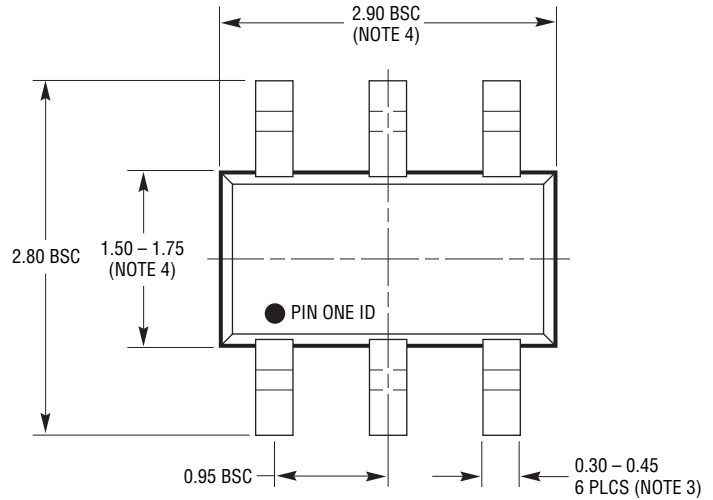
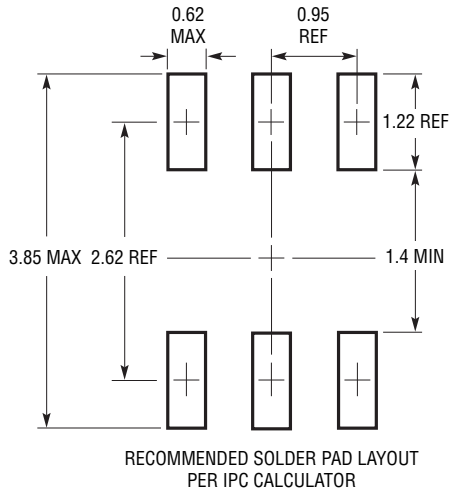
$$R10 = R12$$

$$R15 = R16$$

623345 F05

**PACKAGE DESCRIPTION**

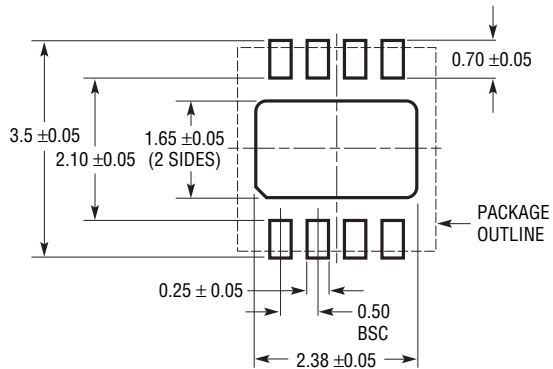
**S6 Package**  
**6-Lead Plastic TSOT-23**  
 (Reference LTC DWG # 05-08-1636)



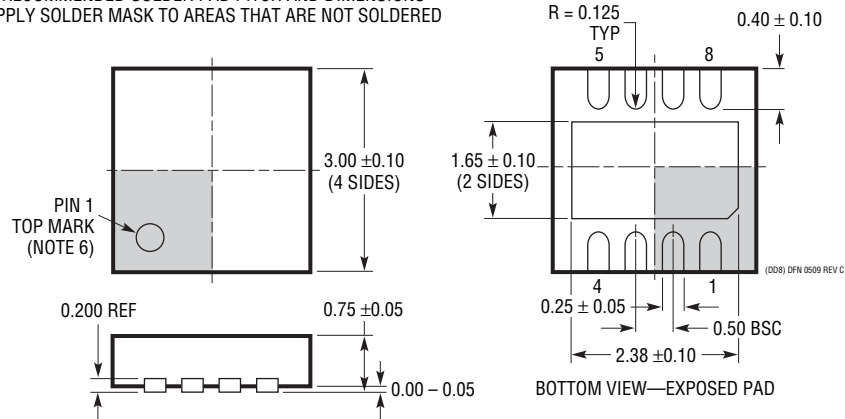
- NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
  2. DRAWING NOT TO SCALE
  3. DIMENSIONS ARE INCLUSIVE OF PLATING
  4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
  5. MOLD FLASH SHALL NOT EXCEED 0.254mm
  6. JEDEC PACKAGE REFERENCE IS MO-193

## PACKAGE DESCRIPTION

**DD Package**  
**8-Lead Plastic DFN (3mm × 3mm)**  
 (Reference LTC DWG # 05-08-1698 Rev C)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS  
 APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED

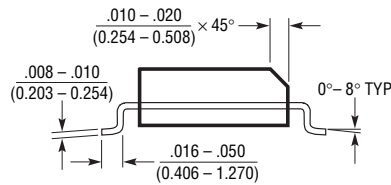
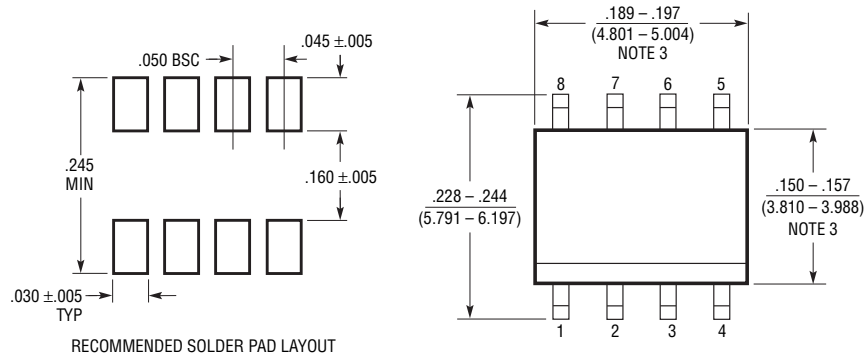


**NOTE:**

1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-1)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON TOP AND BOTTOM OF PACKAGE

## PACKAGE DESCRIPTION

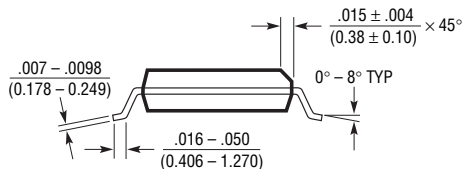
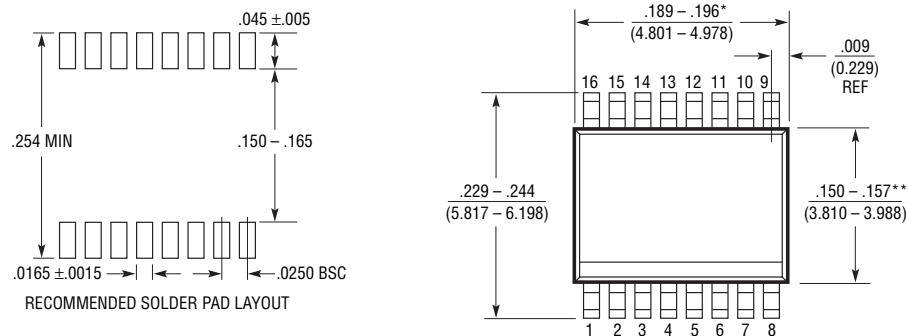
### S8 Package 8-Lead Plastic Small Outline (Narrow .150 Inch) (Reference LTC DWG # 05-08-1610)



- NOTE:  
 1. DIMENSIONS IN  $\frac{\text{INCHES}}{\text{MILLIMETERS}}$   
 2. DRAWING NOT TO SCALE  
 3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.  
 MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

S08 0203

### GN Package 16-Lead Plastic SSOP (Narrow .150 Inch) (Reference LTC DWG # 05-08-1641)



- NOTE:  
 1. CONTROLLING DIMENSION: INCHES  
 2. DIMENSIONS ARE IN  $\frac{\text{INCHES}}{\text{MILLIMETERS}}$   
 3. DRAWING NOT TO SCALE  
 \*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE  
 \*\*DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

GN16 (SSOP) 0204

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## REVISION HISTORY (Revision history begins at Rev C)

REV	DATE	DESCRIPTION	PAGE NUMBER
C	1/11	Revised y-axis label on curve G40 in Typical Performance Characteristics	14
		Updated ENABLE Pin section in Applications Information	18