ANALOG DEVICES

25μV, 0.3μV/°C, Low Noise Instrumentation Amplifier

FEATURES

- **Single Gain Set Resistor: G = 1 to >1000**
- **Excellent DC Precision**
  - **Input Offset Voltage: 25μV Max**
  - **Input Offset Voltage Drift: 0.3μV/°C Max**
  - **Low Gain Error: 0.01% Max (G = 1)**
  - **Low Gain Drift: 30ppm/°C Max (G > 1)**
  - **High DC CMRR: 94dB Min (G = 1)**
- Input Bias Current: 400pA Max
- 3.1MHz –3dB Bandwidth (G = 1)
- Low Noise:
  - 0.1Hz to 10Hz Noise: $0.2\mu V_{P-P}$
  - 1kHz Voltage Noise: $7nV/\sqrt{Hz}$
- Integrated Input RFI Filter
- Wide Supply Range 4.75V to 35V
- Specified Temperature Ranges: –40°C to 85°C, –40°C to 125°C
- MS8, S8E and 10-pin 3mm × 3mm DFN Packages

APPLICATIONS

- Bridge Amplifier
- Data Acquisition
- Multiplexed Signals
- Thermocouple Amplifier
- Strain Gauge Amplifier
- Medical Instrumentation
- Transducer Interfaces
- Differential to Single-Ended Conversion

DESCRIPTION

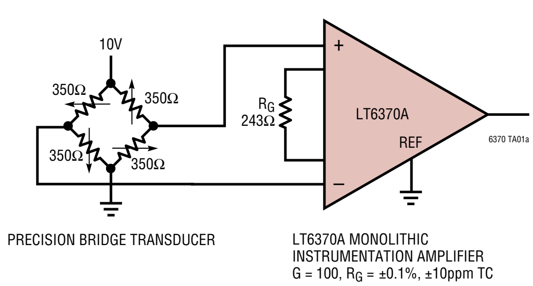
The LT®6370 is a gain programmable, high precision instrumentation amplifier that delivers industry leading DC precision. This high precision enables smaller signals to be sensed and eases calibration requirements, particularly over temperature.

The LT6370 uses a proprietary high performance bipolar process which enables industry leading accuracy coupled with exceptional long-term stability. The LT6370 is laser trimmed for very low input offset voltage (25μV) and high CMRR (94dB, G = 1). Proprietary on-chip test capability allows the input offset voltage drift (0.3μV/°C) and gain drift (30ppm/°C) to be guaranteed with automated testing on the S8E package.

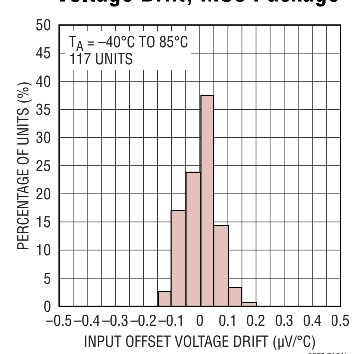
In addition to excellent DC specifications, the LT6370's wide bandwidth (3.1MHz, G = 1) and fast settling time allow it to operate well in multiplexed applications. EMI filtering is integrated on the LT6370's inputs to maintain accuracy in the presence of harsh RF interference.

The LT6370 is available in a compact 8-pin MSOP or S8E which use the conventional instrumentation amplifier pin-out as well as a 10-pin 3mm × 3mm DFN. The S8E package is also offered as an A grade which has superior DC specifications. The LT6370 is fully specified over the –40°C to 85°C and –40°C to 125°C temperature ranges.

TYPICAL APPLICATION



Distribution of Input Offset Voltage Drift, MS8 Package



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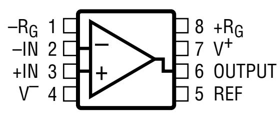
ABSOLUTE MAXIMUM RATINGS

(Note 1)

Total Supply Voltage (V^+ to V^-)................................36V
Input Voltage (+IN, –IN, +R_G, –R_G, REF).................. (V^- – 0.3V) to (V^+ + 0.3V)
Differential Input Voltage (+IN to –IN).....................±36V
Input Current (+R_G, –R_G) ....±2mA
Input Current (+IN, –IN) .... ±10mA
Input Current (REF) ....–10mA
Output Short-Circuit Duration.............Thermally Limited
Output Current...80mA
Operating and Specified Temperature Range
I-Grade...–40°C to 85°C
H-Grade ....–40°C to 125°C
Maximum Junction Temperature .... 150°C
Storage Temperature Range ....–65°C to 150°C
Lead Temperature (Soldering, 10 sec)...................300°C

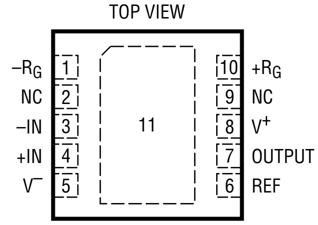
PIN CONFIGURATION

TOP VIEW



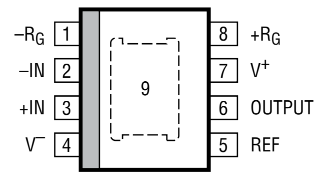
MS8 PACKAGE
8-LEAD MS
θ_{JA} = 163°C/W, θ_{JC} = 40°C/W

TOP VIEW



DD PACKAGE
10-LEAD (3mm × 3mm) PLASTIC DFN
θ_{JA} = 43°C/W, θ_{JC} = 5.5°C/W
EXPOSED PAD (PIN 11) IS CONNECTED TO V^- (PIN 5)
(PCB CONNECTION OPTIONAL)

TOP VIEW



S8E PACKAGE
8-LEAD PLASTIC SOIC
θ_{JA} = 33°C/W, θ_{JC} = 5°C/W
EXPOSED PAD (PIN 9) MUST FLOAT
OR BE CONNECTED TO V^+ IN ADDITION TO PIN 7

ORDER INFORMATION

TUBE	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT6370IS8E#PBF	LT6370IS8E#TRPBF	6370	8-Lead Plastic SO	–40°C to 85°C
LT6370HS8E#PBF	LT6370HS8E#TRPBF	6370	8-Lead Plastic SO	–40°C to 125°C
LT6370IMS8#PBF	LT6370IMS8#TRPBF	LTGZP	8-Lead Plastic MSOP	–40°C to 85°C
LT6370HMS8#PBF	LT6370HMS8#TRPBF	LTGZP	8-Lead Plastic MSOP	–40°C to 125°C
LT6370IDD#PBF	LT6370IDD#TRPBF	LGZN	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C
LT6370HDD#PBF	LT6370HDD#TRPBF	LGZN	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LT6370AIS8E#PBF	LT6370AIS8E#TRPBF	6370	8-Lead Plastic SO	–40°C to 85°C
LT6370AHS8E#PBF	LT6370AHS8E#TRPBF	6370	8-Lead Plastic SO	–40°C to 125°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

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ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified temperature range, otherwise specifications are at T_A = 25°C. V_S = ±15V, V_{CM} = V_{REF} = 0V, R_L = 2kΩ.

SYMBOL	PARAMETER	CONDITIONS		LT6370A MIN	LT6370A TYP	LT6370A MAX	LT6370 MIN	LT6370 TYP	LT6370 MAX	UNITS
G	Gain Range	G = (1 + 24.2k/R_G) (Note 2)		1		1000	1		1000	V/V
	Gain Error (Notes 3, 4)	G = 1			–0.004	0.01		–0.004	0.015	%
		G = 1	●			0.02			0.025	%
		G = 10			–0.02	0.08		–0.02	0.1	%
		G = 10, T_A = –40°C to 85°C	●			0.4			0.42	%
		G = 10, T_A = –40°C to 125°C	●			0.58			0.6	%
		G = 100			–0.02	0.08		–0.02	0.1	%
		G = 100, T_A = –40°C to 85°C	●			0.4			0.42	%
		G = 100, T_A = –40°C to 125°C	●			0.58			0.6	%
		G = 1000			–0.05	0.15		–0.05	0.2	%
		G = 1000, T_A = –40°C to 85°C	●			0.47			0.52	%
		G = 1000, T_A = –40°C to 125°C	●			0.65			0.7	%
	Gain vs Temperature (Notes 3, 4)	G = 1 (Note 5)	●		0.2	0.5		0.2	0.5	ppm/°C
		G > 1(Note 6)	●		20	30		20	50	ppm/°C
	Gain Nonlinearity (Notes 3, 7)	V_{OUT} = ±10V, G = 1			1	3		1	5	ppm
		V_{OUT} = ±10V, G = 1	●			6			8	ppm
		V_{OUT} = ±10V, G = 10			3	20		3	30	ppm
		V_{OUT} = ±10V, G = 10	●			65			75	ppm
		V_{OUT} = ±10V, G = 100			20	30		20	55	ppm
		V_{OUT} = ±10V, G = 100	●			105			130	ppm
		V_{OUT} = ±10V, G = 1000			50	200		50	300	ppm
		V_{OUT} = ±10V, G = 1000	●			270			370	ppm
		V_{OUT} = ±10V, G = 1, R_L = 600Ω			4			4		ppm
		V_{OUT} = ±10V, G = 10, R_L = 600Ω			6			6		ppm
		V_{OUT} = ±10V, G = 100, R_L = 600Ω			30			30		ppm
		V_{OUT} = ±10V, G = 1000, R_L = 600Ω			250			250		ppm
V_{OST}, Total Input Referred Offset Voltage, V_{OST} = V_{OSI} + V_{OSO}/G										
V_{OSI}	Input Offset Voltage (Note 8)	S8E Package			±9	±25		±15	±55	µV
		MS8 Package						±8	±35	µV
		DD10 Package						±15	±60	µV
		S8E Package, T_A = –40°C to 85°C	●			±100			±130	µV
		S8E Package, T_A = –40°C to 125°C	●			±125			±155	µV
		MS8 Package, T_A = –40°C to 85°C	●						±125	µV
		MS8 Package, T_A = –40°C to 125°C	●						±150	µV
		DD10 Package, T_A = –40°C to 85°C	●						±155	µV
		DD10 Package, T_A = –40°C to 125°C	●						±180	µV
V_{OSO}	Output Offset Voltage (Note 8)	S8E Package			±60	±165		±70	±265	µV
		MS8 Package						±30	±150	µV
		DD10 Package						±45	±250	µV
		S8E Package, T_A = –40°C to 85°C	●			±390			±490	µV
		S8E Package, T_A = –40°C to 125°C	●			±515			±615	µV
		MS8 Package, T_A = –40°C to 85°C	●						±325	µV
		MS8 Package, T_A = –40°C to 125°C	●						±400	µV
		DD10 Package, T_A = –40°C to 85°C	●						±510	µV
		DD10 Package, T_A = –40°C to 125°C	●						±650	µV
V_{OSI}/T	Input Offset Voltage Drift (Notes 5, 8)	S8E Package, T_A = –40°C to 85°C	●			±0.3			±0.4	µV/°C
		S8E Package, T_A = –40°C to 125°C	●			±0.4			±0.5	µV/°C
		MS8 Package, T_A = –40°C to 85°C	●						±0.3	µV/°C
		MS8 Package, T_A = –40°C to 125°C	●						±0.4	µV/°C
		DD10 Package, T_A = –40°C to 85°C	●						±0.4	µV/°C
		DD10 Package, T_A = –40°C to 125°C	●						±0.5	µV/°C
	Input Offset Voltage Hysteresis (Note 9)	T_A = –40°C to 85°C	●		±1.5			±1.5		µV
		T_A = –40°C to 125°C	●		±3			±3		µV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified temperature range, otherwise specifications are at $T_A = 25°C$. $V_S = ±15V$, $V_{CM} = V_{REF} = 0V$, $R_L = 2kΩ$.

SYMBOL	PARAMETER	CONDITIONS		LT6370A MIN	LT6370A TYP	LT6370A MAX	LT6370 MIN	LT6370 TYP	LT6370 MAX	UNITS
V_{OSO}/T	Output Offset Voltage Drift (Notes 5, 8)	S8E Package, T_A = –40°C to 85°C	●			±1.5			±2.5	µV/°C
		S8E Package, T_A = –40°C to 125°C	●			±1.5			±3.5	µV/°C
		MS8 Package, T_A = –40°C to 85°C	●						±2	µV/°C
		MS8 Package, T_A = –40°C to 125°C	●						±2.5	µV/°C
		DD10 Package, T_A = –40°C to 85°C	●						±3	µV/°C
		DD10 Package, T_A = –40°C to 125°C	●						±4	µV/°C
	Output Offset Voltage Hysteresis (Note 9)	T_A = –40°C to 85°C	●		±10			±10		µV
		T_A = –40°C to 125°C	●		±20			±20		µV
I_B	Input Bias Current	MS8 and S8E Packages			±0.1	±0.4		±0.1	±0.6	nA
		DD10 Package						±0.1	±0.8	nA
		T_A = –40°C to 85°C, MS8 and S8E Packages	●			±1.3			±1.5	nA
		T_A = –40°C to 85°C, DD10 Package	●						±1.7	nA
		T_A = –40°C to 125°C, MS8 and S8E Packages	●			±2.8			±3	nA
		T_A = –40°C to 125°C, DD10 Package	●						±3.2	nA
I_{OS}	Input Offset Current	MS8 and S8E Packages			±0.2	±0.7		±0.2	±1	nA
		DD10 Package						±0.2	±1.4	nA
		MS8 and S8E Packages	●			±1.7			±2	nA
		DD10 Package	●						±2.4	nA
	Input Noise Voltage (Note 10)	0.1Hz to 10Hz, G = 1			2			2		$µV_{P-P}$
		0.1Hz to 10Hz, G = 1000			0.2			0.2		$µV_{P-P}$
Total RTI Noise = $\sqrt{e_{ni}^2 + (e_{no}/G)^2}$ (Note 10)										
e_{ni}	Input Noise Voltage Density	f = 1kHz			7			7		$nV/\sqrt{Hz}$
e_{no}	Output Noise Voltage Density	f = 1kHz			65			65		$nV/\sqrt{Hz}$
	Input Noise Current	0.1Hz to 10Hz			10			10		pA_{P-P}
i_n	Input Noise Current Density	f = 1kHz			200			200		$fA/\sqrt{Hz}$
R_{IN}	Input Resistance	V_{IN} = –12.6V to 13V			225			225		GΩ
C_{IN}	Differential	f = 100kHz			0.9			0.9		pF
	Common Mode	f = 100kHz			15.9			15.9		pF
V_{CM}	Input Voltage Range	Guaranteed by CMRR			$V^- + 1.8$/ $V^+ - 1.4$			$V^- + 1.8$/ $V^+ - 1.4$		V
			●	$V^- + 2.4$		$V^+ - 2$	$V^- + 2.4$		$V^+ - 2$	V
CMRR	Common Mode Rejection Ratio	DC to 60Hz, 1k Source Imbalance, V_{CM} = –12.6V to 13V								
		G = 1		94	112		88	112		dB
		G = 1	●	87			83			dB
		G = 10		112	132		110	132		dB
		G = 10	●	106			104			dB
		G = 100		126	144		120	144		dB
		G = 100	●	120			114			dB
		G = 1000		134	148		130	148		dB
		G = 1000	●	122			120			dB
	AC Common Mode Rejection Ratio	f = 20kHz, DD10 Package								
		G = 1						77		dB
		G = 10						98		dB
		G = 100						135		dB
		G = 1000						128		dB
		f = 20kHz, MS8 Package f = 20kHz, S8E Package								
		G = 1			71			71		dB
		G = 10			91			91		dB
		G = 100			101			101		dB
		G = 1000			103			103		dB

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified temperature range, otherwise specifications are at T_A = 25°C. V_S = ±15V, V_{CM} = V_{REF} = 0V, R_L = 2kΩ.

SYMBOL	PARAMETER	CONDITIONS		LT6370A MIN	LT6370A TYP	LT6370A MAX	LT6370 MIN	LT6370 TYP	LT6370 MAX	UNITS
PSRR	Power Supply Rejection Ratio	V_S = ±2.375V to ±17.5V								
		G = 1		116	130		110	130		dB
		G = 1	●	114			106			dB
		G = 10		134	140		130	140		dB
		G = 10	●	124			120			dB
		G = 100		136	142		130	142		dB
		G = 100	●	125			120			dB
		G = 1000		136	146		130	146		dB
		G = 1000	●	125			120			dB
V_S	Supply Voltage	Guaranteed by PSRR	●	4.75		35	4.75		35	V
I_S	Supply Current	V_S = ±15V			2.65	2.75		2.65	2.75	mA
		T_A = –40°C to 85°C	●			2.9			2.9	mA
		T_A = –40°C to 125°C	●			3			3	mA
		V_S = ±2.375V			2.55	2.6		2.55	2.6	mA
		T_A = –40°C to 85°C	●			2.75			2.75	mA
		T_A = –40°C to 125°C	●			2.85			2.85	mA
V_{OUT}	Output Voltage Swing	V_S = ±15V, R_L = 10kΩ		–14.5	–14.9/14	13.7	–14.5	–14.9/14	13.7	V
			●	–14.3		13.6	–14.3		13.6	V
		V_S = ±2.375V, R_L = 10kΩ		–2	–2.3/1.6	1.5	–2	–2.3/1.6	1.5	V
			●	–1.8		1.3	–1.8		1.3	V
I_{OUT}	Output Short Circuit Current			35	55		35	55		mA
			●	30			30			mA
BW	–3dB Bandwidth	G = 1			3100			3100		kHz
		G = 10			1150			1150		kHz
		G = 100			184			184		kHz
		G = 1000			19			19		kHz
SR	Slew Rate	G = 1, V_{OUT} = ±10V		8	11		8	11		V/µs
			●	6			6			V/µs
t_S	Settling Time	20V Output Step to 0.0015%								
		G = 1			5.8			5.8		µs
		G = 10			9.8			9.8		µs
		G = 100			16			16		µs
		G = 1000			100			100		µs
R_{REFIN}	REF Input Resistance				20			20		kΩ
I_{REFIN}	REF Input Current	V_{+IN} = $V_{–IN}$ = V_{REF} =0V		–40	–27	–14	–40	–27	–14	µA
			●	–60		6	–60		6	µA
V_{REF}	REF Voltage Range		●	$V^–$		V^+	$V^–$		V^+	V
A_{VREF}	REF Gain to Output	V_{REF} = ±10V			1			1		V/V
	REF Gain Error	V_{REF} = ±10V		–80	–20	40	–100	–20	60	ppm
			●	–95		55	–115		75	ppm

ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Gains higher than 1000 are possible but the resulting low R_G values can make PCB and package lead resistance a significant error source.

Note 3: Gain tests are performed with –IN at mid-supply and +IN driven.

Note 4: When the gain is greater than 1 the gain error and gain drift specifications do not include the effect of external gain set resistor R_G.

Note 5: This specification is guaranteed by design.

Note 6: This specification is guaranteed with high-speed automated testing on the LT6370A. This specification is guaranteed by design and characterization on the LT6370.

Note 7: This parameter is measured in a high speed automatic tester that does not measure the thermal effects with longer time constants. The magnitude of these thermal effects are dependent on the package used, PCB layout, heat sinking and air flow conditions.

Note 8: For more information on how offsets relate to the amplifiers, see section “Input and Output Offset Voltage” in the Applications section.

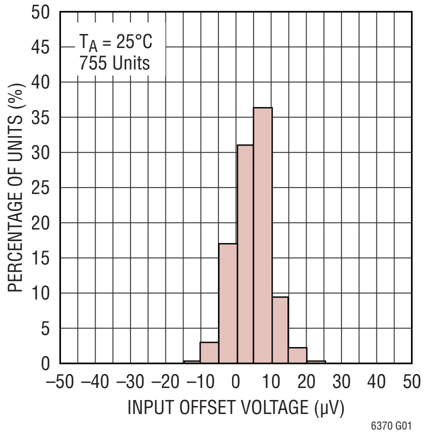
Note 9: Hysteresis in output voltage is created by mechanical stress that differs depending on whether the IC was previously at a higher or lower temperature. Output voltage is always measured at 25°C, but the IC is cycled to the hot or cold temperature limit before successive measurements. Hysteresis is roughly proportional to the square of the temperature change. For instruments that are stored at well controlled temperatures (within 20 or 30 degrees of operational temperature), hysteresis is usually not a significant error source. Typical hysteresis is the worst case of 25°C to cold to 25°C or 25°C to hot to 25°C, preconditioned by one thermal cycle.

Note 10: Referred to the input.

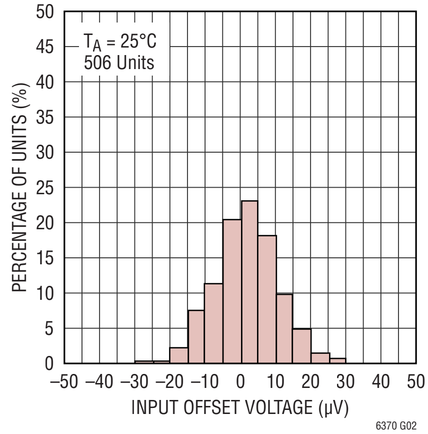
TYPICAL PERFORMANCE CHARACTERISTICS

V_S = ±15V, V_{CM} = V_{REF} = 0V, T_A = 25°C, R_L = 2k, unless otherwise noted.

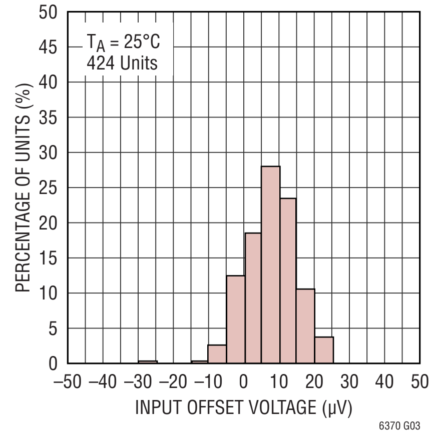
Distribution of Input Offset Voltage, MS8 Package



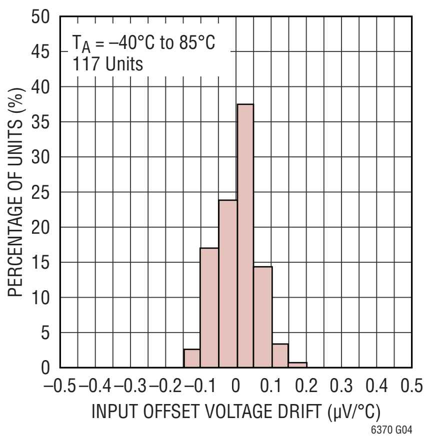
Distribution of Input Offset Voltage, S8E Package



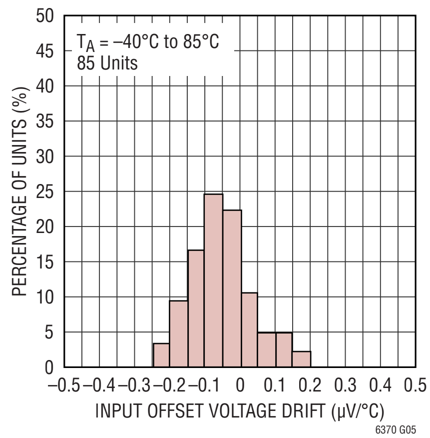
Distribution of Input Offset Voltage, DD10 Package



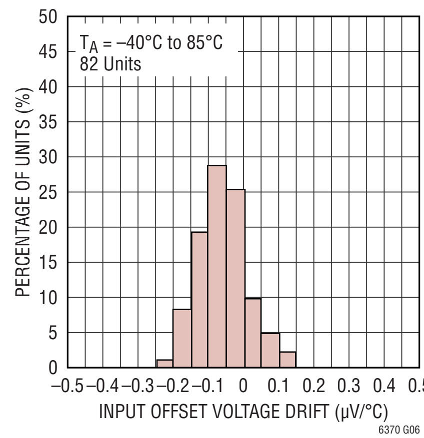
Distribution of Input Offset Voltage Drift, MS8 Package



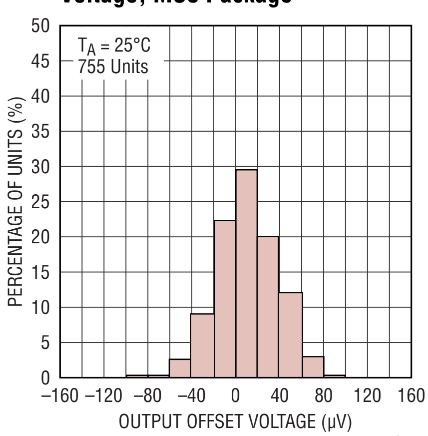
Distribution of Input Offset Voltage Drift, S8E Package



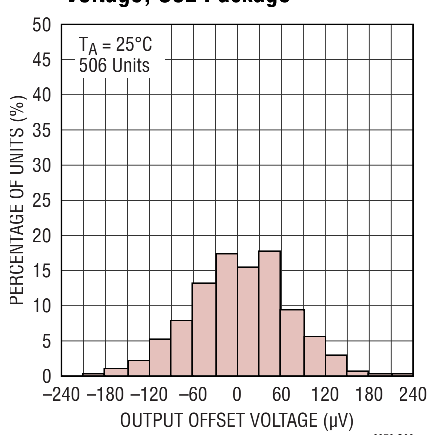
Distribution of Input Offset Voltage Drift, DD10 Package



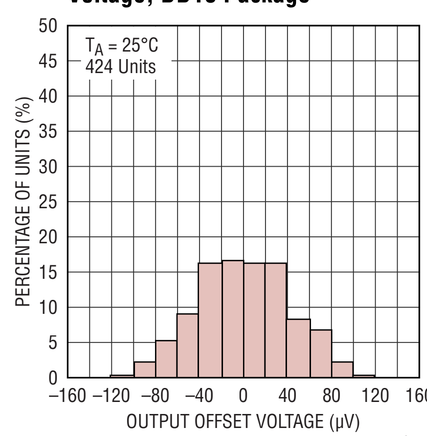
Distribution of Output Offset Voltage, MS8 Package



Distribution of Output Offset Voltage, S8E Package



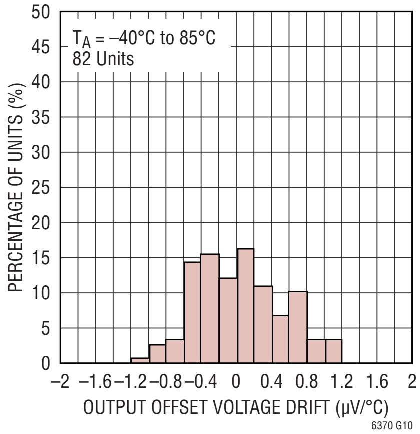
Distribution Output Offset Voltage, DD10 Package



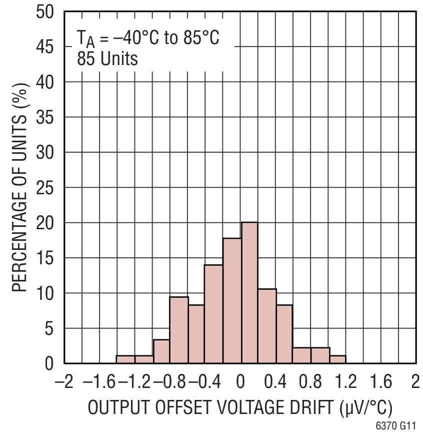
TYPICAL PERFORMANCE CHARACTERISTICS

$V_S = \pm15V$, $V_{CM} = V_{REF} = 0V$, $T_A = 25°C$, $R_L = 2k$, unless otherwise noted.

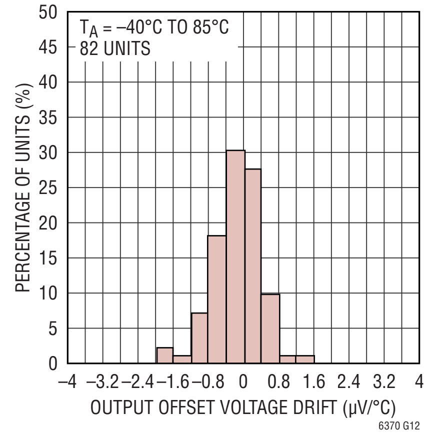
Distribution of Output Offset Voltage Drift, MS8 Package



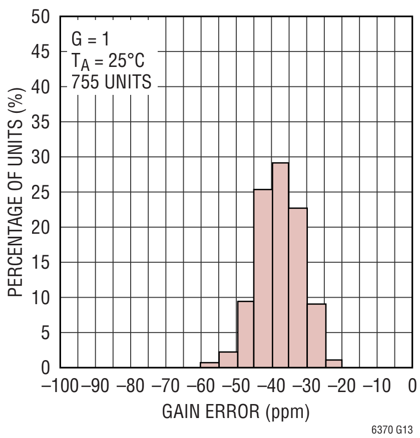
Distribution of Output Offset Voltage Drift, S8E Package



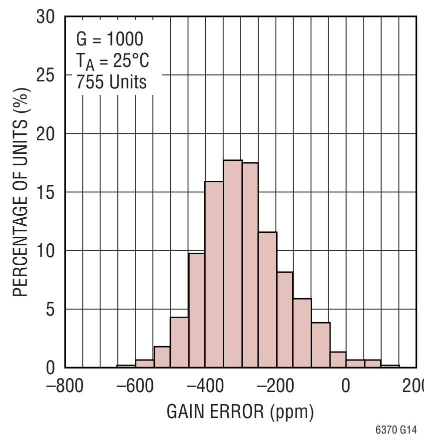
Distribution of Output Offset Voltage Drift, DD10 Package



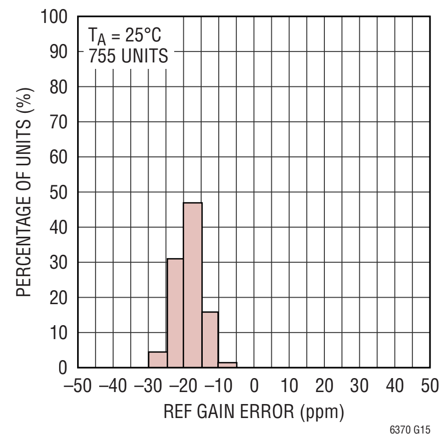
Distribution of Gain Error



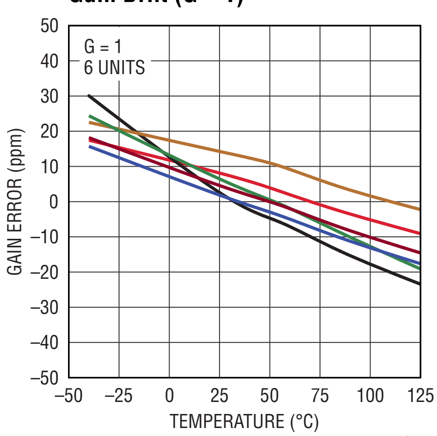
Distribution of Gain Error



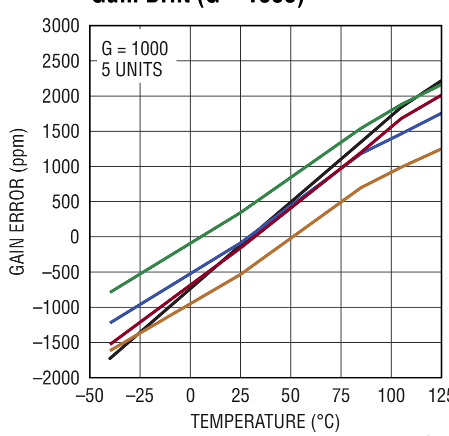
Distribution of REF Gain Error



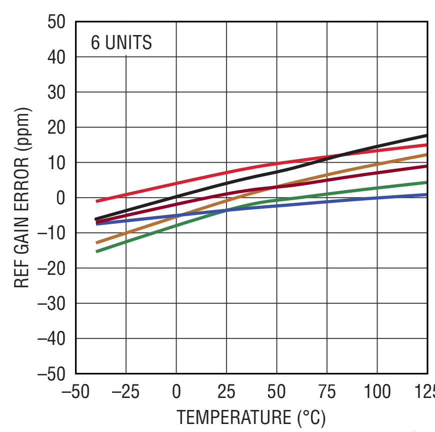
Gain Drift (G = 1)



Gain Drift (G = 1000)



REF Gain Drift



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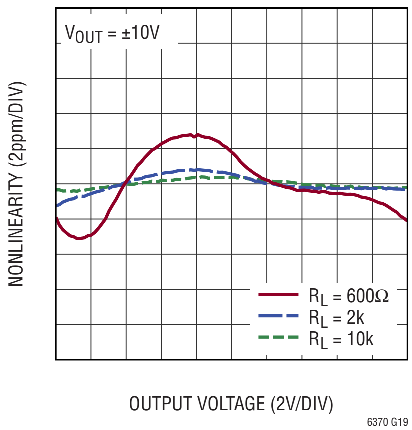
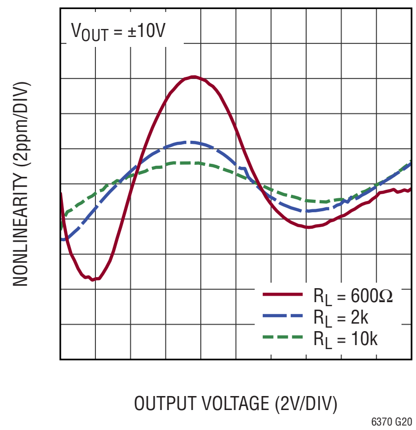
TYPICAL PERFORMANCE CHARACTERISTICS

V_S = ±15V, V_{CM} = V_{REF} = 0V, T_A = 25°C, R_L = 2k, unless otherwise noted.

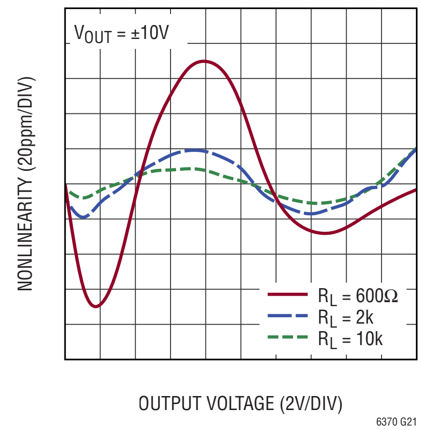
Gain Nonlinearity (G = 1)



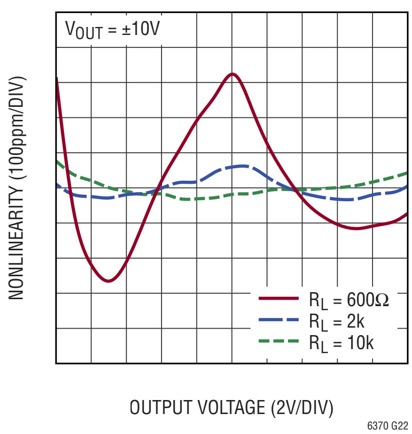
Gain Nonlinearity (G = 10)



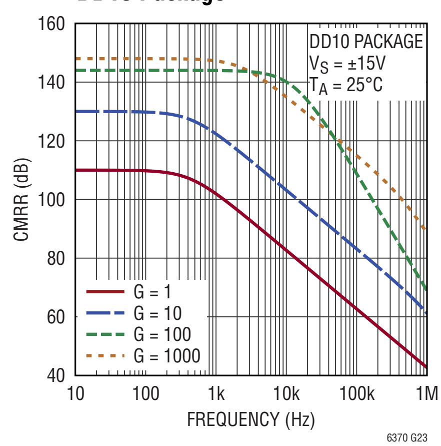
Gain Nonlinearity (G = 100)



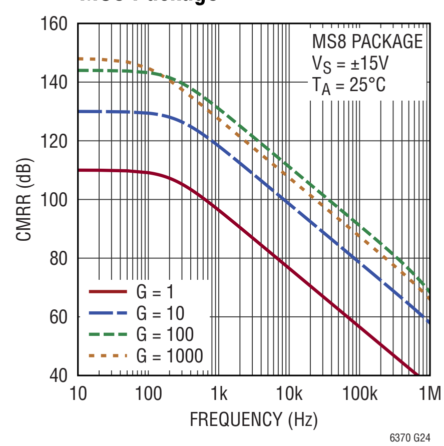
Gain Nonlinearity (G = 1000)



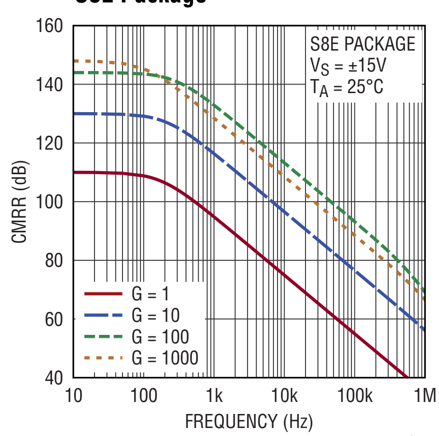
CMRR vs Frequency, RTI DD10 Package



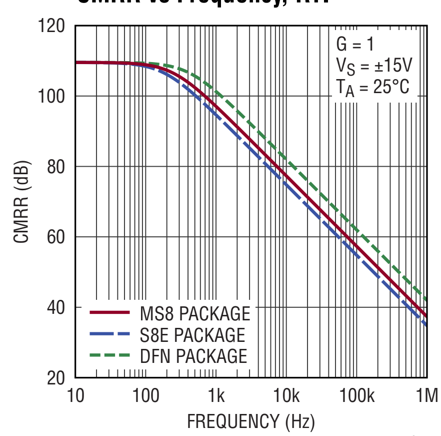
CMRR vs Frequency, RTI MS8 Package



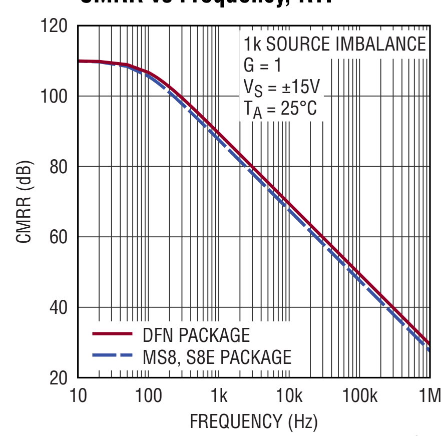
CMRR vs Frequency, RTI S8E Package



CMRR vs Frequency, RTI



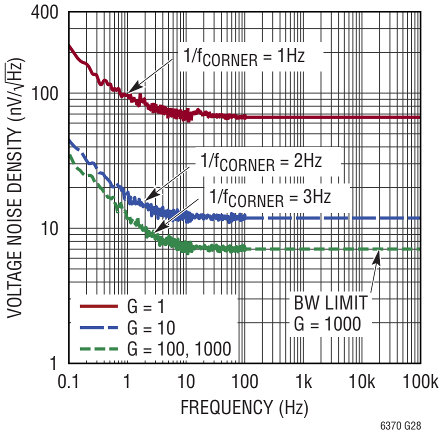
CMRR vs Frequency, RTI



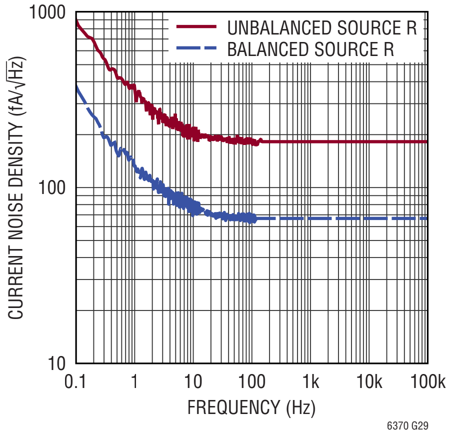
TYPICAL PERFORMANCE CHARACTERISTICS

V_S = ±15V, V_{CM} = V_{REF} = 0V, T_A = 25°C, R_L = 2k, unless otherwise noted.

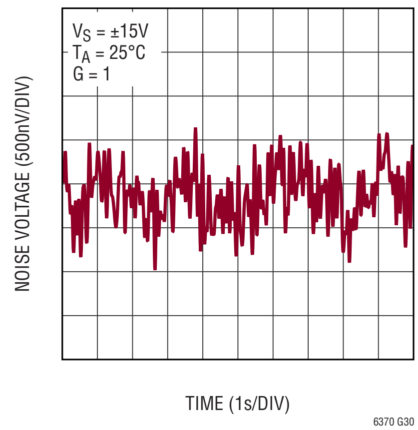
Input-Referred Voltage Noise Density vs Frequency



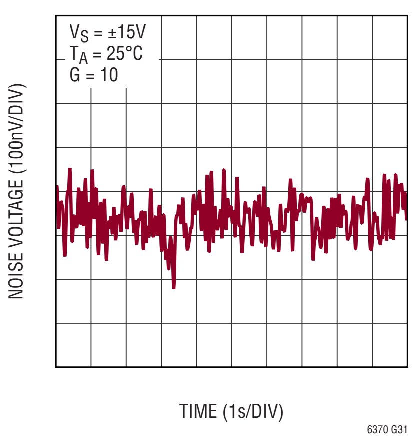
Current Noise Density vs Frequency



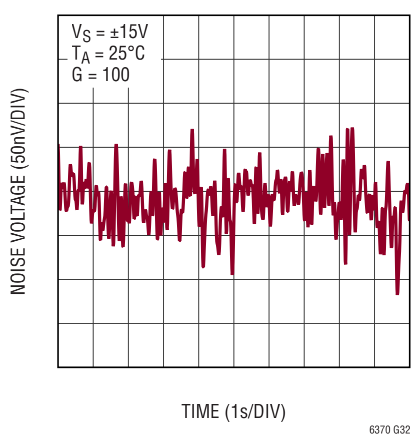
0.1Hz to 10Hz Voltage Noise, G = 1, RTI



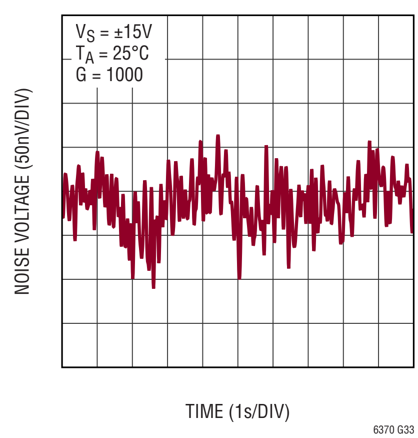
0.1Hz to 10Hz Voltage Noise, G = 10, RTI



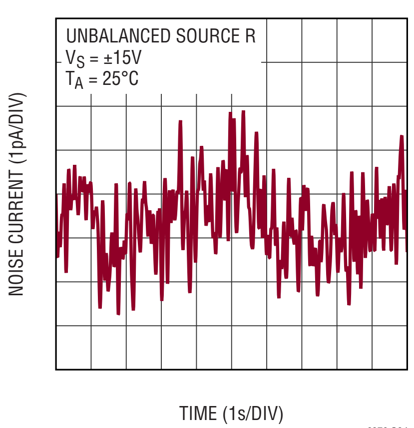
0.1Hz to 10Hz Voltage Noise, G = 100, RTI



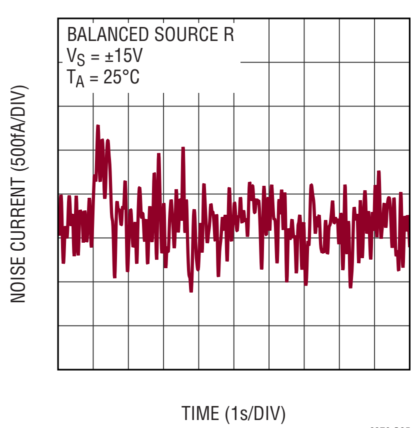
0.1Hz to 10Hz Voltage Noise, G = 1000, RTI



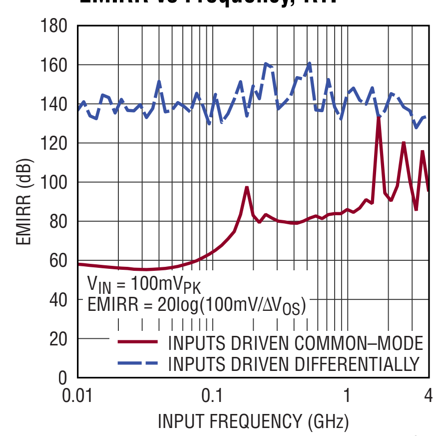
0.1Hz to 10Hz Noise Current, Unbalanced Source R



0.1Hz to 10Hz Noise Current, Balanced Source R



EMIRR vs Frequency, RTI



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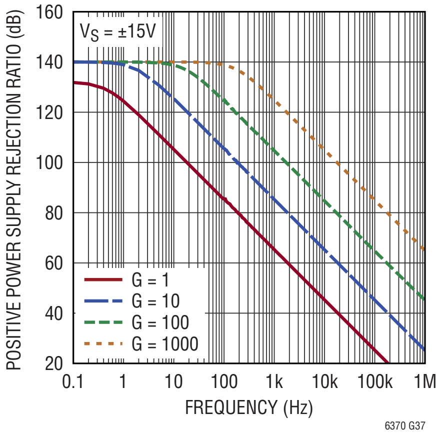
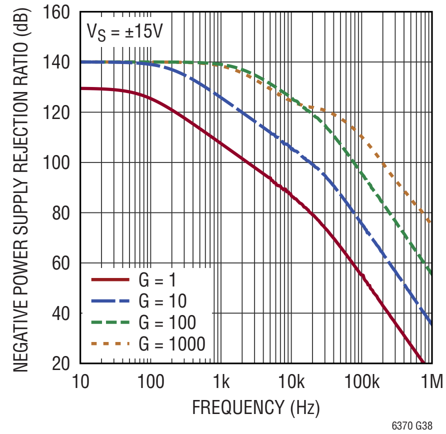
TYPICAL PERFORMANCE CHARACTERISTICS

$V_S = \pm 15V$, $V_{CM} = V_{REF} = 0V$, $T_A = 25°C$, $R_L = 2k$, unless otherwise noted.

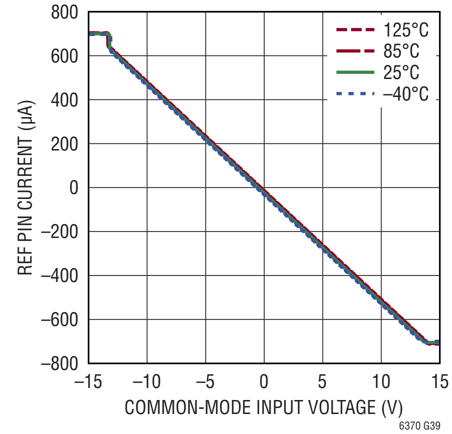
Positive Power Supply Rejection Ratio vs Frequency



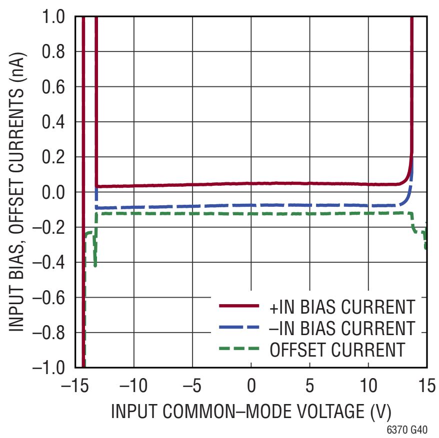
Negative Power Supply Rejection Ratio vs Frequency



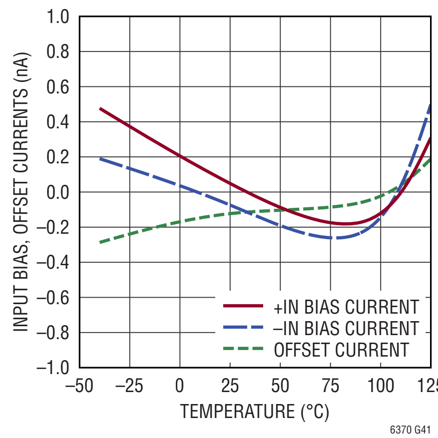
REF Pin Current vs Input Common Mode Voltage



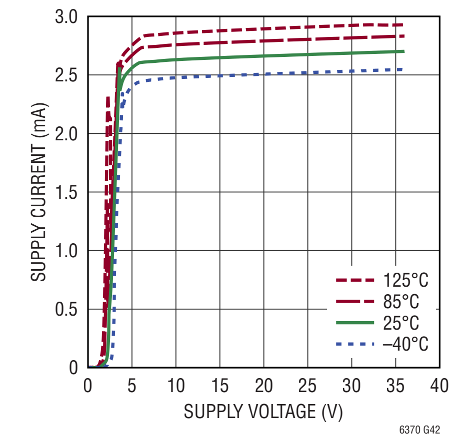
Input Bias Current vs Common Mode Voltage



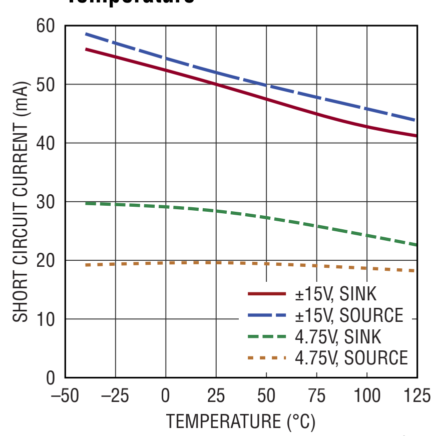
Input Bias and Offset Current vs Temperature



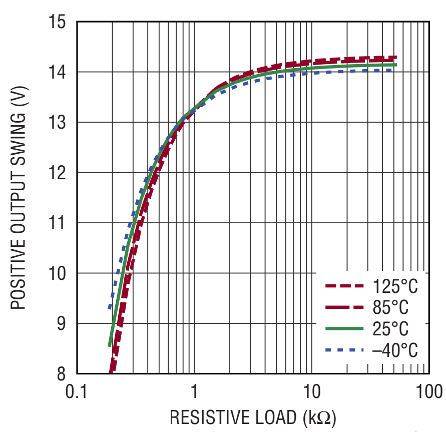
Supply Current vs Supply Voltage



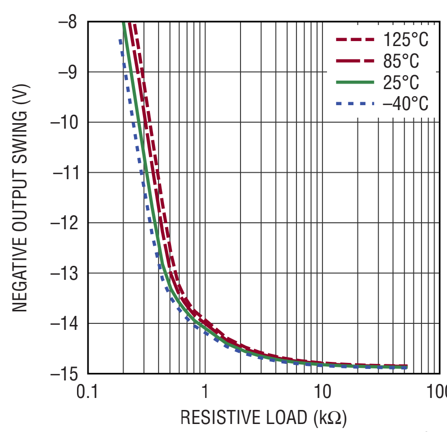
Output Short Circuit Current vs Temperature



Output Voltage Swing vs Load Resistance



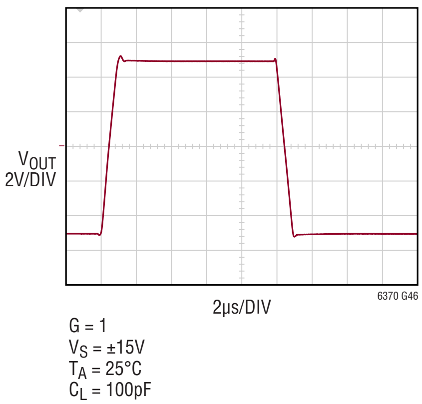
Output Voltage Swing vs Load Resistance



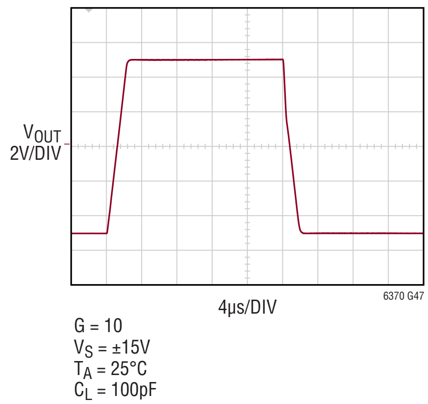
TYPICAL PERFORMANCE CHARACTERISTICS

$V_S = \pm15V$, $V_{CM} = V_{REF} = 0V$, $T_A = 25°C$, $R_L = 2k$, unless otherwise noted.

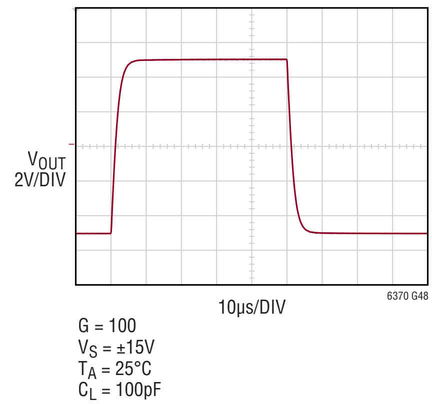
Large Signal Transient Response



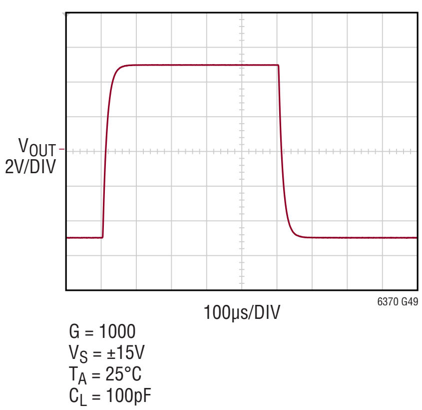
Large Signal Transient Response



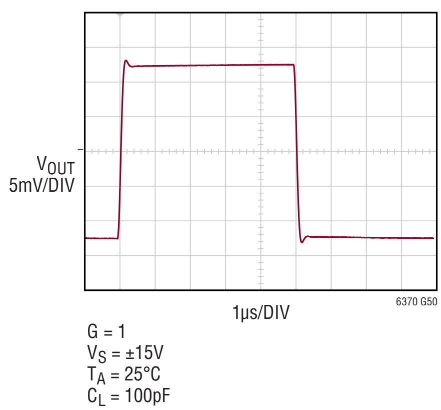
Large Signal Transient Response



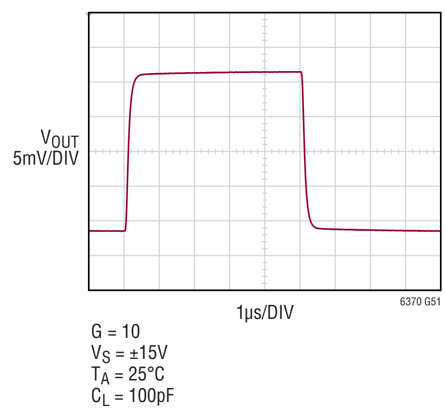
Large Signal Transient Response



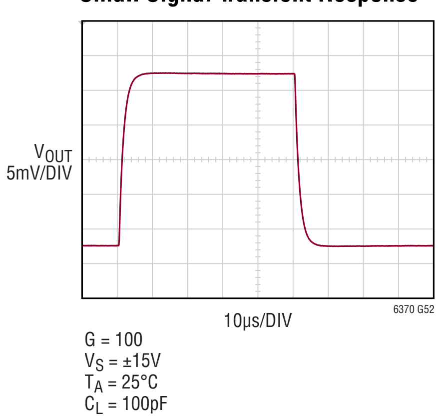
Small Signal Transient Response



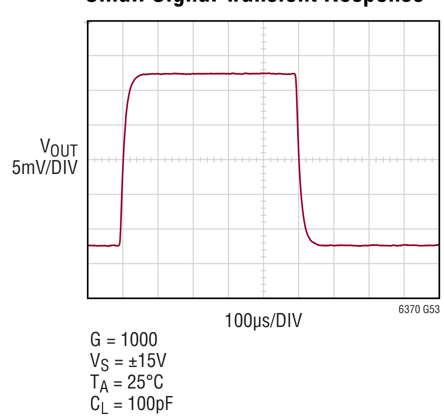
Small Signal Transient Response



Small Signal Transient Response



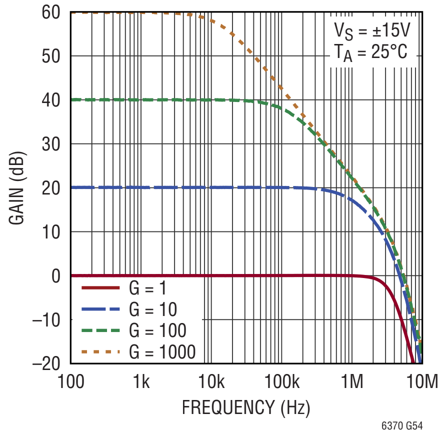
Small Signal Transient Response



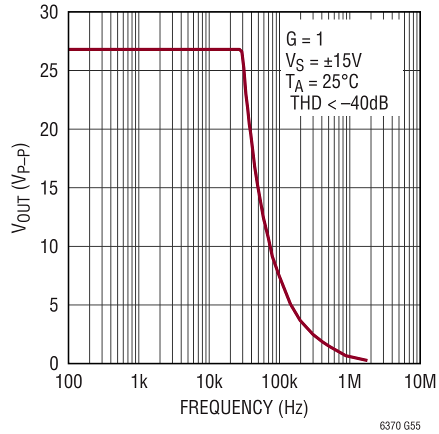
TYPICAL PERFORMANCE CHARACTERISTICS

V_S = ±15V, V_{CM} = V_{REF} = 0V, T_A = 25°C, R_L = 2k, unless otherwise noted.

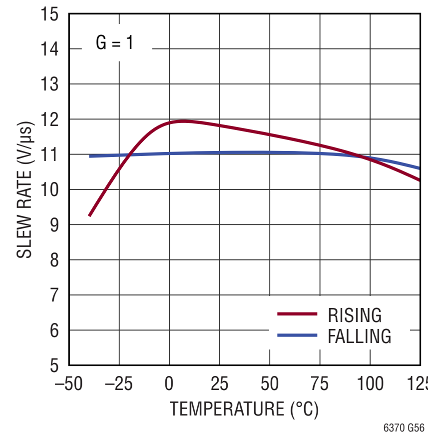
Gain vs Frequency



Undistorted Output Swing vs Frequency



Slew Rate vs Temperature



PIN FUNCTIONS (MS/DFN/SOIC)

–R_G (Pin 1/Pin 1/Pin 1): For use with an external gain setting resistor.

–IN (Pin 2/Pin 3/Pin 2): Negative Input Terminal. This input is high impedance.

+IN (Pin 3/Pin 4/Pin 3): Positive Input Terminal. This input is high impedance.

$V^–$ (Pin 4/Pin 5/Pin 4): Negative Power Supply. A bypass capacitor should be used between supply pins and ground.

REF (Pin 5/Pin 6/Pin 5): Reference for the output voltage.

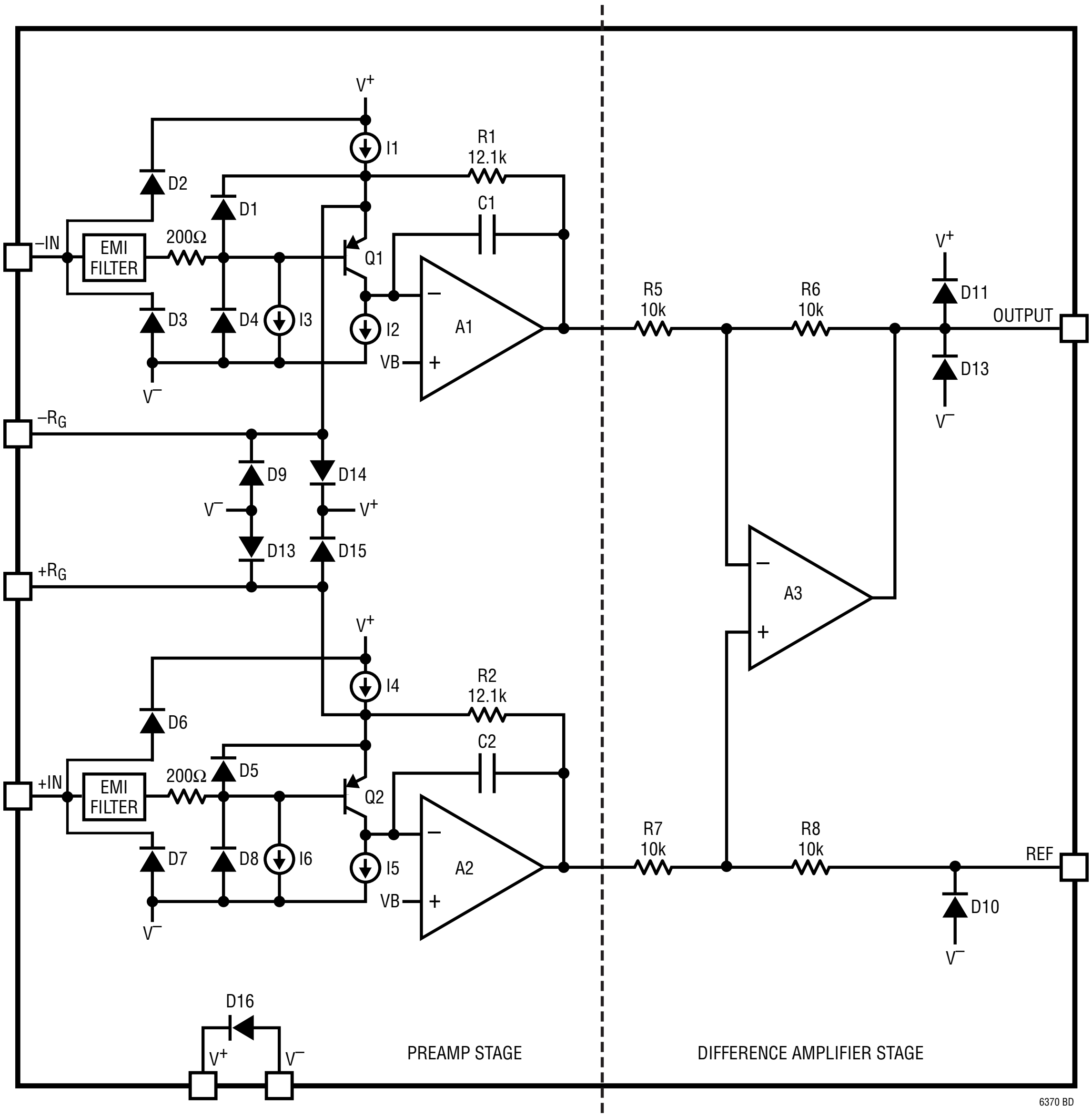
OUTPUT (Pin 6/Pin 7/Pin 6): Output voltage referenced to the REF pin.

V^+ (Pin 7/Pin 8/Pin 7): Positive Power Supply. A bypass capacitor should be used between supply pins and ground.

+R_G (Pin 8/Pin 10/Pin 8): For use with an external gain setting resistor.

NC (DFN Pins 2, 9): No Internal Connection.

SIMPLIFIED BLOCK DIAGRAM



THEORY OF OPERATION

The LT6370 is an improved version of the classic three op amp instrumentation amplifier topology. Laser trimming and proprietary monolithic construction allow for tight matching and extremely low drift of circuit parameters over the specified temperature range. Refer to the Simplified Block Diagram to aid in understanding the following circuit description. The collector currents in Q1 and Q2 as well as I1 and I4 are trimmed to minimize input offset voltage drift, thus assuring a high level of performance. R1 and R2 are trimmed to an absolute value of 12.1k to assure that the gain can be set accurately (0.08% at G = 100) with only one external resistor, R_G. The value of R_G determines the transconductance of the preamp stage. As R_G is reduced to increase the programmed gain, the transconductance of the input preamp stage also increases to that of the input transistors Q1 and Q2. This causes the open-loop gain to increase when the programmed gain is increased, reducing the input related errors and noise. The input voltage noise at high gains is determined only by Q1 and Q2. At lower gains the noise of the difference amplifier and preamp gain setting resistors may increase the noise. The gain bandwidth product is determined by C1, C2 and the preamp transconductance, which increases with programmed gain. Therefore, the bandwidth is self-adjusting and does not drop directly proportional to gain.

The input transistors Q1 and Q2 offer excellent matching, drift and noise performance, which is due to using a proprietary high performance process, as well as low input bias current due to the high beta of these input devices. The input bias current is further reduced by trimming I3 and I6. The collector currents in Q1 and Q2 are held constant due to the feedback through the Q1-A1-R1 loop and Q2-A2-R2 loop. The action of the amplifier loops impresses the differential input voltage across the external gain set resistor R_G. Since the current that flows through R_G also flows through R1 and R2, the ratios provide a gained-up differential voltage,

$$G = 1 + \frac{R1 + R2}{R_G}$$

to the difference amplifier A3. The difference amplifier removes the common mode voltage and provides a single-ended output voltage referenced to the voltage on the REF pin. The offset voltage of the difference amplifier is trimmed to minimize output offset voltage drift, thus assuring a high level of performance, even in low gains. Resistors R5 to R8 are trimmed to maximize CMRR and minimize gain error. The resulting gain equation is:

$$G = 1 + \frac{24.2k}{R_G}$$

Solving for the gain set resistor gives:

$$R_G = \frac{24.2k}{G - 1}$$

Table 1 shows appropriate 1% resistor values for a variety of gains.

Table 1. LT6370 Gain and R_G Lookup.

Resulting Gains for Various 1% Standard Resistor Values	
Gain	**Standard 1% Resistor Value (Ω)**
1	–
1.996	24.3k
5.007	6.04k
10.06	2.67k
20.06	1.27k
50.69	487
100.6	243
201	121
497.9	48.7
996.9	24.3
Convenient Integer Gains Using Various Standard 1% Resistor Values	
Integer Gain	**Standard 1% Resistor Value (Ω)**
1	–
3	12.1k
21	1.21k
23	1.1k
122	200
201	121
221	110
243	100
1211 (Note 2)	20

APPLICATIONS INFORMATION

Valid Input and Output Range

Instrumentation amplifiers traditionally specify a valid input common mode range and an output swing range. This however often fails to identify limitations associated with internal swing limits. Referring to the Simplified Block Diagram, the output swing of pre-amplifiers A1 and A2 as well as the common-mode input range of the difference amplifier A3 impose limitations on the valid operating range. The following graphs show the operating region where a valid output is produced.

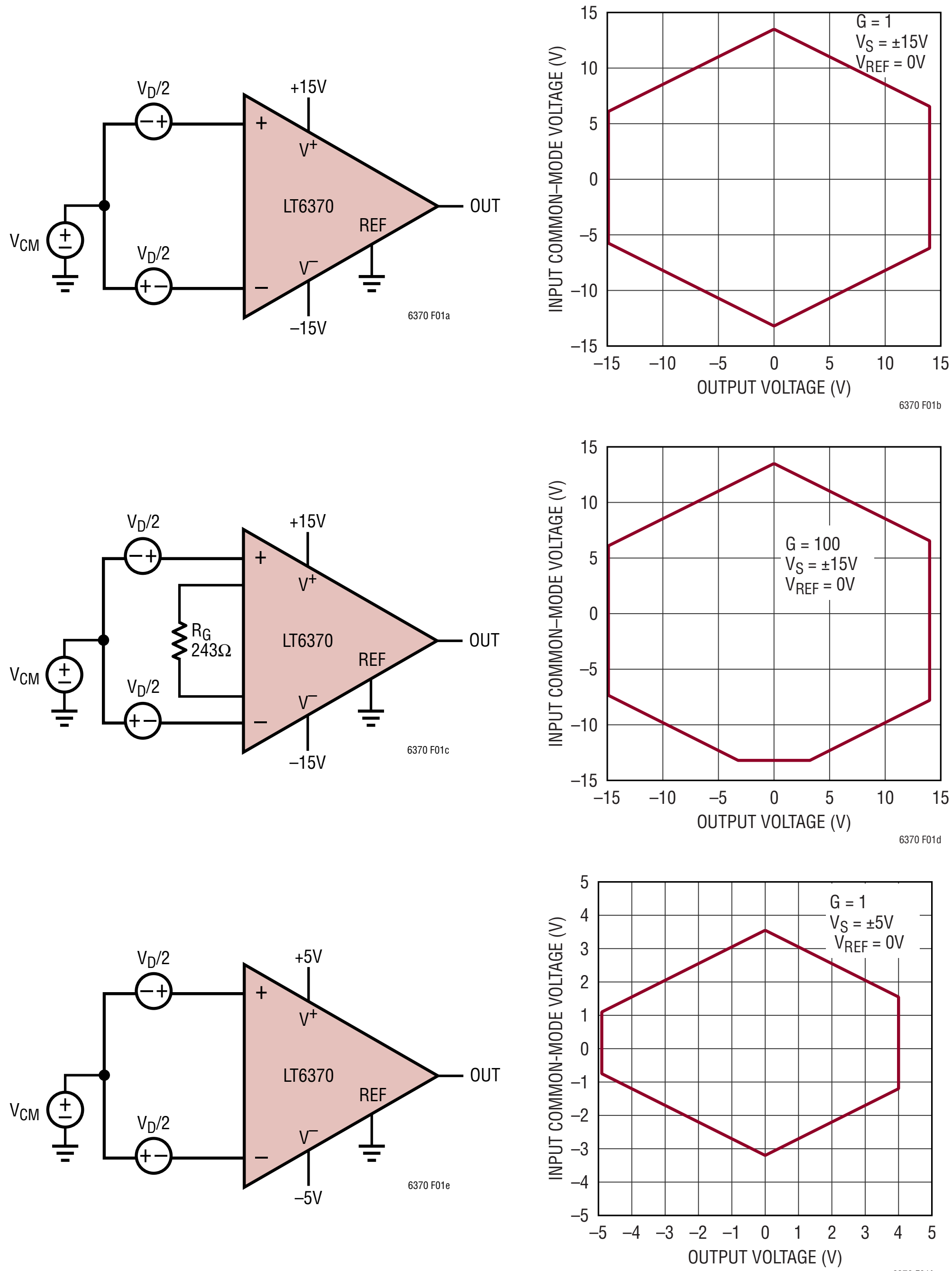


Figure 1. Input Common Mode Range vs Output Voltage

APPLICATIONS INFORMATION

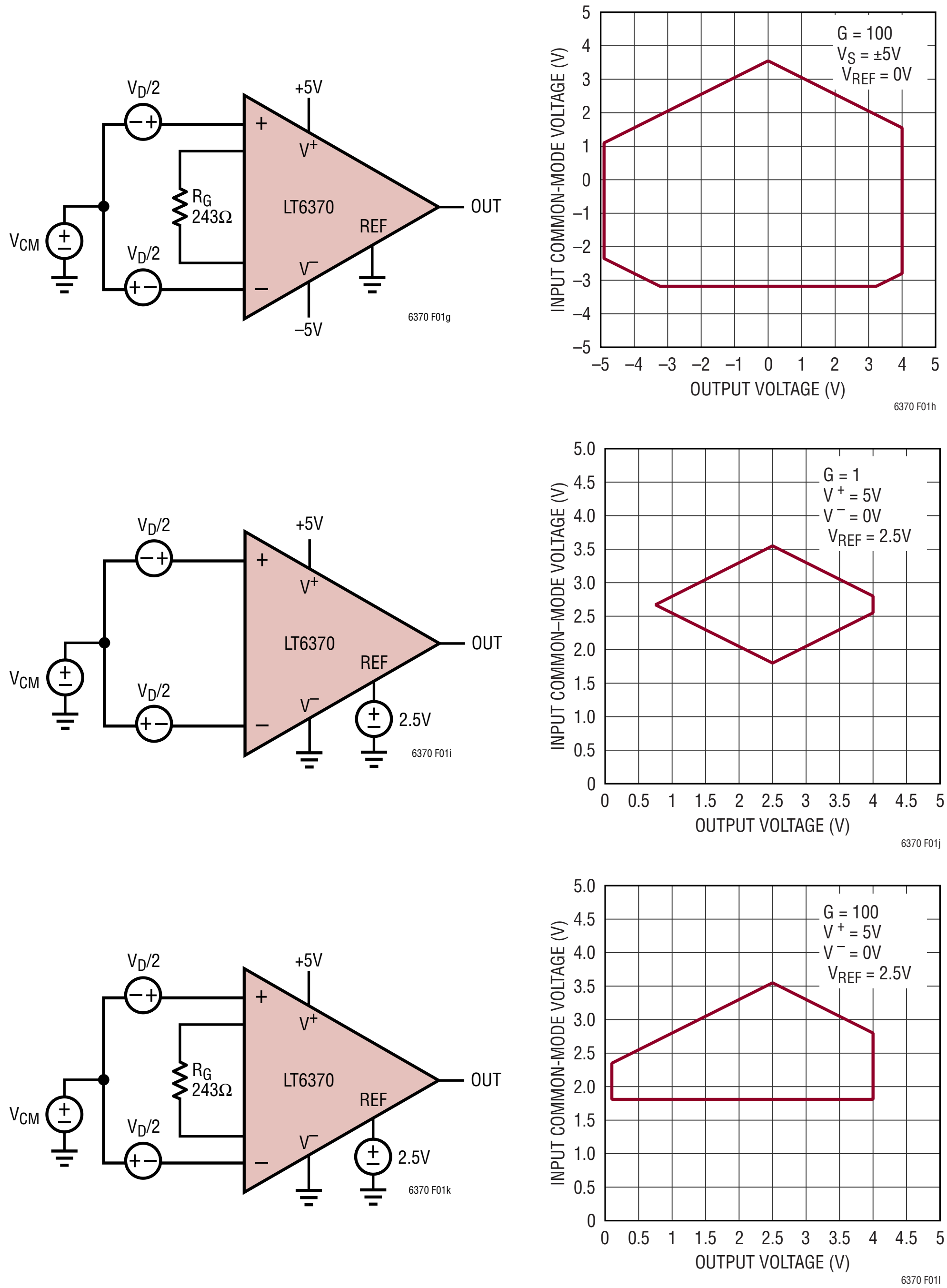


Figure 1 (Continued). Input Common Mode Range vs Output Voltage

APPLICATIONS INFORMATION

REF Pin

The REF pin has a nominal gain of 1 to the output. Resistance in series with the REF pin must be minimized to preserve high common mode rejection. For example, a series resistance of 2Ω from the REF pin to ground will not only increase the gain error by 0.02% but will lower the CMRR to 80dB. If this pin is driven by an amplifier as shown in Figure 2, the closed-loop output impedance of this amplifier at the desired frequency must also be low to avoid degrading the AC CMRR shown in the typical curves section.

It is also important to note that the drift in the circuitry used to drive the REF pin will result in an additional output drift term. Therefore, it may be important to consider the temperature accuracy of the circuitry used to drive the REF pin.

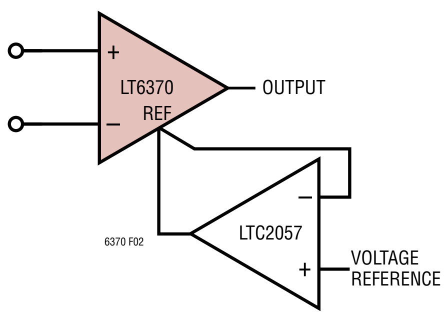


Figure 2. Buffering the REF Pin

Input and Output Offset Voltage

The offset voltage of the LT6370 has two main components: the input offset voltage due to the input amplifiers and the output offset due to the output amplifier. The total offset voltage referred to the input (RTI) is found by dividing the output offset by the programmed gain and adding it to the input offset voltage. At high gains the input offset voltage dominates, whereas at low gains the output offset voltage dominates. The total offset voltage is:

Total input offset voltage (RTI) = $V_{OSI} + V_{OSO}/G$

Total output offset voltage (RTO) = $V_{OSI} \bullet G + V_{OSO}$

The preceding equations can also be used to calculate offset drift in a similar manner.

Output Offset Trimming

The LT6370 is laser trimmed for low offset voltage so that no external offset trimming is required for most applications. In the event that the offset voltage needs to be adjusted, the circuit in Figure 3 is an example of an optional offset adjustment circuit. The op amp buffer provides a low impedance signal to the REF pin in order to achieve the best CMRR and lowest gain error.

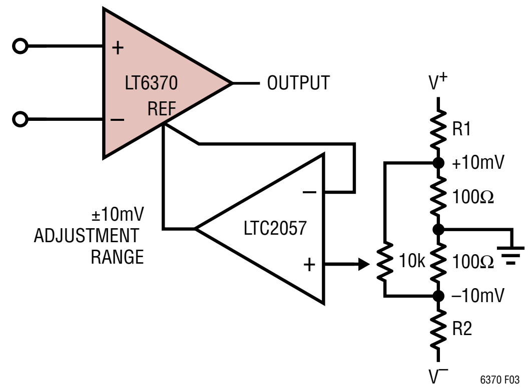


Figure 3. Optional Trimming of Output Offset Voltage

Thermocouple Effects

In order to achieve accuracy on the microvolt level, thermocouple effects must be considered. Any connection of dissimilar metals forms a thermoelectric junction and generates a small temperature-dependent voltage. Also known as the Seebeck Effect, these thermal EMFs can be the dominant error source in low-drift circuits.

Connectors, switches, relay contacts, sockets, resistors, and solder are all candidates for significant thermal EMF generation. Even junctions of copper wire from different manufacturers can generate thermal EMFs of 200nV/°C, which is comparable to the maximum input offset voltage drift specification of the LT6370. Figures 4 and 5 illustrate the potential magnitude of these voltages and their sensitivity to temperature.

In order to minimize thermocouple-induced errors, attention must be given to circuit board layout and component selection. It is good practice to minimize the number of junctions in the amplifier's input and R_G signal paths and avoid connectors, sockets, switches, and relays whenever possible. If such components are required, they should be

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selected for low thermal EMF characteristics. Furthermore, the number, type, and layout of junctions should be matched for both inputs with respect to thermal gradients on the circuit board. Doing so may involve deliberately introducing dummy junctions to offset unavoidable junctions.

Air currents can also lead to thermal gradients and cause significant noise in measurement systems. It is important to prevent airflow across sensitive circuits. Doing so will often reduce thermocouple noise substantially. Placing PCB input traces close together, and on an internal PCB layer, can help minimize temperature differentials resulting from air currents reacting with the input trace thermal surface area.

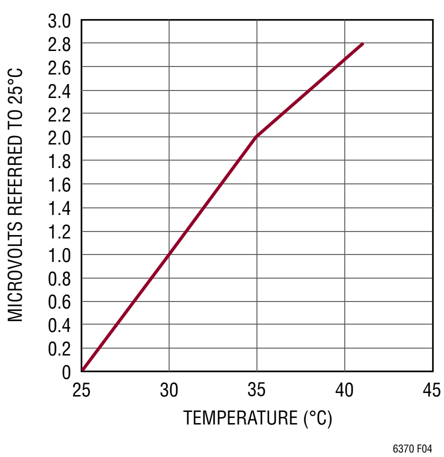

Figure 4. Thermal EMF Generated by Two Copper Wires From Different Manufacturers

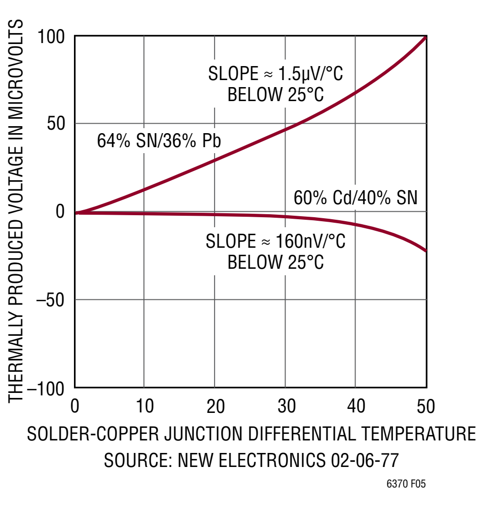

Figure 5. Solder-Copper Thermal EMFs

Reducing Board-Related Leakage Effects

Leakage currents can have a significant impact on system accuracy, particularly in high temperature and high voltage applications. Quality insulation materials should be used, and insulating surfaces should be cleaned to remove fluxes and other residues. For humid environments, surface coating may be necessary to provide a moisture barrier.

Leakage into the R_G pin conducts through the on-chip feedback resistor, creating an error at the output of the pre-amplifiers. This error is independent of gain and degrades accuracy the most at low gains. This leakage can be minimized by encircling the R_G connections with a guard-ring operated at a potential very close to that of the R_G pins. The DFN package has NC pins adjacent to each R_G pin which can be used to simplify the implementation of this guard-ring. These NC pins do not provide any bias and have no internal connections. In some cases, the guard-ring can be connected to the input voltage which biases one diode drop below R_G.

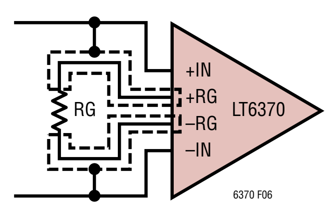

Figure 6. Guard-Rings Can Be Used to Minimize Leakage into the R_G Pins

Leakage into the input pins reacts with the source resistance, creating an error directly at the input. This leakage can be minimized by encircling the input connections with a guard-rings operated at a potential very close to that of the input pins. In some cases, the guard-ring can be connected to R_G which biases one diode above the input.

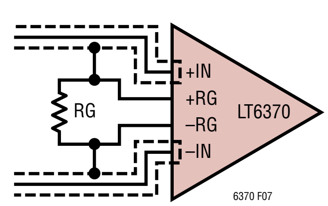

Figure 7. Guard-Rings Can Be Used to Minimize Leakage into the Input Pins

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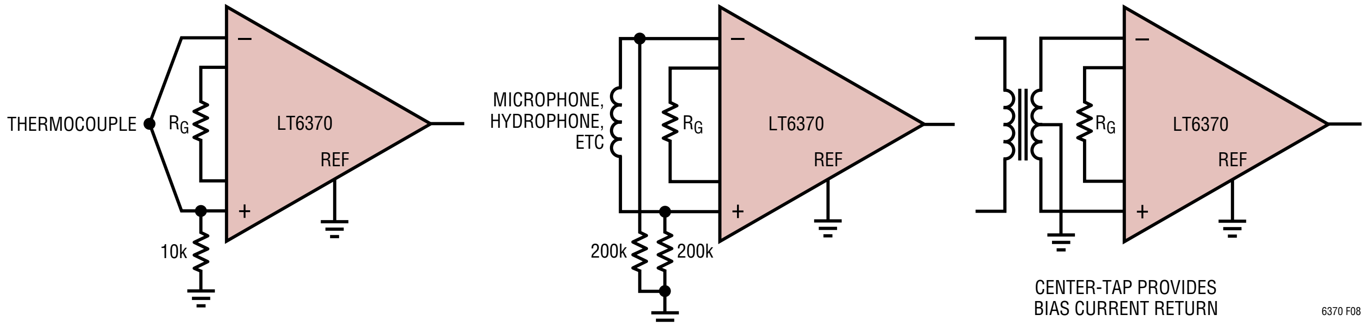

Figure 8. Providing an Input Common Mode Current Path

For the lowest leakage, amplifiers can be used to drive the guard ring. These buffers must have very low input bias current since that will now be a leakage.

Input Bias Current Return Path

The low input bias current of the LT6370 (400pA max) and high input impedance (225GΩ) allow the use of high impedance sources without introducing additional offset voltage errors, even when the full common mode range is required. However, a path must be provided for the input bias currents of both inputs when a purely differential signal is being amplified. Without this path, the inputs will float to either rail and exceed the input common mode range of the LT6370, resulting in a saturated input amplifier. Figure 8 shows three examples of an input bias current path. The first example is of a purely differential signal source with a 10kΩ input current path to ground. Since the impedance of the signal source is low, only one resistor is needed. Two matching resistors are needed for higher impedance signal sources as shown in the second example. Balancing the input impedance improves both AC and DC common mode rejection and DC offset. The need for input resistors is eliminated if a center tap is present as shown in the third example.

Input Protection

Additional input protection can be achieved by adding external resistors in series with each input. If low value resistors are needed, a clamp diode from the positive supply to each input will help improve robustness. A 2N4394 drain/source to gate is a good low leakage diode which can be used as shown in Figure 9. Robust input resistors should be chosen, such as carbon composite or bulk metal foil. Metal film and carbon film should not be used because of their poor performance.

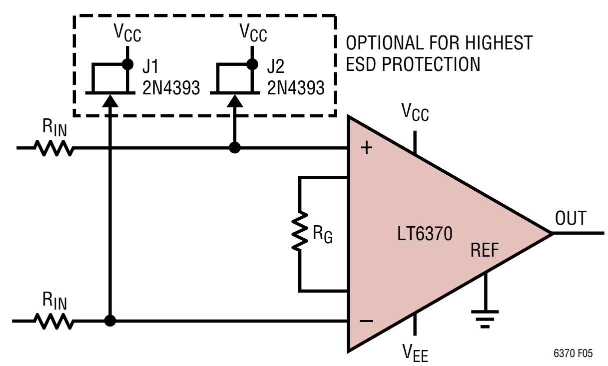

Figure 9. Input Protection

Maintaining AC CMRR

To achieve optimum AC CMRR, it is important to balance the capacitance on the R_G gain setting pins. Furthermore, if the source resistance on each input is not equal, adding an additional resistance to one input to improve input source resistance matching will improve AC CMRR.

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RFI Reduction/Internal RFI Filter

In many industrial and data acquisition applications, the LT6370 will be used to amplify small signals accurately in the presence of large common mode voltages or high levels of noise. Typically, the sources of these very small signals (on the order of microvolts or millivolts) are sensors that can be a significant distance from the signal conditioning circuit. Although these sensors may be connected to signal conditioning circuitry using shielded or unshielded twisted-pair cabling, the cabling may act as an antenna, conveying very high frequency interference directly into the input stage of the LT6370.

The amplitude and frequency of the interference can have an adverse effect on an instrumentation amplifier's input stage by causing any unwanted DC shift in the amplifier's input offset voltage. This well known effect is called RFI rectification and is produced when out-of-band interference is coupled (inductively, capacitively or via radiation) and rectified by the instrumentation amplifier's input transistors. These transistors act as high frequency signal detectors, in the same way diodes were used as RF envelope detectors in early radio designs. Regardless of the type of interference or the method by which it is coupled into the circuit, an out-of-band error signal appears in series with the instrumentation amplifier's inputs.

To help minimize this effect, the LT6370 has 50MHz on-chip RFI filters to help attenuate high frequencies before they can interact with its input transistors. These on-chip filters are well matched due to their monolithic construction, which helps minimize any degradation in AC CMRR. To reduce the effect of these out-of-band signals on the input offset voltage of the LT6370 further, an additional external low-pass filter can be used at the inputs. The filter should be located very close to the input pins of the circuit. An effective filter configuration is illustrated in Figure 10, where three capacitors have been added to the inputs of the LT6370.

The filter limits the input signal according to the following relationship:

$$\text{FilterFreq}_{DIFF} = \frac{1}{2\pi R(2C_D + C_C)}$$

$$\text{FilterFreq}_{CM} = \frac{1}{2\pi RC_C}$$

where $C_D \geq 10C_C$.

C_D affects the difference signal. C_C affects the common-mode signal. Any mismatch in $R \times C_C$ degrades the LT6370 CMRR. To avoid inadvertently reducing CMRR-bandwidth performance, make sure that C_C is at least one order of magnitude smaller than C_D.The effect of mismatched C_Cs is reduced with a larger C_D:C_C ratio.

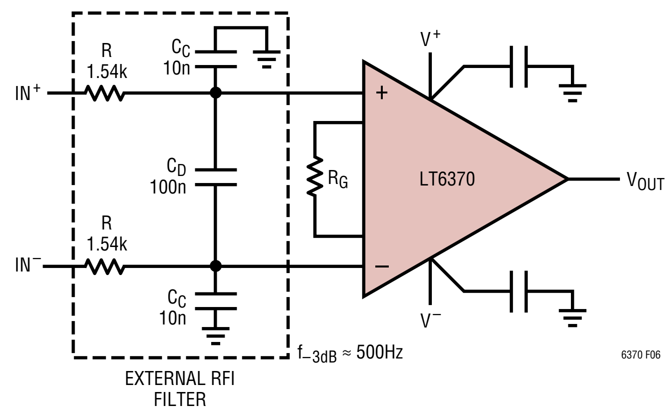

Figure 10. Adding a Simple External RC Filter at the Inputs to an Instrumentation Amplifier Is Effective in Further Reducing Rectification of High Frequency Out-Of-Band Signals.

To avoid any possibility of common mode to differential mode signal conversion, match the common mode low-pass filter on each input to 1% or better. Here are the steps to help determine appropriate values for the filter:

1. Pick R and C_D to have a low pass pole at least 10x higher than the highest signal of interest (e.g. 500Hz for a 50Hz signal) using:

$$\text{FilterFreq}_{DIFF} = \frac{1}{2\pi R(2C_D + C_C)} = \frac{1}{2\pi R(2C_D + 0.1C_D)} = \frac{1}{4.2\pi RC_D}$$

2. Select $C_C = C_D/10$.

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If implemented this way, the common-mode pole frequency is placed about 20x higher than the differential pole frequency. Here are the differential and common-mode low pass pole frequencies for the values shown in Figure 10:

$FilterFreq_{DIFF}$ = 500Hz

$FilterFreq_{CM}$ = 10kHz

Error Budget Analysis

The LT6370 offers performance superior to that of competing monolithic instrumentation amplifiers. A typical application that amplifies and buffers a bridge transducer's differential output is shown in Figure 11. The amplifier is set to a gain of 100 and amplifies a differential, full-scale transducer's output voltage of 20mV over the industrial temperature range. The LT6370 will be compared to other monolithic instrumentation amplifiers. As shown, the LT6370 outperforms these other instrumentation amplifiers. The error budget comparison in Table 2 shows how various errors are calculated and how each error affects the total error budget. The table shows the clear benefit to low offset voltage, low offset voltage drift and low gain drift.

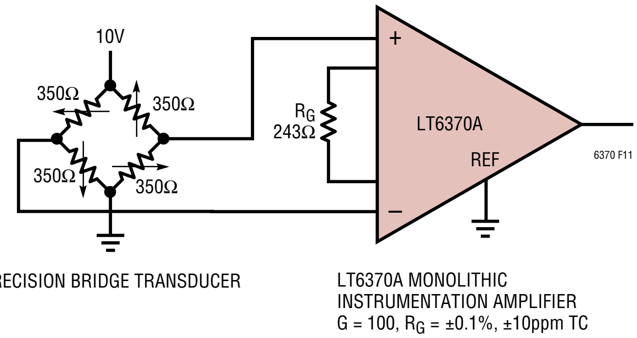

Figure 11. Precision Bridge Amplifier

Table 2. Error Budget Comparison

		ERROR, ppm OF FULL SCALE						
ERROR SOURCE	**CALCULATION**	**LT6370A**	**IA1**	**IA2**	**IA3**	**IA4**	**IA5**	**IA6**
Absolute Accuracy at T_A = 25°C								
Gain Error, %	Gain Error in % • 10k + 1000	1800	2500	2500	2000	6000	2500	1800
Input Offset Voltage, µV	V_{OSI}/20mV	1250	6250	1250	3500	2500	7500	3000
Output Offset Voltage, µV	[V_{OSO}/100]/20mV	83	500	100	300	250	350	150
Input Offset Current, nA	[(I_{OS})(350)/2]/20mV	6.1	18	3.5	17.5	43.75	43.75	4
CMRR, dB	[(CMRR in ppm)(5V)/20mV	125	791	79	158	250	250	790
	Total Accuracy Error	**3264.1**	**10059**	**3932.5**	**5975.5**	**9043.75**	**10643.75**	**5744**
Drift to 85°C								
Gain Drift, ppm/°C	(Gain Drift + 10ppm)(60°C)	2400	3600	3600	5400	6600	2700	3600
Input Offset Voltage Drift, µV/°C	[(V_{OSI} Drift)(60°C)]/20mV	900	3000	900	2700	1500	6000	1200
Output Offset Voltage Drift, µV/°C	[(V_{OSO} Drift)(60°C)]/100/20mV	45	450	150	270	600	300	180
	Total Drift Error	**3345**	**7050**	**4650**	**8370**	**8700**	**9000**	**4980**
Resolution								
Gain Nonlinearity, ppm of Full Scale		30	40	15	10	20	5	15
Typ 0.1Hz to 10Hz Voltage Noise, μV_{P-P}	(0.1Hz to 10Hz Noise)/20mV	10	14	12.5	3.5	10	26	14
	Total Resolution Error	**40**	**54**	**27.5**	**13.5**	**30**	**31**	**29**
	Grand Total Error	**6649.1**	**17163**	**8610**	**14359**	**17773.8**	**19674.8**	**10753**

G = 100

All errors are min/max and referred to input.

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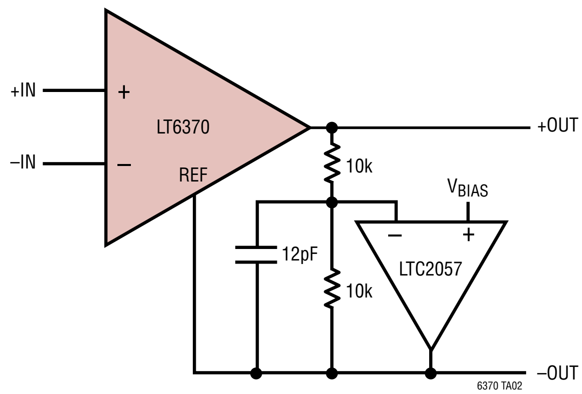
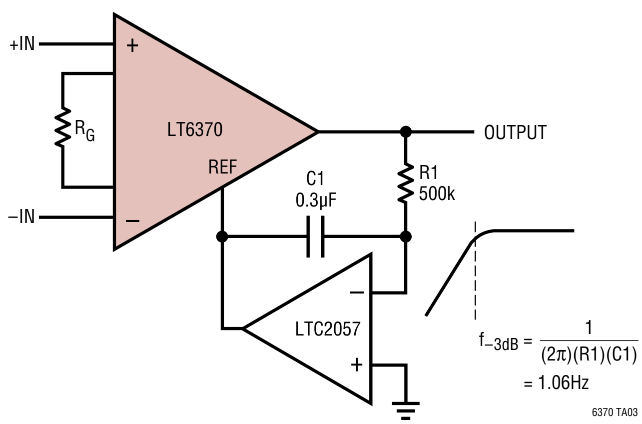
TYPICAL APPLICATIONS

Differential Output Instrumentation Amplifier

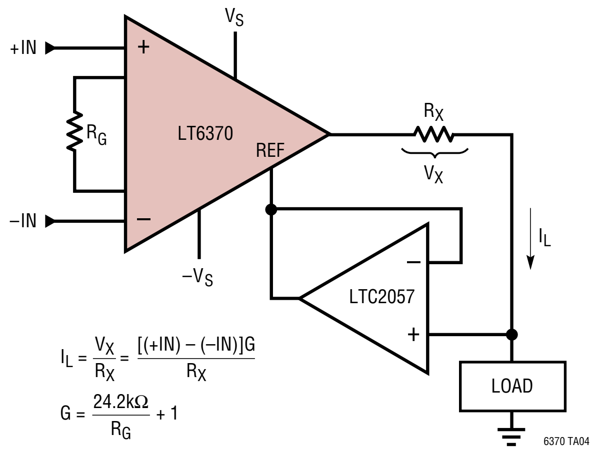


AC Coupled Instrumentation Amplifier

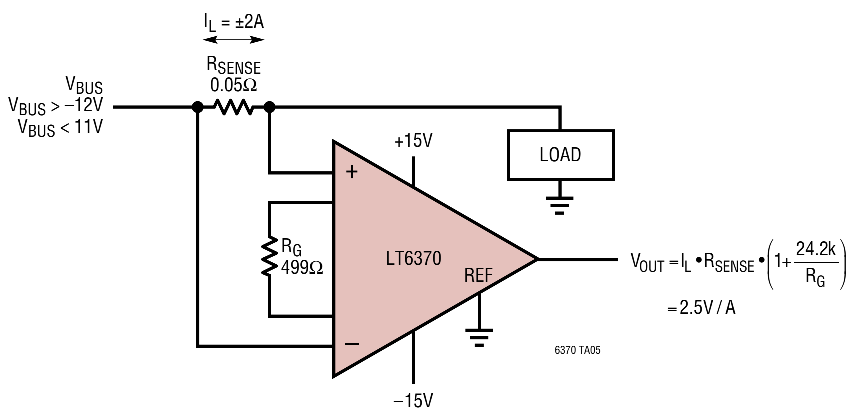


TYPICAL APPLICATIONS

Precision Voltage-to-Current Converter



High Side, Bidirectional Current Sense



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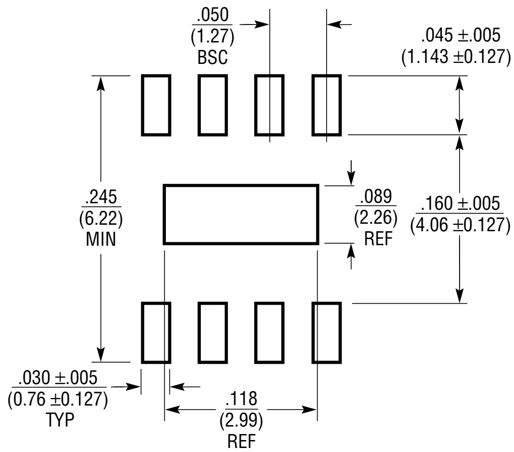
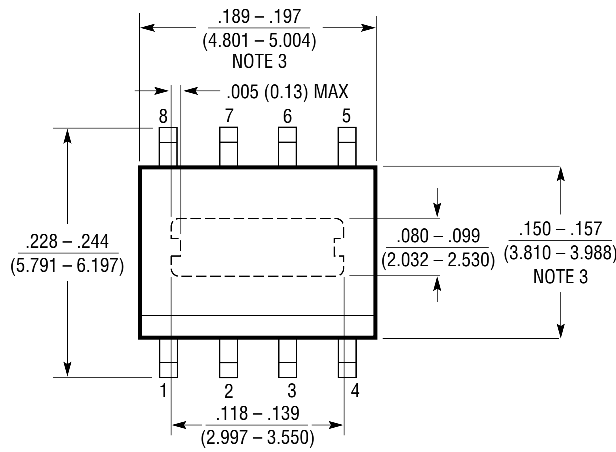
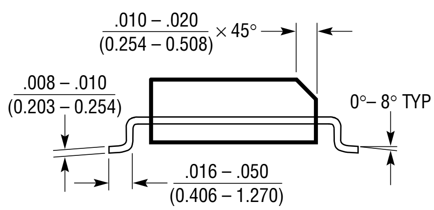
PACKAGE DESCRIPTION

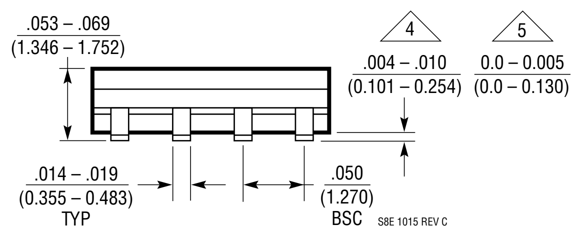
S8E Package
8-Lead Plastic SOIC (Narrow .150 Inch) Exposed Pad
(Reference LTC DWG # 05-08-1857 Rev C)



RECOMMENDED SOLDER PAD LAYOUT







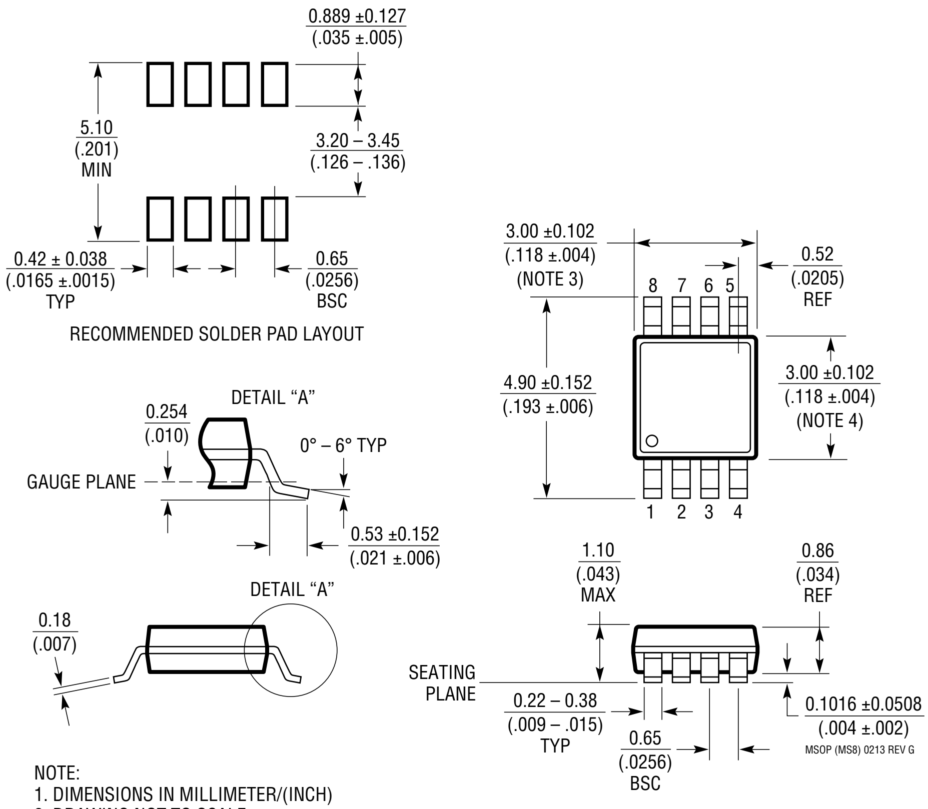
NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{\text{(MILLIMETERS)}}$
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010" (0.254mm)

4. STANDARD LEAD STANDOFF IS 4mils TO 10mils (DATE CODE BEFORE 542)

5. LOWER LEAD STANDOFF IS 0mils TO 5mils (DATE CODE AFTER 542)

PACKAGE DESCRIPTION

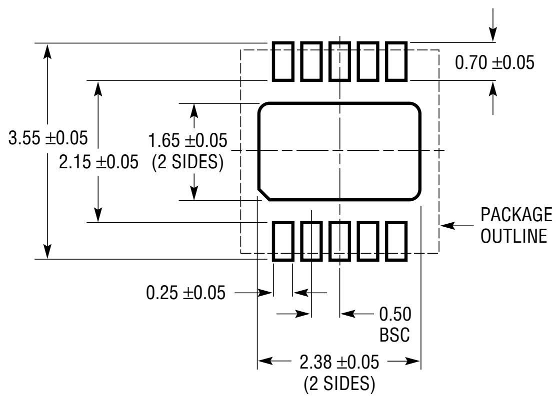
MS8 Package
8-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1660 Rev G)



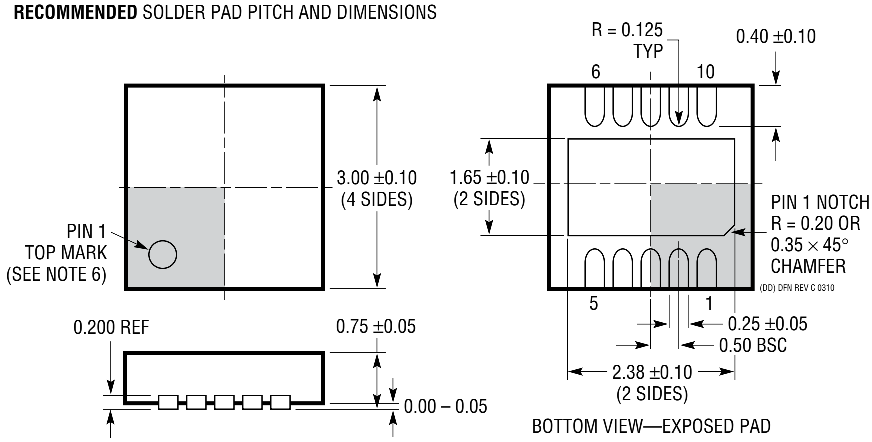
NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

PACKAGE DESCRIPTION

DD Package
10-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1699 Rev C)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-2). CHECK THE LTC WEBSITE DATA SHEET FOR CURRENT STATUS OF VARIATION ASSIGNMENT
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE