±230V Common Mode Voltage G = 10 Difference Amplifier

FEATURES

- ±230V Common Mode Voltage Range
- 105nV/√Hz Input Referred Noise (Resistor Divider = 3.1)
- 90dB Minimum CMRR
- 0.0075% (75ppm) Maximum Gain Error
- 1ppm/°C Maximum Gain Error Drift
- 2ppm Maximum Gain Nonlinearity
- Wide Supply Voltage Range: 3.3V to 50V
- Rail-to-Rail Output
- 350µA Supply Current
- Selectable Internal Resistor Divider Ratio
- 200µV Maximum Input Offset Voltage
- 300kHz –3dB Bandwidth (Resistor Divider = 3.1)
- 160kHz –3dB Bandwidth (Resistor Divider = 10.3)
- –40°C to 125°C Specified Temperature Range
- Low Power Shutdown: 20µA (DFN Package Only)
- Space-Saving MSOP and DFN Packages

APPLICATIONS

- High Side or Low Side Current Sensing
- Bidirectional Wide Common Mode Range Current Sensing
- High Voltage to Low Voltage Level Translation
- Precision Difference Amplifier
- Replacement for Isolation Circuits

DESCRIPTION

The LT®6376 is a gain of 10 difference amplifier which combines excellent DC precision, a very high input common mode range and a wide supply voltage range. It includes a precision op amp and a highly-matched thin film resistor network. It features excellent CMRR, extremely low gain error and extremely low gain drift.

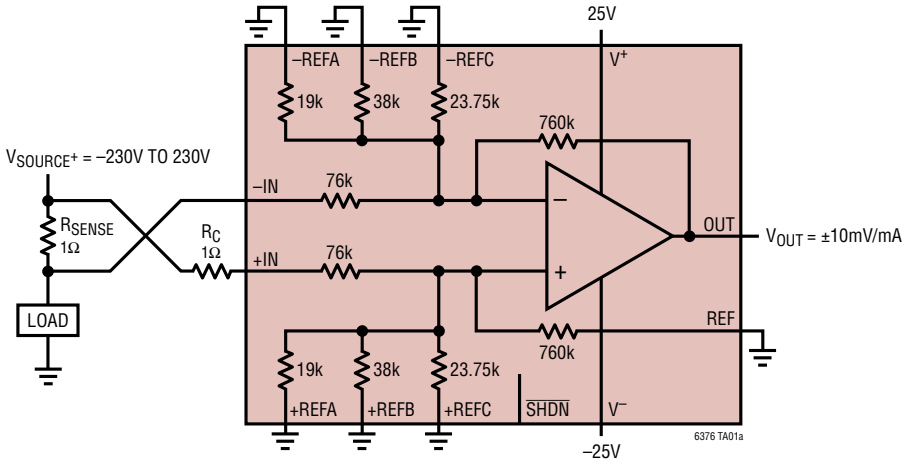
Comparing the LT6376 to existing difference amplifiers with high common mode voltage range, the gain of 10 and selectable resistor divider ratios of the LT6376 offer superior system performance by allowing the user to achieve low input referred noise with maximum precision and speed.

The op amp at the core of the LT6376 has Over-The-Top® protected inputs which allow for robust operation in environments with unpredictable voltage conditions. See the Applications Information section for more details.

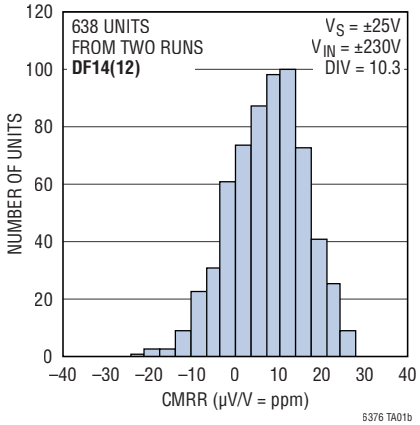
The LT6376 is specified over the –40°C to 125°C temperature range and is available in space-saving MSOP16 and DFN14 packages.

TYPICAL APPLICATION

Precision Wide Voltage Range, Bidirectional Current Monitor



Typical Distribution of CMRR



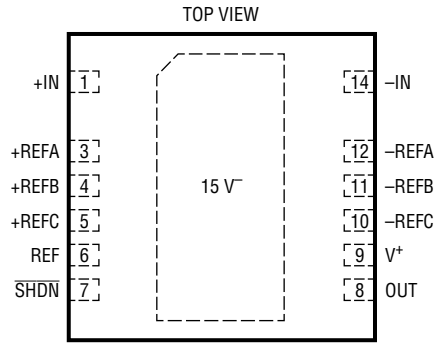
ABSOLUTE MAXIMUM RATINGS

(Note 1)

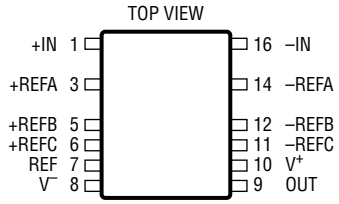
Supply Voltages
(V^+ to V^-) 60V
+IN, –IN, (Note 2)
Each Input ..... ±240V
Differential ..... ±480V
+REFA, –REFA, +REFB, –REFB, +REFC, –REFC,
REF, $\overline{SHDN}$ (Note 2) ..... (V^+ + 0.3V) to (V^- –0.3V)
Output Current (Continuous) (Note 6) 50mA

Output Short-Circuit Duration (Note 3) Thermally Limited
Temperature Range (Notes 4, 5)
LT6376I ..... –40°C to 85°C
LT6376H ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
MSOP Lead Temperature (Soldering, 10 sec)..... 300°C

PIN CONFIGURATION



DF PACKAGE
14(12)-LEAD (4mm × 4mm) PLASTIC DFN
T_{JMAX} = 150°C, θ_{JA} = 43°C/W, θ_{JC} = 4°C/W
EXPOSED PAD (PIN 15) IS V^-, MUST BE SOLDERED TO PCB



MS PACKAGE
VARIATION: MS16 (12)
16-LEAD PLASTIC MSOP
T_{JMAX} = 150°C, θ_{JA} = 130°C/W

ORDER INFORMATION

http://www.linear.com/product/LT6376#orderinfo

TUBE	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT6376IDF#PBF	LT6376IDF#TRPBF	6376	14-Lead (4mm × 4mm) Plastic DFN	–40°C to 85°C
LT6376HDF#PBF	LT6376HDF#TRPBF	6376	14-Lead (4mm × 4mm) Plastic DFN	–40°C to 125°C
LT6376IMS#PBF	LT6376IMS#TRPBF	6376	16-Lead Plastic MSOP	–40°C to 85°C
LT6376HMS#PBF	LT6376HMS#TRPBF	6376	16-Lead Plastic MSOP	–40°C to 125°C

*The temperature grade is identified by a label on the shipping container.
Consult ADI Marketing for parts specified with wider operating temperature ranges. Parts ending with PBF are RoHS and WEEE compliant.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, –40°C < T_A < 85°C for I-grade parts, –40°C < T_A < 125°C for H-grade parts, otherwise specifications are at T_A = 25°C, V^+ = 15V, V^- = –15V, V_{CM} = V_{OUT} = V_{REF} = 0V. V_{CMOP} is the common mode voltage of the internal op amp. For Resistor Divider Ratio = 3.1, ±REFA = ± REFC = OPEN, ±REFB = 0V. For Resistor Divider Ratio = 8.3, ±REFA = ±REFC = 0V, ±REFB = OPEN. For Resistor Divider Ratio = 10.3, ±REFA = ±REFB = ±REFC = 0V.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
G	Gain	V_{OUT} = ±10V			10		V/V
ΔG	Gain Error, MS16 Package	V_{OUT} = ±10V	 ●		±0.002	±0.0075 ±0.0085	% %
ΔG	Gain Error, DF14 Package	V_{OUT} = ±10V	 ●		±0.002	±0.0085 ±0.0095	% %
ΔG/ΔT	Gain Drift vs Temperature (Note 6)	V_{OUT} = ±10V	●		±0.2	±1	ppm/°C
GNL	Gain Nonlinearity	V_{OUT} = ±10V	 ●		±1	±2 ±3	ppm ppm
V_{OS}	Input Offset Voltage	V^- < V_{CMOP} < V^+ –1.75V Resistor Divider Ratio = 3.1 Resistor Divider Ratio = 3.1 Resistor Divider Ratio = 8.3 Resistor Divider Ratio = 8.3 Resistor Divider Ratio = 10.3 Resistor Divider Ratio = 10.3	 ● ● ●		 50 120 160 	 200 600 500 1600 600 2000	 µV µV µV µV µV µV
$ΔV_{OS}/ΔT$	Input Offset Voltage Drift (Note 6)	V^- < V_{CMOP} < V^+ –1.75V Resistor Divider Ratio = 3.1 Resistor Divider Ratio = 10.3	 ● ●		 1.5 5	 4 12	 µV/°C µV/°C
R_{IN}	Input Impedance (Note 8)	Common Mode Resistor Divider Ratio = 3.1 Resistor Divider Ratio = 8.3 Resistor Divider Ratio = 10.3 Differential	 ● ● ● ●	 47 36 35 128	 56 43 42 152	 65 50 49 176	 kΩ kΩ kΩ kΩ
CMRR	Common Mode Rejection Ratio, MS16 Package	Resistor Divider Ratio = 3.1, V_{CM} = ±28V	 ●	90 88	98		dB dB
		Resistor Divider Ratio = 8.3, V_{CM} = ±28V	 ●	90 88	98		dB dB
		Resistor Divider Ratio = 10.3, V_{CM} = ±28V	 ●	90 88	98		dB dB
CMRR	Common Mode Rejection Ratio, DF14 Package	Resistor Divider Ratio = 3.1, V_{CM} = ±28V	 ●	88 86	95		dB dB
		Resistor Divider Ratio = 8.3, V_{CM} = ±28V	 ●	88 86	95		dB dB
		Resistor Divider Ratio = 10.3, V_{CM} = ±28V	 ●	88 86	95		dB dB
		Resistor Divider Ratio = 10.3, V_{CM} = ±150V, V_S = ±25V, T_A = –40°C to 125°C	 ●	90 86	96		dB dB
		Resistor Divider Ratio = 10.3, V_{CM} = ±230V, V_S = ±25V, T_A = –40°C to 85°C	 ●	90 89	96		dB dB
V_{CM}	Input Voltage Range (Note 7)		●	–230		230	V
PSRR	Power Supply Rejection Ratio (Input Referred)	V_S = ±1.65V to ±25V, V_{CM} = V_{OUT} = Mid-Supply Resistor Divider Ratio = 3.1 Resistor Divider Ratio = 8.3 Resistor Divider Ratio = 10.3	 ● ● ●	 105 98 96	 120 110 107	 	 dB dB dB
e_{ni}	Input Referred Noise Voltage Density	f = 1kHz Resistor Divider Ratio = 3.1 Resistor Divider Ratio = 10.3			 105 245	 	 nV/√Hz nV/√Hz

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, –40°C < T_A < 85°C for I-grade parts, –40°C < T_A < 125°C for H-grade parts, otherwise specifications are at T_A = 25°C, V^+ = 15V, V^- = –15V, V_{CM} = V_{OUT} = V_{REF} = 0V. V_{CMOP} is the common mode voltage of the internal op amp. For Resistor Divider Ratio = 3.1, ±REFA = ± REFC = OPEN, ±REFB = 0V. For Resistor Divider Ratio = 8.3, ±REFA = ±REFC = 0V, ±REFB = OPEN. For Resistor Divider Ratio = 10.3, ±REFA = ±REFB = ±REFC = 0V.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Input Referred Noise Voltage	f = 0.1Hz to 10Hz Resistor Divider Ratio = 3.1 Resistor Divider Ratio = 10.3			 4 10		 μV_{P-P} μV_{P-P}
V_{OL}	Output Voltage Swing Low (Referred to V^-)	No Load I_{SINK} = 5mA	● ●		5 280	50 500	mV mV
V_{OH}	Output Voltage Swing High (Referred to V^+)	No Load I_{SOURCE} = 5mA	● ●		5 400	20 750	mV mV
I_{SC}	Short-Circuit Output Current	50Ω to V^+ 50Ω to V^-	● ●	10 10	28 30		mA mA
SR	Slew Rate	ΔV_{OUT} = ±5V	●	2.2	4.1		V/µs
BW	Small Signal –3dB Bandwidth	Resistor Divider Ratio = 3.1 Resistor Divider Ratio = 8.3 Resistor Divider Ratio = 10.3			300 190 160		kHz kHz kHz
t_S	Settling Time	Resistor Divider Ratio = 3.1 0.01%, ΔV_{OUT} = 10V 0.1%, ΔV_{OUT} = 10V 0.01%, ΔV_{CM} = 10V, ΔV_{DIFF} = 0V			 41 26 15		 µs µs µs
		Resistor Divider Ratio = 10.3 0.01%, ΔV_{OUT} = 10V 0.1%, ΔV_{OUT} = 10V 0.01%, ΔV_{CM} = 10V, ΔV_{DIFF} = 0V			 26 16 5		 µs µs µs
V_S	Supply Voltage		 ●	3 3.3		50 50	V V
t_{ON}	Turn-On Time				16		µs
V_{IL}	$\overline{SHDN}$ Input Logic Low (Referred to V^+)		●			–2.5	V
V_{IH}	$\overline{SHDN}$ Input Logic High (Referred to V^+)		●	–1.2			V
$I_{\overline{SHDN}}$	$\overline{SHDN}$ Pin Current		●		–10	–15	µA
I_S	Supply Current	Active, $V_{\overline{SHDN}} \geq V^+ - 1.2V$ Active, $V_{\overline{SHDN}} \geq V^+ - 1.2V$ Shutdown, $V_{\overline{SHDN}} \leq V^+ - 2.5V$ Shutdown, $V_{\overline{SHDN}} \leq V^+ - 2.5V$	 ● ●		350 20 	400 600 25 70	µA µA µA µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, –40°C < T_A < 85°C for I-grade parts, –40°C < T_A < 125°C for H-grade parts, otherwise specifications are at T_A = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = V_{OUT} = V_{REF} = Mid-Supply. V_{CMOP} is the common mode voltage of the internal op amp. For Resistor Divider Ratio = 3.1, ±REFA = ±REFC = OPEN, ±REFB = Mid-Supply. For Resistor Divider Ratio = 8.3, ±REFA = ±REFC = Mid-Supply, ±REFB = OPEN. For Resistor Divider Ratio = 10.3, ±REFA = ±REFB = ±REFC = Mid-Supply.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
G	Gain	V_{OUT} = 1V to 4V			10		V/V
ΔG	Gain Error, MS16 Package	V_{OUT} = 1V to 4V	 ●		±0.002	±0.01 ±0.012	% %
ΔG	Gain Error, DF14 Package	V_{OUT} = 1V to 4V	 ●		±0.002	±0.012 ±0.013	% %
ΔG/ΔT	Gain Drift vs Temperature (Note 6)	V_{OUT} = 1V to 4V	●		±0.2	±1	ppm/°C
GNL	Gain Nonlinearity	V_{OUT} = 1V to 4V			±1		ppm
V_{OS}	Input Offset Voltage	0 < V_{CMOP} < V^+ –1.75V Resistor Divider Ratio = 3.1 Resistor Divider Ratio = 3.1 Resistor Divider Ratio = 8.3 Resistor Divider Ratio = 8.3 Resistor Divider Ratio = 10.3 Resistor Divider Ratio = 10.3	 ● ● ●		 50 120 160 	 200 600 500 1600 600 2000	 µV µV µV µV µV µV
$ΔV_{OS}/ΔT$	Input Offset Voltage Drift (Note 6)	0 < V_{CMOP} < V^+ –1.75V Resistor Divider Ratio = 3.1 Resistor Divider Ratio = 10.3	 ● ●		 1.5 5	 4 12	 µV/°C µV/°C
R_{IN}	Input Impedance (Note 8)	Common Mode Resistor Divider Ratio = 3.1 Resistor Divider Ratio = 8.3 Resistor Divider Ratio = 10.3 Differential	 ● ● ● ●	 47 36 35 128	 56 43 42 152	 65 50 49 176	 kΩ kΩ kΩ kΩ
CMRR	Common Mode Rejection Ratio, MS16 Package	Resistor Divider Ratio = 3.1 V_{CM} = –5.25V to +4.825V	 ●	90 87	97		dB dB
		Resistor Divider Ratio = 8.3 V_{CM} = –18.25V to +8.725V	 ●	90 87	97		dB dB
		Resistor Divider Ratio = 10.3 V_{CM} = –23.25V to +10.225V	 ●	90 87	97		dB dB
CMRR	Common Mode Rejection Ratio, DF14 Package	Resistor Divider Ratio = 3.1 V_{CM} = –5.25V to +4.825V	 ●	86 85	94		dB dB
		Resistor Divider Ratio = 8.3 V_{CM} = –18.25V to +8.725V	 ●	86 85	94		dB dB
		Resistor Divider Ratio = 10.3 V_{CM} = –23.25V to +10.225V	 ●	86 85	94		dB dB
PSRR	Power Supply Rejection Ratio (Input Referred)	V_S = ±1.65V to ±25V, V_{CM} = V_{OUT} = Mid-Supply Resistor Divider Ratio = 3.1 Resistor Divider Ratio = 8.3 Resistor Divider Ratio = 10.3	 ● ● ●	 105 98 96	 120 110 107	 	 dB dB dB
e_{ni}	Input Referred Noise Voltage Density	f = 1kHz Resistor Divider Ratio = 3.1 Resistor Divider Ratio = 10.3			 105 245	 	 nV/√Hz nV/√Hz
	Input Referred Noise Voltage	f = 0.1Hz to 10Hz Resistor Divider Ratio = 3.1 Resistor Divider Ratio = 10.3			 4 10	 	 $µV_{P-P}$ $µV_{P-P}$
V_{OL}	Output Voltage Swing Low (Referred to V^-)	No Load I_{SINK} = 5mA	● ●		5 280	50 500	mV mV
V_{OH}	Output Voltage Swing High (Referred to V^+)	No Load I_{SOURCE} = 5mA	● ●		5 400	20 750	mV mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, –40°C < T_A < 85°C for I-grade parts, –40°C < T_A < 125°C for H-grade parts, otherwise specifications are at T_A = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = V_{OUT} = V_{REF} = Mid-Supply. V_{CMOP} is the common mode voltage of the internal op amp. For Resistor Divider Ratio = 3.1, ±REFA = ±REFC = OPEN, ±REFB = Mid-Supply. For Resistor Divider Ratio = 8.3, ±REFA = ±REFC = Mid-Supply, ±REFB = OPEN. For Resistor Divider Ratio = 10.3, ±REFA = ±REFB = ±REFC = Mid-Supply.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{SC}	Short-Circuit Output Current	50Ω to V^+ 50Ω to V^-	● ●	10 10	27 25		mA mA
SR	Slew Rate	ΔV_{OUT} = 3V	●	1.9	3		V/µs
BW	Small Signal –3dB Bandwidth	Resistor Divider Ratio = 3.1 Resistor Divider Ratio = 8.3 Resistor Divider Ratio = 10.3			300 190 160		kHz kHz kHz
t_S	Settling Time	Resistor Divider Ratio = 3.1 0.01%, ΔV_{OUT} = 2V 0.1%, ΔV_{OUT} = 2V 0.01%, ΔV_{CM} = 2V, ΔV_{DIFF} = 0V			 34 20 10		 µs µs µs
		Resistor Divider Ratio = 10.3 0.01%, ΔV_{OUT} = 2V 0.1%, ΔV_{OUT} = 2V 0.01%, ΔV_{CM} = 2V, ΔV_{DIFF} = 0V			 40 16 5		 µs µs µs
V_S	Supply Voltage		 ●	3 3.3		50 50	V V
t_{ON}	Turn-On Time				22		µs
V_{IL}	$\overline{SHDN}$ Input Logic Low (Referred to V^+)		●			–2.5	V
V_{IH}	$\overline{SHDN}$ Input Logic High (Referred to V^+)		●	–1.2			V
$I_{\overline{SHDN}}$	$\overline{SHDN}$ Pin Current		●		–10	–15	µA
I_S	Supply Current	Active, $V_{\overline{SHDN}} \geq V^+ - 1.2V$ Active, $V_{\overline{SHDN}} \geq V^+ - 1.2V$ Shutdown, $V_{\overline{SHDN}} \leq V^+ - 2.5V$ Shutdown, $V_{\overline{SHDN}} \leq V^+ - 2.5V$	 ● ●		330 15 	370 525 20 40	µA µA µA µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: See Common Mode Voltage Range in the Applications Information section of this data sheet for other considerations when taking +IN/–IN pins to ±240V. All other pins should not be taken more than 0.3V beyond the supply rails.

Note 3: A heat sink may be required to keep the junction temperature below absolute maximum. This depends on the power supply, input voltages and the output current.

Note 4: The LT6376I is guaranteed functional over the operating temperature range of –40°C to 85°C. The LT6376H is guaranteed functional over the operating temperature range of –40°C to 125°C.

Note 5: The LT6376I is guaranteed to meet specified performance from –40°C to 85°C. The LT6376H is guaranteed to meet specified performance from –40°C to 125°C.

Note 6: This parameter is not 100% tested.

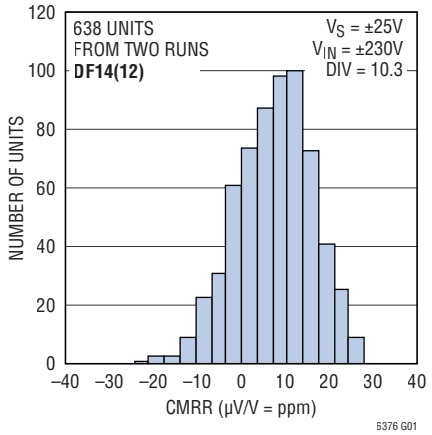
Note 7: Input voltage range is guaranteed by the CMRR test at V_S = ±25V and all REF pins at ground (Resistor Divider Ratio = 10.3). For the other voltages, this parameter is guaranteed by design and through correlation with the ±25V test. See Common Mode Voltage Range in the Applications Information section to determine the valid input voltage range under various operating conditions.

Note 8: Input impedance is tested by a combination of direct measurement and correlation to the CMRR and gain error tests.

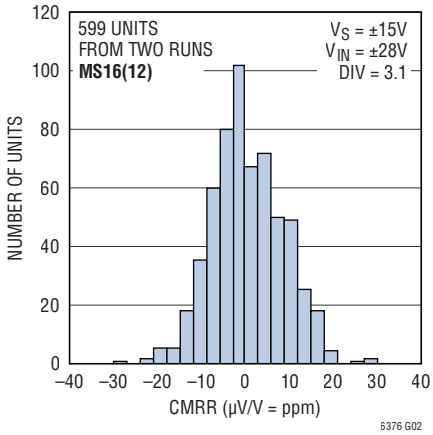
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_S = ±15V, unless otherwise noted.

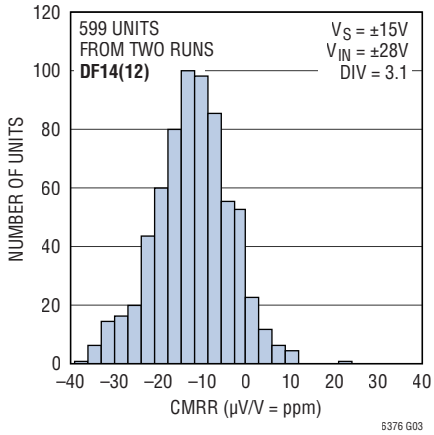
Typical Distribution of CMRR



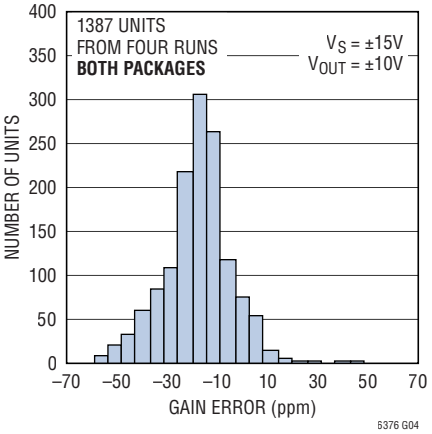
Typical Distribution of CMRR



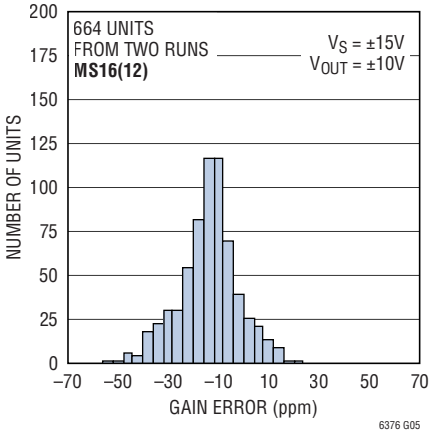
Typical Distribution of CMRR



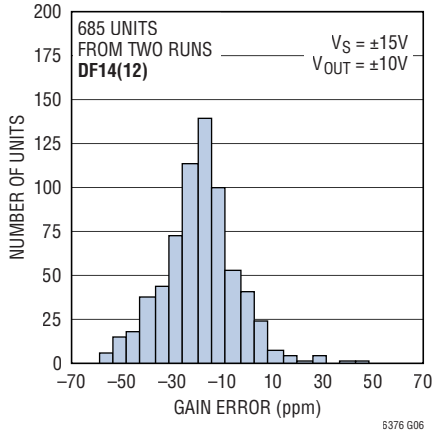
Typical Distribution of Gain Error



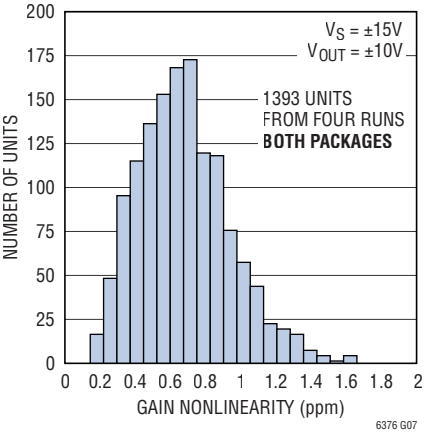
Typical Distribution of Gain Error



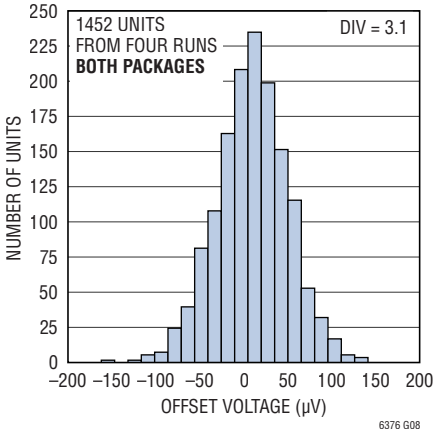
Typical Distribution of Gain Error



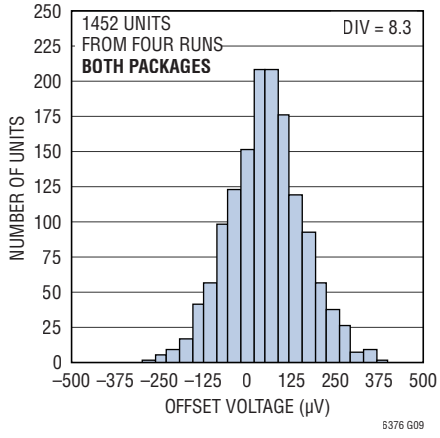
Typical Distribution of Gain Nonlinearity



Typical Distribution of Input Offset Voltage



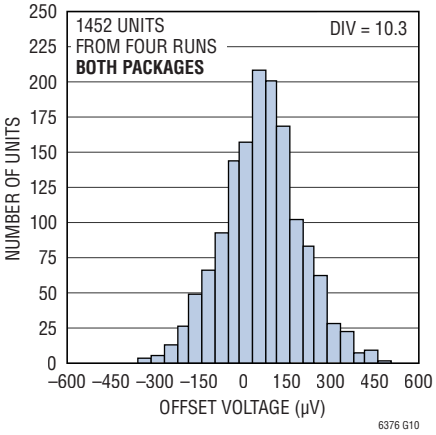
Typical Distribution of Input Offset Voltage



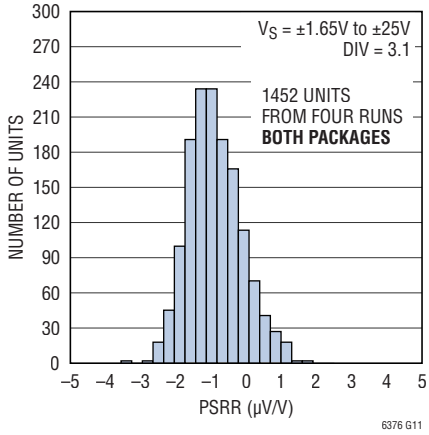
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_S = ±15V, unless otherwise noted.

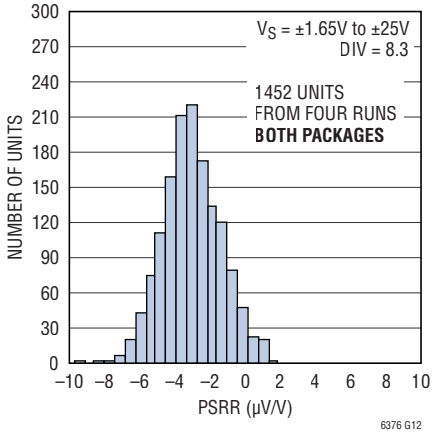
Typical Distribution of Input Offset Voltage



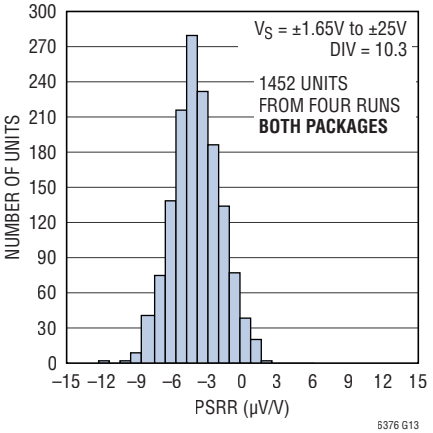
Typical Distribution of PSRR (Input Referred)



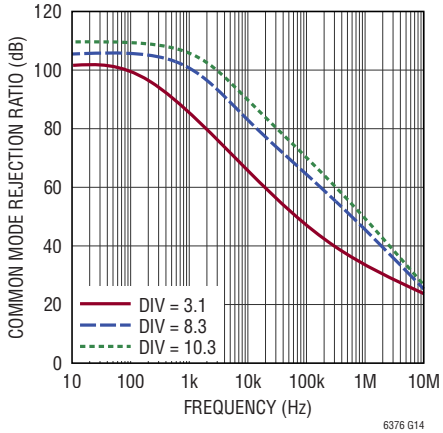
Typical Distribution of PSRR (Input Referred)



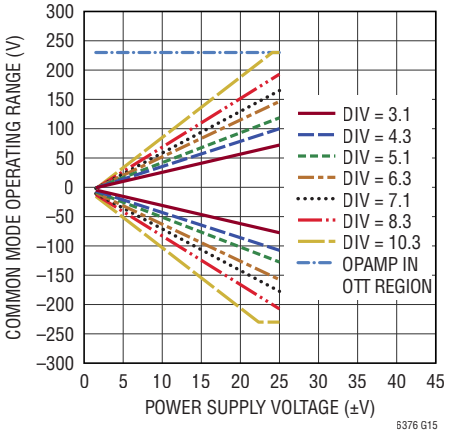
Typical Distribution of PSRR (Input Referred)



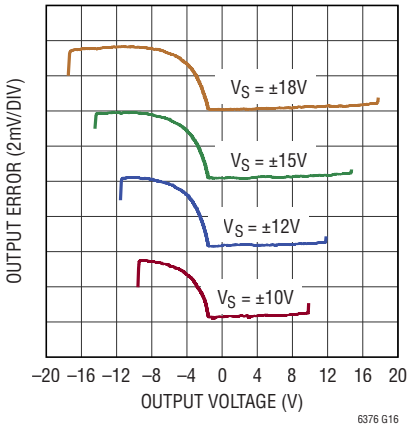
CMRR vs Frequency



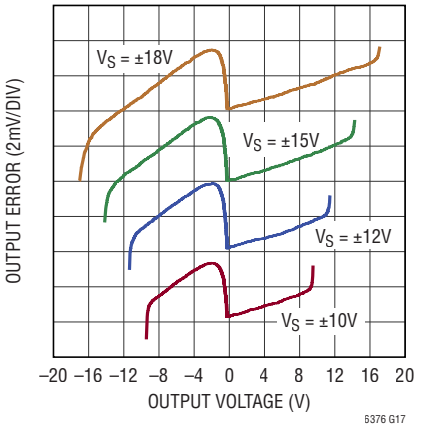
Common Mode Voltage Range vs Power Supply Voltage



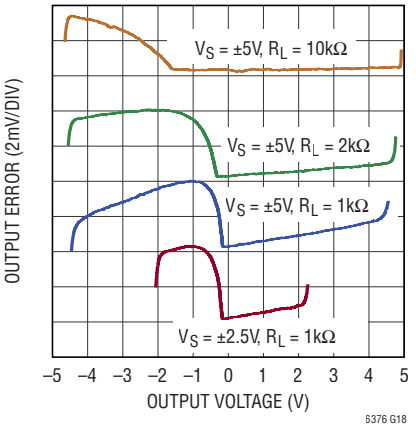
Typical Gain Error for R_L = 10kΩ (Curves Offset for Clarity)



Typical Gain Error for R_L = 2kΩ (Curves Offset for Clarity)



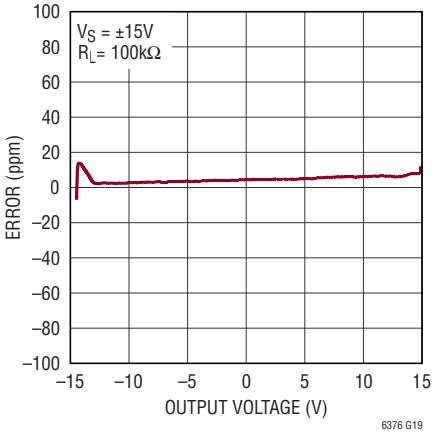
Typical Gain Error for Low Supply Voltages (Curves Offset for Clarity)



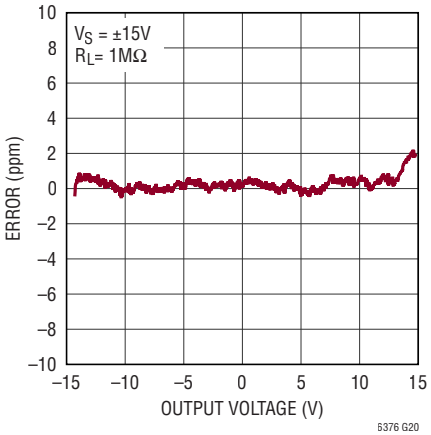
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_S = ±15V, unless otherwise noted.

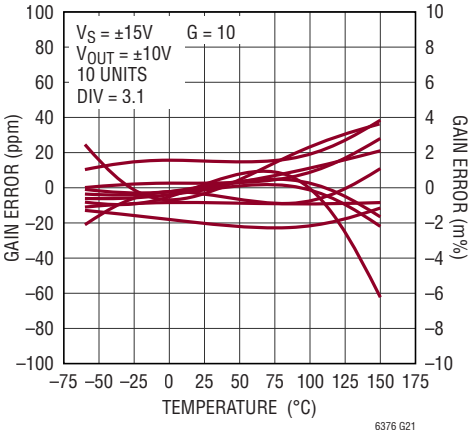
Gain Nonlinearity



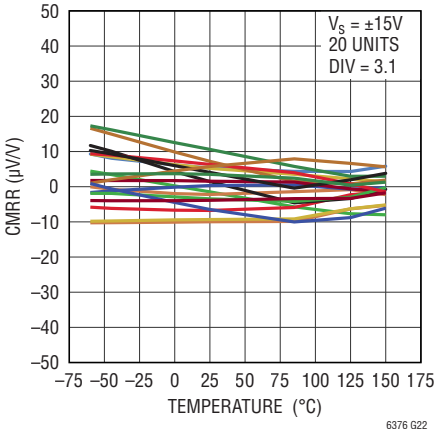
Gain Nonlinearity



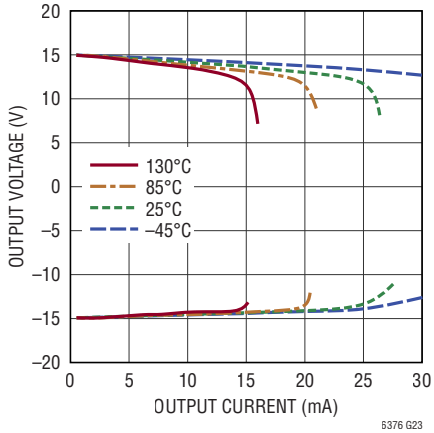
Gain Error vs Temperature



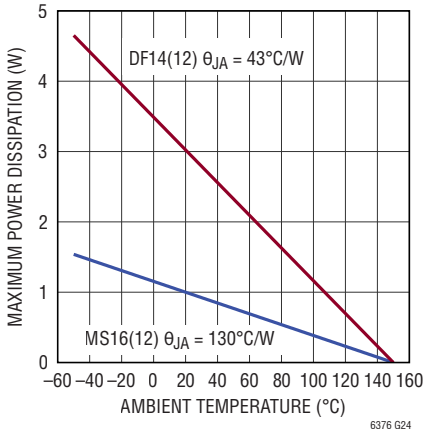
CMRR vs Temperature



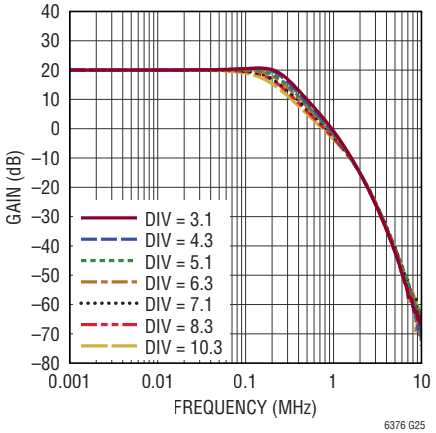
Output Voltage vs Load Current



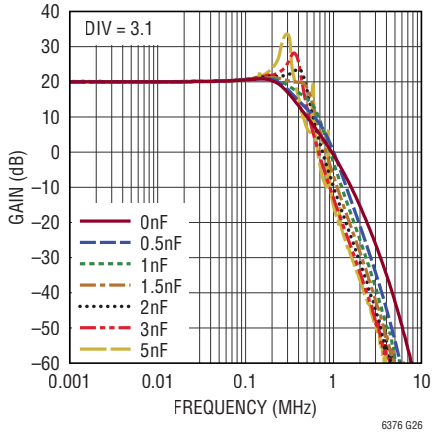
Maximum Power Dissipation vs Temperature



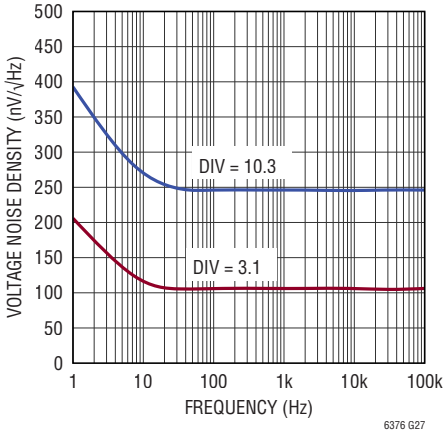
Gain vs Frequency



Frequency Response vs Capacitive Load



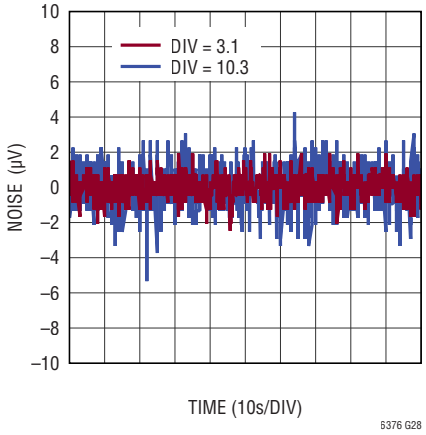
Input Referred Noise Density vs Frequency



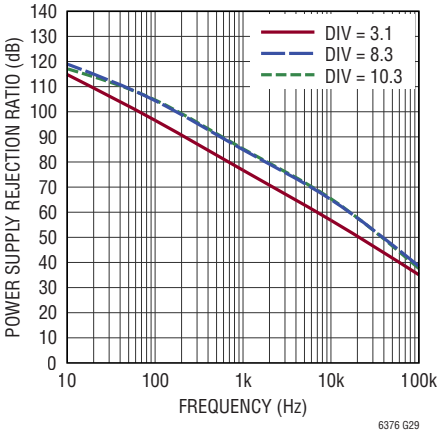
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_S = ±15V, unless otherwise noted.

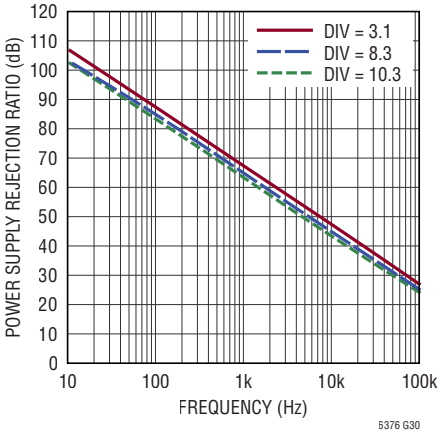
0.1Hz to 10Hz Noise (Input Referred)



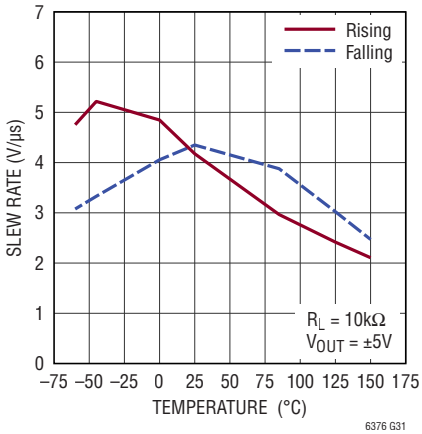
Positive PSRR vs Frequency



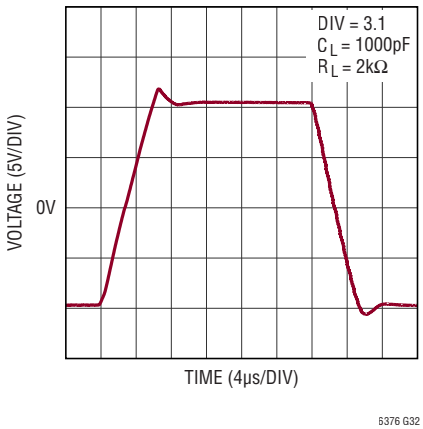
Negative PSRR vs Frequency



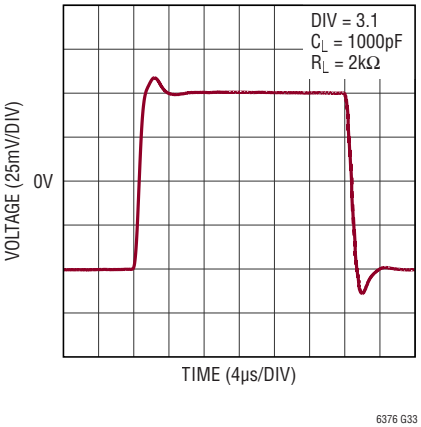
Slew Rate vs Temperature



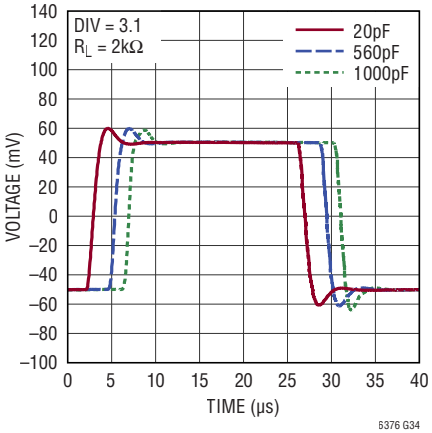
Large-Signal Step Response



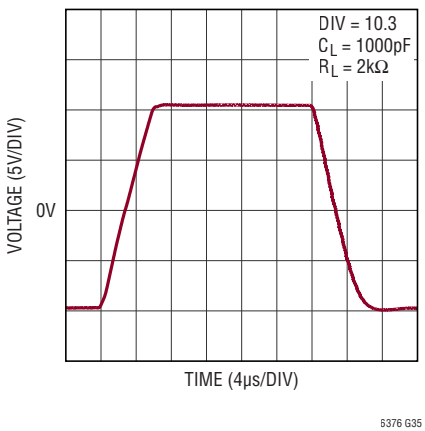
Small-Signal Step Response



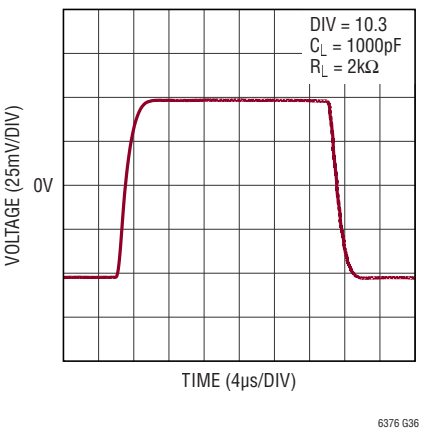
Small-Signal Step Response vs Capacitive Load



Large-Signal Step Response



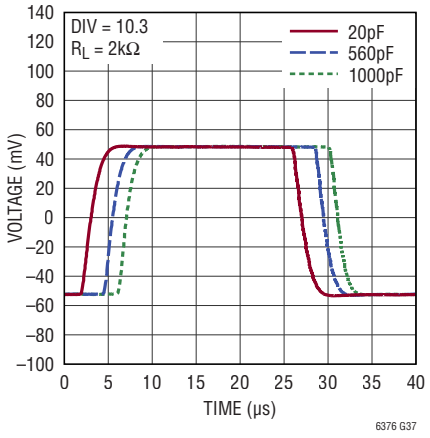
Small-Signal Step Response



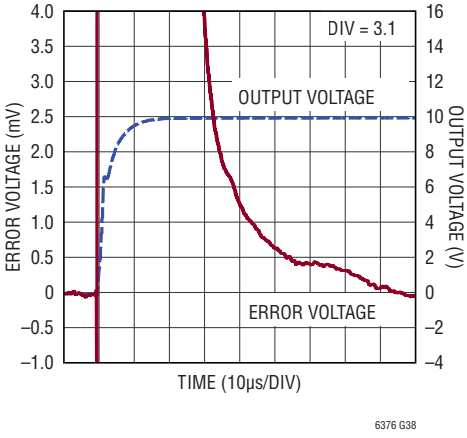
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_S = ±15V, unless otherwise noted.

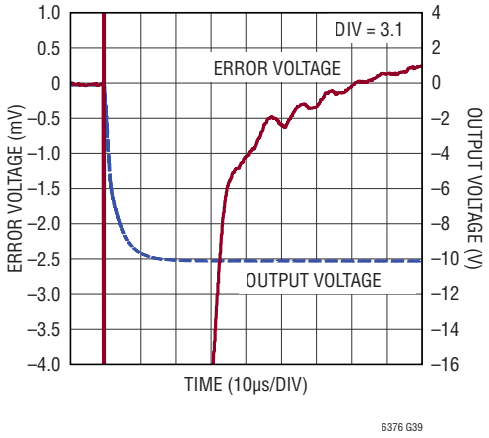
Small-Signal Step Response vs Capacitive Load



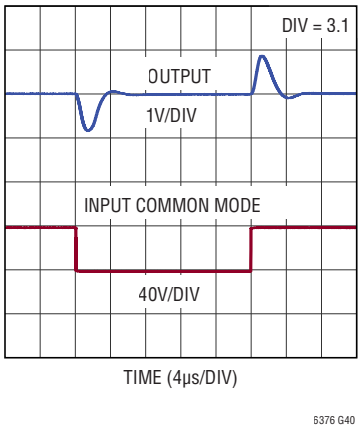
Settling Time



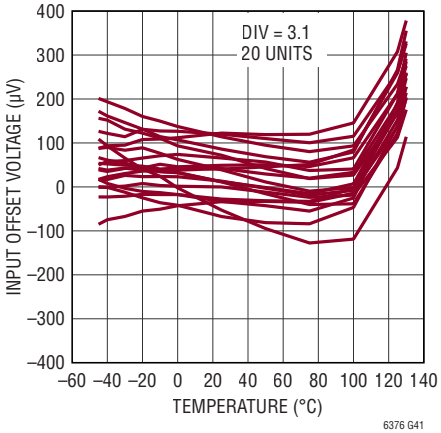
Settling Time



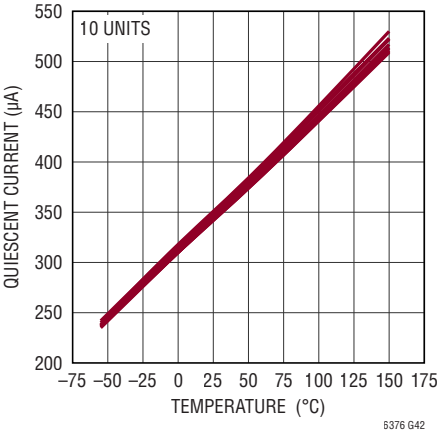
Input Common Mode Step Response



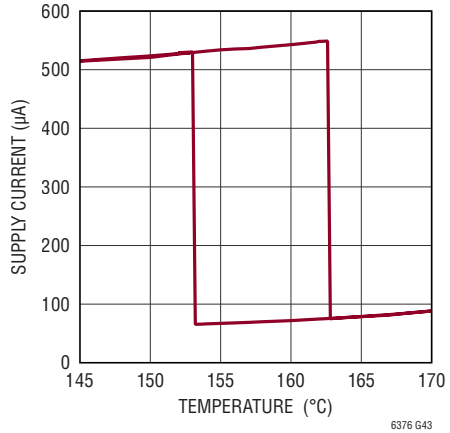
Input Offset Voltage vs Temperature



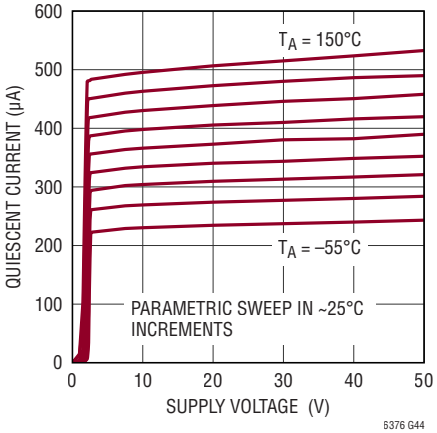
Quiescent Current vs Temperature



Thermal Shutdown Hysteresis



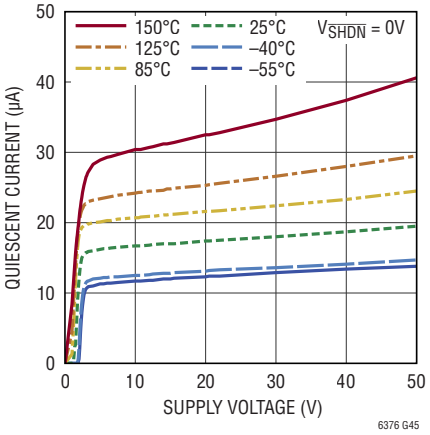
Quiescent Current vs Supply Voltage



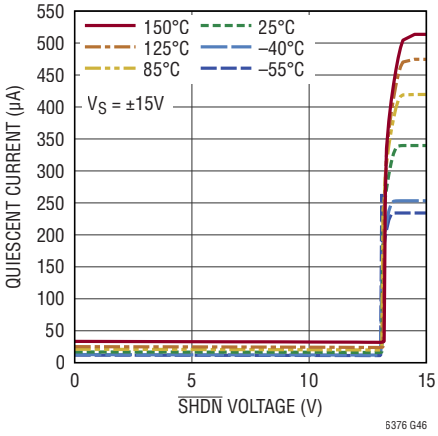
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_S = ±15V, unless otherwise noted.

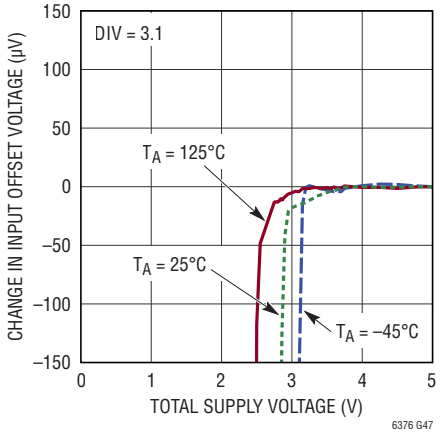
Shutdown Quiescent Current vs Supply Voltage



Quiescent Current vs $\overline{SHDN}$ Voltage



Minimum Supply Voltage



PIN FUNCTIONS (DFN/MSOP)

V^+ (Pin 9/Pin 10): Positive Supply Pin.

V^- (Exposed Pad Pin 15/Pin 8): Negative Supply Pin.

OUT (Pin 8/Pin 9): Output Pin.

+IN (Pin 1/Pin 1): Noninverting Input Pin. Accepts input voltages from 230V to –230V.

+REFA (Pin 3/Pin 3): Reference Pin A. Sets the input common mode range and the output noise and offset.

+REFB (Pin 4/Pin 5): Reference Pin B. Sets the input common mode range and the output noise and offset.

+REFC (Pin 5/Pin 6): Reference Pin C. Sets the input common mode range and the output noise and offset.

–IN (Pin 14/Pin 16): Inverting Input Pin. Accepts input voltages from 230V to –230V.

–REFA (Pin 12/Pin 14): Reference Pin A. Sets the input common mode range and the output noise and offset.

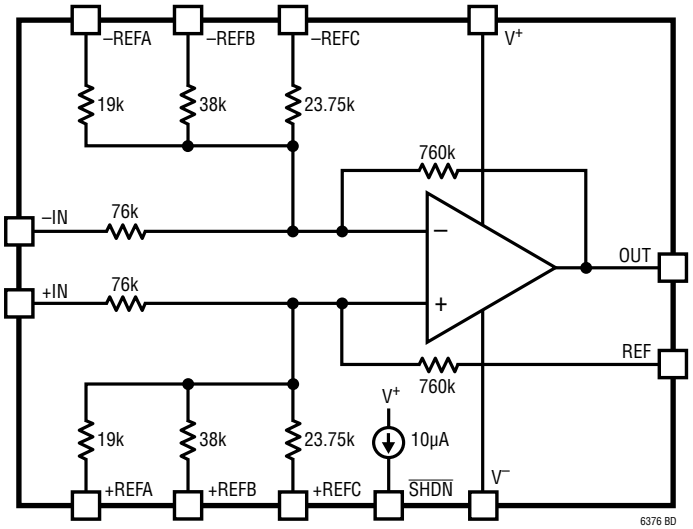
–REFB (Pin 11/Pin 12): Reference Pin B. Sets the input common mode range and the output noise and offset.

–REFC (Pin 10/Pin 11): Reference Pin C. Sets the input common mode range and the output noise and offset.

REF (Pin 6/Pin 7): Reference Input. Sets the output level when the difference between the inputs is zero.

$\overline{\text{SHDN}}$ (Pin 7) DFN Only: Shutdown Pin. Amplifier is active when this pin is tied to V^+ or left floating. Pulling the pin >2.5V below V^+ causes the amplifier to enter a low power state.

BLOCK DIAGRAM



APPLICATIONS INFORMATION

TRANSFER FUNCTION

The LT6376 is a gain of 10 difference amplifier with the transfer function:

$$V_{OUT} = 10 \bullet (V_{+IN} – V_{–IN}) + V_{REF}$$

The voltage on the REF pin sets the output voltage when the differential input voltage ($V_{DIFF} = V_{+IN} – V_{–IN}$) is zero. This reference is used to shift the output voltage to the desired input level of the next stage of the signal chain.

BENEFITS OF SELECTABLE RESISTOR DIVIDER RATIOS

The LT6376 offers smaller package size, better gain accuracy and better noise performance than existing high common mode voltage range difference amplifiers. Additionally, the LT6376 allows users to maximize system performance by selecting the resistor divider ratio (DIV) appropriate to their input common mode voltage range. A higher resistor divider ratio (DIV) enables a higher common mode voltage range at the input pins, but it also increases output noise and output offset/drift and decreases the –3dB bandwidth. Therefore, a trade-off exists between input range and DC, AC, and drift performance of the part. It is recommended to use the lowest resistor divider ratio that achieves the required input common mode voltage range of the application in order to maximize the system SNR, precision and speed.

Table 1 shows the noise, offset/drift, and –3dB bandwidth of the LT6376 in gain of 10 configurations.

COMMON MODE VOLTAGE RANGE

The wide common mode voltage range of the LT6376 is enabled by both a resistor divider at the input of the op amp and by an internal op amp that can withstand high input voltages.

The internal resistor network of the LT6376 divides down the input common mode voltage. The resulting voltage at the op amp inputs determines the op amp's operating region. In the configuration shown in Figure 1, a resistor divider is created at both op amp inputs by the 76k input resistor and the resistance from each input to ground, which is ~36.19k. The resistance to ground is formed by the 38k (REFB resistors) in parallel with the 760k (feedback/REF resistor). The result is a divide by 3.1 of the input voltage. As shown in Tables 1 to 5, different connections to reference pins (i.e. pins +REFA, –REFA,

APPLICATIONS INFORMATION

Table 1. LT6376 Performance at Different Resistor Divider Ratios

RESISTOR DIVIDER OPTIONS				RESISTOR DIVIDER RATIO (DIV)	DIFFERENTIAL GAIN	INPUT NOISE AT 1kHz (nV/√Hz)	MAXIMUM INPUT OFFSET (µV)	MAXIMUM INPUT OFFSET DRIFT (µV/°C)	–3dB BANDWIDTH (kHz)
+REFA AND –REFA	+REFB AND –REFB	+REFC AND –REFC	REF						
19k	38k	23.75k	760k						
OPEN	GND	OPEN	REF	3.1	10	105	200	4	300
OPEN	OPEN	GND	REF	4.3	10	130	250	5.5	275
GND	OPEN	OPEN	REF	5.1	10	145	300	6.5	245
OPEN	GND	GND	REF	6.3	10	170	380	7.5	225
GND	GND	OPEN	REF	7.1	10	185	420	8.5	200
GND	OPEN	GND	REF	8.3	10	210	500	10	190
GND	GND	GND	REF	10.3	10	245	600	12	160

+REFB, –REFB, +REFC, –REFC) result in different resistor divider ratios (DIV) and different attenuation of the LT6376's input common mode voltage.

The internal op amp of LT6376 has two operating regions: a) If the common mode voltage at the inputs of the internal op amp (V_{CMOP}) is between V^- and V^+ –1.75V, the op amp operates in its normal region; b) If V_{CMOP} is between V^+ –1.75V and V^- +76V, the op amp continues to operate, but in its Over-The-Top region with degraded performance (see Over-The-Top operation section of this data sheet for more detail).

Table 2 lists the valid input common mode voltage range for an LT6376 with different configurations of the reference pins when used with dual power supplies. Using the voltage ranges in this table ensures that the internal op amp is operating in its normal (and best) region. The figure entitled Common Mode Voltage Range vs Power Supply Voltage, in the Typical Performance Characteristics section of this data sheet, illustrates the information in Table 2 graphically.

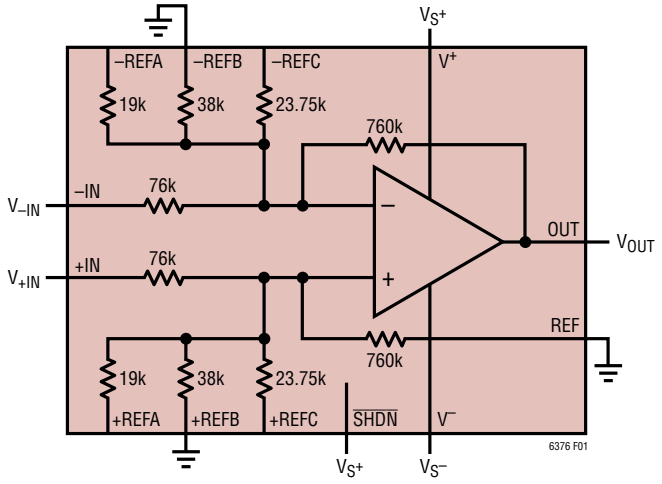


Figure 1. Basic Connections for Dual-Supply Operation (Resistor Divider Ratio = 3.1)

Table 3 lists the valid input common mode voltage range for an LT6376 that results in the internal op amp operating in its Over-The-Top region.

The reference pins can be connected to ground (as in Tables 2 and 3) or to any reference voltage. In order to achieve the specified gain accuracy and CMRR performance of the LT6376, this reference must have a very low impedance over the entire bandwidth of interest. As needed, ensure there are quality high frequency ceramic or film capacitors and low frequency electrolytic capacitors, from the reference to ground.

The valid input common mode range changes depending on the voltages chosen for reference pins. Table 4 lists the valid input common mode voltage range for an LT6376 when the part is used with a single power supply, and REF and the other reference pins are connected to mid-supply. If, as shown in Table 5, the REF pin remains connected to mid-supply, while the other reference pins are connected to ground, the result is a higher positive input range at the expense of a more restricted negative input range.

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Table 2. Common Mode Voltage Operating Range with Dual Power Supplies (Normal Region)

INPUT RANGE (REF = GND)									
+REFA AND –REFA	+REFB AND –REFB	+REFC AND –REFC	DIV	V_S = ±2.5V		V_S = ±15V		V_S = ±25V	
				HIGH	LOW	HIGH	LOW	HIGH	LOW
OPEN	GND	OPEN	3.1	2.325	–7.75	41.075	–46.5	72.075	–77.5
OPEN	OPEN	GND	4.3	3.225	–10.75	56.975	–64.5	99.975	–107.5
GND	OPEN	OPEN	5.1	3.825	–12.75	67.575	–76.5	118.575	–127.5
OPEN	GND	GND	6.3	4.725	–15.75	83.475	–94.5	146.475	–157.5
GND	GND	OPEN	7.1	5.325	–17.75	94.075	–106.5	165.075	–177.5
GND	OPEN	GND	8.3	6.225	–20.75	109.975	–124.5	192.975	–207.5
GND	GND	GND	10.3	7.725	–25.75	136.475	–154.5	230	–230

Table 3. Common Mode Voltage Operating Range with Dual Power Supplies (Over-The-Top Region)

INPUT RANGE (REF = GND)									
+REFA AND –REFA	+REFB AND –REFB	+REFC AND –REFC	DIV	V_S = ±2.5V		V_S = ±15V		V_S = ±25V	
				HIGH	LOW	HIGH	LOW	HIGH	LOW
OPEN	GND	OPEN	3.1	227.85	–7.75	189.1	–46.5	158.1	–77.5
OPEN	OPEN	GND	4.3	230	–10.75	230	–64.5	219.3	–107.5
GND	OPEN	OPEN	5.1	230	–12.75	230	–76.5	230	–127.5
OPEN	GND	GND	6.3	230	–15.75	230	–94.5	230	–157.5
GND	GND	OPEN	7.1	230	–17.75	230	–106.5	230	–177.5
GND	OPEN	GND	8.3	230	–20.75	230	–124.5	230	–207.5
GND	GND	GND	10.3	230	–25.75	230	–154.5	230	–230

Table 4. Common Mode Voltage Operating Range with a Single Power Supply, References to Mid-Supply (Normal Region)

INPUT RANGE (REF = V_S/2)									
+REFA AND –REFA	+REFB AND –REFB	+REFC AND –REFC	DIV	V_S = 5V		V_S = 30V		V_S = 50V	
				HIGH	LOW	HIGH	LOW	HIGH	LOW
OPEN	V_S/2	OPEN	3.1	4.825	–5.25	56.075	–31.5	97.075	–52.5
OPEN	OPEN	V_S/2	4.3	5.725	–8.25	71.975	–49.5	124.975	–82.5
V_S/2	OPEN	OPEN	5.1	6.325	–10.25	82.575	–61.5	143.575	–102.5
OPEN	V_S/2	V_S/2	6.3	7.225	–13.25	98.475	–79.5	171.475	–132.5
V_S/2	V_S/2	OPEN	7.1	7.825	–15.25	109.075	–91.5	190.075	–152.5
V_S/2	OPEN	V_S/2	8.3	8.725	–18.25	124.975	–109.5	217.975	–182.5
V_S/2	V_S/2	V_S/2	10.3	10.225	–23.25	151.475	–139.5	230	–230

Table 5. Common Mode Voltage Operating Range with a Single Power Supply, References to GND (Normal Region)

INPUT RANGE (REF = V_S/2)									
+REFA AND –REFA	+REFB AND –REFB	+REFC AND –REFC	DIV	V_S = 5V		V_S = 30V		V_S = 50V	
				HIGH	LOW	HIGH	LOW	HIGH	LOW
OPEN	GND	OPEN	3.1	9.825	–0.25	86.075	–1.5	147.075	–2.5
OPEN	OPEN	GND	4.3	13.725	–0.25	119.975	–1.5	204.975	–2.5
GND	OPEN	OPEN	5.1	16.325	–0.25	142.575	–1.5	230	–2.5
OPEN	GND	GND	6.3	20.225	–0.25	176.475	–1.5	230	–2.5
GND	GND	OPEN	7.1	22.825	–0.25	199.075	–1.5	230	–2.5
GND	OPEN	GND	8.3	26.725	–0.25	230	–1.5	230	–2.5
GND	GND	GND	10.3	33.225	–0.25	230	–1.5	230	–2.5

The LT6376 will not operate correctly if the common mode voltage at its input pins goes below the range specified in above tables, but the part will not be damaged as long as the lowest common mode voltage at the inputs of the internal op amp (V_{CMOP}) is always greater than $V^–$ –25V. Also, the voltage at LT6376 input pins should never be higher than 230V or lower than –230V under any circumstances.

SHUTDOWN

The LT6376 in the DFN14 package has a shutdown pin ($\overline{SHDN}$). Under normal operation this pin should be tied to V^+ or allowed to float. Driving this pin to at least 2.5V below V^+ will cause the part to enter a low power state. The supply current is reduced to less than 25µA and the op amp output becomes high impedance.

SUPPLY VOLTAGE

The positive supply pin of the LT6376 should be bypassed with a small capacitor (typically 0.1µF) as close to the supply pin as possible. When driving heavy loads an additional 4.7µF electrolytic capacitor should be added. When using split supplies, the same is true for the $V^–$ supply pin.

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ACCURATE CURRENT MEASUREMENTS

The LT6376 can be used in high side, low side and bi-directional wide common mode range current sensing. Figure 2 shows the LT6376 sensing current by measuring the voltage across R_{SENSE}. The added sense resistors create a CMRR error and a gain error. For R_{SENSE} greater than 0.5Ω the source resistance mismatch degrades the CMRR. Adding a resistor equal in value to R_{SENSE} in series with the +IN terminal (R_C) eliminates this mismatch.

Using an R_{SENSE} greater than 4.7Ω will cause the gain error to exceed the 0.0075% specification of the LT6376. This is due to the loading effects of the LT6376.

$$V_{OUT} = 10 \bullet I_{LOAD} \bullet R_{SENSE} \bullet 76k/(76k + R_{SENSE})$$

Increasing R_{SENSE} and R_C slightly to R_{SENSE}' removes the gain error.

$$R_{SENSE}' = R_{SENSE} \bullet 76k/(76k - R_{SENSE}).$$

NOISE AND FILTERING

The noise performance of the LT6376 can be optimized both by appropriate choice of its internal attenuation setting and by the addition of a filter to the amplifier output (Figure 3). For applications that do not require the full bandwidth of the LT6376, the addition of an output filter will lower system noise. Table 6 shows the output noise for different internal resistor divider ratios and output filter bandwidths.

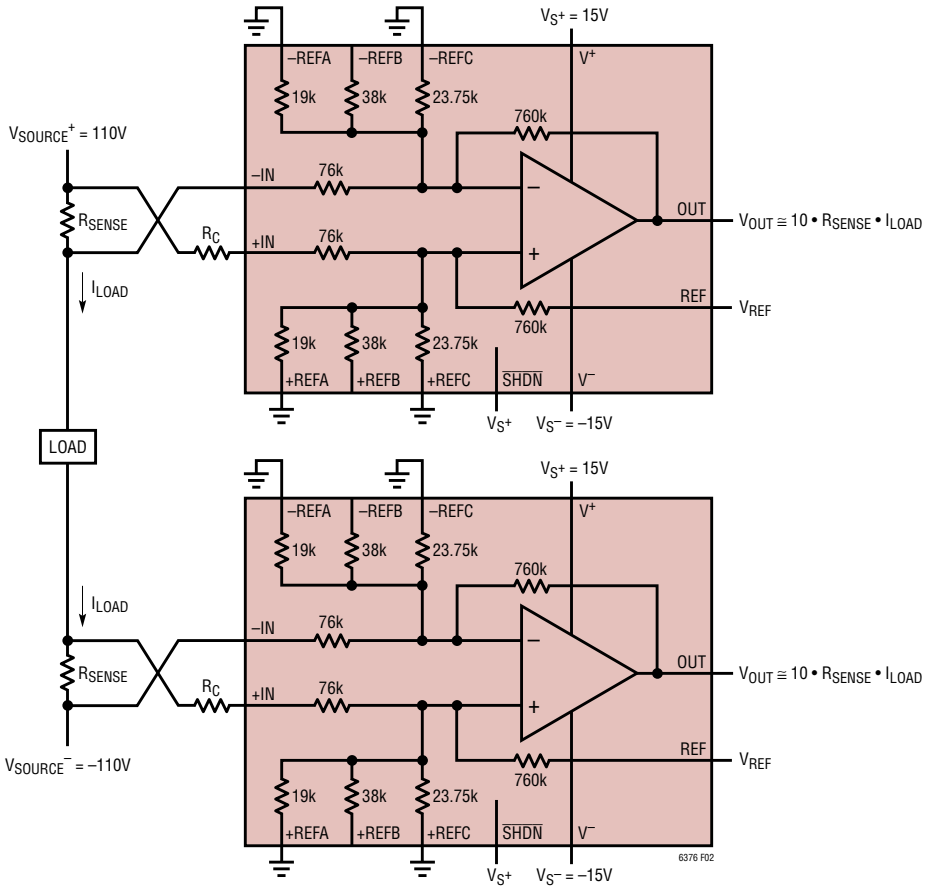

Figure 2. Wide Voltage Range Current Sensing

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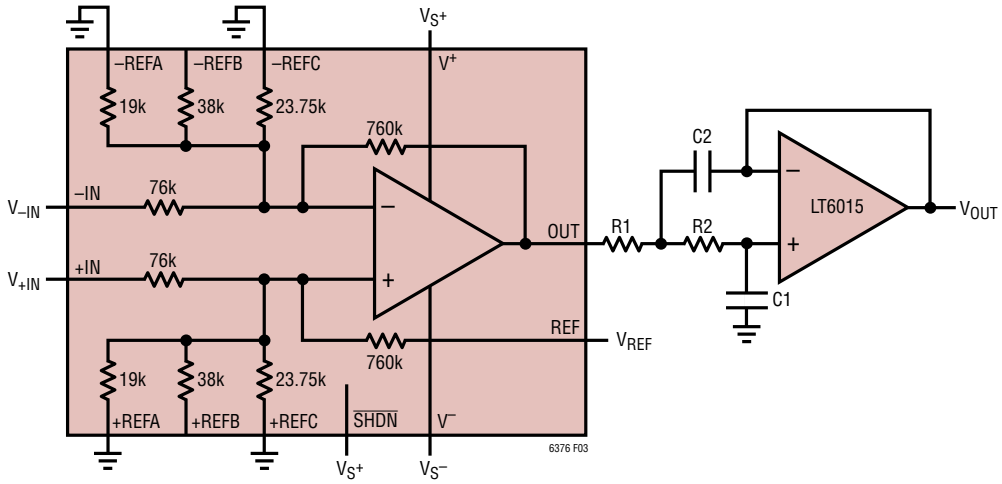

Figure 3. Output Filtering with 2-Pole Butterworth Filter

Table 6. Output Noise (V_{P-P}) for 2-Pole Butterworth Filter for Different Internal Resistor Divider Ratios

Corner Frequency	3.1	4.3	5.1	6.3	7.1	8.3	10.3
No Filter	548µV	606µV	638µV	678µV	707µV	747µV	809µV
100kHz	328µV	394µV	434µV	488µV	523µV	572µV	649µV
10kHz	107µV	131µV	146µV	168µV	183µV	204µV	239µV
1kHz	33µV	41µV	46µV	53µV	57µV	64µV	75µV
100Hz	12µV	15µV	17µV	19µV	21µV	24µV	28µV

Table 7. Component Values for Different 2-Pole Butterworth Filter Bandwidths

Corner Frequency	R1	R2	C1	C2
100kHz	11kΩ	11.3kΩ	100pF	200pF
10kHz	11kΩ	11.3kΩ	1nF	2nF
1kHz	11kΩ	11.3kΩ	10nF	20nF
100Hz	11kΩ	11.3kΩ	0.1µF	0.2µF

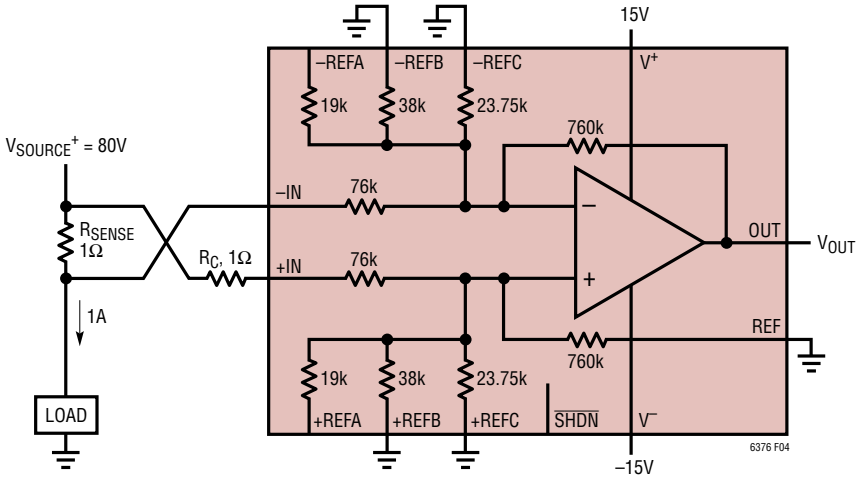

Figure 4. Current Measurement Application

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ERROR BUDGET ANALYSIS

Figure 4 shows the LT6376 in a current measurement application. The error budget for this application is shown in Table 8. The resistor divider ratio is set to 6.3 to divide the 80V input common mode voltage down to 12.7V at the op amp inputs. The 1A current and 1Ω sense resistor produce an output full-scale (FS) voltage of 10V (in the LT6376) and 1V (in all the other listed parts). Table 8 shows the error sources in parts per million (ppm) of the output full-scale voltage across the temperature range of 25°C to 85°C.

Different sources of error contribute to the maximum accuracy that can be achieved in an application. Gain error, offset voltage and common mode rejection error combine to set the initial error. Additionally, the gain error and offset voltage drift across the temperature range. The excellent gain accuracy, low offset voltage, high CMRR, low offset voltage drift and low gain error drift of the LT6376 all combine to enable extremely accurate measurements.

Over-The-Top OPERATION

When the input common mode voltage of the internal op amp (V_{CMOP}) in the LT6376 is biased near or above the V^+ supply, the op amp is operating in the Over-The-Top region. The op amp continues to operate with an input common mode voltage of up to 76V above $V^–$ (regardless of the positive power supply voltage V^+), but its performance is degraded. The op amp's input bias currents change from under ±2nA to 14µA. The op amp's input offset current rises to ±50nA which adds ±3.8mV to the input offset voltage.

In addition, when operating in the Over-The-Top region, the differential input impedance decreases from 1MΩ in normal operation to approximately 3.7kΩ in Over-The-Top operation. This resistance appears across the summing nodes of the internal op amp and boosts noise and offset while decreasing speed. Noise and offset will increase by between 66% and 83% depending on the resistor divider ratio setting. The bandwidth will be reduced by between 40% to 45%. For more detail on Over-The-Top operation, consult the LT6015 data sheet.

OUTPUT

The output of the LT6376 can typically swing to within 5mV of either rail with no load and is capable of sourcing and sinking approximately 25mA. The LT6376 is internally compensated to drive at least 1nF of capacitance under any output loading conditions. A 0.22µF capacitor in series with a 150Ω resistor between the output and ground will compensate the amplifier to drive capacitive loads greater than 1nF. Additionally, the LT6376 has more gain and phase margin as the resistor divider ratio is increased.

Table 8. Error Budget Analysis

ERROR SOURCE	LT6376 (DIV = 6.3)	LT6375 (DIV = 7)	AD629B	COMPETITOR	ERROR, ppm of OUTPUT FS			
					LT6376	LT6375	AD629B	COMPETITOR
Differential Gain (V/V)	10	1	1	1				
Output FS Voltage (V)	10	1	1	1				
Accuracy, T_A = 25°C								
Initial Gain Error	0.0075% FS	0.006% FS	0.03% FS	0.02% FS	75	60	300	200
Output Offset Voltage	3800µV	450µV	500µV	1100µV	380	450	500	1100
Common Mode	10 • (80V/90dB) = 25300µV	80V/89dB = 2839µV	80V/86dB = 4009µV	80V/90dB = 2530µV	2530	2839	4009	2530
Total Accuracy Error					2985	3349	4809	3830
Temperature Drift								
Gain	1ppm/°C ×60°C	1ppm/°C ×60°C	10ppm/°C ×60°C	10ppm/°C ×60°C	60	60	600	600
Output Offset Voltage	75µV/°C ×60°C	12µV/°C ×60°C	10µV/°C ×60°C	15µV/°C ×60°C	450	720	600	900
Total Drift Error					510	780	1200	1500
Total Error					3495	4129	6009	5330

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DISTORTION

The LT6376 features excellent distortion performance when the internal op amp is operating within the supply rails. Operating the LT6376 with input common mode voltages that go from normal to Over-The-Top operation will significantly degrade the LT6376's linearity as the op amp must transition between two different input stages.

POWER DISSIPATION CONSIDERATIONS

Because of the ability of the LT6376 to operate on power supplies up to ±25V, to withstand very high input voltages and to drive heavy loads, there is a need to ensure the die junction temperature does not exceed 150°C. The LT6376 is housed in DF14 (θ_{JA} = 43°C/W, θ_{JC} = 4°C/W) and MS16 (θ_{JA} = 130°C/W) packages.

In general, the die junction temperature (T_J) can be estimated from the ambient temperature (T_A), and the device power dissipation (P_D):

$$T_J = T_A + P_D \bullet \theta_{JA}$$

Power is dissipated by the amplifier's quiescent current, by the output current driving a resistive load and by the input current driving the LT6376's internal resistor network.

$$P_D = ((V_S^+ - V_S^-) \bullet I_S) + P_{OD} + P_{RESD}$$

For a given supply voltage, the worst-case output power dissipation $P_{OD(MAX)}$ occurs with the output voltage at half of either supply voltage. $P_{OD(MAX)}$ is given by:

$$P_{OD(MAX)} = (V_S/2)^2/R_{LOAD}$$

The power dissipated in the internal resistors (P_{RESD}) depends on the input voltage, the resistor divider ratio (DIV), the output voltage and the voltage on REF and the other reference pins. The following equations and Figure 5 show different components of P_{RESD} corresponding to different groups of LT6376's internal resistors (assuming that LT6376 is used with a dual supply configuration with REF and all reference pins at ground).

$$P_{RESDA} = (V_{+IN})^2/(76k + 76k/(DIV - 1))$$

$$P_{RESDB} = (V_{-IN} - V_{+IN}/DIV)^2/(76k)$$

$$P_{RESDC} = (V_{+IN}/DIV)^2/(76k/(DIV - 1.1))$$

$$P_{RESDD} = (V_{+IN}/DIV - V_{OUT})^2/(760k)$$

$$P_{RESD} = P_{RESDA} + P_{RESDB} + P_{RESDC} + P_{RESDD}$$

P_{RESD} simplifies to:

$$P_{RESD} = 2(V_{+IN}^2((DIV-1)/DIV - V_{OUT}/(10 \bullet V_{+IN})) + 0.055 \bullet V_{OUT}^2)/76k$$

In general, P_{RESD} increases with higher input voltage, higher resistor divider ratio (DIV), and lower output, REF and reference pin voltages.

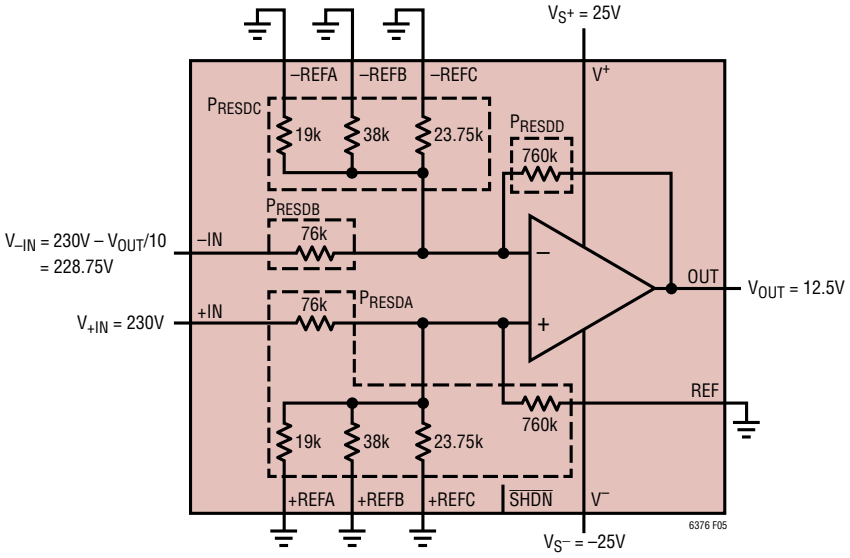

Figure 5. Power Dissipation Example

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Example: An LT6376 in a DFN package mounted on a PC board has a thermal resistance of 43°C/W. Operating on ±25V supplies and driving a 2.5kΩ load to 12.5V with V_{+IN} = 230V and DIV = 10.3, the total power dissipation is given by:

$$P_D = (50 \bullet 0.6mA) + 12.5^2/2.5k + 230^2/84.17k + (228.75 – 230/10.3)^2/76k + (230/10.3)^2/8.26k + (230/10.3 – 12.5)^2/760k = 1.342W$$

Assuming a thermal resistance of 43°C/W, the die temperature will experience a 57.7°C rise above ambient. This implies that the maximum ambient temperature the LT6376 should operate under the above conditions is:

$$T_A = 150°C – 57.7°C = 92.3°C$$

Keep in mind that the DFN package has an exposed pad which can be used to lower the θ_{JA} of the package. The more PCB metal connected to the exposed pad, the lower the thermal resistance.

The MSOP package has no exposed pad and a higher thermal resistance (θ_{JA} = 130°C/W). It should not be used in applications which have a high ambient temperature, require driving a heavy load, or require an extreme input voltage.

THERMAL SHUTDOWN

For safety, the LT6376 will enter shutdown mode when the die temperature rises to approximately 163°C. This thermal shutdown has approximately 9°C of hysteresis requiring the die temperature to cool 9°C before enabling the amplifier again.

USE AT OTHER PRECISION DC GAINS

The array of resistors within the LT6376 provides numerous configurable connections that provide precision gains other than the G = 10 differential gain options described previously. Note that only the +IN and –IN pins can operate outside of the supply window. Since most of these alternate configurations involve driving the REFx pins, as well as the +IN and –IN pins, the input signals must be less than the supply voltages. Fully differential gains are available as shown in Table 9, and may be output-shifted with a REF offset signal. These configurations allow the LT6376 to be used as a versatile precision gain block with essentially no external components besides the supply decoupling. In most cases, only a single positive supply will be required. In Table 9, connections are identified as NC (no connect), INPUT (refers to both inputs driven, +signal to +pins,–signal to –pins), CROSS (refers to inputs cross-coupled, +signal to –pins, –signal to +pins), OUT (refers to the output fed back to –pins), or REF (refers to connecting the REF pin to +pins). The same configurations provide inverting gains by grounding any pins intended for the +signal source. The differential input resistance is also tabulated as well as the amplification factor of the internal gain section involved (noise-gain, which helps to estimate the error-budget of the configuration).

Single-ended noninverting gains are also available as shown in Table 10, including many that operate as buffers (loaded only by the op amp input bias). A rich option set exists by using the REF pin as an additional variable. In Table 10, connections are identified as NC (no connect), INPUT (driven by the input), OUT (fed back from the output), or GROUND (grounded). Table 10 also includes tabulations of the internal resistor divider (DIV), noise gain (re-amplification), and the input loading presented by the circuit.

USE AS PRECISION AC GAIN BLOCK

In AC-coupled applications operating from a single power supply, it is useful to set the output voltage near mid-supply to maximize dynamic range. The LT6376 readily supports this with no additional biasing components by connecting specific pins to the V^+ and $V^–$ potentials and AC-coupling the signal paths. Table 11 shows the available inverting gains and also tabulates the load resistances presented at the input. In Table 11, connections are identified as NC (no connect), AC IN (AC-coupled to the input) OUT (fed back from the output), tied to V^+, tied to $V^–$, or AC GND (AC- grounded). All pins that require an AC ground can share a single bypass capacitor. Likewise, all pins driven from the source signal may share a coupling capacitor as well. The output should also connect to the load circuitry using a coupling capacitor to block the mid-supply DC voltage.

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The LT6376 may also be used for single-supply noninverting AC gains by employing a combination of input attenuation and re-amplification. With numerous choices of attenuation and re-amplification, several hundred overall gain combinations are possible, ranging from 0.1 to 73. The combinations are more plentiful than the DC configurations because there is no constraint on matching internal source resistances to minimize offset.

The input attenuator section dedicates some pins to establishing a bias point and with the remaining pins, provides several choices of input signal division factors as shown in Table 12. The bias point varies between 20% and 49% of the supply voltage depending on the configuration. Swapping V^+ and V^- will bias the circuit closer to V^+.

The high attenuations that only use +IN for the signal path can accept waveform peaks that significantly exceed the supply range. Table 12 also includes tabulations of the resulting AC load resistance presented to the signal source. Here again, all pins that require an AC-ground connection may share a single bypass capacitor, and all AC signal connections may share a coupling capacitor.

The single-supply AC-coupled noninverting circuit is completed by configuring the post-attenuator amplification factor. Table 13 shows the available re-amplification factors. Once again, all pins that require an AC-ground connection may share a single bypass capacitor, and the output should use a coupling capacitor to its load destination as well.

Table 9. Configurations for Precision Differential Gains

LT6376 DIFFERENTIAL AND INVERTING PRECISION DC GAINS

GAIN	±IN	±REFA	±REFB	±REFC	REF	DIFF R_{IN} (k)	NOISE GAIN
2	CROSS	NC	CROSS	INPUT	REF	24.52	63
8	NC	INPUT	NC	CROSS	REF	21.11	73
10	INPUT	NC	NC	NC	REF	152	11
12	NC	NC	CROSS	INPUT	REF	29.23	53
18	INPUT	INPUT	NC	CROSS	REF	18.54	83
20	NC	NC	INPUT	NC	REF	76	21
22	CROSS	NC	NC	INPUT	REF	36.19	43
30	INPUT	NC	INPUT	NC	REF	50.67	31
32	NC	NC	NC	INPUT	REF	47.50	33
40	NC	INPUT	NC	NC	REF	38	41
42	INPUT	NC	NC	INPUT	REF	36.19	43
50	INPUT	INPUT	NC	NC	REF	30.40	51
52	NC	NC	INPUT	INPUT	REF	29.23	53
60	NC	INPUT	INPUT	NC	REF	25.33	61
62	INPUT	NC	INPUT	INPUT	REF	24.52	63
70	INPUT	INPUT	INPUT	NC	REF	21.71	71
72	NC	INPUT	NC	INPUT	REF	21.11	73
82	INPUT	INPUT	NC	INPUT	REF	18.54	83
92	NC	INPUT	INPUT	INPUT	REF	16.52	93
102	INPUT	INPUT	INPUT	INPUT	REF	14.90	103

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Table 10. Configurations for Precision Noninverting Gains

LT6376 NONINVERTING PRECISION DC GAINS

GAIN	FEATURE	+IN	+REFA	+REFB	+REFC	REF	–IN	–REFA	–REFB	–REFC	NOISE GAIN	DIV	R_{IN} (k)
1		GROUND	NC	NC	NC	INPUT	GROUND	NC	NC	NC	11	11	836
10		INPUT	NC	NC	NC	GROUND	GROUND	NC	NC	NC	11	1.10	836
11	BUFFER	INPUT	NC	NC	NC	INPUT	GROUND	NC	NC	NC	11	1	Hi-Z
30		INPUT	NC	INPUT	NC	GROUND	GROUND	NC	GROUND	NC	31	1.03	785.33
31	BUFFER	INPUT	NC	INPUT	NC	INPUT	GROUND	NC	GROUND	NC	31	1	Hi-Z
32		NC	NC	NC	INPUT	GROUND	NC	NC	NC	GROUND	33	1.03	783.75
40		NC	INPUT	NC	NC	GROUND	NC	GROUND	NC	NC	41	1.03	779
41	BUFFER	NC	INPUT	NC	NC	INPUT	NC	GROUND	NC	NC	41	1	Hi-Z
42		INPUT	NC	NC	INPUT	GROUND	GROUND	NC	NC	GROUND	43	1.02	778.10
50		INPUT	INPUT	NC	NC	GROUND	GROUND	GROUND	NC	NC	51	1.02	775.20
51	BUFFER	INPUT	INPUT	NC	NC	INPUT	GROUND	GROUND	NC	NC	51	1	Hi-Z
52		NC	NC	INPUT	INPUT	GROUND	NC	NC	GROUND	GROUND	53	1.02	774.62
60		NC	INPUT	INPUT	NC	GROUND	NC	GROUND	GROUND	NC	61	1.02	772.67
61	BUFFER	NC	INPUT	INPUT	NC	INPUT	NC	GROUND	GROUND	NC	61	1	Hi-Z
62		INPUT	NC	INPUT	INPUT	GROUND	GROUND	NC	GROUND	GROUND	63	1.02	772.26
70		INPUT	INPUT	INPUT	NC	GROUND	GROUND	GROUND	GROUND	NC	71	1.01	770.86
72		NC	INPUT	NC	INPUT	GROUND	NC	GROUND	NC	GROUND	73	1.01	770.56
82		INPUT	INPUT	NC	INPUT	GROUND	GROUND	GROUND	NC	GROUND	83	1.01	769.27
83	BUFFER	INPUT	INPUT	NC	INPUT	INPUT	GROUND	GROUND	NC	GROUND	83	1	Hi-Z
92		NC	INPUT	INPUT	INPUT	GROUND	NC	GROUND	GROUND	GROUND	93	1.01	768.26
93	BUFFER	NC	INPUT	INPUT	INPUT	INPUT	NC	GROUND	GROUND	GROUND	93	1	Hi-Z
102		INPUT	INPUT	INPUT	INPUT	GROUND	GROUND	GROUND	GROUND	GROUND	103	1.01	767.45
103	BUFFER	INPUT	INPUT	INPUT	INPUT	INPUT	GROUND	GROUND	GROUND	GROUND	103	1	Hi-Z

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Table 11. Configurations for Single-Supply AC-Coupled Inverting Gains

LT6376 SINGLE-SUPPLY INVERTING AC GAINS

GAIN	–IN	–REFA	–REFB	–REFC	+IN	+REFA	+REFB	+REFC	REF	AC R_{IN} (k)
–10	AC IN	NC	NC	NC	V^-	AC GND	V^-	V^+	V^-	76
–20	NC	NC	AC IN	NC	V^-	AC GND	V^-	V^+	V^-	38
–30	AC IN	NC	AC IN	NC	V^-	AC GND	V^-	V^+	V^-	25
–32	NC	NC	NC	AC IN	V^-	AC GND	V^-	V^+	V^-	24
–40	NC	AC IN	NC	NC	V^-	AC GND	V^-	V^+	V^-	19
–42	AC IN	NC	NC	AC IN	V^-	AC GND	V^-	V^+	V^-	18
–50	AC IN	AC IN	NC	NC	V^-	AC GND	V^-	V^+	V^-	15
–52	NC	NC	AC IN	AC IN	V^-	AC GND	V^-	V^+	V^-	15
–60	NC	AC IN	AC IN	NC	V^-	AC GND	V^-	V^+	V^-	13
–62	AC IN	NC	AC IN	AC IN	V^-	AC GND	V^-	V^+	V^-	12
–70	AC IN	AC IN	AC IN	NC	V^-	AC GND	V^-	V^+	V^-	11
–72	NC	AC IN	NC	AC IN	V^-	AC GND	V^-	V^+	V^-	11
–82	AC IN	AC IN	NC	AC IN	V^-	AC GND	V^-	V^+	V^-	9
–92	NC	AC IN	AC IN	AC IN	V^-	AC GND	V^-	V^+	V^-	8
–102	AC IN	AC IN	AC IN	AC IN	V^-	AC GND	V^-	V^+	V^-	7

Table 12. Configurations for Single-Supply AC-Coupled Input Attenuations

LT6376 SINGLE-SUPPLY AC ATTENUATOR CONFIGURATIONS

DIV	DC BIAS	+IN	+REFA	+REFB	+REFC	REF	AC R_{IN} (k)
1.41	0.33	V^+	AC IN	V^-	AC IN	AC IN	36
1.42	0.33	V^+	AC IN	V^-	AC IN	NC	36
1.43	0.35	V^+	AC IN	V^-	AC IN	V^+	35
1.69	0.24	V^+	AC IN	AC IN	V^-	AC IN	31
1.70	0.24	V^+	AC IN	AC IN	V^-	NC	31
1.72	0.26	V^+	AC IN	AC IN	V^-	V^+	30
1.73	0.33	V^+	AC IN	V^-	NC	AC IN	44
1.75	0.33	V^+	AC IN	V^-	NC	NC	44
1.78	0.35	V^+	AC IN	V^-	NC	V^+	44
1.91	0.33	V^+	NC	V^-	AC IN	AC IN	48
1.94	0.33	V^+	NC	V^-	AC IN	NC	49
1.94	0.20	V^+	V^-	AC IN	AC IN	AC IN	30
1.96	0.20	V^+	V^-	AC IN	AC IN	NC	30
1.97	0.35	V^+	NC	V^-	AC IN	V^+	48
1.98	0.22	V^+	V^-	AC IN	AC IN	V^+	30
2.02	0.38	AC IN	AC IN	V^+	V^-	AC IN	30

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Table 12. Configurations for Single-Supply AC-Coupled Input Attenuations (continued)

LT6376 SINGLE-SUPPLY AC ATTENUATOR CONFIGURATIONS

DIV	DC BIAS	+IN	+REFA	+REFB	+REFC	REF	AC R_{IN} (k)
2.04	0.38	AC IN	AC IN	V+	V–	NC	30
2.06	0.40	AC IN	AC IN	V+	V–	V+	30
2.27	0.38	NC	AC IN	V+	V–	AC IN	33
2.30	0.38	NC	AC IN	V+	V–	NC	34
2.33	0.40	NC	AC IN	V+	V–	V+	33
2.51	0.48	V+	AC IN	V+	V–	AC IN	31
2.55	0.48	V+	AC IN	V+	V–	NC	31
2.58	0.49	V+	AC IN	V+	V–	V+	31
3.12	0.43	V+	V–	V+	AC IN	AC IN	34
3.19	0.43	V+	V–	V+	AC IN	NC	35
3.22	0.44	V+	V–	V+	AC IN	V+	34
3.32	0.44	AC IN	V–	AC IN	V+	AC IN	35
3.40	0.44	AC IN	V–	AC IN	V+	NC	36
3.43	0.45	AC IN	V–	AC IN	V+	V+	36
3.38	0.20	V+	V–	AC IN	NC	AC IN	51
3.50	0.20	V+	V–	AC IN	NC	NC	53
3.55	0.22	V+	V–	AC IN	NC	V+	53
4.90	0.49	V–	V+	AC IN	V–	AC IN	45
5.10	0.49	V–	V+	AC IN	V–	NC	47
5.15	0.48	V–	V+	AC IN	V–	V–	47
5.73	0.38	AC IN	NC	V+	V–	AC IN	84
6.20	0.38	AC IN	NC	V+	V–	NC	91
6.30	0.40	AC IN	NC	V+	V–	V+	90
9.36	0.44	AC IN	V–	AC GND	V+	AC IN	77
10.20	0.44	AC IN	V–	AC GND	V+	NC	84
10.30	0.45	AC IN	V–	AC GND	V+	V+	84
31	0.33	V+	NC	V–	NC	AC IN	785
43	0.24	V+	NC	NC	V–	AC IN	778
51	0.20	V+	V–	NC	NC	AC IN	775
53	0.38	NC	NC	V+	V–	AC IN	775
61	0.33	NC	V–	V+	NC	AC IN	773
63	0.48	V+	NC	V+	V–	AC IN	772
71	0.43	V+	V–	V+	NC	AC IN	771
73	0.44	NC	V–	NC	V+	AC IN	771
83	0.49	V–	V+	NC	V–	AC IN	769
93	0.43	NC	V+	V–	V–	AC IN	768
103	0.49	V+	V+	V–	V–	AC IN	767

APPLICATIONS INFORMATION

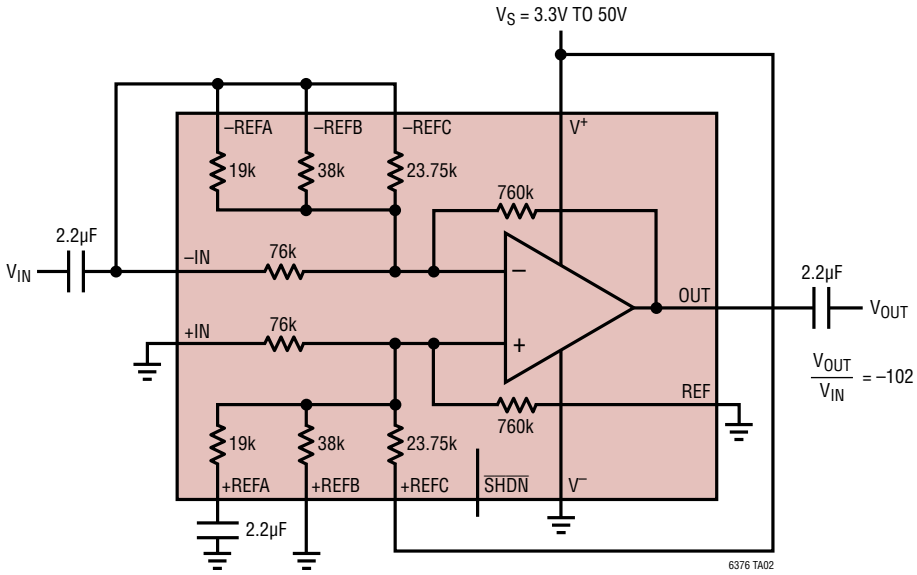
Table 13. Configurations for Single-Supply AC-Coupled Re-Amplications

LT6376 NONINVERTING AC RE-AMPLIFICATIONS

GAIN	–IN	–REFA	–REFB	–REFC
11	AC GND	NC	NC	NC
21	NC	NC	AC GND	NC
31	AC GND	NC	AC GND	NC
33	NC	NC	NC	AC GND
41	NC	AC GND	NC	NC
43	AC GND	NC	NC	AC GND
51	AC GND	AC GND	NC	NC
53	NC	NC	AC GND	AC GND
61	NC	AC GND	AC GND	NC
63	AC GND	NC	AC GND	AC GND
71	AC GND	AC GND	AC GND	NC
73	NC	AC GND	NC	AC GND
83	AC GND	AC GND	NC	AC GND
93	NC	AC GND	AC GND	AC GND
103	AC GND	AC GND	AC GND	AC GND

TYPICAL APPLICATIONS

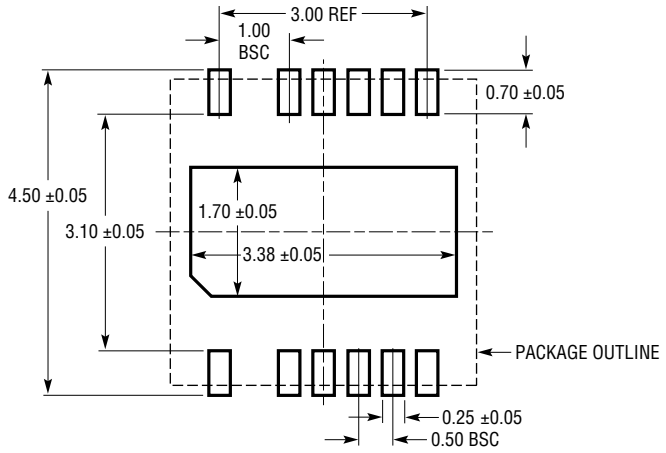
40.2dB Audio Gain Stage



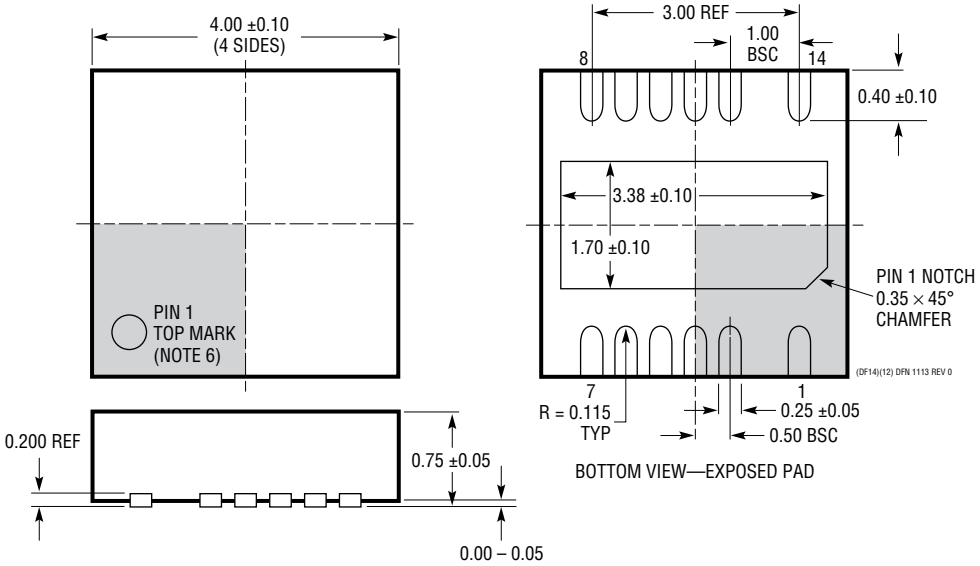
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LT6376#packaging for the most recent package drawings.

DF Package
14(12)-Lead Plastic DFN (4mm × 4mm)
(Reference LTC DWG # 05-08-1963 Rev Ø)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



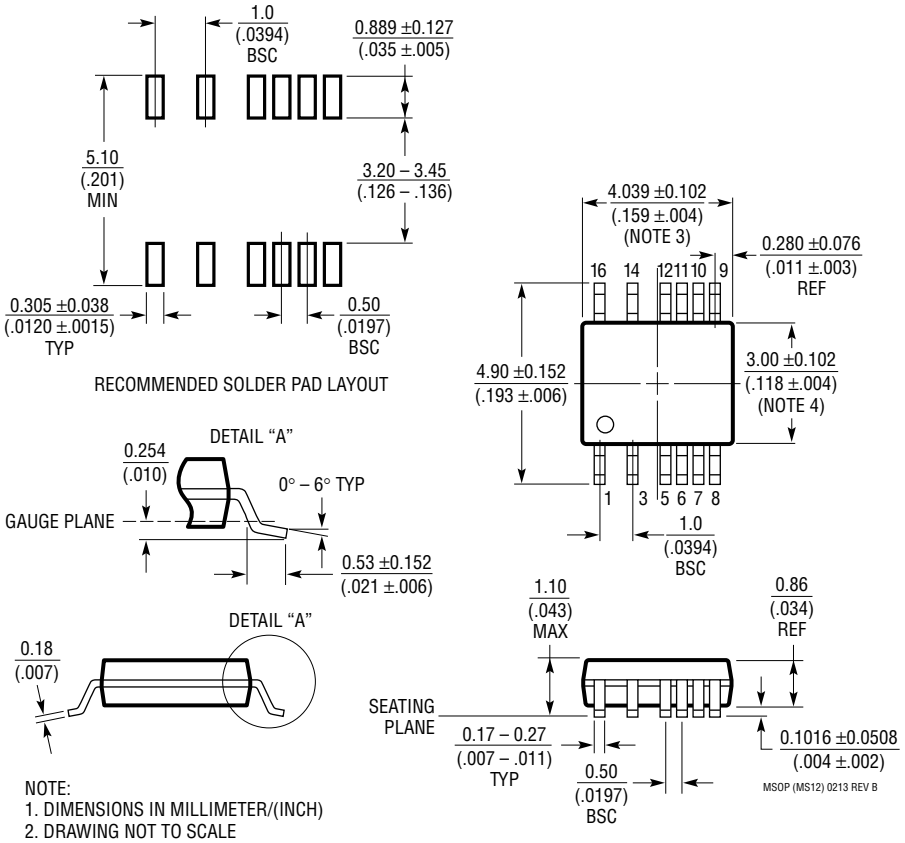
BOTTOM VIEW—EXPOSED PAD

NOTE:
1. PACKAGE OUTLINE DOES NOT CONFORM TO JEDEC MO-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LT6376#packaging for the most recent package drawings.

MS Package
16 (12)-Lead Plastic MSOP with 4 Pins Removed
(Reference LTC DWG # 05-08-1847 Rev B)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX