650MHz Differential ADC Driver/Dual Selectable Gain Amplifier

FEATURES

- **650MHz –3dB Small-Signal Bandwidth**
- **600MHz –3dB Large-Signal Bandwidth**
- **High Slew Rate: 3300V/µs**
- **Easily Configured for Single-Ended to Differential Conversion**
- 200MHz ±0.1dB Bandwidth
- User Selectable Gain of +1, +2 and –1
- No External Resistors Required
- 46.5dBm Equivalent OIP3 at 30MHz When Driving an ADC
- IM3 with $2V_{P-P}$ Composite, Differential Output: –87dBc at 30MHz, –83dBc at 70MHz
- –77dB SFDR at 30MHz, $2V_{P-P}$ Differential Output
- 6ns 0.1% Settling Time for 2V Step
- Low Supply Current: 8mA per Ampifier
- Differential Gain of 0.02%, Differential Phase of 0.01°
- 50dB Channel Separation at 100MHz
- Wide Supply Range: ±2.25V (4.5V) to ±6.3V (12.6V)
- 3mm × 3mm 16-Pin QFN Package

APPLICATIONS

- Differential ADC Driver
- Single-Ended to Differential Conversion
- Differential Video Line Driver

DESCRIPTION

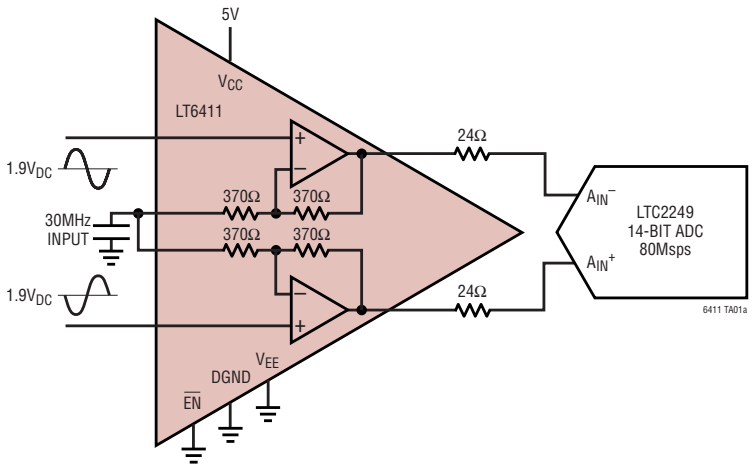
The LT®6411 is a dual amplifier with individually selectable gains of +1, +2 and –1. The amplifiers have excellent distortion performance for driving ADCs as well as excellent bandwidth and slew rate for video, data transmission and other high speed applications. Single-ended to differential conversion with a system gain of 2 is particularly straightforward by configuring one amplifier with a gain of +1 and the other amplifier with a gain of –1. The LT6411 can be used on split supplies as large as ±6V and on a single supply as low as 4.5V.

Each amplifier draws only 8mA of quiescent current when enabled. When disabled, the output pins become high impedance and each amplifier draws less than 350µA.

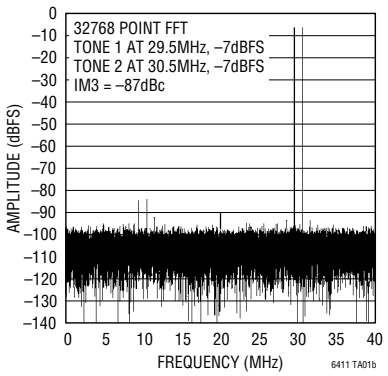
The LT6411 is manufactured on Linear Technology's proprietary, low voltage, complimentary, bipolar process and is available in the ultra-compact, 3mm × 3mm, 16pin QFN package.

TYPICAL APPLICATION

Differential ADC Driver



30MHz 2-Tone 32768 Point FFT, LT6411 Driving an LTC®2249 14-Bit ADC

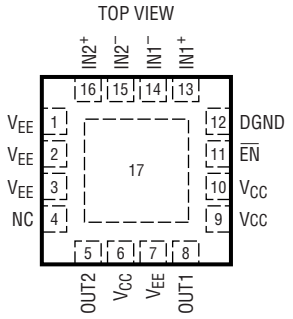


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Total Supply Voltage (V_{CC} to V_{EE}) 12.6V
Input Current (Note 2).....±10mA
Output Current (Continuous) .....±70mA
$\overline{EN}$ to DGND Voltage (Note 2) 5.5V
Output Short-Circuit Duration (Note 3) ..... Indefinite
Operating Temperature Range (Note 4) ... –40°C to 85°C
Specified Temperature Range (Note 5) .... –40°C to 85°C
Storage Temperature Range..... –65°C to 125°C
Junction Temperature ..... 125°C

PACKAGE/ORDER INFORMATION



UD PACKAGE
16-LEAD (3mm × 3mm) PLASTIC QFN
T_{JMAX} = 125°C, θ_{JA} = 68°C/W, θ_{JC} = 4.2°C/W
EXPOSED PAD (PIN 17) IS V_{EE}, MUST BE SOLDERED TO PCB

ORDER PART NUMBER	UD PART MARKING*
LT6411CUD LT6411IUD	LCGP LCGP

Order Options Tape and Reel: Add #TR
Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: http://www.linear.com/leadfree/

Consult LTC Marketing for parts specified with wider operating temperature ranges.
*Temperature grade is identified by a label on the shipping container.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_S = ±5V, A_V = 2, R_L = 150Ω, C_L = 1.5pF, $V_{\overline{EN}}$ = 0.4V, V_{DGND} = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Referred Offset Voltage	V_{IN} = 0V, V_{OS} = V_{OUT}/2	 ●		3	±10 ±20	mV mV
I_{IN}	Input Current		●		–17	±50	µA
R_{IN}	Input Resistance	V_{IN} = ±1V	●	150	500		kΩ
C_{IN}	Input Capacitance	f = 100kHz			1		pF
V_{CMR}	Maximum Input Common Mode Voltage Minimum Input Common Mode Voltage				V_{CC} – 1 V_{EE} + 1		V V
PSRR	Power Supply Rejection Ratio	V_S (Total) = 4.5V to 12V (Note 6)	●	56	62		dB
I_{PSRR}	Input Current Power Supply Rejection	V_S (Total) = 4.5V to 12V (Note 6)	●		1	±4	µA/V
A_V ERR	Gain Error	V_{OUT} = ±2V	●		–1.2	±5	%
A_V MATCH	Gain Matching	V_{OUT} = ±2V			±1		%
V_{OUT}	Maximum Output Voltage Swing	R_L = 1k R_L = 150Ω R_L = 150Ω	 ●	±3.70 ±3.25 ±3.10	±3.95 ±3.6		V V V
I_S	Supply Current, Per Amplifier		 ●		8	11 14	mA mA
	Supply Current, Disabled, per Amplifier	$V_{\overline{EN}}$ = 4V $V_{\overline{EN}}$ = Open	● ●		22 0.5	350 350	µA µA
$I_{\overline{EN}}$	Enable Pin Current	$V_{\overline{EN}}$ = 0.4V $V_{\overline{EN}}$ = V^+	● ●	–200	–95 0.5	 50	µA µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_S = ±5V, A_V = 2, R_L = 150Ω, C_L = 1.5pF, $V_{\overline{EN}}$ = 0.4V, V_{DGND} = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{SC}	Output Short-Circuit Current	R_L = 0Ω, V_{IN} = ±1V	●	±50	±105		mA
SR	Slew Rate	±1V on ±2V Output Step (Note 9)		1700	3300		V/µs
–3dB BW	Small-Signal –3dB Bandwidth	V_{OUT} = 200mV_{P-P}, Single Ended			650		MHz
0.1dB BW	Gain Flatness ±0.1dB Bandwidth	V_{OUT} = 200mV_{P-P}, Single Ended			200		MHz
FPBW	Full Power Bandwidth 2V Differential	V_{OUT} = 2V_{P-P} Differential, –3dB			600		MHz
	Full Power Bandwidth 2V	V_{OUT} = 2V_{P-P} (Note 7)		270	525		MHz
	Full Power Bandwidth 4V	V_{OUT} = 4V_{P-P} (Note 7)			263		MHz
	All Hostile Crosstalk	f = 10MHz, V_{OUT} = 2V_{P-P} f = 100MHz, V_{OUT} = 2V_{P-P}			–75 –50		dB dB
t_s	Settling Time	0.1% to V_{FINAL}, V_{STEP} = 2V			6		ns
t_r, t_f	Small-Signal Rise and Fall Time	10% to 90%, V_{OUT} = 200mV_{P-P}			550		ps
dG	Differential Gain	(Note 8)			0.02		%
dP	Diffierential Phase	(Note 8)			0.01		Deg

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 5V, V_{EE} = 0V, A_V = 2, No R_{LOAD}, $V_{\overline{EN}}$ = 0.4V, V_{DGND} = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Noise/Harmonic Performance Input/Output Characteristics							
1MHz Signal							
HD	Second/Third Harmonic Distortion	2V_{P-P} Differential 2V_{P-P} Differential, R_L = 200Ω Differential			–88 –87		dBc dBc
$IMD3_{1M}$	Third-Order IMD	2V_{P-P} Differential Composite, f1 = 0.95MHz, f2 = 1.05MHz			–93		dBc
		2V_{P-P} Differential Composite, f1 = 0.95MHz, f2 = 1.05MHz, R_L = 200Ω Differential			–91		dBc
$OIP3_{1M}$	Output Third-Order Intercept	Differential, f1 = 0.95MHz, f2 = 1.05MHz (Note 10)			49.5		dBm
NF	Noise Figure	Single Ended			25.1		dB
e_{n1M}	Input Referred Noise Voltage Density				8		nV/√Hz
P1dB	1dB Compression Point	(Note 10)			19.5		dBm
10MHz Signal							
HD	Second/Third Harmonic Distortion	2V_{P-P} Differential 2V_{P-P} Differential, R_L = 200Ω Differential			–85 –76		dBc dBc
$IMD3_{10M}$	Third-Order IMD	2V_{P-P} Differential Composite, R_L = 1k, f1 = 9.5MHz, f2 = 10.5MHz			–92		dBc
		2V_{P-P} Differential Composite, f1 = 9.5MHz, f2 = 10.5MHz, R_L = 200Ω Differential			–89		dBc
$OIP3_{10M}$	Output Third-Order Intercept	Differential, f1 = 9.5MHz, f2 = 10.5MHz (Note 10)			49		dBm
NF	Noise Figure	Single Ended			24.7		dB
e_{n10M}	Input Referred Noise Voltage Density				7.7		nV/√Hz
P1dB	1dB Compression Point	(Note 10)			19.5		dBm

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 5V, V_{EE} = 0V, A_V = 2, No R_{LOAD}, $V_{\overline{EN}}$ = 0.4V, V_{DGND} = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
30MHz Signal							
HD	Second/Third Harmonic Distortion	$2V_{P-P}$ Differential $2V_{P-P}$ Differential, R_L = 200Ω Differential			–77 –64		dBc dBc
$IMD3_{30M}$	Third-Order IMD	$2V_{P-P}$ Differential Composite, f1 = 29.5MHz, Differential, f2 = 30.5MHz			–87		dBc
		$2V_{P-P}$ Differential Composite, f1 = 29.5MHz, f2 = 30.5MHz, R_L = 200Ω Differential			–75		dBc
$OIP3_{30M}$	Output Third-Order Intercept	Differential, f1 = 29.5MHz, f2 = 30.5MHz (Note 10)			46.5		dBm
NF	Noise Figure	Single Ended			24.6		dB
e_{n30M}	Input Referred Noise Voltage Density				7.6		$nV/\sqrt{Hz}$
P1dB	1dB Compression Point	(Note 10)			19.5		dBm
70MHz Signal							
HD	Second/Third Harmonic Distortion	$2V_{P-P}$ Differential $2V_{P-P}$ Differential, R_L = 200Ω Differential			–63 –52		dBc dBc
$IMD3_{70M}$	Third-Order IMD	$2V_{P-P}$ Differential Composite, f1 = 69.5MHz, Differential, f2 = 70.5MHz			–83		dBc
		$2V_{P-P}$ Differential Composite, f1 = 69.5MHz, f2 = 70.5MHz, R_L = 200Ω Differential			–64		dBc
$OIP3_{70M}$	Output Third-Order Intercept	Differential, f1 = 69.5MHz, f2 = 70.5MHz (Note 10)			44.5		dBm
NF	Noise Figure	Single Ended			24.7		dB
e_{n70M}	Input Referred Noise Voltage Density				7.7		$nV/\sqrt{Hz}$
P1dB	1dB Compression Point	(Note 10)			19.5		dBm

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: This parameter is guaranteed to meet specified performance through design and characterization. It is not production tested.

Note 3: As long as output current and junction temperature are kept below the Absolute Maximum Ratings, no damage to the part will occur. Depending on the supply voltage, a heat sink may be required.

Note 4: The LT6411C is guaranteed functional over the operating temperature range of –40°C to 85°C.

Note 5: The LT6411C is guaranteed to meet specified performance from 0°C to 70°C. The LT6411C is designed, characterized and expected to meet specified performance from –40°C and 85°C but is not tested or QA sampled at these temperatures. The LT6411I is guaranteed to meet specified performance from –40°C to 85°C.

Note 6: The two supply voltage settings for power supply rejection are shifted from the typical $\pm V_S$ points for ease of testing. The first measurement is taken at V_{CC} = 3V, V_{EE} = –1.5V to provide the required 3V headroom for the enable circuitry to function with EN, DGND and all inputs connected to 0V. The second measurement is taken at V_{CC} = 8V, V_{EE} = –4V.

Note 7: Full power bandwidth is calculated from the slew rate:

$FPBW = SR/(\pi \bullet V_{P-P})$

Note 8: Differential gain and phase are measured using a Tektronix TSG120YC/NTSC signal generator and a Tektronix 1780R video measurement set. The resolution of this equipment is better than 0.05% and 0.05°. Ten identical amplifier stages were cascaded giving an effective resolution of better than 0.005% and 0.005°.

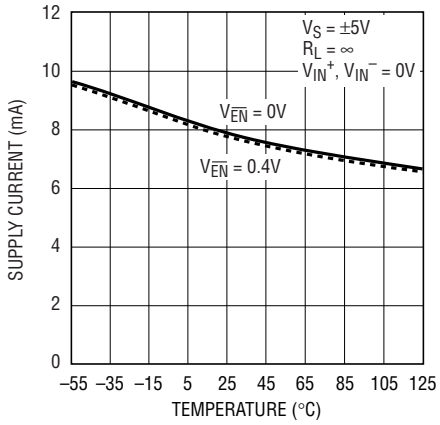
Note 9: Slew rate is 100% production tested on channel 1. Slew rate of channel 2 is guaranteed through design and characterization.

Note 10: Since the LT6411 is a feedback amplifier with low output impedance, a resistive load is not required when driving an ADC. Therefore, typical output power is very small. In order to compare the LT6411 with typical g_m amplifiers that require 50Ω output loading, the LT6411 output voltage swing driving an ADC is converted to OIP3 and P1dB as if it were driving a 50Ω load.

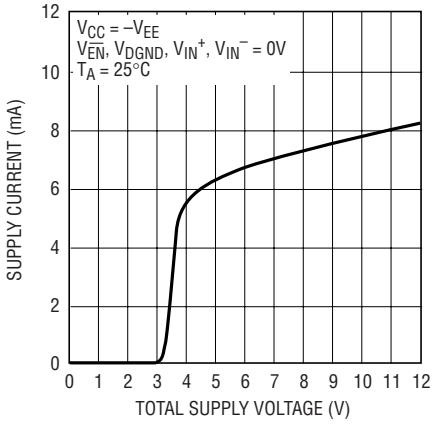
TYPICAL PERFORMANCE CHARACTERISTICS

All measurements are per amplifier with single-ended outputs unless otherwise noted.

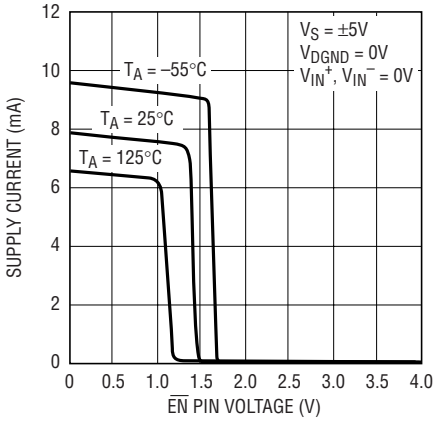
Supply Current per Amplifier vs Temperature



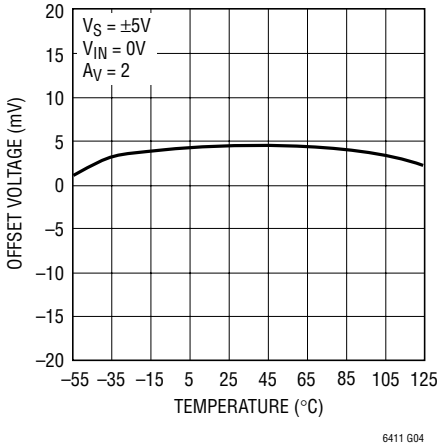
Supply Current per Ampifier vs Supply Voltage



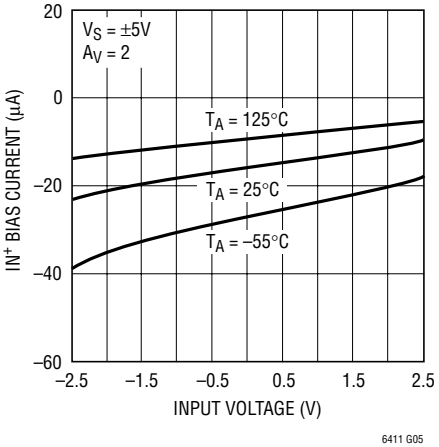
Supply Current per Amplifier vs $\overline{EN}$ Pin Voltage



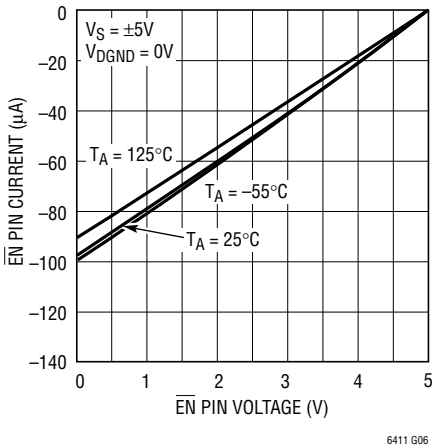
Output Offset Voltage vs Temperature



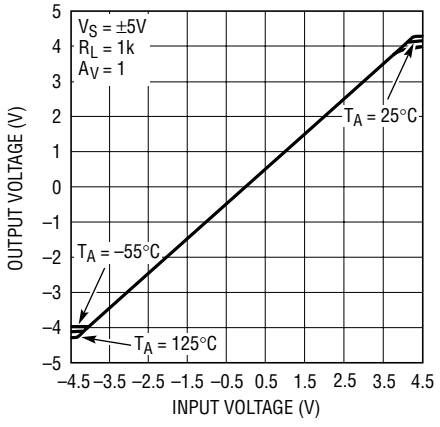
Positive Input Bias Current vs Input Voltage



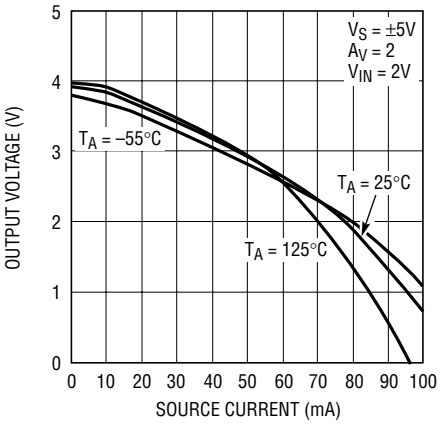
$\overline{EN}$ Pin Current vs $\overline{EN}$ Pin Voltage



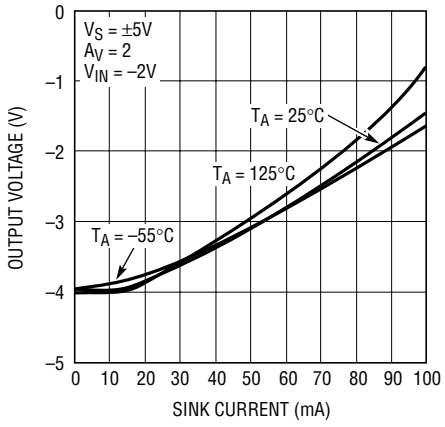
Output Voltage vs Input Voltage



Output Voltage Swing vs I_{LOAD} (Output High)



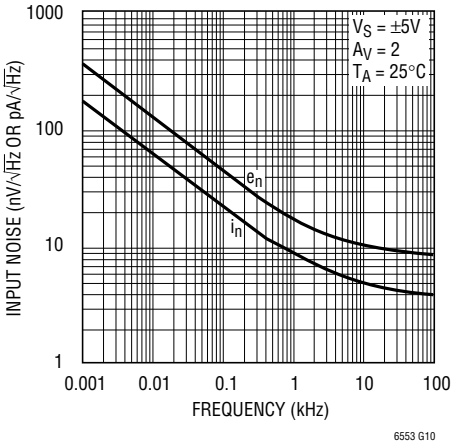
Output Voltage Swing vs I_{LOAD} (Output Low)



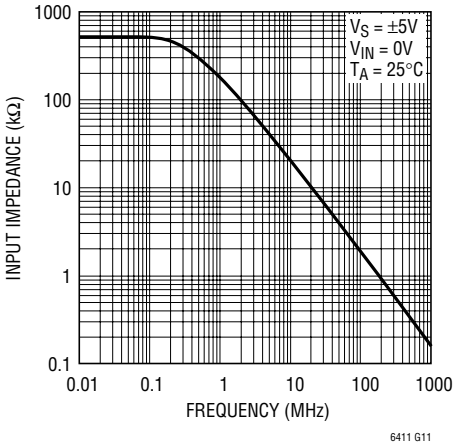
TYPICAL PERFORMANCE CHARACTERISTICS

All measurements are per amplifier with single-ended outputs unless otherwise noted.

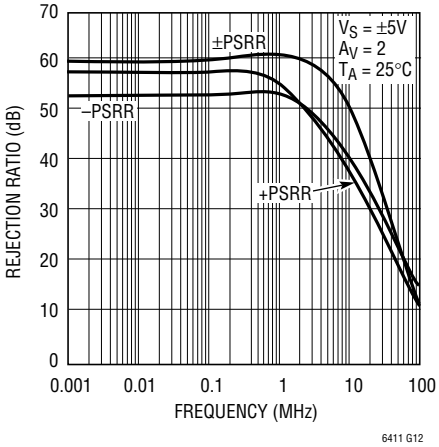
Input Noise Spectral Density



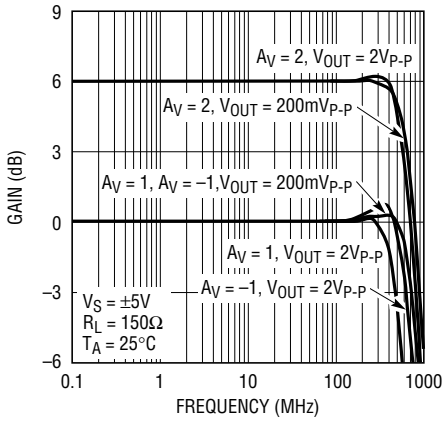
Positive Input Impedance vs Frequency



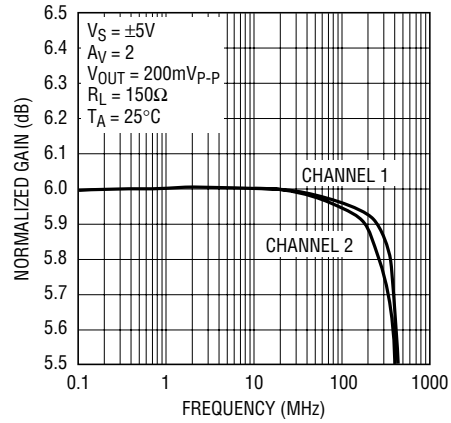
PSRR vs Frequency



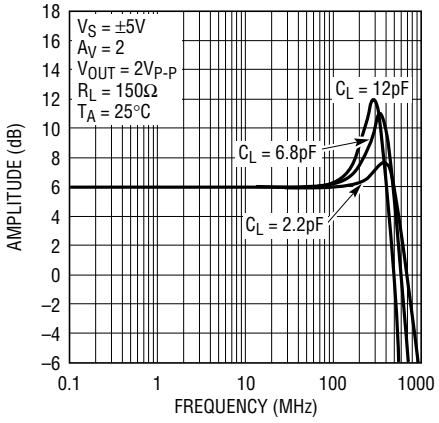
Frequency Response vs Gain Configuration



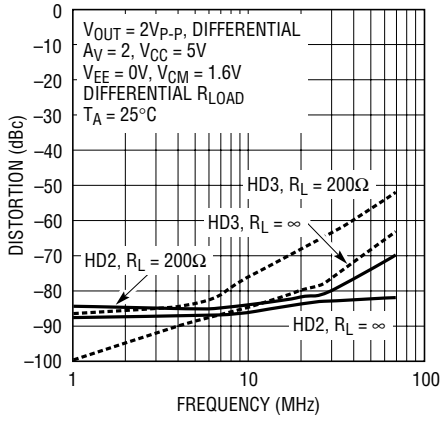
Gain Flatness vs Frequency



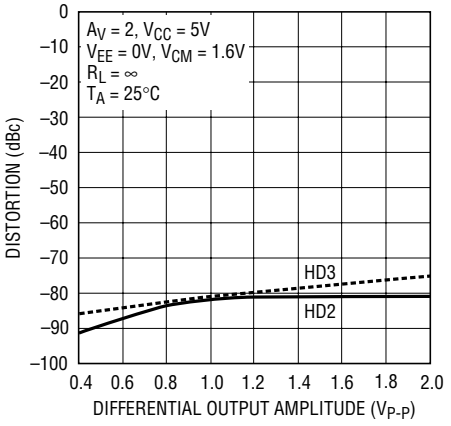
Frequency Response with Capacitive Loads



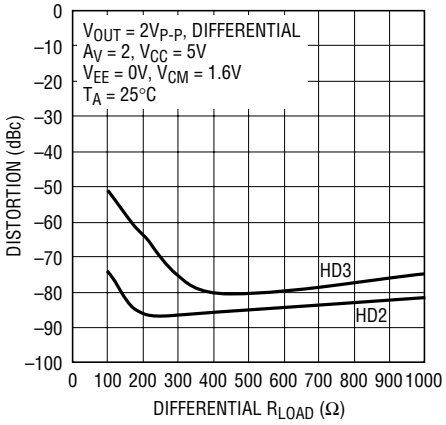
Harmonic Distortion vs Frequency, Differential Input



Harmonic Distortion vs Amplitude, 30MHz, Differential Input



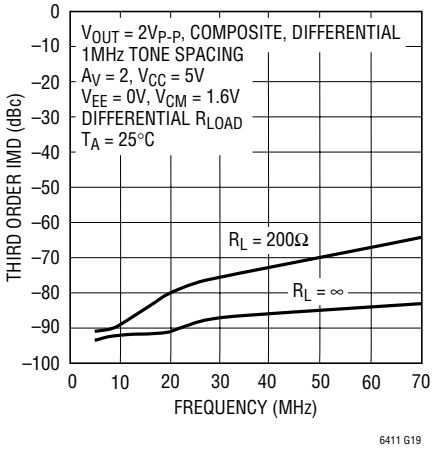
Harmonic Distortion vs Load, 30MHz, Differential Input



TYPICAL PERFORMANCE CHARACTERISTICS

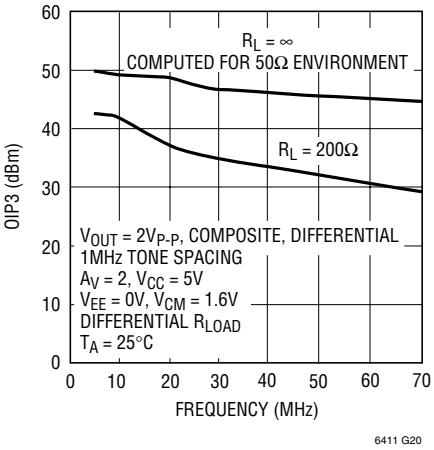
All measurements are per amplifier with single-ended outputs unless otherwise noted.

Third Order Intermodulation Distortion vs Frequency, Differential Input



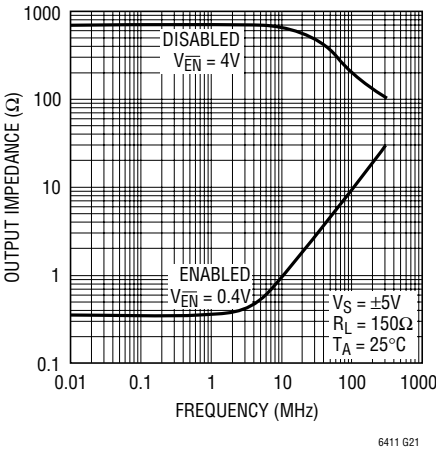
6411 G19

Output Third Order Intercept vs Frequency, Differential Input



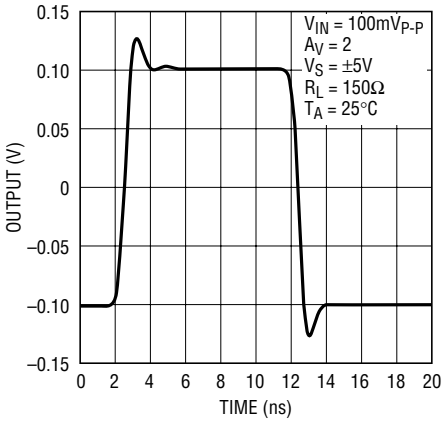
6411 G20

Output Impedance vs Frequency



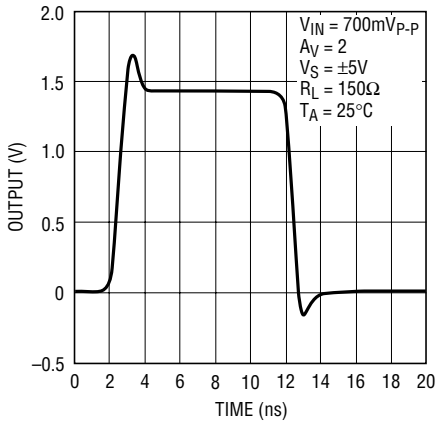
6411 G21

Small-Signal Transient Response



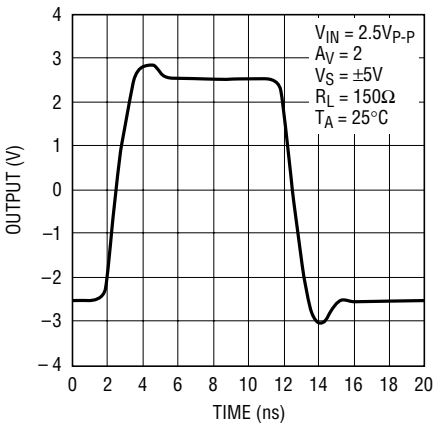
6411 G22

Video Amplitude Transient Response



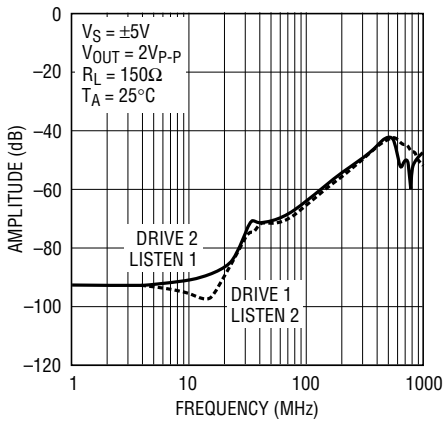
6411 G23

Large-Signal Transient Response



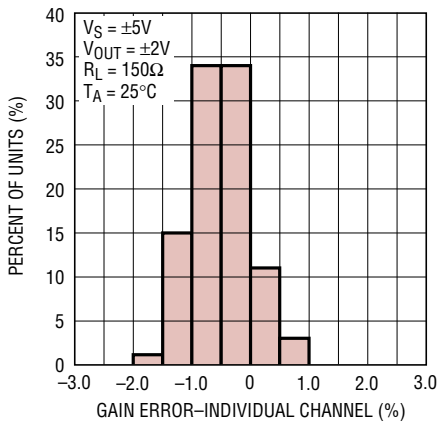
6411 G24

Crosstalk vs Frequency



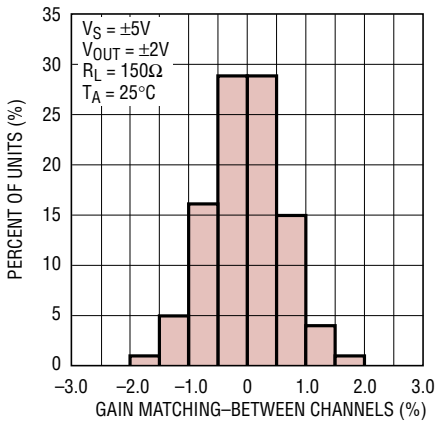
1635 G25

Gain Error Distribution



6411 G26

Gain Matching Distribution



6411 G27

PIN FUNCTIONS

V_{EE} (Pins 1, 2): Negative Supply Voltage. V_{EE} pins are not internally connected to each other and must all be connected externally. Proper supply bypassing is necessary for best performance. See the Applications Information section.

V_{EE} (Pins 3, 7): Negative Supply Voltage for Output Stage. V_{EE} pins are not internally connected to each other and must all be connected externally. Proper supply bypassing is necessary for best performance. See the Applications Information section.

NC (Pin 4): This pin is not internally connected.

OUT2 (Pin 5): Output of Channel 2. The gain between the input and the output of this channel is set by the connection of the channel 2 input pins. See Table 1 in Applications Information for details.

V_{CC} (Pins 6, 9): Positive Supply Voltage for Output Stage. V_{CC} pins are not internally connected to each other and must all be connected externally. Proper supply bypassing is necessary for best performance. See the Applications Information section.

OUT1 (Pin 8): Output of Channel 1. The gain between the input and the output of this channel is set by the connection of the channel 1 input pins. See Table 1 in Applications Information for details.

V_{CC} (Pin 10): Positive Supply Voltage. V_{CC} pins are not internally connected to each other and must all be connected externally. Proper supply bypassing is necessary for best performance. See the Applications Information section.

$\overline{EN}$ (Pin 11): Enable Control Pin. An internal pull-up resistor of 46k will turn the part off if the pin is allowed to float and defines the pin's impedance. When the pin is pulled low, the part is enabled.

DGND (Pin 12): Digital Ground Reference for Enable Pin. This pin is normally connected to ground.

$IN1^+$ (Pin 13): Channel 1 Positive Input. This pin has a nominal impedance of 400kΩ and does not have an internal termination resistor.

$IN1^-$ (Pin 14): This pin connects to the internal resistor network of the channel 1 amplifier, connecting by a 370Ω resistor to the inverting input.

$IN2^-$ (Pin 15): This pin connects to the internal resistor network of the channel 2 amplifier, connecting by a 370Ω resistor to the inverting input.

$IN2^+$ (Pin 16): Channel 2 Positive Input. This pin has a nominal impedance of 400kΩ and does not have an internal termination resistor.

Exposed Pad (Pin 17): The pad is internally connected to V_{EE} (Pin 1). If split supplies are used, **do not** tie the pad to ground.

APPLICATIONS INFORMATION

Power Supplies

The LT6411 can be operated on as little as ±2.25V or a single 4.5V supply and as much as ±6V or a single 12V supply. Internally, each supply is independent to improve channel isolation. Note that the Exposed Pad is internally connected to V_{EE} and must not be grounded when using split supplies. **Do not leave any supply pins disconnected or the part may not function correctly!**

Enable/Shutdown

The LT6411 has a TTL compatible shutdown mode controlled by the $\overline{EN}$ pin and referenced to the DGND pin. If the amplifier will be enabled at all times, the $\overline{EN}$ pin can be connected directly to DGND. If the enable function is desired, either driving the pin above 2V or allowing the internal 46k pull-up resistor to pull the $\overline{EN}$ pin to the top rail will disable the amplifier. When disabled, the DC output impedance will rise to approximately 740Ω through the internal feedback and gain resistors (assuming inputs at ground). Supply current into the amplifier in the disabled state will be primarily through V_{CC} and approximately equal to $(V_{CC} – V_{\overline{EN}})/46k$.

It is important that the two following constraints on the DGND pin and the $\overline{EN}$ pin are always followed:

$V_{CC} – V_{DGND} \geq 3V$

$–0.5V \leq V_{\overline{EN}} – V_{DGND} \leq 5.5V$

Split supplies of ±3V to ±5.5V will satisfy these requirements with DGND connected to 0V.

In dual supply cases with V_{CC} less than 3V, DGND should be connected to a potential below ground such as V_{EE}. Since the $\overline{EN}$ pin is referenced to DGND, it may need to be pulled below ground in those cases. In order to protect the internal enable circuitry, the $\overline{EN}$ pin should not be forced more than 0.5V below DGND.

In single supply applications above 5.5V, an additional resistor may be needed from the $\overline{EN}$ pin to DGND if the pin is ever allowed to float. For example, on a 12V single supply, a 33k resistor would protect the pin from floating too high while still allowing the internal pull-up resistor to disable the part.

The DGND pin should not be pulled above the $\overline{EN}$ pin since doing so will turn on an ESD protection diode. If the $\overline{EN}$ pin voltage is forced a diode drop below the DGND pin, current should be limited to 10mA or less.

The enable/disable times of the LT6411 are fast when driven with a logic input. Turn on (from 50% $\overline{EN}$ input to 50% output) typically occurs in less than 50ns. Turn off is slower, but is less than 300ns.

Gain Selection

The gain of the internal amplifiers of the LT6411 is configured by connecting the IN^+ and $IN^–$ pins to the input signal or ground in the combinations shown in Figure 1.

As shown in the Simplified Schematic, the $IN^–$ pins connect to the internal gain resistor of each amplifier, and therefore, each pin can be configured independently. Floating the $IN^–$ pins is not recommended as the parasitic capacitance causes an AC gain of 2 at high frequencies, despite a DC gain of +1. Both inputs are connected together in the gain of +1 configuration to avoid this limitation.

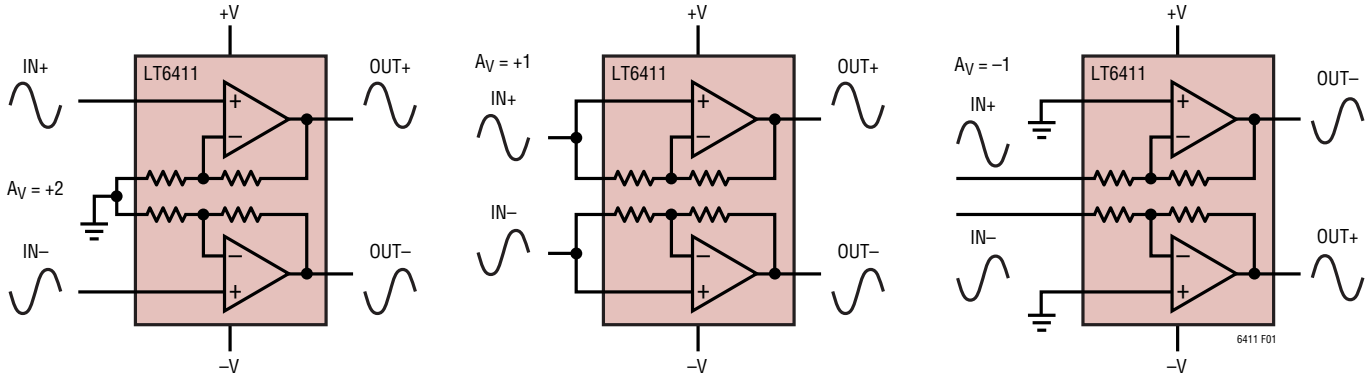


Figure 1. LT6411 Configured in Noninverting Gain of 2, Noninverting Gain of 1 and Inverting Gain of 1, All Shown with Dual Supplies

APPLICATIONS INFORMATION

Input Considerations

The LT6411 input voltage range is from V_{EE} + 1V to V_{CC} – 1V. Therefore, on split supplies the LT6411 input range is always as large as or larger than the output swing. On a single positive supply with a gain of +2 and IN^- connected to ground, however, the input range limit of +1V limits the linear output low swing to 2V (1V multiplied by the internal gain of 2).

The inputs can be driven beyond the point at which the output clips so long as input currents are limited to ±10mA. Continuing to drive the input beyond the output limit can result in increased current drive and slightly increased swing, but will also increase supply current and may result in delays in transient response at larger levels of overdrive.

DC Biasing Differential Amplifier Applications

The inputs of the LT6411 must be DC biased within the input common mode voltage range, typically V_{EE} + 1V to V_{CC} – 1V. If the inputs are AC coupled or DC biased beyond the input voltage range of a driven A-to-D converter, DC biasing or level shifting will be required. In the basic circuit configurations shown in Figure 1, the DC input common mode voltage and the differential input signal are both multiplied by the amplifier gain. In the gain of +2 configuration, the DC common mode voltage gain can be set to unity by adding a capacitor at the IN^- pins as shown in Figure 2.

If the inputs are AC coupled or the LT6411 is preceded by a highpass filter, the input common mode voltage can be set by resistor dividers as shown in Figure 3. Adding the blocking capacitor to the gain setting resistors sets the input and output DC common mode voltages equal. When using the LT6411 to drive an A-to-D converter, the DC common mode voltage level will affect the harmonic distortion of the combined amplifier/ADC system. Figure 4 shows the measured distortion of an LTC2249 ADC when driven by the LT6411 at different common mode voltage levels with the inputs configured as shown in Figure 3. Adjusting the DC bias voltage can optimize the design for the lowest possible distortion.

If the input signals are within the input voltage range and output swing of the LT6411, but outside the input range of an ADC or other circuit the LT6411 is driving,

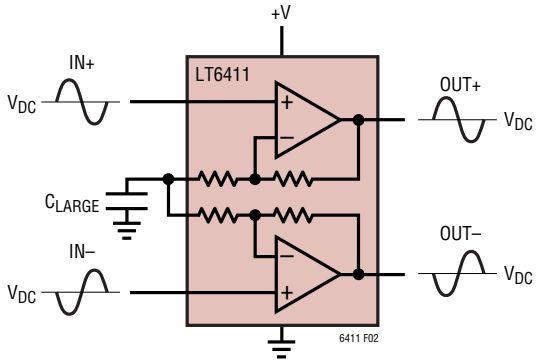


Figure 2. LT6411 Configured with a Differential Gain of 2 and Unity DC Common Mode Gain

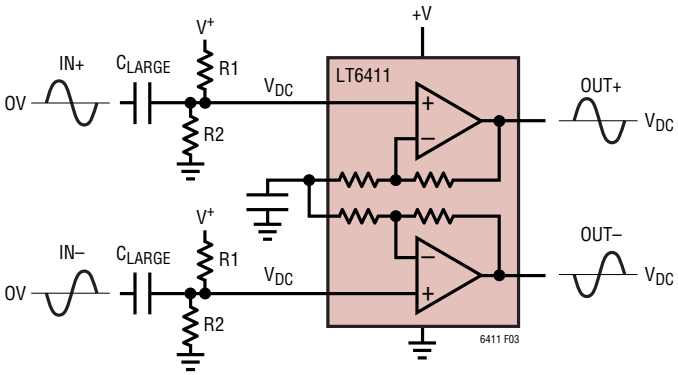


Figure 3. Using Resistor Dividers to Set the Input Common Mode Voltage When AC Coupling

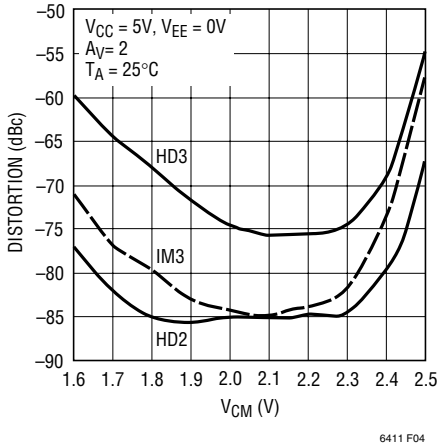


Figure 4. Harmonic and Intermodulation Distortion of the LT6411 Driving an LTC2249 Versus DC Common Mode Voltage. Harmonic Distortion Measured with a –1dBFS Signal at 30.2MHz. Intermodulation Distortion Measured with Two –7dBFS Tones at 30.2MHz and 29.2MHz

APPLICATIONS INFORMATION

the output signals can be AC coupled and DC biased in a manner similar to what is shown at the inputs in Figure 3. A simpler alternative when using an ADC such as the LTC2249 is to use the ADC's V_{CM} pin to set the optimal common mode voltage as shown in Figure 5.

If unity common mode gain and difference mode response to DC is desired, there is another configuration available. Figure 6 shows the LT6411 connected to provide a differential signal gain of +3 with unity common mode gain. For differential signal gain between unity and +3, three resistors can be added to provide attenuation and set the differential input impedance of the stage as illustrated in Figure 7. The general expression for the differential gain is:

$$A_{V(DIFF)} = 1 + \frac{2 \bullet k}{k + 2}$$

Scaling factor 'k' is the multiple between the two equal-value series input resistors and the resistor connected between the two positive inputs. The correct value of R for the external resistors can be computed from the desired differential input impedance, Z_{IN}, as a function of k and the 370Ω internal gain setting resistors, as described in the equation:

$$R = \frac{Z_{IN} \bullet 370\Omega}{370\Omega(k + 2) - Z_{IN}(k + 1)}$$

In Figure 7 k = 2 and R = 13.7Ω, setting the differential gain to +2 and the differential input impedance to approximately 50Ω.

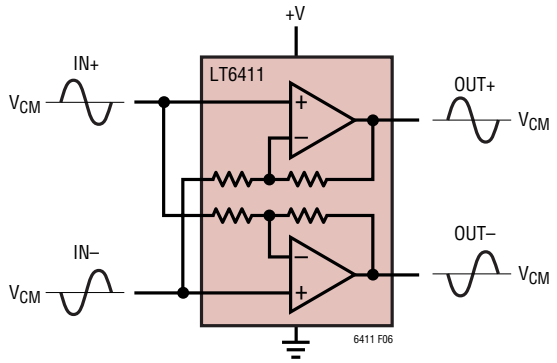


Figure 6. LT6411 Configured for a Differential Gain of +3 and Unity Common Mode Gain with Response to DC

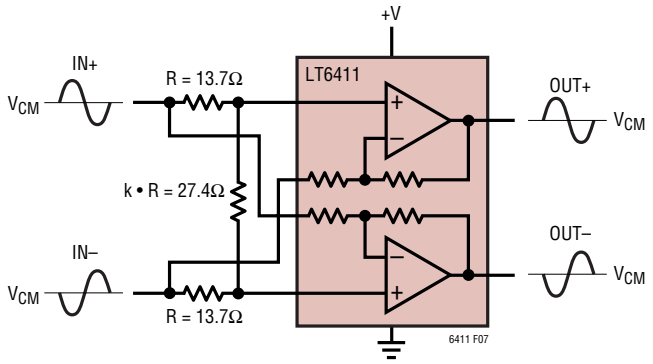


Figure 7. LT6411 Configured with a Differential Input Impedance of 50Ω, a Differential Gain of +2 and Unity Common Mode Gain

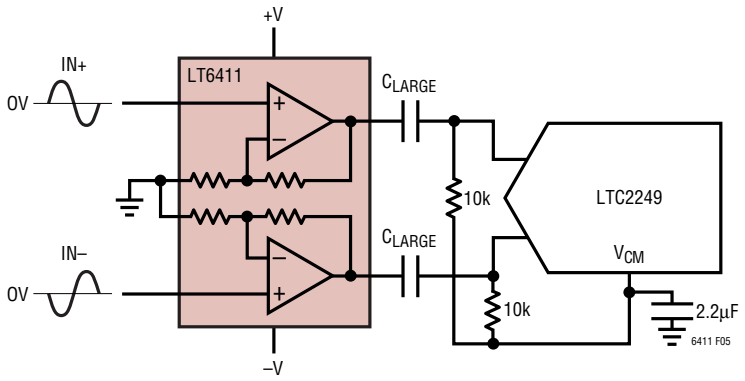


Figure 5. Level Shifting the Output Common Mode Voltage of the LT6411 Using the V_{CM} Pin of an LTC2249

APPLICATIONS INFORMATION

Layout and Grounding

It is imperative that care is taken in PCB layout in order to utilize the very high speed and very low crosstalk of the LT6411. Separate power and ground planes are highly recommended and trace lengths should be kept as short as possible. If input or output traces must be run over a distance of several centimeters, they should use a controlled impedance with matching series and shunt resistances to maintain signal fidelity.

Series termination resistors should be placed as close to the output pins as possible to minimize output capacitance. See the Typical Performance Characteristics section for a plot of frequency response with various output capacitors—only 12pF of parasitic output capacitance causes 6dB of peaking in the frequency response!

Low ESL/ESR bypass capacitors should be placed as close to the positive and negative supply pins as possible. One 4700pF ceramic capacitor is recommended for both V_{CC} and V_{EE}. Additional 470pF ceramic capacitors with minimal trace length on each supply pin will further improve AC and transient response as well as channel isolation. For high current drive and large-signal transient applications, additional 1µF to 10µF tantalums should be added on each supply. The smallest value capacitors should be placed closest to the LT6411 package.

If the undriven input pins are not connected directly to a low impedance ground plane, they must be carefully bypassed to maintain minimal impedance over frequency. Although crosstalk will be very dependent on the board layout, a recommended starting point for bypass capacitors would be 470pF as close as possible to each input pin with one 4700pF capacitor in parallel.

To maintain the LT6411's channel isolation, it is beneficial to shield parallel input and output traces using a ground plane or power supply traces. Vias between topside and backside metal may be required to maintain a low inductance ground near the part where numerous traces converge.

ESD Protection

The LT6411 has reverse-biased ESD protection diodes on all pins. If any pins are forced a diode drop above the positive supply or a diode drop below the negative supply, large currents may flow through these diodes. If the current is kept below 10mA, no damage to the devices will occur.

TYPICAL APPLICATIONS

Single-Ended to Differential Converter

Because the gains of each channel of the LT6411 can be configured independently, the LT6411 can be used to provide a gain of +2 when amplifying differential signals and when converting single-ended signals to differential. With both channels connected to a single-ended input, one channel configured with a gain of +1 and the other configured with a gain of –1, the output will be a differential version of the input with twice the peak-to-peak (differential) amplitude. Figure 8 shows the proper connections and Figure 9 displays the resulting performance when driving an LTC2249. This configuration can preserve signal amplitude when converting single ended video signals to differential signals when driving double terminated cables. The 10k resistors in Figure 8 set the common mode voltage at the output.

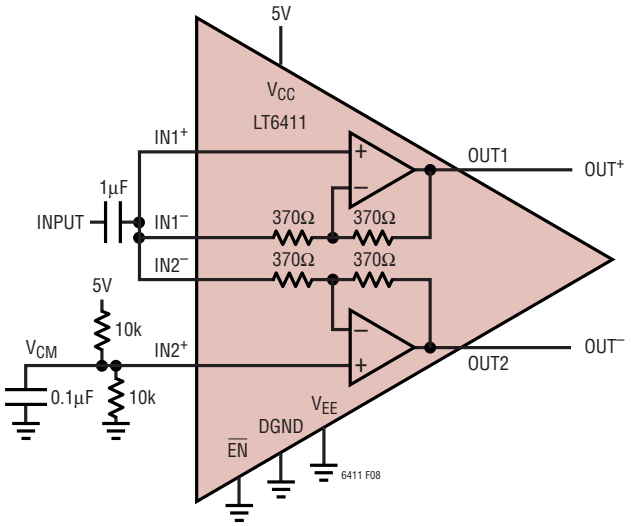


Figure 8. Single-Ended to Differential Converter with Gain of +2 and Common Mode Control

TYPICAL APPLICATIONS

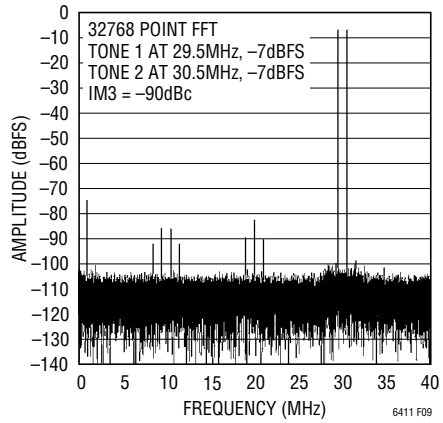


Figure 9. 2-Tone Response of the LT6411 Configured with Single-Ended Inputs Driving the LTC2249 at 29.5MHz, 30.5MHz

Twisted-Pair Line Driver

The LT6411 is ideal when used for driving inexpensive unshielded twisted-pair wires as often found in telephone or communications infrastructure. The input can be composite video, or if three parts are used, RGB or similar and can be either single ended or differential. The LT6411 has excellent performance with all formats.

Double termination of the video cable will enhance fidelity and isolate the LT6411 from capacitive loads. Although most twisted-pair cables have a characteristic impedance

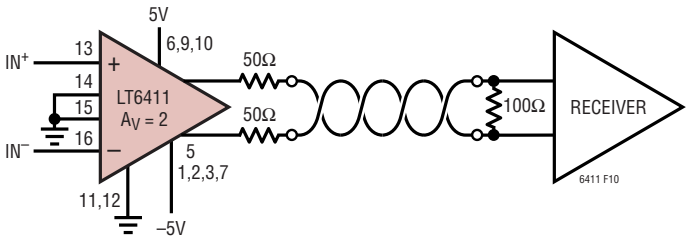


Figure 10. Twisted-Pair Driver

of 100Ω, the cables can be terminated with a smaller series resistance or a larger shunt resistance in order to compensate for attenuation. A typical circuit for a twisted-pair driver is shown in Figure 10.

Single Supply Differential ADC Driver

The LT6411 is well suited for driving differential analog to digital converters. The low output impedance of the LT6411 is capable of driving a variety of filters as well as interfacing with the typically high impedance inputs of ADCs. In addition, the LT6411's excellent distortion allows the part to perform with an SFDR below the limits of many high speed ADCs. The DC1057 demo board, shown schematically in Figure 11 and physically in Figure 12, allows implementation and testing of the LT6411 with a variety of different Linear Technology high speed ADCs.

TYPICAL APPLICATIONS

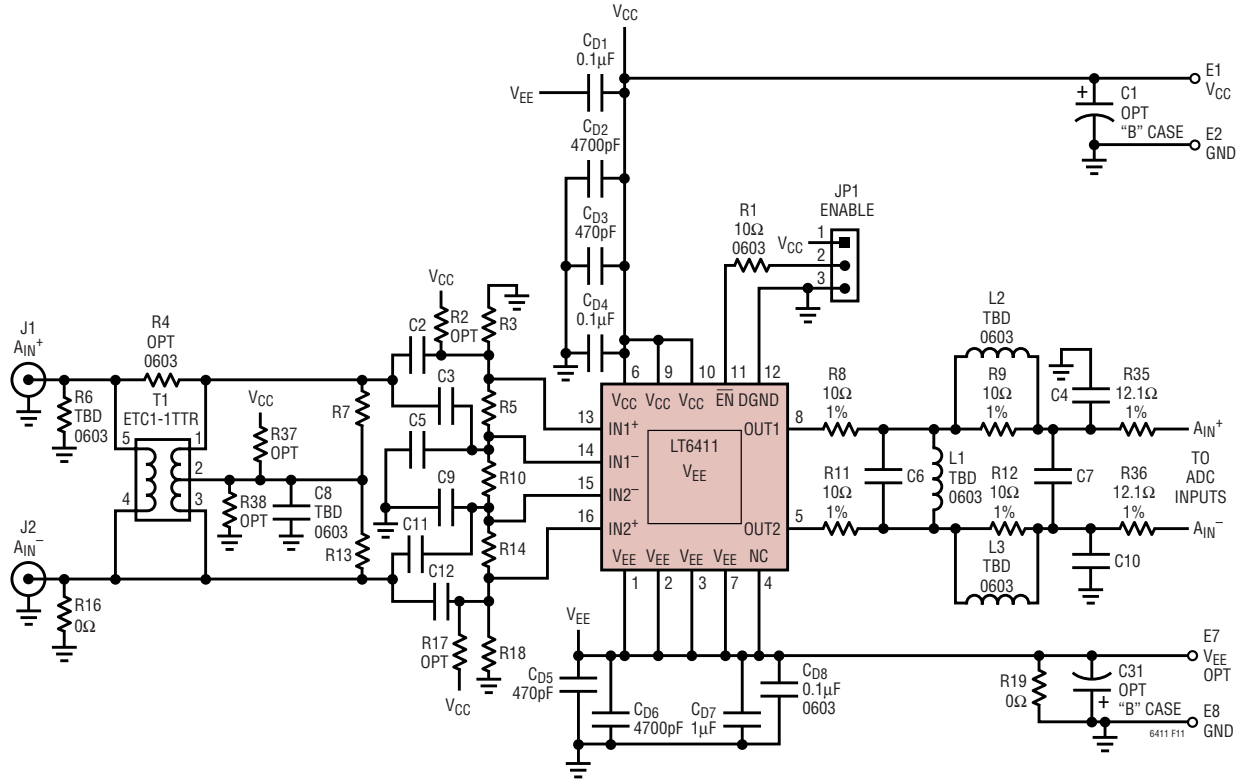


Figure 11. DC1057 Demo Circuit Schematic

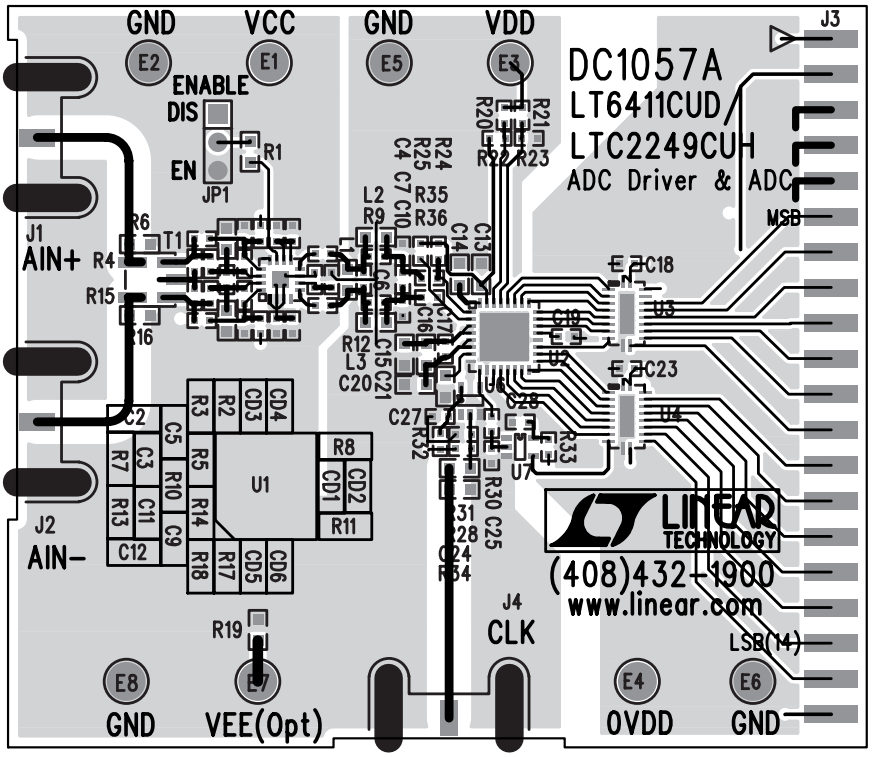
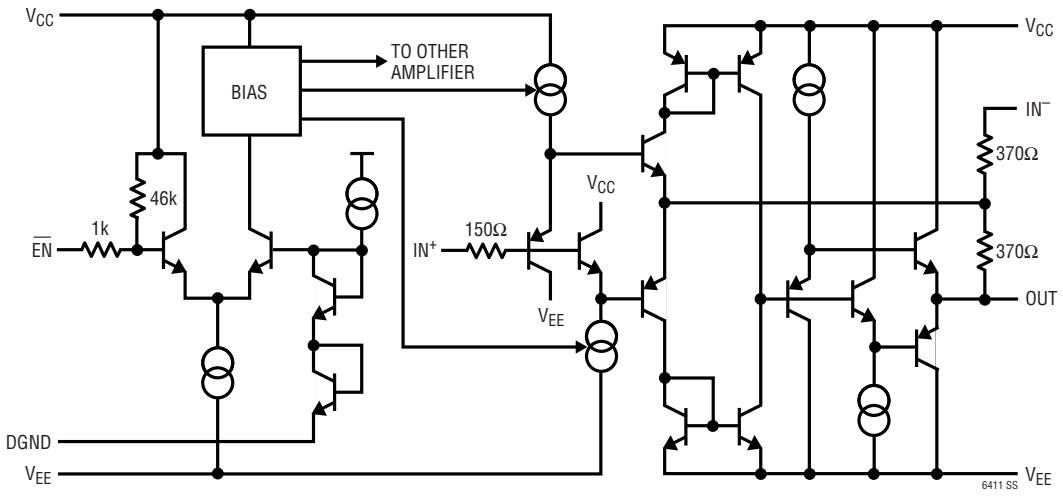


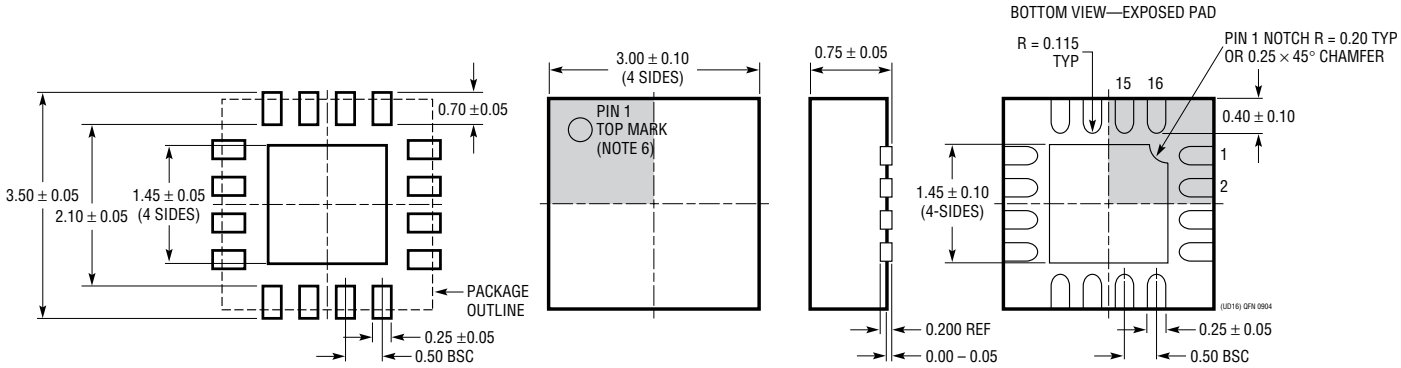
Figure 12. Layout of DC1057 Demo Circuit

SIMPLIFIED SCHEMATIC



PACKAGE DESCRIPTION

UD Package
16-Lead Plastic QFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1691)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE MO-220 VARIATION (WEED-2)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE