

3.3V Single Supply Video Difference Amplifier

FEATURES

- Differential or Single-Ended Gain Block
- Wide Supply Range 3V to 12.6V
- Output Swings Rail-to-Rail
- Input Common Mode Range Includes Ground
- 600V/ μ s Slew Rate
- -3dB Bandwidth = 75MHz, $A_V = \pm 2$
- CMRR at 10MHz: $>60\text{dB}$
- Specified on 3.3V, 5V and $\pm 5\text{V}$ Supplies
- High Output Drive: $\pm 70\text{mA}$
- Power Shutdown to 300 μ A
- Operating Temperature Range: -40°C to 85°C
- Available in 8-Lead SO and Tiny 3mm x 3mm x 0.8mm DFN Packages

APPLICATIONS

- Differential to Single-Ended Conversion
- Video Line Driver
- Automotive Displays
- RGB Amplifiers
- Coaxial Cable Drivers
- Low Voltage High Speed Signal Processing

DESCRIPTION

The LT[®]6552 is a video difference amplifier optimized for low voltage single supply operation. This versatile amplifier features uncommitted high input impedance (+) and (–) inputs and can be used in differential or single-ended configurations. A second set of inputs gives gain adjustment and DC control to the differential amplifier.

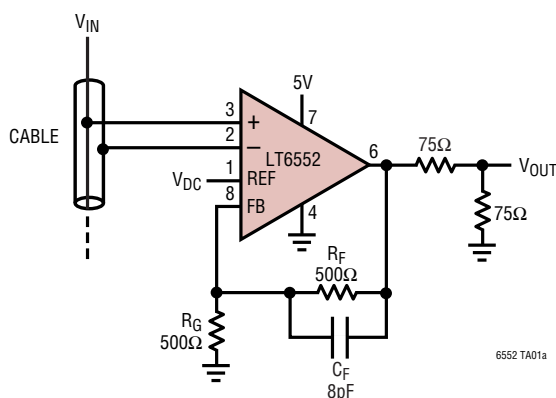
On a single 3.3V supply, the input voltage range extends from ground to 1.3V and the output swings from ground to 2.9V while driving a 150 Ω load. The LT6552 features 75MHz -3dB bandwidth, 600V/ μ s slew rate, and $\pm 70\text{mA}$ output current making it ideal for driving cables directly. The LT6552 maintains its performance for supplies from 3V to 12.6V and is fully specified at 3.3V, 5V and $\pm 5\text{V}$ supplies. The shutdown feature reduces power dissipation to less than 1mW and allows multiple amplifiers to drive the same cable.

The LT6552 is available in the 8-lead SO package as well as a tiny, dual fine pitch leadless package (DFN). The device is specified over the commercial and industrial temperature ranges.

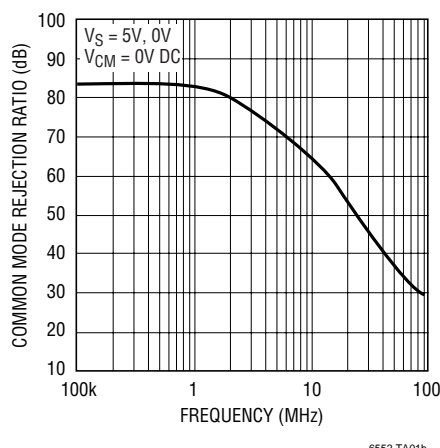
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TYPICAL APPLICATION

Cable Sense Amplifier for Loop Through Connections with DC Adjust



Input Referred CMRR vs Frequency



ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (V^+ to V^-)	12.6V	Specified Temperature Range (Note 5)	-40°C to 85°C
Input Current (Note 2)	$\pm 10\text{mA}$	Maximum Junction Temperature	150°C
Input Voltage Range	V^- to V^+	(DD Package)	125°C
Differential Input Voltage		Storage Temperature Range	-65°C to 150°C
+Input (Pin 3) to -Input (Pin 2)	$\pm V_S$	(DD Package)	-65°C to 125°C
Output Short-Circuit Duration (Note 3)	Indefinite	Lead Temperature	
Operating Temperature Range (Note 4) ...	-40°C to 85°C	(Soldering, 10 sec)	300°C

PACKAGE/ORDER INFORMATION

<p>DD PACKAGE 8-LEAD (3mm x 3mm) PLASTIC DFN $T_{JMAX} = 125^{\circ}\text{C}$, $\theta_{JA} = 160^{\circ}\text{C/W}$ UNDERSIDE METAL CONNECTED TO V^- (PCB CONNECTION OPTIONAL)</p>	ORDER PART NUMBER	<p>S8 PACKAGE 8-LEAD PLASTIC SO $T_{JMAX} = 150^{\circ}\text{C}$, $\theta_{JA} = 100^{\circ}\text{C/W}$</p>	ORDER PART NUMBER
	LT6552CDD LT6552IDD		LT6552CS8 LT6552IS8
	DD PART MARKING*		S8 PART MARKING
	LADR		6552 6552I

*The temperature grade is identified by a label on the shipping container. Consult LTC Marketing for parts specified with wider operating temperature ranges.

3.3V ELECTRICAL CHARACTERISTICS The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^{\circ}\text{C}$. $V_S = 3.3\text{V}$, 0V . Figure 1 shows the DC test circuit, $V_{REF} = V_{CM} = 1\text{V}$, $V_{DIFF} = 0\text{V}$, $V_{SHDN} = V^+$, unless otherwise noted. $R_L = R_F + R_G = 1\text{k}$. (Note 6)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	Both Inputs (Note 7)		5	20	mV
			●		25	mV
$\Delta V_{OS}/\Delta T$	Input V_{OS} Drift			40		$\mu\text{V}/^{\circ}\text{C}$
I_B	Input Bias Current	Any Input		20	50	μA
I_{OS}	Input Offset Current	Either Input Pair		1	5	μA

3.3V ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $V_S = 3.3\text{V}$, 0V . Figure 1 shows the DC test circuit, $V_{\text{REF}} = V_{\text{CM}} = 1\text{V}$, $V_{\text{DIFF}} = 0\text{V}$, $V_{\text{SHDN}} = V^+$, unless otherwise noted. $R_L = R_F + R_G = 1\text{k}$. (Note 6)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
e_n	Input Noise Voltage Density	$f = 10\text{kHz}$		55		$\text{nV}/\sqrt{\text{Hz}}$	
i_n	Input Noise Current Density	$f = 10\text{kHz}$		0.7		$\text{pA}/\sqrt{\text{Hz}}$	
R_{IN}	Input Resistance	Common Mode, $V_{\text{CM}} = 0\text{V}$ to 1.3V		300		$\text{k}\Omega$	
CMRR	Common Mode Rejection Ratio	$V_{\text{CM}} = 0\text{V}$ to 1.3V	●	58	83	dB	
	Input Range		●	0	1.3	V	
PSRR	Power Supply Rejection	$V_S = 3\text{V}$ to 12V	●	48	54	dB	
	Minimum Supply (Note 8)		●	3		V	
G_E	Gain Error	$V_O = 0.5\text{V}$ to 2V , $R_L = 1\text{k}$	●		1	3	%
		$R_L = 150\Omega$	●		1	3	%
V_{OH}	Swing High	$(V_{\text{DIFF}} = 0.4\text{V})$, V_{REF} (Pin 1) = 0V , $A_V = 10$	●	3.1	3.2	V	
		$R_L = 1\text{k}$	●	2.5	2.9	V	
		$R_L = 75\Omega$		2	2.5	V	
V_{OL}	Swing Low	$(V_{\text{DIFF}} = -0.1\text{V})$, V_{REF} (Pin 1) = 0V , $A_V = 10$	●		8	50	mV
		$R_L = 1\text{k}$	●		65	120	mV
		$I_{\text{SINK}} = 5\text{mA}$	●		40	200	mV
SR	Slew Rate	$V_{\text{OUT}} = 0.5\text{V}$ to 2.5V Measure from 1V to 2V , $R_L = 150\Omega$, $A_V = 2$		350		$\text{V}/\mu\text{s}$	
FPBW	Full-Power Bandwidth (Note 9)	$V_O = 2V_{\text{P-P}}$		55		MHz	
BW	Small-Signal -3dB Bandwidth	$A_V = 2$, $R_L = 150\Omega$		65		MHz	
t_r , t_f	Rise Time, Fall Time (Note 10)	$A_V = 50$, $V_O = 0.5\text{V}$ to 2.5V , 20% to 80%, $R_L = 150\Omega$		125	175	ns	
t_s	Settling Time to 3%	$A_V = 2$, $\Delta V_{\text{OUT}} = 2\text{V}$, Positive Step		20		ns	
	Settling Time to 1%	$R_L = 150\Omega$		30		ns	
	Differential Gain	$A_V = 2$, $R_L = 150\Omega$, Output Black Level = 0.6V		0.4		%	
	Differential Phase	$A_V = 2$, $R_L = 150\Omega$, Output Black Level = 0.6V		0.15		Deg	
I_{SC}	Short-Circuit Current	$V_{\text{OUT}} = 0\text{V}$, $V_{\text{DIFF}} = 1\text{V}$	●	35	50	mA	
				25		mA	
I_S	Supply Current		●	12.5	13.5	mA	
	Supply Current, Shutdown	$V_{\text{SHDN}} = 0.5\text{V}$	●		15	mA	
V_L	Shutdown Pin Input Low Voltage		●		0.5	V	
V_H	Shutdown Pin Input High Voltage		●	3		V	
	Shutdown Pin Current	$V_{\text{SHDN}} = 0.5\text{V}$	●	40	150	μA	
		$V_{\text{SHDN}} = 3\text{V}$	●	3	10	μA	
t_{ON}	Turn On-Time	V_{SHDN} from 0.5V to 3V		250		ns	
t_{OFF}	Turn Off-Time	V_{SHDN} from 3V to 0.5V		450		ns	
	Shutdown Output Leakage Current	$V_{\text{SHDN}} = 0.5\text{V}$, $0\text{V} \leq V_{\text{OUT}} \leq V^+$	●	0.25		μA	

5V ELECTRICAL CHARACTERISTICS The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $V_S = 5\text{V}$, 0V ; Figure 1 shows the DC test circuit, $V_{\text{REF}} = V_{\text{CM}} = 1\text{V}$, $V_{\text{DIFF}} = 0\text{V}$, $V_{\text{SHDN}} = V^+$, unless otherwise noted. $R_L = R_F + R_G = 1\text{k}$. (Note 6)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS		
V_{OS}	Input Offset Voltage	Both Inputs (Note 7)	●	5	20	mV		
					25	mV		
$\Delta V_{\text{OS}}/\Delta T$	Input V_{OS} Drift		●	40		$\mu\text{V}/^\circ\text{C}$		
I_B	Input Bias Current	Any Input	●	20	50	μA		
I_{OS}	Input Offset Current	Either Input Pair	●	1	5	μA		
e_n	Input Noise Voltage Density	$f = 10\text{kHz}$		55		$\text{nV}/\sqrt{\text{Hz}}$		
i_n	Input Noise Current Density	$f = 10\text{kHz}$		0.7		$\text{pA}/\sqrt{\text{Hz}}$		
R_{IN}	Input Resistance	Common Mode, $V_{\text{CM}} = 0\text{V}$ to 3V		300		$\text{k}\Omega$		
CMRR	Common Mode Rejection Ratio	$V_{\text{CM}} = 0\text{V}$ to 3V	●	58	83	dB		
	Input Range		●	0	3	V		
PSRR	Power Supply Rejection	$V_S = 3\text{V}$ to 12V	●	48	54	dB		
	Minimum Supply (Note 8)		●	3		V		
G_E	Gain Error	$V_0 = 0.5\text{V}$ to 3.5V , $R_L = 1\text{k}$ $R_L = 150\Omega$	●	1	3	%		
				1	3	%		
V_{OH}	Swing High	$(V_{\text{DIFF}} = 0.6\text{V})$, $V_{\text{REF}}(\text{Pin } 1) = 0\text{V}$, $A_V = 10$ $R_L = 1\text{k}$ $R_L = 150\Omega$ $R_L = 75\Omega$, $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ (Only)	●	4.8	4.875	V		
				3.6	4.3	V		
				2.75	3.4	V		
V_{OL}	Swing Low	$(V_{\text{DIFF}} = -0.1\text{V})$, $V_{\text{REF}}(\text{Pin } 1) = 0\text{V}$, $A_V = 10$ $R_L = 1\text{k}$ $I_{\text{SINK}} = 5\text{mA}$ $I_{\text{SINK}} = 10\text{mA}$	●		8	50	mV	
						65	120	mV
						110	200	mV
SR	Slew Rate	$V_{\text{OUT}} = 0.5\text{V}$ to 3.5V Measure from 1V to 3V , $R_L = 150\Omega$, $A_V = 2$		450		$\text{V}/\mu\text{s}$		
FPBW	Full-Power Bandwidth (Note 9)	$V_0 = 2V_{\text{P-P}}$		70		MHz		
BW	Small-Signal -3dB Bandwidth	$A_V = 2$, $R_L = 150\Omega$		70		MHz		
t_r , t_f	Rise Time, Fall Time	5V , 0V ; $A_V = 50$, $V_0 = 0.5\text{V}$ to 3.5V , 20% to 80%, $R_L = 1\text{k}$		125	175	ns		
t_s	Settling Time to 3%	$A_V = 2$, $\Delta V_{\text{OUT}} = 2\text{V}$, Positive Step $R_L = 150\Omega$		20		ns		
	Settling Time to 1%			30		ns		
	Differential Gain	$A_V = 2$, $R_L = 150\Omega$, Output Black Level = 1V		0.25		%		
	Differential Phase	$A_V = 2$, $R_L = 150\Omega$, Output Black Level = 1V		0.04		Deg		
I_{sc}	Short-Circuit Current	$V_{\text{OUT}} = 0\text{V}$, $V_{\text{DIFF}} = 1\text{V}$ $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	●	50	70	mA		
				45		mA		
				35		mA		
I_S	Supply Current		●	13.5	14.5	mA		
	Supply Current Shutdown	$V_{\text{SHDN}} = 0.5\text{V}$	●		16	mA		
			●	400	900	μA		
V_L	Shutdown Pin Input Low Voltage		●		0.5	V		
V_H	Shutdown Pin Input High Voltage		●	4.7		V		
	Shutdown Pin Current	$V_{\text{SHDN}} = 0.5\text{V}$ $V_{\text{SHDN}} = 4.7\text{V}$	●	60	200	μA		
				4	10	μA		

5V ELECTRICAL CHARACTERISTICS The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $V_S = 5\text{V}$, 0V . Figure 1 shows the DC test circuit, $V_{\text{REF}} = V_{\text{CM}} = 1\text{V}$, $V_{\text{DIFF}} = 0\text{V}$, $V_{\text{SHDN}} = V^+$, unless otherwise noted. $R_L = R_F + R_G = 1\text{k}$. (Note 6)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{ON}	Turn-On Time	V_{SHDN} from 0.5V to 4.7V		250		ns
t_{OFF}	Turn-Off Time	V_{SHDN} from 4.7V to 0.5V		450		ns
	Shutdown Output Leakage Current	$V_{\text{SHDN}} = 0.5\text{V}$, $0\text{V} \leq V_{\text{OUT}} \leq V^+$	●	0.25		μA

±5V ELECTRICAL CHARACTERISTICS The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $V_S = \pm 5\text{V}$. Figure 2 shows the DC test circuit, $V_{\text{REF}} = V_{\text{CM}} = 0\text{V}$, $V_{\text{DIFF}} = 0\text{V}$, $V_{\text{SHDN}} = V^+$, unless otherwise noted. $R_L = R_F + R_G = 1\text{k}$. (Note 6)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	Both Inputs (Note 7)		10	25 30	mV mV
$\Delta V_{\text{OS}}/\Delta T$	Input V_{OS} Drift			50		$\mu\text{V}/^\circ\text{C}$
I_{B}	Input Bias Current	Any Input		25	50	μA
I_{OS}	Input Offset Current	Either Input Pair		1	5	μA
e_{n}	Input Noise Voltage Density	$f = 10\text{kHz}$		55		$\text{nV}/\sqrt{\text{Hz}}$
i_{n}	Input Noise Current Density	$f = 10\text{kHz}$		0.7		$\text{pA}/\sqrt{\text{Hz}}$
R_{IN}	Input Resistance	Common Mode, $V_{\text{CM}} = -5\text{V}$ to 3V		300		$\text{k}\Omega$
CMRR	Common Mode Rejection Ratio	$V_{\text{CM}} = -5\text{V}$ to 3V	●	58	75	dB
	Input Range		●	-5	3	V
PSRR	Power Supply Rejection	$V_S = \pm 2\text{V}$ to $\pm 6\text{V}$, $V_{\text{CM}} = 0\text{V}$	●	48	54	dB
G_{E}	Gain Error	$V_0 = -3\text{V}$ to 3V , $R_L = 1\text{k}$ $R_L = 150\Omega$	● ●	1	3 3	% %
	Output Voltage Swing	$(V_{\text{DIFF}} = \pm 0.6\text{V})$, V_{REF} (Pin 1) = 0V , $A_V = 10$ $R_L = 1\text{k}$ $R_L = 150\Omega$ $R_L = 75\Omega$, $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ (Only)	● ● ●	± 4.8 ± 3.6 ± 2.75	± 4.875 ± 4.3 ± 3.4	V V V
SR	Slew Rate	$V_{\text{CM}} = 0\text{V}$, $V_{\text{DIFF}} = -1.5\text{V}$ to $+1.5\text{V}$, $V_0 = -5\text{V}$ to 5V Measure from -2V to 2V , $R_L = 150\Omega$		400	600	$\text{V}/\mu\text{s}$
FPBW	Full-Power Bandwidth	$V_0 = 6V_{\text{P-P}}$ (Note 9)		30		MHz
BW	Small-Signal -3dB Bandwidth	$A_V = 2$, $R_L = 150\Omega$		75		MHz
t_r , t_f	Rise Time, Fall Time	$A_V = 50$, $V_0 = -3\text{V}$ to 3V , 20% to 80%		125	175	ns
t_s	Settling Time to 3% Settling Time to 1%	$A_V = 2$, $\Delta V_{\text{OUT}} = 6\text{V}$, Positive Step $R_L = 150\Omega$		25 35		ns ns
	Differential Gain	$A_V = 2$, $R_L = 150\Omega$, Output Black Level = 0V		0.2		%
	Differential Phase	$A_V = 2$, $R_L = 150\Omega$, Output Black Level = 0V		0.15		Deg
I_{SC}	Short-Circuit Current	$V_{\text{OUT}} = 0\text{V}$, $V_{\text{DIFF}} = \pm 1\text{V}$ $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	● ●	50 45 35	70	mA mA mA
	Supply Current Shutdown	$V_{\text{SHDN}} = -4.5\text{V}$	●	650	1400	μA
I_{S}	Supply Current			14	16.5 18.5	mA mA
V_{L}	Shutdown Pin Input Low Voltage		●		-4.5	V
V_{H}	Shutdown Pin Input High Voltage		●	4.7		V

±5V ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $V_S = \pm 5\text{V}$. Figure 2 shows the DC test circuit, $V_{\text{REF}} = V_{\text{CM}} = 0\text{V}$, $V_{\text{DIFF}} = 0\text{V}$, $V_{\text{SHDN}} = V^+$, unless otherwise noted. $R_L = R_F + R_G = 1\text{k}$. (Note 6)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
	Shutdown Pin Current	$V_{\text{SHDN}} = -4.5\text{V}$ $V_{\text{SHDN}} = 4.7\text{V}$	●	85 3	250 10	μA μA
t_{ON}	Turn-On Time	V_{SHDN} from -4.5V to 4.7V		200		ns
t_{OFF}	Turn-Off Time	V_{SHDN} from 4.7V to -4.5V		400		ns
	Shutdown Output Leakage Current	$V_{\text{SHDN}} = -4.5\text{V}$, $V^- \leq V_{\text{OUT}} \leq V^+$	●	0.25		μA

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: The inputs are protected from ESD with diodes to the supplies.

Note 3: A heat sink may be required to keep the junction temperature below absolute maximum.

Note 4: The LT6552C/LT6552I are guaranteed functional over the temperature range of -40°C to 85°C .

Note 5: The LT6552C is guaranteed to meet specified performance from 0°C to 70°C and is designed, characterized and expected to meet specified performance from -40°C to 85°C , but is not tested or QA sampled at these temperatures. The LT6552I is guaranteed to meet specified performance from -40°C to 85°C .

Note 6: When $R_L = 1\text{k}$ is specified, the load resistor is $R_F + R_G$, but when $R_L = 150\Omega$ or $R_L = 75\Omega$ is specified, then an additional resistor of that value is added to the output.

Note 7: V_{OS} measured at the output (Pin 6) is the contribution from both input pairs and is input referred.

Note 8: Minimum supply is guaranteed by the PSRR test.

Note 9: Full power bandwidth is calculated from the slew rate.

$$\text{FPBW} = \text{SR}/2\pi V_p$$

Note 10: $V_S = 3.3\text{V}$, t_r and t_f limits are guaranteed by correlation to $V_S = 5\text{V}$ and $\pm 5\text{V}$ tests.

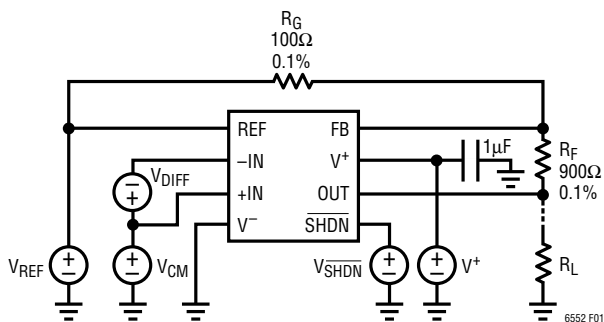


Figure 1. 3.3V, 5V DC Test Circuit

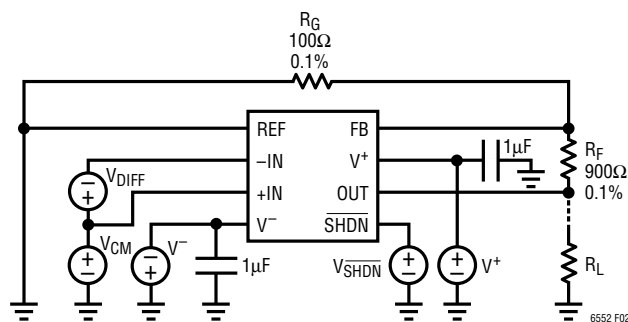
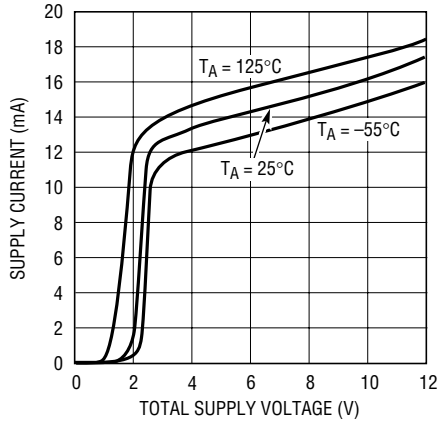


Figure 2. ±5V DC Test Circuit

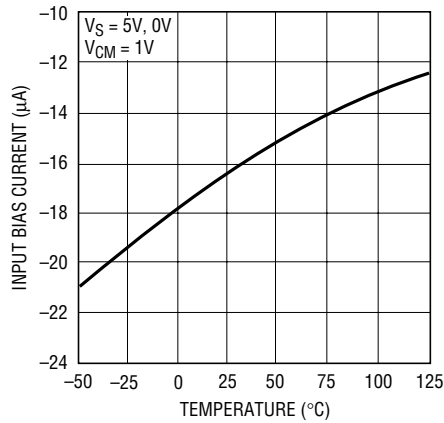
TYPICAL PERFORMANCE CHARACTERISTICS

Supply Current vs Supply Voltage



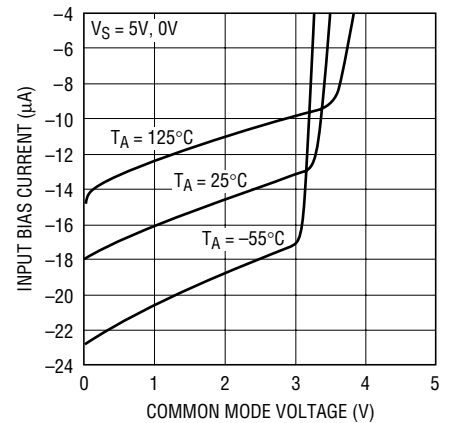
6552 G01

Input Bias Current vs Temperature



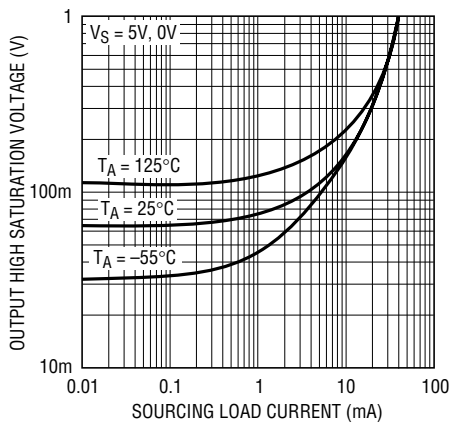
6552 G02

Input Bias Current vs Common Mode Voltage



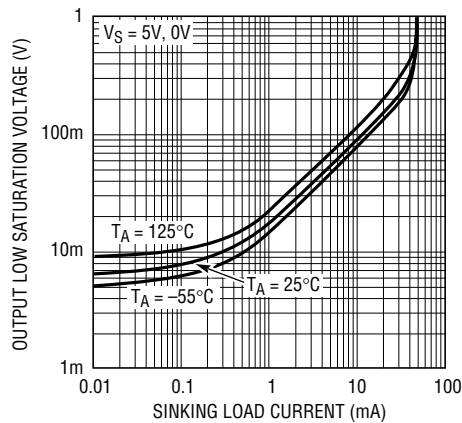
6552 G03

Output Saturation Voltage vs Load Current (Output High)



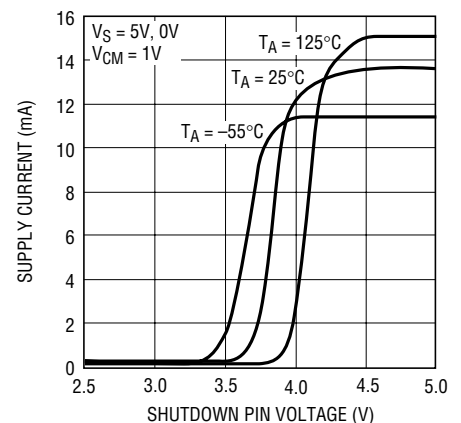
6552 G04

Output Saturation Voltage vs Load Current (Output Low)



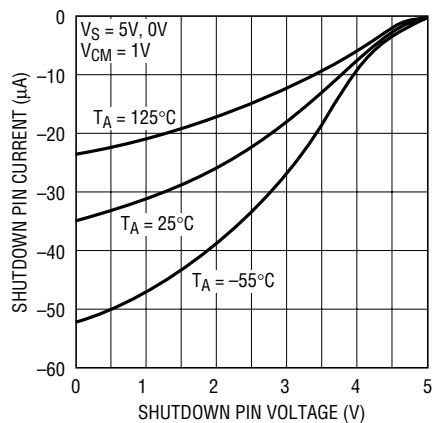
6552 G05

Supply Current vs Shutdown Pin Voltage



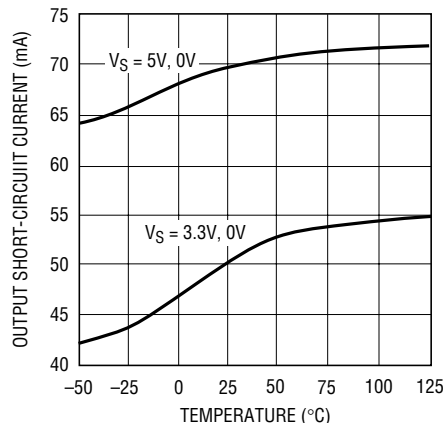
6552 G06

Shutdown Pin Current vs Shutdown Pin Voltage



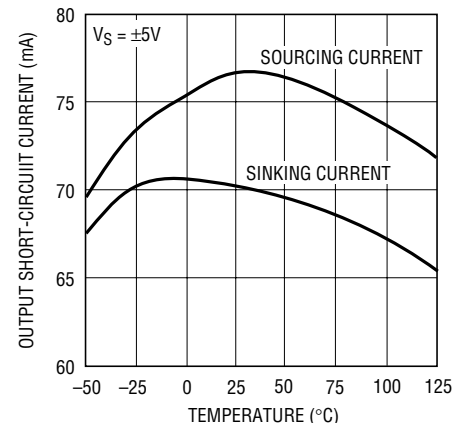
6552 G07

Output Short-Circuit Current vs Temperature



6552 G08

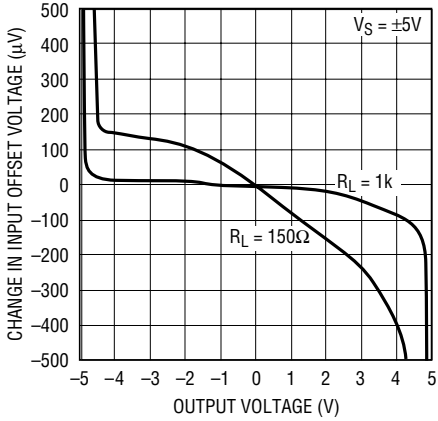
Output Short-Circuit Current vs Temperature



6552 G09

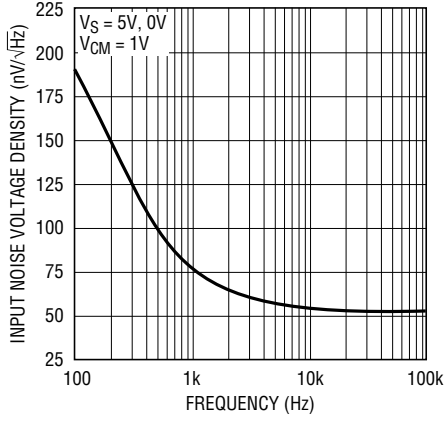
TYPICAL PERFORMANCE CHARACTERISTICS

Open-Loop Gain



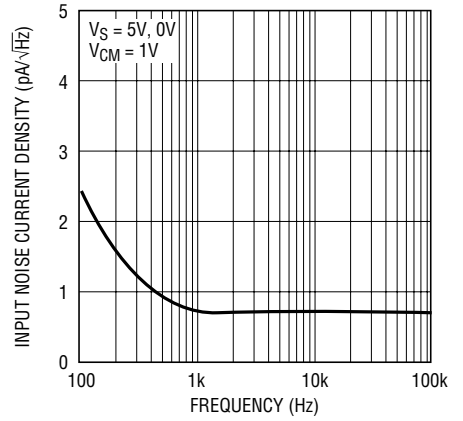
6552 G10

Input Noise Voltage Density vs Frequency



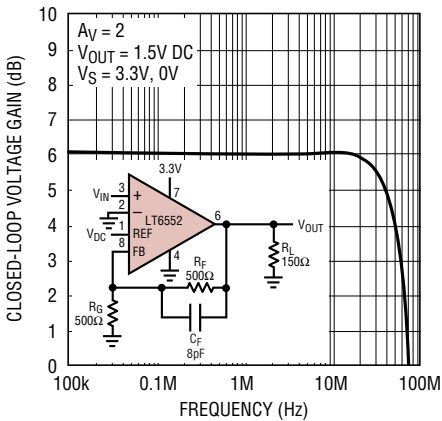
6552 G11

Input Noise Current Density vs Frequency



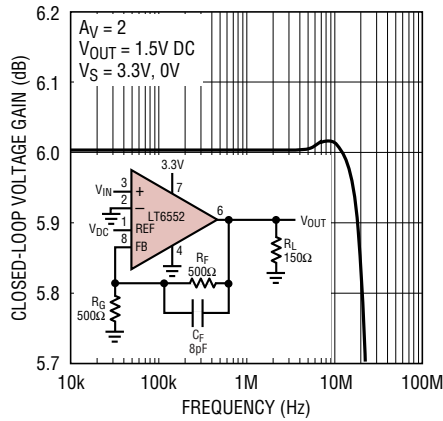
6552 G12

Closed-Loop Voltage Gain vs Frequency



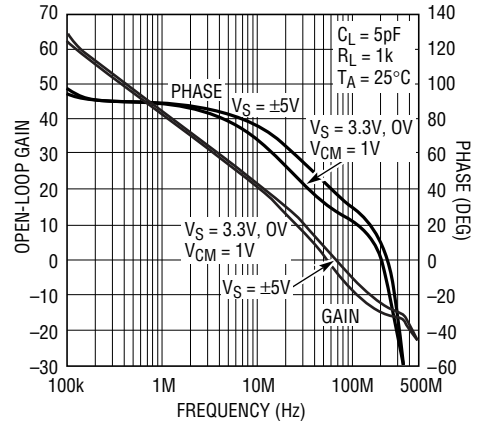
6552 G13

Gain Flatness vs Frequency



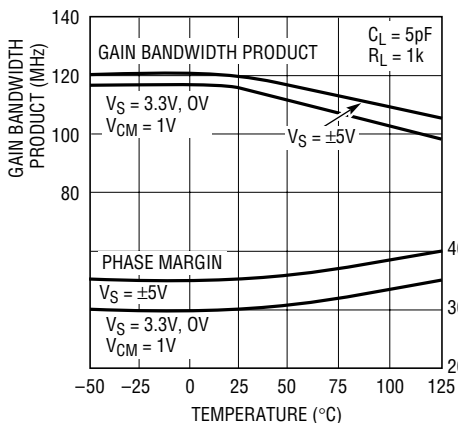
6552 G14

Open-Loop Gain and Phase vs Frequency



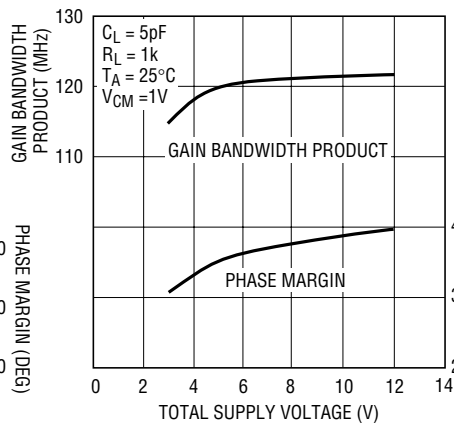
6552 G15

Gain Bandwidth Product and Phase Margin vs Temperature



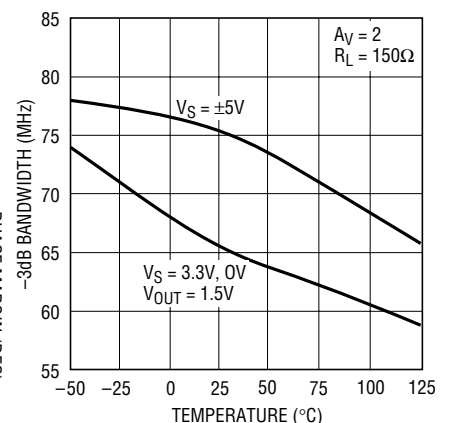
6552 G16

Gain Bandwidth Product and Phase Margin vs Supply Voltage



6552 G17

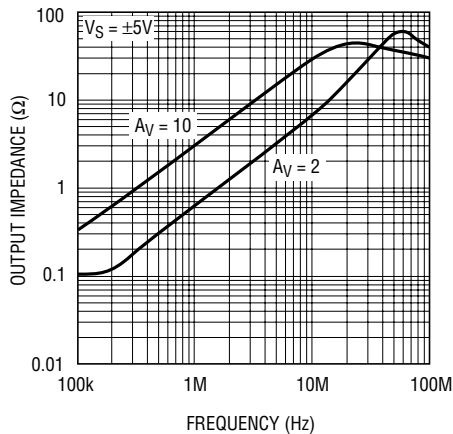
-3dB Bandwidth vs Temperature



6552 G18

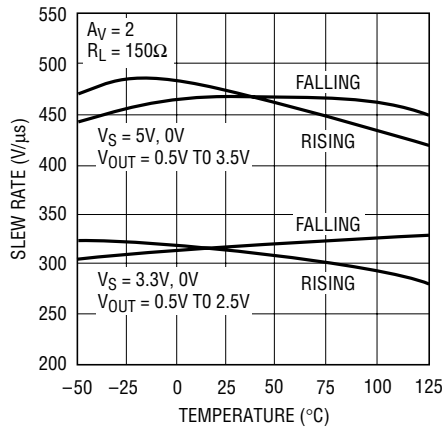
TYPICAL PERFORMANCE CHARACTERISTICS

Output Impedance vs Frequency



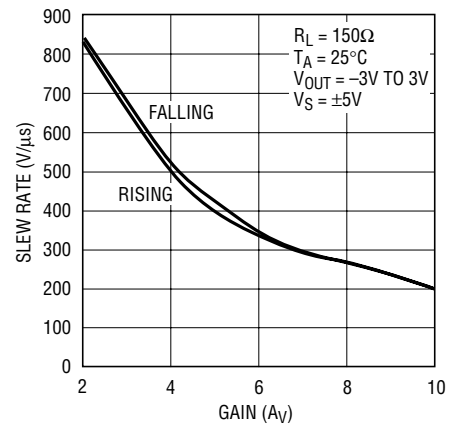
6552 G19

Slew Rate vs Temperature



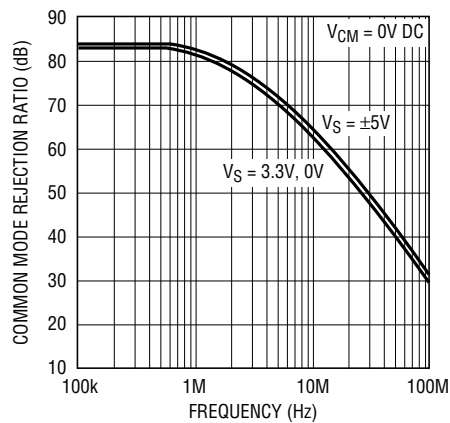
6552 G20

Slew Rate vs Closed-Loop Gain



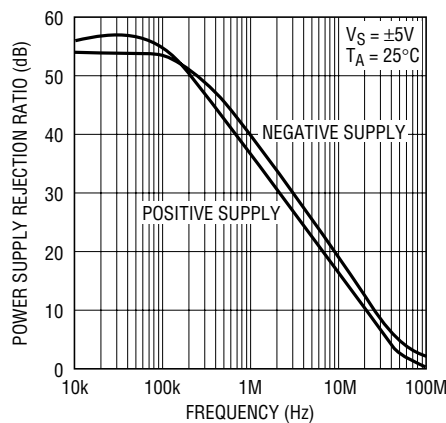
6552 G21

Common Mode Rejection Ratio vs Frequency



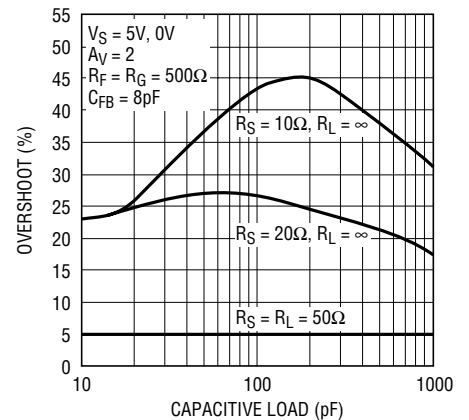
6552 G22

Power Supply Rejection Ratio vs Frequency



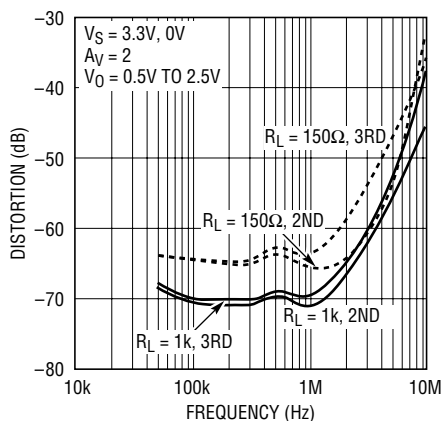
6552 G23

Series Output Resistor vs Capacitive Load



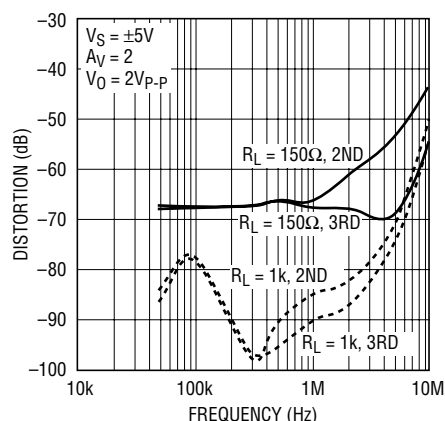
6552 G24

2nd and 3rd Harmonic Distortion vs Frequency



6552 G25

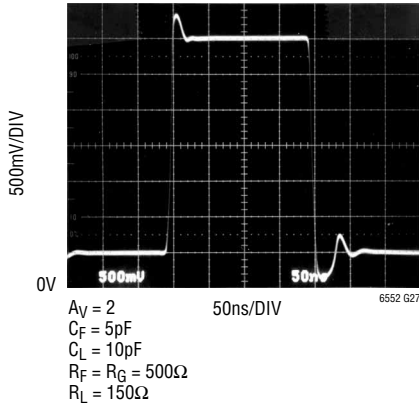
2nd and 3rd Harmonic Distortion vs Frequency



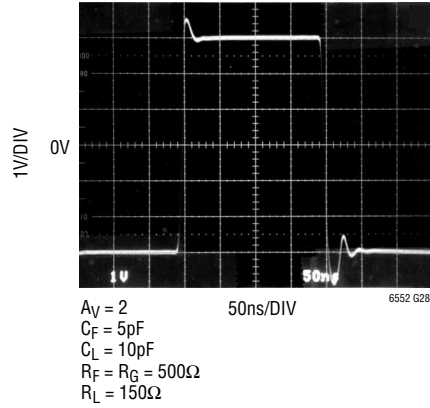
6552 G26

TYPICAL PERFORMANCE CHARACTERISTICS

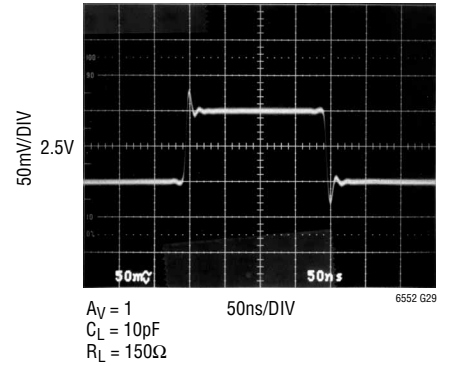
**Large Signal Response,
 $V_S = 5V, 0V$**



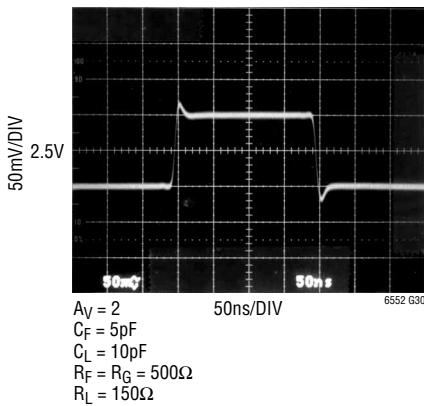
**Large Signal Response,
 $V_S = \pm 5V$**



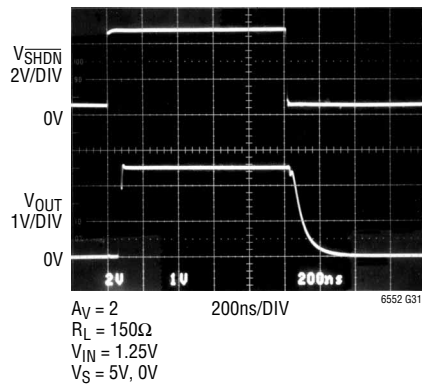
**Small Signal Response,
 $V_S = 5V, 0V$**



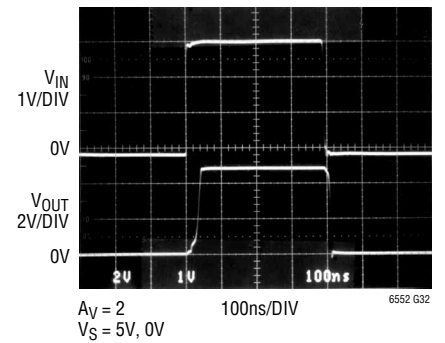
**Small Signal Response,
 $V_S = 5V, 0V$**



Shutdown Response



Output Overdrive Recovery



APPLICATIONS INFORMATION

The LT6552 is a video difference amplifier with two pairs of high impedance inputs. The primary purpose of the LT6552 is to convert high frequency differential signals into a single-ended output, while rejecting any common mode noise. In the simplest configuration, one pair of inputs is connected to the incoming differential signal, while the other pair of inputs is used to set amplifier gain and DC level. The device will operate on either single or dual supplies and has an input common mode range which includes the negative supply. The common mode rejection ratio is greater than 60dB at 10MHz. Feedback is

applied to Pin 8 and the LT6552's transient response is optimized for gains of 2 or greater.

Figure 3 shows the single supply connection. The amplifier gain is set by a feedback network from the output to Pin 8 (FB). A DC signal applied to Pin 1 (REF) establishes the output quiescent voltage and the differential signal is applied to Pins 2 and 3.

Figure 4 shows several other connections using dual supplies. In each case, the amplifier gain is set by a feedback network from the output to Pin 8 (FB).

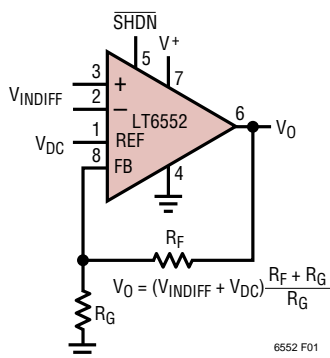


Figure 3

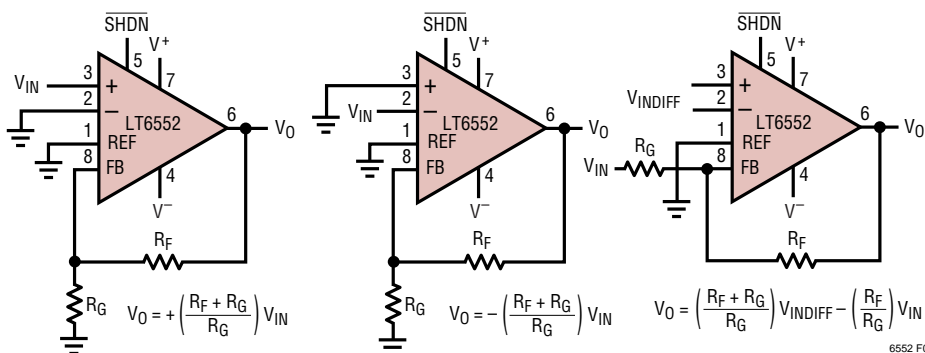


Figure 4

APPLICATIONS INFORMATION

Amplifier Characteristics

Figure 5 shows a simplified schematic of the LT6552. There are two input stages; the first one consists of transistors Q1 to Q8 for the (+) and (-) inputs while the second input stage consists of transistors Q9 to Q16 for the reference and feedback inputs. This topology provides high slew rates at low supply voltages. The input common mode range extends from ground to typically 1.75V from V_{CC} , and is limited by $2V_{BE}$'s plus a saturation voltage of current sources I1-I4. Each input stage drives the degeneration resistors of PNP and NPN current mirrors, Q17 to Q20, that convert the differential signals into a single-ended output. The complementary drive generator supplies current to the output transistors that swing from rail-to-rail.

The current generated through R1 or R2, divided by the capacitor CM, determines the slew rate. Note that this current, and hence the slew rate, are proportional to the magnitude of the input step. The input step equals the output step divided by the closed-loop gain. The highest slew rates are therefore obtained in the lowest gain configurations. The Typical Performance Characteristic Curve of Slew Rate vs Closed-Loop Gain shows the details.

ESD

The LT6552 has reverse-biased ESD protection diodes on all inputs and outputs, as shown in Figure 5. If these pins are forced beyond either supply, unlimited current will flow through these diodes. If the current is transient in nature and limited to 100mA or less, no damage to the device will occur.

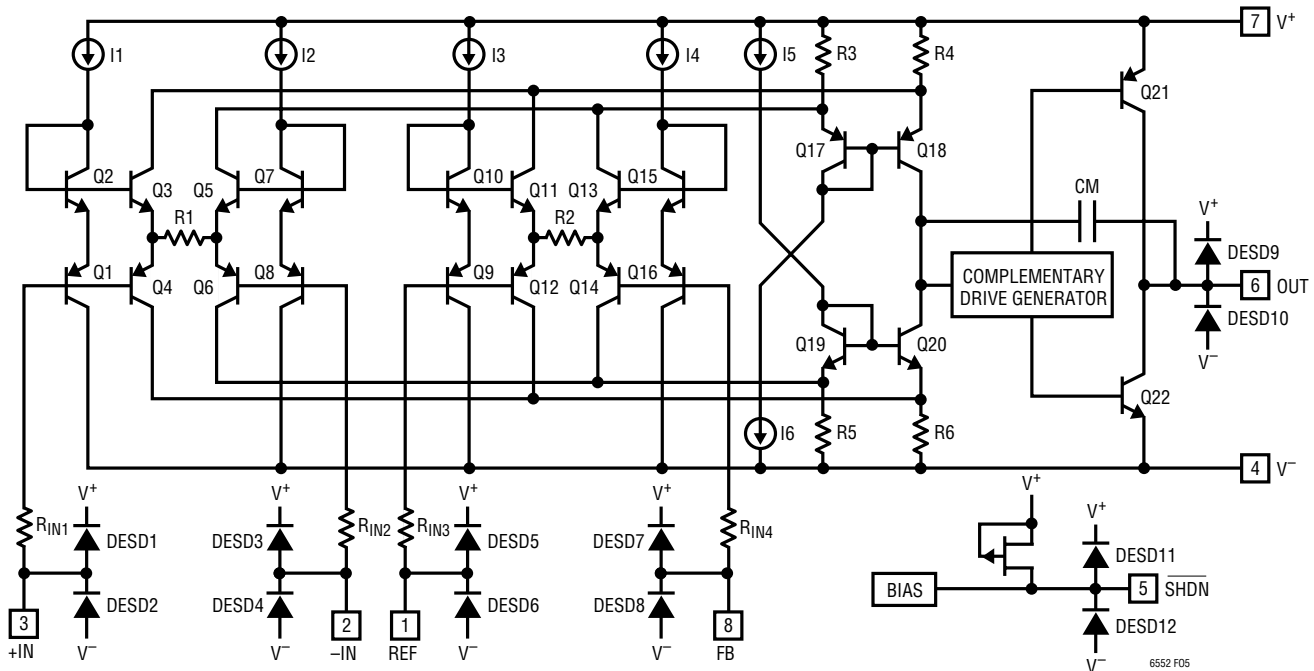


Figure 5. Simplified Schematic

APPLICATIONS INFORMATION

Layout and Passive Components

With a bandwidth of 75MHz and a slew rate of 600V/ μ s, the LT6552 requires special attention to board layout and supply bypassing. Use a ground plane, short lead lengths and RF quality low ESR supply bypass capacitors. The positive supply pin should be bypassed with a small capacitor (typically 0.1 μ F) within 1 inch of the pin. When driving loads greater than 10mA, an additional 4.7 μ F electrolytic capacitor should be used. When using split supplies, the same is true for the negative supply pin. The parallel combination of the feedback resistor and gain setting resistor on Pin 8 (FB) can combine with the input capacitance to form a pole which can degrade stability. In general, use feedback resistors of 1k or less.

Operating with Low Closed-Loop Gains

The LT6552 has been optimized for closed-loop gains of 2 or greater. For a closed-loop gain of 2 the response peaks about 3dB. Peaking can be reduced by using low value feedback resistors, and can be eliminated by placing a capacitor across the feedback resistor (feedback zero). Figure 6 shows the closed-loop gain of 2 frequency response with various values of the feedback capacitor. This peaking shows up as a time domain overshoot of 40%; with an 8pF feedback capacitor the overshoot is eliminated. Figures 7A and 7B show the Small Signal Response of the LT6552 with and without an 8pF feedback capacitor.

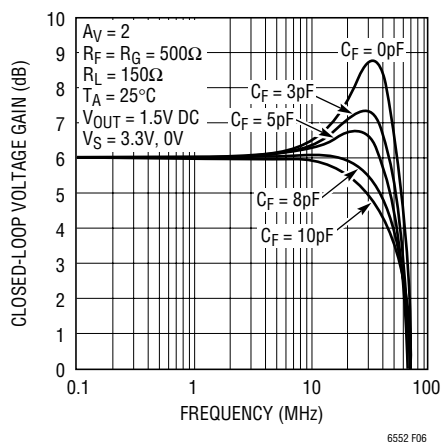


Figure 6. Closed-Loop Gain vs Frequency

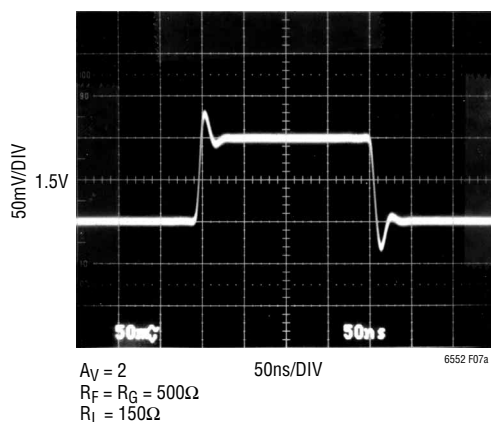


Figure 7A. Small Signal Transient Response, $V_S = 3.3\text{V}, 0\text{V}$

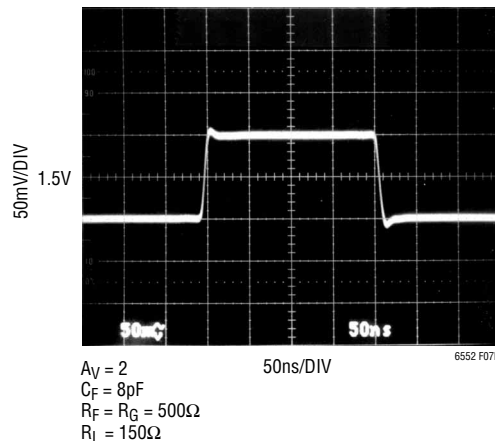


Figure 7B. Small Signal Transient Response, $V_S = 3.3\text{V}, 0\text{V}$ with 8pF Feedback Capacitor

APPLICATIONS INFORMATION

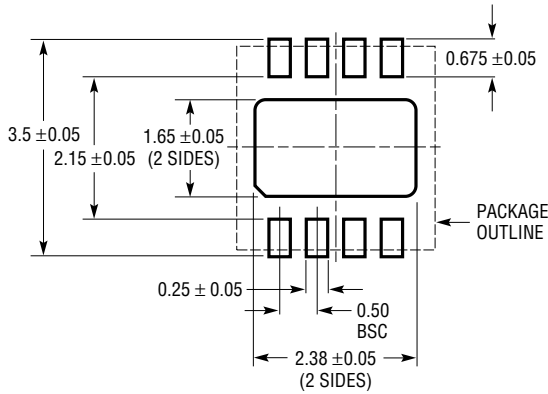
SHDN Pin

The LT6552 includes a shutdown feature that disables the part, reducing quiescent current and making the output high impedance. The part can be shutdown by bringing the SHDN pin within 0.5V of V^- . When shutdown the supply current is typically 400 μ A and the output leakage current

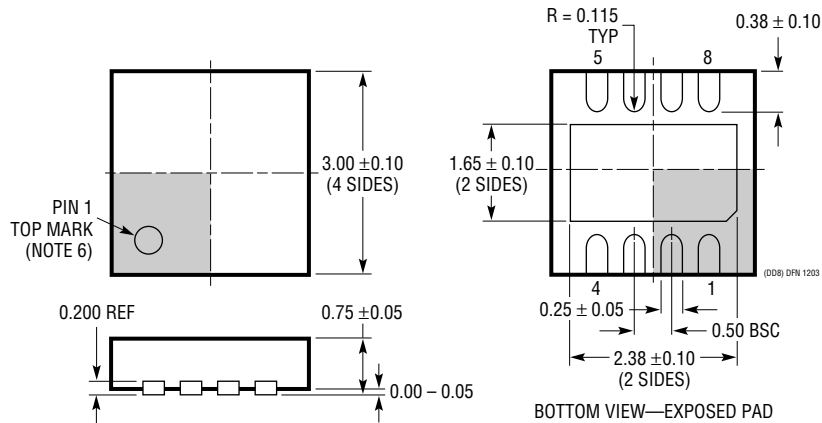
is 0.25 μ A ($V^- \leq V_{OUT} \leq V^+$). In normal operation the SHDN can be tied to V^+ or left floating; if the pin is left unconnected, an internal FET pull-up will keep the LT6552 fully operational.

PACKAGE DESCRIPTION

DD Package
8-Lead Plastic DFN (3mm \times 3mm)
 (Reference LTC DWG # 05-08-1698)



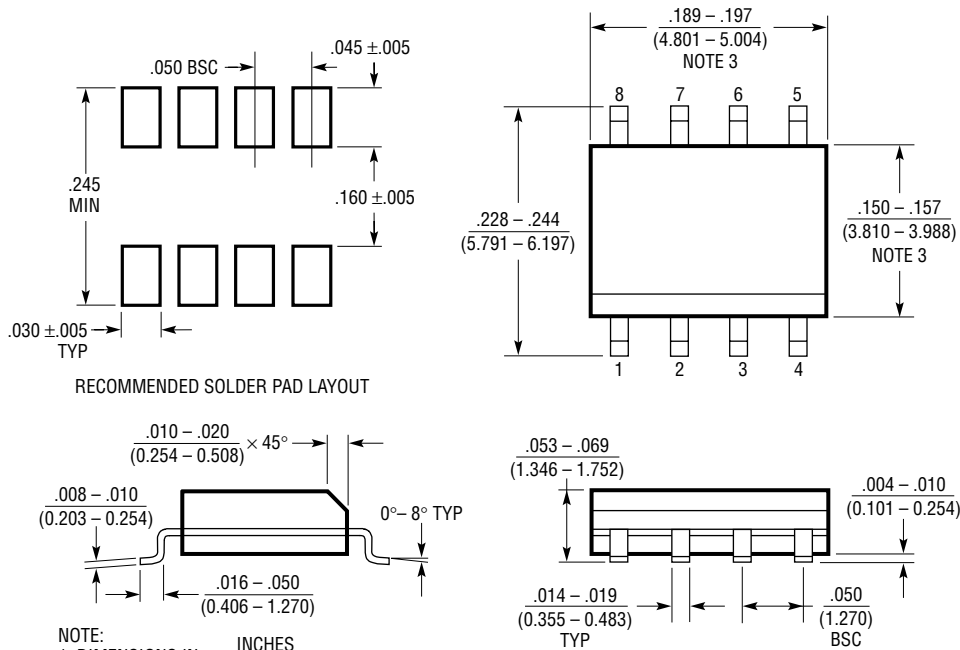
RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



- NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-1)
 2. DRAWING NOT TO SCALE
 3. ALL DIMENSIONS ARE IN MILLIMETERS
 4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
 5. EXPOSED PAD SHALL BE SOLDER PLATED
 6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

S8 Package 8-Lead Plastic Small Outline (Narrow .150 Inch) (Reference LTC DWG # 05-08-1610)



- NOTE:
 1. DIMENSIONS IN $\frac{\text{INCHES}}{\text{MILLIMETERS}}$
 2. DRAWING NOT TO SCALE
 3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
 MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED $.006''$ (0.15mm)

S08 0303