650MHz Gain of 2 Triple Video Amplifier

FEATURES

- **650MHz –3dB Small Signal Bandwidth**
- **400MHz –3dB $2V_{P-P}$ Large Signal Bandwidth**
- **150MHz ±0.1dB Bandwidth**
- **High Slew Rate: 2500V/µs**
- **Fixed Gain of 2 Requires No External Resistors**
- 75dB Channel Separation at 10MHz
- 50dB Channel Separation at 100MHz
- –82dBc 2nd Harmonic Distortion at 10MHz, $2V_{P-P}$
- –72dBc 3rd Harmonic Distortion at 10MHz, $2V_{P-P}$
- Low Supply Current: 8mA per Amplifier
- 6ns 0.1% Settling Time for 2V Step
- TTL Compatible Enable $I_{SS} \leq 100\mu A$ when Disabled
- Differential Gain of 0.022%, Differential Phase of 0.006°
- Wide Supply Range: ±2.25V (4.5V) to ±6V (12V)
- Available in 16-Lead SSOP Package

APPLICATIONS

- RGB Amplifiers
- Coaxial Cable Drivers
- LCD Projectors

DESCRIPTION

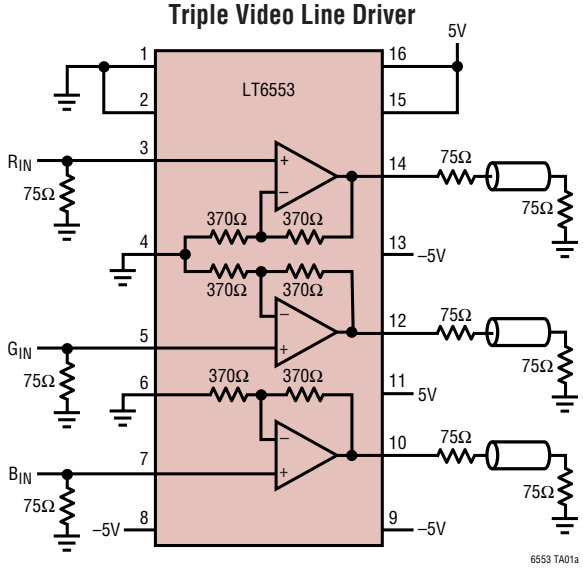
The LT®6553 is a high-speed triple video amplifier with an internally fixed gain of 2. The individual amplifiers are optimized for performance with a double terminated 75Ω video load and feature a $2V_{P-P}$ full signal bandwidth of 400MHz, making them ideal for driving very high-resolution video signals. Separate power supply pins for each amplifier boost channel separation to 75dB, allowing the LT6553 to excel in many high-speed applications.

While the performance of the LT6553 is optimized for dual supply operation, it can also be used on a single supply as small as 4.5V. Using dual 5V supplies, each amplifier draws only 8mA. When disabled, the amplifiers draw less than 100µA and the output pins become high impedance. Furthermore, the amplifiers are capable of turning on in less than 50ns, making them ideal for multiplexing and portable applications.

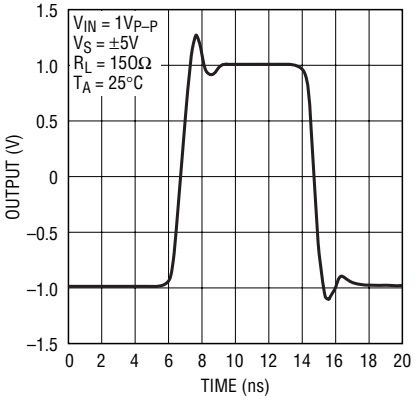
The LT6553 is manufactured on Linear Technology's proprietary low voltage complementary bipolar process and is available in the 16-lead SSOP package that fits in the same PCB area as an SO-8 package.

TYPICAL APPLICATION

Triple Video Line Driver



Large Signal Transient Response

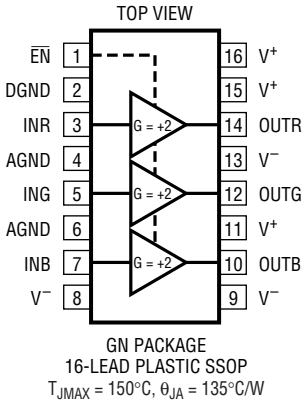


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Total Supply Voltage (V^+ to V^-) 13.2V
Input Current (Note 2) ..... ±10mA
Output Current (Continuous) ..... ±70mA
$\overline{EN}$ to DGND Voltage (Note 2) 5.5V
Output Short-Circuit Duration (Note 3) ..... Indefinite
Operating Temperature Range (Note 4) ... –40°C to 85°C
Specified Temperature Range (Note 5) .... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Junction Temperature ..... 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



GN PACKAGE
16-LEAD PLASTIC SSOP
T_{JMAX} = 150°C, θ_{JA} = 135°C/W

ORDER PART NUMBER
LT6553CGN LT6553IGN
GN PART MARKING
6553 6553I

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_S = ±5V, R_L = 150Ω, C_L = 1.5pF, $V_{\overline{EN}}$ = 0.4V, V_{AGND}, V_{DGND} = 0V.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Referred Offset Voltage	V_{IN} = 0V, V_{OS} = V_{OUT}/2	 ●		3	±10 ±20	mV mV
I_{IN}	Input Current		●		–17	±50	µA
R_{IN}	Input Resistance	V_{IN} = ±1V	●	150	400		kΩ
C_{IN}	Input Capacitance	f = 100kHz			1		pF
PSRR	Power Supply Rejection Ratio	V_S (Total) = 4.5V to 12V (Note 6)	●	56	62		dB
I_{PSRR}	Input Current Power Supply Rejection	V_S (Total) = 4.5V to 12V (Note 6)	●		1	±4	µA/V
A_V ERR	Gain Error	V_{OUT} = ±2V	●		–1.2	±5	%
A_V MATCH	Gain Matching	Any One Channel to Another			±1		%
V_{OUT}	Maximum Output Voltage Swing	 ●	 ●	±3.25 ±3.1	±3.5		V V
I_S	Supply Current, Per Amplifier	 ●	 ●		8	11 14	mA mA
	Supply Current, Disabled, Total	$V_{\overline{EN}}$ = 4V $V_{\overline{EN}}$ = Open	● ●		22 0.5	100 100	µA µA
$I_{\overline{EN}}$	Enable Pin Current	$V_{\overline{EN}}$ = 0.4V $V_{\overline{EN}}$ = V^+	● ●	–200	–95 0.5	 50	µA µA
I_{SC}	Output Short-Circuit Current	R_L = 0Ω, V_{IN} = ±1V	●	±50	±105		mA
SR	Slew Rate	±1V on ±2V Output Step (Note 9)		1700	2500		V/µs
–3dB BW	Small Signal –3dB Bandwidth	V_{OUT} = 200mV_{P-P}			650		MHz
0.1dB BW	Gain Flatness ±0.1dB Bandwidth	V_{OUT} = 200mV_{P-P}			150		MHz

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_S = ±5V, R_L = 150Ω, C_L = 1.5pF, $V_{\overline{EN}}$ = 0.4V, V_{AGND}, V_{DGND} = 0V.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
FPBW	Full Power Bandwidth 2V	V_{OUT} = $2V_{P-P}$ (Note 7)		270	400		MHz
FPBW	Full Power Bandwidth 4V	V_{OUT} = $4V_{P-P}$ (Note 7)			200		MHz
	All-Hostile Crosstalk	f = 10MHz, V_{OUT} = $2V_{P-P}$ f = 100MHz, V_{OUT} = $2V_{P-P}$			–75 –50		dB dB
t_S	Settling Time	0.1% of V_{FINAL}, V_{STEP} = 2V			6		ns
t_R, t_F	Small-Signal Rise and Fall Time	10% to 90%, V_{OUT} = $200mV_{P-P}$			550		ps
dG	Differential Gain	(Note 8)			0.022		%
dP	Differential Phase	(Note 8)			0.006		Deg
HD2	2nd Harmonic Distortion	f = 10MHz, V_{OUT} = $2V_{P-P}$			–82		dBc
HD3	3rd Harmonic Distortion	f = 10MHz, V_{OUT} = $2V_{P-P}$			–72		dBc

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: This parameter is guaranteed to meet specified performance through design and characterization. It is not production tested.

Note 3: As long as output current and junction temperature are kept below the Absolute Maximum Ratings, no damage to the part will occur. Depending on the supply voltage, a heat sink may be required.

Note 4: The LT6553C is guaranteed functional over the operating temperature range of –40°C to 85°C.

Note 5: The LT6553C is guaranteed to meet specified performance from 0°C to 70°C. The LT6553C is designed, characterized and expected to meet specified performance from –40°C and 85°C but is not tested or QA sampled at these temperatures. The LT6553I is guaranteed to meet specified performance from –40°C to 85°C.

Note 6: The two supply voltage settings for power supply rejection are shifted from the typical $±V_S$ points for ease of testing. The first measurement is taken at V^+ = 3V, $V^–$ = –1.5V to provide the required 3V headroom for the enable circuitry to function with $\overline{EN}$, DGND, AGND and all inputs connected to 0V. The second measurement is taken at V^+ = 8V, $V^–$ = –4V.

Note 7: Full power bandwidth is calculated from the slew rate:

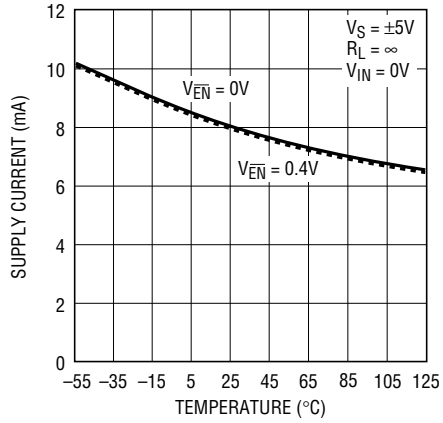
$FPBW = SR/(\pi \bullet V_{P-P})$

Note 8: Differential gain and phase are measured using a Tektronix TSG120YC/NTSC signal generator and a Tektronix 1780R video measurement set. The resolution of this equipment is better than 0.05% and 0.05°. Nine identical amplifier stages were cascaded giving an effective resolution of better than 0.0056% and 0.0056%.

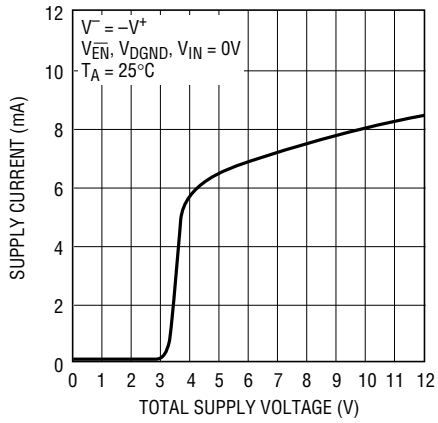
Note 9: Slew rate is 100% production tested on the G channel. Slew rate of the R and B channels is guaranteed through design and characterization.

TYPICAL PERFORMANCE CHARACTERISTICS

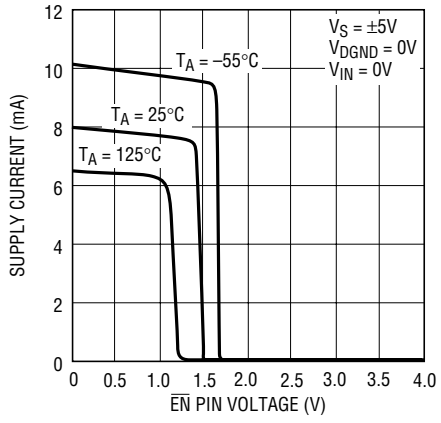
Supply Current per Amplifier vs Temperature



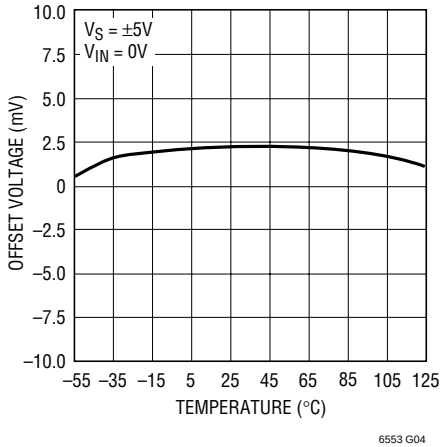
Supply Current per Amplifier vs Supply Voltage



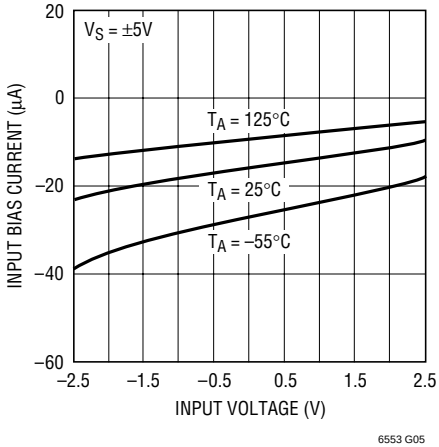
Supply Current per Amplifier vs $\overline{EN}$ Pin Voltage



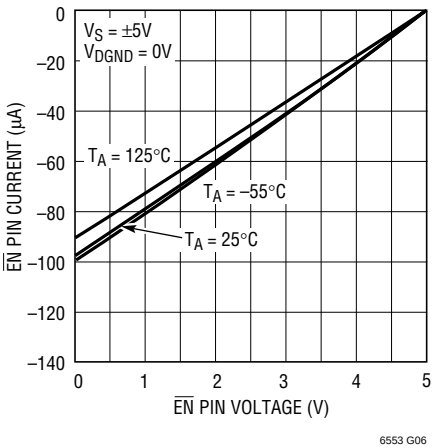
Input Referred Offset Voltage vs Temperature



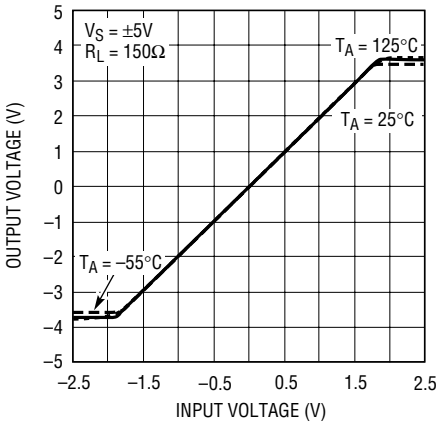
Input Bias Current vs Input Voltage



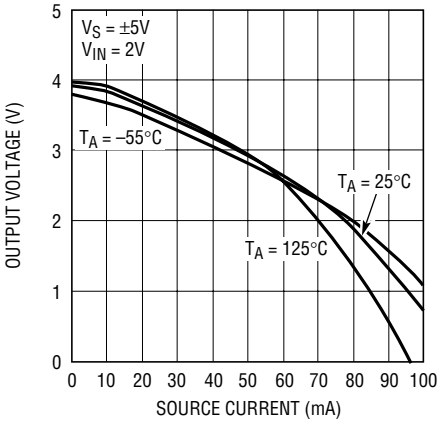
$\overline{EN}$ Pin Current vs $\overline{EN}$ Pin Voltage



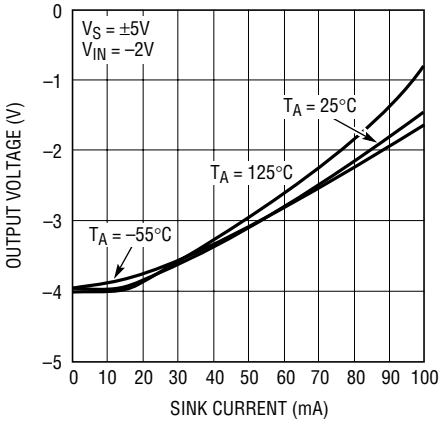
Output Voltage vs Input Voltage



Output Voltage Swing vs I_{LOAD} (Output High)

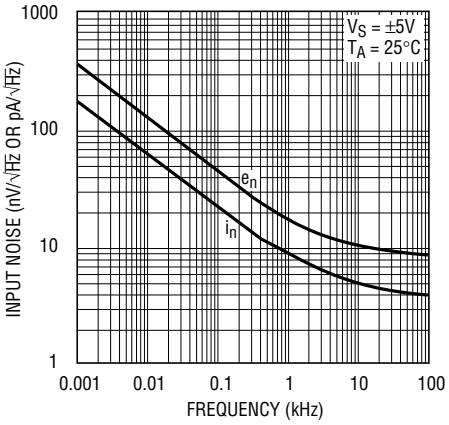


Output Voltage Swing vs I_{LOAD} (Output Low)

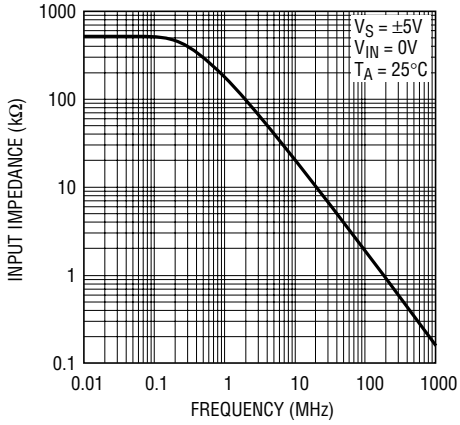


TYPICAL PERFORMANCE CHARACTERISTICS

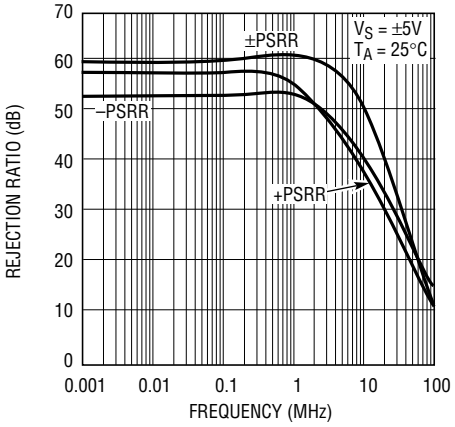
Input Noise Spectral Density



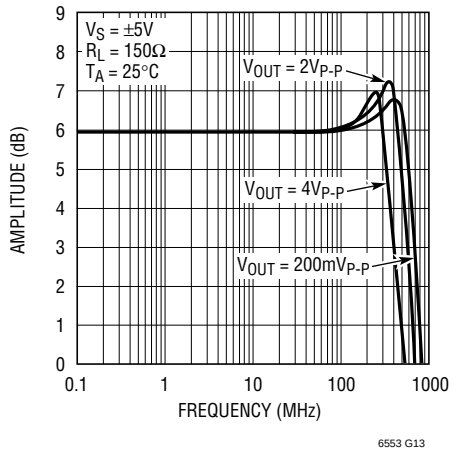
Input Impedance vs Frequency



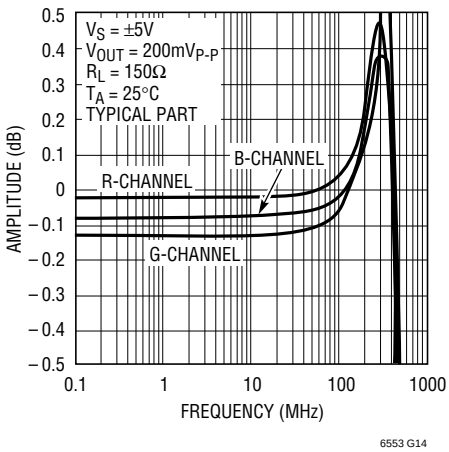
PSRR vs Frequency



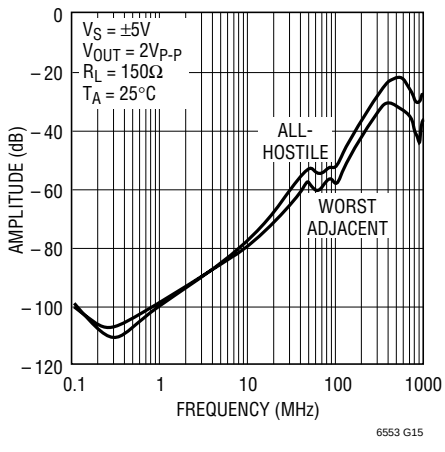
Frequency Response vs Output Amplitude



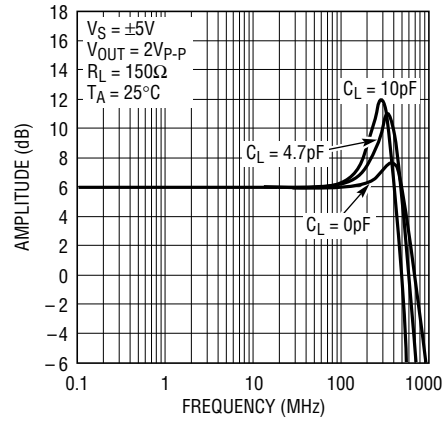
Gain Flatness vs Frequency



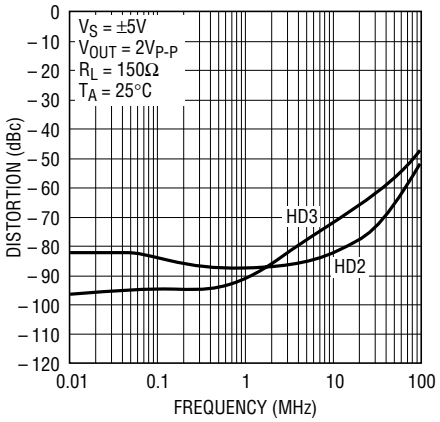
Crosstalk vs Frequency



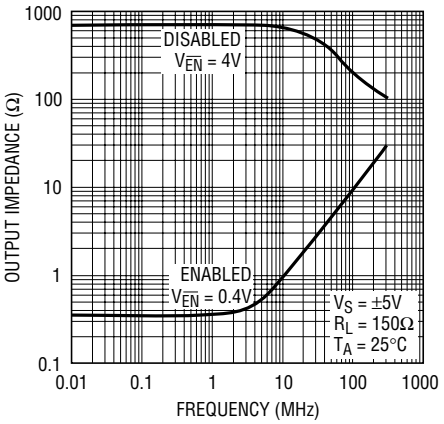
Frequency Response with Capacitive Loads



Harmonic Distortion vs Frequency

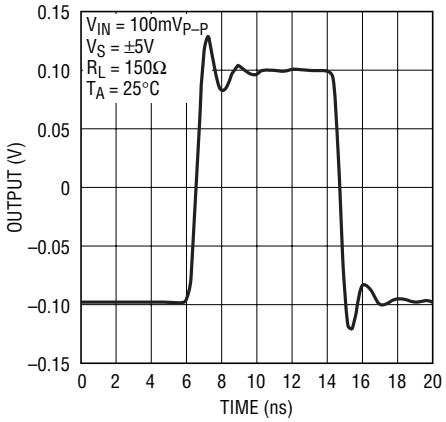


Output Impedance vs Frequency

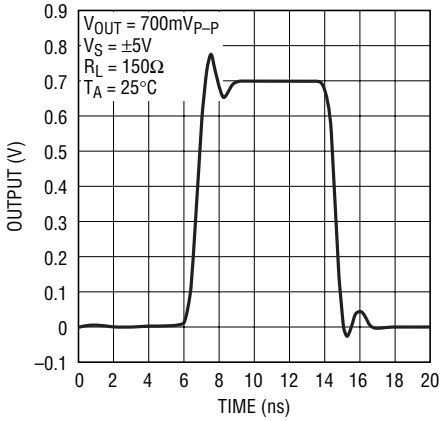


TYPICAL PERFORMANCE CHARACTERISTICS

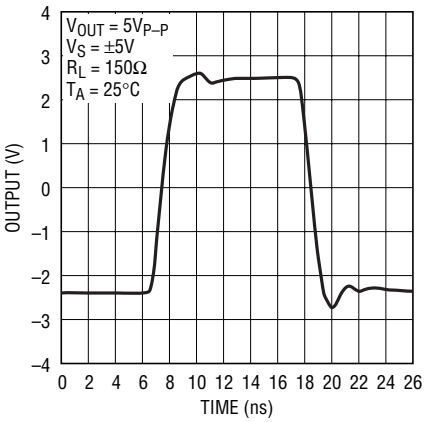
Small Signal Transient Response



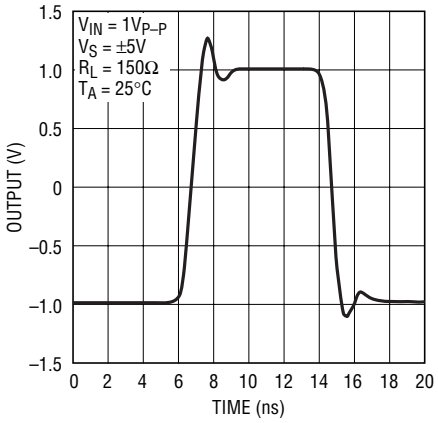
Video Amplitude Transient Response



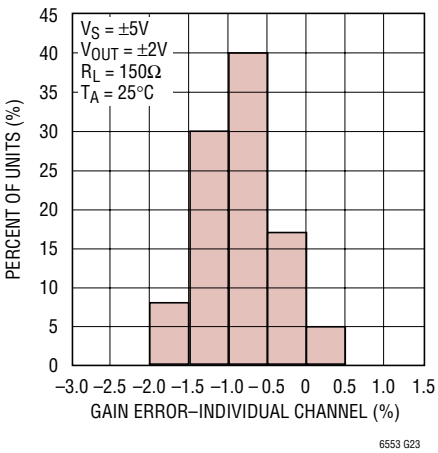
Large Signal Transient Response



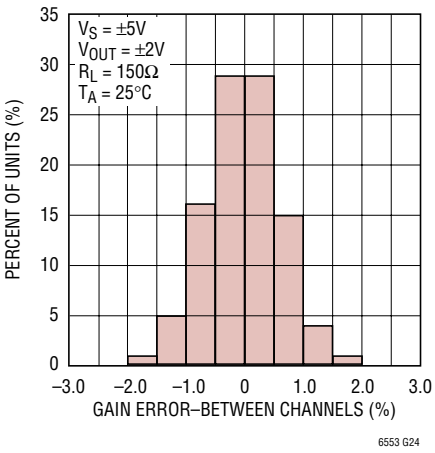
Large Signal Transient Response



Gain Error Distribution



Gain Error Matching Distribution



PIN FUNCTIONS

$\overline{EN}$ (Pin 1): Enable Control Pin. An internal pull-up resistor of 46k defines the pin's impedance and will turn the part off if the pin is unconnected. When the pin is pulled low, the part is enabled.

DGND (Pin 2): Digital Ground Reference for Enable Pin. This pin is normally connected to ground.

INR (Pin 3): Red Channel Input. This pin has a nominal impedance of 400kΩ and does not have any internal termination resistor.

AGND (Pin 4): Analog Ground for 370Ω Gain Resistor of Red Channel Amplifier.

ING (Pin 5): Green Channel Input. This pin has a nominal impedance of 400kΩ and does not have any internal termination resistor.

AGND (Pin 6): Analog Ground Shared for the 370Ω Gain Resistors of both Green and Blue Channel Amplifiers. Additional resistance at this pin will increase the crosstalk between the green and blue channels.

INB (Pin 7): Blue Channel Input. This pin has a nominal impedance of 400kΩ and does not have any internal termination resistor.

V^- (Pin 8): Negative Supply Voltage. V^- pins are not internally connected to each other, and must all be connected externally. Proper supply bypassing is necessary for best performance. See the Applications Information section.

V^- (Pin 9): Negative Supply Voltage for Blue Channel Output Stage. V^- pins are not internally connected to each other, and must all be connected externally. Proper supply bypassing is necessary for best performance. See the Applications Information section.

OUTB (Pin 10): Blue Channel Output. It is twice the blue channel input, and performs optimally with a 150Ω load (a double terminated 75Ω cable).

V^+ (Pin 11): Positive Supply Voltage for Output Stages of Amplifiers B and G. V^+ pins are not internally connected to each other, and must all be connected externally. Proper supply bypassing is necessary for best performance. See the Applications Information section.

OUTG (Pin 12): Green Channel Output. It is twice the green channel input, and performs optimally with a 150Ω load (a double terminated 75Ω cable).

V^- (Pin 13): Negative Supply Voltage for Output Stage of Amplifiers G and R. V^+ pins are not internally connected to each other, and must all be connected externally. Proper supply bypassing is necessary for best performance. See the Applications Information section.

OUTR (Pin 14): Red Channel Output. It is twice the red channel input, and performs optimally with a 150Ω load (a double terminated 75Ω cable).

V^+ (Pin 15): Positive Supply Voltage for Output Stage R. V^+ pins are not internally connected to each other, and must all be connected externally. Proper supply bypassing is necessary for best performance. See the Applications Information section.

V^+ (Pin 16): Positive Supply Voltage. V^+ pins are not internally connected to each other, and must all be connected externally. Proper supply bypassing is necessary for best performance. See the Applications Information section.

APPLICATIONS INFORMATION

Power Supplies

The LT6553 is optimized for ±5V supplies but can be operated on as little as ±2.25V or a single 4.5V supply and as much as ±6V or a single 12V supply. Internally, each supply is independent to improve channel isolation. **Do not leave any supply pins disconnected or the part may not function correctly!**

Enable/Shutdown

The LT6553 has a TTL compatible shutdown mode controlled by the $\overline{EN}$ pin and referenced to the DGND pin. If the amplifier will be enabled at all times, the $\overline{EN}$ pin can be connected directly to DGND. If the enable function is desired, either driving the pin above 2V or allowing the internal 46k pull-up resistor to pull the $\overline{EN}$ pin to the top rail will disable the amplifier. When disabled, the DC output impedance will rise to approximately 700Ω through the internal feedback and gain resistors. Supply current into the amplifier in the disabled state will be primarily through V^+ and approximately equal to $(V^+ – V_{\overline{EN}})/46k$.

It is important that the two following constraints on the DGND pin and the $\overline{EN}$ pin are always followed:

$$V^+ – V_{DGND} \geq 3V$$
$$V_{\overline{EN}} – V_{DGND} \leq 5.5V$$

Split supplies of ±3V to ±5.5V will satisfy these requirements with DGND connected to 0V.

In single supply applications above 5.5V, an additional resistor may be needed from the $\overline{EN}$ pin to DGND if the pin is ever allowed to float. For example, on a 12V single supply, a 33k resistor would protect the pin from floating too high while still allowing the internal pull-up resistor to disable the part.

On dual ±2.25V supplies, connecting the $\overline{EN}$ and DGND pins to $V^–$ is the easiest way of ensuring that $V^+ – V_{DGND}$ is more than 3V.

The DGND pin should not be pulled above the $\overline{EN}$ pin since doing so will turn on an ESD protection diode. If the $\overline{EN}$ pin voltage is forced a diode drop below the DGND pin, current should be limited to 10mA or less.

The enable/disable times of the LT6553 are fast when driven with a logic input. Turn on (from 50% $\overline{EN}$ input to 50% output) typically occurs in less than 50ns. Turn off is slower, but is nonetheless below 300ns.

Input Considerations

The LT6553 input voltage range is from $V^–$ + 1V to V^+ – 1V. Therefore, on split supplies the LT6553 input range is always larger than the output swing. On a single positive supply, however, the input range limits the output low swing to 2V (1V multiplied by the internal gain of 2).

The inputs can be driven beyond the point at which the output clips so long as input currents are limited to below ±10mA. Continuing to drive the input beyond the output limit can result in increased current drive and slightly increased swing, but will also increase supply current and may result in delays in transient response at larger levels of overdrive.

Layout and Grounding

It is imperative that care is taken in PCB layout in order to utilize the very high speed and very low crosstalk of the LT6553. Separate power and ground planes are highly recommended and trace lengths should be kept as short as possible. If input or output traces must be run over a distance of several centimeters, they should use a controlled impedance with matching series and shunt resistances (nominally 75Ω) to maintain signal fidelity.

Series termination resistors should be placed as close to the output pins as possible to minimize output capacitance. See the Typical Performance Characteristics section for a plot of frequency response with various output capacitors—only 10pF of parasitic output capacitance causes 6dB of peaking in the frequency response!

Low ESL/ESR bypass capacitors should be placed as close to the positive and negative supply pins as possible. One 4700pF ceramic capacitor is recommended for both V^+ and $V^–$. Additional 470pF ceramic capacitors with minimal trace length on each supply pin will further improve AC and transient response as well as channel isolation. For high current drive and large-signal transient applications, additional 1µF to 10µF tantalums should be added on each supply. The smallest value capacitors should be placed closest to the package.

APPLICATIONS INFORMATION

If the AGND pins are not connected directly to a low impedance ground plane, they must be carefully bypassed to maintain minimal impedance over frequency. Pin 6 is a shared connection of the gain resistors of both channel G and channel B, and any resistance external to this node can significantly decrease the isolation between those channels. Although crosstalk will be very dependent on the board layout, a recommended starting point for bypass capacitors would be 470pF as close as possible to each AGND pin with one 4700pF capacitor in parallel.

To maintain the LT6553's channel isolation, it is beneficial to shield parallel input and output traces using a ground plane or power supply traces. Vias between topside and backside metal may be required to maintain a low inductance ground near the part where numerous traces converge.

ESD Protection

The LT6553 has reverse-biased ESD protection diodes on all pins. If any pins are forced a diode drop above the positive supply or a diode drop below the negative supply, large currents may flow through these diodes. If the current is kept below 10mA, no damage to the devices will occur.

TYPICAL APPLICATION

RGB Buffer Demo Board

The DC714 Demo Board illustrates optimal routing, bypassing and termination using the LT6553 as an RGB video buffer. The schematic is shown in Figure 1. All inputs and outputs are routed to have a characteristic impedance of 75Ω and 75Ω input shunt and output series terminations are connected as close to the part as possible. For ideal operation, a 75Ω load termination should be connected at the output. The LT6553's gain of 2 will compensate for the resulting divider between the series and load termination resistors.

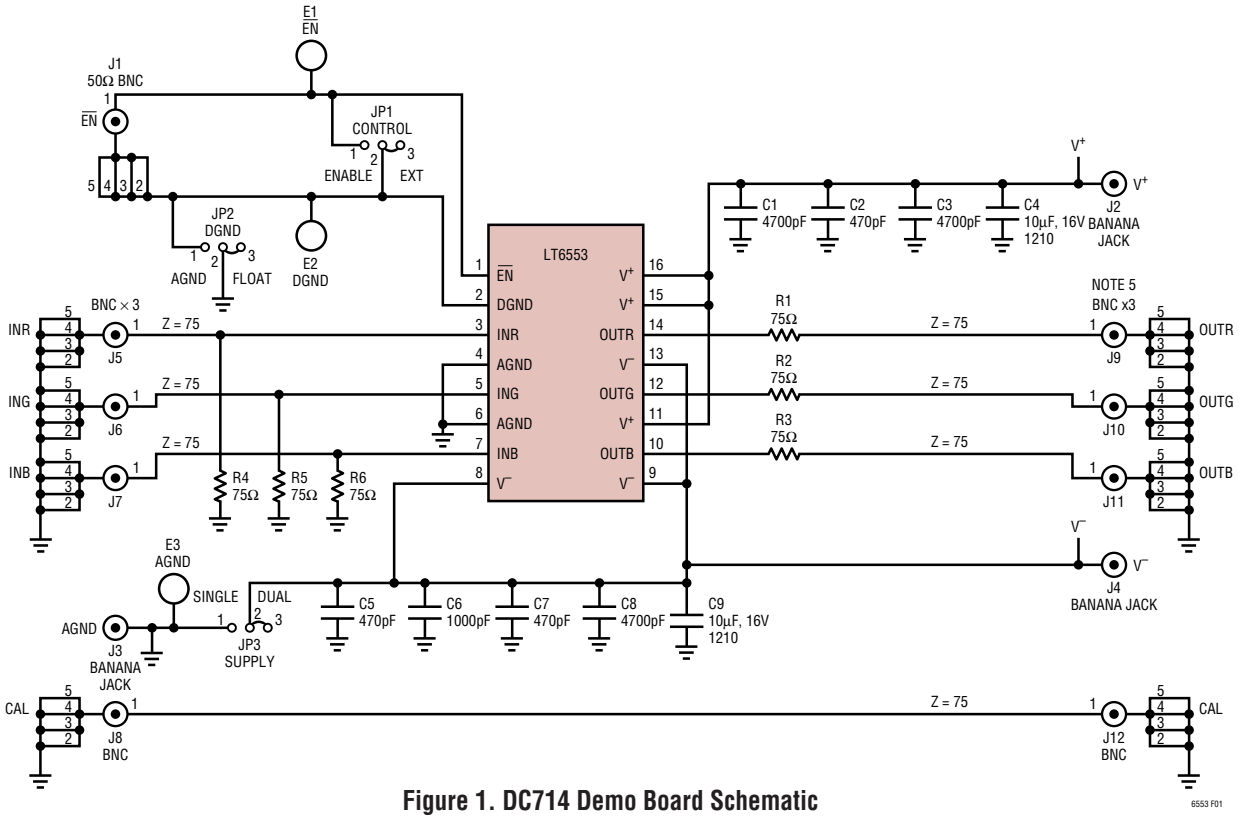


Figure 1. DC714 Demo Board Schematic

TYPICAL APPLICATIONS

A fourth signal trace is provided at the bottom of the DC714 demo board with dimensions identical to the combined input and output of the other channels. This trace can be used for calibrating the effects of electrical delay and impedance mismatching and is not necessary in an end-user application. Several jumpers and additional connectors are also included to allow for testing of the enable feature and single supply operation.

Single Supply RGB Buffer Demo Board

The DC743A Demo Board uses the LT6553 in a single supply application with AC coupled inputs and outputs. It is nearly identical to the DC714 RGB Buffer Demo Board but has the additional components required for AC coupling and setting a DC bias point at the input. A schematic of a single channel is shown in Figure 2. AC performance of the LT6553 in the single supply application as shown is nearly identical to performance with dual supplies.

The 6.8k and 2.2k bias resistors at the input set up a nominal DC voltage at the input that keeps a video signal within the input and output common mode range of the part. On a 9V single supply, the input would sit at 2.2V DC, and the output would sit at 4.4V.

Due to the 220µF coupling cap at the output, the only additional power dissipation due to the positive output voltage is through the feedback and gain resistors. Since those resistors are approximately 740Ω in series, the additional quiescent current is only 6mA per channel.

RGB Video Selector/Cable Driver

A video multiplexer can be implemented using the $\overline{EN}$ pins of parallel LT6553s as shown in Figure 3. In this application, all outputs are connected together and one LT6553 is switched on while the other is switched off. A fast inverter provides a complementary signal to ensure that only one set of R, G and B channels is buffered at any time. As shown, the outputs are connected before the 75Ω series termination resistors in order to reduce any DC attenuation that may result from the non-infinite output impedance of the disabled LT6553.

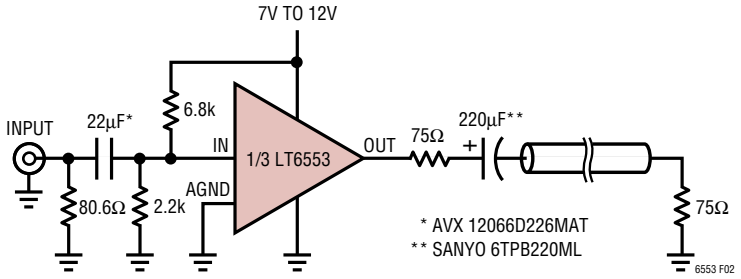
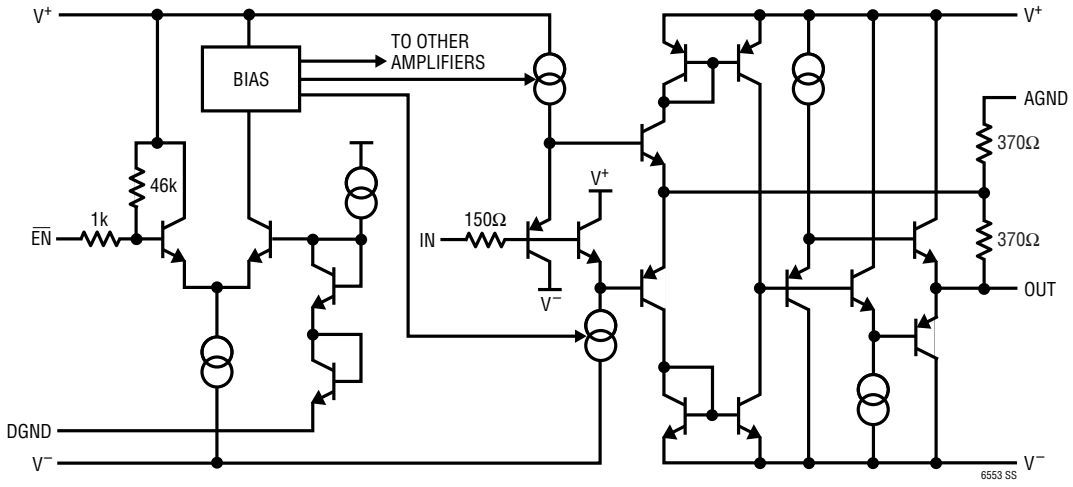


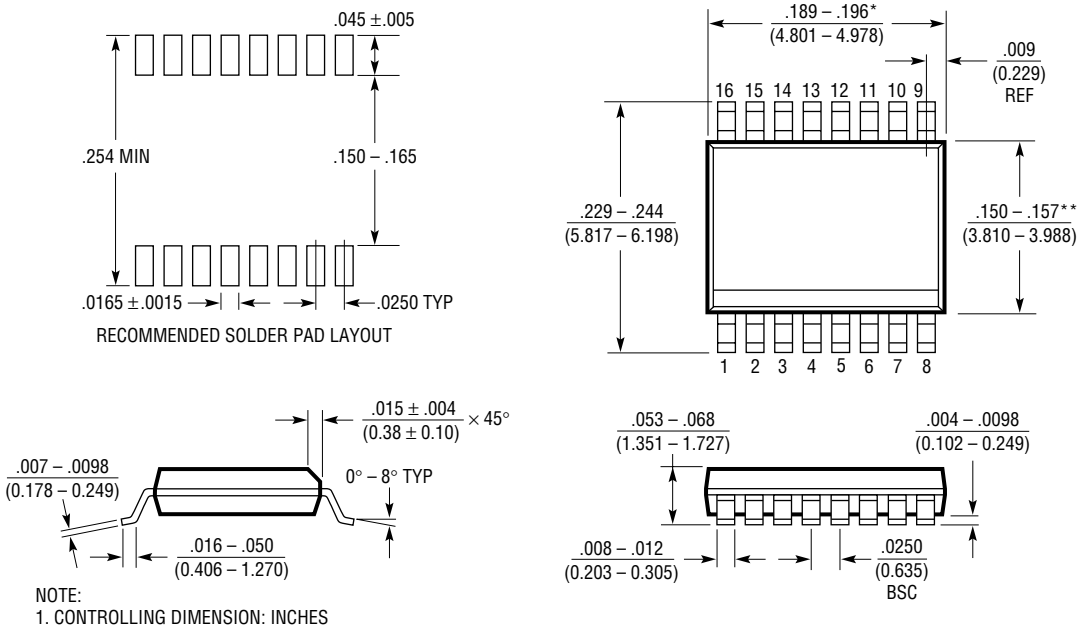
Figure 2. Single Supply Configuration, One Channel Shown

SIMPLIFIED SCHEMATIC



PACKAGE DESCRIPTION

GN Package
16-Lead Plastic SSOP (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1641)



NOTE:
1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
3. DRAWING NOT TO SCALE

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

GN16 (SSOP) 0502