Dual Very Low Noise, Differential Amplifier and 15MHz Lowpass Filter

FEATURES

- Dual Differential Amplifier with 15MHz Lowpass Filters
  - 4th Order Filters
  - Approximates Chebyshev Response
  - Guaranteed Phase and Gain Matching
  - Resistor-Programmable Differential Gain
- 76dB Signal-to-Noise (3V Supply, $2V_{P-P}$ Output)
- Low Distortion, $2V_{P-P}$, 800Ω Load, V_S = 3V
  - 1MHz: 86dBc 2nd, 90dBc 3rd
  - 10MHz: 63dBc 2nd, 69dBc 3rd
- Specified for Operation with 3V, 5V and ±5V Supplies
- Fully Differential Inputs and Outputs
- Adjustable Output Common Mode Voltage
- Small 4mm × 7mm × 0.75mm QFN Package

APPLICATIONS

- Dual Differential ADC Driver Plus Filter
- Single-Ended to Differential Converter
- Matched, Dual, Differential Filter Stage
- Common Mode Translation of Differential Signals
- High Speed ADC Antialiasing and DAC Smoothing in Wireless Infrastructure or Networking Applications
- High Speed Test and Measurement Equipment
- Medical Imaging

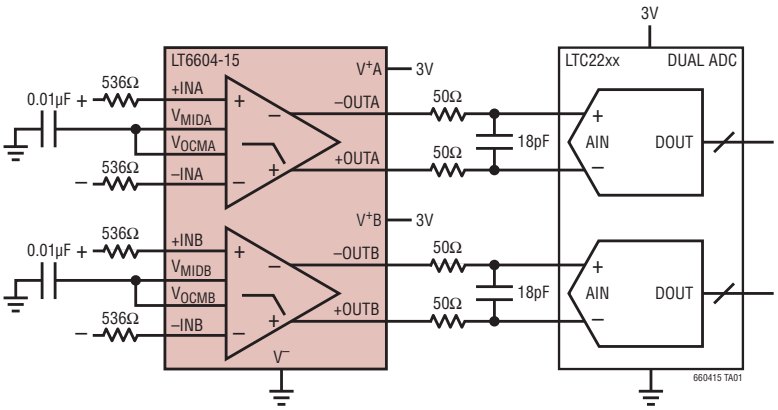
DESCRIPTION

The LT®6604-15 consists of two matched, fully differential amplifiers, each with a 4th order, 15MHz lowpass filter. The fixed frequency lowpass filter approximates a Chebyshev response. By integrating a filter and a differential amplifier, distortion and noise are made exceptionally low. At unity gain, the measured in band signal-to-noise ratio is an impressive 76dB. At higher gains, the input referred noise decreases, allowing the part to process smaller input differential signals without significantly degrading the signal-to-noise ratio.

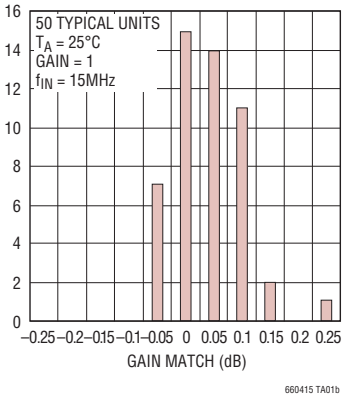
Gain and phase are highly matched between the two channels. Gain for each channel is independently programmed using two external resistors. The LT6604-15 enables level shifting by providing an adjustable output common mode voltage, making it ideal for directly interfacing to ADCs.

The LT6604-15 is fully specified for 3V operation. The differential design enables outstanding performance at a $2V_{P-P}$ signal level for a single 3V supply. See the back page of this datasheet for a complete list of related single and dual differential amplifiers with integrated 2.5MHz to 20MHz lowpass filters.

TYPICAL APPLICATION



Channel to Channel Gain Matching

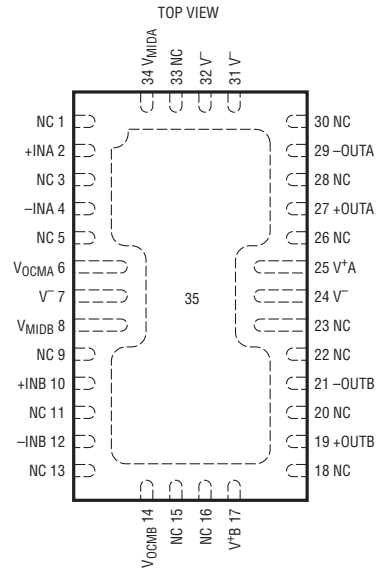


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Total Supply Voltage 11V
Operating Temperature Range (Note 6).... –40°C to 85°C
Specified Temperature Range (Note 7) .... –40°C to 85°C
Junction Temperature ..... 150°C
Storage Temperature Range..... –65°C to 150°C
Input Current
+IN, –IN, V_{OCM}, V_{MID} (Note 8) .....±10mA
Lead Temperature (Soldering, 10 sec) ..... 300°C

PIN CONFIGURATION



UFF PACKAGE
34-LEAD (4mm × 7mm) PLASTIC QFN

T_{JMAX} = 150°C, θ_{JA} = 34°C/W, θ_{JC} = 2.7°C/W
EXPOSED PAD (PIN 35) IS V–, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LT6604CUFF-15#PBF	LT6604CUFF-15#TRPBF	60415	34-Lead (4mm × 7mm) Plastic QFN	0°C to 70°C
LT6604IUFF-15#PBF	LT6604IUFF-15#TRPBF	60415	34-Lead (4mm × 7mm) Plastic QFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes specifications that apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. Unless otherwise specified V_S = 5V (V^+ = 5V, $V^–$ = 0V), R_{IN} = 536Ω, and R_{LOAD} = 1k.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Filter Gain Either Channel, V_S = 3V	V_{IN} = $2V_{P-P}$, f_{IN} = DC to 260kHz		–0.5	0.1	0.5	dB
	V_{IN} = $2V_{P-P}$, f_{IN} =1.5MHz (Gain Relative to 260kHz)	●	–0.1	0	0.1	dB
	V_{IN} = $2V_{P-P}$, f_{IN} = 7.5MHz (Gain Relative to 260kHz)	●	–0.3	0	0.4	dB
	V_{IN} = $2V_{P-P}$, f_{IN} = 12MHz (Gain Relative to 260kHz)	●	–0.3	0.2	1.0	dB
	V_{IN} = $2V_{P-P}$, f_{IN} = 15MHz (Gain Relative to 260kHz)	●	–0.7	0	1.0	dB
	V_{IN} = $2V_{P-P}$, f_{IN} = 45MHz (Gain Relative to 260kHz)	●		–29	–25	dB
	V_{IN} = $2V_{P-P}$, f_{IN} = 75MHz (Gain Relative to 260kHz)	●		–46		dB

ELECTRICAL CHARACTERISTICS

The ● denotes specifications that apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. Unless otherwise specified V_S = 5V (V^+ = 5V, V^- = 0V), R_{IN} = 536Ω, and R_{LOAD} = 1k.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Matching of Filter Gain, V_S = 3V	V_{IN} = 2V_{P-P}, f_{IN} = DC to 260kHz			0.05	0.5	dB
	V_{IN} = 2V_{P-P}, f_{IN} = 1.5MHz (Gain Relative to 260kHz)	●		0.01	0.1	dB
	V_{IN} = 2V_{P-P}, f_{IN} = 7.5MHz (Gain Relative to 260kHz)	●		0.02	0.3	dB
	V_{IN} = 2V_{P-P}, f_{IN} = 12MHz (Gain Relative to 260kHz)	●		0.03	0.4	dB
	V_{IN} = 2V_{P-P}, f_{IN} = 15MHz (Gain Relative to 260kHz)	●		0.06	0.6	dB
	V_{IN} = 2V_{P-P}, f_{IN} = 45MHz (Gain Relative to 260kHz)	●		0.13	1.5	dB
	V_{IN} = 2V_{P-P}, f_{IN} = 75MHz (Gain Relative to 260kHz)	●		0.15	2.8	dB
Matching of Filter Phase, V_S = 3V	V_{IN} = 2V_{P-P}, f_{IN} = 1.5MHz	●		0.6	1	deg
	V_{IN} = 2V_{P-P}, f_{IN} = 7.5MHz	●		0.8	3	deg
	V_{IN} = 2V_{P-P}, f_{IN} = 12MHz	●		0.9	4	deg
Filter Gain Either Channel, V_S = 5V	V_{IN} = 2V_{P-P}, f_{IN} = DC to 260kHz		–0.5	0	0.5	dB
	V_{IN} = 2V_{P-P}, f_{IN} =1.5MHz (Gain Relative to 260kHz)	●	–0.1	0	0.1	dB
	V_{IN} = 2V_{P-P}, f_{IN} = 7.5MHz (Gain Relative to 260kHz)	●	–0.4	0	0.3	dB
	V_{IN} = 2V_{P-P}, f_{IN} = 12MHz (Gain Relative to 260kHz)	●	–0.4	0.1	0.9	dB
	V_{IN} = 2V_{P-P}, f_{IN} = 15MHz (Gain Relative to 260kHz)	●	–0.8	0	0.9	dB
	V_{IN} = 2V_{P-P}, f_{IN} = 45MHz (Gain Relative to 260kHz)	●		–29	–25	dB
	V_{IN} = 2V_{P-P}, f_{IN} = 75MHz (Gain Relative to 260kHz)	●		–46		dB
Matching of Filter Gain, V_S = 5V	V_{IN} = 2V_{P-P}, f_{IN} = DC to 260kHz			0.05	0.5	dB
	V_{IN} = 2V_{P-P}, f_{IN} =1.5MHz (Gain Relative to 260kHz)	●		0.01	0.1	dB
	V_{IN} = 2V_{P-P}, f_{IN} = 7.5MHz (Gain Relative to 260kHz)	●		0.02	0.3	dB
	V_{IN} = 2V_{P-P}, f_{IN} = 12MHz (Gain Relative to 260kHz)	●		0.03	0.4	dB
	V_{IN} = 2V_{P-P}, f_{IN} = 15MHz (Gain Relative to 260kHz)	●		0.06	0.6	dB
	V_{IN} = 2V_{P-P}, f_{IN} = 45MHz (Gain Relative to 260kHz)	●		0.13	1.5	dB
	V_{IN} = 2V_{P-P}, f_{IN} = 75MHz (Gain Relative to 260kHz)	●		0.15	2.8	dB
Matching of Filter Phase, V_S = 5V	V_{IN} = 2V_{P-P}, f_{IN} = 1.5MHz	●		0.6	1	deg
	V_{IN} = 2V_{P-P}, f_{IN} = 7.5MHz	●		0.8	3	deg
	V_{IN} = 2V_{P-P}, f_{IN} = 12MHz	●		0.9	4	deg
Filter Gain Either Channel, V_S = ±5V	V_{IN} = 2V_{P-P}, f_{IN} = DC to 260kHz		–0.6	–0.1	0.4	dB
Filter Gain, R_{IN} = 133Ω	V_{IN} = 0.5V_{P-P}, f_{IN} = DC to 260kHz, V_S = 3V		11.5	12.0	12.5	dB
	V_S = 5V		11.5	12.0	12.5	dB
	V_S = ±5V		11.4	11.9	12.4	dB
Filter Gain Temperature Coefficient (Note 2)	f_{IN} = 250kHz, V_{IN} = 2V_{P-P}			780		ppm/°C
Noise	Noise BW = 10kHz to 15MHz, R_{IN} = 536Ω			109		μV_{RMS}
Distortion (Note 4)	1MHz, 2V_{P-P}, R_L = 800Ω, V_S = 3V, 2nd Harmonic			86		dBc
	3rd Harmonic			90		dBc
	10MHz, 2V_{P-P}, R_L = 800Ω, V_S = 3V, 2nd Harmonic			63		dBc
	3rd Harmonic			69		dBc
Channel Separation (Note 9)	1MHz, 2V_{P-P}, R_L = 800Ω			–117		dB
	10MHz, 2V_{P-P}, R_L = 800Ω			–102		dB
Differential Output Swing	Measured Between +OUT and –OUT, V_{OCM} shorted to V_{MID}					
	V_S = 5V	●	3.80	4.75		V_{P-P_DIFF}
	V_S = 3V	●	3.75	4.50		V_{P-P_DIFF}
Input Bias Current	Average of IN^+ and IN^-	●	–90	–35		µA
Input Referred Differential Offset	R_{IN} = 536Ω, V_S = 3V	●		5	25	mV
	V_S = 5V	●		10	30	mV
	V_S = ±5V	●		10	35	mV
	R_{IN} = 133Ω, V_S = 3V	●		5	15	mV
	V_S = 5V	●		5	17	mV
	V_S = ±5V	●		5	20	mV

ELECTRICAL CHARACTERISTICS

The ● denotes specifications that apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. Unless otherwise specified V_S = 5V (V^+ = 5V, V^- = 0V), R_{IN} = 536Ω, and R_{LOAD} = 1k.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Differential Offset Drift				10		µV/°C
Input Common Mode Voltage (Note 3)	Differential Input = 500mV$_{P-P}$, R_{IN} = 133Ω V_S = 3V	●	0		1.5	V
	V_S = 5V	●	0		3	V
	V_S = ±5V	●	–2.5		1	V
Output Common Mode Voltage (Note 5)	Differential Output = 2V$_{P-P}$, V_{MID} = Open, Common Mode Voltage at V_{OCM}					
	V_S = 3V	●	1		1.5	V
	V_S = 5V	●	1.5		3	V
	V_S = ±5V	●	–1		2	V
Output Common Mode Offset (with Respect to V_{OCM})	V_S = 3V	●	–35	5	40	mV
	V_S = 5V	●	–40	5	40	mV
	V_S = ±5V	●	–55	–10	35	mV
Common Mode Rejection Ratio				64		dB
Voltage at V_{MID}	V_S = 3V	●	2.45	2.50	2.56	V
	V_S = 5V			1.5		V
V_{MID} Input Resistance		●	4.3	5.7	7.7	kΩ
V_{OCM} Bias Current	V_{OCM} = V_{MID} = V_S/2 V_S = 3V	●	–10	–2		µA
	V_S = 5V	●	–10	–2		µA
Power Supply Current (per Channel)	V_S = 3V, V_S = 5V			35	39	mA
	V_S = 3V	●			44	mA
	V_S = 5V	●		34	45	mA
	V_S = ±5V	●		38	48	mA
Power Supply Voltage		●	3		11	V

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: This is the temperature coefficient of the internal feedback resistors assuming a temperature independent external resistor (R_{IN}).

Note 3: The input common mode voltage is the average of the voltages applied to the external resistors (R_{IN}). Specification guaranteed for $R_{IN} \geq 100\Omega$.

Note 4: Distortion is measured differentially using a differential stimulus. The input common mode voltage, the voltage at V_{OCM}, and the voltage at V_{MID} are equal to one half of the total power supply voltage.

Note 5: Output common mode voltage is the average of the +OUT and –OUT voltages. The output common mode voltage is equal to V_{OCM}.

Note 6: The LT6604C-15 is guaranteed functional over the operating temperature range –40°C to 85°C.

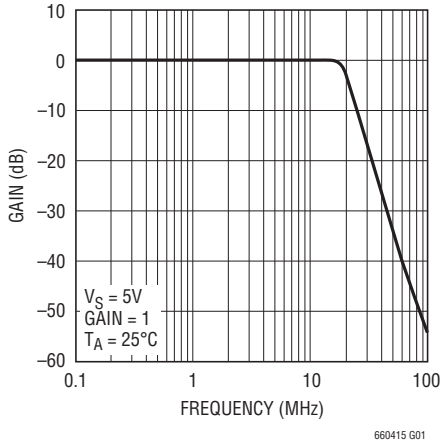
Note 7: The LT6604C-15 is guaranteed to meet 0°C to 70°C specifications and is designed, characterized and expected to meet the extended temperature limits, but is not tested at –40°C and 85°C. The LT6604I-15 is guaranteed to meet specified performance from –40°C to 85°C.

Note 8: Input pins (+IN, –IN, V_{OCM} and V_{MID}) are protected by steering diodes to either supply. If the inputs should exceed either supply voltage, the input current should be limited to less than 10mA. In addition, the inputs +IN, –IN are protected by a pair of back-to-back diodes. If the differential input voltage exceeds 1.4V, the input current should be limited to less than 10mA.

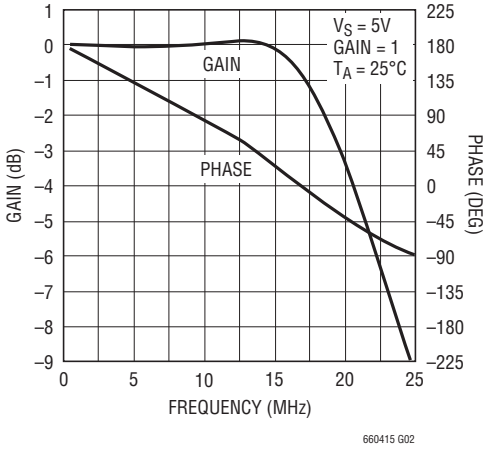
Note 9: Channel separation (the inverse of crosstalk) is measured by driving a signal into one input, while terminating the other input. Channel separation is the ratio of the resulting output signal at the driven channel to the output at the channel that is not driven.

TYPICAL PERFORMANCE CHARACTERISTICS

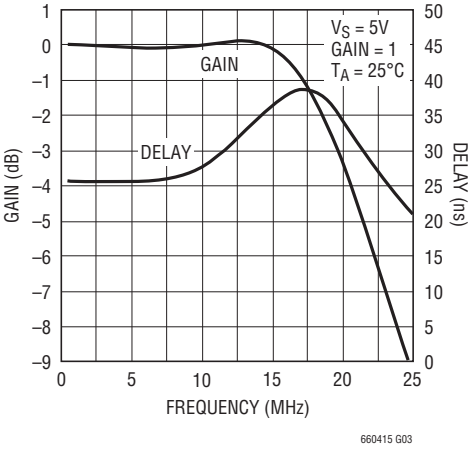
Amplitude Response



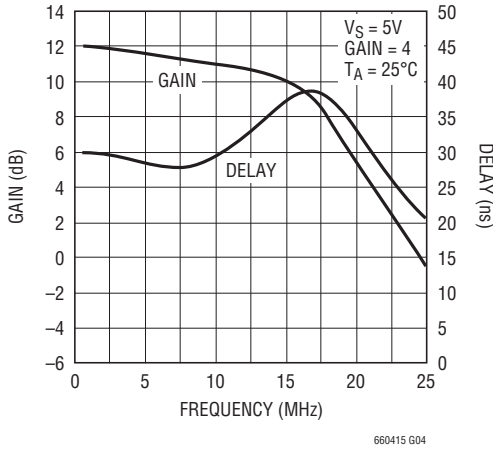
Passband Gain and Phase



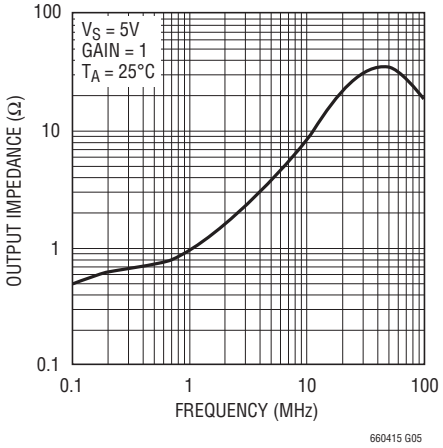
Passband Gain and Delay



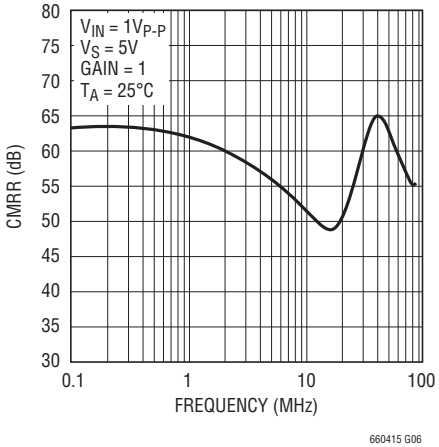
Passband Gain and Delay



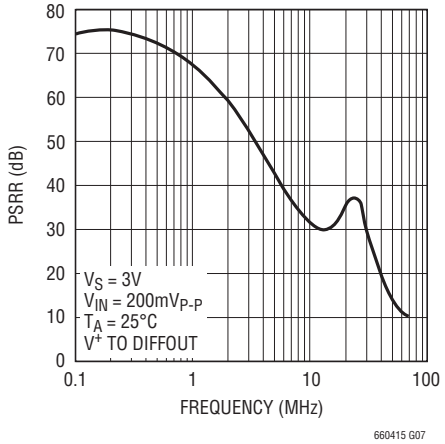
Output Impedance



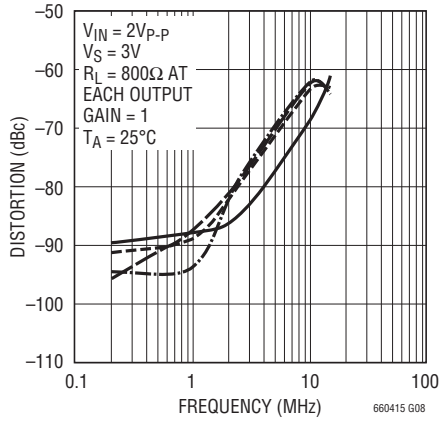
Common Mode Rejection Ratio



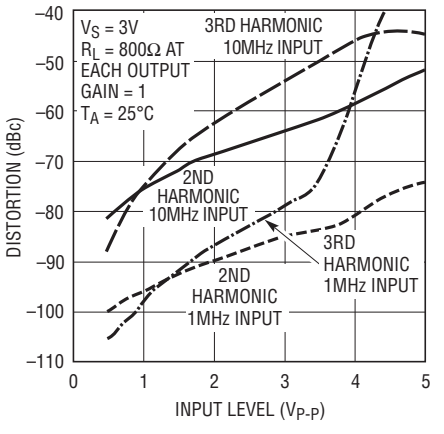
Power Supply Rejection Ratio



Distortion vs Frequency

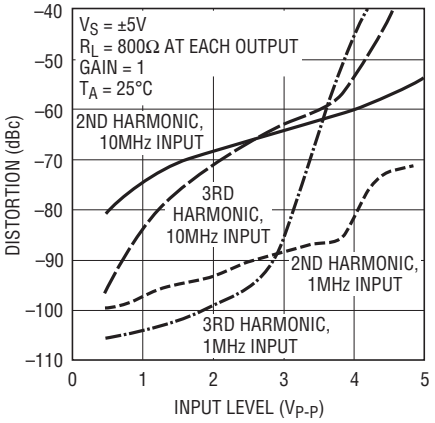


Distortion vs Signal Level

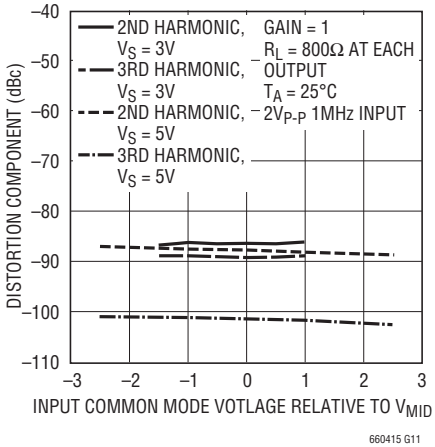


TYPICAL PERFORMANCE CHARACTERISTICS

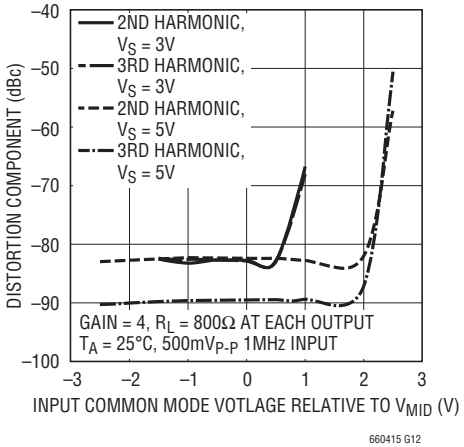
Distortion vs Signal Level



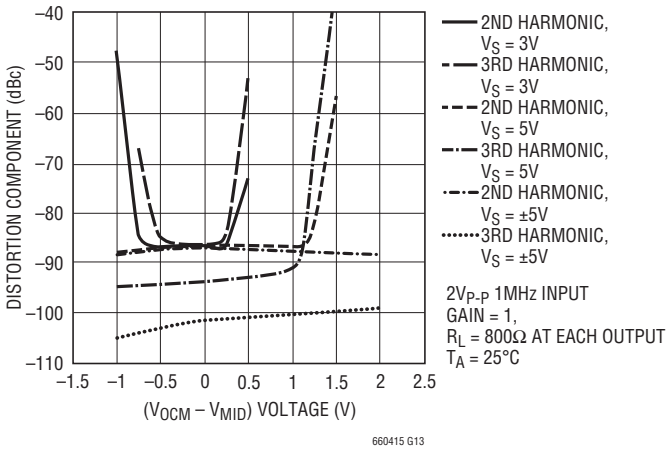
Distortion vs Input Common Mode Level



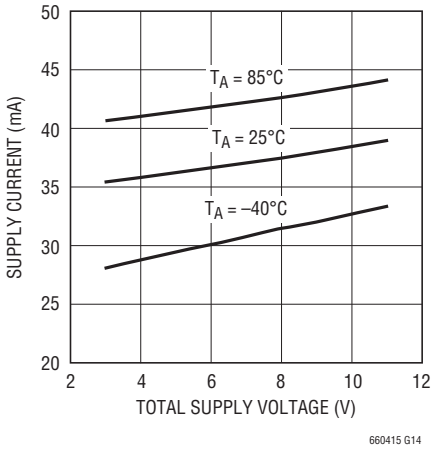
Distortion vs Input Common Mode Level



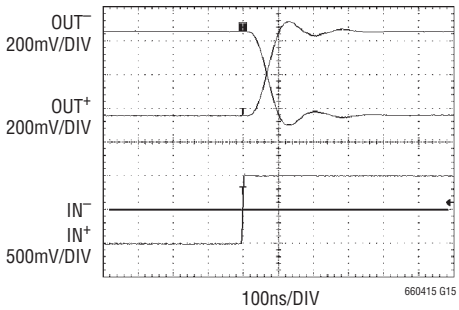
Distortion vs Output Common Mode Level



Single Channel Supply Current vs Total Supply Voltage

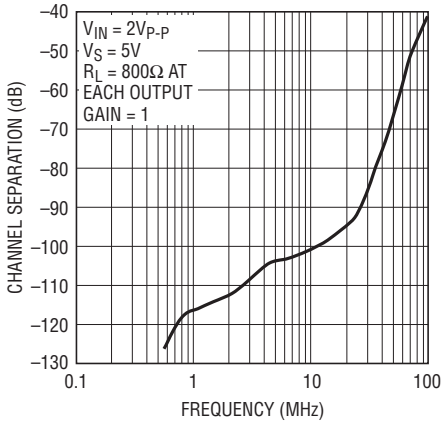


Transient Response,



DIFFERENTIAL GAIN = 1
SINGLE-ENDED INPUT
DIFFERENTAL OUTPUT

Channel Separation vs Frequency (Note 9)



PIN FUNCTIONS

+INA and –INA (Pins 2, 4): Channel A Input Pins. Signals can be applied to either or both input pins through identical external resistors, R_{IN}. The DC gain from differential inputs to the differential outputs is $536\Omega/R_{IN}$.

V_{OCMA} (Pin 6): DC Common Mode Reference Voltage for the 2nd Filter Stage in Channel A. Its value programs the common mode voltage of the differential output of the filter. Pin 6 is a high impedance input, which can be driven from an external voltage reference, or Pin 6 can be tied to Pin 34 on the PC board. Pin 6 should be bypassed with a 0.01µF ceramic capacitor unless it is connected to a ground plane.

V^- (Pins 7, 24, 31, 32, 35): Negative Power Supply Pin (can be ground).

V_{MIDB} (Pin 8): The V_{MIDB} pin is internally biased at mid-supply, see Block Diagram. For single supply operation the V_{MIDB} pin should be bypassed with a quality 0.01µF ceramic capacitor to ground. For dual supply operation, Pin 8 can be bypassed or connected to a high quality DC ground. A ground plane should be used. A poor ground will increase noise and distortion. Pin 8 sets the output common mode voltage of the 1st Filter Stage in channel B. It has a 5.5kΩ impedance, and it can be overridden with an external low impedance voltage source.

+INB and –INB (Pins 10, 12): Channel B Input Pins. Signals can be applied to either or both input pins through identical external resistors, R_{IN}. The DC gain from differential inputs to the differential outputs is $536\Omega/R_{IN}$.

V_{OCMB} (Pin 14): Is the DC Common Mode Reference Voltage for the 2nd Filter Stage in Channel B. Its value programs the common mode voltage of the differential output of the filter. Pin 14 is a high impedance input, which can be driven from an external voltage reference, or Pin 14 can be tied to Pin 8 on the PC board. Pin 14 should be bypassed with a 0.01µF ceramic capacitor unless it is connected to a ground plane.

V^+A and V^+B (Pins 25, 17): Positive Power Supply Pins for Channels A and B. For a single 3.3V or 5V supply (Pins 7, 24, 31, 32 and 35 grounded) a quality 0.1µF ceramic bypass capacitor is required from the positive supply pin (Pins 25, 17) to the negative supply pin (Pins 7, 24, 31, 32 and 35). The bypass should be as close as possible to the IC. For dual supply applications, bypass the negative supply pins to ground and Pins 25 and 17 to ground with a quality 0.1µF ceramic capacitor.

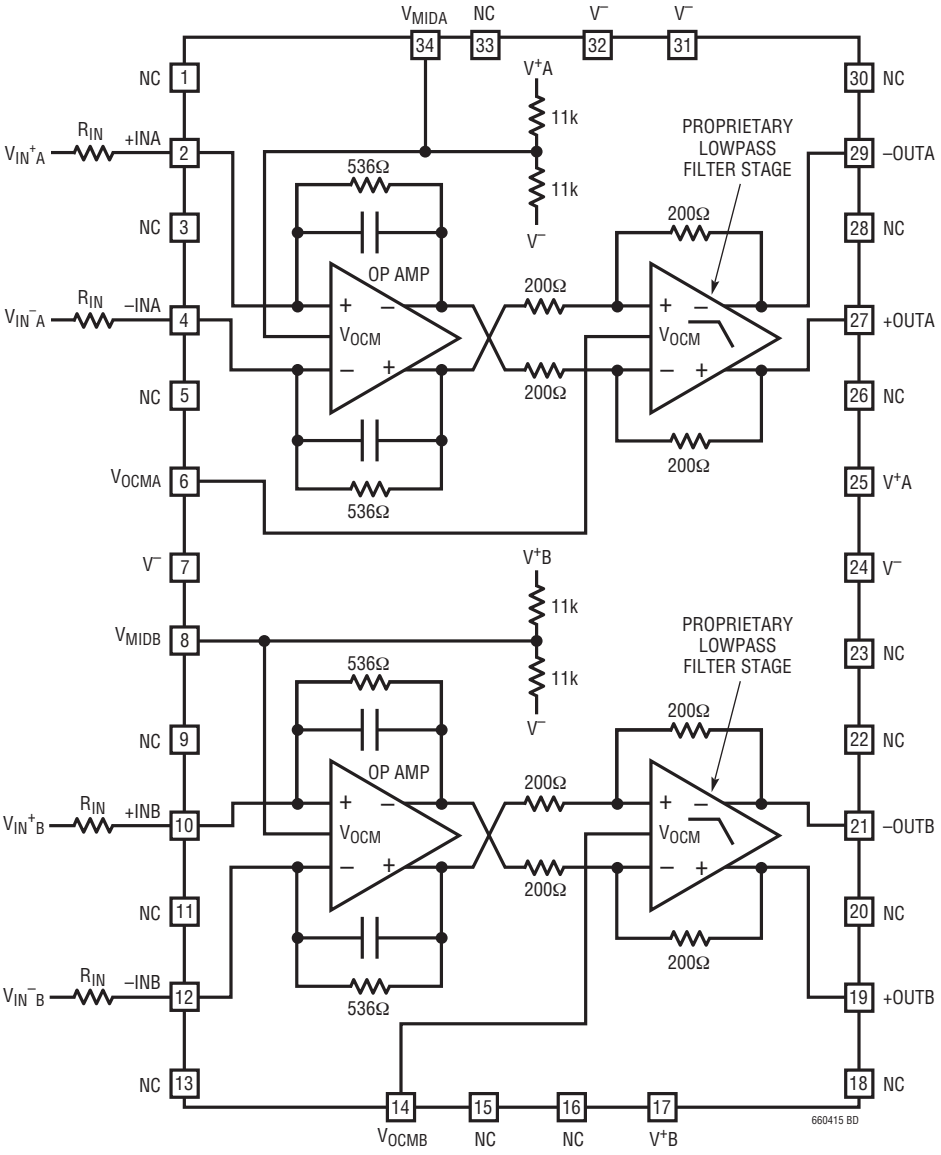
+OUTB and –OUTB (Pins 19, 21): Output Pins. Pins 19 and 21 are the filter differential outputs for channel B. With a typical short-circuit current limit greater than ±40mA each pin can drive a 100Ω and/or 50pF load to AC ground.

+OUTA and –OUTA (Pins 27, 29): Output Pins. Pins 27 and 29 are the filter differential outputs for channel A. With a typical short-circuit current limit greater than ±40mA each pin can drive a 100Ω and/or 50pF load to AC ground.

V_{MIDA} (Pin 34): The V_{MIDA} pin is internally biased at mid-supply, see Block Diagram. For single supply operation the V_{MIDA} pin should be bypassed with a quality 0.01µF ceramic capacitor to ground. For dual supply operation, Pin 34 can be bypassed or connected to a high quality DC ground. A ground plane should be used. A poor ground will increase noise and distortion. Pin 34 sets the output common mode voltage of the 1st stage filter stage in channel A. It has a 5.5kΩ impedance, and it can be overridden with an external low impedance voltage source.

Exposed Pad (Pin 35): V^-. The Exposed Pad must be soldered to the PCB.

BLOCK DIAGRAM



APPLICATIONS INFORMATION

Interfacing to the LT6604-15

Note: The LT6604-15 contains two identical filters. The following applications information only refers to one filter. The two filters are independent except that they share the same negative supply voltage V^-. The two filters can be used simultaneously by replicating the example circuits. The referenced pin numbers correspond to the A channel filter

The LT6604-15 channel requires two equal external resistors, R_{IN}, to set the differential gain to $536\Omega/R_{IN}$. The inputs to the filter are the voltages V_{IN}^+ and V_{IN}^- presented to these external components, Figure 1. The difference between V_{IN}^+ and V_{IN}^- is the differential input voltage. The average of V_{IN}^+ and V_{IN}^- is the common mode input voltage. Similarly, the voltages V_{OUT}^+ and V_{OUT}^- appearing at Pins 27 and 29 of the LT6604-15 are the filter outputs. The difference between V_{OUT}^+ and V_{OUT}^- is the differential output voltage. The average of V_{OUT}^+ and V_{OUT}^- is the common mode output voltage. Figure 1 illustrates the LT6604-15 operating with a single 3.3V supply and unity passband gain; the input signal is DC coupled. The common mode input voltage is 0.5V, and the differential input voltage is $2V_{P-P}$. The common mode output voltage is 1.65V, and the differential output voltage is $2V_{P-P}$ for frequencies below 15MHz. The common mode output voltage is determined by the voltage at V_{OCM}. Since V_{OCM} is shorted to V_{MID}, the output common mode is the mid-supply voltage. In addition, the common mode input voltage can be equal to the mid-supply voltage of V_{MID}.

Figure 2 shows how to AC couple signals into the LT6604-15. In this instance, the input is a single-ended signal. AC coupling allows the processing of single-ended or differential signals with arbitrary common mode levels. The 0.1µF coupling capacitor and the 536Ω gain setting resistor form a high pass filter, attenuating signals below 3kHz. Larger values of coupling capacitors will proportionally reduce this highpass 3dB frequency.

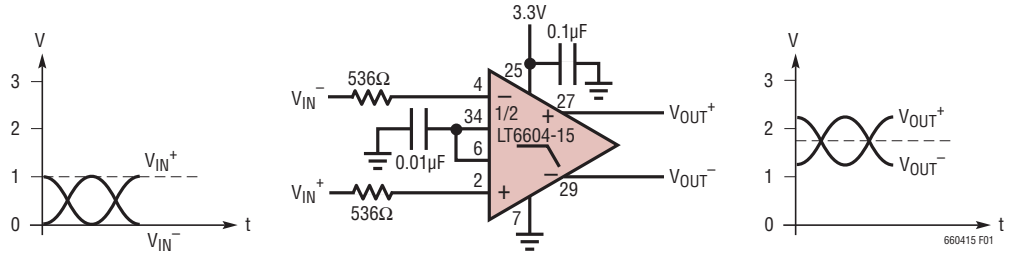


Figure 1

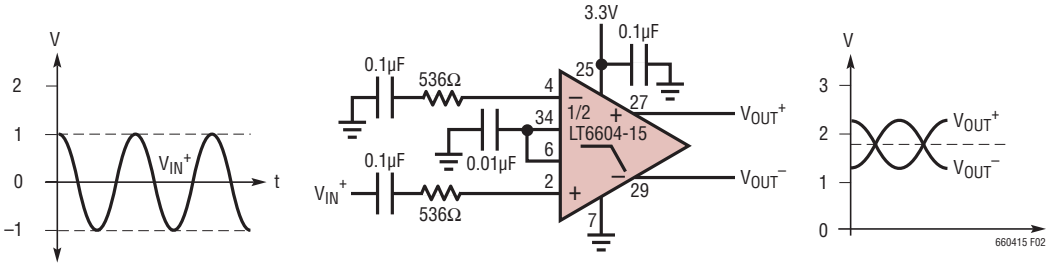


Figure 2

APPLICATIONS INFORMATION

In Figure 3 the LT6604-15 is providing 12dB of gain. The gain resistor has an optional 62pF in parallel to improve the passband flatness near 15MHz. The common mode output voltage is set to 2V.

Use Figure 4 to determine the interface between the LT6604-15 and a current output DAC. The gain, or "transimpedance," is defined as $A = V_{OUT}/I_{IN}$. To compute the transimpedance, use the following equation:

$$A = \frac{536 \bullet R1}{(R1+R2)} (\Omega)$$

By setting R1 + R2 = 536Ω, the gain equation reduces to A = R1 (Ω).

The voltage at the pins of the DAC is determined by R1, R2, the voltage on V_{MID} and the DAC output current. Consider Figure 4 with R1 = 49.9Ω and R2 = 487Ω. The voltage at V_{MID}, for V_S = 3.3V, is 1.65V. The voltage at the DAC pins is given by:

$$V_{DAC} = V_{MID} \bullet \frac{R1}{R1+R2+536} + I_{IN} \bullet \frac{R1 \bullet R2}{R1+R2}$$

$$= 77mV + I_{IN} \bullet 45.3\Omega$$

I_{IN} is I_{IN}^+ or I_{IN}^-. The transimpedance in this example is 49.8Ω.

Evaluating the LT6604-15

The low impedance levels and high frequency operation of the LT6604-15 require some attention to the matching networks between the LT6604-15 and other devices. The previous examples assume an ideal (0Ω) source impedance and a large (1k) load resistance. Among practical examples

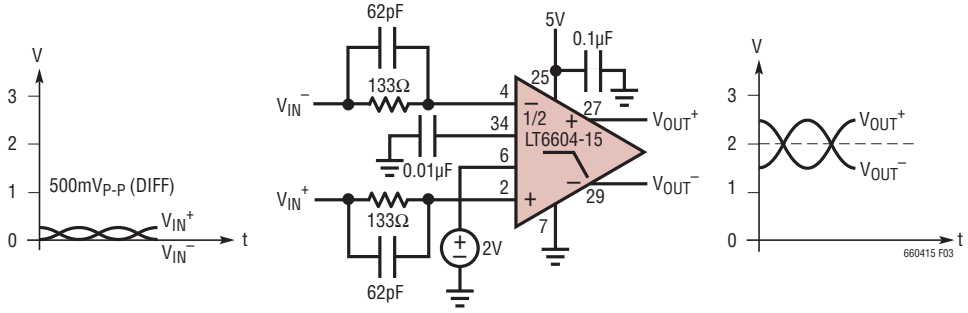


Figure 3

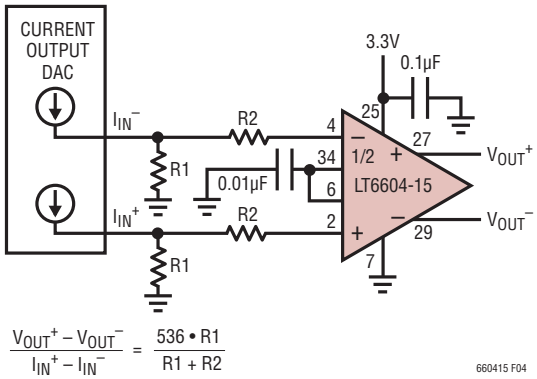


Figure 4

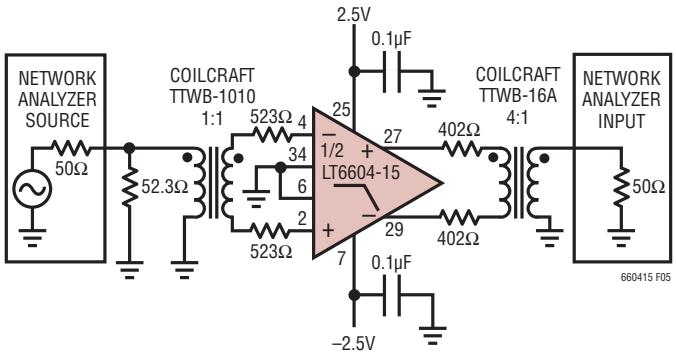


Figure 5

APPLICATIONS INFORMATION

where impedance must be considered is the evaluation of the LT6604-15 with a network analyzer.

Figure 5 is a laboratory setup that can be used to characterize the LT6604-15 using single-ended instruments with 50Ω source impedance and 50Ω input impedance. For a unity gain configuration the LT6604-15 requires an 536Ω source resistance yet the network analyzer output is calibrated for a 50Ω load resistance. The 1:1 transformer, 52.3Ω and 523Ω resistors satisfy the two constraints above. The transformer converts the single-ended source into a differential stimulus. Similarly, the output of the LT6604-15 will have lower distortion with larger load resistance yet the analyzer input is typically 50Ω. The 4:1 turns (16:1 impedance) transformer and the two 402Ω resistors of Figure 5, present the output of the LT6604-15 with a 1600Ω differential load, or the equivalent of 800Ω to ground at each output. The impedance seen by the network analyzer input is still 50Ω, reducing reflections in the cabling between the transformer and analyzer input.

Differential and Common Mode Voltage Ranges

The differential amplifiers inside the LT6604-15 contain circuitry to limit the maximum peak-to-peak differential voltage through the filter. This limiting function prevents excessive power dissipation in the internal circuitry and provides output short-circuit protection. The limiting function begins to take effect at output signal levels above $2V_{P-P}$ and it becomes noticeable above $3.5V_{P-P}$. This is illustrated in Figure 6; the LT6604-15 channel was configured with unity passband gain and the input of the filter was driven with a 1MHz signal. Because this voltage limiting takes place well before the output stage of the filter reaches the supply rails, the input/output behavior of the IC shown in Figure 6 is relatively independent of the power supply voltage.

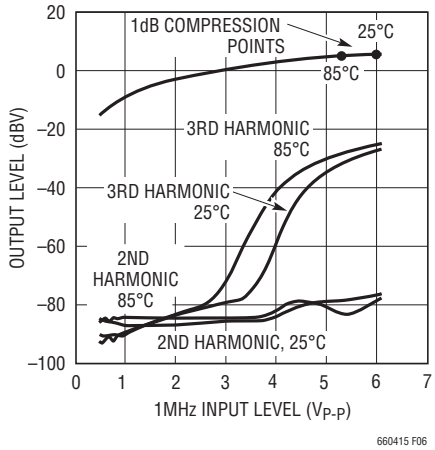


Figure 6. Output Level vs Input Level, Differential 1MHz Input, Gain = 1

The two amplifiers inside the LT6604-15 channel have independent control of their output common mode voltage (see the Block Diagram section). The following guidelines will optimize the performance of the filter.

V_{MID} can be allowed to float, but it must be bypassed to an AC ground with a 0.01µF capacitor or some instability may be observed. V_{MID} can be driven from a low impedance source, provided it remains at least 1.5V above V^- and at least 1.5V below V^+. An internal resistor divider sets the voltage of V_{MID}. While the internal 11k resistors are well matched, their absolute value can vary by ±20%. This should be taken into consideration when connecting an external resistor network to alter the voltage of V_{MID}.

V_{OCM} can be shorted to V_{MID} for simplicity. If a different common mode output voltage is required, connect V_{OCM} to a voltage source or resistor network. For 3V and 3.3V supplies the voltage at V_{OCM} must be less than or equal to the mid supply level. For example, voltage (V_{OCM}) ≤ 1.65V on a single 3.3V supply. For power supply voltages higher than 3.3V the voltage at V_{OCM} can be set above mid supply. The voltage on V_{OCM} should not be more than 1V below the voltage on V_{MID}. The voltage on V_{OCM} should not be more than 2V above the voltage on V_{MID}. V_{OCM} is a high impedance input.

The LT6604-15 was designed to process a variety of input signals including signals centered on the mid-supply voltage and signals that swing between ground and a positive voltage in a single supply system (Figure 1). The range of allowable input common mode voltage (the average of V_{IN}^+ and V_{IN}^- in Figure 1) is determined by the power supply level and gain setting (see Distortion vs Input Common Mode Level in the Typical Performance Characteristics).

APPLICATIONS INFORMATION

Common Mode DC Currents

In applications like Figure 1 and Figure 3 where the LT6604-15 not only provides lowpass filtering but also level shifts the common mode voltage of the input signal, DC currents will be generated through the DC path between input and output terminals. Minimize these currents to decrease power dissipation and distortion. Consider the application in Figure 3. V_{MID} sets the output common mode voltage of the 1st differential amplifier inside the LT6604-15 channel (see the Block Diagram section) at 2.5V. Since the input common mode voltage is near 0V, there will be approximately a total of 2.5V drop across the series combination of the internal 536Ω feedback resistor and the external 133Ω input resistor. The resulting 3.7mA common mode DC current in each input path, must be absorbed by the sources V_{IN}^+ and V_{IN}^-. V_{OCM} sets the common mode output voltage of the 2nd differential amplifier inside the LT6604-15 channel, and therefore sets the common mode output voltage of the filter. Since, in the example of Figure 3, V_{OCM} differs from V_{MID} by 0.5V, an additional 2.5mA (1.25mA per side) of DC current will flow in the resistors coupling the 1st differential amplifier output stage to the filter output. Thus, a total of 9.9mA per channel is used to translate the common mode voltages.

A simple modification to Figure 3 will reduce the DC common mode currents by 40%. If V_{MID} is shorted to V_{OCM} the common mode output voltage of both op amp stages will be 2V and the resulting DC current will be 6mA per channel. Of course, by AC coupling the inputs of Figure 3, the common mode DC current can be reduced to 2.5mA per channel.

Noise

The noise performance of the LT6604-15 channel can be evaluated with the circuit of Figure 6. Given the low noise output of the LT6604-15 and the 6dB attenuation of the transformer coupling network, it will be necessary to measure the noise floor of the spectrum analyzer and subtract the instrument noise from the filter noise measurement.

Example: With the IC removed and the 25Ω resistors grounded, Figure 6, measure the total integrated noise (e_S) of the spectrum analyzer from 10kHz to 15MHz. With the IC inserted, the signal source (V_{IN}) disconnected, and the input resistors grounded, measure the total integrated noise out of the filter (e_O). With the signal source connected, set the frequency to 1 MHz and adjust the amplitude until V_{IN} measures $100mV_{P-P}$. Measure the output amplitude, V_{OUT}, and compute the passband gain $A = V_{OUT}/V_{IN}$. Now compute the input referred integrated noise (e_{IN}) as:

$$e_{IN} = \frac{\sqrt{(e_O)^2 - (e_S)^2}}{A}$$

Table 1 lists the typical input referred integrated noise for various values of R_{IN}.

Table 1. Noise Performance

PASSBAND GAIN	R_{IN}	INPUT REFERRED INTEGRATED NOISE 10kHz TO 15MHz	INPUT REFERRED INTEGRATED NOISE 10kHz TO 30MHz
4	133Ω	$36\mu V_{RMS}$	$51\mu V_{RMS}$
2	267Ω	$62\mu V_{RMS}$	$92\mu V_{RMS}$
1	536Ω	$109\mu V_{RMS}$	$169\mu V_{RMS}$

APPLICATIONS INFORMATION

Figure 8 is plot of the noise spectral density as a function of frequency for an LT6604-15 with R_{IN} = 536Ω using the fixture of Figure 7 (the instrument noise has been subtracted from the results). The noise at each output is comprised of a differential component and a common mode component. Using a transformer or combiner to convert the differential outputs to single-ended signal rejects the common mode noise and gives a true measure of the S/N achievable in the system. Conversely, if each output is measured individually and the noise power added together, the resulting calculated noise level will be higher than the true differential noise.

Power Dissipation

The LT6604-15 amplifiers combine high speed with large signal currents in a small package. There is a need to ensure that the die's junction temperature does not exceed 150°C. The LT6604-15 has an Exposed Pad (pin 35) which is connected to the lower supply ($V^–$). Connecting the pad to a ground plane helps to dissipate the heat generated by the chip. Metal trace and plated through-holes can be used to spread the heat generated by the device to the backside of the PC board.

Junction temperature, T_J, is calculated from the ambient temperature, T_A, and power dissipation, P_D. The power dissipation is the product of supply voltage, V_S, and supply current, I_S. Therefore, the junction temperature is given by:

$$T_J = T_A + (P_D \bullet \theta_{JA}) = T_A + (V_S \bullet I_S \bullet \theta_{JA})$$

where the supply current, I_S, is a function of signal level, load impedance, temperature and common mode voltages. For a given supply voltage, the worst-case power dissipation occurs when the differential input signal is maximum, the common mode currents are maximum (see Applications Information regarding Common Mode DC Currents), the load impedance is small and the ambient temperature is maximum. To compute the junction temperature, measure the supply current under these worstcase conditions, use 34°C/W as the package thermal resistance, then apply the equation for TJ. For example, using the circuit in Figure 3 with DC differential input voltage of 250mV, a differential output voltage of 1V, no load resistance and an ambient temperature of 85°C, the supply current (current into V^+) measures 50mA The resulting junction temperature is: $T_J = T_A + (P_D \bullet \theta_{JA}) = 85 + (5 \bullet 2 \bullet 0.05 \bullet 34) = 102°C$. The thermal resistance can be affected by the amount of copper on the PCB that is connected to $V^–$. The thermal resistance of the circuit can increase if the exposed pad is not connected to a large ground plane with a number of vias.

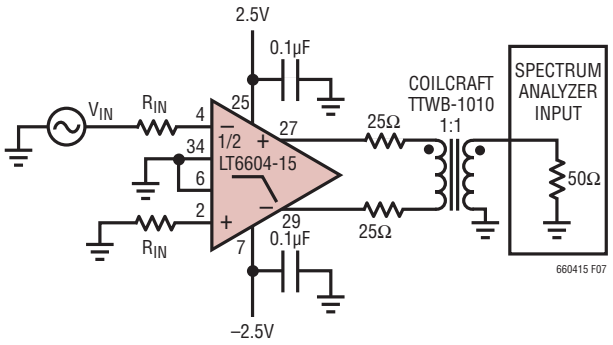


Figure 7

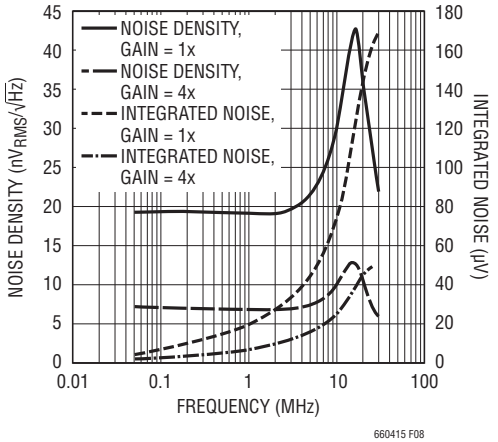
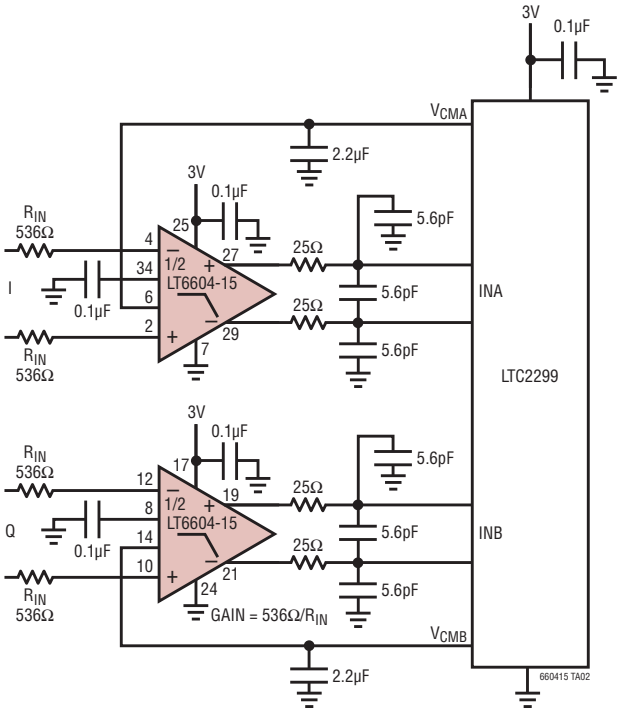


Figure 8. Input Referred Noise, Gain = 1

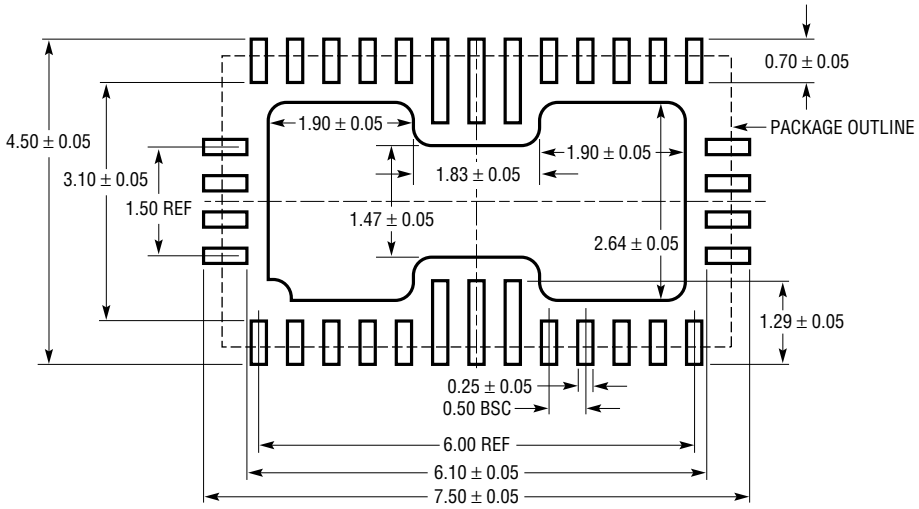
TYPICAL APPLICATION

Dual Matched I and Q Lowpass Filter and ADC (Typical Phase Matching ±1 Degree)

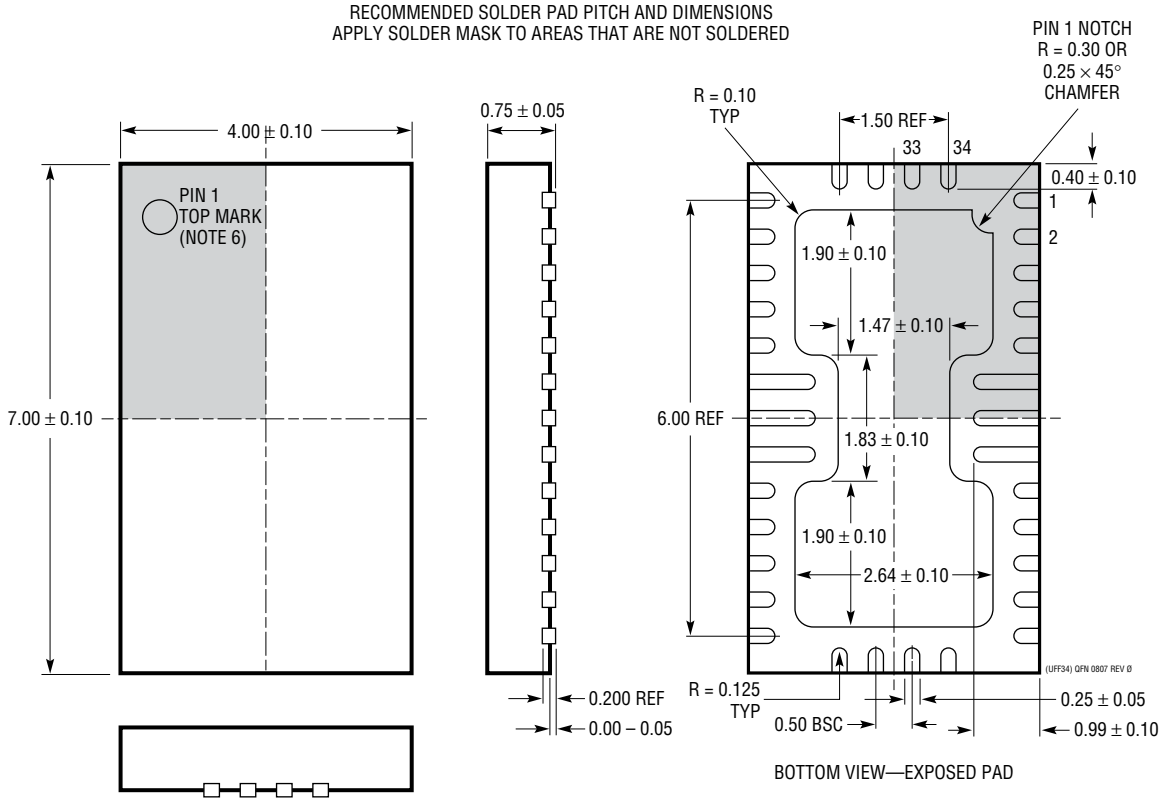


PACKAGE DESCRIPTION

UFF Package
34-Lead Plastic QFN (4mm × 7mm)
(Reference LTC DWG # 05-08-1758 Rev Ø)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE