Synchronous Rectifier Controller with Opto-Coupler Driver for Forward Converters

FEATURES

- **Wide Input Supply Range: 3.7V to 30V**
- **Preactive Mode:**
  - **No Pulse Transformer Required**
  - **DCM Operation at Light Load**
- **SYNC Mode:**
  - **FCM or DCM Operation at Light Load**
  - **Achieves Highest Efficiency**
- **1.5% Feedback Voltage Reference**
- **10mA Opto-Coupler Driver**
- **Output Power Good Indicator**
- Integrated Soft-Start Function

APPLICATIONS

- Offline and HV Car Battery Isolated Power Supplies
- 48V Isolated Power Supplies
- Industrial, Automotive and Military Systems

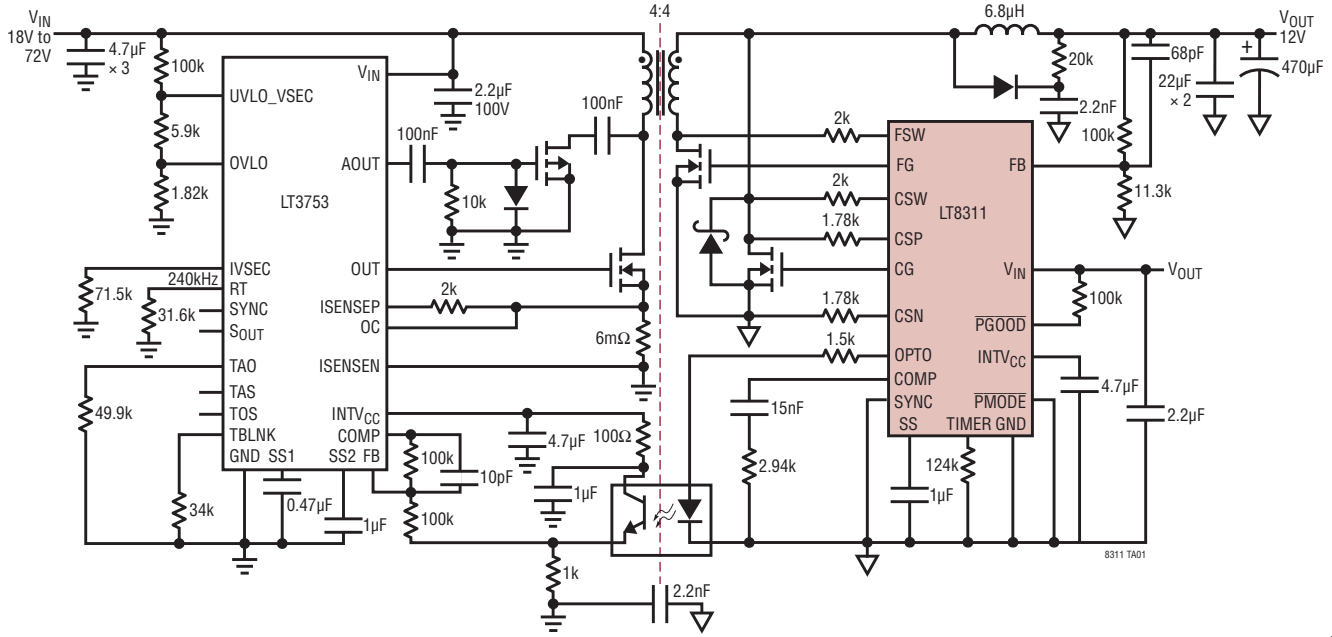
DESCRIPTION

The LT®8311 is used on the secondary side of a forward converter to provide synchronous MOSFET control and output voltage feedback through an opto-coupler. The LT8311's unique preactive mode allows control of the secondary-side MOSFETs without requiring a traditional pulse transformer for primary- to secondary-side communication. In preactive mode, the output inductor current operates in discontinuous conduction mode (DCM) at light load. If forced continuous mode (FCM) operation is desired at light load, the LT8311 can, alternatively, be used in SYNC mode, where a pulse transformer is required to send synchronous control signals from the primary-side IC to the LT8311.

The LT8311 offers a full featured opto-coupler controller, incorporating a 1.5% reference, a transconductance error amplifier and a 10mA opto-driver. Power good monitoring and output soft-start/overshoot control are also included. The LT8311 is available in a 16-lead FE package with pins removed for high voltage spacing requirements.

TYPICAL APPLICATION

18V to 72V, 12V/8A Active Clamp Isolated Forward Converter



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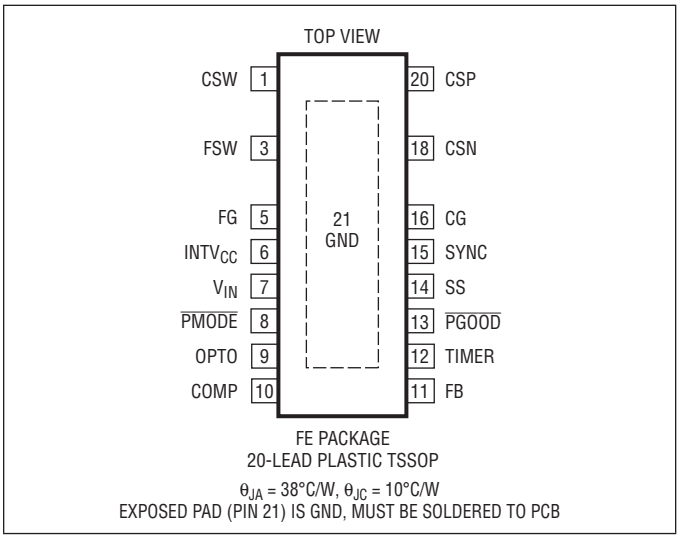
ABSOLUTE MAXIMUM RATINGS

(Note 1)

CSW, FSW, CSP ..... –0.3V to 150V
SYNC ..... –12V to 12V
V_{IN}, $\overline{PGOOD}$ ..... –0.3V to 30V
$INTV_{CC}$, $\overline{PMODE}$ ..... –0.3V to 18V
FB, SS, COMP ..... –0.3V to 2.5V
TIMER ..... –0.3V to 1.5V
CSN ..... –0.3V to 0.4V
OPTO, TIMER Short-Circuit
Current Duration ..... Infinite (Note 5)
Operating Junction Temperature Range
LT8311E (Notes 2, 3) ..... –40°C to 125°C
LT8311I (Notes 2, 3) ..... –40°C to 125°C
LT8311H (Notes 2, 3) ..... –40°C to 150°C
LT8311MP (Notes 2, 3) ..... –55°C to 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10sec) ..... 300°C

PIN CONFIGURATION



FE PACKAGE
20-LEAD PLASTIC TSSOP

θ_{JA} = 38°C/W, θ_{JC} = 10°C/W
EXPOSED PAD (PIN 21) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT8311EFE#PBF	LT8311EFE#TRPBF	LT8311FE	20-Lead Plastic TSSOP	–40°C to 125°C
LT8311IFE#PBF	LT8311IFE#TRPBF	LT8311FE	20-Lead Plastic TSSOP	–40°C to 125°C
LT8311HFE#PBF	LT8311HFE#TRPBF	LT8311FE	20-Lead Plastic TSSOP	–40°C to 150°C
LT8311MPFE#PBF	LT8311MPFE#TRPBF	LT8311FE	20-Lead Plastic TSSOP	–55°C to 150°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, V_{IN} = 12V, V_{INTVCC} = 8V, $\overline{PMODE}$ = 5V, C_{CG} = C_{FG} = 100pF, unless otherwise noted. (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supply						
V_{IN} Operating Range		●	3.7		30	V
V_{IN} UVLO	V_{IN} Rising Hysteresis	●	 50	3.6 100	3.7 150	V mV
Quiescent Current	Not Switching			4.5	5.5	mA
Error Amplifier						
Feedback Reference Voltage	V_{IN} = 12V	●	1.209	1.227	1.245	V
Feedback Voltage Line Regulation	3.7V ≤ V_{IN} ≤ 30V, % of FB Ref Voltage			0.015	0.1	%
Feedback Voltage Load Regulation	1.3V ≤ COMP ≤ 1.8V, % of FB Ref Voltage			0.05	0.1	%
Feedback Pin Bias Current	Current Out of FB pin			120	200	nA
Error Amplifier Transconductance	1.3V ≤ COMP ≤ 1.8V			370		µmhos
Error Amplifier Voltage Gain	1.3V ≤ COMP ≤ 1.8V			65		dB
Error Amplifier Output Swing High	FB = 1V		1.9	2.3	2.8	V
Error Amplifier Output Swing Low	FB = 1.5V		0.75	1	1.25	V
Power Good						
Power NOT Good (Outside This Window)	% Relative to FB Ref Voltage		±4	±10	±16	%
Power Good (Inside This Window)	% Relative to FB Ref Voltage			±7		%
Power Good Indicator Wait Time	Minimum Time That FB Must Stay within Power Good Window Before $\overline{PGOOD}$ Pin Goes Low			175		µs
Power Good Leakage	$\overline{PGOOD}$ = 30V				±1	µA
Power Good Output Low Voltage	Current into $\overline{PGOOD}$ Pin = 1mA	●		0.2	0.3	V
Soft-Start (SS)						
SS Wake-Up Slew Current	Current Exists Upon Part Wake Up, Shuts Off After SS Wake Up Offset Voltage Is Satisfied (Note 6)			1		mA
SS Wake-Up Offset Voltage	V_{FB} – V_{SS}, Upon Part Wake Up SS Is Slewed Up to an Offset Voltage Below FB by SS Wake-Up Slew Current			16		mV
SS Charge Current	SS = 0V, FB = 0.6V (Note 9)	●	9	10	11	µA
SS Pull-Down Amplifier Offset Voltage	V_{SS} – V_{FB}, Pull-Down Amplifier Prevents SS from Rising Beyond This Offset Voltage Above FB When the FB Pin Voltage Is Below 50% of the FB Reference Voltage			100		mV
SS Pull-Down Amplifier Maximum Sink Current	SS = 1.5V, FB = 0.6V (Note 7)			13		mA
SS High Clamp Voltage			1.8	2		V
Opto Driver						
COMP Buffer Input Offset Voltage	1.3V ≤ COMP (Note 5)			0.9		V
Opto-Driver Reference Voltage	(Note 5)			1		V
Opto-Driver DC Gain	(Note 5)			–7		V/V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, V_{IN} = 12V, V_{INTVCC} = 8V, $\overline{PMODE}$ = 5V, C_{CG} = C_{FG} = 100pF, unless otherwise noted. (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Inverting DC Gain From COMP Pin to OPTO Pin	($\Delta V_{OPTO}/\Delta V_{COMP}$), 1.290V ≤ COMP ≤ 1.310V			–5		V/V
	($\Delta V_{OPTO}/\Delta V_{COMP}$), 1.490V ≤ COMP ≤ 1.510V			–5.9		V/V
	($\Delta V_{OPTO}/\Delta V_{COMP}$), 1.890V ≤ COMP ≤ 1.910V			–6.2		V/V
Opto-Driver –3dB Bandwidth	No Load (Note 5)			400		kHz
Opto-Driver Output Swing Low	FB = 1V, COMP = SS = OPTO = Open	●		0.5	0.85	V
Opto-Driver Output Swing High	V_{IN} = 3.7V, FB = 1.5V, COMP = SS = Open, I_{OPTO} = 10mA	●	V_{IN} – 1.7	V_{IN} – 1.4		V
	V_{IN} = 30V, FB = 1.5V, COMP = SS = Open, I_{OPTO} = 10mA	●	5.2	6.5		V
Opto-Driver Output Short-Circuit Current	V_{IN} = 30V, FB = 1.5V, COMP = SS = Open, OPTO = 0V (Note 6)	●	10.5	15	18	mA
Opto-Driver Output Sink Current	FB = 1V, OPTO = 1.2V (Note 7)	●	200	300	420	µA
Internal Linear Regulator						
$INTV_{CC}$ Regulation Voltage	No Load	●	6.5	7	7.5	V
$INTV_{CC}$ Load Regulation	($\Delta V_{INTVCC}/\Delta I_{INTVCC}$), 0A ≤ I_{INTVCC} ≤ 20mA			1.8	3	mV/mA
$INTV_{CC}$ UVLO Rising		●		4.6	4.8	V
$INTV_{CC}$ UVLO Falling		●	4.1	4.3		V
$INTV_{CC}$ OVLO Rising		●		16.5	17.5	V
$INTV_{CC}$ OVLO Falling		●	14	15		V
$INTV_{CC}$ Current Limit	$INTV_{CC}$ > $I_{INTVCC\_UVLO\_RISING}$ (= 4.6V)	●	38	48	58	mA
	$INTV_{CC}$ < $I_{INTVCC\_UVLO\_FALLING}$ (= 4.3V)			20		mA
$INTV_{CC}$ Dropout Voltage	V_{IN} = 6V, I_{INTVCC} = 10mA, Not Switching			400		mV
CG and FG Gate Drivers						
Driver Output Rise Time	C_{CG} = C_{FG} = 3.3nF, $INTV_{CC}$ = 8V (Note 4)			25		ns
Driver Output Fall Time	C_{CG} = C_{FG} = 3.3nF, $INTV_{CC}$ = 8V (Note 4)			25		ns
Driver Output High Voltage		●	V_{INTVCC} – 0.2			V
Driver Output Low Voltage		●			0.7	V
$\overline{PMODE}$ Selection						
$\overline{PMODE}$ Trip Voltage	$\overline{PMODE}$ Ramp Up Hysteresis	●	1	1.2 30	1.4	V mV
$\overline{PMODE}$ Input Current	$\overline{PMODE}$ = 18V	●		60	90	µA
Preactive Mode (Tie $\overline{PMODE}$ to 0V)						
Preactive Mode Operating Frequency Range		●	100		300	kHz
CSW High Trip Voltage	CSW Ramp Up	●	1	1.2	1.4	V
CSW High Input Current	CSW = 150V (Note 7)	●		250	500	µA
CSW Low Trip Voltage	CSW Ramp Down	●	–250	–150	–50	mV
FSW Trip Voltage		●	1	1.2	1.4	V
FSW High Input Current	FSW = 150V (Note 7)	●		250	500	µA
CG Falling Edge to CSW Rising Edge Prediction Delay	CSW = 150kHz (Note 10), FSW = 0V, CSP = –500mV	●	5	100	300	ns
CG Falling Edge Delay to FG Rising Edge	CSW = 150kHz (Note 10), FSW = 0V, CSP = –500mV	●	10	50	80	ns

ELECTRICAL CHARACTERISTICS

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PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SYNC Mode (Tie $\overline{PMODE}$ to $INTV_{CC}$)						
SYNC High Trip Voltage	SYNC Ramp Up Hysteresis	●	0.9	1.2 –2.4	1.5	V V
SYNC Low Trip Voltage	SYNC Ramp Down Hysteresis	●	–1.5	–1.2 2.4	–0.9	V V
SYNC Minimum Pulse Width	SYNC = 0V to ±2V Pulse SYNC = 0V to ±6V Pulse (Note 5)	●		40 20	100	ns ns
SYNC Input Current	–3.5V < SYNC < 3.5V SYNC = ±10V (Note 6, 7)	 ●		 300	±1 400	µA µA
SYNC Propagation Delay To CG/FG Outputs	SYNC Rising Edge (0V to 2V) to CG Rising Edge (Note 8) SYNC Rising Edge (0V to 6V) to CG Rising Edge (Notes 5, 8) SYNC Falling Edge (0V to 2V) to FG Rising Edge (Note 8) SYNC Falling Edge (0V to 6V) to FG Rising Edge (Notes 5, 8), C_{CG} = C_{FG} = 3.3nF	● ● 		100 75 100 85	150 150 	ns ns ns ns
TIMER Timeout Frequency	R_{TIMER} = 41.2k R_{TIMER} = 71.5k R_{TIMER} = 221k	● ● ●	425 255 80	505 300 100	585 345 120	kHz kHz kHz
TIMER Short-Circuit Current	TIMER = 0V	●		40	60	µA
Current Comparator						
Current Comparator Trip Threshold	CSP Ramp Up, R_{CSP} = R_{CSN} = 0Ω	●	48	62	72	mV
	CSP Ramp Up, R_{CSP} = R_{CSN} = 1.62kΩ (Note 5)			0		mV
Current Comparator Blank Time in Preactive Mode	From Rising CG Edge Until Blanking Ends (Note 5)			250		ns
Current Comparator Blank Time in SYNC Mode	From Rising CG Edge Until Blanking Ends			400		ns
CSP Current at Low CSP Voltage	CSP = 0V (Note 6)	●	30	38	50	µA
CSP Current at High CSP Voltage	CSP = 150V (Note 7)	●		200	500	µA
CSN Current	CSN = 0V (Note 6)	●		0.1	1	µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LT8311 is tested under pulsed load conditions such that T_J ~ T_A. The LT8311E is guaranteed to meet specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature are assured by design, characterization and correlation with statistical process controls. The LT8311I is guaranteed over the –40°C to 125°C operating junction temperature range. The LT8311H is guaranteed over the –40°C to 150°C operating junction temperature range, and the LT8311MP is guaranteed over the –55°C to 150°C operating junction temperature range. High junction temperatures degrade operating lifetimes; operating lifetime is derated for junction temperatures greater than 125°C.

Note 3: The LT8311 includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed the maximum operating junction temperature when overtemperature is active. Continuous operating above the specified maximum operating junction temperature may impair device reliability.

Note 4: Rise and fall times of are measured between 10% and 90% points of a signal edge.

Note 5: Guaranteed by design and/or correlation to static test.

Note 6: Current flows out of pin.

Note 7: Current flows into pin.

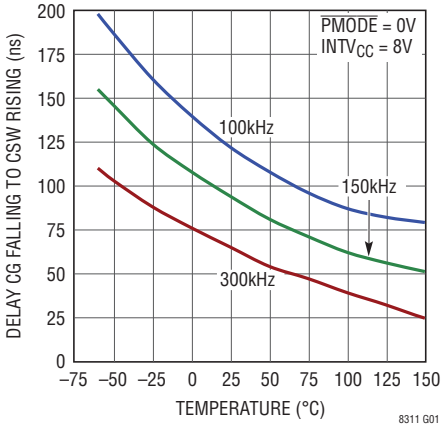
Note 8: Propagation delay is measured between 50% point of the two signal edges of interest.

Note 9: SS charge current refers to current flowing out of SS pin after certain conditions satisfied upon LT8311 wake-up (see the flowchart for Opto-Control Operation at Start-Up in Figure 9).

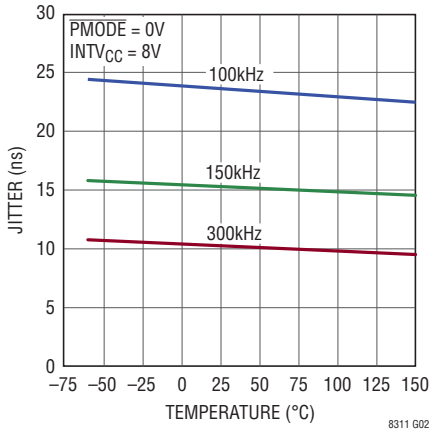
Note 10: CSW is a square waveform (duty cycle = 50%) with V_{HIGH} = 7V and V_{LOW} = –0.7V.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

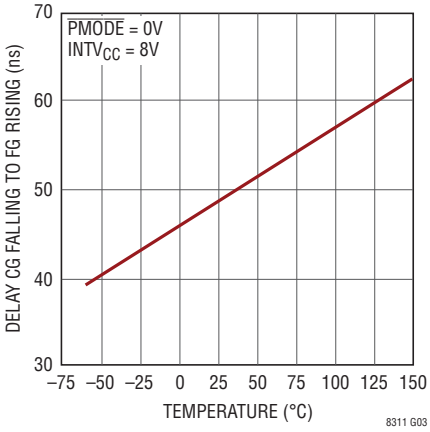
Delay from CG Turn-Off to CSW Rising Edge vs CSW Switching Frequency and Junction Temp



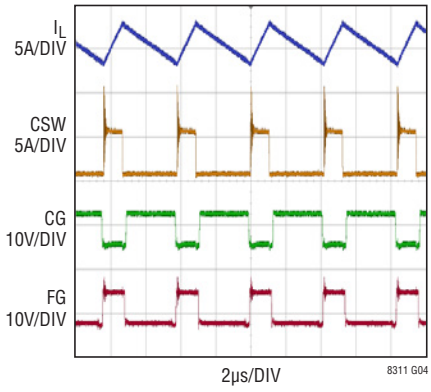
Jitter in CG Turn-Off Delay to CSW Rising Edge vs CSW Switching Frequency and Junction Temp



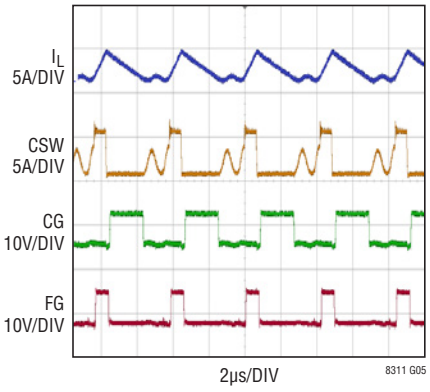
Delay from CG Turn-Off to FG Turn-On



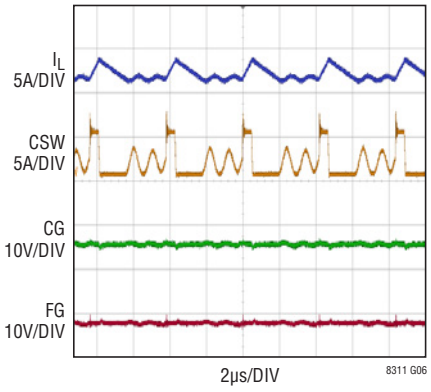
Preactive Scheme Waveforms (Active Clamp Reset, CCM)



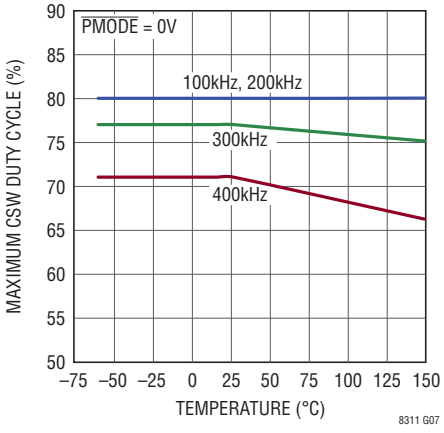
Preactive Scheme Waveforms (Active Clamp Reset, Light DCM)



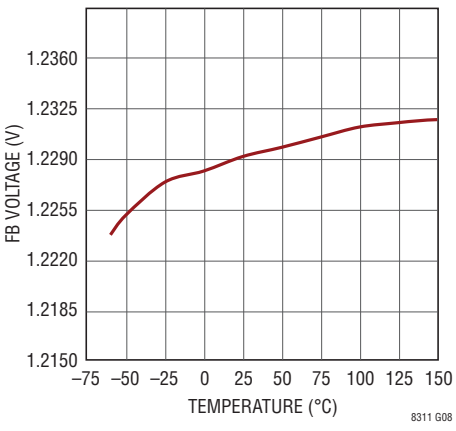
Preactive Scheme Waveforms (Active Clamp Reset, Deep DCM)



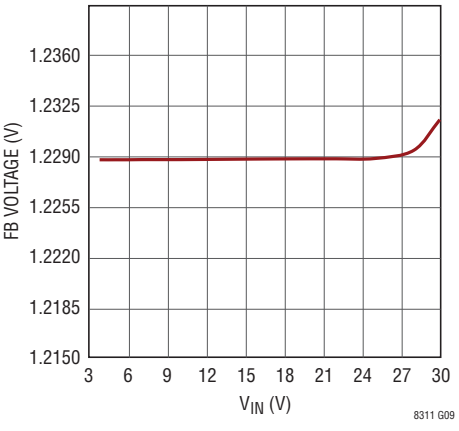
Maximum CSW Duty Cycle Derating Curve vs CSW Switching Frequency and Junction Temperature



Feedback Reference Voltage

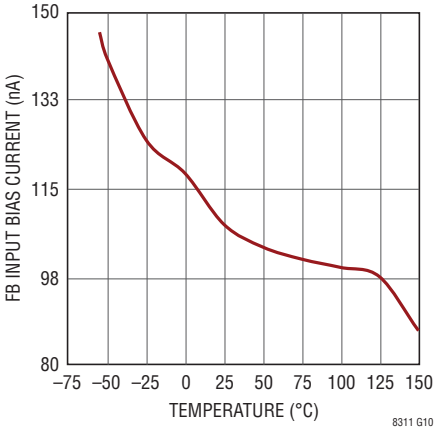


Feedback Reference Voltage vs V_{IN}

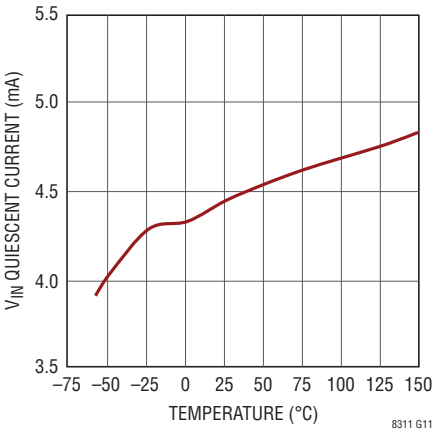


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

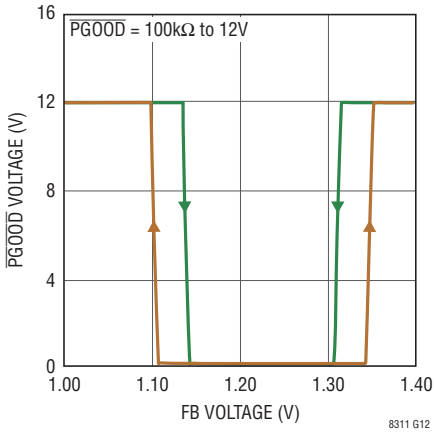
Feedback Input Bias Current



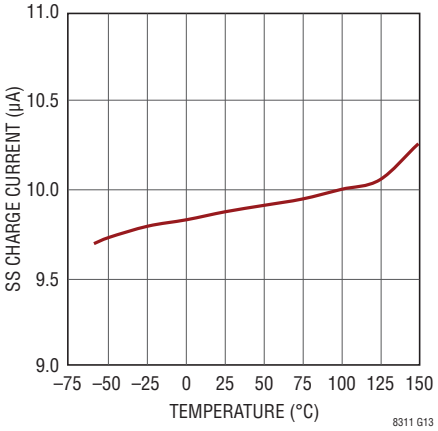
V_{IN} Quiescent Current, No Switching



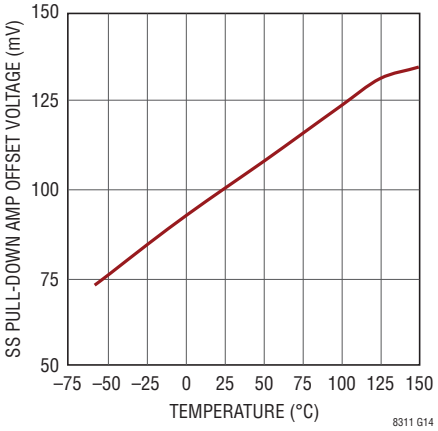
Power Good Window



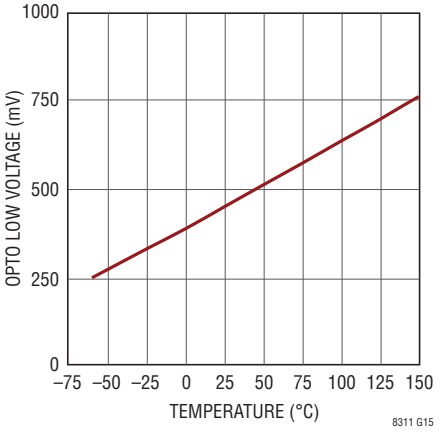
SS Charge Current



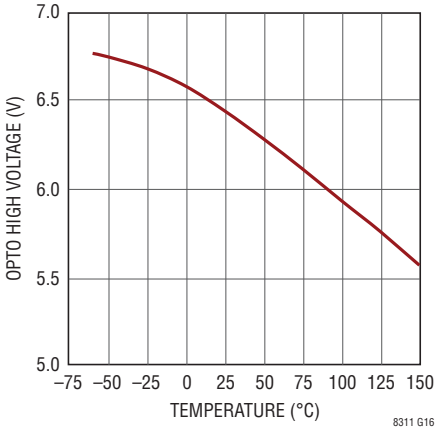
SS Pull-Down Amplifier Offset Voltage



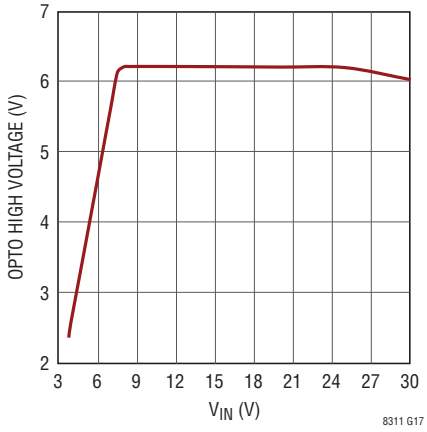
Opto-Driver Output Swing Low



Opto-Driver Output Swing High



Opto-Driver Output Swing High vs Line Voltage



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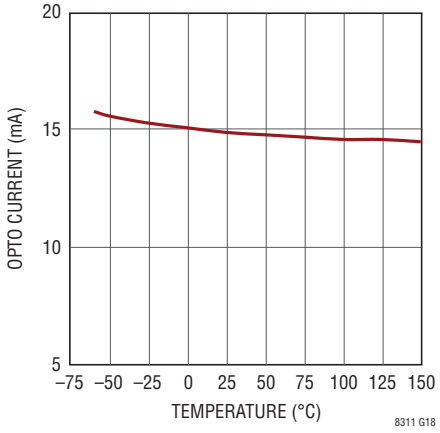
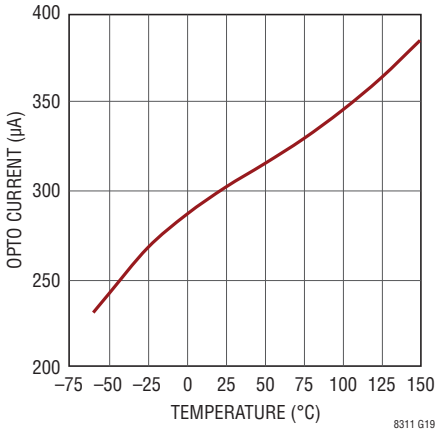
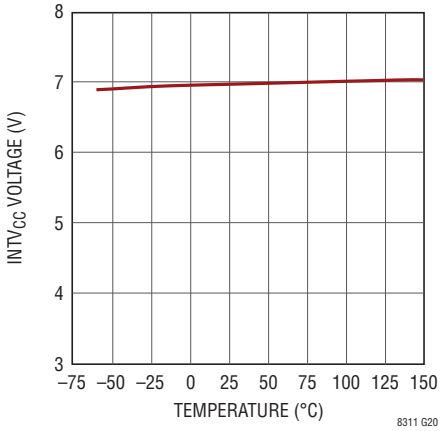
Opto-Driver Short-Circuit Current



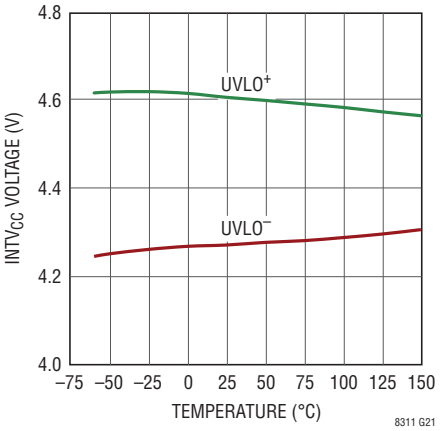
Opto-Driver Sink Current



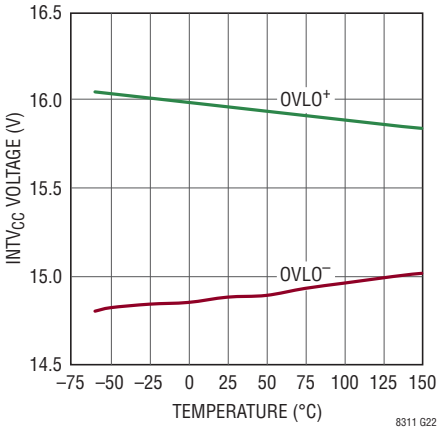
$INTV_{CC}$ Regulation Voltage



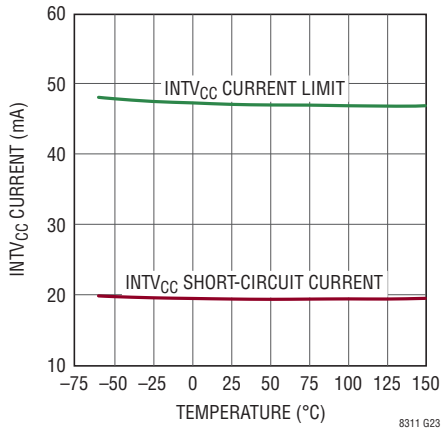
$INTV_{CC}$ UVLO



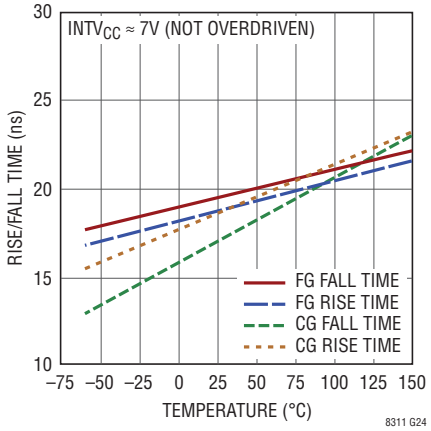
$INTV_{CC}$ OVLO



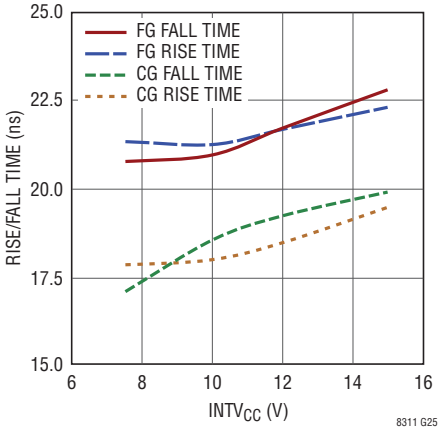
$INTV_{CC}$ Current Limit and Short-Circuit Current



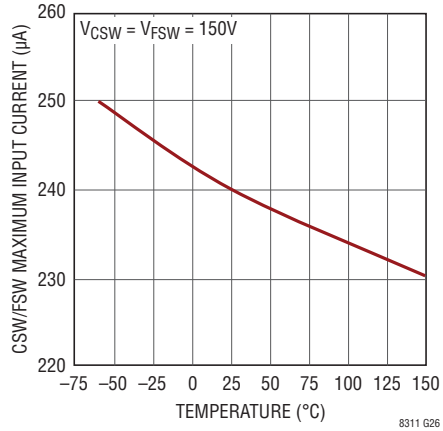
CG/FG Rise/Fall Time



CG/FG Rise/Fall Time vs $INTV_{CC}$ Voltage

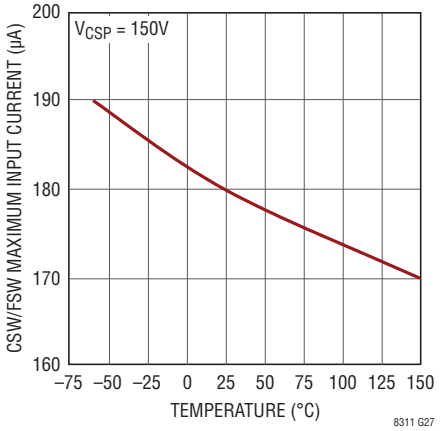


CSW/FSW Maximum Input Current

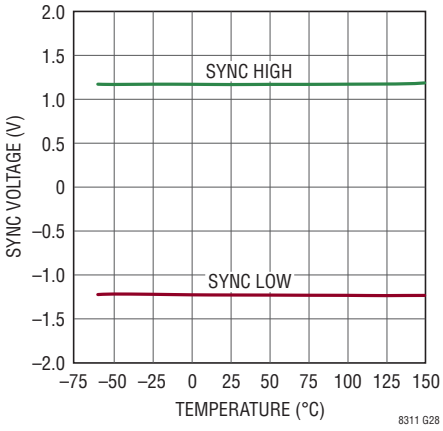


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

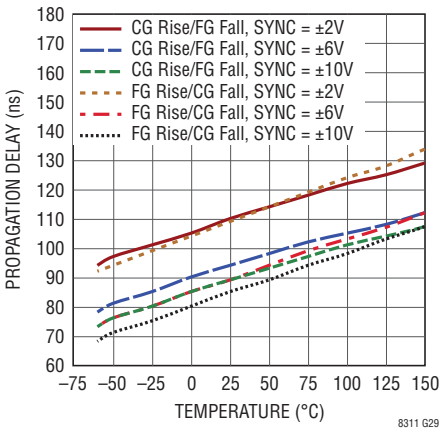
CSP Maximum Input Current



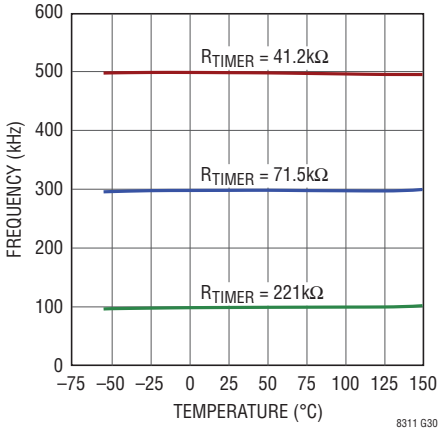
SYNC High/Low Trip Voltage



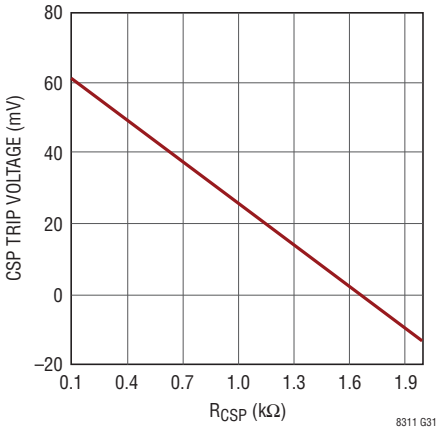
Prop Delay from SYNC Input to CG/FG Outputs



TIMER Frequency



CSP Trip Voltage vs Series CSP Resistor (R_{CSP})



PIN FUNCTIONS

CSW (Pin 1): Catch MOSFET Drain Sense Pin. Connect this pin to the external N-channel catch MOSFET's drain through a 2k resistor (typical) in preactive mode. Minimize parasitic capacitance on the pin. Connect to GND in SYNC mode.

FSW (Pin 3): Forward MOSFET Drain Sense Pin. Connect this pin to the external N-channel forward MOSFET's drain through 2k resistor (typical) in preactive mode. Minimize parasitic capacitance on the pin. Connect to GND in SYNC mode.

FG (Pin 5): Forward MOSFET Gate Driver Pin. This pin drives the gate of the external N-channel forward MOSFET. Minimize trace length between this pin and the forward MOSFET gate.

$INTV_{CC}$ (Pin 6): Internal Linear Regulator's Output Pin. $INTV_{CC}$ powers the gate drivers on the LT8311. The voltage on this pin is internally regulated to 7V. Alternatively, the pin can be overdriven externally. A minimum of 4.7µF (ceramic capacitor) must be placed from this pin to GND.

V_{IN} (Pin 7): Input Supply Pin. This pin must be locally bypassed.

$\overline{PMODE}$ (Pin 8): Preactive Mode Select Pin. Tying $\overline{PMODE}$ to GND enables preactive mode. Tying $\overline{PMODE}$ to $INTV_{CC}$ enables SYNC mode.

OPTO (Pin 9): Opto Driver Output Pin. Tie this pin, through a series resistor, to the input of the opto-coupler. This pin can source up to 10mA, sink 300µA typically, and is short-circuit protected.

COMP (Pin 10): Error Amplifier Output Pin. Tie an external compensation network to this pin when using the LT8311's transconductance error amplifier as part of a voltage feedback loop.

FB (Pin 11): Feedback Pin. This is the inverting input of the LT8311's internal error amplifier. The FB pin voltage tracks the lower of the internal 1.227V reference and the SS pin voltage. 75nA (bias current) typically flows out of the pin. Tie this pin to a resistor divider network from the output to set the desired output voltage.

TIMER (Pin 12): Switching Period Timeout Pin. A resistor from this pin to ground sets an upper limit on the sum of the forward and catch MOSFET on times (including dead time between the two MOSFETs on period), every cycle. If the sum of the on times of the catch and forward MOSFET, per cycle (including the dead time), exceeds the timeout period programmed by the TIMER resistor, then all synchronous conduction will be shut down. Synchronous conduction resumes when the timeout period is reset again. See the Applications Information section for more details on programming the TIMER resistor. Keep the ground return trace of this pin short, and away from paths with switching noise.

$\overline{PGOOD}$ (Pin 13): Output Power Good Pin. The open-drain output will be pulled to ground when the FB pin voltage stays within ±7% of the internal 1.227V reference for a period of 175µs. The internal $\overline{PGOOD}$ comparator has a hysteresis of ±3%. Therefore, when FB exists outside ±10% of the 1.227V reference, the $\overline{PGOOD}$ pin will be pulled high by an external pull-up resistor or current source.

SS (Pin 14): Soft-Start Pin. A capacitor from the SS pin to GND will be charged up by SS's internally trimmed 10µA current source. Since FB tracks the lower of the SS pin voltage and the internal reference of 1.227V, the charge rate of the SS pin can be used to set the slew rate at which the FB pin charges up to its regulation voltage of 1.227V. The SS pin typically charges up to 2V. When using the LT8311 as part of voltage feedback loop, place a ceramic capacitor of at least 1nF on this pin to GND. For details on SS start-up and overshoot control functions, please refer to the Applications Information section.

SYNC (Pin 15): Synchronization Pin. The SYNC pin, used only in SYNC mode, serves as an edge-sensitive input to receive timing information for synchronous switching. It is typically driven with PWM synchronization signals from the primary-side IC through a pulse transformer. A negative voltage slew on the SYNC pin (–1.2V threshold) turns on the forward MOSFET and turns off the catch MOSFET. Equivalently, a positive voltage slew (1.2V threshold) turns on the catch MOSFET and turns off the forward MOSFET. Tie the SYNC pin to GND in preactive mode.

CG (Pin 16): Catch MOSFET Gate Driver Pin. This pin drives the gate of the external N-channel catch MOSFET. Minimize trace length between this pin and the catch MOSFET gate.

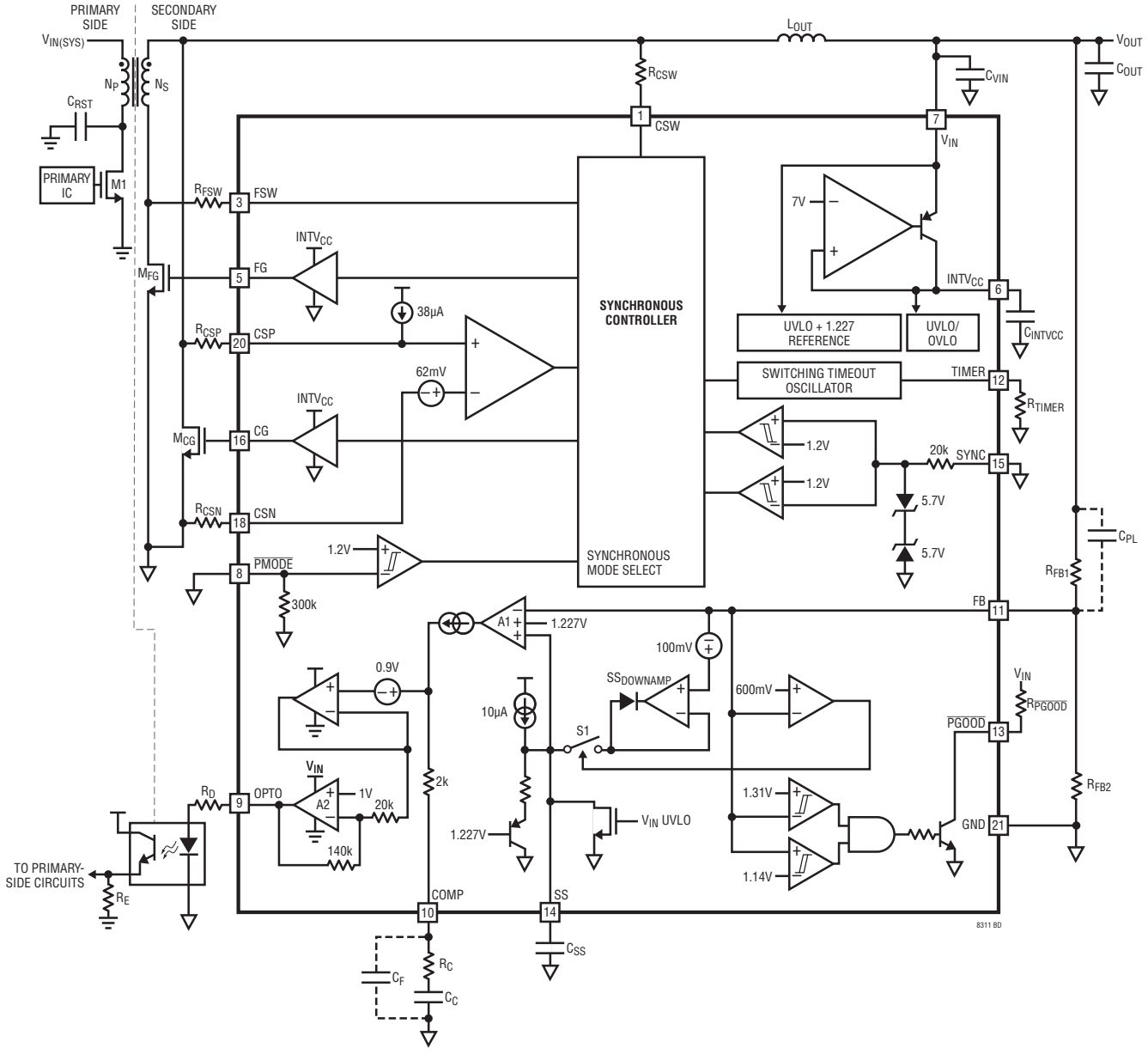
CSN, CSP (Pin 18, Pin 20): Current Sense Differential Inputs. CSP and CSN are the positive and negative inputs, respectively, of the LT8311's internal current sense comparator. The pins are typically connected across the catch

PIN FUNCTIONS

MOSFET to perform V_{DS} current sensing. Alternatively, if a more precise current sensing mechanism is desired, the pins may be connected across a sense resistor at the catch MOSFET's source. The current comparator trips at 62mV typical. The CSP pin sources 38µA current, allowing trip voltages less than 62mV to be set by placing a resistor in series with the CSP pin. It is recommended to place an identical resistor in series with the CSN pin to match any voltage offsets created by the input bias current (100nA) of the current comparator. In preactive mode, the CSP and CSN pins must be configured to trip at zero or positive values of source to drain current in the catch MOSFET (current in catch MOSFET cannot be allowed to flow from drain to source in preactive mode).

GND (Exposed Pad Pin 21): Ground. Exposed pad must be soldered directly to local ground plane.

BLOCK DIAGRAM



OPERATION

The LT8311 controls the synchronous MOSFETs and opto-coupler on the secondary side of a forward converter. Synchronous control of low $R_{DS(ON)}$ MOSFETs can typically lead to lower power dissipation in forward converters. The lower power dissipation can improve converter efficiency, resulting in long term cost savings by lowering input power requirements to support a certain level of output power. Improved efficiency can also reduce the size of heat sinks required to dissipate the heat generated in the rectifiers; consequently increasing the operating ambient temperature range which may be useful in many industrial applications.

The LT8311 also offers opto-coupler control for accurate output voltage regulation over line and load. The LT8311's opto-coupler control circuitry comes with a host of start-up and steady-state functions to ensure robust transient response during power-on and output short-circuit recovery.

FUNDAMENTALS OF FORWARD CONVERTER OPERATION IN CCM

The timing diagram of a forward converter operating in continuous conduction mode (CCM) is shown in Figure 2. The timing diagram is broken into six regions of operation. Please refer to Figures 1 and 2 for the following explanation of each region of operation.

Region 1 (Figure 2)

When OUT goes high, M1 turns on. CG should already be at 0V before OUT goes high, to ensure that M_{CG} does not cross conduct with M1. The LT8311's preactive mode, which will be explained later, is an innovative scheme to turn off M_{CG} before M1 turns on. FG must be high during this period to keep the forward MOSFET, M_{FG} on, thereby conducting the output inductor current, I_{LOUT}, (via the transformer's secondary winding) through a low impedance path. During this phase, magnetizing current, I_{LMAG}, builds up in the transformer's magnetic core, and flows from V_{IN} to GND through M1. Output inductor current, I_{LOUT}, ramps up at a rate of $(V_{CSW} - V_{OUT})/L_{OUT}$.

Region 2 (Figure 2)

When OUT goes low, and turns off M1, the transformer becomes high impedance, and stops conducting I_{LOUT}. Since current in the output inductor cannot go to zero instantaneously, it pulls the drain of the catch MOSFET, CSW, towards ground. Ultimately CSW gets clamped at a diode voltage below ground by M_{CG}'s body diode which now sources the output inductor current (similar to a catch diode in a traditional buck converter). CSW collapsing equivalently causes the transformer's secondary winding voltage to become smaller. Through transformer action,

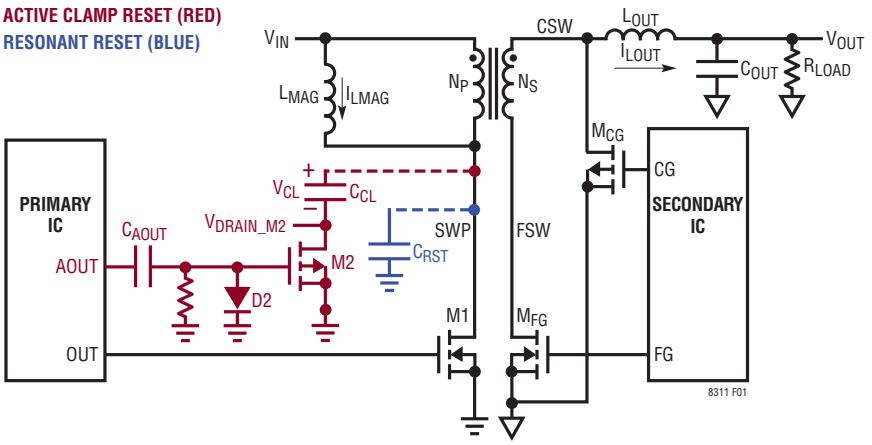


Figure 1. Forward Converter with Active Clamp Reset (in Red) or Resonant Reset (in Blue)

OPERATION

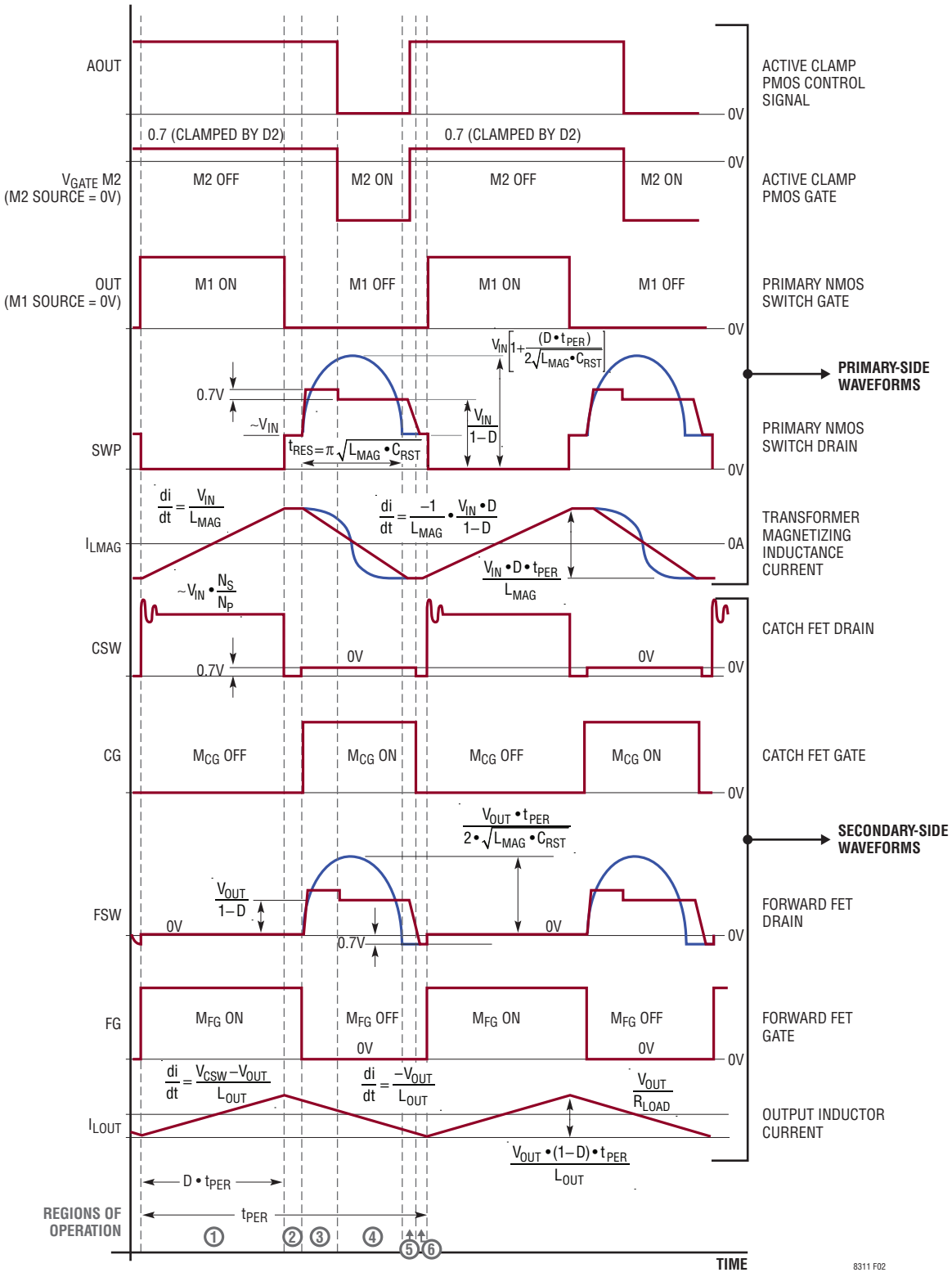


Figure 2. Active Clamp Forward Converter Timing Diagram in CCM. Resonant Reset Waveforms in Blue

OPERATION

the primary winding voltage gets smaller too, effectively moving SWP towards V_{IN}. Since M_{FG} is still on, and M_{CG}'s body diode is on, the secondary winding voltage gets clamped at about a diode voltage. Through transformer action, SWP gets clamped to approximately V_{IN}. I_{LMAG} flows in the secondary windings, as shown in Figure 3, flowing from the drain to source of M_{FG}, to ground. M_{CG}'s body diode sources I_{LOUT} and I_{LMAG}.

Region 3 (Figure 2)

When FG goes low, it allows transformer reset action to begin. I_{LMAG} no longer has a low impedance path through M_{FG} on the secondary side. As a result, it "jumps back" to the primary side, flowing into the primary-side resonant capacitor. In resonant reset, I_{LMAG} flows into C_{RST} as soon as M_{FG} turns off, causing SWP's voltage to rise up quasi-sinusoidally, with a time constant set by L_{MAG} and C_{RST}. In active clamp reset, when M_{FG} turns off, I_{LMAG} intially slews up SWP's voltage quickly. As shown in Figure 2, I_{LMAG} does not flow into the active clamp capacitor as soon as M_{FG} turns off. The voltage across C_{CL} (= V_{CL} = V_{IN}/(1-D)) initially reverse biases M2's body diode. Only when SWP's voltage gets high enough to forward bias M2's body diode, does I_{LMAG} begin to flow into C_{CL}. The voltage where this happens is when SWP = V_{CL} + 0.7V. At this point, SWP's voltage rises up at a rate determined by the time constant of L_{MAG} and the active clamp capacitor, which is typically much larger than the resonant reset capacitor.

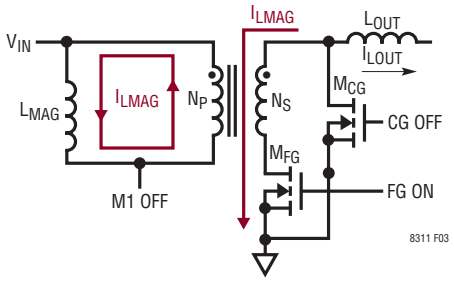


Figure 3. With FG On, I_{LMAG} Is Conducted Through M_{FG} to Ground on the Secondary Side When M1 Turns Off

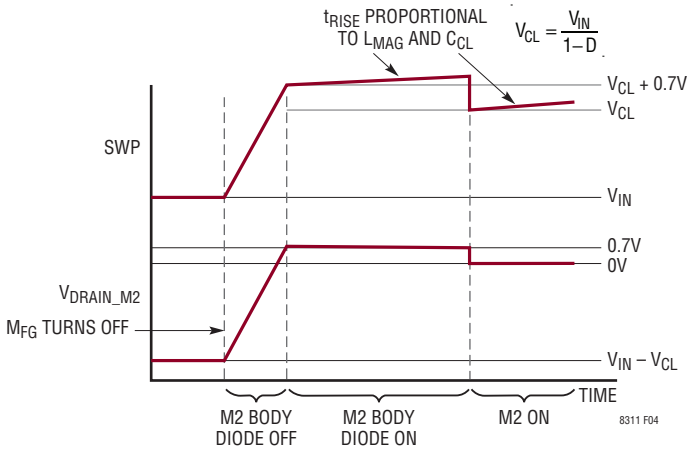


Figure 4. Detail of Region 3 from the Timing Diagram in Figure 2. When M_{FG} Turns Off in Active Clamp Reset, I_{LMAG} Initially Slews Up SWP's Voltage from V_{IN} to V_{CL} + 0.7V, at Which Point M2's Body Diode Turns On and Allows I_{LMAG} to Flow into C_{CL}

OPERATION

The ultimate goal of both reset mechanisms is to raise the SWP node to a voltage higher than V_{IN}, imposing appropriate volt seconds on L_{MAG}, and allowing the magnetizing current to reset. Resetting the magnetic core every cycle prevents magnetic flux buildup within the core, and thereby prevents transformer saturation. FSW tracks the SWP node during transformer reset. CG going high, allows I_{LOUT} to switch over from being conducted by M_{CG}'s body diode to M_{CG} itself.

Region 4 (Figure 2)

1. **Active Clamp Reset Case (red waveform):** AOUT going low causes the gate of M2 to be driven below ground by the decoupling capacitor, C_{AOUT}. This causes M2, the active clamp PMOS, to turn on. M2 must be turned on before I_{LMAG} becomes negative, to allow I_{LMAG} to sustain conduction through the active clamp capacitor and get fully reset. Active clamp reset completes by the end of region 4, and I_{LMAG} is reset to a negative value.
2. **Resonant Reset Case** (blue waveform): Resonant reset ultimately completes when SWP's quasi-sinusoidal waveform returns to V_{IN}, by which point I_{LMAG} is reset to a negative value. FSW is eventually clamped by M_{FG}'s body diode, and conducts I_{LMAG}, through the secondary windings, towards the output inductor (similar to Figure 3, but with I_{LMAG} direction reversed on primary and secondary sides). With a diode voltage imposed across the secondary windings, transformer action causes the primary winding to have a similar voltage (scaled by turns ratio), resulting in SWP's voltage getting clamped to V_{IN}. M_{CG} continues conducting $I_{LOUT} - I_{LMAG}$.

Region 5 (Figure 2)

Active Clamp Reset Case: AOUT goes high, turning off M2. I_{LMAG}, being negative, causes the voltage on SWP (M1's drain) to get pulled towards V_{IN}, resulting in the transformer's primary winding voltage becoming smaller. By transformer action, the secondary winding voltage also becomes smaller. With M_{CG} on (holding CSW at 0V), and the transformer secondary winding voltage becoming smaller, FSW collapses towards 0V.

Region 6 (Figure 2)

Eventually, in similar fashion to the resonant reset case, FSW is clamped to a diode voltage below GND by M_{FG}'s body diode, which now conducts I_{LMAG} through the secondary windings, towards the output inductor. With M_{FG}'s body diode on, and M_{CG} on, the secondary winding voltage gets clamped to about a diode voltage. Through transformer action, SWP gets clamped to approximately V_{IN}. CG goes low, turning off M_{CG} before M1 can turn on. $I_{LOUT} - I_{LMAG}$ is conducted through M_{CG}'s body diode. FG goes high, turning on M_{FG}. Eventually, when M1 turns on, I_{LOUT} will be conducted through the transformer's secondary winding, and will flow from the source to drain of M_{FG}.

OPERATION

LT8311 SYNCHRONOUS CONTROL SCHEMES

The LT8311 offers two modes of synchronous control:

1. **Preactive Mode:** No pulse transformer needed; DCM operation at light load. Enabled by tying the $\overline{PMODE}$ pin to 0V. Use a Schottky diode across M_{CG} (Figure 20).
2. **SYNC Mode:** Pulse Transformer needed; FCM or DCM operation at light load. Enabled by tying the $\overline{PMODE}$ pin to $INTV_{CC}$.

PREACTIVE MODE SYNCHRONOUS CONTROL

M_{CG} Turn-On/Off Timings in Preactive Mode

"Preactive" is short for "predictive" + "reactive". In preactive mode, the LT8311 controls the secondary synchronous MOSFETs without any communication from the primary-side IC. In preactive mode, the catch MOSFET, M_{CG}, is turned on (CG rising edge in Figure 5) when the voltage on its drain, CSW, is detected to be below –150mV, and the forward MOSFET, M_{FG}, is detected to be off. M_{CG} is turned off when the first of two events after M_{CG}'s turn-on occurs:

- **Predictive M_{CG} Turn-Off** (Figure 5): In predictive turn-off, the LT8311 predicts when M1 will turn on in the next cycle, and turns off M_{CG} 100ns prior to this event. Predictive turn-off of M_{CG} prevents cross conduction between M_{CG} and M1. M1's turn-on timings are predicted by phase locking to the rising edge of present and past CSW cycles. Predictive turn-off relies on the periodicity of M1's turn-on edge, an inherent aspect of fixed-frequency operation. Furthermore, the predictive turn-off is designed to be independent of the duty cycle of the system, which allows M_{CG} to be correctly turned off, even during load/line transients. Predictive turn-off will typically be the dominant turn-off mechanism for M_{CG} in CCM.
- **Reactive M_{CG} Turn-Off** (Figure 6): Reactive turn-off forces the forward converter to operate in DCM at light load. In reactive turn-off, the LT8311 turns off M_{CG} when the current in M_{CG} (I_{MCG}) trips the LT8311's internal current comparator. The inputs to this current comparator are the CSP and CSN pins. Typically, the CSP and CSN pins will be configured to trip at almost zero current in M_{CG}, which should correspond to nearly zero current in the output inductor. Reactive turn-off will typically be the dominant turn-off mechanism for M_{CG} in DCM.

The LT8311's seamless transition between predictive and reactive portions of preactive mode allows the catch MOSFET to be turned off at the correct time to avoid cross conduction or avalanching.

M_{FG} Turn-On/Off in Preactive Mode

In preactive mode, M_{FG} is turned on after M_{CG}'s turn-off edge is detected, and the voltage on the drain of the forward MOSFET, FSW, is detected to be below 1.2V. Waiting for FSW to fall below 1.2V ensures that transformer reset is close to completion. M_{FG} is turned off when the voltage on CSW is detected to be below –150mV.

Since preactive mode requires each MOSFET to be turned on only after the other MOSFET's turn-off edge is detected, the system requires a start point where one of the two MOSFETs begins switching. Preactive mode's start point happens by turning on M_{CG} first to commence switching.

Preactive Mode Shutdown and Start-Up

Preactive mode is designed with many features to facilitate smooth start-up of synchronous control and shut down of the scheme when necessary. Prior to starting switching activity, the LT8311 evaluates conditions on the forward converter's secondary side to determine if switching can commence. The evaluation period ends when four specific conditions, are satisfied for a period of three continuous CSW switching cycles (rising edge to rising edge). If any of the conditions are violated, the evaluation period is reset, and switching activity is kept shut off. During this evaluation period, the secondary side current will flow through the body diodes of M_{CG} and M_{FG}. The four conditions are:

1. V_{IN} must be greater than its UVLO voltage
2. $INTV_{CC}$ must be within its UVLO/OVLO limits
3. The TIMER pin should not have timed out. This feature exists to ensure that the LT8311 ceases switching in the event that the primary side stops switching.

OPERATION

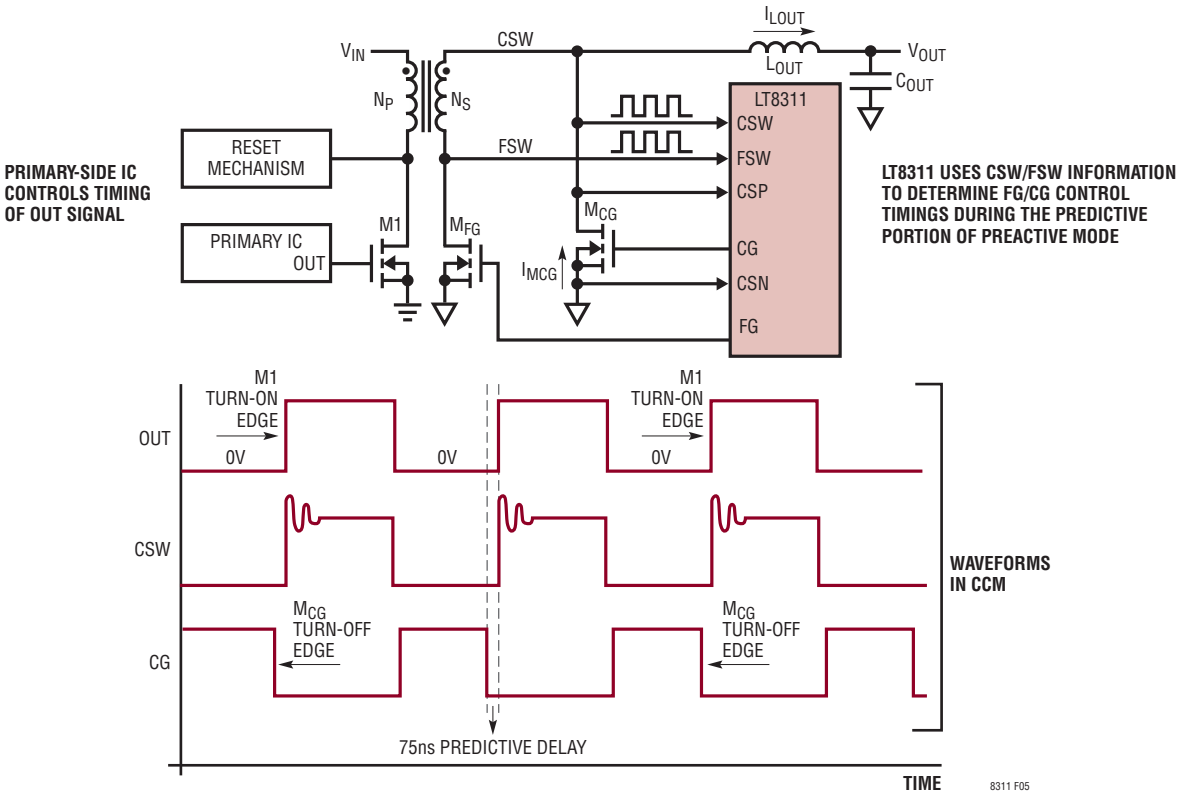


Figure 5. During the Predictive Portion of Preactive Mode, the LT8311 Phase Locks into the CSW Rising Edge and Turns Off M_{CG} 75ns Prior to This Edge

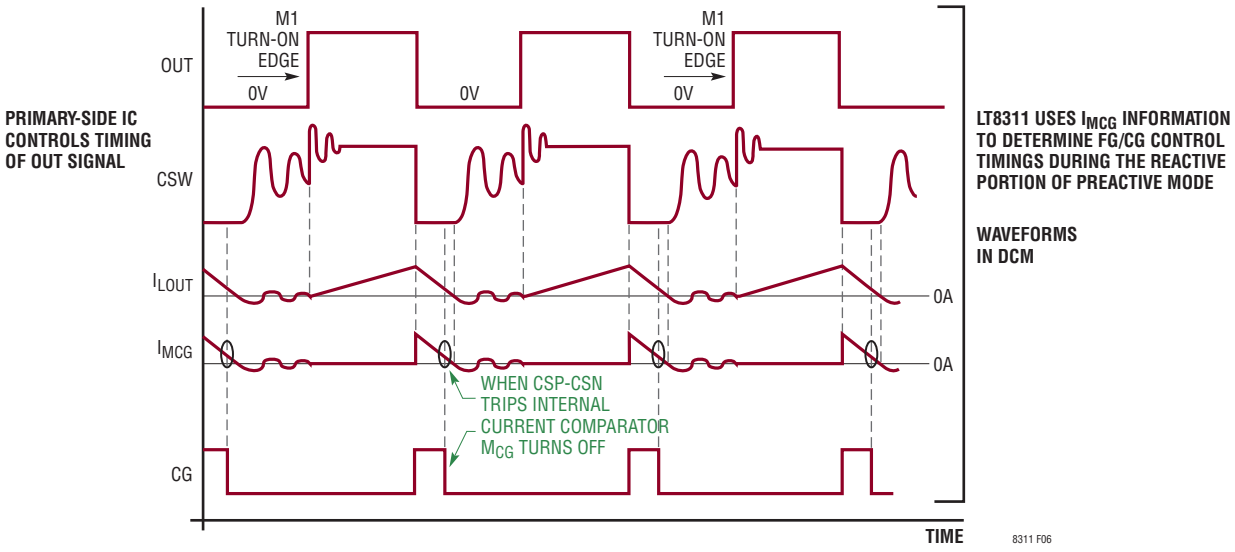


Figure 6. During the Reactive Portion of Preactive Mode, the LT8311 Turns Off M_{CG} When the Current in M_{CG}, I_{MCG}, Trips the LT8311's Internal Current Comparator. The Inputs to the Comparator Are CSP and CSN and the Current Sense Trip Voltage Is Programmed by Choosing Appropriate CSP/CSN Series Resistors

OPERATION

4. The CSP and CSN pins must not trip the internal current comparator within a 150ns period of time called "current sample window." This function helps the LT8311 detect very light load conditions, during which time it will keep synchronous conduction shut off, thereby improving system efficiency.

   How the current sample window works:
   The current sample window exists regardless of whether M_{CG} is turned on or not, in any given cycle. When CSW is detected to fall below –150mV, the LT8311 starts a blank time of 200ns. Upon completion of this blank time, the LT8311 starts a 150ns current sample window. If the CSP/CSN pin inputs cause the internal current comparator to trip during this 150ns window, the LT8311 will interpret this as a condition of very light load, at which point it will stop synchronous conduction and start the evaluation period again. Please see "Configuring CSP/CSN Inputs of Current Sense Comparator in Preactive Mode" in the Applications Information section.

When all four conditions are valid for three continuous CSW cycles, the evaluation period ends and the LT8311 gets ready to start switching. Switching commences with the LT8311 turning on M_{CG} for its minimum on-time. **If any of the four conditions listed are violated at any point during switching activity, the LT8311 will shut down all synchronous conduction and restart the evaluation period.**

During preactive mode start-up, the LT8311 internally soft-starts the on-time of M_{CG}, allowing the forward converter to gradually transition from full cycles of nonsynchronous M_{CG} conduction (secondary-side current flowing through body diode of M_{CG}) to full cycles of synchronous M_{CG} conduction.

SYNC MODE SYNCHRONOUS CONTROL

SYNC mode allows the LT8311 to operate in forced continuous mode (FCM) at light loads. In SYNC mode, a pulse transformer (see T2 in Figure 7) is required to allow the LT8311 to receive synchronization control signals from the primary-side IC. These control signals are interpreted digitally (high or low) by the LT8311 to turn on/off the catch and forward MOSFETs.

FCM operation allows the forward converter to avoid operation in discontinuous conduction mode (DCM) at light loads, by letting the inductor current go negative. Hence, even at zero load, the inductor current remains continuous and the converter runs at a fixed frequency.

M_{CG} Turn-On/Off Timings in SYNC Mode

In SYNC mode, M_{CG} turns on when the signal on the SYNC pin is higher than 1.2V. M_{CG} turns off when the signal on the SYNC pin is lower than –1.2V.

M_{FG} Turn-On/Off Timings in SYNC Mode

In SYNC mode, M_{FG} turns on when the signal on the SYNC pin is lower than –1.2V. M_{FG} turns off when the signal on the SYNC pin is higher than 1.2V.

The R_{SYNC} and C_{SYNC} time constant must be appropriately chosen to generate a sufficient pulse width at a particular overdrive voltage (see "Picking Pulse Transformer and High Pass Filter" in the Applications Information section). Typical values for C_{SYNC} and R_{SYNC} are 220pF and 560Ω, respectively.

OPERATION

SYNC Mode Shutdown

In SYNC mode, the LT8311 will shut off both secondary-side MOSFETs, M_{CG} and M_{FG}, if any of the following conditions are true:

1. V_{IN} is less than its UVLO voltage
2. $INTV_{CC}$ outside its UVLO/OVLO limits
3. The TIMER pin has timed out (see the Applications Information section for details on programming the TIMER pin resistor).
4. The CSP and CSN pins have tripped the LT8311's internal current comparator during M_{CG}'s on-time. The current in M_{CG}, I_{MCG}, is sensed after a 400ns blank time has expired. This blank time starts at the turn-on edge of M_{CG}. See the Applications Information section for details on configuring the CSP and CSN pins in SYNC mode.

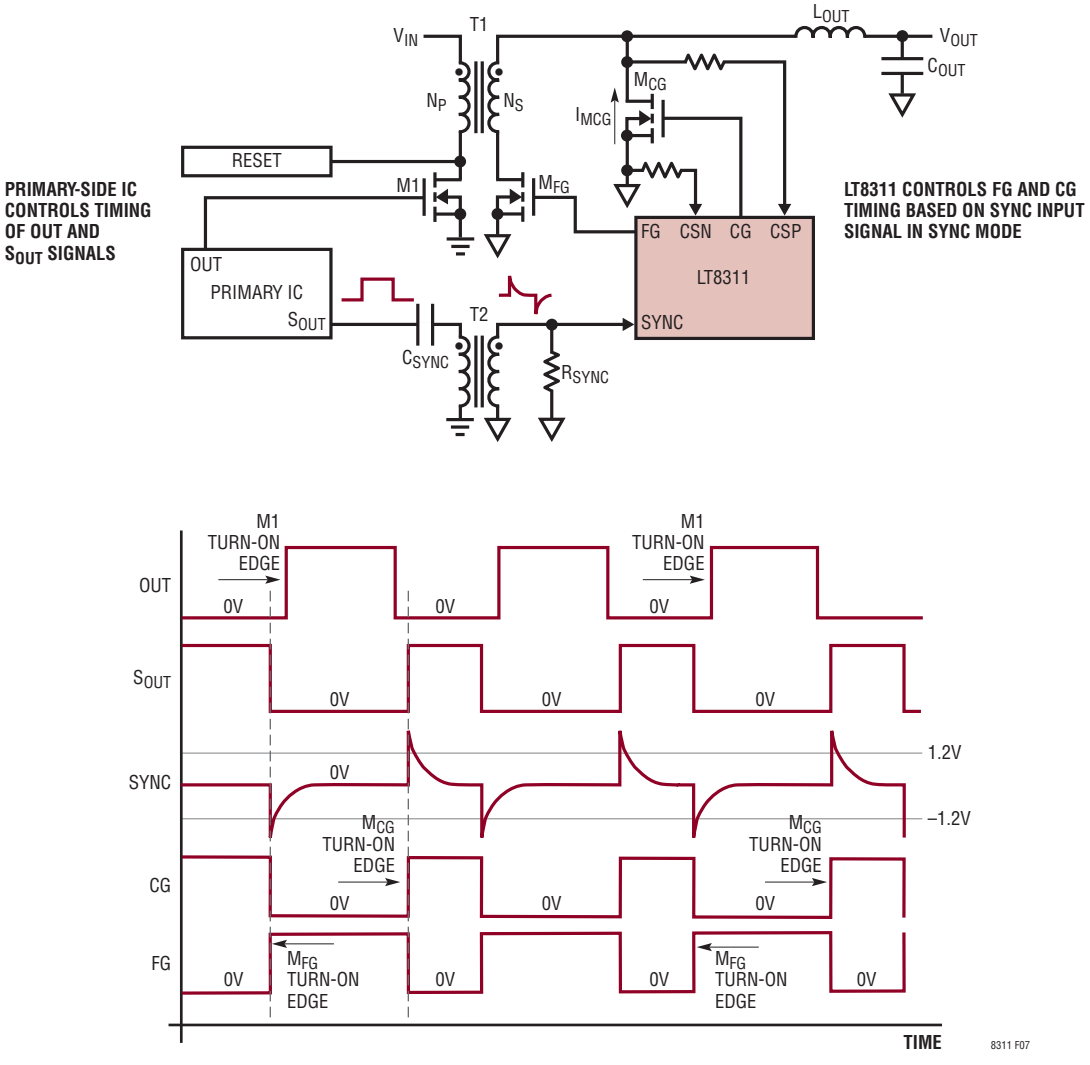


Figure 7. In SYNC Mode, the Primary Side IC Sends S_{OUT} Signals Through a Pulse Transformer to the LT8311's SYNC Pin. SYNC < 1.2V Turns on M_{FG} and Turns Off M_{CG}. SYNC > 1.2V Turns On M_{CG} and Turns Off M_{FG}

OPERATION

OPTO-COUPLER CONTROL

The LT8311 offers opto-coupler control to allow output voltage feedback from the secondary to the primary side in a forward converter. Used in conjunction with a primary-side IC, the entire system offers fixed frequency peak current mode control that has excellent line/load regulation and quick transient response.

A basic understanding of the LT8311's opto-coupler control scheme can be obtained by referring to Figure 8. The LT8311 senses the output voltage through a resistor divider (R_{FB1} and R_{FB2}) connected to its FB pin. The FB pin voltage is compared to the lower of two inputs:

- An internal voltage reference of 1.227V
- Soft-start (SS) pin

At start-up, the SS pin capacitor, C_{SS}, is charged up by the LT8311's internally trimmed 10µA current source. Since FB tracks the lower of the SS pin and the 1.227V reference, the FB pin (and by extension the output voltage) is forced to soft-start at the slew rate set by the capacitor, C_{SS}, connected to the SS pin.

NOTE: To ensure that the soft-start time of the converter is controlled by the LT8311's SS capacitor, C_{SS}, it is important to program the primary IC's soft-start faster, to get out of the way. If this is not done, the converter's soft-start time will be dominated by the primary IC's soft start, and the LT8311 will simply adjust its SS pin voltage and slew rate to match the slower soft start time set by the primary-side IC.

When the SS pin voltage gets higher than the 1.227V reference, the FB pin starts to track the 1.227V reference. The output, therefore, regulates at a voltage set by the R_{FB1}/R_{FB2} divider network, and the FB pin's regulation voltage of 1.227V. The SS pin capacitor continues to get charged up by the 10µA current source until it reaches its internal clamp voltage of 2V.

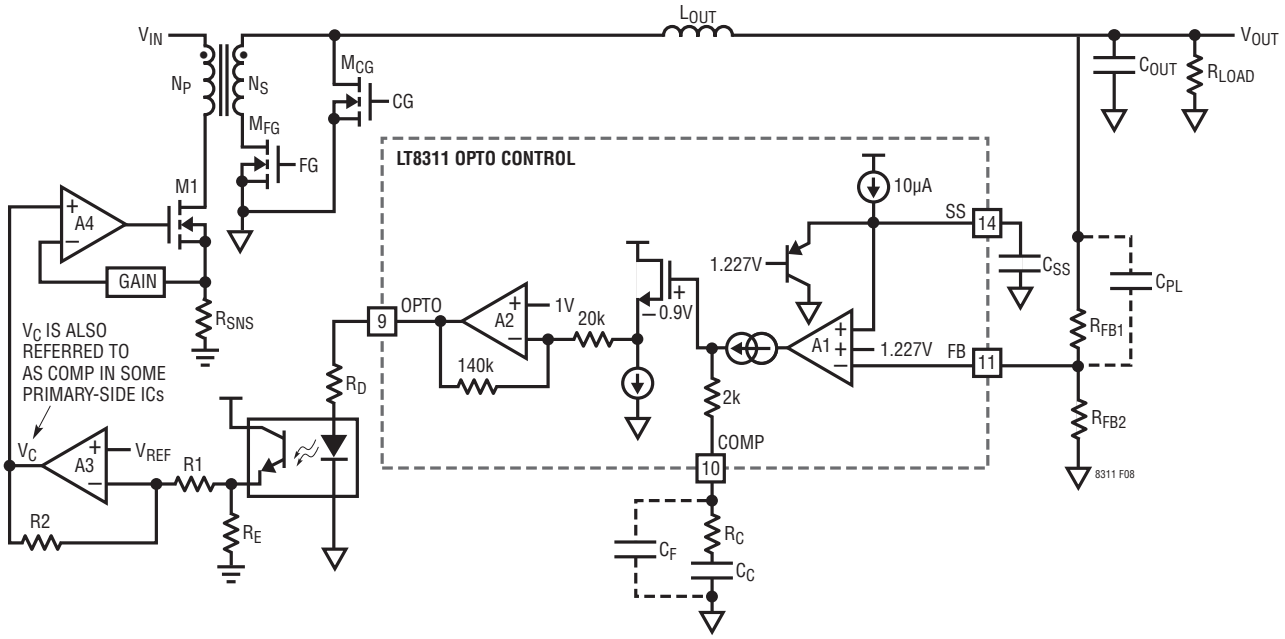


Figure 8. The LT8311 Provides Voltage Feedback, as Part of a Peak Current Mode Control System, in a Forward Converter

OPERATION

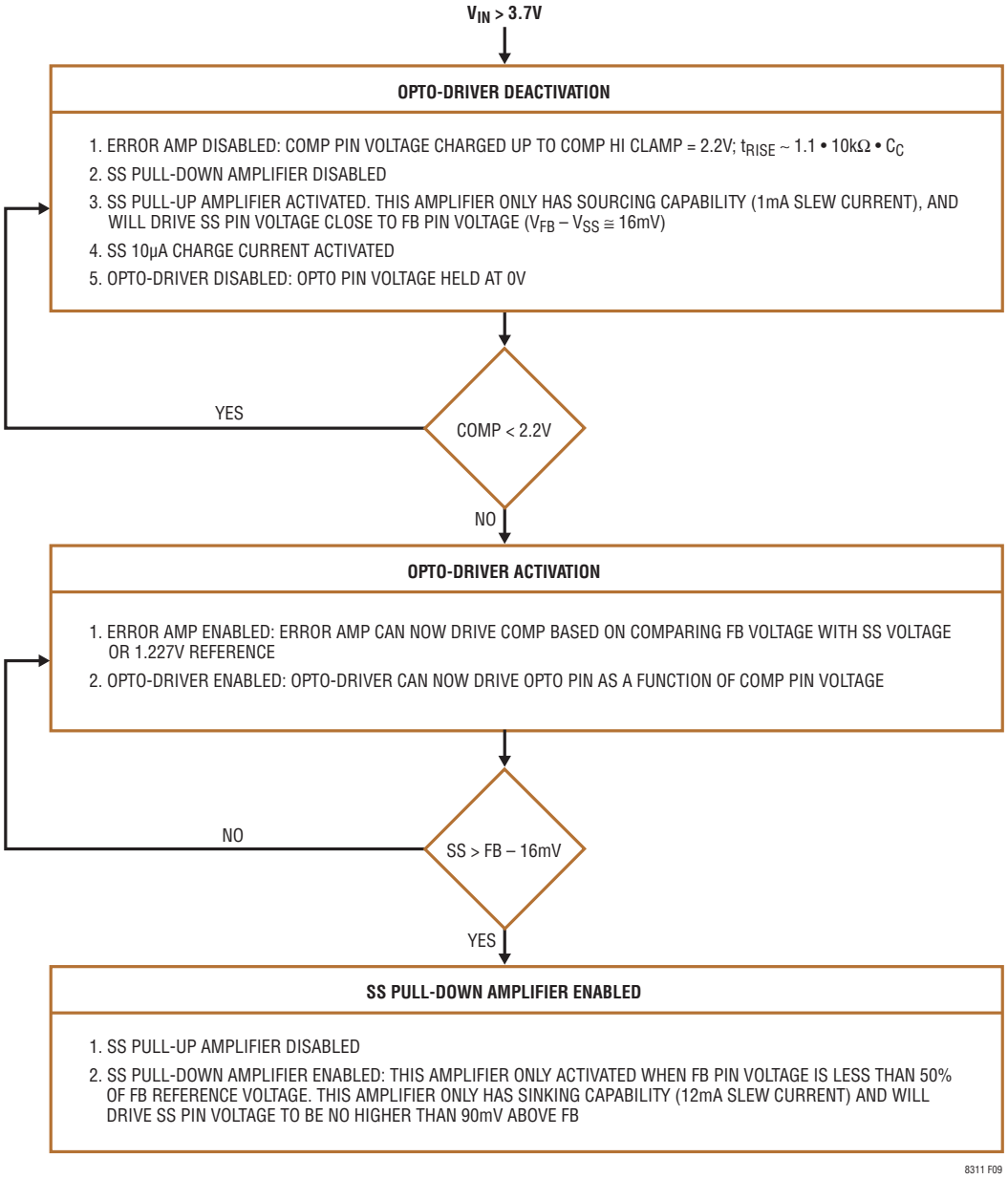


Figure 9. Flowchart for LT8311 Opto Control Operation at Start-Up

With SS charged up to 2V, the transconductance error amplifier, A1, sinks or sources current from its output, COMP, if there is any voltage difference between the FB pin voltage and the 1.227V reference. The COMP pin, offset by 0.9V, serves as the input to the opto-driver, A2. If an increase in output load current causes the FB pin voltage to be lower than 1.227V, A1 drives the COMP pin high. COMP going high forces A2 to drive OPTO low, sourcing less current through R_D into the opto-coupler.

Since an opto-coupler's output current is directly proportional to its input current, this decreased input current for the opto-coupler will cause its output current, and therefore its emitter voltage at R_E, to decrease as well. The drop in R_E voltage causes A3, through its inverting action, to drive its output, V_C, higher. An increase in the V_C voltage causes the comparator, A4, to command a higher sense voltage across the R_{SNS} resistor, commanding M1 to run at a higher peak current. Since the current through M1 is

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directly proportional to the output inductor current (M1 Current • $N_P/N_S = I_{LOUT}$), an increase in M1's peak current translates into an increase in the output inductor's peak current. In essence, the feedback loop is commanding the output inductor peak current to meet the demands of the increased load current, with the ultimate goal of helping the output voltage recover from a load step and stay regulated.

Opto-Control Operation at Start-Up

For applications connecting the LT8311's V_{IN} pin directly to the converter output, the LT8311 includes intelligent circuitry to ensure no interruption in the switching of the primary-side MOSFET upon the LT8311's turn-on. The LT8311 turns on when its V_{IN} pin (and therefore the converter output voltage when V_{IN} is directly connected to the output) exceeds 3.7V. Without intelligent circuitry, this V_{OUT} level will cause the FB pin voltage of the LT8311 to be greater than the voltage on the LT8311's SS pin (which is typically at 0V upon turn-on of the IC), causing amplifier A1 to drive the COMP pin low. This drives the OPTO pin high, which causes full current into the opto-coupler and terminates switching of the primary-side MOSFET. Termination of the primary-side MOSFET's switching can lead to the converter's output voltage dropping, which could cause the LT8311 to lose power and shut off. The LT8311's intelligent circuitry prevents this situation using two unique features. It has a built-in 100mV hysteresis on its V_{IN} UVLO voltage, so that upon getting power, it can tolerate up to a 100mV drop on its V_{IN} pin before losing power again. Even more importantly, the LT8311 has an opto-control start-up system that keeps the LT8311's "opto-control brains" turned off until all relevant node voltages within the voltage loop are prebiased to a state where they will not cause switching activity to cease when the loop is eventually enabled.

As shown in Figure 9 and the scope shot in Figure 10, the LT8311's opto-control operation at start-up involves slewing the SS pin voltage close to the FB pin voltage, slewing the COMP pin voltage to its high clamp voltage, and keeping the OPTO pin voltage held low. During this phase, the inductor current (and by extension, the output voltage) is controlled by the soft-start function provided by the primary-side IC. Upon completion of the state machine, the LT8311 allows the feedback loop to be functional again, and the FB pin voltage tracks the LT8311's SS pin voltage until FB finally gets to its regulation target of 1.227V.

Power Good

The LT8311 offers output power good monitoring to assist with system level design. The LT8311's $\overline{\text{PGOOD}}$ pin is pulled low internally when the FB pin voltage stays within a ±7% window of the 1.227V reference for a period of 175µs. Waiting for 175µs to elapse prevents the $\overline{\text{PGOOD}}$ pin from indicating false positives during transient events.

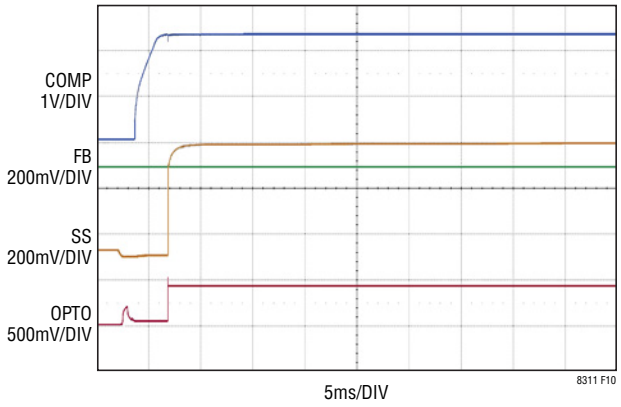

Figure 10. Opto Control Operation at Start-Up

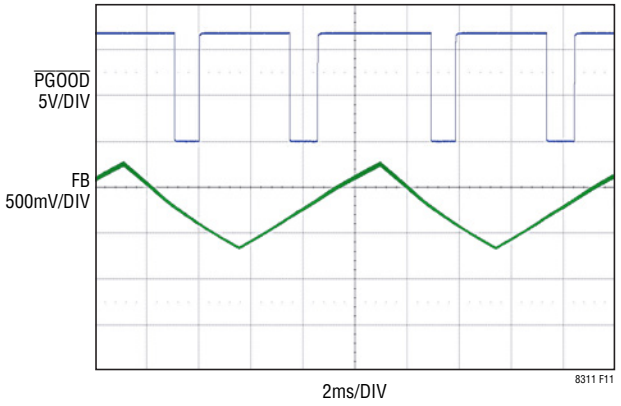

Figure 11. Power Good Activates ($\overline{\text{PGOOD}}$ = Low) When the LT8311's FB Pin Voltage Is Within ±7% of Its Regulated Target (1.227V). The $\overline{\text{PGOOD}}$ Pin Is Pulled Up Externally to a 12V Housekeeping Supply Through a 100k External Resistor

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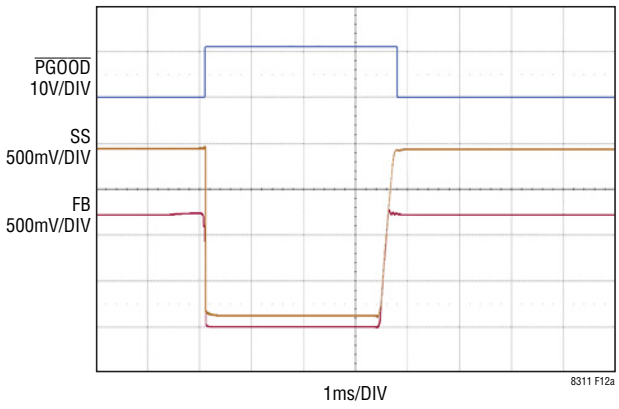
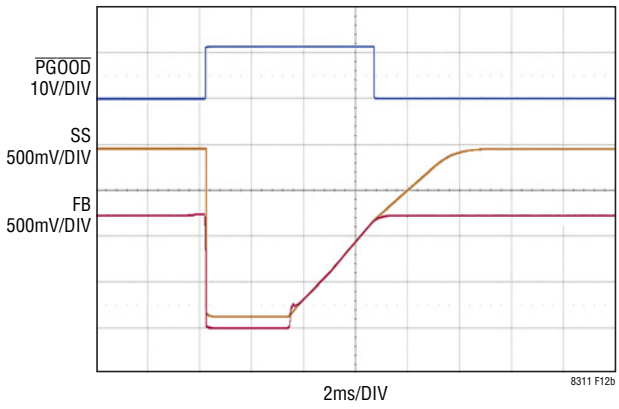
The $\overline{\text{PGOOD}}$ comparator has ±3% hysteresis. Therefore, when the FB pin voltage is driven away from its regulated value of 1.227V by ±10%, the $\overline{\text{PGOOD}}$ pin's internal pull-down shuts off immediately. As a result, the pin is pulled high by an external resistor or external current source connected to a supply voltage. The $\overline{\text{PGOOD}}$ pin's output can be fed to a microcontroller that make decisions based on the state of the output voltage.

Output Overshoot Control Helps with Short-Circuit Recovery

The LT8311 provides output overshoot control by activating its soft-start pull-down amplifier ($SS_{DOWNAMP}$ in the Block Diagram) any time the FB pin voltage is less than 50% of the FB reference voltage (1.227V). This is particularly helpful with output voltage recovery after the removal of a short-circuit condition or after a heavy load transient. The SS pull-down amplifier will sink whatever current is necessary (up to its maximum sink capability of 13mA), to ensure that the SS pin voltage gets no higher than 100mV above the FB pin voltage. During output short-circuit events, when the FB pin voltage is pulled to ground, the SS pull-down amplifier gets activated and pulls the SS pin voltage to 100mV above the FB pin voltage. Eventually, when the short-circuit condition is over, the FB pin voltage gradually rises up with the SS pin at a slew rate set by C_{SS} and the 10µA charge current. This allows the output to recover gradually from the short-circuit condition. Note that when the LT8311 has its V_{IN} pin powered directly from the output of the forward converter, it will lose all its brains during a short-circuit event. Under this scenario, output overshoot control will not be in effect until the LT8311 gets brains again, until which point, the output inductor current and the output voltage will be controlled by the primary-side IC's soft-start function.



(a) Output Overshoot Control with C_{SS} = 1nF. LT8311 V_{IN} Powered from a 12V Housekeeping Supply, Which Also Pulls Up on the $\overline{\text{PGOOD}}$ Pin Through a 100k External Resistor



(b) Output Overshoot Control with C_{SS} = 33nF. LT8311 V_{IN} Powered from a 12V Housekeeping Supply, Which Also Pulls Up on the $\overline{\text{PGOOD}}$ Pin Through a 100k External Resistor

Figure 12. Output Overshoot Control at Start-Up

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V_{IN} BIAS SUPPLY

The LT8311's V_{IN} pin can be powered in various ways. Place at least a 2.2µF ceramic bypass capacitor close to the pin.

Picking an appropriate bias supply to power up the LT8311 requires consideration of the following criteria:

1. The V_{IN} pin, in certain configurations, may be the only supply to the LT8311's $INTV_{CC}$ pin, which provides gate drive to the catch and forward MOSFETs. In such situations, V_{IN}'s bias supply must be high enough to provide adequate gate-drive voltage (typically 5V to 7V) for both synchronous MOSFETs.
2. V_{IN}'s bias supply must be able to source:
   a. LT8311's V_{IN} current (4.5mA typical)
   b. $INTV_{CC}$ gate-drive current when using V_{IN} to supply the $INTV_{CC}$ pin (typically 10mA to 30mA)
   c. Opto-driver source current (typically 1mA to 5mA)
3. V_{IN} start-up and short-circuit conditions:
   a. V_{IN} must come up in reasonable time to allow the LT8311 to begin synchronous and opto-coupler control. While synchronous control is shut off, the secondary-side current will flow through the body diodes of the secondary synchronous MOSFETs. While opto-control is off, the forward converter will operate open-loop, using a volt-second clamp to control V_{OUT} if operating with LT3752, LT3752-1 or LT3753 on the primary side.
   b. V_{IN} may be shorted to GND during transient events. For instance, V_{IN} powered from the output voltage, will be driven to 0V during an output short-circuit. The forward converter must be able to ride through the momentary loss of power to the LT8311, which is often easily accomplished by appropriately configuring soft-start control on the primary-side ICs. Refer to the LT3752/LT8310 data sheets for details on configuring soft-start control on the primary-side IC.

With the previous criteria in mind, there are three methods (1-3), listed below, for powering up the LT8311. For preactive mode, use method 1, 2 or 3. For SYNC mode FCM, use method 1 or 3; for DCM, use method 1, 2 or 3.

1. Power from the LT3752's housekeeping supply (see Figure 21 in the Typical Application section). Being a flyback converter rather than a LDO, the LT3752's housekeeping supply is an efficient supply source. It can be connected through an external winding to the LT8311's V_{IN} and $INTV_{CC}$ pins, and can be set high enough to provide adequate gate drive for the catch and forward MOSFETs, but low enough to minimize efficiency and thermal losses. The housekeeping supply comes up as soon as the LT3752 receives input power, so power is delivered to the LT8311 without delay.
2. Power directly from V_{OUT}. At output voltages lower than 10V, careful consideration must be given to the output voltage start-up time, ensuring that the LT8311 can turn on and provide synchronous/opto control well before the output voltage approaches regulation. It is also important to ensure, at these lower output voltages, that sufficient gate drive voltage can be provided to the external MOSFETs. At higher V_{OUT} voltages, efficiency and thermal considerations related to the IC's internal power dissipation can become important criteria. In addition, at higher V_{OUT} voltages, it is important to ensure that voltage transients on the V_{IN} pin do not exceed the pin's abs max rating of 30V.
3. Use a buck circuit from an auxiliary transformer winding, as shown in Figure 13. This circuit has the benefit of being highly efficient, and is fairly simple to design. It is particularly useful for low output voltage applications (3.3V or 5V) that do not have an external housekeeping supply, and where powering directly from the output voltage is inadequate. In this configuration, the buck circuit's output voltage derives its energy from secondary-side switching pulses that also source energy to the forward converter's main output voltage, V_{OUT}. Careful consideration must be given to ensure that the buck output voltage comes up well in time, and turns on the LT8311 to provide synchronous and opto control before the forward converter's actual output voltage gets close to regulation. If there is a need to speed up

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the time taken by the buck converter output voltage to get to its target, relative to the forward converter's main output voltage, often a simple technique is to slow down the main output voltage start-up time by increasing the soft-start capacitor on the primary-side IC.

$INTV_{CC}$ BIAS SUPPLY

The $INTV_{CC}$ pin powers the catch and forward MOSFET gate drivers of the LT8311. Two configurations exist for biasing up the $INTV_{CC}$ pin, as shown in Figure 14:

1. In the first configuration, the LT8311's on-chip LDO regulates the $INTV_{CC}$ pin voltage from the V_{IN} supply. When the V_{IN} pin voltage is low, the internal LDO will operate in drop-out, driving the $INTV_{CC}$ pin to about 400mV below the V_{IN} pin voltage. When the V_{IN} pin voltage is high, the internal LDO will regulate $INTV_{CC}$'s voltage to 7V. Ensure that V_{IN}'s supply voltage does not exceed V_{IN}'s abs max voltage of 30V. If $INTV_{CC}$ drops below its UVLO voltage (4.6V rising and 4.3V falling), all synchronous switching will be stopped. The maximum guaranteed current that the $INTV_{CC}$ LDO can source is 40mA. Ensure that the total gate charge (Q_g) current required by both secondary MOSFETs, M_{CG} and M_{FG}, is less than 40mA:

$$I_{MOSFET\_TOTAL} = f_{SW} \bullet (Q_{g\_MCG} + Q_{g\_MFG}) < 40mA$$

where f_{SW} is the converter's switching frequency, Q_{g_MCG} is the gate charge (Q_g) rating of M_{CG} and Q_{g_MFG} is the gate charge (Q_g) rating of M_{FG}.

This configuration, utilizing the LT8311's internal LDO, will suffice for most applications, limited only by thermal considerations related to the LDO's power dissipation. Keeping the power dissipation to a minimum will help lower the operating junction temperature of the LT8311, potentially allowing the system to operate over a wider ambient temperature range:

$$\text{LDO Power Dissipation} = (V_{IN} - INTV_{CC}) \bullet I_{MOSFET\_TOTAL}$$

$$\text{LT8311 Operating Junction Temperature} \approx \theta_{JA} \bullet (V_{IN} \bullet 4.5mA + \text{LDO Power Dissipation} + V_{IN} \bullet I_{OPTO}) + T_A$$

where θ_{JA} is LT8311's junction-to-ambient thermal resistance and is typically 38°C/W; I_{OPTO} is the current

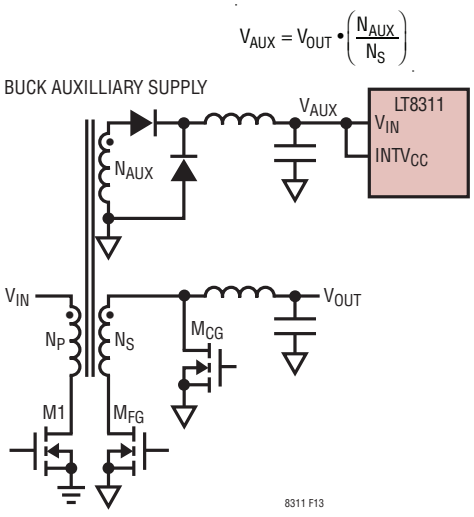

Figure 13. Buck Circuit Generates V_{AUX} Supply, Which Powers LT8311's V_{IN} and $INTV_{CC}$ Pins

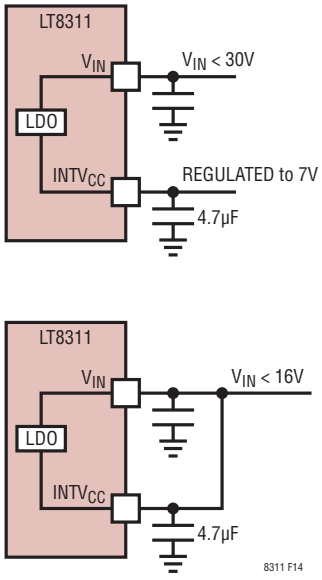

Figure 14. V_{IN} and $INTV_{CC}$ Pin Configurations

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sourced into the opto-coupler by the LT8311's OPTO pin; 4.5mA is the typical V_{IN} current of the LT8311; T_A is the ambient temperature.

2. In the second configuration, the V_{IN} pin's bias supply drives the $INTV_{CC}$ pin through a direct connection, bypassing the internal LDO. This configuration reduces power dissipation inside the IC by not having to incur any power loss within the $INTV_{CC}$ LDO. Use this optional configuration for V_{IN} voltages that are below 16V, allowing sufficient margin for $INTV_{CC}$ to stay below its OVLO(+) voltage of 16.5V. Ensure that V_{IN}, during transients, does not exceed $INTV_{CC}$'s abs max voltage of 18V.

   When an external supply or auxiliary winding is available, use this configuration (tying V_{IN} and $INTV_{CC}$ together) to deliver power to the IC. This configuration is most applicable when using the LT3752 as a primary-side IC. The LT3752's housekeeping supply can be connected to the LT8311's V_{IN} and $INTV_{CC}$ through an auxiliary winding, as shown in Figure 21 in the Typical Applications section.

$INTV_{CC}$ should be bypassed with a minimum of 4.7µF ceramic capacitor to ground for all three configurations. Place the capacitor close to the $INTV_{CC}$ pin, ensuring that the ground terminal of the capacitor has the shortest possible return path to the LT8311's ground (exposed pad).

LT8311 OPTO CONTROL FUNDAMENTALS

Setting Output Voltage

Figure 15 shows how to program the forward converter's output voltage with a resistor divider feedback network. Connect the top of R_{FB1} to V_{OUT}, the tap point of R_{FB1}/R_{FB2} to the FB pin, and the bottom of R_{FB2} to ground. The ground return of R_{FB2} must be kept as close as possible to the ground of the LT8311, and must be kept away from the forward converter's power path. The power path contains switching currents, and possibly large value currents (depending upon the load) which may introduce unintended noise, or I • R drops into the FB resistor divider path. The FB pin regulates to 1.227V and has a typical input pin bias current of 120nA flowing out of the pin. The output voltage is set by the formula:

$$V_{OUT} = 1.227 \bullet \left(1 + \frac{R_{FB1}}{R_{FB2}}\right) - 120nA \bullet R_{FB1}$$

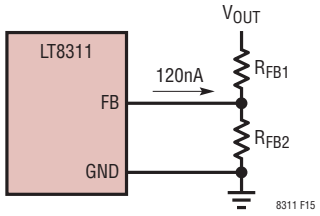

Figure 15. Setting Output Voltage of Forward Converter

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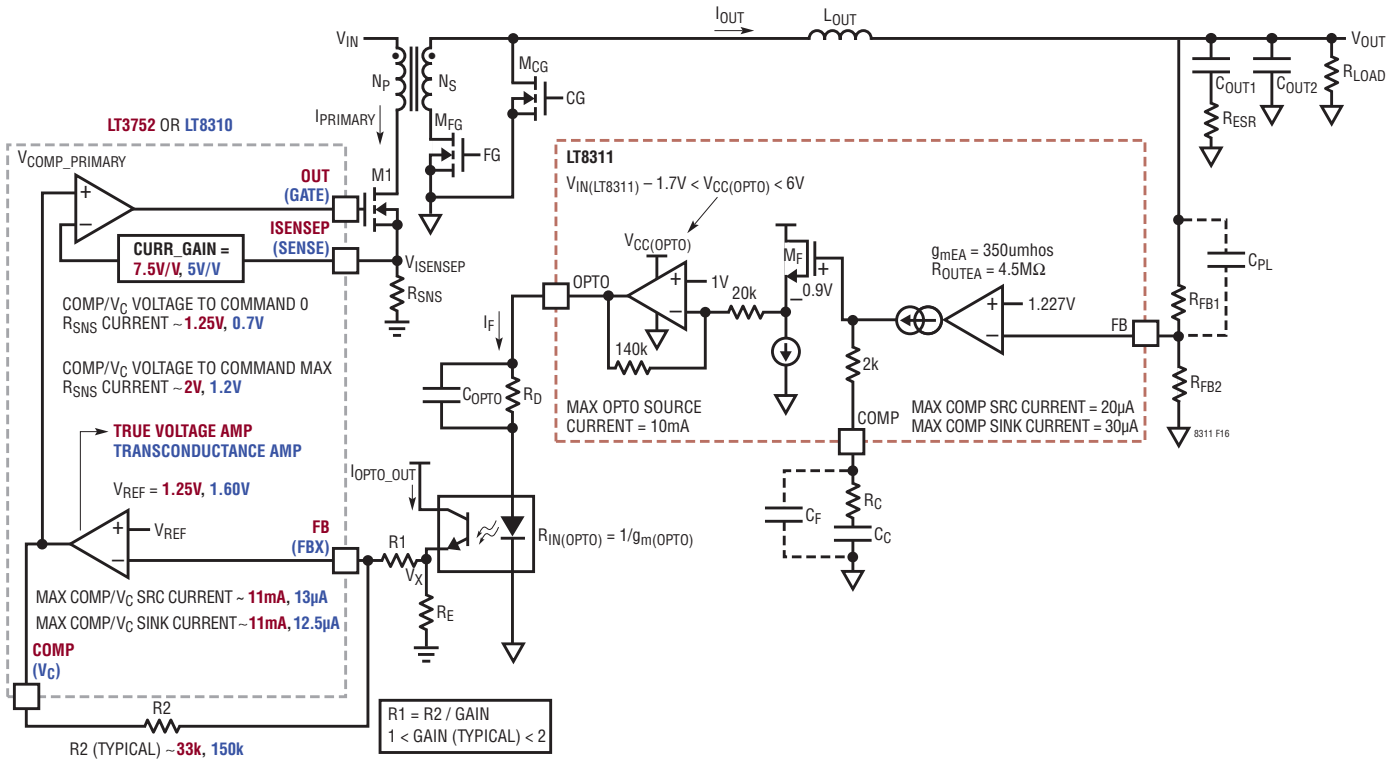

Figure 16. Forward Converter Voltage Feedback Loop with LT8311 on Secondary Side and LT3752 (or) LT8310 on Primary Side

Picking Loop Compensation Components

Figure 16 shows a typical loop associated with a forward converter, using the LT8311 on the secondary side, and the LT3752 or LT8310 as the primary-side ICs. Parametric values specific to the LT3752 are shown in red, while those specific to the LT8310 are shown in blue. The forward converter loop shown is a peak current mode control system.

The optimum values for loop compensation depend on the IC used on the primary side and the LT8311, as well as the operating conditions of the converter (input voltage range, output voltage, load current, etc.). To compensate the voltage feedback loop around the LT8311, a series resistor/capacitor network is usually connected from the LT8311's COMP pin to GND. For most applications, the capacitor C_C should be in the range of 4.7nF to 47nF, and the resistor R_C should be in the range of 2k to 20k. If the R_C value is too large, the part will be more susceptible to high frequency noise and jitter. If the R_C value is too small, the transient performance will suffer. The value choice for C_C is somewhat the inverse of the R_C choice: if too small a C_C value is used, the loop may be unstable and if too large a C_C value is used, the transient performance may suffer. A small capacitor, C_F, is often connected in parallel with the RC compensation network to attenuate the COMP pin voltage ripple induced from the output voltage ripple (through the internal error amplifier). The C_F capacitor usually ranges in value from 10pF to 100pF. For certain applications, a phase-lead zero capacitor C_{PL} (in parallel with R_{FB1} resistor), or a pole-zero pair (C_{OPTO} and R_D) on the OPTO pin may help improve the transient performance of the loop. A practical approach to design the compensation network is to start with one of the circuits in this data sheet that is similar to your application, and tune the compensation network to optimize the performance. Stability should then be checked across all operating conditions, including load current, input voltage range and temperature.

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Picking the Opto-Coupler

The voltage feedback loop, explained earlier, uses an opto-coupler to convey output voltage information from the secondary side to the primary side (see Figure 17). An opto-coupler is used because of its wide prevalence, relatively low cost, and its ability to convey DC signal information over an isolation boundary with potential differences of up to 5000V.

The input of an opto-coupler typically consists of an infrared light-emitting diode (LED), while the output is typically a phototransistor. Current flowing into the opto-coupler's input LED, called I_F, causes photons to be emitted. These photons cross the opto-coupler's isolation barrier and get collected in the base of the output phototransistor. This photo current, which essentially forms the phototransistor's base current, is gained up by the phototransistor's ß (current gain) before flowing out of the opto-coupler, and is called I_{OPTO_OUT}. The key parameter of interest in an opto-coupler is the current transfer ratio (CTR). CTR is typically expressed in units of %, and is calculated as follows:

$$CTR(\%) = \frac{I_{OPTO\_OUT}}{I_F}$$

where I_{OPTO_OUT} is the output current of the opto-coupler and I_F is the opto-coupler's input LED current

Opto-couplers have historically been disliked, and justifiably so, for having CTRs that degrade with operating lifetime, at higher operating temperatures, and at higher input currents (I_F). Much of this CTR degradation comes from a reduction in the quantum efficiency of the input LED, which is a function of the LED's operating current (I_F), operating temperature and operating lifetime.

Fortunately, LED technology has matured over the last couple of decades, and has allowed improvements in opto-coupler performance, a discussion of which is beyond the scope of this data sheet. Avago Technologies has published documentation showing 3-sigma CTR degradation of no more than 10% over 30 field years of operation for their opto-couplers manufactured with AlGaAs type LEDs running 5mA of input current (I_F) at 100% duty cycle, and at 85°C ambient temperature.

Please refer to the application/design notes from opto-coupler vendors such as Avago Technologies, CEL and Vishay, to procure further information on opto-couplers. A typically recommended opto-coupler is the PS2801 from California Eastern Laboratories (CEL).

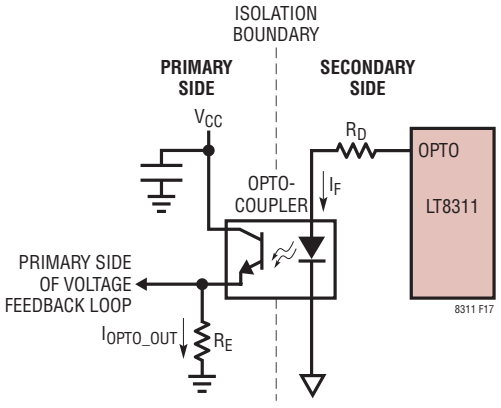

Figure 17. Typical Opto-Coupler Configuration in a Voltage Feedback Loop

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Opto-Coupler Design Guidance

An opto-coupler's CTR degradation affects a forward converter's voltage feedback loop in two ways:

1. **Large Signal Effect:** A drop in CTR means that to sustain the same output current from the opto-coupler, the input current of the opto-coupler will have to increase. The input current of the opto-coupler is sourced by the LT8311's OPTO pin. The opto-feedback loop should be designed such that, at the lowest CTR possible, the LT8311's OPTO pin is not current limited. The maximum current that the LT8311's internal opto-driver can source out of the OPTO pin is 10mA. Design the system so that, nominally, the OPTO pin is sourcing 2mA to 3mA maximum current into the opto-coupler's input.
2. **Small Signal Effect:** A reduction in CTR by 2x will cause the DC gain and crossover frequency of the forward converter's voltage feedback loop to drop by 2x, assuming all other parameters are constant. Likewise, an increase in CTR by 2x, assuming no change in other parameters, will cause the DC gain and the crossover frequency of the voltage feedback loop to increase by 2x. The voltage feedback loop must be designed ensuring that at $CTR_{(MAX)}$ (maximum CTR of the opto-coupler), the crossover frequency of the feedback loop stays well within the Nyquist frequency of the system (= switching frequency/2). A good rule of thumb is to design the voltage feedback loop's crossover at about 1/10 of the switching frequency for an opto-coupler at the nominal value of CTR.

As explained earlier, improvements in opto-coupler technology have allowed CTR changes over the operating lifetime of an opto-coupler to become significantly smaller and well controlled. However, the more challenging design aspect of an opto-coupler is the absolute variation in its CTR over a large sample size and operating temperature range. It is this spread in CTR that must be accounted for when designing an opto-coupler based voltage feedback loop. Picking an opto-coupler whose CTR variation is no more than 2x its nominal value, is typically a good starting point (see Table 1 for a list of opto-couplers with small CTR spreads at room temperature).

The following guidelines help calculate initial values for the input and output resistors of the opto-coupler (R_D and R_E, respectively) for a generic application. The final values for R_D and R_E should be determined after bread-boarding a system. Use Figure 16 as a reference when reading the following guidelines:

Step 1: Pick resistors, R1 and R2, that set the inverting gain of the primary-side IC's error amplifier. A typical starting value for R1 would be 22k on the LT3752, and 100k on the LT8310. A typical starting value for R2 would be 33k on the LT3752, and 150k on the LT8310.

Step 2: Calculate the maximum voltage required at the emitter of the opto-coupler's output transistor (V_{X_MAX}) to drive the primary-side IC's COMP or V_C pin to the voltage needed to command zero inductor current (referred to as V_{C_LOW} in the following equation):

$$V_{X\_MAX} = V_{REF}\left[1+\frac{R1}{R2}\right] - V_{C\_LOW} \bullet \frac{R1}{R2}$$

V_{C_LOW} is approximately 0.7V for the LT8310, and 1.25V for the LT3752. V_{REF} is 1.6V for the LT8310 and 1.25V for the LT3752.

Step 3: Pick a maximum opto-coupler output current ($I_{OPTO\_OUT\_HIGH}$) in the range of 1mA to 10mA. A typical choice for $I_{OPTO\_OUT\_HIGH}$ might be 2.5mA. Now calculate R_E to be:

$$R_E = \frac{V_{X-MAX}}{I_{OPTO\_OUT\_HIGH}}$$

Step 4: Estimate the maximum input current (I_{F_HIGH}) needed to be sourced into opto-coupler by the LT8311's OPTO pin, at the opto-coupler's minimum CTR (CTR_{MIN}):

$$I_{F\_HIGH} = \frac{I_{OPTO\_OUT\_HIGH}}{CTR_{MIN}}$$

Ensure that I_{F_HIGH} is well within the 10mA limit that the LT8311's OPTO pin can source.

Step 5: Estimate the R_D value needed for the OPTO pin to source the I_{F_HIGH} current at the maximum OPTO pin

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voltage ($V_{OPTO(MAX)}$). The opto-coupler's input LED has a turn-on voltage of 1.2V:

$$R_D = \frac{V_{OPTO(MAX)} - 1.2V - 0.5V}{I_{F\_HIGH}}$$

The extra 0.5V in the equation is margin to account for the OPTO pin's linear range. The maximum OPTO pin voltage is 6V (minimum guaranteed), when the LT8311's V_{IN} pin is at 8V or higher. At lower V_{IN} pin voltages, V_{OPTO_MAX} is V_{IN} – 1.7V.

The previous equations show how R_D and R_E ought to be calculated for large signal characteristics of an opto-coupler-based voltage feedback loop. The final values chosen for R_D and R_E may need to be tweaked from the values calculated here to achieve a satisfactory compromise between the large and small signal characteristics of the voltage feedback loop.

Picking Soft-Start Capacitor (C_{SS}) for Output Soft-Start

The Operation section explained how the LT8311's SS pin helps with output soft-start at start-up, with output overshoot control during short-circuit recovery, and to prebias the voltage feedback loop during start-up of the LT8311's opto-control scheme. The soft-start capacitor, C_{SS}, is charged by the LT8311's internally trimmed 10µA current source at start-up. Since the FB pin voltage tracks the SS pin voltage when the voltage on SS is below 1.227V, setting the SS pin's slew rate will set the FB pin's slew rate, setting the time taken by the output to come up to its regulation voltage. It is important to recognize that the tracking between the SS pin's slew rate and the FB's pin slew rate is only valid as long as the LT8311's soft-start of output voltage is slower than the primary-side IC's soft-start of output voltage, as explained in the Operation section. By observing this criteria, the following equation applies:

$$\frac{\partial V_{OUT}}{\partial t} = \frac{\partial V_{FB}}{\partial t} = \frac{10\mu A}{C_{SS}}$$

where C_{SS} is the capacitor from the LT8311's SS pin to GND, V_{OUT} is the output voltage of the forward converter, and V_{FB} is the LT8311's FB pin voltage.

In steady state, the SS pin voltage is clamped to a maximum of 2V by an internal clamp.

LT8311 SYNCHRONOUS CONTROL FUNDAMENTALS

Catch and Forward MOSFET Selection

When selecting the secondary-side synchronous MOSFETs, it is important to choose the following parameters carefully to ensure robust operation of the system: maximum drain-source voltage, maximum drain-source current and maximum gate-source voltage. Furthermore, to maximize system efficiency, it is important to lower power dissipation in the MOSFETs by minimizing their on-resistance ($R_{DS(ON)}$) and gate charge (Q_g). Please use the following guidelines to choose appropriate catch and forward MOSFETs for a specific application:

1. Maximum V_{DS} Rating

The maximum voltage seen on the drain of the catch MOSFET is a function of the maximum input voltage ($V_{IN(MAX)}$) of the system, and the transformer turns ratio (N_S/N_P).

$$\text{Catch MOSFET } V_{DS(MAX)} = V_{IN(MAX)} \bullet \frac{N_S}{N_P} \bullet \text{Margin}$$

where Margin is a number from 1 to 3 (typically 1.5 to 2), allowing a certain safety margin in the catch MOSFET's $V_{DS(MAX)}$ equation. This will account for voltage spikes associated with the leakage inductance of the transformer's secondary winding. Using a snubber on the drain of the catch MOSFET will minimize leakage inductance spikes and allow Margin to approach the lower end of its range.

The maximum voltage seen on the drain of the forward MOSFET is a function of the reset mechanism used on the primary side of the forward converter to reset the transformer's magnetic flux.

When using active clamp reset:

$$\text{Forward MOSFET } V_{DS(MAX)} \approx \frac{V_{OUT}}{1 - \frac{V_{OUT}}{V_{IN(MIN)} \bullet \frac{N_S}{N_P}}}$$

where $V_{IN(MIN)}$ is the minimum input voltage of the system, and V_{OUT} is the forward converter's output voltage. Note that this equation for the forward MOSFET's $V_{DS(MAX)}$ assumes that the primary side's active clamp capacitor (C_{CL}) is large enough to be treated as a voltage source.

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In reality, the drain voltage of the forward MOSFET will have some "bowing" over and above the voltage calculated here, associated with the energy shuttled between L_{MAG} and C_{CL} during the reset process. For most applications, this bowing can be accounted for by adding a 20% safety margin on the forward MOSFET's $V_{DS(MAX)}$ equation.

When using resonant reset:

$$\text{Forward MOSFET } V_{DS(MAX)} \approx \frac{V_{OUT}}{f_{SW} \bullet 2 \bullet \sqrt{L_{MAG} \bullet C_{RST}}}$$

where f_{SW} is the forward converter's switching frequency, L_{MAG} is the magnetizing inductance of the transformer's primary winding, and C_{RST} is the resonant reset capacitor used on the primary side.

Unlike the catch MOSFET, the $V_{DS(MAX)}$ equation of the forward MOSFET typically does not need to account for leakage inductance voltage spikes. This is because the turn-on and turn-off events of the forward MOSFET, typically, do not involve the forward MOSFET's drain having to dissipate large amounts of stored leakage inductance energy.

2. Maximum I_{DS} Rating

Most power MOSFET data sheets have a rating for continuous-drain current, and pulse-drain current. Continuous-drain current is the RMS drain current of the catch and forward MOSFET, which is a function of the inductor current, and the duty cycle at which the forward converter is operating. Pulse-drain current is the instantaneous maximum drain current seen by the MOSFETs, and is typically the peak of the inductor current waveform.

Prior to calculating the maximum continuous-drain current, it is useful to calculate the minimum, maximum and average duty cycles of the forward converter:

$$D_{MIN} = \frac{V_{OUT}}{V_{IN(MAX)} \bullet \left(\frac{N_S}{N_P}\right)}$$

$$D_{MAX} = \frac{V_{OUT}}{V_{IN(MIN)} \bullet \left(\frac{N_S}{N_P}\right)}$$

$$D_{AVG} = \frac{D_{MAX} + D_{MIN}}{2}$$

where $V_{IN(MAX)}$ and $V_{IN(MIN)}$ are the maximum and minimum input voltages of the forward converter.

The catch MOSFET's maximum continuous drain current, I_{CAT_RMS}, can be calculated as:

$$I_{CAT\_RMS} = \sqrt{(1 - D_{MIN}) \bullet \left(I_{LOAD(MAX)}{}^2 + \frac{I_{RIPP(P-P)}{}^2}{12} \right)}$$

where D_{MIN} is the minimum duty cycle of the forward converter, $I_{LOAD(MAX)}$ is the maximum output load current of the forward converter, and $I_{RIPP(P-P)}$ is the peak-to-peak ripple current in the output inductor. $I_{RIPP(P-P)}$ is calculated as follows:

$$I_{RIPP(P-P)} = V_{OUT} \bullet \frac{1 - D_{AVG}}{f_{SW} \bullet L_{OUT}}$$

where D_{AVG} is the average duty cycle of the forward converter, f_{SW} is the converter's switching frequency, and L_{OUT} is the output inductance value.

The forward MOSFET's maximum continuous-drain current (I_{FWD_RMS}) is:

$$I_{FWD\_RMS} = \sqrt{D_{MAX} \bullet \left(I_{LOAD(MAX)}{}^2 + \frac{I_{RIPP(P-P)}{}^2}{12} \right)}$$

Both, the forward and catch MOSFET should have a peak pulse current rating that is higher than the highest possible peak of the inductor current. This highest possible peak occurs at the maximum load current, and is equal to:

$$I_{LOAD(MAX)} + \frac{I_{RIPP(P-P)}}{2}$$

3. Maximum V_{GS} Rating

As explained earlier in the $INTV_{CC}$ Bias Supply section, $INTV_{CC}$ is regulated internally to 7V by the LT8311. By extension, the catch and forward MOSFET gates can be driven as high as 7V when using the LT8311's internal LDO to regulate $INTV_{CC}$. For applications using the LT8311's internal LDO, picking a maximum V_{GS} greater than 10V should suffice.

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Alternatively, the $INTV_{CC}$ pin can be overdriven externally up to 16V. For such applications, picking MOSFETs with a maximum V_{GS} of ±20V should suffice.

4. Calculating MOSFET Losses Due to $R_{DS(ON)}$

The conduction/ohmic loss associated with the catch and forward MOSFET is a function of the MOSFET's RMS current and its on-resistance. For the vast majority of forward converter applications, which typically have high maximum load currents on the output (5A or higher), minimizing losses associated with the MOSFET's $R_{DS(ON)}$ will be far more critical than minimizing losses associated with the MOSFET's gate charge.

$$\text{Catch MOSFET Ohmic Loss} = (I_{CAT\_RMS})^2 \bullet R_{CAT}$$

where R_{CAT} is the on-resistance ($R_{DS(ON)}$) of the catch MOSFET.

$$\text{Forward MOSFET Ohmic Loss} = (I_{FWD\_RMS})^2 \bullet R_{FWD}$$

where R_{FWD} is the on-resistance ($R_{DS(ON)}$) of the forward MOSFET.

5. Calculating Q_g Based Loss

There are two aspects to the gate charge (Q_g) based loss associated with the secondary synchronous MOSFETs:

A. Q_g Based MOSFET Switching Loss:

The catch MOSFET's turn-on and turn-off timings, regardless of preactive or SYNC mode, are ZVS (zero voltage switching) events. The catch MOSFET turns on after the inductor current is already flowing through its body diode. Similarly, when the catch MOSFET turns off, the inductor current subsequently flows through its body diode. As a result, the voltage across the drain-source terminals of the catch MOSFET is small during switching events, resulting in the catch MOSFET having insignificant switching loss.

The forward MOSFET's turn-on and turn-off timings, regardless of preactive or SYNC mode, are ZVS (zero voltage switching) and ZCS (zero current switching) events, respectively. The forward MOSFET turns on after transformer reset is complete. Transformer reset completion is marked by the transformer's magnetizing current flowing through the forward MOSFET's body diode, which allows the forward MOSFET to turn on with a small drain-to-source voltage across it. Similarly, the forward MOSFET typically turns off after the primary-side MOSFET has turned off. When the primary-side MOSFET turns off, the only current flowing through the forward MOSFET is the transformer magnetizing current, which for all intents and purposes, can be assumed to be zero. Consequently, the forward MOSFET has insignificant switching losses.

B. Q_g Based Converter Power Loss:

As explained earlier in the $INTV_{CC}$ Bias Supply section, there is a power loss incurred in turning on/off the catch and forward MOSFETs, associated with supplying gate charge (Q_g) to the gates of these MOSFETs. This charge is supplied either by the supply voltage connected to the LT8311's V_{IN} pin, when using the internal LDO to regulate $INTV_{CC}$, or by the supply voltage connected to the LT8311's $INTV_{CC}$ pin, when driving the $INTV_{CC}$ pin externally. In either case, the total loss associated with supplying the gate charge is:

$$\text{Power Loss} = V_{SUPP} \bullet (Q_{gCAT} + Q_{gFWD}) \bullet f_{SW}$$

where V_{SUPP} is the supply voltage connected to the LT8311's V_{IN} pin when $INTV_{CC}$ is internally regulated. Alternatively V_{SUPP} is the supply voltage connected to the LT8311's $INTV_{CC}$ pin when $INTV_{CC}$ is externally driven. Q_{gCAT} and Q_{gFWD} is the gate charge (Q_g) of the catch and forward MOSFETs, respectively. f_{SW} is the forward converter's switching frequency.

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Setting R_{TIMER} in Preactive Mode

In preactive mode, the TIMER pin resistor, R_{TIMER}, programs the maximum period that can elapse between two CSW rising edges before a timeout period is triggered. Timeout allows the LT8311 to stop all synchronous activity in the event that the primary-side IC stops switching. Since CSW rising edges represent primary-side switching activity, timeout of CSW rising edges is interpreted as stoppage of switching—at which point the LT8311 ceases all secondary-side synchronous switching, and starts its evaluation period. Refer to the Operation section for details on the evaluation period. Secondary-side switching resumes when all conditions within the evaluation period are satisfied. Timeout also ensures that switching activity within preactive mode occurs at a frequency that is within preactive mode's operating frequency range.

As shown in Figure 18, every time the CSW pin voltage is detected to rise past 1.2V from a voltage level below –150mV, the LT8311 resets its internal timeout signal. The gate of the catch MOSFET, CG turns on (after some propagation delay) when CSW is detected to fall below –150mV. Upon CG going high, the catch MOSFET turns on and pulls its drain voltage (CSW) close to its source voltage, which is tied to GND. CG turns off predictively in CCM before an anticipated CSW rising edge. If a CSW rising edge (rising from below –150mV to above 1.2V) does not come along in time to reset the timeout signal, the signal eventually charges up to voltage $V_{REF\_TIMEOUT}$ and triggers an internal timeout condition. Consequently, the LT8311 shuts down all synchronous conduction and starts the evaluation period. The evaluation period ends only when the four conditions listed in the Operation section, including the timely reset of the internal timeout signal, are satisfied for three consecutive CSW rising edges. Upon completion of the evaluation period, the LT8311 restarts synchronous control.

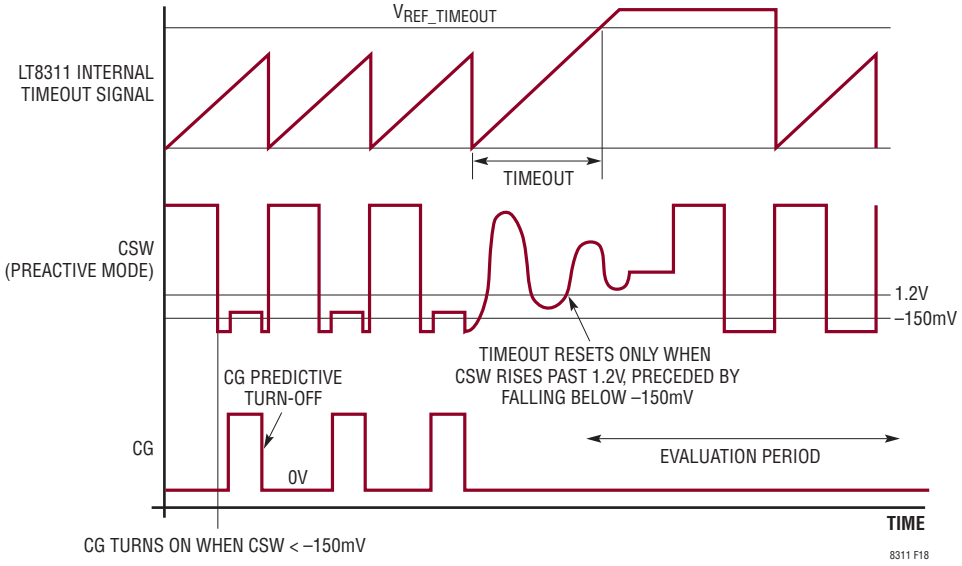

Figure 18. If Timeout Is Triggered in Preactive Mode, LT8311 Shuts Down All Synchronous Conduction and Starts the Evaluation Period (Note: CSW's ringing waveform is caused by the inductor current getting to 0A.)

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The TIMER resistor is typically picked to set a timeout period that is 20% higher than the forward converter's nominal switching period.

$$\text{Timeout} = \frac{1.20}{f_{SW}}$$

where f_{SW} is converter switching frequency in Hz.

Once a timeout period is calculated, the TIMER pin resistor, R_{TIMER}, can be calculated as follows:

$$R_{TIMER}\ (k\Omega) \sim 22.1E6 \bullet \text{Timeout}$$

where Timeout has units of seconds.

The relationship between R_{TIMER} and timeout is not perfectly linear. Table 1 shows R_{TIMER} values (nearest 1%) for a range of typical forward converter switching frequencies:

Table 1. R_{TIMER} 1% Resistor Values for Different Forward Converter Switching Frequencies

SWITCHING FREQUENCY (kHz)	TIMEOUT (µs) = 1.2/f_{SW}	R_{TIMER} (kΩ)
100	12	267
150	8	178
200	6	133
250	4.8	107
300	4	88.7
400	3	66.5
500	2.4	53.6

Setting the timeout period at 1.2 • Switching Period will keep synchronous conduction shut off through frequency foldback in preactive mode, until the switching frequency approaches 80% of its final value. For 100kHz switching applications, this means that the LT8311 is ready for synchronous conduction in preactive mode, at 80kHz. Although 80kHz is outside the LT8311's data sheet specifications for preactive mode operating frequency range, the IC is designed to operate down to 80kHz to ride through such a frequency foldback event. Timeout may also shut off synchronous conduction during CSW pulse-skipping events at light output load currents.

Setting R_{TIMER} in SYNC Mode

In SYNC mode, the functionality of the timeout period is similar to preactive mode, except that the resetting of the LT8311's internal timeout signal happens every time the SYNC pin voltage falls below –1.2V. The goal of the timeout function in SYNC mode is primarily to limit the catch MOSFET on-time in the event that the catch MOSFET stays on too long and conducts an unsafe level of reverse-output inductor current (current flows from the output capacitor back towards the drain of the catch MOSFET). Refer to the section, "Configuring CSP/CSN Inputs of the Current Sense Comparators in SYNC Mode," for further information on what constitutes an unsafe level of reverse-output inductor current.

In SYNC mode, set the timeout period to be 20% longer than the longest switching period of the primary-side IC. Typically, the longest switching period of the primary-side IC corresponds to the smallest frequency foldback frequency ($f_{SW\_SMALLEST}$):

$$\text{Timeout} = \frac{1.2}{f_{SW\_SMALLEST}}$$

Once a timeout period is calculated, the TIMER pin resistor, R_{TIMER}, can be calculated as follows:

$$R_{TIMER}(k\Omega) \sim 22.1E6 \bullet \text{Timeout}$$

where Timeout has units of seconds, and $f_{SW\_SMALLEST}$ is in units of Hz.

Configuring CSP/CSN Inputs of Current Sense Comparator in Preactive Mode

The differential input current sense comparator in the LT8311 is used to provide the IC with information about the current in the catch MOSFET. Connect the CSP and CSN pins, through series resistors, to the drain and source of the catch MOSFET (M_{CG}), to allow the LT8311 to sense the drain-source voltage of M_{CG}, and make inferences about its current. Alternatively, CSP and CSN can be tied, through series resistors, across a sense resistor which is placed from the source of M_{CG} to ground. As explained earlier in the Operation section, the CSP and CSN pins should be configured, in preactive mode, to trip at zero current in the catch MOSFET. Since the current comparator internally trips at 66mV, and the CSP pin sources 40µA,

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placing 1%, 1.65k resistors in series with CSP and CSN should allow the LT8311 to trip with approximately zero volts across the catch MOSFET. Note that the current comparator has a propagation delay of 100ns nominally, so the time taken from the current comparator getting tripped to the catch MOSFET turning off is about 100ns. During this 100ns, the current in the output inductor can reverse and flow from the drain-to-source of the catch MOSFET. If negative current flow in M_{CG} is not desired, the CSP pin series resistor can be chosen to trip at a positive value of source-to-drain catch MOSFET current. The following equation allows calculation of the resistor (R_{CSP}) to be placed in series with the CSP pin for a desired value of catch MOSFET trip current (I_{TRIP}):

$$R_{CSP} = \frac{66mV - I_{TRIP} \bullet R_{SNS}}{40\mu A}$$

where R_{SNS} is the $R_{DS(ON)}$ of the catch MOSFET when the CSP and CSN pins are connected directly across the drain-source terminals of the catch MOSFET. Alternatively, R_{SNS} is the sense resistor in the source of the catch MOSFET if the CSP/CSN pins are connected directly across the sense resistor. Once the resistor in series with the CSP pin (R_{CSP}) is decided, place an identical resistor in series with the CSN pin.

Configuring CSP/CSN Inputs of the Current Sense Comparator in SYNC Mode

The LT8311 is typically operated in SYNC mode when the forward converter needs to be operated in FCM (forced continuous mode). In SYNC mode, the LT8311 receives synchronous control signals on its SYNC pin, through a pulse transformer, from the primary-side IC's S_{OUT} pin. Connecting the LT8311's CSP/CSN pins across the catch MOSFET's drain and source, in SYNC mode, is done to protect the catch MOSFET from conducting too large a reverse inductor current at light load.

The following guidelines offered (Steps 1 to 5) may be used to determine an appropriate catch MOSFET reverse current trip point (V_{TRIP}):

Step 1: Determine the worst-case negative inductor current value during regular FCM operation, which will likely happen at the smallest frequency foldback frequency, highest V_{IN}, and at 0A load. An easy way to determine this is to run the forward converter with the LT8311 working in SYNC mode and keeping the CSP/CSN pins shorted to GND. Observing the inductor current waveform on an oscilloscope at start-up, with V_{IN} at its maximum value, and the load at 0A, can quickly give the user an idea of the worst-case negative inductor current value (I_{CATCH_FET}) during regular start-up operation. This will set a lower bound on the CSP/CSN trip point (V_{TRIP} minimum):

$$V_{TRIP}\ \text{Minimum} = |I_{CATCH\_FET}| \bullet R_{DS(ON)}$$

where $R_{DS(ON)}$ is the on-resistance of the catch MOSFET, and I_{CATCH_FET} is the worst-case magnitude of negative inductor current (current flowing from drain to source of catch MOSFET) during FCM operation at startup.

Step 2: Pick a trip point (V_{TRIP}) that allows some margin from the value calculated in Step 1. Typical margin might be 20%, thereby setting a trip point of:

$$V_{TRIP} = 1.2 \bullet V_{TRIP}\ \text{Minimum}$$

Step 3: Determine the selected catch MOSFET's single pulse avalanche energy rating (E_{AS} in mJ) from the MOSFET's data sheet and its drain-source break down voltage ($V_{BR(DSS)}$ in V).

Step 4: Make sure that the chosen CSP/CSN trip voltage does not allow so much negative current in the catch MOSFET, such that when the catch MOSFET turns off, its avalanche energy rating (based on the following equation) is violated:

$$V_{TRIP}\ (\text{in Volts}) < R_{DS(ON)} \bullet \sqrt{\left[2 \bullet E_{AS} \bullet \frac{(1.3 \bullet V_{BR(DSS)} - V_{OUT})}{(1.3 \bullet V_{BR(DSS)} \bullet L_{OUT})}\right]}$$

where,

E_{AS} (Joules) = Catch MOSFET's single-pulse avalanche energy rating.

$V_{BR(DSS)}$ (V) = Catch MOSFET's drain-source break down voltage rating.

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$R_{DS(ON)}$ (Ω) = Catch MOSFET's on-resistance rating from the MOSFET's data sheet.

V_{OUT} (V) = Forward converter's output voltage in steady-state.

L_{OUT} (H) = Output inductor.

If the V_{TRIP} voltage is too large, causing the catch MOSFET's avalanche energy rating to be violated, then go back to Steps 1 and 2, or pick a different MOSFET, until the avalanche energy experienced by the MOSFET in the application is within its data sheet specified SOA.

Step 5: Upon selecting the appropriate trip point, the series resistors, R_{CSP} and R_{CSN}, may be determined based on the following equation:

$$R_{CSP} = R_{CSN} = \frac{66mV - V_{TRIP}}{40\mu A}$$

Connect R_{CSP} between the CSP pin and the catch MOSFET's drain, and R_{CSN} between the CSN pin and the catch MOSFET's source.

PREACTIVE MODE SYNCHRONOUS CONTROL

Preactive Mode General Guidelines

The following guidelines are meant to summarize the connections and operating conditions typically needed to set up the LT8311's synchronous control in preactive mode. While these guidelines are meant to serve as a starting point, they are not a substitute for bench evaluation. Ultimately, each application that uses the LT8311's preactive mode scheme must be evaluated for its specific requirements, and the IC must be configured accordingly.

1. Bias up V_{IN} and $INTV_{CC}$ as per data sheet recommendations.
2. Place a minimum of 2.2µF ceramic capacitor from the V_{IN} pin to GND.
3. Place a minimum of 4.7µF ceramic capacitor from the $INTV_{CC}$ pin to GND.
4. Tie the $\overline{PMODE}$ and SYNC pins to 0V.
5. Configure R_{TIMER} to set a timeout period that is 20% higher than the steady-state switching period of the forward converter.
6. Connect the CSW and FSW pins, through 2k ceramic resistors, to the drains of the catch and forward MOSFET, respectively. Keep the connection as short in length as possible.
7. Connect the CSP and CSN pins, each through a 1.65k resistor, directly across the drain-source terminals of the catch MOSFET for V_{DS} sensing. A small 10pF filter capacitor may be required across the CSP and CSN pins to filter out external noise that couples in.
8. Connect CG and FG to the gates of the catch and forward MOSFET, respectively, with connections that are as short as possible.

Once synchronous control is up and running:

9. Ensure that the voltage at the CSW and FSW pins does not exceed the abs max rating of 150V. If the CSW or FSW pin voltage exceeds 150V, you may need to use a RC snubber on the drain of the catch and/or the forward MOSFET.
10. If the catch MOSFET current trip point is causing the inductor current to reverse (flowing from output back to the drain of the catch MOSFET) at light loads, reconfigure the CSP/CSN trip point to trip at a slightly positive value of source-to-drain current in the catch MOSFET. This typically involves increasing the CSP and CSN series resistors to a value greater than 1.65k.
11. If the catch MOSFET's current trip point does not seem consistent, and the catch MOSFET's turn-off edge seems to show jitter at the trip current, the filter capacitor across the CSP and CSN pins may need to be adjusted.

Note that typically, the FB pin will be connected through a resistor divider network to the output voltage, when using the LT8311 as part of a voltage feedback loop.

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SYNC MODE SYNCHRONOUS CONTROL

Picking the Pulse Transformer and High Pass Filter

In SYNC Mode, the LT8311 determines the turn-on/off timings of the catch and forward MOSFETs based on voltage signals on its SYNC pin. Figure 7 in the Operation section shows a typical circuit used to communicate synchronous control signals from the primary-side IC's S_{OUT} pin to the LT8311's SYNC pin. This circuit utilizes a pulse transformer (T2 in Figure 7) to provide isolation between the primary and secondary sides, and a high pass filter (R_{SYNC} and C_{SYNC}). C_{SYNC} blocks DC signals from being applied directly to T2. Eliminating the DC component of the S_{OUT} signal, through the highpass filter (R_{SYNC} and C_{SYNC}), allows the SYNC pin signal to go positive or negative at the rising and falling edges of S_{OUT}, as shown in Figure 19. Positive and negative signals of equal magnitudes and duration allow equal positive and negative volt-seconds to be maintained on transformer T2, preventing any net magnetizing current build-up.

Appropriate values of R_{SYNC} and C_{SYNC} must be chosen to satisfy all of the following criteria:

1. The $R_{SYNC} \bullet C_{SYNC}$ time constant must be large enough to allow a sufficiently long pulse width to be generated on the SYNC pin with sufficient overdrive voltage. This is shown in Figure 19 where t1 must be at least 50ns at a SYNC voltage of ±2V (or greater over drive) to trip the SYNC comparators. Using this constraint, the equation below sets a limit on the minimum $R_{SYNC} \bullet C_{SYNC}$ product required:

$$R_{SYNC} \bullet C_{SYNC} \geq \frac{50ns}{\left[-1 \bullet \ell n\left(\frac{2V}{V_{MAX}}\right)\right]}$$

where V_{MAX} is the maximum S_{OUT} voltage, as shown in Figure 19.

2. R_{SYNC} must be small enough to ensure that the SYNC signal is sufficiently damped. An underdamped SYNC signal can cause ringing large enough to cause false triggering of the SYNC detection comparators, which may lead to improper secondary-synchronous control. The equation used to calculate R_{SYNC} for optimal damping is given by:

$$R_{SYNC} \leq \left(\frac{1}{2 \bullet \zeta}\right) \bullet \sqrt{\frac{L_m}{C_{SYNC}}}$$

where ζ is the damping factor and should typically be chosen to be about 1. L_m is the magnetizing inductance of the pulse transformer's primary winding.

Choosing L_m to be larger allows the damping factor to increase, so it would be wise to choose a pulse transformer with a larger primary winding inductance to increase the damping of the SYNC signal.

Smaller R_{SYNC} values also reduce the sensitivity of the highpass filter to stray signals (parasitic magnetic fields) that may couple in.

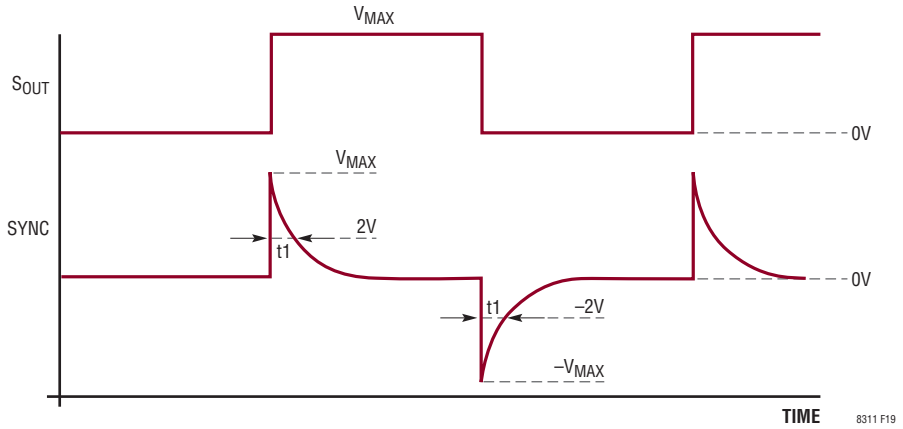


Figure 19. Positive and Negative SYNC Edges Are Generated on the Rising and Falling Edges of S_{OUT}, Respectively. The LT8311 Requires Pulse Width Time, t1, to Be at Least 50ns (Typical) with the SYNC Pin Voltage at ±2V (or Greater Overdrive) to Trigger the Internal SYNC Detect Comparators.

APPLICATIONS INFORMATION

3. R_{SYNC} must be large enough to limit the amount of source/sink current required each time a positive or negative SYNC pin voltage signal is generated. The S_{OUT} pin's gate drivers offer limited source current capability; R_{SYNC} must be large enough to ensure that this constraint in current-drive is not violated. For instance, the LT3752's S_{OUT} drivers are rated for a maximum current of about 100mA. This results in:

$$R_{SYNC} \geq \frac{V_{MAX}}{100mA}$$

V_{MAX} is the S_{OUT} gate driver high voltage, which is typically about 8V to 12V for the LT3752.

The following steps can be used as guidelines to calculate R_{SYNC} and C_{SYNC} values:

Step 1: Choose Pulse Transformer. A typically recommended choice is the PE-68386NL from Pulse Electronics.

Step 2: Determine the primary-side IC's maximum S_{OUT} signal magnitude, V_{MAX} (see Figure 19). This sets the maximum magnitude of the signal on the LT8311's SYNC pin.

Step 3: Guess a capacitance value for C_{SYNC}. A good starting value might be between 220pF and 1nF.

Step 4: Pick R_{SYNC} based on constraint shown in the following equation:

$$\frac{1}{2} \bullet \sqrt{\left(\frac{L_m}{C_{SYNC}}\right)} \geq R_{SYNC} \geq MAX$$

$$\left\{\frac{50ns}{\left[C_{SYNC} \bullet -1 \bullet IN(2V / V_{MAX})\right]}, \left(\frac{V_{MAX}}{I_{MAX}}\right)\right\}$$

where I_{MAX} is the maximum current source/sink capability of the primary-side IC's S_{OUT} pin (LT3752's maximum capability is about 100mA and LT8310's maximum current capability is about 300mA). It is recommended to design for an I_{MAX} that is lower than the maximum recommended source current specified, to allow for design margin over process and temperature.

If the R_{SYNC} calculation in Step 4 yields an unreasonable resistance value, go back to steps 1 to 3, and change either L_m, V_{MAX}, or C_{SYNC}. Recalculate R_{SYNC} in Step 4 until all criteria are satisfied.

Design Example

In a LT3752-LT8311 forward converter design, pulse transformer PE-68386NL is chosen for communication of LT3752 S_{OUT} signals, through a highpass filter, to the LT8311's SYNC pin.

Step 1: This transformer has a magnetizing inductance of L_m = 785µH.

Step 2: LT3752's V_{MAX} = 12V.

Step 3: Choose C_{SYNC} = 220pF

Step 4: Designing for I_{MAX} = 70mA, L_m = 785µH, C_{SYNC} = 220pF, V_{MAX} = 12V, results in the following calculation for R_{SYNC}:

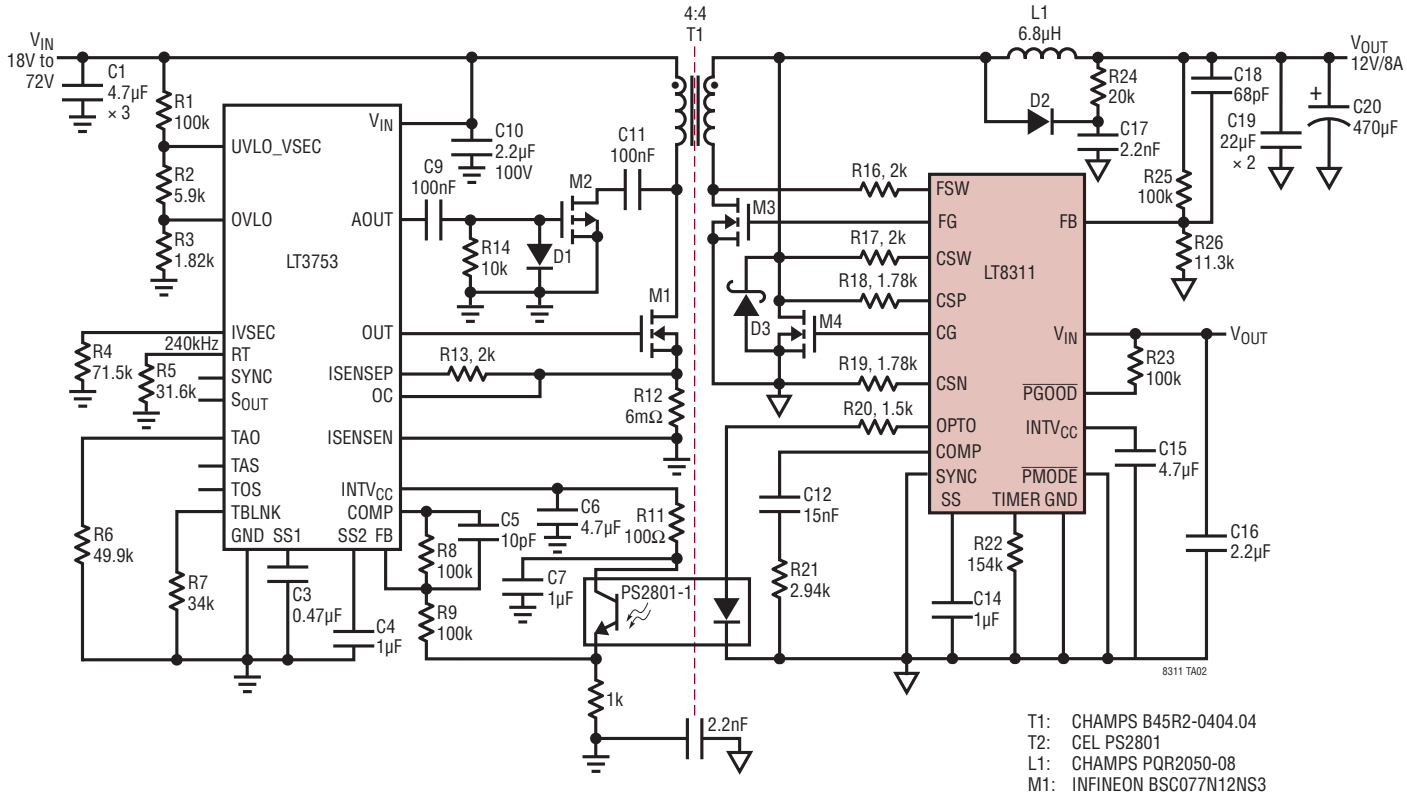
$$944\Omega \geq R_{SYNC} \geq Max\ \{127\Omega, 171\Omega\}$$

Conclusion

In this example, R_{SYNC} = 560Ω is chosen along with C_{SYNC} = 220pF as the highpass filter to be used along with pulse transformer, PE-68386NL to communicate the LT3752's S_{OUT} signals to the LT8311's SYNC pin.

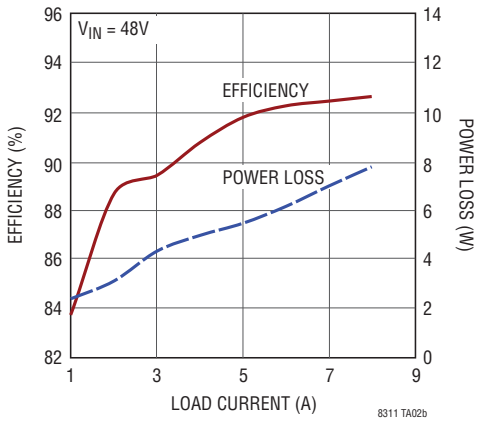
TYPICAL APPLICATIONS

18V to 72V, 12V/8A Active Clamp Isolated Forward Converter



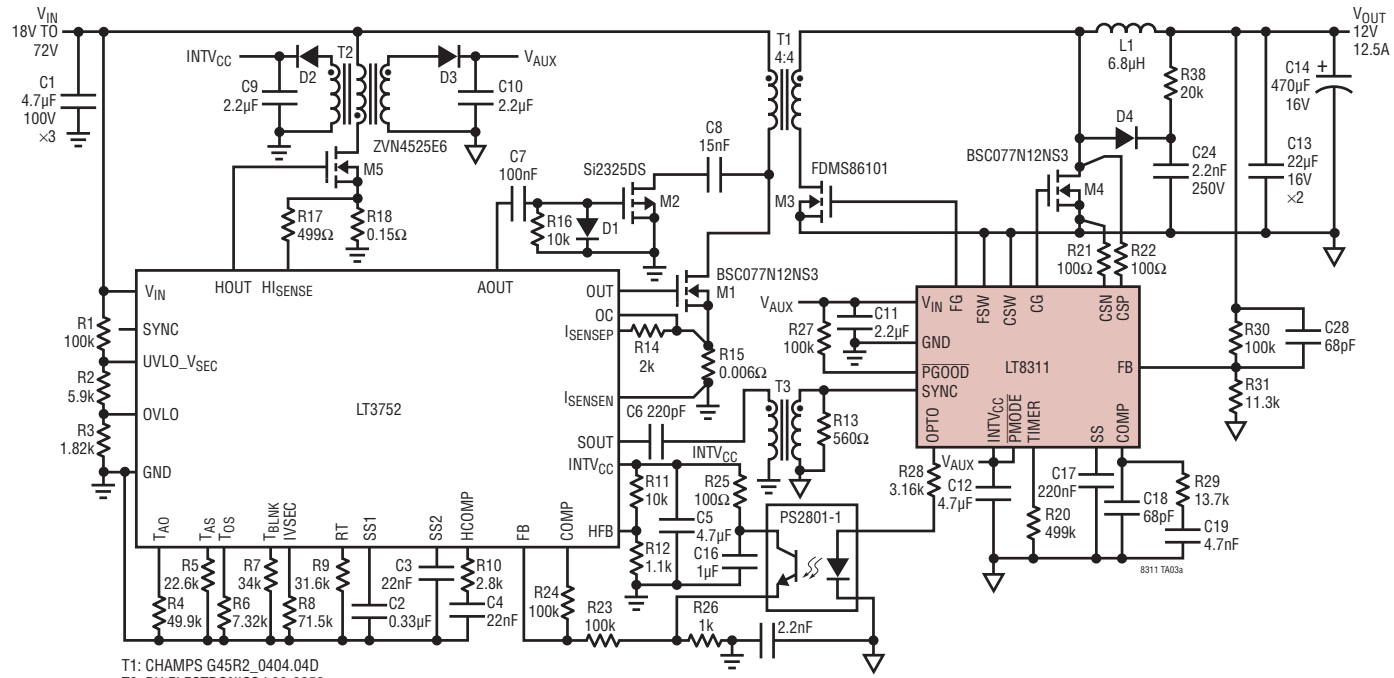
T1: CHAMPS B45R2-0404.04
T2: CEL PS2801
L1: CHAMPS PQR2050-08
M1: INFINEON BSC077N12NS3
M2: IR IRF6217PBF
M3: FAIRCHILD SEMI. FDMS86101DC
M4: INFINEON BSC077N12NS3
D2: CENTRAL SEMI. CMMR1U-02
D3: DIODES INC. SBRIU150

Efficiency and Power Loss at V_{IN} = 48V



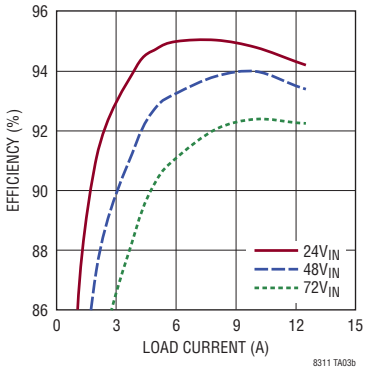
TYPICAL APPLICATIONS

18V to 72V, 12V/12.5A, 150W Active Clamp Isolated Forward Converter



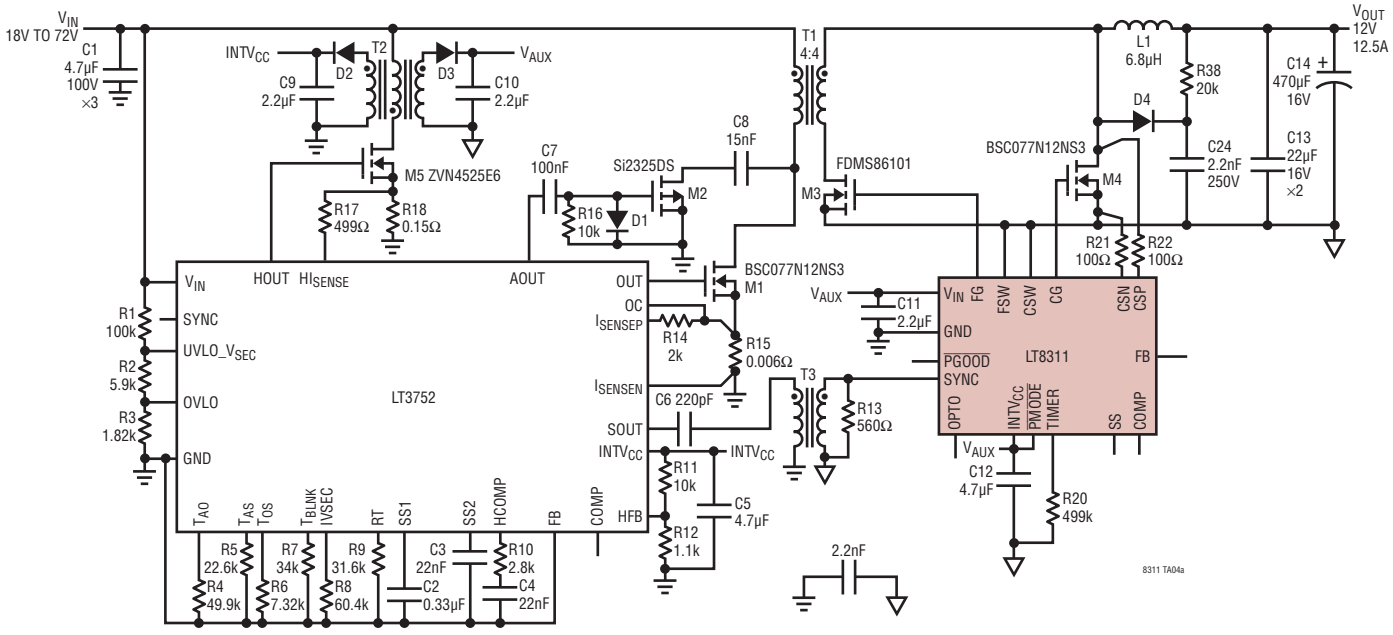
T1: CHAMPS G45R2_0404.04D
T2: BH ELECTRONICS L00-3250
T3: PULSE PE-68386NL
L1: CHAMPS G45AH2-0404-D4
D1, D2, D3: BAS516
D4: CENTRAL SEMI CMMR1U-02

Efficiency vs Load Current



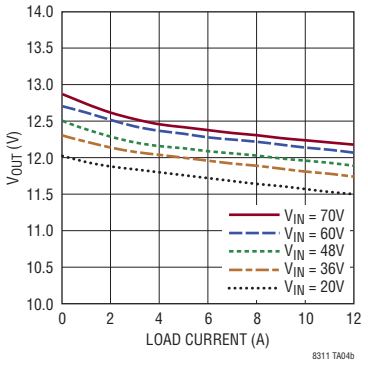
TYPICAL APPLICATIONS

18V to 72V, 12V/12.5A, 150W No-Opto, Active Clamp Isolated Forward Converter

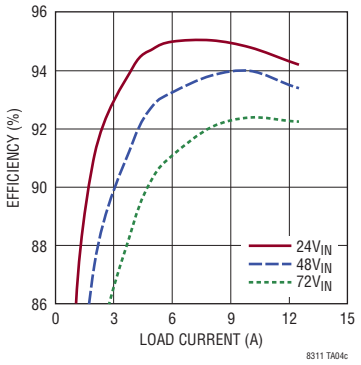


T1: CHAMPS G45R2_0404.04D
T2: BH ELECTRONICS L00-3250
T3: PULSE PE-68386NL
L1: CHAMPS G45AH2-0404-D4
D1, D2, D3: BAS516
D4: CENTRAL SEMI CMMR1U-02

V_{OUT} vs Load Current (No-Opto)

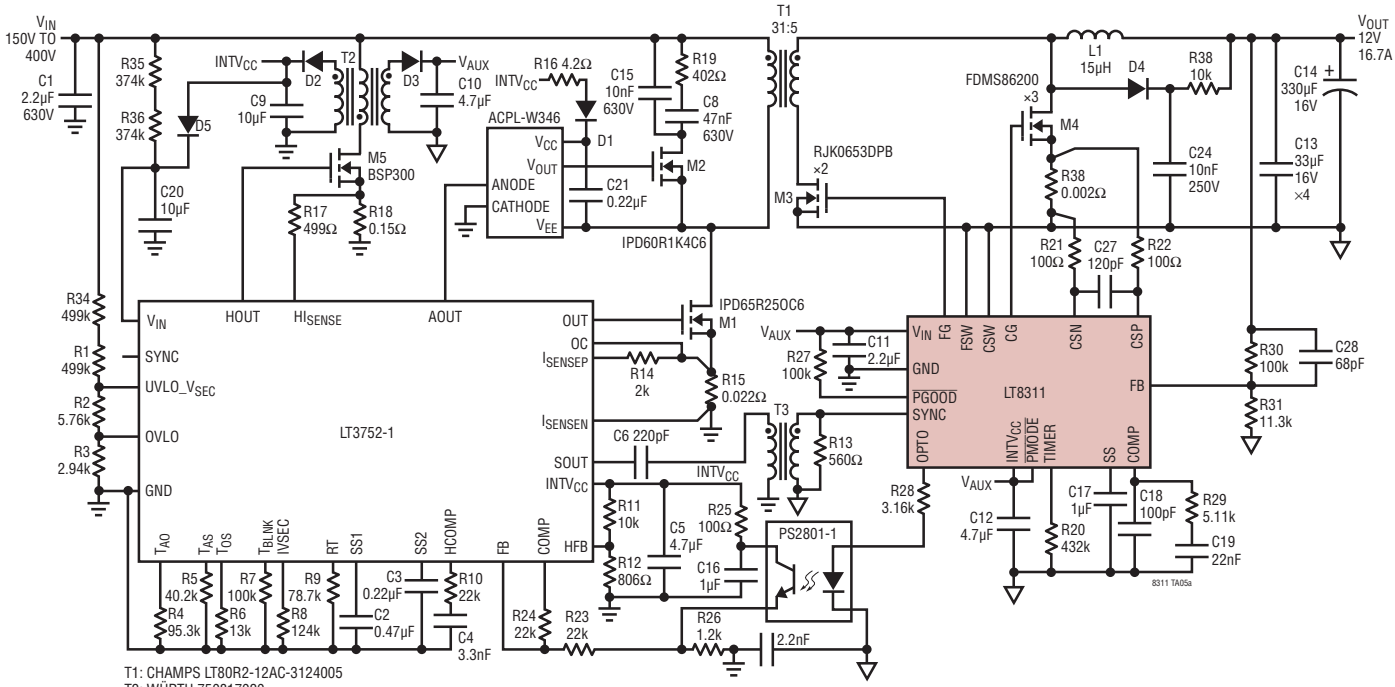


Efficiency vs Load Current



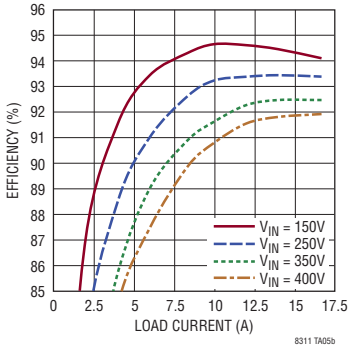
TYPICAL APPLICATIONS

150V to 400V, 12V/16.7A, 200W Active Clamp Isolated Forward Converter



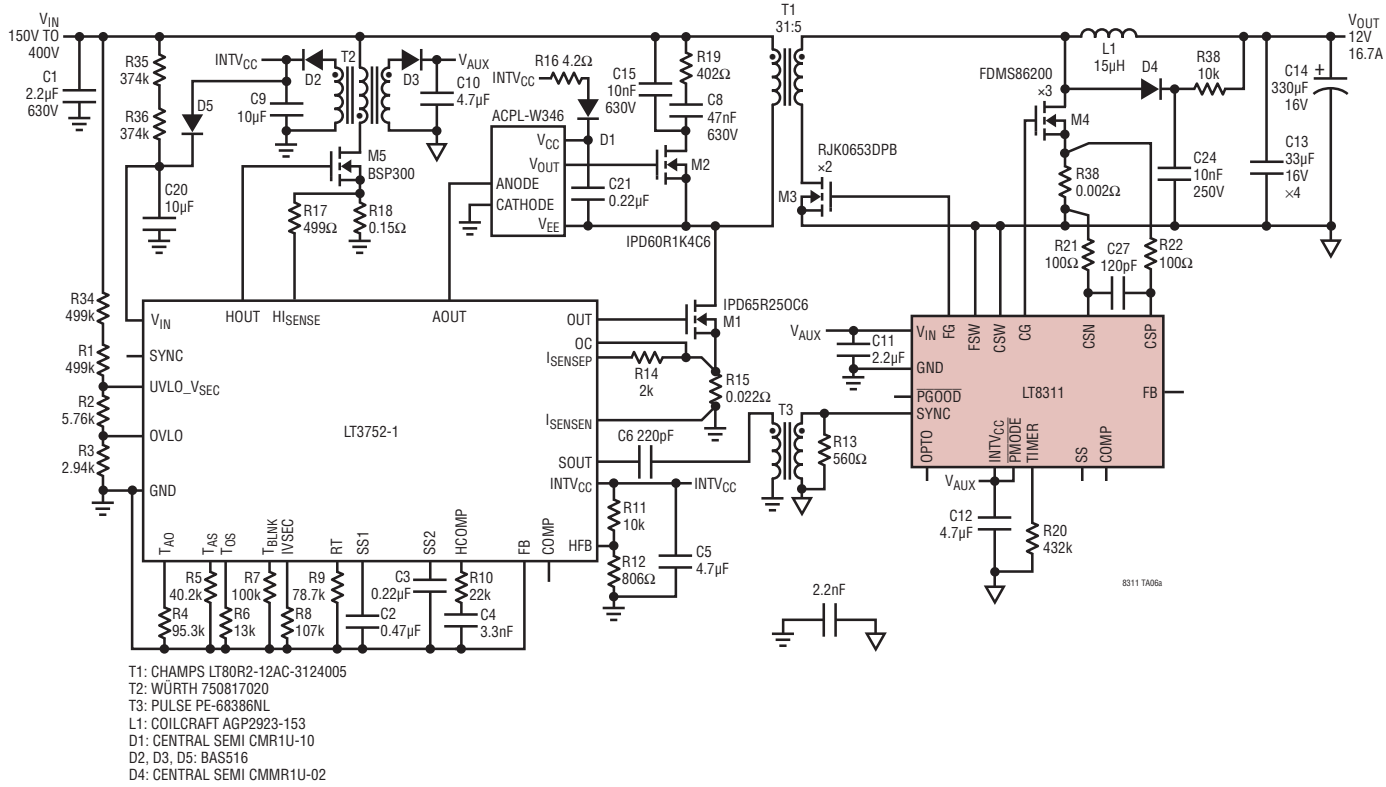
T1: CHAMPS LT80R2-12AC-3124005
T2: WÜRTH 750817020
T3: PULSE PE-68386NL
L1: COILCRAFT AGP2923-153
D1: CENTRAL SEMI CMR1U-10
D2, D3, D5: BAS516
D4: CENTRAL SEMI CMMR1U-02

Efficiency vs Load Current



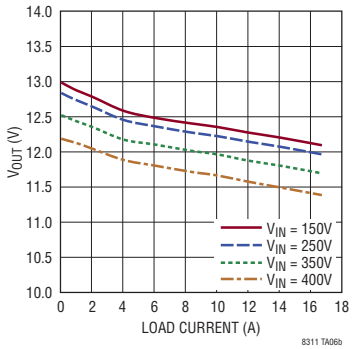
TYPICAL APPLICATIONS

150V to 400V, 12V/16.7A, 200W No-Opto, Active Clamp Isolated Forward Converter

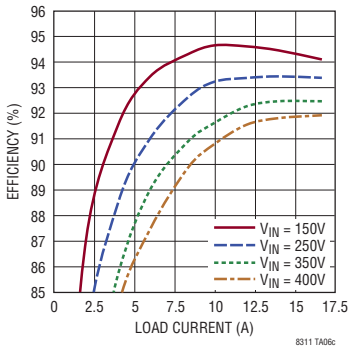


T1: CHAMPS LT80R2-12AC-3124005
T2: WÜRTH 750817020
T3: PULSE PE-68386NL
L1: COILCRAFT AGP2923-153
D1: CENTRAL SEMI CMR1U-10
D2, D3, D5: BAS516
D4: CENTRAL SEMI CMMR1U-02

V_{OUT} vs Load Current (No-Opto)

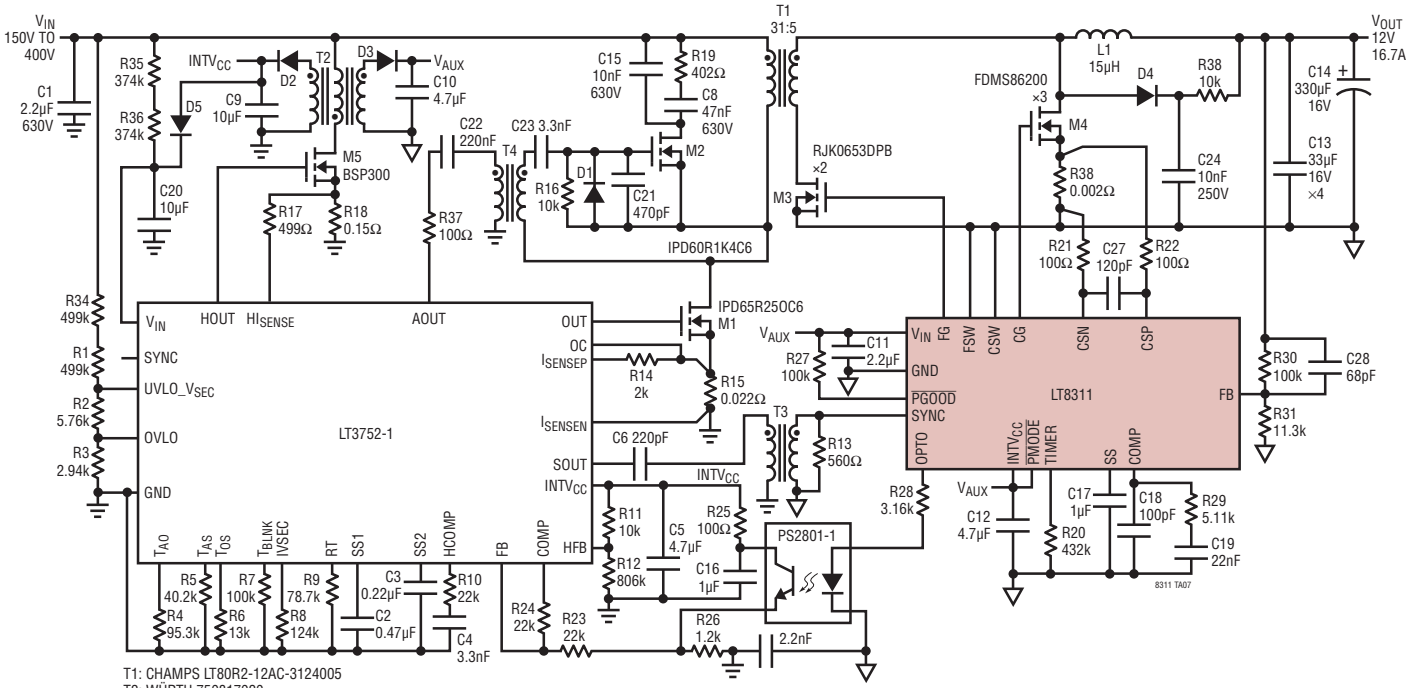


Efficiency vs Load Current



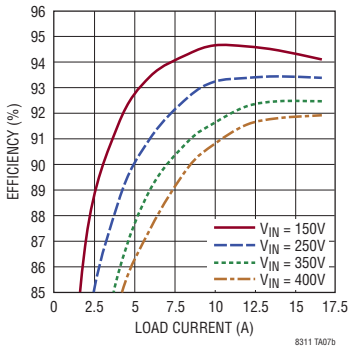
TYPICAL APPLICATIONS

150V to 400V, 12V/16.7A, 200W, Active Clamp Isolated Forward Converter (Using Gate Drive Transformer for High Side Active Clamp)



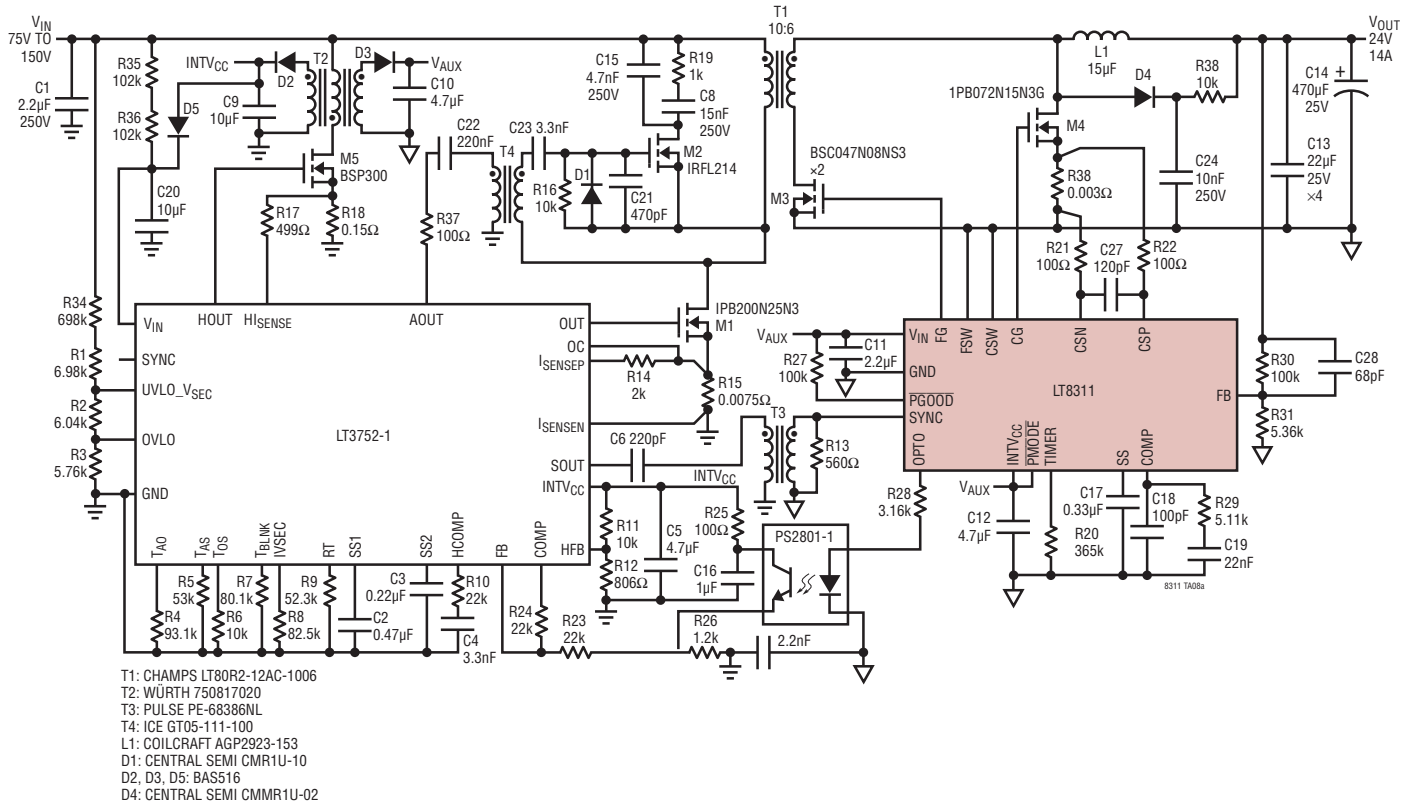
T1: CHAMPS LT80R2-12AC-3124005
T2: WÜRTH 750817020
T3: PULSE PE-68386NL
T4: ICE GT05-111-100
L1: COILCRAFT AGP2923-153
D1: CENTRAL SEMI CMR1U-10
D2, D3, D5: BAS516
D4: CENTRAL SEMI CMMR1U-02

Efficiency vs Load Current



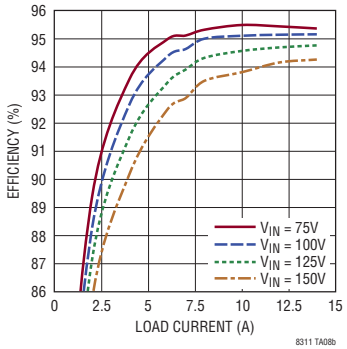
TYPICAL APPLICATIONS

75V to 150V, 24V/14A 340W Active Clamp Isolated Forward Converter (Using Gate Drive Transformer for High Side Active Clamp)



T1: CHAMPS LT80R2-12AC-1006
T2: WÜRTH 750817020
T3: PULSE PE-68386NL
T4: ICE GT05-111-100
L1: COILCRAFT AGP2923-153
D1: CENTRAL SEMI CMR1U-10
D2, D3, D5: BAS516
D4: CENTRAL SEMI CMMR1U-02

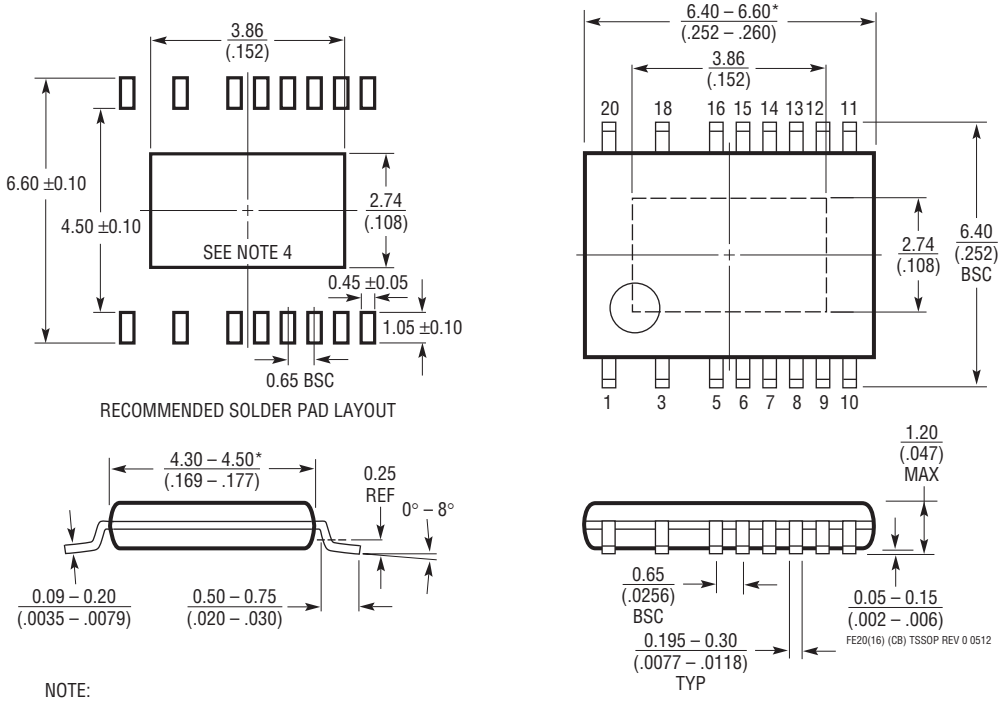
Efficiency vs Load Current



PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

FE Package
Variation: FE20(16)
20-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1924 Rev Ø)
Exposed Pad Variation CB



NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN MILLIMETERS (INCHES)
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT

*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE