60V_{IN}/120V_{OUT} Dual LED Controller with Exponential PWM and Scalable Dimming

FEATURES

- **Two independent High Voltage LED Driver Controllers Channels**
- **128:1 Internal Exponential PWM Dimming**
- **Two-Pin Multiplying Analog Dimming (CH2)**
- **Spread Spectrum Frequency Modulation**
- **20,000:1 External PWM Dimming at 100Hz**
- **Rail-to-Rail LED Current Sensing: 0V to 120V**
- **±2% LED Current Regulation**
- **±2% Output Voltage Regulation**
- **LED Short/Open Protection and Indication**
- **Wide Input Voltage Range (5V to 60V)**
- **PMOS Switch Driver for PWM and Output Disconnect**
- Independent Channel Dimming
- Constant-Voltage and Constant-Current Regulation
- Adjustable Switching Frequency 100kHz to 2MHz
- Independent OPEN/SHORT LED FAULT per channel
- Programmable V_{IN} UVLO with Hysteresis
- Side Solderable 28-Lead 4mm × 5mm QFN Package
- AEC-Q100 Qualified for Automotive Applications

APPLICATIONS

- High Voltage LED Applications
- Automotive Head Lamps/Running Lamps
- Accurate Current Limited Voltage Regulator

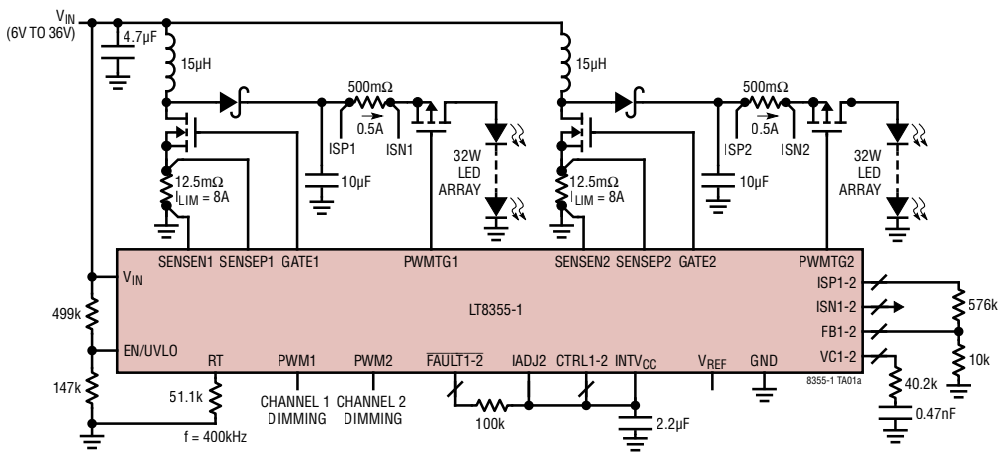
DESCRIPTION

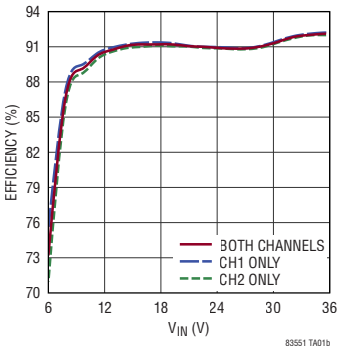
The LT®8355-1 a dual-channel DC/DC controller designed to drive two strings of high current LEDs. The fixed frequency, current mode architecture results in stable operation over a wide range of supply and output voltages. Voltage feedback pins serve as the inputs for several LED protection features and makes it possible for the converters to operate as a constant-voltage sources.

The LT8355-1 senses output current at the high or low side of the load. The product of CTRL2 and IADJ2 inputs provides analog programming of the output current for channel 2. Channel 1 output current is programmed through CTRL1 input. The PWM input and PWMTG high side PMOS driver provides precision time-based LED dimming capability. When driven by an external digital signal, the PWM input provides LED dimming ratios of up to 20,000:1 at 100Hz. When driven by a constant voltage, the PWM input selects from one of 128 internally generated, precision, exponentially spaced dimming ratios ranging from 0.78% up to 100%.

TYPICAL APPLICATION

Dual 32W Boost LED Driver





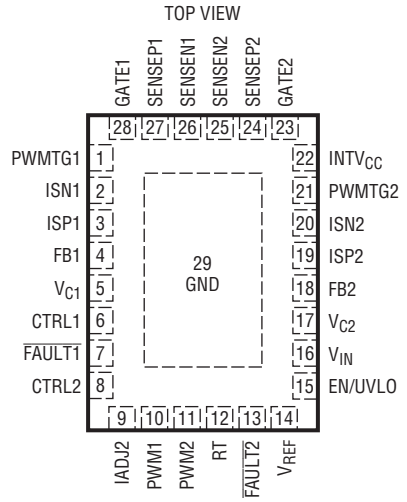
Rev. A

ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN} 62V
EN/UVLO.....62V, –0.3V
ISP1, ISP2, ISN1 and ISN2.....120V
ISP1 – ISN1, ISP2 – ISN2 ..... ±1V (Note 9)
CTRL1, CTRL2, FB1 and FB2.....15V
$\overline{FAULT1}$, $\overline{FAULT2}$, IADJ2, PWM1 and PWM2.....15V
$INTV_{CC}$.....V_{IN} + 0.3V, 8V
SENSEP1, SENSEN1, SENSEP2, SENSEN2 .....±0.5V
RT, GATE1, GATE2, PWMTG1 and PWMTG2 ..... (Note 2)
V_{C1}, V_{C2}, and V_{REF} ..... (Note 2)
Operating Junction Temperature Range (Notes 3, 4)
LT8355I-1 .....–40°C to 125°C
Storage Temperature Range .....–65°C to 150°C

PIN CONFIGURATION



UFDM PACKAGE
28-LEAD (4mm × 5mm) SIDE-SOLDERABLE PLASTIC QFN
θ_{JA} = 43°C/W, θ_{JC} = 3.4°C/W
EXPOSED PAD (PIN 29) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
AUTOMOTIVE PRODUCTS*				
LT8355IUFDM-1#WPBF	LT8355IUFDM-1#WTRPBF	83551	28-Lead (4mm × 5mm) Side-Solderable Plastic QFN	–40°C to 125°C

Contact the factory for parts specified with wider operating temperature ranges.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

*Versions of this part are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. These models are designated with a #W suffix. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 2). Unless otherwise noted, V_{IN} = EN/UVLO = 12V, ISP1,2 = ISN1,2 = 60V, CTRL1,2 = IADJ2 = 2V, PWM1,2 = $INTV_{CC}$, FB1,2 = 1V, SENSEN1,2 = 0V.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Supply Range		●	5		60	V
Input (V_{IN}) Quiescent Current	PWM1,2 = 0V			3		mA
Input (V_{IN}) Shutdown Current	EN/UVLO = 0.3V EN/UVLO = 1.1V, EN/UVLO Rising			0.1 12	1 20	µA µA
EN/UVLO Shutdown Threshold	EN/UVLO Falling	●	1.15	1.25	1.35	V
EN/UVLO Rising Hysteresis	EN/UVLO Rising			60		mV
EN/UVLO Pin Current (Device Off)	EN/UVLO = 1.1V, EN/UVLO Rising			2.4		µA
EN/UVLO Pin Current (Device On)	EN/UVLO = 1.35V			0		µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 2). Unless otherwise noted, V_{IN} = EN/UVLO = 12V, ISP1,2 = ISN1,2 = 60V, CTRL1,2 = IADJ2 = 2V, PWM1,2 = $INTV_{CC}$, FB1,2 = 1V, SENSEN1,2 = 0V.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Internal Voltage Regulators						
$INTV_{CC}$ Regulation Voltage	PWM1,2 = 0V, I_{INTVCC} = 1mA, 12V < V_{IN} < 60V		7.35	7.5	7.65	V
$INTV_{CC}$ Line Regulation	PWM1,2 = 0V, 10 < V_{IN} < 60V			0.75	3	mV/V
$INTV_{CC}$ Load Regulation	PWM1,2 = 0V, 1mA < I_{INTVCC} < 30mA			2.25	4.5	mV/mA
$INTV_{CC}$ Current Limit	PWM1,2 = 0V, V_{IN} = 12V, $INTV_{CC}$ = 7V PWM1,2 = 0V, V_{IN} = 60V, $INTV_{CC}$ = 7V		110 30	140 45	170 60	mA mA
$INTV_{CC}$ Dropout Voltage	PWM1,2 = 0V, V_{IN} = 5V, I_{LOAD} = 10mA			250		mV
$INTV_{CC}$ Undervoltage Lockout Threshold	PWM1,2 = 0V, $INTV_{CC}$ Falling			4.3		V
V_{REF} Voltage	I_{VREF} = 0.5mA	●	1.97	2	2.02	V
V_{REF} Load Regulation	I_{VREF} = 0.1mA to 1mA			5	8	mV/mA
V_{REF} Current Limit	V_{REF} = 1.8V		2.5	3.2	4.0	mA
Channel 1, Channel 2 Current Regulation (Note 5)						
ISP, ISN Common Mode Voltage Range		●	0		110	V
LED Current Sense Threshold (V_{ISP} – V_{ISN})	CTRL1,2 = 2V, IADJ2 = 2V (100%), ISP1,2 = 100V CTRL1,2 = 1V, IADJ2 = 2V (50%), ISP1,2 = 100V CTRL1,2 = 0.6V, IADJ2 = 2V (10%), ISP1,2 = 100V CTRL1,2 = 2V, IADJ2 = 2V (100%), ISN1,2 = 0V	● ● ● 	245 120 20 240	250 125 25 250	255 130 30 260	mV mV mV mV
LED2 Current Sense Threshold (V_{ISP2} – V_{ISN2})	CTRL2 = 2V, IADJ2 = 1V (50%), ISP = 100V	●	118	125	134	mV
SENSE Current Limit Threshold (SENSEP – SENSEN)	50% Duty Cycle at GATE (Note 6)	●	95	108	120	mV
CTRL Off Threshold (Falling)		●	285	310	335	mV
IADJ2 Off Threshold (Falling)				500		mV
CTRL Off Hysteresis				30		mV
IADJ2 Off Hysteresis				20		mV
CTRL Pin Current	Current Out of Pin, CTRL1,2 = 0			20		nA
IADJ2 Pin Current	IADJ2 = 1.5V			0		nA
ISP, ISN Pin Current (Combined)	PWM1,2 = $INTV_{CC}$, ISP1,2 = 100V (Active) PWM1,2 = 0V, ISP1,2 = 100V (Standby)			600 20	 25	µA µA
Error Amp Transconductance	CTRL1,2 = 2V, IADJ2 = 2V (Full-Scale)			65		µS
Error Amp Output Resistance				15		MΩ
Channel 1, Channel 2 Output Voltage Regulation						
FB Regulation Voltage (V_{FB})	CTRL1,2 = 2V, IADJ2 = 2V CTRL1,2 = 2V, IADJ2 = 2V	 ●	1.182 1.176	1.2 1.2	1.218 1.224	V V
FB Pin Current	Current Out of Pin, $V_{FB1,2}$ = 1.18V			20		nA
FB Amplifier Transconductance				380		µS
Oscillator						
Programmed Switching Frequency (f_{SW1}, Channel 1)	R_T = 9.09kΩ R_T = 51.1kΩ R_T = 215kΩ	 ● 	1800 380 96	1950 400 102	2100 420 108	kHz kHz kHz
Channel Frequency Difference (f_{SW2} – f_{SW1})	R_T = 51.1kΩ		4.5			$\%f_{SW1}$
Spread Spectrum Frequency Range			100		126	$\%f_{SW}$
Minimum Off-Time	R_T = 9.09kΩ R_T = 51.1kΩ R_T = 215kΩ	● ● ●	30 75 100	60 120 170	85 165 240	ns ns ns

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 2). Unless otherwise noted, V_{IN} = EN/UVLO = 12V, ISP1,2 = ISN1,2 = 60V, CTRL1,2 = IADJ2 = 2V, PWM1,2 = $INTV_{CC}$, FB1,2 = 1V, SENSEN1,2 = 0V.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum On-Time	$C_{GATE1,2}$ = 3.3nF $C_{GATE1,2}$ = 10nF, RT = 51.1kΩ (Note 7)			100 180		ns ns
Channel 1, Channel 2 External NMOS Power Switch Driver						
Pull-Up Device On-Resistance				5		Ω
Pull-Down Device On-Resistance				3		Ω
GATE Rise Time (Note 8)	$C_{GATE1,2}$ = 3.3nF, 10% to 90%			45		ns
GATE Fall Time (Note 8)	$C_{GATE1,2}$ = 3.3nF, 90% to 10%			40		ns
Channel 1, Channel 2 External PMOS Driver						
PWMTG ON Voltage (V_{ISP} – V_{PWMTG})	$V_{ISP1,2}$ = 100V		7.5	8.5	9.5	V
PWMTG OFF Voltage (V_{ISP} – V_{PWMTG})	$V_{ISP1,2}$ = 100V			0	0.3	V
PWMTG Turn-On Time	C_L = 470pF, $V_{ISP1,2}$ = 100V			150		ns
PWMTG Turn-Off Time	C_L = 470pF, $V_{ISP1,2}$ = 100V			180		ns
Channel 1, Channel 2 Fault Detection						
FB LED Open Threshold	$V_{ISP1,2}$ = $V_{ISN\ 1,2}$, FB Rising		1.116	1.14	1.164	V
FB Overvoltage Threshold	FB1,2 Rising		1.235	1.26	1.285	V
FB Shorted LED Threshold	FB1,2 Falling			300	330	mV
LED Overcurrent Protection Threshold (V_{ISP} – V_{ISN})			580	670	760	mV
$\overline{FAULT}$ Pin Pull Down Current	$V_{\overline{FAULT1-2}}$ = 0.3V, $V_{FB1,2}$ = 1.3V		0.5			mA
$\overline{FAULT}$ Pin Leakage Current	$V_{\overline{FAULT1-2}}$ = 15V, $V_{FB1,2}$ = 0.7V				100	nA
Channel 1, Channel 2 Internal PWM Generator						
PWM Pin Voltage for Max Duty Ratio				1.5		V
PWM Pin Voltage for Min Duty Ratio				0.5		V
PWM Off Threshold (Falling)				0.4		V
PWM On Threshold (Rising)				1.6		V
Minimum Duty Ratio	$V_{PWM1,2}$ = 0.5V, R_T = 51.1kΩ			0.78		%
Maximum Duty Ratio	$V_{PWM1,2}$ = 1.5V, R_T = 51.1kΩ			100		%
PWM Voltage Step per Duty Ratio Setting	(Note 8)			7.8		mV
PWM Pin Current	$V_{PWM1,2}$ = 1V			0		nA
PWM Clock Frequency				f_{SW}/1000		Hz
Fraction of V_{REF} for 10% Duty	R_T = 51.1kΩ			0.511V_{REF}		V

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Do not apply a positive or negative voltage to the PWMTG1, PWMTG2, RT, V_{REF}, V_{C1}, V_{C2}, GATE1 or GATE2 pin, otherwise permanent damage may occur. Use these pins only as directed in the Pin Functions and Applications Information sections.

Note 3: LT8355I-1 is guaranteed to meet performance specifications from –40°C to 125°C junction temperature. Operation lifetime is derated at junction temperatures greater than 125°C.

Note 4: This IC include overtemperature protection that is intended to protect the device during momentary overload conditions. The maximum rated junction temperature will be exceeded when this protection is active. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability or permanently damage the device.

Note 5: LED voltage and current sense amplifier parameters are measured in a servo loop with V_C.

Note 6: Tested in a non-switching setup and correlated by design.

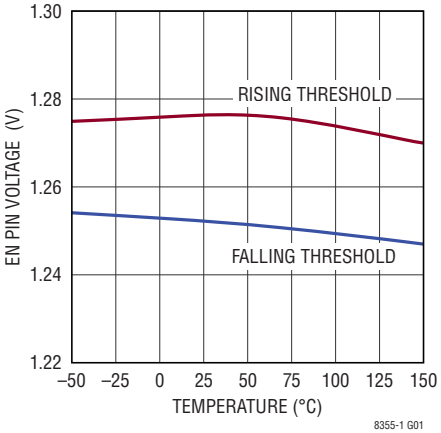
Note 7: Tested at R_T = 51.1kΩ, guaranteed for all R_T by design.

Note 8: GATE1,2 rise and fall times as well as the step size for the PWM ADC are guaranteed by design and not tested.

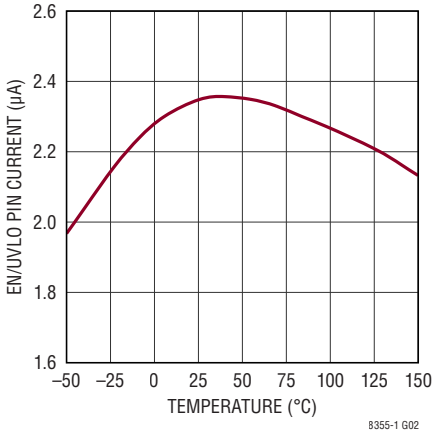
Note 9: ISP1 – ISN1 and ISP2 – ISN2 may exceed 10V transiently. Do not exceed ISP1 – ISN1 = 10V or ISP2 – ISN2 = 10V for more than 1 ms.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

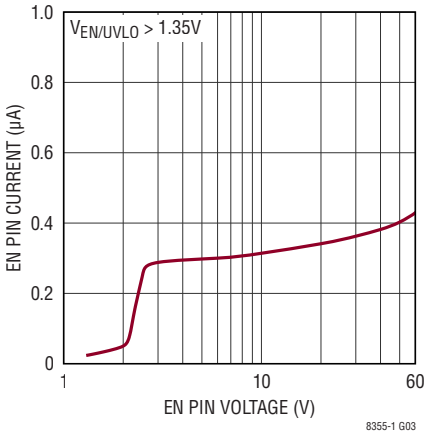
EN/UVLO Thresholds vs Temperature



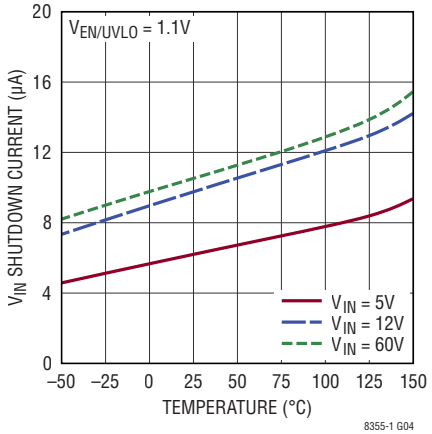
EN/UVLO Hysteresis Current vs Temperature



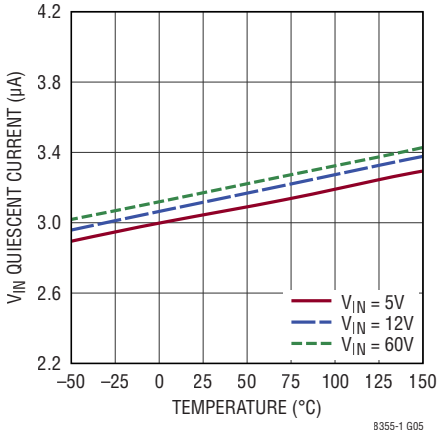
EN/UVLO Current vs Voltage Above Turn-On Threshold



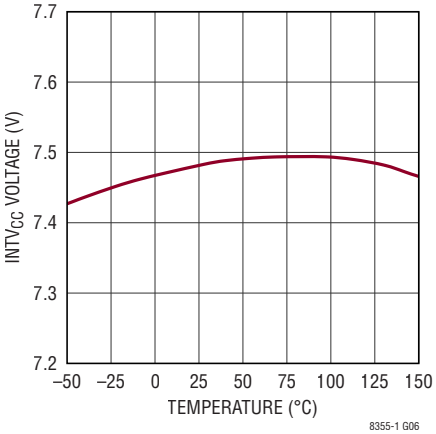
V_{IN} Shutdown Current vs Temperature



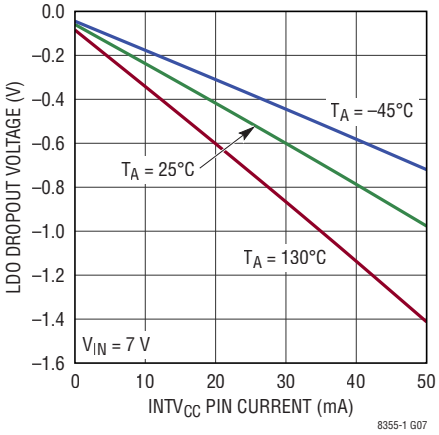
V_{IN} Quiescent Current vs Temperature



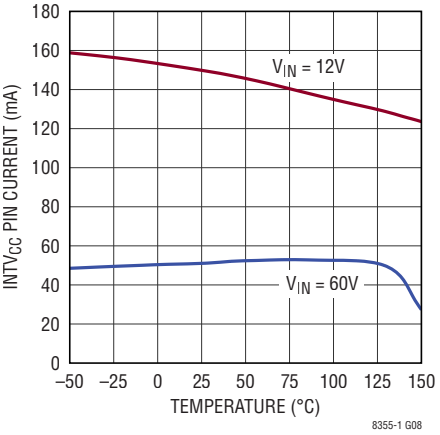
$INTV_{CC}$ Voltage vs Temperature



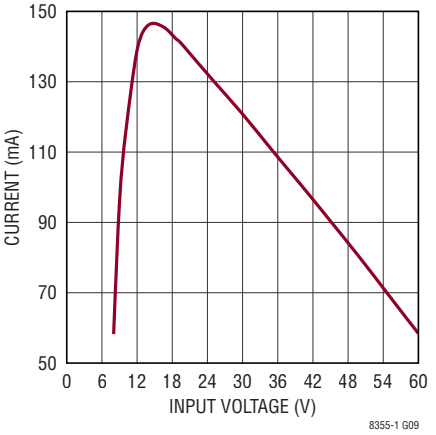
$INTV_{CC}$ Dropout vs Temperature



$INTV_{CC}$ Current Limit vs Temperature

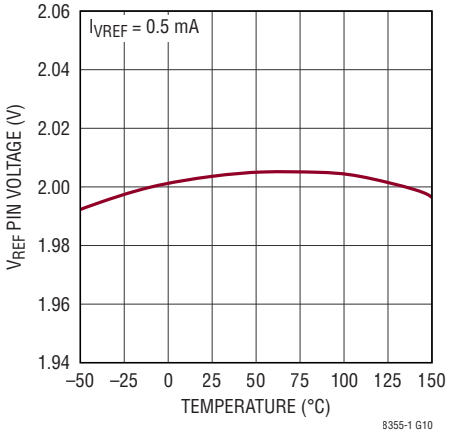


$INTV_{CC}$ Current Limit vs V_{IN}

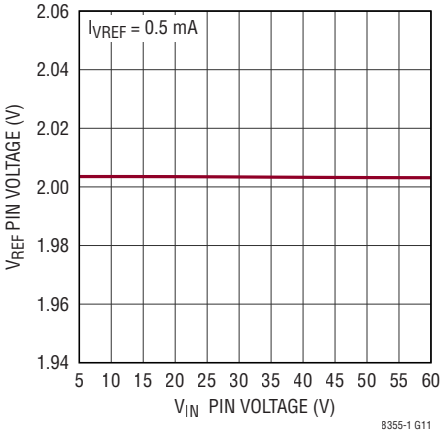


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

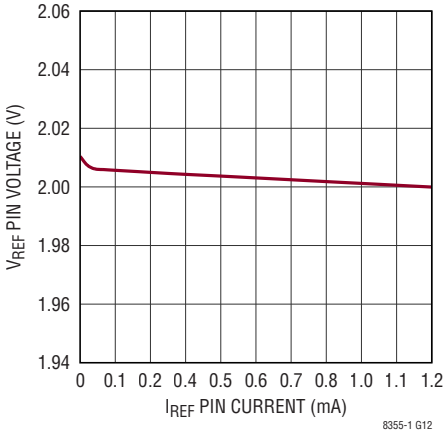
V_{REF} Voltage vs Temperature



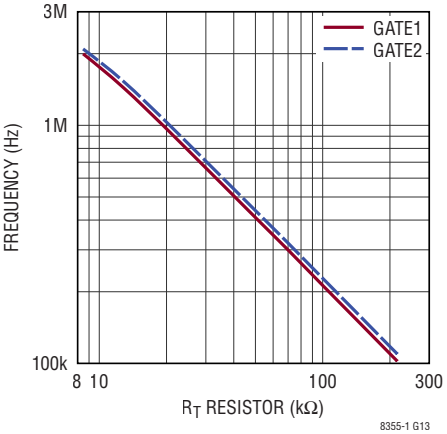
V_{REF} Line Regulation



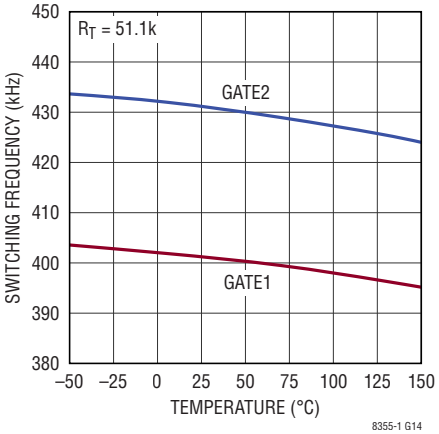
V_{REF} Load Regulation



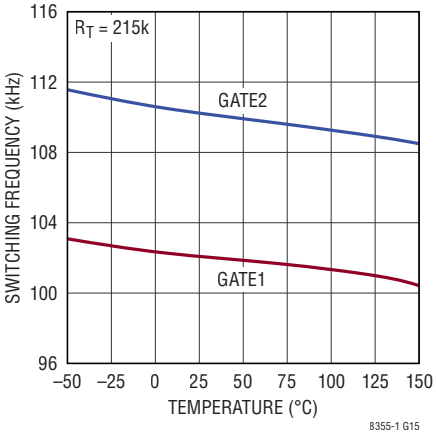
Switching Frequency vs R_T Resistor



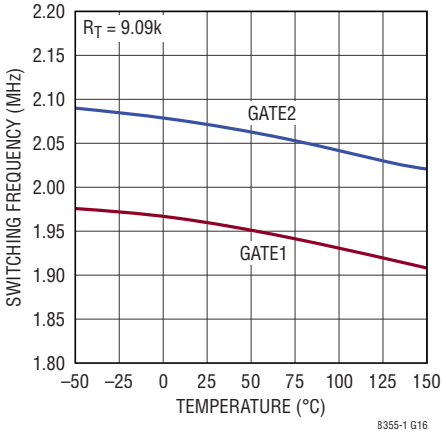
Switching Frequency (400kHz) vs Temperature



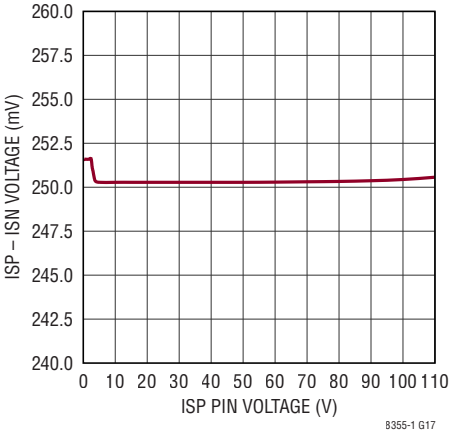
Switching Frequency (100kHz) vs Temperature



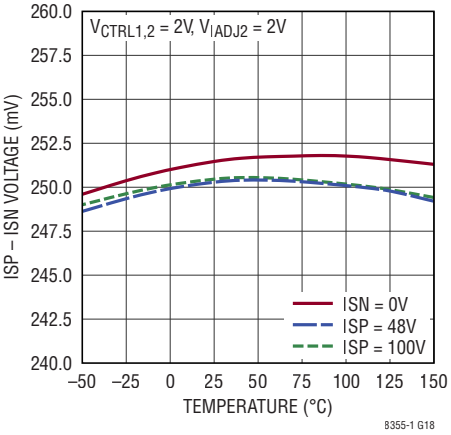
Switching Frequency (2MHz) vs Temperature



ISP – ISN Voltage vs ISP Voltage

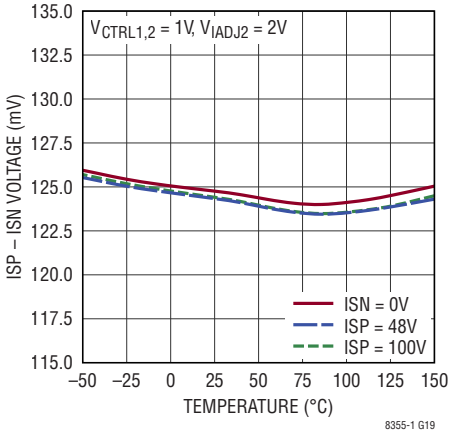


ISP – ISN Accuracy Full-Scale Threshold vs Temperature

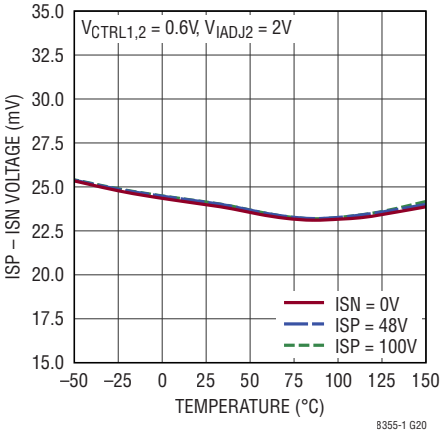


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

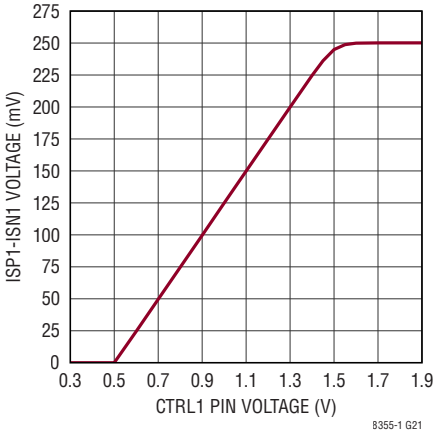
ISP – ISN Accuracy at CTRL = 1V vs Temperature



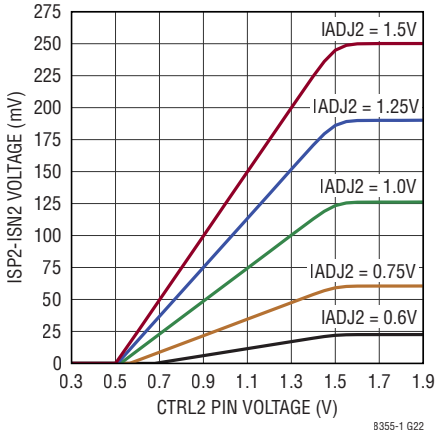
ISP – ISN Accuracy at CTRL = 0.6V vs Temperature



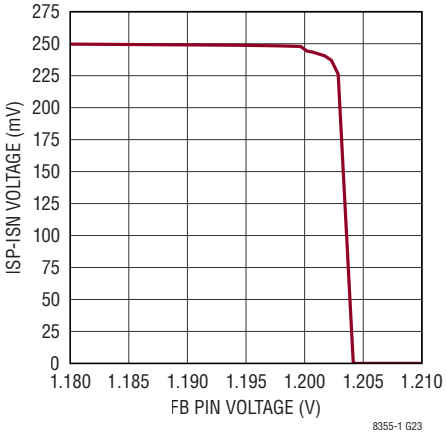
ISP1-ISN1 Regulation Voltage vs CTRL1 Pin Voltage



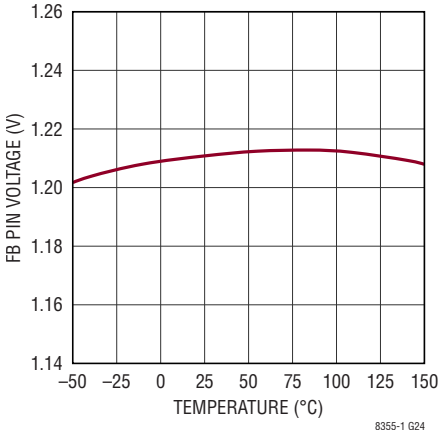
ISP2-ISN2 Regulation Voltage vs CTRL2, IADJ2 Pin Voltage



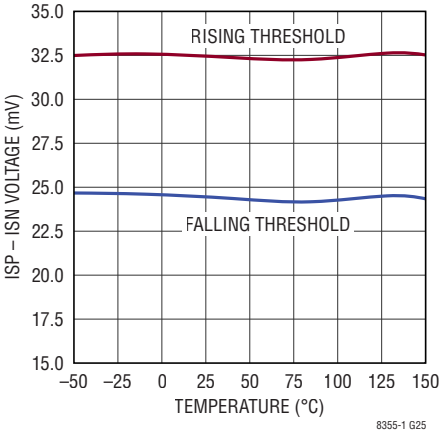
ISP-ISN Voltage vs FB Pin Voltage



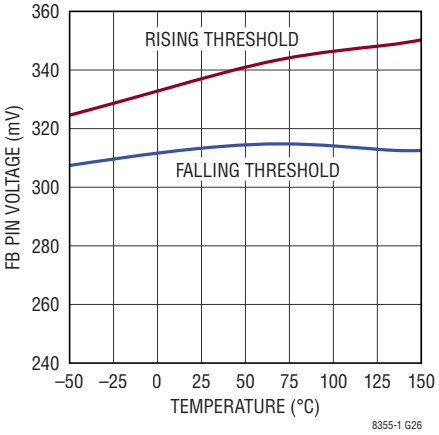
Output Voltage Regulation vs Temperature



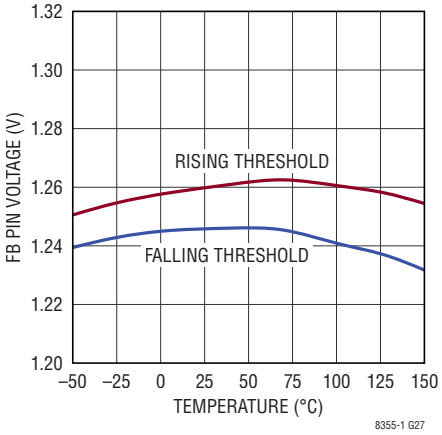
C/10 Threshold vs Temperature



FB Short LED Threshold vs Temperature

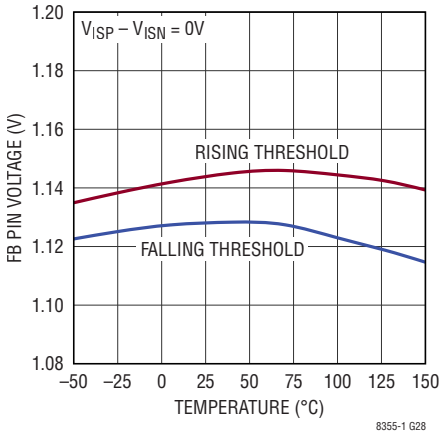


FB Overvoltage Threshold vs Temperature

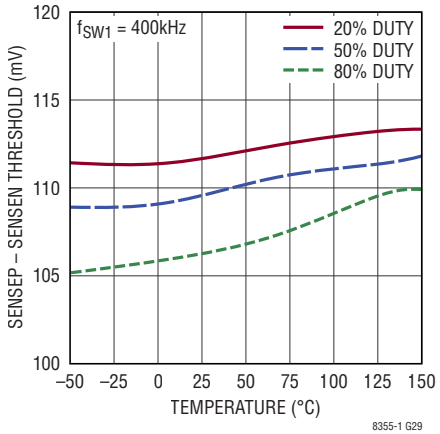


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

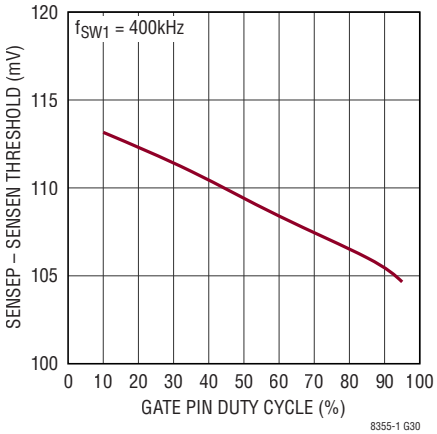
FB Open LED Threshold vs Temperature



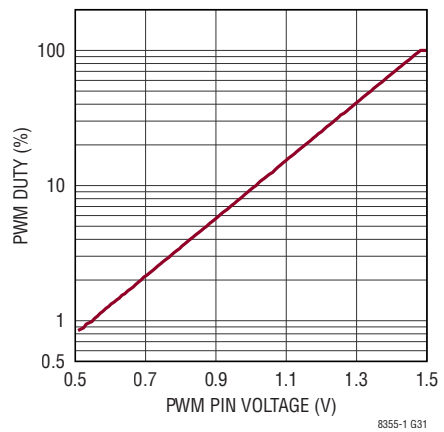
SENSEP – SENSEN Current Limit vs Temperature



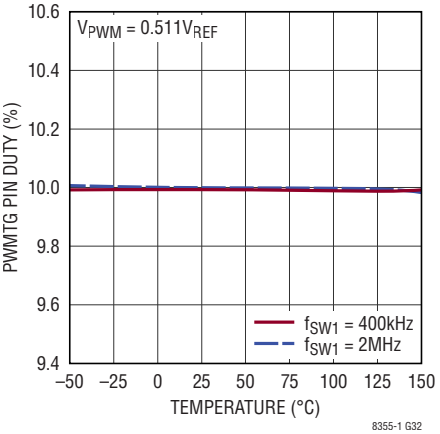
SENSEP – SENSEN Current Limit vs Duty Ratio



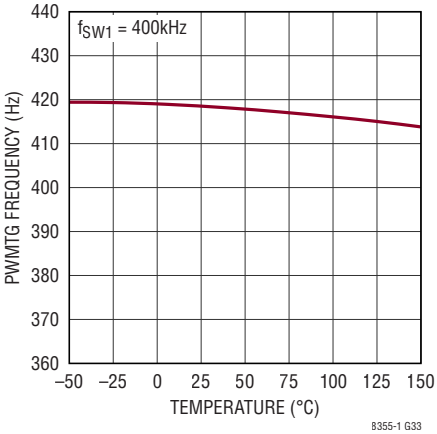
PWMTG Duty vs PWM Pin Voltage



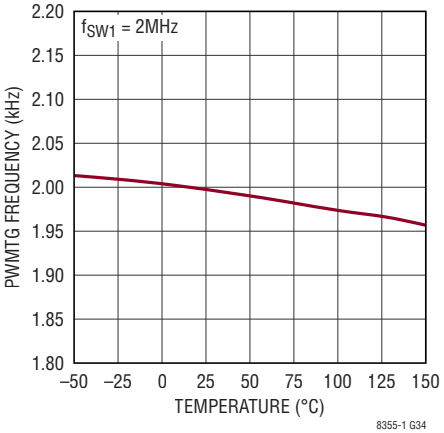
PWMTG Duty vs Temperature



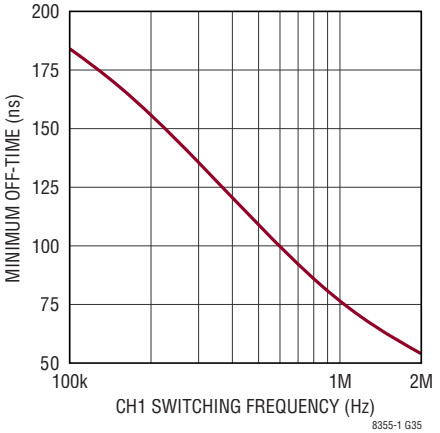
PWMTG Frequency vs Temperature



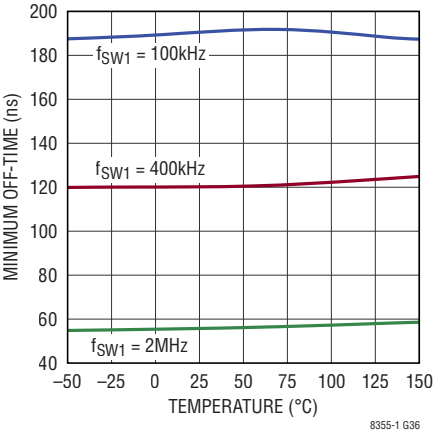
PWMTG Frequency vs Temperature



Minimum Off-Time vs CH1 Switching Frequency

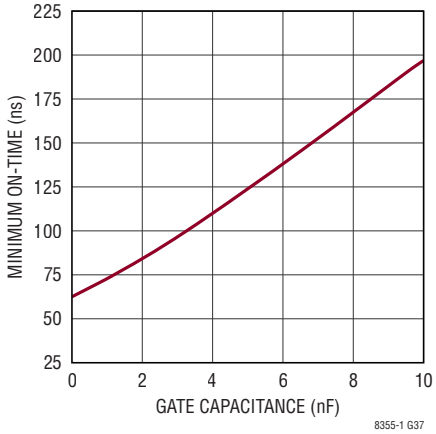


Minimum Off-Time vs Temperature

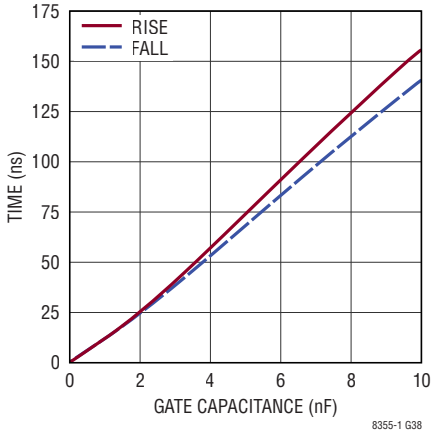


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

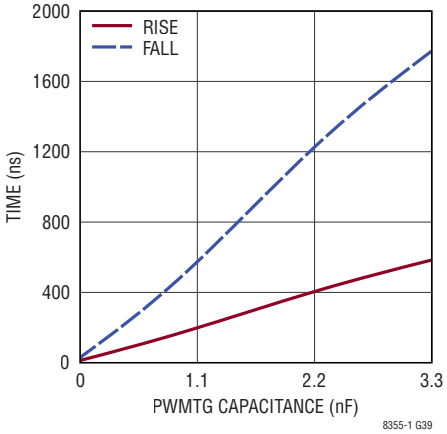
Minimum On-Time vs Gate Capacitance



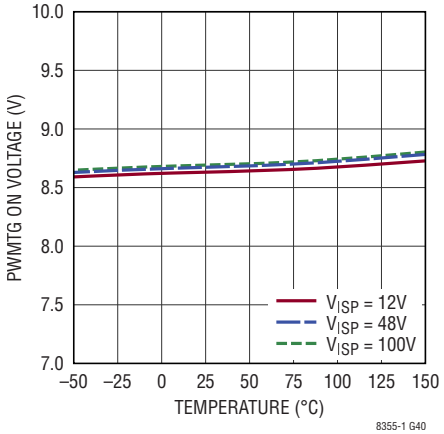
GATE Rise/Fall Time vs GATE Capacitance



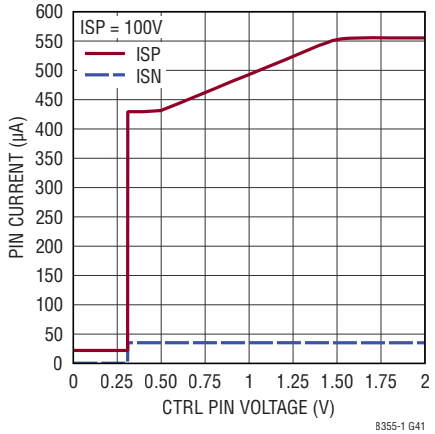
PWMTG Driver Rise/Fall Time vs PWMTG Capacitance



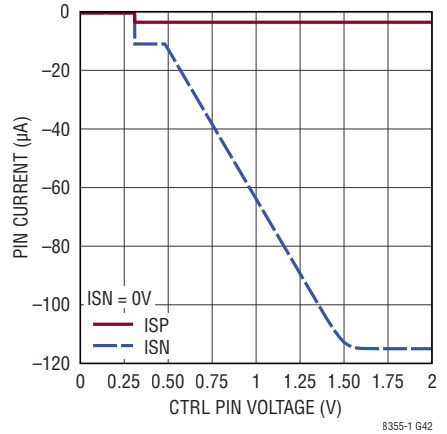
PWMTG ON Voltage vs Temperature



ISP/ISN Pin Current vs CTRL Voltage at ISP = 100V



ISP/ISN Pin Current vs CTRL Voltage at ISN = 0V



PIN FUNCTIONS

PWMTG1, PWMTG2 (Pins 1, 21): High Side Gate Driver for the External Series PMOS Switch of Each Channel. Use these pins to disconnect the load for PWM dimming as well as fault events. PWMTG drives the PMOS gate between ISP – 8.5V and ISP (typical) to cut off the flow of residual charge from the output capacitor when the LED load should be disconnected, as well as to prevent the long transient that would result from needing to recharge the output capacitor at the end of a long PWM off period. Leave open if unused. The voltage at PWMTG is limited to 8.5V (typical) below the voltage at ISP to protect the gate of the PMOS switch.

ISN1, ISN2 (Pins 2, 20): Kelvin connect this pin to the low side of the LED current feedback sense resistors $R_{ILED1,2}$ of each channel. Current through sense resistor, R_{ILED2} is 250mV/R_{ILED2} while CTRL2 > 1.5V and IADJ2 > 1.5V. It varies as [(CTRL2 – 0.48V) • (IADJ2 – 0.5V) –0.02V]/($4R_{ILED2}$) if the voltage at the CTRL2 and IAJD2 pins vary between 0.5V to 1.5V. The current through sense resistor R_{ILED1} is 250mV/R_{ILED1} while CTRL1 > 1.5V. It varies as (CTRL1 – 500mV)/($4R_{ILED1}$) if the voltage at the CTRL1 pin is between 500mV and 1.5V.

ISP1, ISP2 (Pins 3, 19): Kelvin connect this pin to the high side of the LED current feedback sense resistor R_{ILED} of each channel, see ISN1, ISN2 for more details. If the voltage difference $V_{ISP} – V_{ISN}$ ever exceeds around 670mV (typical), switching stops, PWMTG goes high to disconnect the load, and soft-start resets. After a cooldown period, the part will re-enter soft-start. See the Applications Information section for more details.

FB1, FB2 (Pins 4, 18): Output Voltage Feedback Pin for Each Channel. This pin is used for output voltage regulation and limiting. Tie this pin to a resistive voltage divider from the output voltage. When the voltage at FB reaches 1.2V (typical), the control loop will reduce the switch current to regulate the output voltage such that FB remains around 1.2V. If the voltage at FB exceeds 1.26V (typical), PWMTG is driven high and switching briefly stops. If the voltage at FB falls below 300mV (typical) after soft-start has finished, PWMTG is driven high, soft-start resets, and switching stops. After a cooldown period, the part will re-enter soft-start. See the Applications Information section for more info on the use of the FB pin for general applications.

V_{C1}, V_{C2} (Pins 5, 17): An Internal Error Amplifier Node Used for Compensation. Stabilize the loop by connecting a capacitor or RC network between this pin and ground for each channel. Read more in the Applications Information section for details about compensation.

CTRL1, CTRL2, IADJ2 (Pins 6, 8, 9): Two-Pin Analog Alternative to PWM Dimming. Tie CTRL1,2 and IADJ2 to V_{REF} or $INTV_{CC}$ to set R_{ILED} current to full-scale for each channel. The product of the offset CTRL2 and IADJ2 pin voltages sets the current in R_{ILED2} as [(CTRL2 – 0.48V) • (IADJ2 – 0.5V) – 0.02V]/($4R_{ILED2}$) when the voltages at CTRL2 and IADJ2 pins vary between 0.5V to 1.5V. The pin voltage of CTRL1 linearly sets the current in R_{ILED1} as (CTRL1 – 0.5V)/($4R_{ILED1}$) when the voltage at CTRL1 pin varies between 0.5V and 1.5V.

$\overline{FAULT1}$, $\overline{FAULT2}$ (Pins 7, 13): Open-Drain Fault Indication Pin Indicating Short LED, Open LED, Overvoltage and Overcurrent Faults for Each Channel. Tie these pins through 100k resistors to $INTV_{CC}$, or any supply less than 15V or use them as open-drain signals. LT8355-1 pulls these pins low to signal all reported fault events from each channel independently.

PWM1, PWM2 (Pins 10, 11): Pulse Width Modulation (PWM) Dimming Generation Control Pin for Each Channel. Connect an analog signal to this pin to use the internal exponential PWM dimming generator. When the voltages at these pins remain between 0.5V and 1.5V, the duty ratio of the internal dimming PWM generator will vary with the pin voltage. A linear ramp of voltage on the PWM pins between 0.5V and 1.5V lasting many PWMTG cycles at f_{SW}/1000 will result in an exponentially increasing PWM duty ratio. An external PWM signal can also drive this pin directly if the ON and OFF voltages are above 1.6V and below 0.4V, respectively. If PWM dimming is not used, tie these pins to $INTV_{CC}$ or V_{REF}.

RT (Pin 12): Connect a resistor between this pin and ground to set the switching frequency and PWM dimming frequency. Do not connect anything but a resistor to this pin or the device may not function correctly.

PIN FUNCTIONS

V_{REF} (Pin 14): A 2V (Typical) Reference Voltage. It can supply a maximum of 2.5mA at room temperature, useful for resistor networks that set voltages across CTRL1,2; IADJ2; and PWM1,2 pins. The output is stable without a local bypass but, if needed, bypass this pin to ground with a 1µF capacitor. If no load is connected or unused, leave pin floating.

EN/UVLO (Pin 15): When the voltage at this pin falls below 1.25V (typical), switching stops and the part shuts down. A hysteresis of approximately 60mV is included when returning over 1.25V. Drive this pin high with a logic level greater than 1.4V or low with a logic level below 0.3V for simple ON/OFF functionality or tie it through a resistive voltage divider to V_{IN} for a precise input undervoltage shutdown threshold. For all uses of this pin, ensure that the minimum Thevenin equivalent resistance is 20k.

V_{IN} (Pin 16): Input Supply Pin. Must be locally bypassed.

$INTV_{CC}$ (Pin 22): Voltage Supply Used by Internal Circuits. Tie a capacitor from this pin to ground. It requires a minimum capacitance of 2.2µF; but considering temperature and voltage coefficients, 4.7µF is recommended. The typical $INTV_{CC}$ voltage is 7.5V, and a 16V rated capacitor will usually be appropriate. This pin is not intended for use as a power source for external loads and connecting it to certain external loads may interfere with operation of the device. Using the $INTV_{CC}$ pin for any purpose other than those described in the Applications Information section is not recommended.

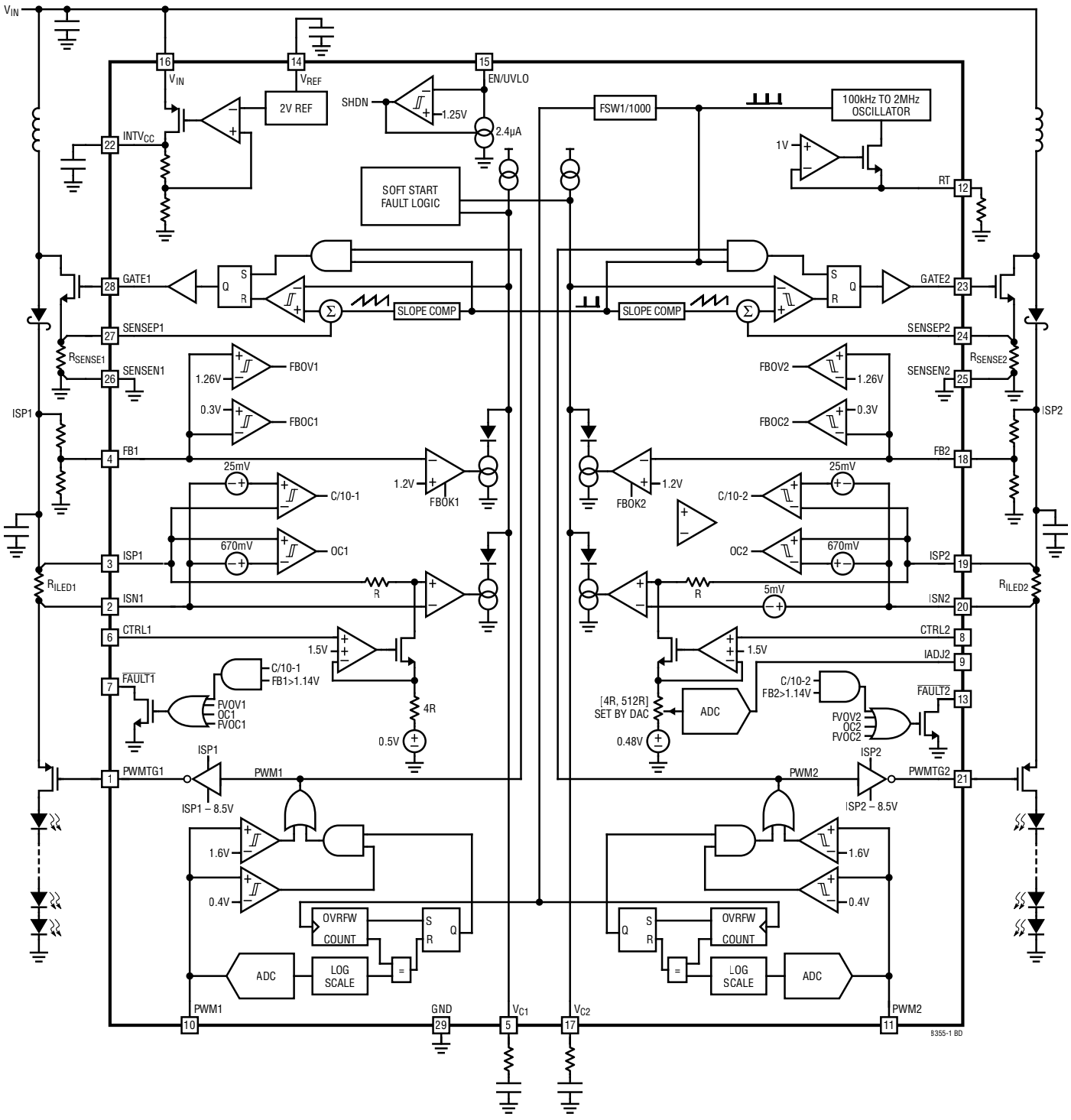
SENSEN1, SENSEN2 (Pins 26, 25): Kelvin connect this pin to the negative side of the switch current sense resistor for each channel. For more information about this, see the PCB layout guidelines in the Applications Information section.

SENSEP1, SENSEP2 (Pins 27, 24): Kelvin connect this pin to the positive side of the grounded switch current sense resistor for each channel. For more information about this, see the PCB layout guidelines in the Applications Information section.

GATE1, GATE2 (Pins 28, 23): External NMOS Power Switch Gate Driver for Each Channel. Connect this pin to the gate of an NMOS whose source is connected to the switch current sense resistor.

GND (Pin 29 Exposed Pad): Ground. Solder the exposed pad directly to the ground plane.

BLOCK DIAGRAM



OPERATION

The LT8355-1 is a dual-channel constant-frequency, constant-current/constant-voltage (CC/CV) boost power stage controller. The operation of the part can be best understood by looking at the Block Diagram. The controller can implement boost, SEPIC, buck mode or buck-boost mode LED drivers. At the beginning of every clock cycle, the clock signal sets an SR-latch controlling the gate driver. The external NMOS switch turns on and connects the inductor to ground. The positive voltage drops across the inductor results in linearly increasing current in the inductor. The switch will remain on until the current comparator resets it. This reset will occur when the switch current, as measured by the switch current sense resistor, exceeds the internal demand current. This demand current comes from the error amplifier of each respective channel. The external LED current sense resistor used to program load current drives the error amplifier. The voltage drop across the sense resistor multiplied by the amplifier's transconductance establishes the demand current. Without a forced offset, the error amplifier regulates the load to zero current based on the voltage across the LED current sense resistor.

To establish the positive offset in the error amplifier needed to program the LED current, a small current is intentionally pulled from only one input of the amplifier through an internal series resistor. The CTRL1,2 and IADJ2 pins establish this offset current by varying the voltage dropped across a second internal resistor to GND. Changing the CTRL1,2 pin voltage will vary the voltage dropped across the second internal resistor, while changing the IADJ2 pin voltage will change the value of that resistor for channel 2. This varies the LED current sense resistor regulation voltage between true zero and 250mV.

During constant-current operation, the FB pin provides overvoltage protection. When the FB pin voltage is below its regulation threshold, the FB amplifier has little effect on demand current. However, as the FB pin voltage approaches 1.2V, the FB amplifier has an increasingly pronounced effect, until it eventually dominates the demand current. If the FB pin voltage exceeds the regulation threshold by 60mV (typical), the part detects an overvoltage event. Similarly, if the voltage at the FB pin ever falls below 300mV (typical, excluding startup) then the part detects a short LED event.

Fast overcurrent protection relies on a separate signal path than the main LED current sense amplifier. If the LED current sense resistor voltage ($V_{ISP} – V_{ISN}$) exceeds 670mV (typical), switching stops. This event causes a brief interruption of switching while soft-start is reset, followed by a soft-start of the switching.

Four different methods for dimming the LED load are provided with LT8355-1. First, the voltages at the CTRL1,2 and IADJ2 pins, which set the LED current sense resistor regulation threshold for each channel, provide continuous, analog dimming of the LED load. In addition, two methods of PWM dimming exist. The first, external PWM, relies on a user-provided PWM signal. This signal drives the PWM pin, directly turning on and off the LED load. This method can achieve dimming ratios of 20,000:1 at 100Hz PWM frequency. Alternatively, the part can generate the PWM signal internally from an analog control signal at the PWM pin.

The internal dimming PWM generator selects one of 128 predetermined duty ratio values based on the analog voltage at the PWM pin. An exponential relationship exists between the PWM pin voltage and these duty ratio values. For example, consider a voltage at the PWM pin starting at 0V. When the voltage increases until the duty ratio is 9.6%, further increasing by 7.8mV(typical) will change the duty ratio to 10%. By the time the voltage is high enough to set 96% duty, the same 7.8mV (typical) increase will move the duty ratio up to 100%. A straight ramp at the PWM pin lasting many PWMTG dimming periods as set by R_T will create an exponentially increasing PWM duty ratio for the LED load.

APPLICATIONS INFORMATION

Introduction

LT8355-1 provides a variety of features to enable a wide range of application options. Due to the small package size and pin count, many pins perform more than one function. The simplest LT8355-1 application is realizable in only a few off-chip components and with very few design choices on the part of the user. To fully utilize the capability of the part, however, requires a good understanding of how the individual features play together. The detailed explanations of each feature below along with several example application circuits will help with developing a good understanding of the part.

Programming the LED Current

Full-scale current through the LED string is easily programmed using a single resistor (R_{ILED}) connected in series with the LED string. For most applications, the LED current sense resistor should be placed on the high side of the LED string; and Kelvin connected to LED current sense pins ISP and ISN for each channel. The loop will regulate a drop of 250mV across the LED current sense resistor, scaled by the voltage at the CTRL1,2 and IADJ2 pins, as discussed later. Choose a resistor with sufficient power dissipation capability for the programmed LED current. For LED currents less than 1.5A, a 0.5W resistor will usually suffice. Since the loop regulates the voltage across R_{ILED}, typical full-scale load current (I_{FS}) is defined in Equation 1.

$$I_{FS} = \frac{1}{4R_{ILED}} A \quad (1)$$

For the best performance and protection, sense at the highest potential in the LED string, and tie the source of the external PWM dimming PMOS to ISN. More details on the PWM dimming PMOS will be discussed later. Note that the loop can regulate LED current when the voltage at ISP is 0V, but a ground sensing configuration is not desirable for many applications. For more information see the Low Voltage (SEPIC) Start-Up section.

Adjusting LED Current with CTRL1,2 and IADJ2 Pins

The CTRL1,2 and IADJ2 pins provide an analog alternative to PWM dimming. The value of the voltage regulated across the LED current sense resistor can be adjusted with the CTRL1 pin for channel 1, and CTRL2 and/or IADJ2 pins for channel 2. As the voltage present at either pin is independently varied, the regulated voltage drop across the LED current sense resistor varies from 0V to 250mV. The system will supply no current if the CTRL1,2 pins voltage falls below 500mV or the IADJ2 pin voltage falls below 500mV, and will continue to supply full-scale current if the voltage at the CTRL1,2 pins exceed 1.5V and the IADJ2 pin exceeds 1.5V. The total LED current, I_{LED}, taking the effects of the CTRL pin into account is shown in Equation 2a and Equation 2b:

$$I_{LED1} = \frac{V_{CTRL1} - 0.5}{4R_{ILED1}} A \quad (2a)$$

$$I_{LED2} = \frac{(V_{CTRL2} - 0.48)(V_{IADJ2} - 0.5) - 0.02}{4R_{ILED2}} A, \quad (2b)$$

$$0.5V < V_{CTRL1-2}, V_{ADJ2} < 1.5V$$

The IADJ2 feature intentionally adds a small offset to ensure that true zero can be reached for LED current regulation. As a result, some combinations of CTRL2 and IADJ2 near the bottom of the range will result in no current flowing in the load. Note that the CTRL1,2 and IADJ2 pins can also be used for PWM by driving either with a digital signal whose low value is below 300mV for CTRL1,2 and 500mV for IADJ2; and whose high value is above 1.6V. Figure 1 shows how CTRL pin voltage affects LED current for varying values of IADJ2 for channel 2.

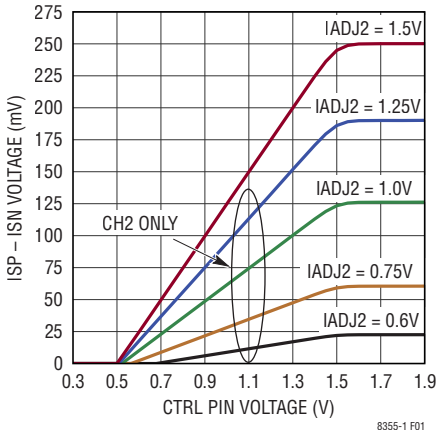


Figure 1. $V_{ISP} – V_{ISN}$ vs CTRL1,2 and VIADJ2 Pin Voltage

APPLICATIONS INFORMATION

Setting the Output Regulation Voltage

In addition to output current regulation, LT8355-1 can also provide output voltage regulation. The loop will go into voltage regulation mode when the voltage at the FB pin of each channel approaches 1.2V, regulating output voltage will reduce LED current below its programmed value. Voltage regulation mode is primarily included as a protection feature, allowing the part to gracefully manage some faults such as an open LED string. To set the output regulation voltage, connect a resistive voltage divider from the output voltage to FB as shown in Figure 2. Choose R_{FB1} and R_{FB2} to set the output voltage according to Equation 3.

$$V_{OUT} = \left(1 + \frac{R_{FB1}}{R_{FB2}}\right) \bullet 1.2V \quad (3)$$

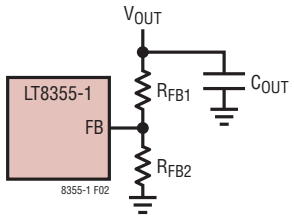


Figure 2. Voltage Feedback Network

It is important that the divider should be Kelvin connected to the output capacitor, as shown in Figure 2. The resistors R_{FB1} and R_{FB2} should be chosen such that their total value is between 1k and 1M. Be sure to keep resistor power dissipation capabilities in mind with higher output voltages.

In some configurations, such as buck mode, where the load voltage is not directly referred to ground, a level shifter may be needed to use constant-voltage mode control. Figure 3 shows an example circuit to accomplish output voltage control for buck and buck-boost topologies.

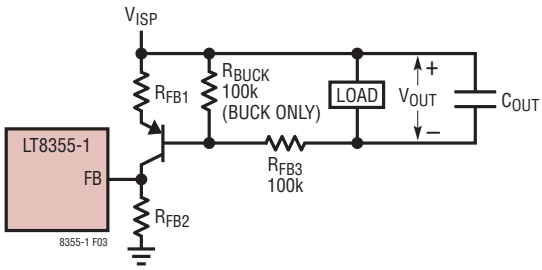


Figure 3. Voltage Feedback Network with Level Shifter

Choose RFB1, RFB2, RFB3, and R_{BUCK} to set the output voltage according to Equation 4. Note the use of R_{BUCK} in buck mode operation to keep PNP properly biased when the input supply gets within 2V of the LED voltage. When not needed, set R_{BUCK} in Equation 4 to infinity.

$$V_{OUT} = \left(1 + \frac{R_{FB3}}{R_{BUCK}}\right)\left(V_{EB} + \frac{R_{FB1}}{R_{FB2}} \bullet 1.2V\right) \quad (4)$$

If the open LED clamp voltage is programmed correctly using the resistor divider, then the FB pin should never exceed 1.12V when LEDs are connected.

Setting Switching and PWM Frequency

To program LT8355-1's switching frequency, connect a single resistor to ground from the RT pin. Use Equation 5 to approximate a starting value for the RT pin resistor, or Table 1 to use suggested values. It is important to connect only a resistor to GND on the RT pin.

$$R_T = \frac{4.4 \bullet 10^{10}}{(f_{SW1})^{1.06}} \quad (5)$$

Table 1. R_T Values for Selected Switching Frequencies

CH1 SWITCHING FREQUENCY	R_T VALUE
102kHz	215kΩ
200kHz	105kΩ
250kHz	84.5kΩ
300kHz	69.8kΩ
350kHz	59kΩ
400kHz	51.1kΩ
1MHz	19.1kΩ
1.95MHz	9.09kΩ

Albeit switching frequency of CH2 is also determined by the R_T value; to achieve high PWM dimming ratios, each channel has an independent switching frequency. For this reason, CH2 switches at a minimum of 5.5% faster than CH1's switching frequency to reduce audible noise.

During start-up, the switching frequency is reduced to allow sufficient switch OFF time, especially for 2MHz operation, so that inductor current can ramp below current limit when there is minimal voltage across the inductor during the OFF time. This condition is encountered

APPLICATIONS INFORMATION

at start-up or after faults, when the output is still low. During start-up, or when restarting after faults, switching frequency will drop to around 20% of its nominal value, and step-up over the duration of around 256 times the nominal switching period. For more information about this, see the Soft-Start section.

The internal dimming PWM generator clock runs at approximately f_{SW1}/1000. Spread spectrum frequency modulation for the switch clock does not affect the PWM generator clock, which continues to run at $f_{SW1(MIN)}$/1000.

Pulse Width Modulation (PWM) Dimming

Pulse width modulation (PWM) allows high dynamic range dimming of the LED load. When using PWM dimming, a pulse train with duty ratio proportional to desired LED current controls the load. During ON periods, the part operates normally. During OFF periods the part stops switching. While the part is not switching, the compensation node is high impedance to minimize changes to the compensation capacitor voltage. This reduces transient settling time when the next ON period arrives. In addition to this, the LT8355-1 provides an optional load disconnect. Disconnecting the load makes turn-off much faster, as the output capacitor does not continue to conduct current into the load. Transient settling time is also shorter when turning back ON, as the output capacitor's state is less affected by the load. To use the external load disconnect, tie a PMOS in series with the load such that the source of the PMOS connects to the ISN node, and the drain to the LED load. Connect the gate of the PMOS to the PWMTG pin. The voltage at the PWMTG pin will vary between V_{ISP} and V_{ISP} – 8.5V (typical) to turn the PMOS off and on. Note that this configuration works for any of the supported power stage topologies. For more information on power stage topologies, see the Typical Applications section.

The PWM1,2 pins allow two modes of PWM dimming. The first mode is external PWM. In this mode, a digital signal created by some other device, such as a microprocessor, drives the PWM1,2 pins. This PWM signal directly controls the part: when this signal is high, the corresponding channel runs, when this signal is low, the corresponding channel does not run, and disconnects the load if an external PMOS is used. Tying the PWM1,2 pins to $INTV_{CC}$ or V_{REF} results in continuous, uninterrupted operation. Conversely, tying the PWM1,2 pins to ground results in the system remaining idle indefinitely. External PWM dimming can support ON periods shorter than 500ns, allowing a PWM dimming dynamic range of 20,000:1 at 100Hz. Careful design of the wiring, including short cabling to reduce parasitic inductance, to the LED load improves turn on speed and regulation accuracy for brief (<1µs), high current (>0.5A) pulses. While sub-microsecond PWM dimming ON times are supported by LT8355-1, very brief OFF times (<0.3µs) are not supported. This means that negative going glitches on the CTRL1,2; IADJ2; and PWM1,2 pins should be avoided. High dynamic range PWM dimming can produce a single pulse of LED current lasting longer than a single nominal PWM on time which may be perceived as a flash. The second mode of PWM dimming is internal.

When using internal PWM dimming, the analog voltages at the PWM1,2 pins control the duty ratio of the PWMTG signal. The voltage range for internal PWM dimming is from 0.5V to 1.5V at the PWM1,2 pins. The internal PWM generator converts the voltages at the PWM1,2 pins to a 7-bit digital representation. The analog-to-digital converter responsible for this uses a linear scale, each code is around 7.8mV wide. Each 7-bit code corresponds to a unique duty ratio value. The values of duty ratio are separated exponentially. Refer to Figure 4 for a graphical representation of this relationship and Table 2 for recommended PWM voltage for selected PWM Duties.

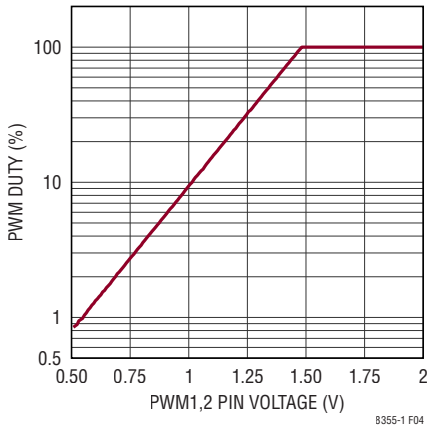


Figure 4. PWM Duty vs PWM1,2 Pin Voltages

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Table 2. Recommended PWM Voltage for Selected PWM Duties

PWM DUTY	PWM PIN VOLTAGE
1%	0.560V
5%	0.880V
10%	1.022V
14.75%	1.095V
20%	1.160V
25%	1.205V
33.3%	1.260V
50%	1.345V
76.5%	1.430V
100%	>1.6V

Spread Spectrum Frequency Modulation

The internal spread spectrum frequency modulation is always enabled in the LT8355-1. The modulating waveform is a triangle wave with steps at the positive and negative peaks. The modulation frequency is around 2kHz, and the switching frequency range is from 100% to 125% of the programmed value. If spread spectrum frequency modulation does not provide sufficient EMI attenuation even with good PCB design, consider slowing the switch turn-on speed by placing a 5Ω to 10Ω resistor between the GATE pin and the external NMOS switch. Please refer to the EVAL-LT8355-1-AZ evaluation circuit for a low EMI reference design and layout.

Maximum Duty Ratio

Since LT8355-1 uses a switch to connect an inductor from V_{IN} to ground, having a duty ratio of 100% would result in zero current flowing to the load. To prevent this situation, the part enforces a minimum off time. During this time, irrespective of load or demand, the switch turns off and allows the inductor current to flow into the load. The duty ratio can, therefore, never reach 100%. The maximum duty ratio varies with frequency. Due to the very wide range of input and output voltages offered by LT8355-1, a significant minimum off time of around 170ns exists to allow the switch node more time to slew up to the output. However, as switching frequency increases, this minimum off time folds back to 60ns to avoid limiting switch duty ratio unreasonably. For this reason, lower switching frequency (<400kHz) is recommended for high voltage (>60V) output applications. See Figure 5 for the typical maximum duty ratio as a function of switching frequency. Consider adding margin to account for variations in component values and LT8355-1 switching frequencies variations.

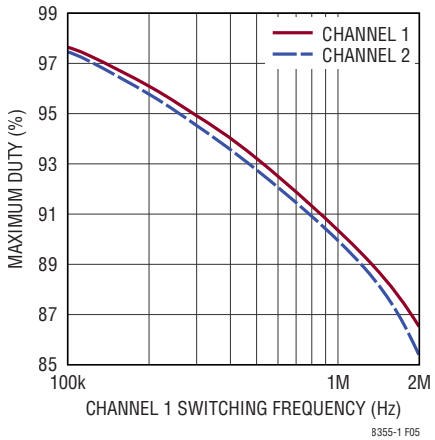

Figure 5. Maximum Duty as a Function of Switching Frequency

Maximum Switch Current

An important system parameter is the current limit. This prevents damage to system components by limiting the maximum instantaneous current conducting through the power switch. In a well-designed system, there will be margin between the maximum switch current to drive the LED load and the switch current limit. The LT8355-1 offers a current limit that has sufficient slope compensation so that reaching the current limit during line and load transients does not result in subharmonic oscillations. The switch current sense resistor programs the switch current limit as $0.1/R_{SENSE}$. Normally, the loop limits switch current based on the value of the sense resistor.

The loop will not typically command a voltage $V_{SENSEP} - V_{SENSEN}$ of more than 100mV. A good rule of thumb for setting maximum LED current for boost and buck-boost power stages appears in Equation 6. This equation assumes that the inductor selection used limits current ripple to around 20% of average current. For more information, see the Inductor Selection section.

$$I_{LED,MAX(20\%ripple)} = \frac{0.9 \bullet (100mV)}{R_{SENSE}} \bullet \frac{V_{IN}}{V_{ISP}} \quad (6)$$

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In the boost and buck-boost topologies, average switch current is related to average LED current by the ratio of V_{IN} to V_{ISP}. In the buck topology, average LED current approximately equals average inductor current. For this reason, the buck topology provides the highest possible LED current capability. The peak instantaneous switch current is thus the average LED current plus half of the peak-to-peak ripple current. This leads to the result in Equation 7 for buck mode current limit.

$$I_{LED,MAX(BUCK)} = \frac{100mV}{R_{SENSE}} - \frac{V_{LED}(V_{IN} - V_{LED})}{2 \bullet V_{IN} \bullet L \bullet f_{SW}} \quad (7)$$

For more information about power stage topologies, review the Typical Applications section. Since LT8355-1 offers a switch current limit that does not significantly change with duty ratio, the switch current limit can also limit the input current. Like the load current, the average input current and average switch current are not always the same. However, while the switch is on, the same instantaneous current flows in the switch and inductor. Because the inductor connects directly to the input, the peak input current, which is also the peak inductor current, cannot exceed the programmed switch current limit. Note that average input and load current will be strictly less than maximum peak switch current.

Loop Compensation

To ensure stable operation of the control loop realized by LT8355-1 it is necessary to limit the loop bandwidth. To do this, connect an RC network between the V_C pin and ground. A single capacitor can fulfill stability requirements if PCB area is extremely limited. The addition of a series resistor, however, will increase response speed and can also recover phase margin. A schematic diagram of the typical compensation scheme is illustrated in Figure 6. For many cases, a 1nF capacitor and 47k resistor will suffice. These are good values to start with for all applications.

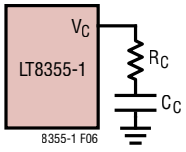

Figure 6. LT8355-1 Compensation Network

If settling time is unacceptable, ringing is too large, or the loop remains unstable the following steps can help. First, try reducing to 10k or eliminating the compensation resistor, R_C, especially if transient response is ringing or underdamped. Reducing the compensation resistor will cause longer settling time and larger deviation from load-steps such as PWM dimming. Next, increase the size of the compensation capacitor, C_C. This will reduce the frequency of the dominant (low frequency) pole and thereby the unity gain frequency. It will usually be possible to stabilize the loop given a big enough compensation capacitor. Increasing the compensation capacitor slows down the transient response to line and load activity. If the compensation capacitor cannot change by a small amount to achieve stability, consider instead decreasing the output capacitor or decreasing the inductor to separate the load pole and right half plane zero (for boost and SEPIC topologies).

Input and Output Capacitor Selection

The input and output capacitors supply the transient current for the power stage and should be placed and chosen according to the transient current requirements. An X7R type ceramic capacitor is usually a good choice for both input and output capacitor. Ceramic capacitors have a large voltage coefficient (i.e. lower capacitance when biased near their rated Voltage). It is generally a good rule of thumb to choose a capacitance 60% higher to compensate for the voltage coefficient. Consult the capacitor manufacturer to ensure capacitance is sufficient at the operating voltage.

The switching frequency, output current, inductor ripple current, and tolerable input voltage ripple are key parameters to consider when determining the value of the input capacitor. Typically, boost and SEPIC converters require a lower value input capacitor than buck mode converters. Use Equation 8 to estimate the value of the input capacitor. If the inductor is selected according to the directions in the Inductor Selection section, the input capacitance value can be calculated.

$$C_{IN(BOOST)} = \frac{20mV}{8 \bullet \Delta V_{IN} \bullet R_{SENSE} \bullet f_{SW}} \quad (8)$$

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For a boost converter switching at 200kHz, a 10µF input capacitor will often be sufficient. In the buck mode configuration, the input capacitor has large pulsed currents due to the current returned through the Schottky diode when the switch is off. The minimum input capacitance can be estimated as:

$$C_{IN(BUCK)} = \frac{I_{LED}}{\Delta V_{IN} \bullet f_{SW}} \quad (9)$$

For the buck case at 2MHz, a 10µF input capacitor would be appropriate to ensure less than 100mV of input voltage ripple with I_{LED} = 1.5A. Additional margin is recommended. In the buck converter case, it is important to place the capacitor as close as possible to the Schottky diode, external NMOS switch and the sense resistor. It is also important to consider the ripple current rating of the capacitor. For best reliability, this capacitor should have low ESR and ESL and have an adequate ripple current rating. Use Equation 10 to estimate the RMS input capacitor current for the buck converter case.

$$I_{CIN(RMS,BUCK)} = I_{LED} \bullet \sqrt{\frac{V_{LED}}{V_{IN}}\left(1-\frac{V_{LED}}{V_{IN}}\right)} \quad (10)$$

The selection of the output capacitor depends on load and power stage configuration. For example, a boost or buck-boost mode converter will require a much larger output capacitor than a buck mode converter for the same conditions. The boost and buck-boost mode configurations will also require similar low ESR and low ESL capacitors like the input capacitor of the buck mode case. Capacitor values will increase proportionally with decreasing switching frequency for the same ripple voltage. The equivalent resistance presented by an LED load is frequently low, so larger capacitors may be needed to further reduce voltage ripple. It is likely that the appropriate output capacitor value will fall between 10µF and 47µF. Use the example applications as a starting point for output capacitor selection.

Schottky Rectifier Selection

Choose a Schottky diode with reverse breakdown voltage greater than the maximum programmed output voltage and a current rating greater than the peak inductor current. Be sure to set the programmable switch current limit lower than the maximum forward current of the Schottky rectifier chosen. It is best to find a rectifier with low equivalent capacitance, around or below 500pF. Pay attention to reverse leakage current if the part is to be used in low frequency PWM dimming situations. The reverse leakage current can discharge the output capacitor. This can lead to lengthy turn-on transient effects that degrade maximum PWM dimming dynamic range. Not all applications will require the combination of high reverse voltage and forward current of this rectifier.

Inductor Selection

Select an inductor for use with LT8355-1 that has a saturation current greater than the switch current limit set by the switch current sense resistor as 0.1V/R_{SENSE}. Include some margin for the saturation current. Choose the inductor value based on desired ripple current given input and output voltage and switching frequency. Use Equation 11 to select an inductor with around 20% ripple.

$$L_{BOOST,\ BUCK\text{-}BOOST} = \frac{R_{SENSE} \bullet V_{IN}}{0.02V \bullet f_{SW}}\left(1-\frac{V_{IN}}{V_{ISP}}\right)$$
$$L_{BUCK} = \frac{R_{SENSE} \bullet V_{LED}}{0.02V \bullet f_{SW}}\left(1-\frac{V_{LED}}{V_{IN}}\right) \quad (11)$$

For boost configurations, $V_{ISP} = V_{LED}$; and for buck-boost mode, $V_{ISP} = V_{LED} + V_{IN}$.

Table 3 provides some recommended inductor vendors.

Table 3. Recommended Inductor Vendors

VENDOR	WEB
Sumida	www.sumida.com
Wurth Elektronik	www.we-online.com
Coiltronics	www.cooperet.com
Vishay	www.vishay.com
Coilcraft	www.coilcraft.com

Power PMOS Selection

For the PMOS to be used with PWMTG, select a device with drain-source voltage rating higher than the external

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NMOS switch and Schottky rectifier. The gate-source voltage rating should be higher than 12V. The drain current rating should be sufficient to conduct the full programmed LED current with some margin. Ensure that the PWMTG drive voltage of 8.5V will fully enhance the PMOS device. Be careful when selecting a PMOS to consider the effect that higher current ratings have on gate charge (Q_g). A very high Q_g PMOS will slow turn-on and turn-off times and can lead to offsets for very brief on-time PWM dimming (shorter than 500ns). A clamping diode might be necessary near PMOS's drain to prevent the drain ringing well below ground when being shorted to ground through a long cable.

Power NMOS Selection

Choose an external NMOS switch with breakdown voltage higher than the programmed output voltage by at least 20%. Select the forward current rating based on the load requirements and maximum current through the switch. Be sure to set the programmable switch current limit lower than the maximum rated forward current of the switch. Like the power PMOS, the gate charge of the external NMOS can impact performance. Very low Q_g MOSFETs (<1nC) can turn on quickly, potentially negatively impacting EMI performance. Conversely, very high Q_g MOSFETs (>100nC) can draw excessive current from the part's internal LDO regulator at higher switching frequencies.

Sense Resistors Selection

Select the LED and switch current sense resistors for power dissipation limits and PCB footprint convenience. The control loop will limit the steady state voltage dropped across the LED current sense resistor to 250mV (typical) and the switch current sense resistor to 100mV (typical). Large footprint resistors such as 2010 may be needed for high power applications. Be sure to Kelvin all sense resistors connections to the LT8355-1.

LED Fault Events

LT8355-1 provides a variety of fault detection to mitigate damage to external components. While LT8355-1 has many self-protection features, three LED types of faults (LED Short, Overvoltage and LED Overcurrent) will cause the part to immediately stop switching and, if an external PMOS is used according to instructions in the PWM Dimming section, disconnect the load from the output capacitor.

The LED overcurrent fault detection uses the LED current sense resistor R_{ILED}. If the voltage drop across the sense resistor is greater than 670mV (typical), an internal fault signal gets asserted. The LED Short fault senses load voltage. This can allow the detection of limited failures, such as one or two of the LEDs in a string becoming shorted. LT8355-1 senses the voltage at the FB pin and detects a LED Short fault if that voltage falls below 300mV (typical, excluding during start-up). It is important to note that the FB resistor divider must be in place to use the LED Short fault detection. After a successful start up, LT8355-1 can regulate $V_{ISP-ISN}$ to any setting provided that FB pin voltage stays above LED Short threshold. The Overvoltage fault occurs when the voltage at the FB pin exceeds 1.26V (typical). The FB resistor divider must be in place to take advantage of the over voltage fault protection. LT8355-1 clears faults and resumes switching depending on the type of fault. Switching resumes as soon as an overvoltage fault has cleared.

Recovery from Short LED and LED Overcurrent faults will enter soft-start as if it had just been turned on via the EN/UVLO pin. Upon successful completion of the soft-start process with no faults, the internal fault clears and normal operation resumes. The PWM dimming logic falling edge is ignored for both internal and external PWM until soft-start is complete or the control loop approaches steady state. Table 4 summarizes operating conditions that can trigger a fault, and/or turn off switching at the PWMTG1,2 and GATE1,2 pins.

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Table 4. Conditions and Effects on $\overline{FAULT}$, PWMTG and GATE

TYPE	CONDITION	$\overline{FAULT}$	PWMTG OFF	GATE OFF
Overvoltage	V_{FB} > 1.26V	Yes	Yes	Yes
Open LED	1.14V < V_{FB} < 1.26V and $V_{ISP-ISN}$ < 25mV	Yes	No	No
Short LED	V_{FB} < 300mV	Yes	Yes	Yes
Overcurrent	$V_{ISP-ISN}$ > 670mV	Yes	Yes	Yes
PWM OFF	PWM < 500mV, or CTRL < 300mV, or IADJ2 < 500mV	No	Yes	Yes
$INTV_{CC}$ UVLO	$INTV_{CC}$ < 4.3V	No	Yes	Yes
Thermal Shutdown	T_J > 170°C	No	Yes	Yes
Above Voltage Regulation	1.26V > V_{FB} > 1.20V	No	No	Yes
Above Current Regulation	0.7V > $V_{ISP-ISN}$ > 0.25V (or set by Equation 2a/2b)	No	No	Yes

Soft-Start

To prevent a surge of current at start-up, LT8355-1 uses an internal soft-start for each channel. This feature affects both current limit and switching frequency. At start-up, the system will switch at around 20% of the switching frequency f_{SW} with near zero current limit. As the clock runs, both constraints relax, leading to normal operation after around 256 switching periods. When a LED overcurrent occurs, or, in steady state, when short LED conditions occur, the part immediately stops switching and enters a cooldown period. The cooldown period lasts for at least 2048 switching periods. At the end of the cooldown period, the system attempts to start again, and enters soft-start as if it had just been powered on for the first time. Regardless of whether it is the first soft-start after power-on or a soft-start resulting from a fault condition, LT8355-1 will wait until the first PWM dimming pulse arrives before beginning to power on the system. This PWM pulse can be from an external source or from the internal dimming PWM generator. At the arrival of the first PWM pulse, soft-start begins, and operation continues until the system has reached steady state. Until the system either finishes soft-start or observes the internal control loop state nearing steady state, the PWM low logic state is ignored and the part runs continuously.

Using the EN/UVLO Pin

The EN/UVLO pin offers two modes of operation. First, it can be driven high (above 1.4V) or low (below 0.3V) to act as an enable pin, turning the part on and off. In addition to this, the pin can also be used to create an accurate external under voltage lockout (UVLO). To use this feature, connect the EN/UVLO pin to a resistive voltage divider from the V_{IN} pin to ground. Select resistors to program the desired minimum V_{IN} value for operation (see Equation 12 and Figure 7).

$$V_{IN(FALLING)} = 1.25V \bullet \left(1 + \frac{R_{UV1}}{R_{UV2}}\right)$$
$$V_{IN(RISING)} = 1.31V \bullet \left(1 + \frac{R_{UV1}}{R_{UV2}}\right) + 2.4\mu A \bullet R_{UV1} \quad (12)$$

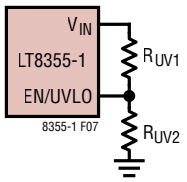

Figure 7. LT8355-1 Resistor Network for Accurate UVLO.

The EN/UVLO threshold has a hysteretic window to prevent oscillating between the on and off states. When the EN/UVLO pin falls below its falling threshold (1.25V typical), switching stops, soft-start is reset, and if an external PMOS is used according to instructions in the PWM Dimming section, the load is disconnected from the output capacitor. While the part is not enabled a current of 2.4µA flows into the EN/UVLO pin to allow for programmable hysteresis. Choose the value of the upper resistor R_{UV1} in the EN/UVLO voltage divider such that around 2.4µA(R_{UV1}) provides the desired hysteresis. When using the divider ratio, ensure that the equivalent Thevenin resistance is at least 20k. When driving this pin, add a 20k resistor in series.

Low Voltage (SEPIC) Start-Up

Certain power stage topologies, such as the SEPIC, may require the part to start-up in the condition where ISP

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and ISN are both near (or at) 0V. The LED current sense amplifier will continue to command the LED current programmed by CTRL1,2 and IADJ2 all the way down to 0V on ISP. However, recall that ISP provides the positive rail for the driver of the external disconnect PMOS. Therefore, the use of low side sensing of LED current is not recommended for applications that use PWM dimming or for any boost configuration applications requiring output short circuit protection.

Planning for Thermal Shutdown

The LT8355-1 will automatically shuts down when the internal temperature is above 170°C (typical). This shutdown is guaranteed to always be outside of the operating region of the device. The effects of thermal shutdown are like that of the load faults: switching stops, soft-start is reset, and if an external PMOS is used according to instructions in the PWM Dimming section, the load is disconnected from the output capacitor. The exposed pad is ground, and must be soldered to a good, large ground plane with many vias to aid thermal management. Since LT8355-1 controls power components and does not itself conduct any meaningful portion of the load current, power dissipation in the LT8355-1 may be lower than a monolithic converter. Power dissipation will increase with V_{IN} and switching frequency. Die temperature will increase with power dissipation. Higher ambient temperature applications will not be able to dissipate as much power, and high power dissipation in any condition may overstress die temperature.

PCB Layout Guidelines and Information

Printed Circuit Board (PCB) layout profoundly affects performance of all power applications. Proper electrical and thermal connection of the IC and power components with the outside world will mean the difference between success or failure of any system. Do not neglect spending adequate design time on the layout of any application PCB. The exposed ground pad on the bottom of the package must be soldered to a ground plane.

The switch current sense resistor R_{SENSE} should connect to a large, unbroken ground plane. The ground terminal of the switch current sense resistor should be Kelvin connected to the SENSE1,2 pins of the respective channel of LT8355-1. Connect the $INTV_{CC}$ bypass capacitor from the $INTV_{CC}$ pin directly to the exposed pad by the shortest route possible. Analog and control functions such as $V_{C1,2}$; PWM1,2; CTRL1,2; IADJ2; and V_{REF} should have a separate ground plane, which includes the exposed pad of the IC. The power and analog ground planes should meet only in a Kelvin connection to the exposed pad and at the power input to the PCB.

Be sure to design proper ground planes for power and analog functions within the application PCB. Ground planes should not be interrupted by other traces, and should be continuous, very wide sheets of copper. Connect the exposed pad of the IC to such a ground plane. Use as many vias as will fit in the exposed pad area to make the connection. Filled or capped vias may ease soldering for the exposed pad area. Do not copy any particular layout for the exposed pad connection, but instead use as many vias as will fit given the capabilities of the PCB fab house.

In addition to soldering down the exposed pad, it is critical to provide a good, robust layout for the power path. Use wide traces for V_{IN} and to connect to the load. Keep the LED and switch current sense resistors close to the IC and ensure that the ISP and ISN traces run as close to one another as possible. It is strongly recommended to not allow ISP and ISN to take different paths to the LED current sense resistor, but instead to keep them beside one another as much as possible. Minimize the total area of any switching node (SW) traces, keep the output capacitor and external catch diode as close as possible to the external NMOS switch and switch current sense resistor to help this. Finally, use wide traces to connect to the external PMOS switch, if used. Note, however, that the gates of both external switches should be connected by a narrow trace. Except for the external switch gates, avoid vias where possible in the power path. If vias are truly unavoidable, use many in parallel. Proper PCB layout is critical for suppressing radiated and conducted Electromagnetic interference (EMI). Minimizing the area of the SW node will decrease the amount of capacitance that the switch sees, and thus reduce the current spike seen during switching events. Failing to minimize the area of the so-called hot loop will dramatically degrade EMI

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performance. Keep the output capacitor and catch diode as close as possible to the external NMOS switch and switch current sense resistor to help this. For more information about hot loops see Analog Devices Application Notes AN136 and AN139.

An example 2-layer layout which takes the above considerations into account is provided in Figure 8. It is imperative that the layout of any PCB carefully consider the capabilities of the PCB manufacturer and other application constraints. The example provided here should guide the layout of an application PCB. If the application or manufacturing capabilities mandate a different layout, be sure to keep the above guidance in mind for all changes. Note that the 4-layer layout is recommended for best performance. Please refer to the EVAL-LT8355-1-AZ evaluation circuit for a 4-layer PCB reference layout design.

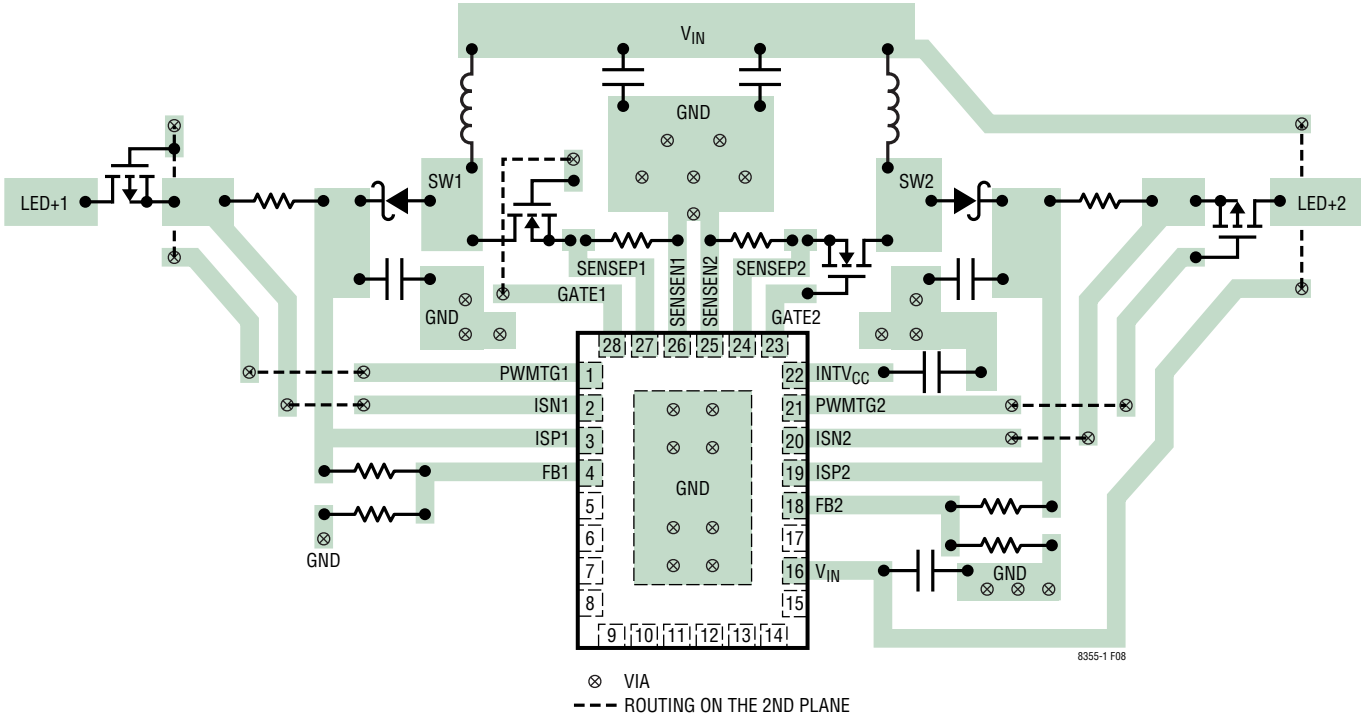
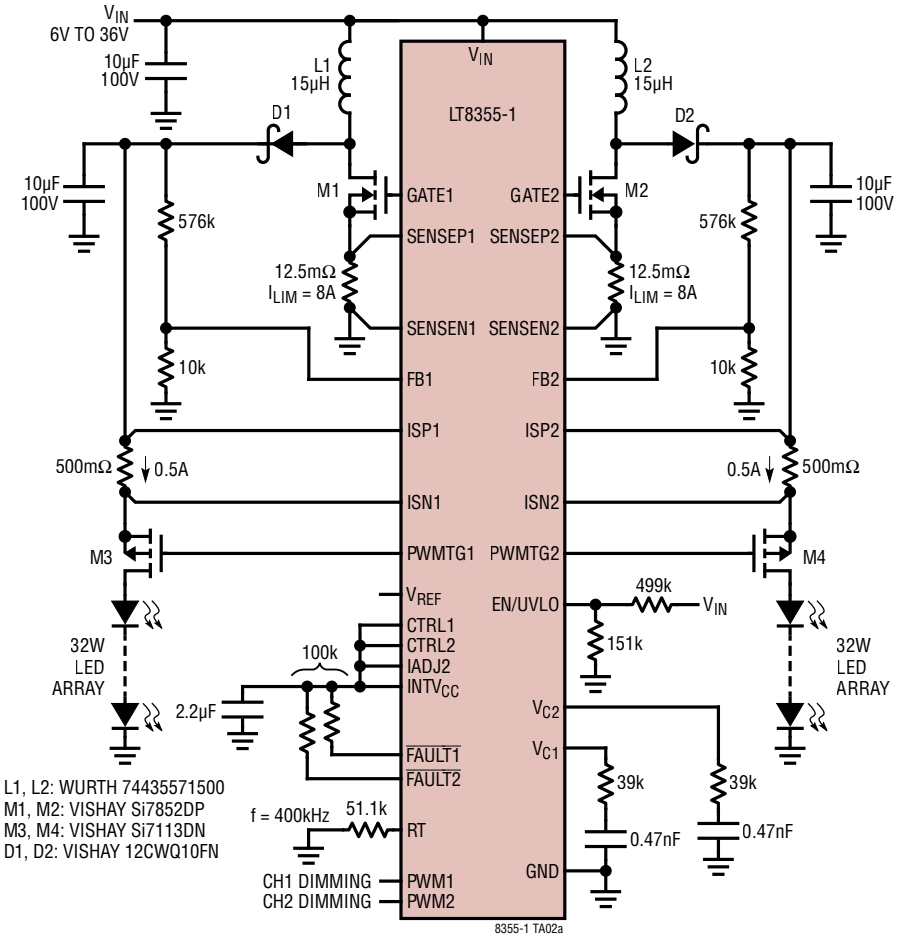


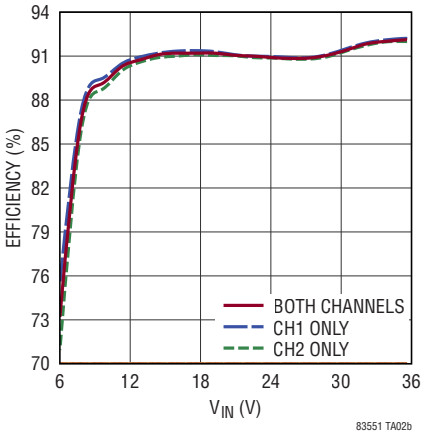
Figure 8. Dual Boost Reference Layout for LT8355-1

TYPICAL APPLICATIONS

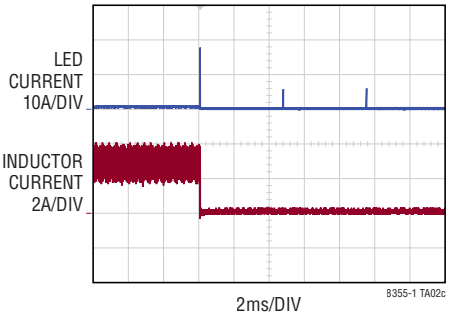
Dual 32W Boost LED Driver



Efficiency vs V_{IN} Voltage

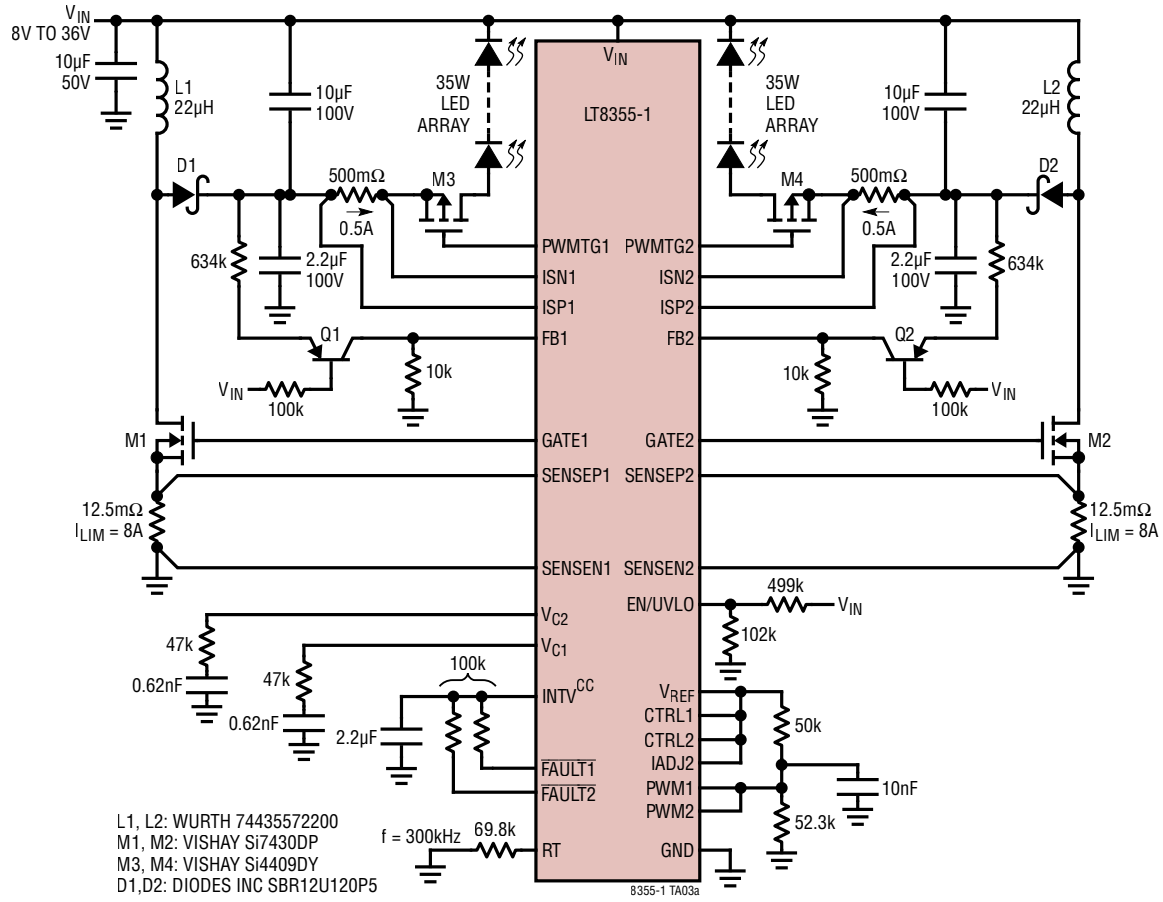


LED Short Fault Detection and Response

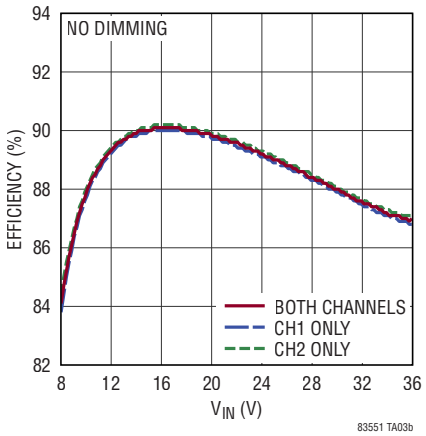


TYPICAL APPLICATIONS

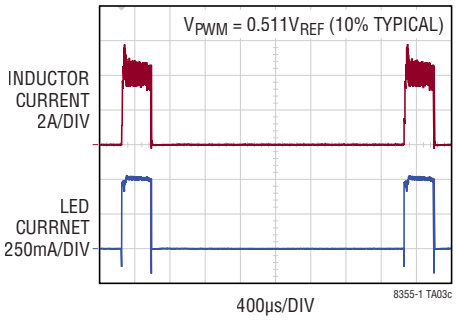
Dual 35W Buck-Boost Mode LED Driver



Efficiency vs V_{IN} Voltage

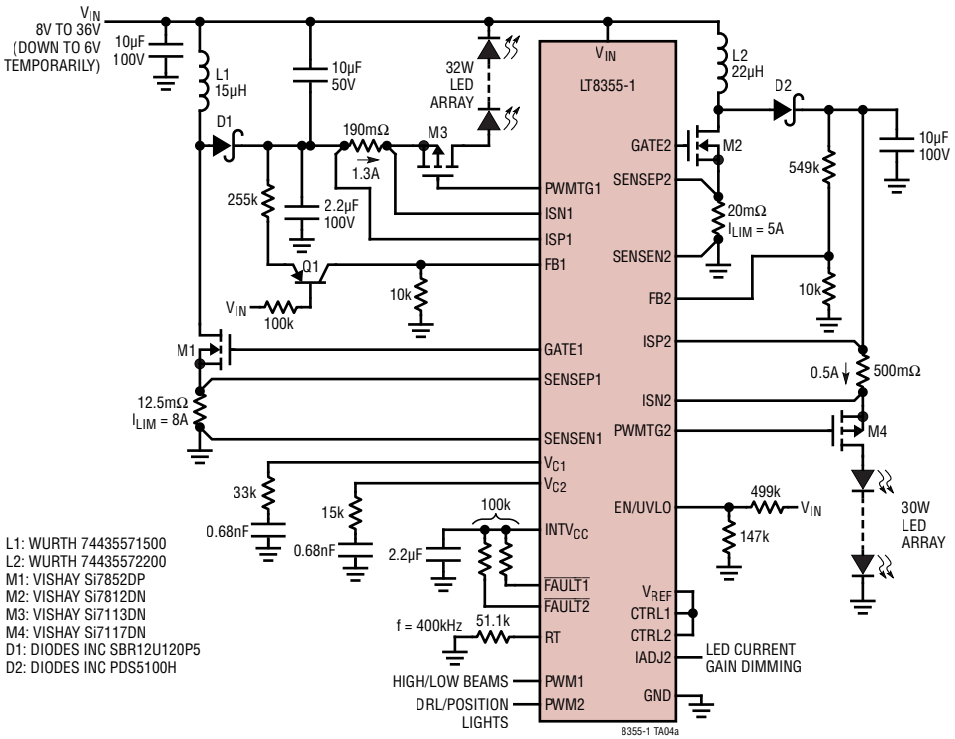


10% Internal PWM Dimming



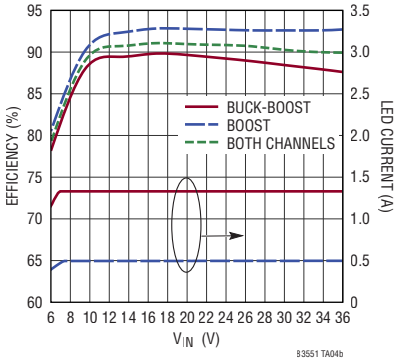
TYPICAL APPLICATIONS

Complete Automotive Headlamp Solution

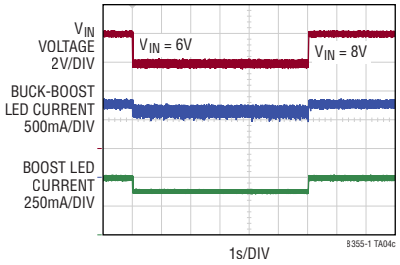


L1: WURTH 74435571500
L2: WURTH 74435572200
M1: VISHAY Si7852DP
M2: VISHAY Si7812DN
M3: VISHAY Si7113DN
M4: VISHAY Si7117DN
D1: DIODES INC SBR12U120P5
D2: DIODES INC PDS5100H

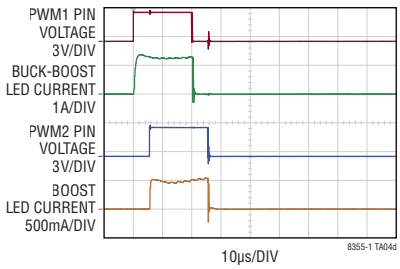
Efficiency vs V_{IN} Voltage



Cold Crank LED Regulation

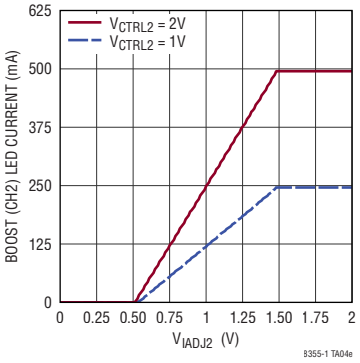


500:1 External PWM Dimming at 100Hz



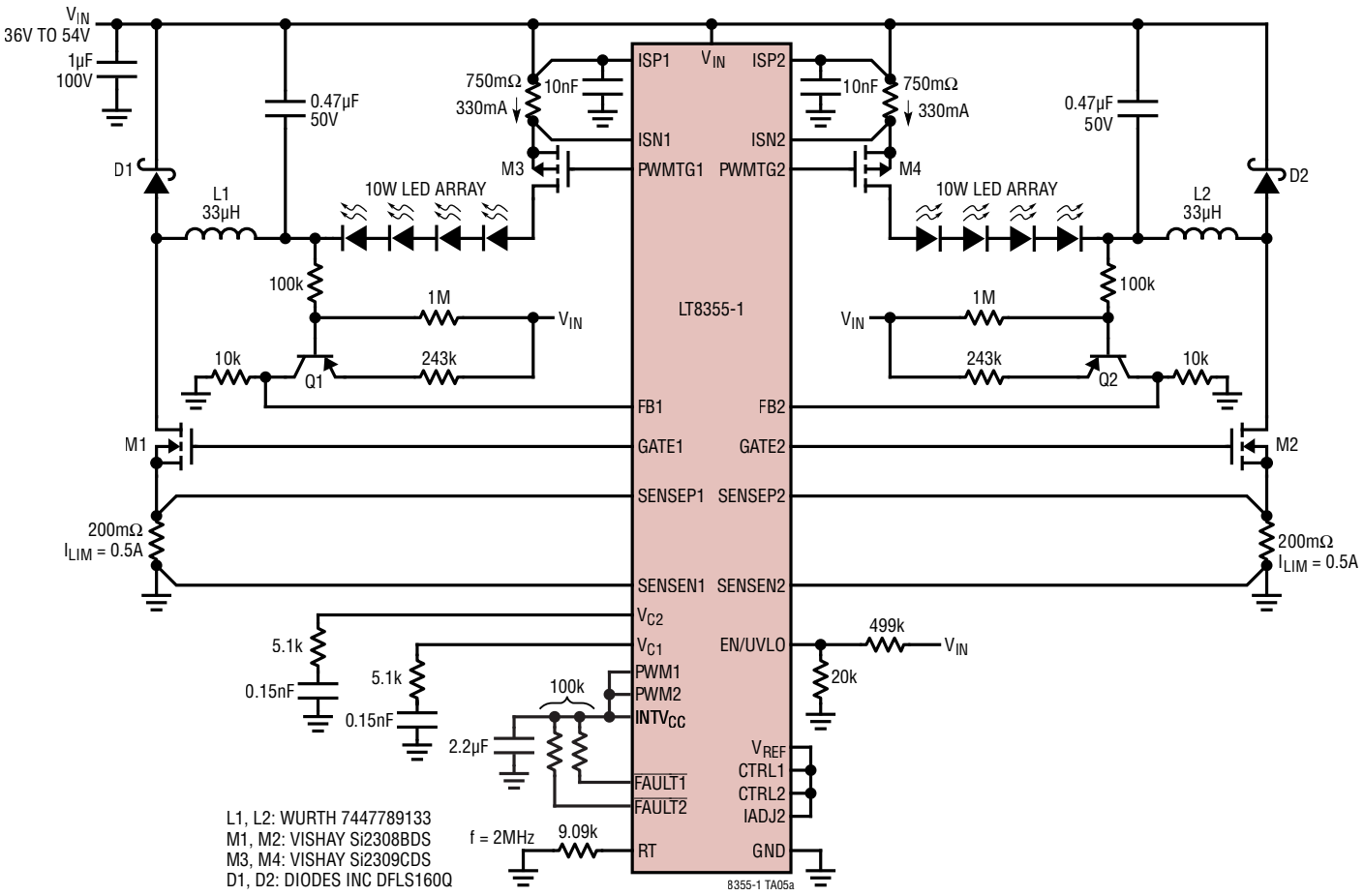
V_{IN} = 14V, INFINITE PERSISTANCE

Boost Channel LED Current vs V_{IADJ2}



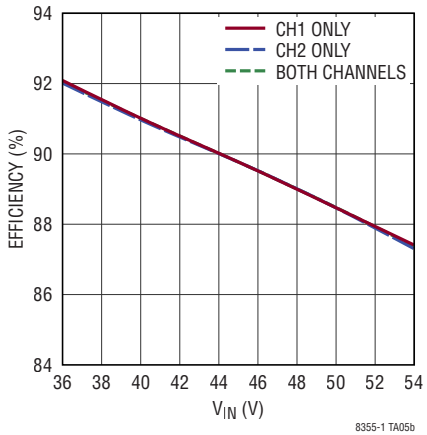
TYPICAL APPLICATIONS

Dual 10W Buck Mode High Switching Frequency (2MHz) LED Driver



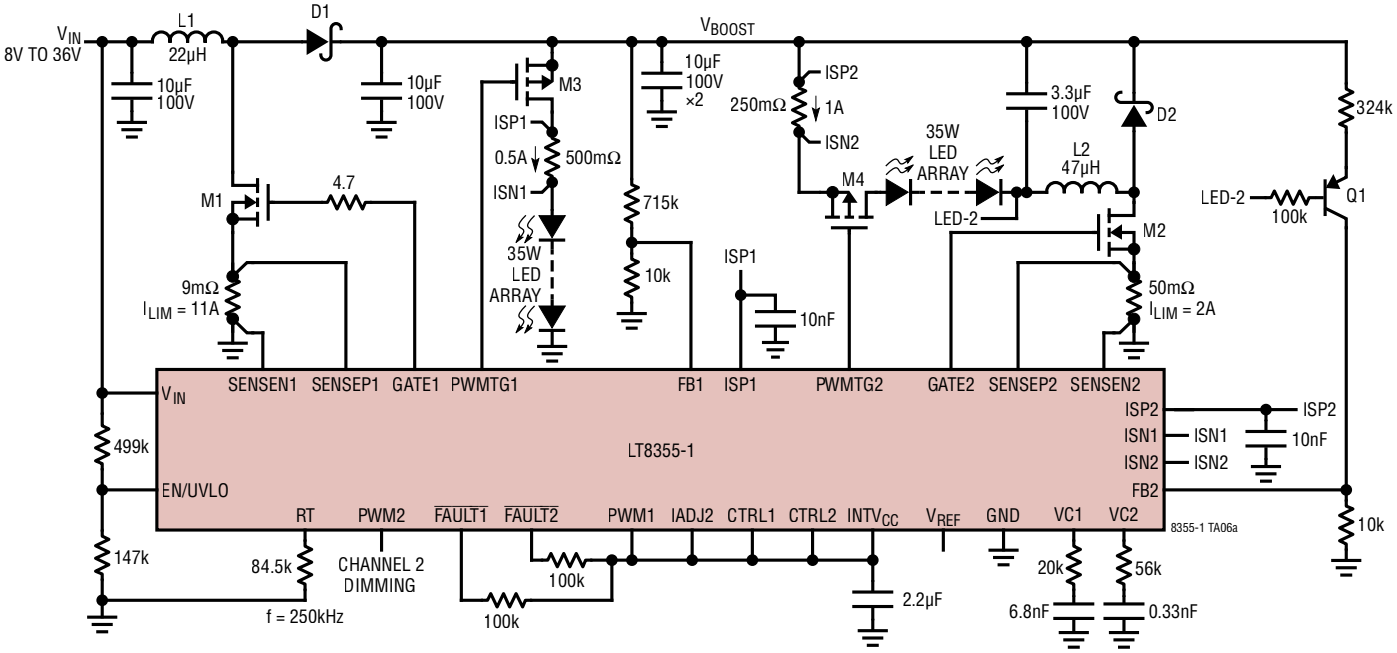
L1, L2: WURTH 7447789133
M1, M2: VISHAY Si2308BDS
M3, M4: VISHAY Si2309CDS
D1, D2: DIODES INC DFLS160Q

Efficiency vs V_{IN} Voltage



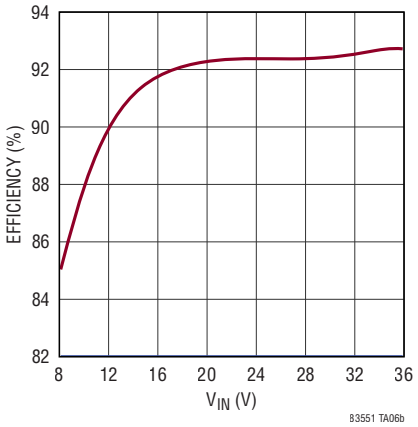
TYPICAL APPLICATIONS

Boost LED Driver as Pre-boost for Buck-Mode LED Driver

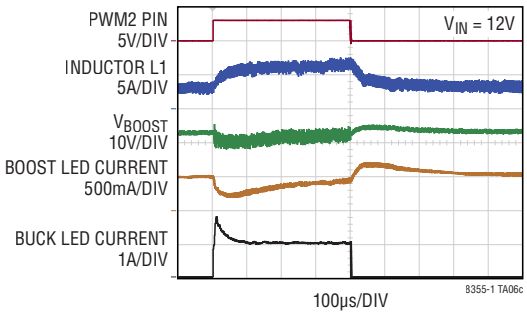


L1: COILCRAFT XAL1510-223MEB
L2: WURTH 74435574700
M1: INFINEON BSC160N10NS3-G
M2: VISHAY Si7810DN
M3: VISHAY Si7113DN
M4: VISHAY Si3437DV
D1: DIODES INC SBR12U120P5
D2: DIODES INC PDS5100H

Efficiency vs V_{IN} Voltage

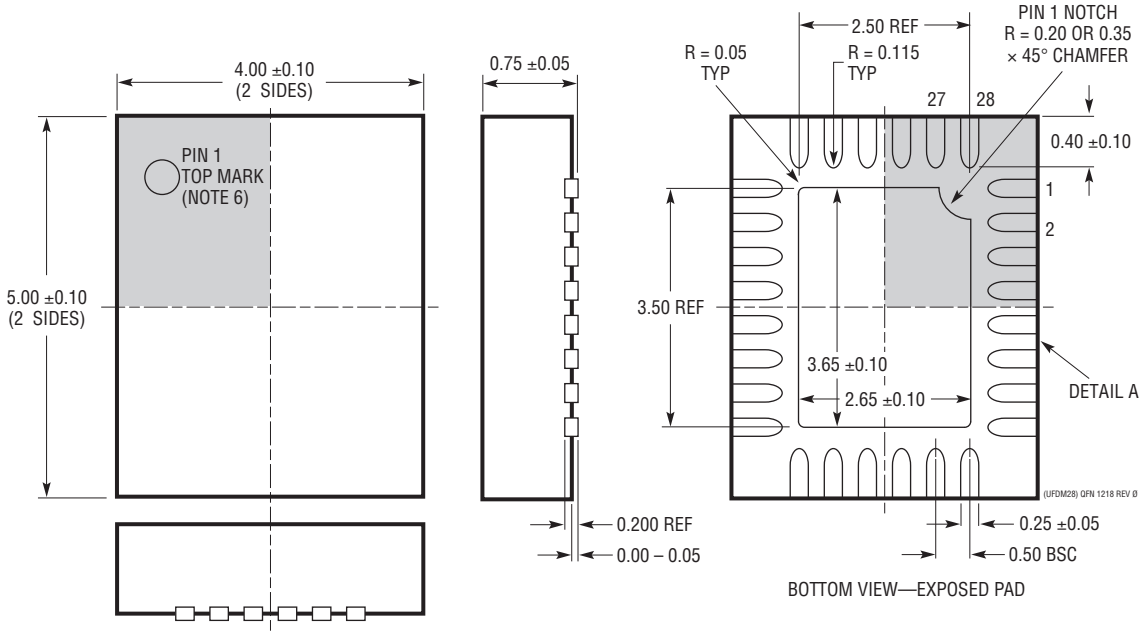


25:1 External PWM Dimming at 100Hz

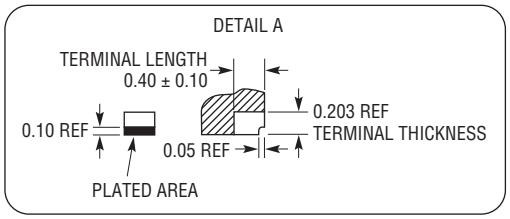


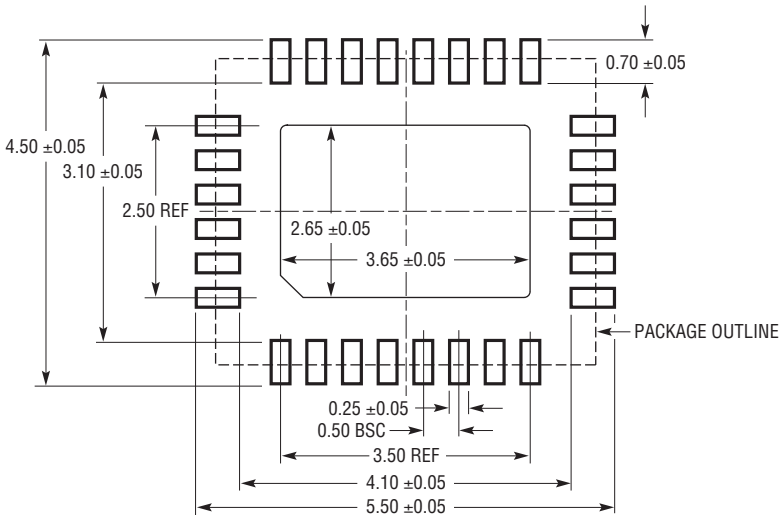
PACKAGE DESCRIPTION

UFDM Package
28-Lead Plastic Side Wettable QFN (4mm × 5mm)
(Reference LTC DWG # 05-08-1682 Rev Ø)



NOTE:
1. DRAWING NOT TO SCALE
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
4. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE





RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	12/22	Updated Pulse Width Modulation (PWM) Dimming section	16
		Updated LED Fault Events section	20