LT8391A

60V 2MHz Synchronous 4-Switch Buck-Boost LED Driver Controller

FEATURES

- **4-Switch Single Inductor Architecture Allows V_{IN} Above, Below or Equal to V_{OUT}**
- **Up to 95% Efficiency at 2MHz**
- **Proprietary Peak-Buck Peak-Boost Current Mode**
- **Wide V_{IN} Range: 4V to 60V**
- **Wide V_{OUT} Range: 0V to 60V (51V LED)**
- **±3% LED Current Accuracy**
- 2000:1 External and 128:1 Internal PWM Dimming
- High Side PMOS PWM Switch Driver
- No Top MOSFET Refresh Noise in Buck or Boost
- Adjustable and Synchronizable: 600kHz to 2MHz
- Flicker-Free Spread Spectrum for Low EMI
- Open and Short LED Protection with Fault Reporting
- Available in 28-Lead TSSOP with Exposed Pad and 28-Lead QFN (4mm × 5mm)
- AEC-Q100 Qualified for Automotive Applications

APPLICATIONS

- Automotive Head Lamps/Running Lamps
- High Frequency LED Lighting

DESCRIPTION

The LT®8391A is a synchronous 4-switch buck-boost LED controller that regulates LED current from input voltage above, below, or equal to the output voltage. The proprietary peak-buck peak-boost current mode control scheme allows adjustable and synchronizable 600kHz to 2MHz fixed frequency operation, or internal 25% triangle spread spectrum operation for low EMI. With 4V to 60V input, 0V to 60V output, and seamless low noise transitions between operation regions, the LT8391A is ideal for LED driver and battery charger applications in automotive, industrial, and battery-powered systems.

The LT8391A provides both internal (up to 128:1) and external (up to 2000:1) LED current PWM dimming with a high-side PMOS switch. Two CTRL pins provide flexible 20:1 analog dimming with ±3% LED current accuracy at 100mV full scale. Fault protection is provided to detect an open or short LED condition, during which the LT8391A retries, latches off, or keeps running.

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TYPICAL APPLICATION

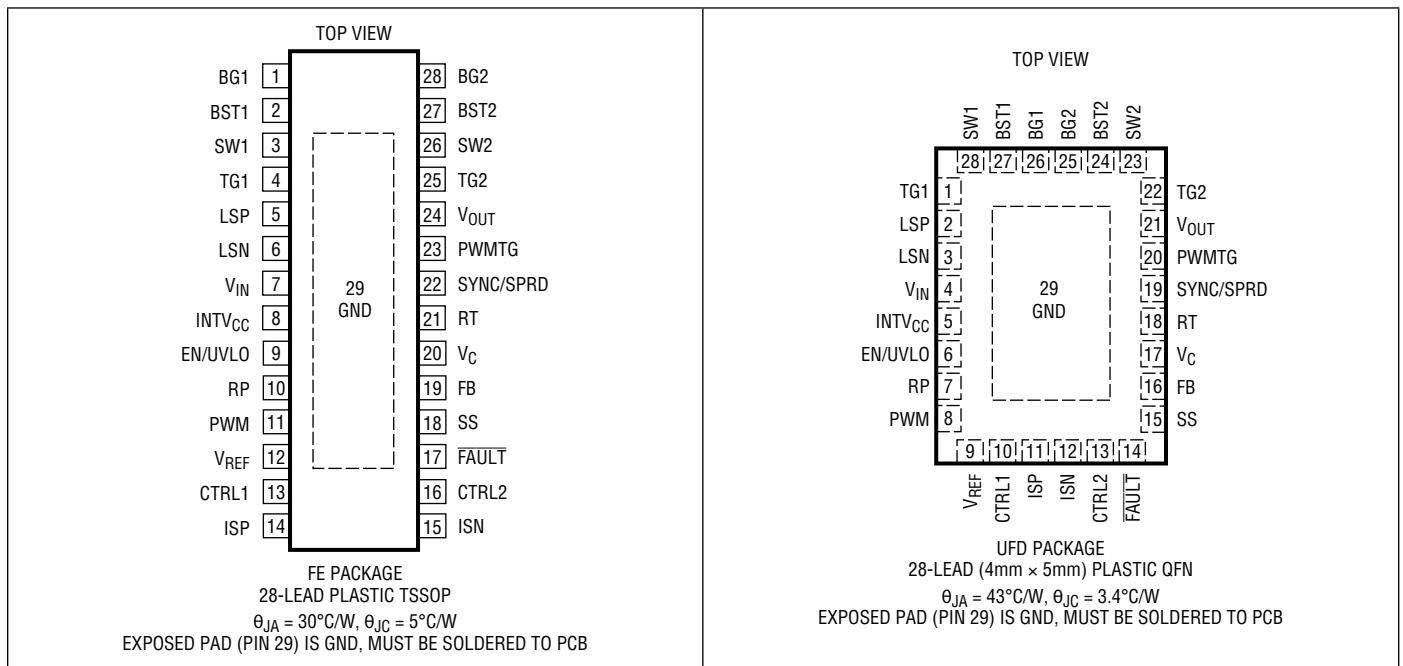**94% Efficient 24W (16V, 1.5A) 2MHz Buck-Boost LED Driver**

Efficiency vs V_{IN}
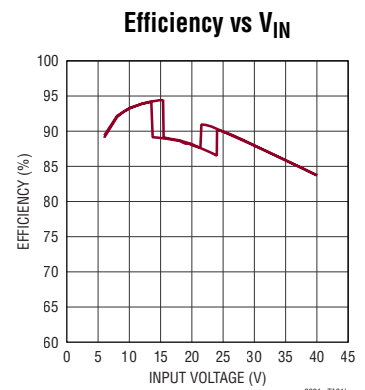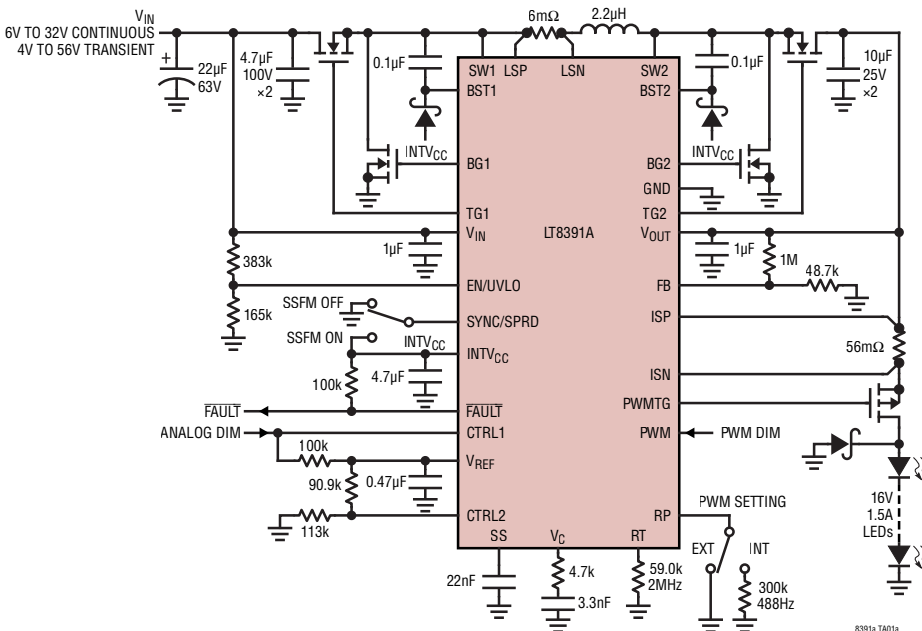
ABSOLUTE MAXIMUM RATINGS (Note 1)

V_{IN}, EN/UVLO, V_{OUT}, ISP, ISN 60V
(ISP-ISN) ....–1V to 1V
BST1, BST2...66V
SW1, SW2, LSP, LSN .... –6V to 60V
$INTV_{CC}$, (BST1-SW1), (BST2-SW2)...........................6V
(BST1-LSP), (BST1-LSN) 6V
FB, PWM, SYNC/SPRD, CTRL1, CTRL2, $\overline{FAULT}$...........6V

Operating Junction Temperature Range (Notes 2, 3)
 LT8391AE ....–40°C to 125°C
 LT8391AI ....–40°C to 125°C
 LT8391AH...–40°C to 150°C
 LT8391AJ...–40°C to 150°C
Storage Temperature Range ....–65°C to 150°C

PIN CONFIGURATION

TOP VIEW

BG1	1	28	BG2
BST1	2	27	BST2
SW1	3	26	SW2
TG1	4	25	TG2
LSP	5	24	V_{OUT}
LSN	6	23	PWMTG
V_{IN}	7	22	SYNC/SPRD
$INTV_{CC}$	8	21	RT
EN/UVLO	9	20	V_C
RP	10	19	FB
PWM	11	18	SS
V_{REF}	12	17	$\overline{FAULT}$
CTRL1	13	16	CTRL2
ISP	14	15	ISN

29 GND

FE PACKAGE
28-LEAD PLASTIC TSSOP
θ_{JA} = 30°C/W, θ_{JC} = 5°C/W
EXPOSED PAD (PIN 29) IS GND, MUST BE SOLDERED TO PCB

TOP VIEW

SW1 BST1 BG1 BG2 BST2 SW2
28 27 26 25 24 23

TG1	1	22	TG2
LSP	2	21	V_{OUT}
LSN	3	20	PWMTG
V_{IN}	4	19	SYNC/SPRD
$INTV_{CC}$	5	18	RT
EN/UVLO	6	17	V_C
RP	7	16	FB
PWM	8	15	SS

29 GND

9 10 11 12 13 14
V_{REF} CTRL1 ISP ISN CTRL2 $\overline{FAULT}$

UFD PACKAGE
28-LEAD (4mm × 5mm) PLASTIC QFN
θ_{JA} = 43°C/W, θ_{JC} = 3.4°C/W
EXPOSED PAD (PIN 29) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT8391AEFE#PBF	LT8391AEFE#TRPBF	LT8391AFE	28-Lead Plastic TSSOP	−40°C to 125°C
LT8391AIFE#PBF	LT8391AIFE#TRPBF	LT8391AFE	28-Lead Plastic TSSOP	−40°C to 125°C
LT8391AHFE#PBF	LT8391AHFE#TRPBF	LT8391AFE	28-Lead Plastic TSSOP	−40°C to 150°C
LT8391AEUFD#PBF	LT8391AEUFD#TRPBF	8391A	28-Lead (4mm × 5mm) Plastic QFN	−40°C to 125°C
LT8391AIUFD#PBF	LT8391AIUFD#TRPBF	8391A	28-Lead (4mm × 5mm) Plastic QFN	−40°C to 125°C
LT8391AHUFD#PBF	LT8391AHUFD#TRPBF	8391A	28-Lead (4mm × 5mm) Plastic QFN	−40°C to 150°C
AUTOMOTIVE PRODUCTS**				
LT8391AJFE#WPBF	LT8391AJFE#WTRPBF	LT8391AFE	28-Lead Plastic TSSOP	−40°C to 150°C
LT8391AHFE#WPBF	LT8391AHFE#WTRPBF	LT8391AFE	28-Lead Plastic TSSOP	−40°C to 150°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

**Versions of this part are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. These models are designated with a #W suffix. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 2). V_{IN} = 12V, $V_{EN/UVLO}$ = 1.5V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	V_{IN} Operating Voltage Range		●	4		60	V
	V_{IN} Quiescent Current	$V_{EN/UVLO}$ = 0.3V $V_{EN/UVLO}$ = 1.1V Not Switching			1 270 2.1	2 2.8	µA µA mA
	V_{OUT} Voltage Range		●	0		60	V
	V_{OUT} Quiescent Current	$V_{EN/UVLO}$ = 0.3V, V_{OUT} = 12V $V_{EN/UVLO}$ = 1.1V, V_{OUT} = 12V Not Switching, V_{OUT} = 12V		 20	0.1 0.1 40	0.5 0.5 60	µA µA µA

Linear Regulators

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	$INTV_{CC}$ Regulation Voltage	I_{INTVCC} = 20mA		4.85	5.0	5.15	V
	$INTV_{CC}$ Load Regulation	I_{INTVCC} = 0mA to 80mA			1	4	%
	$INTV_{CC}$ Line Regulation	I_{INTVCC} = 20mA, V_{IN} = 6V to 60V			1	4	%
	$INTV_{CC}$ Current Limit	V_{INTVCC} = 4.5V		110	145	190	mA
	$INTV_{CC}$ Dropout Voltage (V_{IN} − $INTV_{CC}$)	I_{INTVCC} = 20mA, V_{IN} = 4V			160		mV
	$INTV_{CC}$ Undervoltage Lockout Threshold	Falling		3.44	3.54	3.64	V
	$INTV_{CC}$ Undervoltage Lockout Hysteresis				0.24		V
	V_{REF} Regulation Voltage	I_{VREF} = 100µA	●	1.97	2.00	2.03	V
	V_{REF} Load Regulation	I_{VREF} = 0mA to 1mA			0.4	1	%
	V_{REF} Line Regulation	I_{VREF} = 100µA, V_{IN} = 4V to 60V			0.1	0.2	%
	V_{REF} Current Limit	V_{REF} = 1.8V		2	2.5	3.2	mA
	V_{REF} Undervoltage Lockout Threshold	Falling		1.78	1.84	1.90	V
	V_{REF} Undervoltage Lockout Hysteresis				50		mV

Control Inputs/Outputs

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	EN/UVLO Shutdown Threshold		●	0.3	0.6	1.0	V
	EN/UVLO Enable Threshold	Falling	●	1.196	1.220	1.244	V
	EN/UVLO Enable Hysteresis				13		mV
	EN/UVLO Hysteresis Current	$V_{EN/UVLO}$ = 0.3V $V_{EN/UVLO}$ = 1.1V $V_{EN/UVLO}$ = 1.3V		−0.1 2.2 −0.1	0 2.5 0	0.1 2.8 0.1	µA µA µA
	CTRL1, CTRL2 Input Bias Current	$V_{CTRL1/2}$ = 0.75V (Note 4), Current out of Pin		0	20	50	nA
	CTRL1, CTRL2 Dim-Off Threshold	Falling	●	190	200	210	mV
	CTRL1, CTRL2 Dim-Off Hysteresis				28		mV

PWM Dimming

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	External PWM Dimming Threshold	Rising, R_P = 30k	●	1.3	1.4	1.5	V
	External PWM Dimming Hysteresis	R_P = 30k			220		mV
	Internal PWM Dimming Duty Cycle	V_{PWM} = 1V, R_P ≥ 51k V_{PWM} = 1.5V, R_P ≥ 51k V_{PWM} = 2V, R_P ≥ 51k		 47 97		3 53	% % %
	Switching Frequency to Internal PWM Dimming Frequency Ratio	R_P = 51k R_P = 82k R_P = 130k R_P = 200k R_P = 300k			256 512 1024 2048 4096		

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 2). V_{IN} = 12V, $V_{EN/UVLO}$ = 1.5V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	RP Pin Current Limit	V_{RP} = 0V, Current out of Pin			40		µA
	Minimum V_{OUT} for PWMTG to be On	PWM dimming on			2.4	3	V
	PWMTG On Voltage $V_{(VOUT-PWMTG)}$	V_{OUT} = 12V		4.5	5	5.5	V
	PWMTG Off Voltage $V_{(VOUT-PWMTG)}$	V_{OUT} = 12V		−0.1	0	0.1	V
	PWM to PWMTG Turn On Propagation Delay	C_{PWMTG} = 3.3nF to V_{OUT}, 50% to 50%			90		ns
	PWM to PWMTG Turn Off Propagation Delay	C_{PWMTG} = 3.3nF to V_{OUT}, 50% to 50%			40		ns
	PWMTG Turn On Fall Time PWMTG Turn Off Rise Time	C_{PWMTG} = 3.3nF to V_{OUT}, 10% to 90% C_{PWMTG} = 3.3nF to V_{OUT}, 90% to 10%			300 10		ns ns
Error Amplifier							
	Full Scale LED Current Regulation $V_{(ISP-ISN)}$	$V_{CTRL1/2} \geq$ 1.35V (Note 4), V_{ISP} = 12V $V_{CTRL1/2} \geq$ 1.35V (Note 4), V_{ISP} = 0V	● ●	97 97	100 100	103 103	mV mV
	9/10th LED Current Regulation $V_{(ISP-ISN)}$	$V_{CTRL1/2}$ = 1.15V (Note 4), V_{ISP} = 12V $V_{CTRL1/2}$ = 1.15V (Note 4), V_{ISP} = 0V	● ●	87 87	90 90	93 93	mV mV
	1/2 LED Current Regulation $V_{(ISP-ISN)}$	$V_{CTRL1/2}$ = 0.75V (Note 4), V_{ISP} = 12V $V_{CTRL1/2}$ = 0.75V (Note 4), V_{ISP} = 0V	● ●	47.5 47.5	50 50	52.5 52.5	mV mV
	1/20th LED Current Regulation $V_{(ISP-ISN)}$	$V_{CTRL1/2}$ = 0.30V (Note 4), V_{ISP} = 12V $V_{CTRL1/2}$ = 0.30V (Note 4), V_{ISP} = 0V	● ●	3 3	5 5	7 7	mV mV
	Zero Scale LED Current Regulation $V_{(ISP-ISN)}$	$V_{CTRL1/2}$ = 0.25V (Note 4), V_{ISP} = 12V $V_{CTRL1/2}$ = 0.25V (Note 4), V_{ISP} = 0V	● ●	−2 −2	0 0	2 2	mV mV
	ISP/ISN Input Common Mode Range		●	0		60	V
	ISP/ISN Low Side to High Side Switchover Voltage	V_{ISP} = V_{ISN}			1.8		V
	ISP/ISN High Side to Low Side Switchover Voltage	V_{ISP} = V_{ISN}			1.7		V
	ISP Input Bias Current	V_{PWM} = 5V, V_{ISP} = V_{ISN} = 12V V_{PWM} = 5V, V_{ISP} = V_{ISN} = 0V $V_{EN/UVLO}$ = 0V, V_{ISP} = V_{ISN} = 12V or 0V			23 −10 0		µA µA µA
	ISN Input Bias Current	V_{PWM} = 5V, V_{ISP} = V_{ISN} = 12V V_{PWM} = 5V, V_{ISP} = V_{ISN} = 0V $V_{EN/UVLO}$ = 0V, V_{ISP} = V_{ISN} = 12V or 0V			23 −10 0		µA µA µA
	LED Current Regulation Amplifier g_m				2000		µS
	FB Regulation Voltage	V_C = 1.2V	●	0.98	1.00	1.02	V
	FB Line Regulation	V_{IN} = 4V to 60V			0.2	0.5	%
	FB Load Regulation				0.2	0.8	%
	FB Voltage Regulation Amplifier g_m				660		µS
	FB Input Bias Current	FB in Regulation, Current Out of Pin			10	40	nA
	V_C Output Impedance				10		MΩ
	V_C Standby Leakage Current	V_C = 1.2V, PWM Dimming Off		−10	0	10	nA

ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Current Comparator							
	Maximum Current Sense Threshold $V_{(LSP-LSN)}$	Buck, V_{FB} = 0.8V Boost, V_{FB} = 0.8V	● ●	35 40	50 50	65 60	mV mV
	LSP Pin Bias Current	V_{LSP} = V_{LSN} = 12V			60		µA
	LSN Pin Bias Current	V_{LSP} = V_{LSN} = 12V			60		µA
Fault							
	FB Overvoltage Threshold (V_{FB})	Rising	●	1.03	1.05	1.07	V
	FB Overvoltage Hysteresis		●	15	25	35	mV
	FB Open LED Threshold (V_{FB})	Rising, $V_{(ISP-ISN)}$ = 0V	●	0.93	0.95	0.97	V
	FB Open LED Hysteresis	$V_{(ISP-ISN)}$ = 0V	●	35	50	65	mV
	FB Short LED Threshold (V_{FB})	Falling	●	0.24	0.25	0.26	V
	FB Short LED Hysteresis	Hysteresis	●	35	50	65	mV
	ISP/ISN Over Current Threshold $V_{(ISP-ISN)}$	V_{ISP} = 12V			750		mV
	ISP/ISN Open LED Threshold $V_{(ISP-ISN)}$	Falling, V_{FB} = 1.0V	●	8	10	12	mV
	ISP/ISN Open LED Hysteresis	V_{FB} = 1.0V	●	3	5	7	mV
	$\overline{FAULT}$ Pull-Down Resistance				100	200	Ω
	SS Hard Pull-Down Resistance	$V_{EN/UVLO}$ = 1.1V			100	200	Ω
	SS Pull-Up Current	V_{FB} = 0.8V, V_{SS} = 0V		10.5	12.5	14.5	µA
	SS Pull-Down Current	V_{FB} = 1.0V, V_{SS} = 2V		1.05	1.25	1.45	µA
	SS Fault Latch-Off Threshold	Falling			1.7		V
	SS Fault Latch-Off Hysteresis				50		mV
	SS Fault Reset Threshold				0.2		V
Oscillator							
	RT Pin Voltage	R_T = 100kΩ			1.00		V
	Switching Frequency	$V_{SYNC/SPRD}$ = 0V, R_T = 226k $V_{SYNC/SPRD}$ = 0V, R_T = 100k $V_{SYNC/SPRD}$ = 0V, R_T = 59.0k	 ●	645 1290 1900	685 1360 2000	725 1430 2100	kHz kHz kHz
	SYNC Frequency			600		2100	kHz
	SYNC/SPRD Input Bias Current	$V_{SYNC/SPRD}$ = 5V		−0.1	0	0.1	µA
	SYNC/SPRD Threshold Voltage			0.4		1.5	V
	Highest Spread Spectrum Above Oscillator Frequency	$V_{SYNC/SPRD}$ = 5V		21	23	25	%

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 2). V_{IN} = 12V, $V_{EN/UVLO}$ = 1.5V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Region Transition						
	Buck-Boost to Boost (V_{IN}/V_{OUT})		0.73	0.75	0.77	
	Boost to Buck-Boost (V_{IN}/V_{OUT})		0.83	0.85	0.87	
	Buck to Buck-Boost (V_{IN}/V_{OUT})		1.23	1.25	1.27	
	Buck-Boost to Buck (V_{IN}/V_{OUT})		1.31	1.33	1.35	
	Peak-Buck to Peak-Boost (V_{IN}/V_{OUT})		0.96	0.98	1.00	
	Peak-Boost to Peak-Buck (V_{IN}/V_{OUT})		1.00	1.02	1.04	
NMOS Drivers						
	TG1, TG2 Gate Driver On-Resistance Gate Pull-Up Gate Pull-Down	$V_{(BST-SW)}$ = 5V		2.6 1.4		Ω Ω
	BG1, BG2 Gate Driver On-Resistance Gate Pull-Up Gate Pull-Down	V_{INTVCC} = 5V		3.2 1.2		Ω Ω
	TG1, TG2 Rise Time TG1, TG2 Fall Time	C_L = 3.3nF, 10% to 90% C_L = 3.3nF, 90% to 10%		25 20		ns ns
	BG1, BG2 Rise Time BG1, BG2 Fall Time	C_L = 3.3nF, 10% to 90% C_L = 3.3nF, 90% to 10%		25 20		ns ns
	TG Off to BG On Delay	C_L = 3.3nF		25		ns
	BG Off to TG On Delay	C_L = 3.3nF		25		ns
	TG1 Minimum Duty Cycle in Buck Region	Peak-Buck Current Mode		10		%
	TG1 Maximum Duty Cycle in Buck Region	Peak-Buck Current Mode		90		%
	TG1 Fixed Duty Cycle in Buck-Boost Region	Peak-Boost Current Mode		80		%
	BG2 Fixed Duty Cycle in Buck-Boost Region	Peak-Buck Current Mode		20		%
	BG2 Minimum Duty Cycle in Boost Region	Peak-Boost Current Mode		10		%
	BG2 Maximum Duty Cycle in Boost Region	Peak-Boost Current Mode		90		%

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LT8391AE is guaranteed to meet performance specifications from 0°C to 125°C operating junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT8391AI is guaranteed over the –40°C to 125°C operating junction temperature range. The LT8391AH is guaranteed over the –40°C to 150°C operating junction temperature range. The LT8391AJ specifications over the –40°C to 150°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. High junction temperatures degrade operating lifetimes. Operating lifetime is derated at junction temperatures greater than 125°C.

Note 3: The LT8391A includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 150°C when overtemperature protection is active. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability.

Note 4: $V_{CTRL1/2}$ represents the condition of CTRL1 when CTRL2 is equal to 2V or the condition of CTRL2 when CTRL1 is equal to 2V.

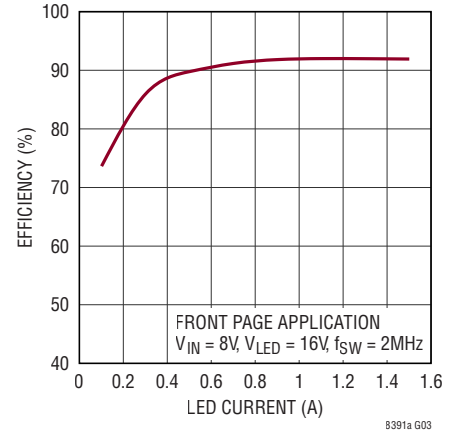# TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25°C$, unless otherwise noted.
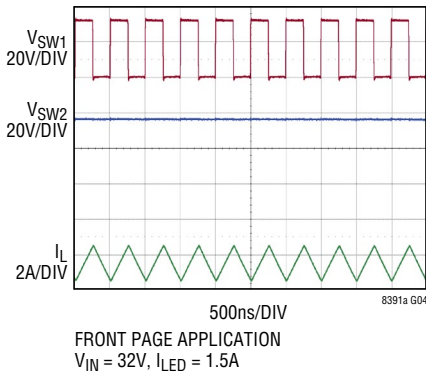
Efficiency vs LED Current (Buck Region)

FRONT PAGE APPLICATION
$V_{IN} = 32V$, $V_{LED} = 16V$, $f_{SW} = 2MHz$

8391a G01
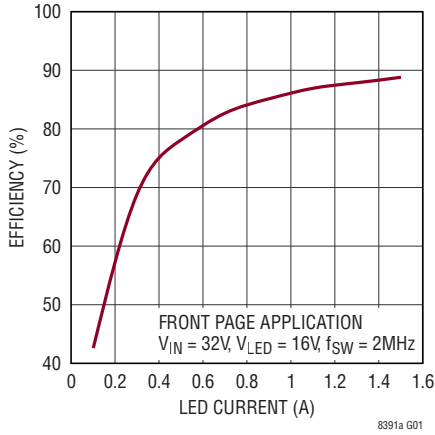
Efficiency vs LED Current (Buck-Boost Region)

FRONT PAGE APPLICATION
$V_{IN} = 18V$, $V_{LED} = 16V$, $f_{SW} = 2MHz$

8391a G02
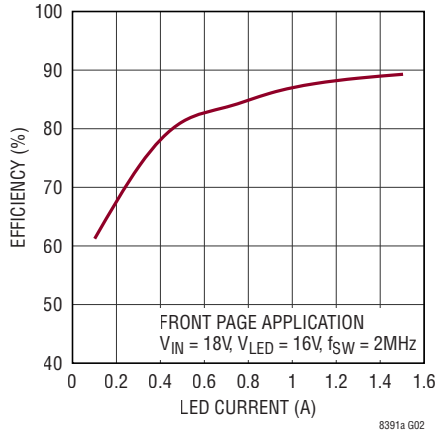
Efficiency vs LED Current (Boost Region)

FRONT PAGE APPLICATION
$V_{IN} = 8V$, $V_{LED} = 16V$, $f_{SW} = 2MHz$

8391a G03

Switching Waveforms (Buck Region)

V_{SW1} 20V/DIV
V_{SW2} 20V/DIV
I_L 2A/DIV

500ns/DIV

8391a G04

FRONT PAGE APPLICATION
$V_{IN} = 32V$, $I_{LED} = 1.5A$

Switching Waveforms (Buck-Boost Region)

V_{SW1} 20V/DIV
V_{SW2} 20V/DIV
I_L 2A/DIV

500ns/DIV

8391a G05

FRONT PAGE APPLICATION
$V_{IN} = 18V$, $I_{LED} = 1.5A$
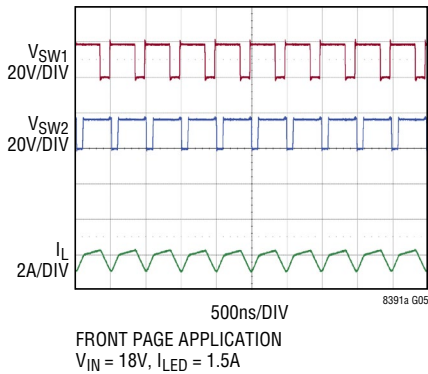
Switching Waveforms (Boost Region)

V_{SW1} 20V/DIV
V_{SW2} 20V/DIV
I_L 2A/DIV

500ns/DIV

8391a G06

FRONT PAGE APPLICATION
$V_{IN} = 8V$, $I_{LED} = 1.5A$
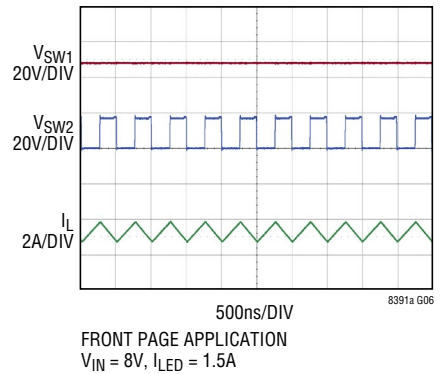
LED Current vs V_{IN}
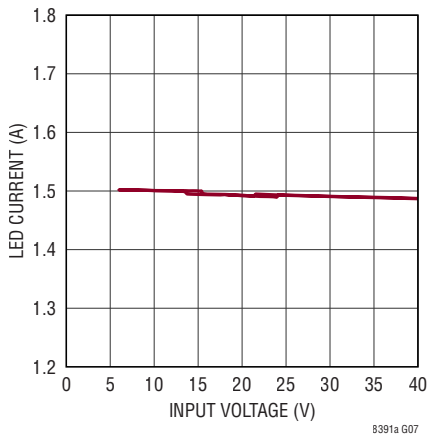
8391a G07

V_{IN} Shutdown Current

$V_{IN} = 60V$
$V_{IN} = 12V$
$V_{IN} = 4V$
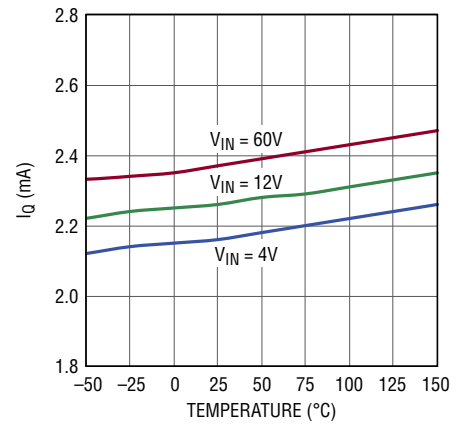
8391a G08

V_{IN} Quiescent Current

$V_{IN} = 60V$
$V_{IN} = 12V$
$V_{IN} = 4V$

8391a G09

Rev. A

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

INTV$_{CC}$ Voltage vs Temperature

INTV$_{CC}$ Voltage vs V$_{IN}$

INTV$_{CC}$ UVLO Threshold

V$_{REF}$ Voltage vs Temperature

V$_{REF}$ Voltage vs V$_{IN}$

V$_{REF}$ UVLO Threshold

EN/UVLO Enable Threshold

EN/UVLO Hysteresis Current

CTRL1/CTRL2 Dim-Off Threshold

TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25°C$, unless otherwise noted.

$V_{(ISP-ISN)}$ Regulation vs V_{CTRL}

8391a G19

$V_{(ISP-ISN)}$ Regulation vs V_{ISP}

8391a G20

$V_{(ISP-ISN)}$ Regulation vs Temperature

8391a G21

$V_{(ISP-ISN)}$ Regulation vs V_{FB}

8391a G22

FB Regulation vs Temperature

8391a G23

Maximum Current Sense vs Temperature

8391a G24

FB Overvoltage Threshold

8391a G25

FB Open LED Threshold

8391a G26

FB Short LED Threshold

8391a G27

Rev. A

10

TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25°C$, unless otherwise noted.

ISP/ISN Open LED Threshold

8391a G28

SS Current vs Temperature

8391a G29

Oscillator Frequency vs Temperature
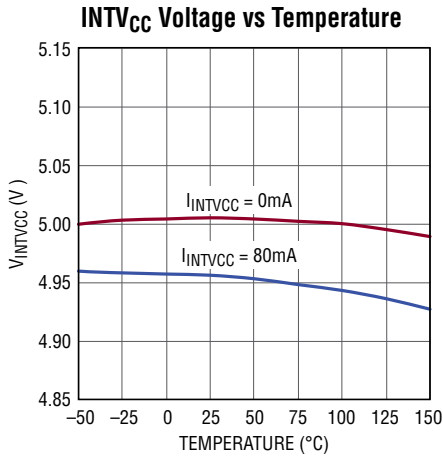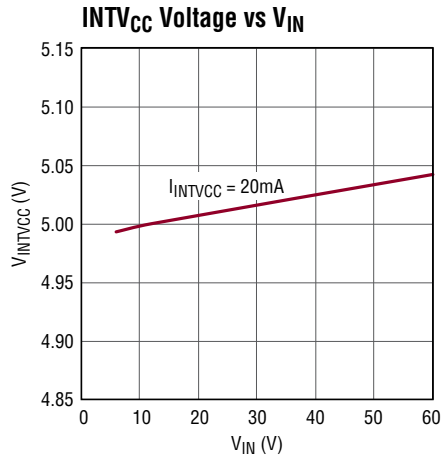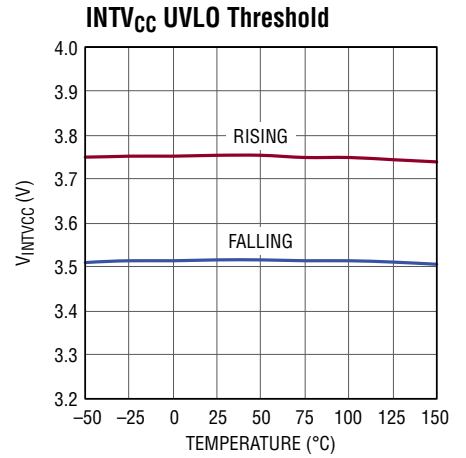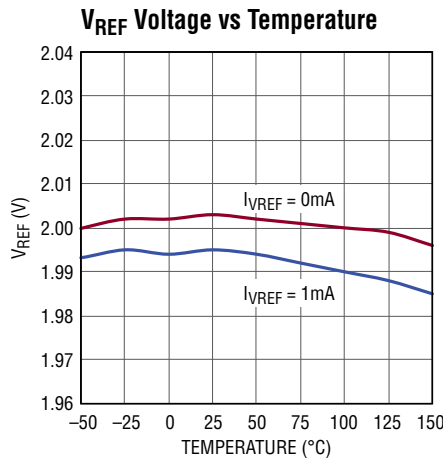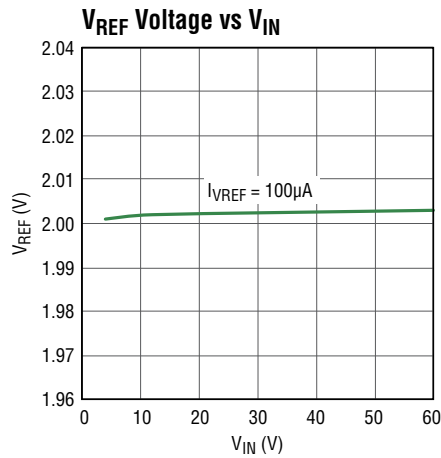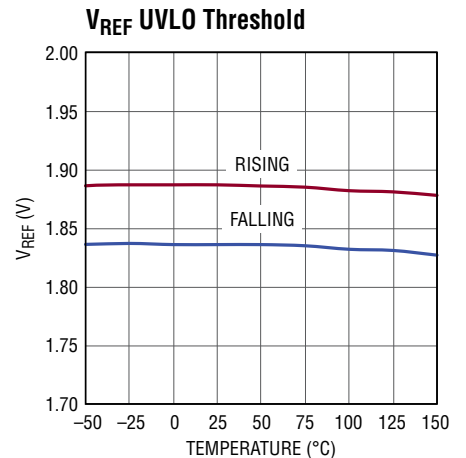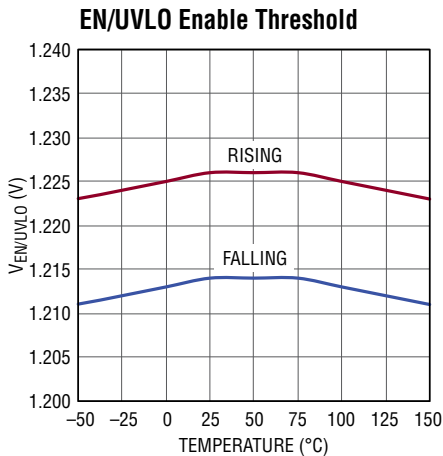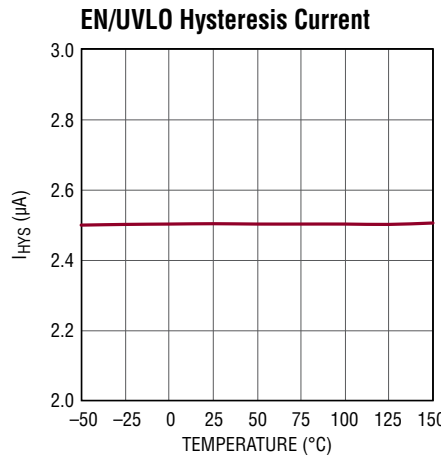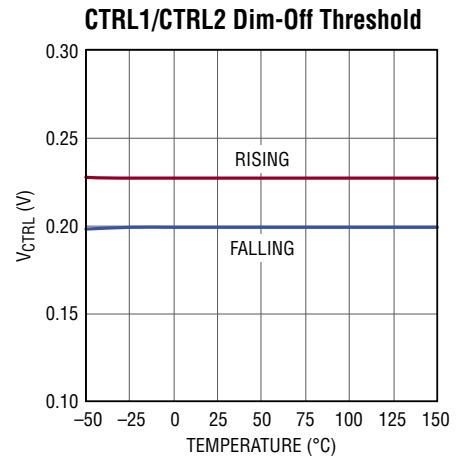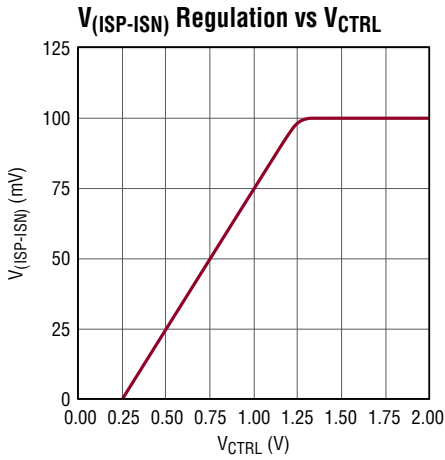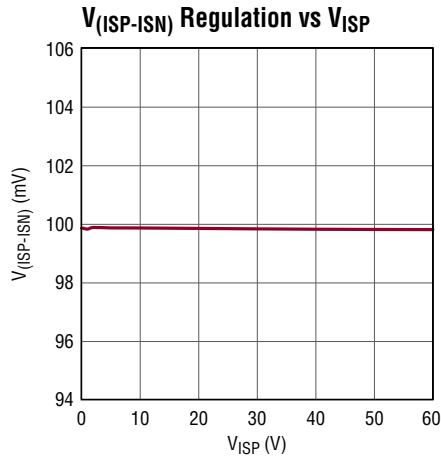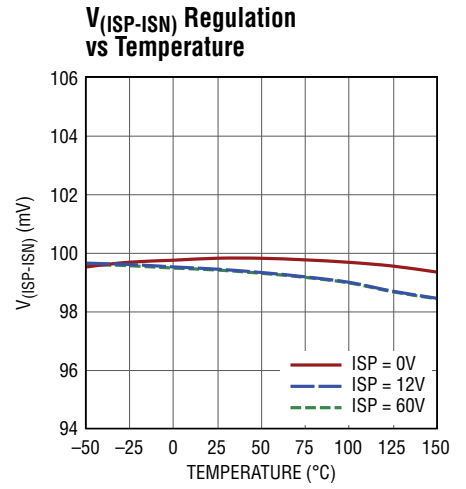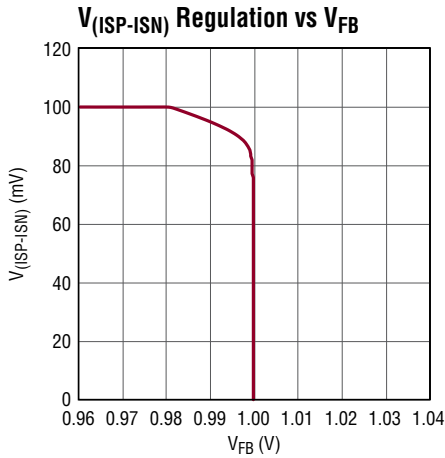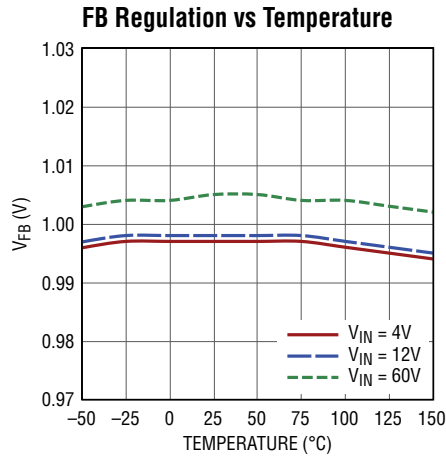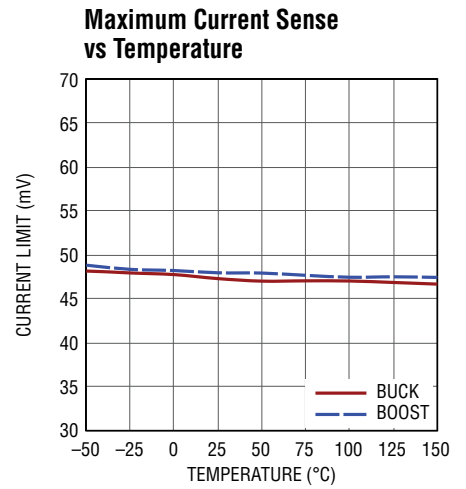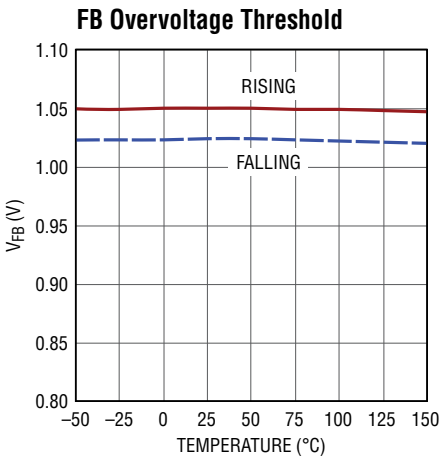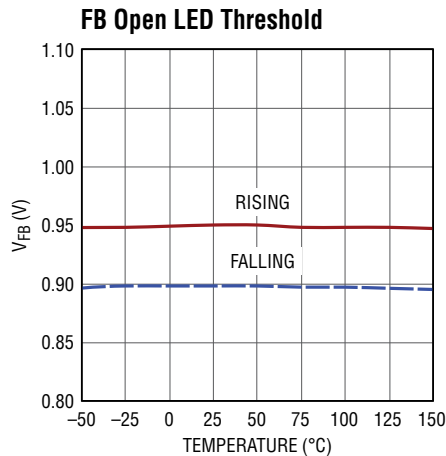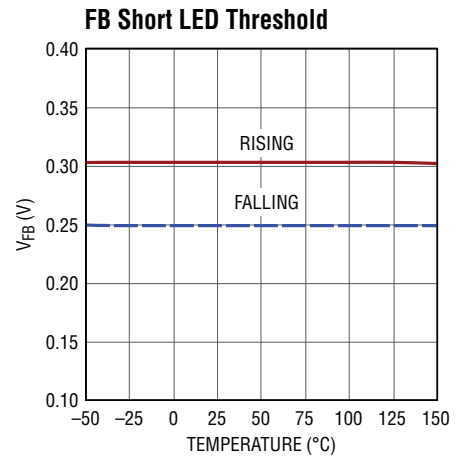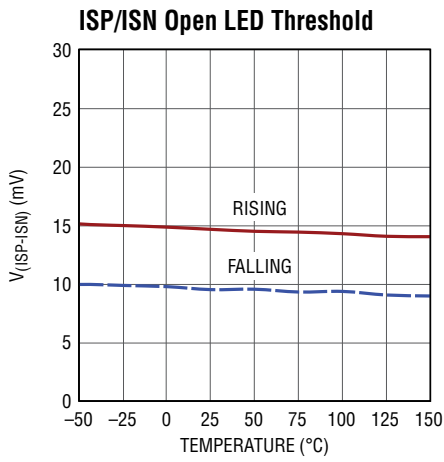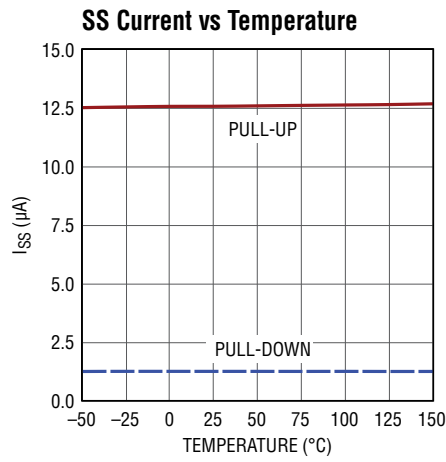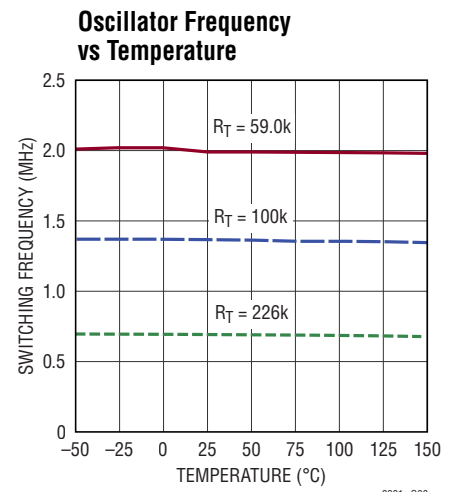
8391a G30

PIN FUNCTIONS

BG1: Buck Side Bottom Gate Drive. Drives the gate of buck side bottom N-channel MOSFET with a voltage swing from ground to $INTV_{CC}$.

BST1: Buck Side Bootstrap Floating Driver Supply. The BST1 pin has an integrated bootstrap Schottky diode from the $INTV_{CC}$ pin and requires an external bootstrap capacitor to the SW1 pin. The BST1 pin swings from a diode voltage drop below $INTV_{CC}$ to (V_{IN} + $INTV_{CC}$).

SW1: Buck Side Switch Node. The SW1 pin swings from a Schottky diode voltage drop below ground up to V_{IN}.

TG1: Buck Side Top Gate Drive. Drives the gate of buck side top N-channel MOSFET with a voltage swing from SW1 to BST1.

LSP: Positive Terminal of the Buck Side Inductor Current Sense Resistor (R_{SENSE}). Ensure accurate current sense with Kelvin connection.

LSN: Negative Terminal of the Buck Side Inductor Current Sense Resistor (R_{SENSE}). Ensure accurate current sense with Kelvin connection.

V_{IN}: Input Supply. The V_{IN} pin must be tied to the power input to determine the buck, buck-boost, or boost operation regions. Locally bypass this pin to ground with a minimum 1µF ceramic capacitor.

$INTV_{CC}$: Internal 5V Linear Regulator Output. The $INTV_{CC}$ linear regulator is supplied from the V_{IN} pin, and powers the internal control circuitry and gate drivers. Locally bypass this pin to ground with a minimum 4.7µF ceramic capacitor.

EN/UVLO: Enable and Undervoltage Lockout. Force the pin below 0.3V to shut down the part and reduce V_{IN} quiescent current below 2µA. Force the pin above 1.233V for normal operation. The accurate 1.220V falling threshold can be used to program an undervoltage lockout (UVLO) threshold with a resistor divider from V_{IN} to ground. An accurate 2.5µA pull-down current allows the programming of V_{IN} UVLO hysteresis. If neither function is used, tie this pin directly to V_{IN}.

RP: Internal PWM Dimming Frequency Setting. The RP pin is used to set the internal PWM dimming frequency with a resistor to ground. Do not use a resistor larger than 1MΩ and do not leave this pin open. If an external PWM dimming pulse is available at the PWM pin, tie this pin to ground.

PWM: PWM Dimming Input. The PWM pin can be used in two ways: external PWM dimming and internal PWM dimming. For external PWM dimming, drive this pin with a digital pulse from 0V to a voltage higher than 1.5V to control PWM dimming of the LED string. Make sure the RP pin is tied to ground in this case. For internal PWM dimming, apply an analog voltage between 1V and 2V to generate an internal digital pulse by comparing with the internal ramp. If PWM dimming is not used, tie this pin to $INTV_{CC}$. Forcing the pin low turns off TG1 and TG2, turns on BG1 and BG2, disconnects the V_C pin from all internal loads, and turns off PWMTG.

V_{REF}: Voltage Reference Output. The V_{REF} pin provides an accurate 2V reference capable of supplying 1mA current. Locally bypass this pin to ground with a 0.47µF ceramic capacitor.

CTRL1: Control Input for LED Current Sense Threshold. The CTRL1 pin is used to program the LED regulation current:

$$I_{LED} = \frac{Min\left(V_{CTRL1} - 0.25V, V_{CTRL2} - 0.25, 1V\right)}{10 \cdot R_{LED}}$$

The V_{CTRL1} can be set by an external voltage reference or a resistor divider from V_{REF} to ground. For $0.25V \leq V_{CTRL1} \leq 1.15V$, the current sense threshold linearly goes up from 0mV to 90mV. For $V_{CTRL1} \geq 1.35V$, the current sense threshold is constant at 100mV full scale value. For $1.15V \leq V_{CTRL1} \leq 1.35V$, the current sense threshold smoothly transitions from the linear function of V_{CTRL1} to the 100mV constant value. Tie CTRL1 to V_{REF} for the 100mV full scale threshold. Force the pin below 0.2V to stop switching.

ISP: Positive Terminal of the LED Current Sense Resistor (R_{LED}). Ensure accurate current sense with Kelvin connection.

ISN: Negative Terminal of the LED Current Sense Resistor (R_{LED}). Ensure accurate current sense with Kelvin connection.

PIN FUNCTIONS

CTRL2: Thermal Control Input for LED Current Sense Threshold. The CTRL2 pin is used to program LED current derating versus temperature. The V_{CTRL2} with a negative temperature coefficient can be set by an external temperature dependent resistor divider from V_{REF} to ground. For $0.25V \leq V_{CTRL2} \leq 1.15V$, the current sense threshold linearly goes up from 0mV to 90mV. For $V_{CTRL2} \geq 1.35V$, the current sense threshold is constant at 100mV full scale value. For $1.15V \leq V_{CTRL2} \leq 1.35V$, the current sense threshold smoothly transitions from the linear function of V_{CTRL2} to the 100mV constant value. Tie CTRL2 to V_{REF} for the 100mV full scale threshold. Force the pin below 0.2V to stop switching.

FAULT: LED Fault Open Drain Output. The $\overline{FAULT}$ pin is pulled low when any of the following conditions happens:

1. Open LED ($V_{FB} > 0.95V$ & $V_{(ISP-ISN)} < 10mV$)
2. Short LED ($V_{FB} < 0.25V$)

To function, the pin requires an external pull-up resistor. The $\overline{FAULT}$ status is updated only during PWM high state and latched during PWM low state.

SS: Soft-Start Timer Setting. The SS pin is used to set soft-start timer by connecting a capacitor to ground. An internal 12.5µA pull-up current charging the external SS capacitor gradually ramps up FB regulation voltage. A 22nF capacitor is recommended on this pin. Any UVLO or thermal shutdown immediately pulls SS pin to ground and stops switching. Using a single resistor from SS to V_{REF}, the LT8391A can be set in three different fault protection modes during open or short LED fault conditions: hiccup (no resistor), latchoff (499k), and keep-running (100k). See more details in the Applications Information section.

FB: Voltage Loop Feedback Input. The FB pin is used for constant-voltage regulation and LED fault protection. The internal error amplifier with its output V_C regulates V_{FB} to 1.00V through the DC/DC converter. During open LED ($V_{FB} > 0.95V$ & $V_{(ISP-ISN)} < 10mV$) or short LED ($V_{FB} < 0.25V$) fault conditions, the part pulls the $\overline{FAULT}$ pin low and gets into one fault mode per customer setting. During an overvoltage ($V_{FB} > 1.05V$) condition, the part turns off all TG1, BG1, TG2, BG2, and PWMTG.

V_C: Error Amplifier Output to Set Inductor Current Comparator Threshold. The V_C pin is used to compensate the control loop with an external RC network. During PWM low state, the V_C pin is disconnected from all internal loads to store its voltage information for the highest PWM dimming performance.

RT: Switching Frequency Setting. Connect a resistor from this pin to ground to set the internal oscillator frequency from 600kHz to 2MHz.

SYNC/SPRD: Switching Frequency Synchronization or Spread Spectrum. Ground this pin for switching at internal oscillator frequency. Apply a clock signal for external frequency synchronization. Tie to $INTV_{CC}$ for 25% triangle spread spectrum above internal oscillator frequency.

PWMTG: PWM Dimming Top Gate Drive. A buffered and inverted version of the PWM input signal, the PWMTG pin drives an external high side PMOS PWM switch with a voltage swing from the higher voltage of (V_{OUT} –5V) and 1.2V to V_{OUT}. Leave this pin unconnected if not used.

V_{OUT}: Output Supply. The V_{OUT} pin must be tied to the power output to determine the buck, buck-boost, or boost operation regions. The V_{OUT} pin also serves as positive rail for the PWMTG drive. Locally bypass this pin to ground with a minimum 1µF ceramic capacitor.

TG2: Boost Side Top Gate Drive. Drives the gate of boost side top N-Channel MOSFET with a voltage swing from SW2 to BST2.

SW2: Boost Side Switch Node. The SW2 pin swings from a Schottky diode voltage drop below ground to V_{OUT}.

BST2: Boost Side Bootstrap Floating Driver Supply. The BST2 pin has an integrated bootstrap Schottky diode from the $INTV_{CC}$ pin and requires an external bootstrap capacitor to the SW2 pin. The BST2 pin swings from a diode voltage drop below $INTV_{CC}$ to (V_{OUT} + $INTV_{CC}$).

BG2: Boost Side Bottom Gate Drive. Drives the gate of boost side bottom N-Channel MOSFET with a voltage swing from ground to $INTV_{CC}$.

GND (Exposed Pad): Ground. Solder the exposed pad directly to the ground plane.

LT8391A

BLOCK DIAGRAM

For more information www.analog.com
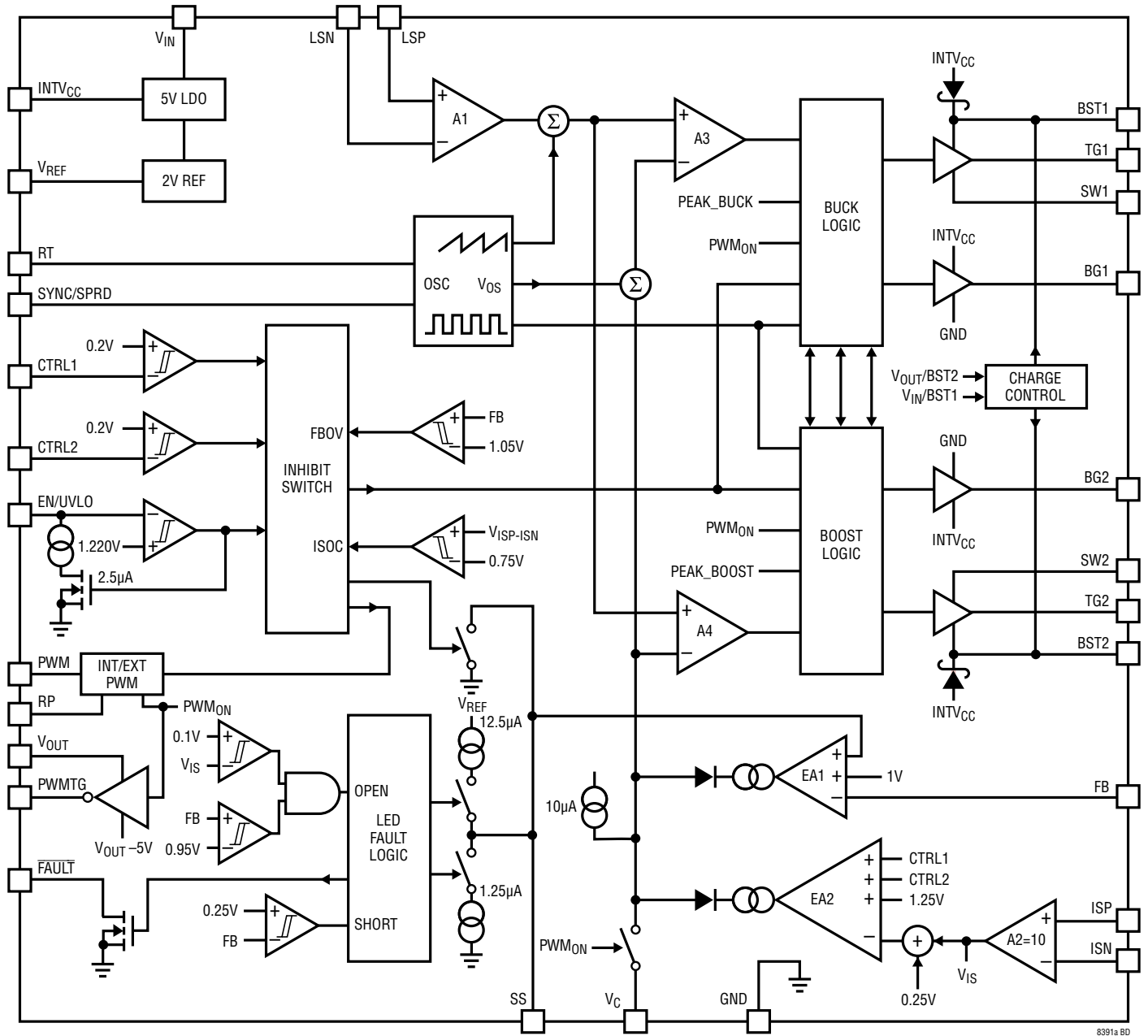
OPERATION

The LT8391A is a current mode LED controller that can regulate LED current from input voltage above, below, or equal to the LED string voltage. The ADI proprietary peak-buck peak-boost current mode control scheme uses a single inductor current sense resistor and provides smooth transition between buck region, buck-boost region, and boost region. Its operation is best understood by referring to the Block Diagram.

Power Switch Control

Figure 1 shows a simplified diagram of how the four power switches A, B, C, and D are connected to the inductor L, the current sense resistor R_{SENSE}, power input V_{IN}, power output V_{OUT}, and ground. The current sense resistor R_{SENSE} connected to the LSP and LSN pins provides inductor current information for both peak current mode control and reverse current detection in buck region, buck-boost region, and boost region. Figure 2 shows the current mode control as a function of V_{IN}/V_{OUT} ratio and Figure 3 shows the operation region as a function of V_{IN}/V_{OUT} ratio. The power switches are properly controlled to smoothly transition between modes and regions. Hysteresis is added to prevent chattering between modes and regions.
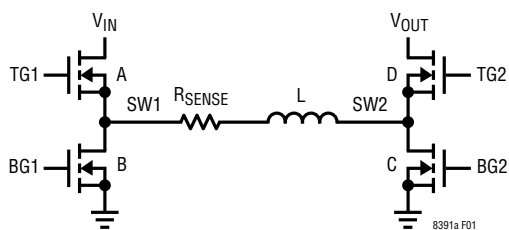

Figure 1. Simplified Diagram of the Power Switches

There are total four states: (1) peak-buck current mode control in buck region, (2) peak-buck current mode control in buck-boost region, (3) peak-boost current mode control in buck-boost region, and (4) peak-boost current mode control in boost region. The following sections give detailed description for each state with waveforms, in which the shoot-through protection dead time between switches A and B, between switches C and D are ignored for simplification.
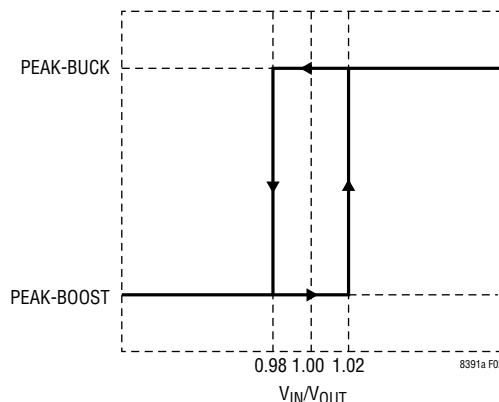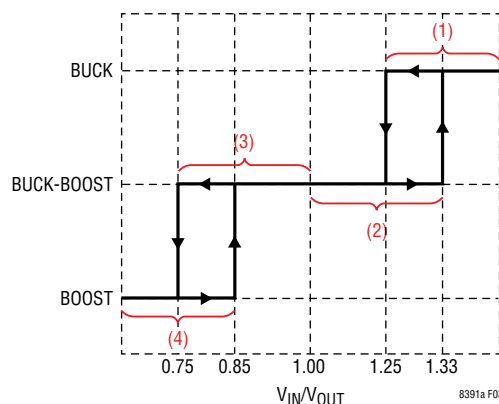

Figure 2. Current Mode vs V_{IN}/V_{OUT} Ratio

Figure 3. Operation Region vs V_{IN}/V_{OUT} Ratio

Peak-Buck in Buck Region ($V_{IN} \gg V_{OUT}$)

When V_{IN} is much higher than V_{OUT}, the LT8391A uses peak-buck current mode control in buck region (Figure 4). Switch C is always off and switch D is always on. At the beginning of every cycle, switch A is turned on and the inductor current ramps up. When the inductor current hits the peak buck current threshold commanded by V_C voltage at buck current comparator A3 during (A+D) phase, switch A is turned off and switch B is turned on for the rest of the cycle. Switches A and B will alternate, behaving like a typical synchronous buck regulator.
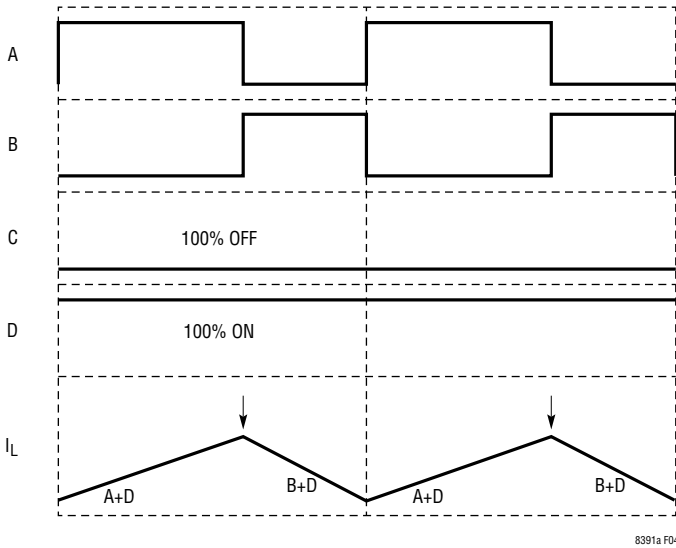
OPERATION

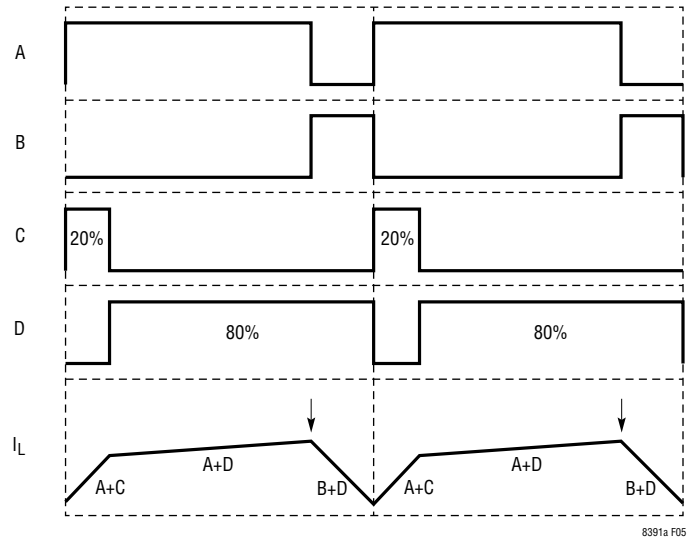Figure 4. Peak-Buck in Buck Region ($V_{IN} >> V_{OUT}$)

Figure 5. Peak-Buck in Buck-Boost Region ($V_{IN} \sim V_{OUT}$)

Peak-Buck in Buck-Boost Region ($V_{IN} \sim> V_{OUT}$)

When V_{IN} is slightly higher than V_{OUT}, the LT8391A uses peak-buck current mode control in buck-boost region (Figure 5). Switch C is always turned on for the beginning 20% cycle and switch D is always turned on for the remaining 80% cycle. At the beginning of every cycle, switches A and C are turned on and the inductor current ramps up. After 20% cycle, switch C is turned off and switch D is turned on, and the inductor keeps ramping up. When the inductor current hits the peak buck current threshold commanded by V_C voltage at buck current comparator A3 during (A+D) phase, switch A is turned off and switch B is turned on for the rest of the cycle.

Peak-Boost in Buck-Boost Region ($V_{IN} <\sim V_{OUT}$)

When V_{IN} is slightly lower than V_{OUT}, the LT8391A uses peak-boost current mode control in buck-boost region (Figure 6). Switch A is always turned on for the beginning 80% cycle and switch B is always turned on for the remaining 20% cycle. At the beginning of every cycle, switches A and C are turned on and the inductor current ramps up. When the inductor current hits the peak boost current threshold commanded by V_C voltage at boost current comparator A4 during (A+C) phase, switch C is turned off and switch D is turned on for the rest of the cycle. After 80% cycle, switch A is turned off and switch B is turned on for the rest of the cycle.
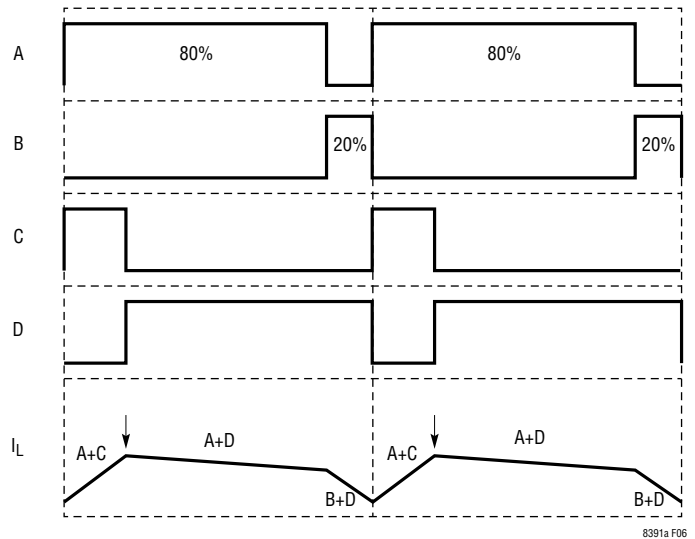

Figure 6. Peak-Boost in Buck-Boost Region ($V_{IN} <\sim V_{OUT}$)

Peak-Boost in Boost Region ($V_{IN} << V_{OUT}$)

When V_{IN} is much lower than V_{OUT}, the LT8391A uses peak-boost current mode control in boost region (Figure 7). Switch A is always on and switch B is always off. At the beginning of every cycle, switch C is turned on and the inductor current ramps up. When the inductor current hits the peak boost current threshold commanded by V_C voltage at boost current comparator A4 during (A+C) phase, switch C is turned off and switch D is turned on for the rest of

OPERATION

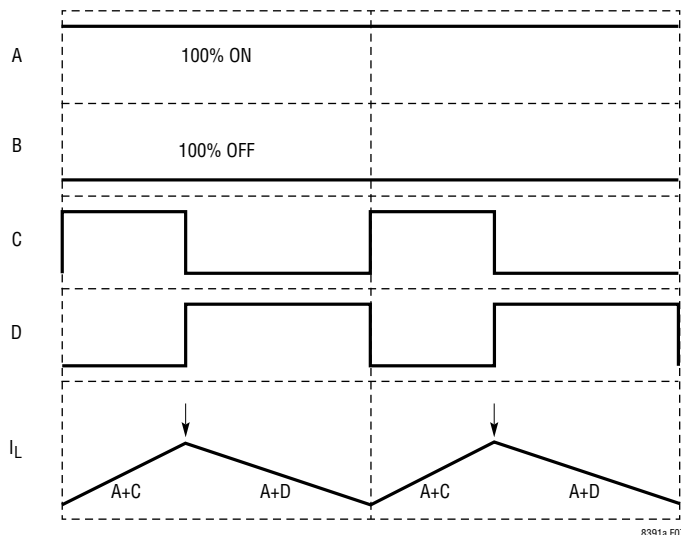the cycle. Switches C and D will alternate, behaving like a typical synchronous boost regulator.

Figure 7. Peak-Boost in Boost Region (V$_{IN}$ << V$_{OUT}$)

Main Control Loop

The LT8391A is a fixed frequency current mode controller. The inductor current is sensed through the inductor sense resistor between the LSP and LSN pins. The current sense voltage is gained up by amplifier A1 and added to a slope compensation ramp signal from the internal oscillator. The summing signal is then fed into the positive terminals of the buck current comparator A3 and boost current comparator A4. The negative terminals of A3 and A4 are controlled by the voltage on the V$_C$ pin, which is the diode-OR of error amplifiers EA1 and EA2.

Depending on the state of the peak-buck peak-boost current mode control, either the buck logic or the boost logic is controlling the four power switches so that either the FB voltage is regulated to 1V or the current sense voltage between the ISP and ISN pins is regulated by the CTRL1 or CTRL2 pin during normal operation. The gains of EA1 and EA2 have been balanced to ensure smooth transition between constant-voltage and constant-current operation with the same compensation network.

Light Load Current Operation

At light load, the LT8391A typically still runs at its full switching frequency in either continuous conduction mode or discontinuous conduction mode because both the buck and boost reverse current sense thresholds are set to –4mV. The negative reverse current sense thresholds allow a small amount of energy flowing from the output to the input in every cycle, thereby preventing the pulse-skip frequency from going below 100Hz, which causes the LED string to flicker.

In the buck region, switch B is turned off whenever the buck reverse current threshold is triggered during (B+D) phase. In the boost region, switch D is turned off whenever the boost reverse current threshold is triggered during (A+D) phase. In the buck-boost region, switch D is turned off whenever the boost reverse current threshold is triggered during (A+D) phase, and both switches B and D are turned off whenever the buck reverse current threshold is triggered during (B+D) phase.

However, when a smaller value inductor is used and the inductor current ripple is bigger, the LT8391A may run in pulse-skip mode, where the switches are held off for multiple cycles (i.e., skipping pulses) to maintain the regulation.

Internal Charge Path

Each of the two top MOSFET drivers is biased from its floating bootstrap capacitor, which is normally recharged by INTV$_{CC}$ through both the external and internal bootstrap diodes when the top MOSFET is turned off. When the LT8391A operates exclusively in the buck or boost regions, one of the top MOSFETs is constantly on. An internal charge path, from V$_{OUT}$ and BST2 to BST1 or from V$_{IN}$ and BST1 to BST2, charges the bootstrap capacitor to 4.6V so that the top MOSFET can be kept on.

OPERATION

Shutdown and Power-On-Reset

The LT8391A enters shutdown mode and drains less than 2µA quiescent current when the EN/UVLO pin is below its shutdown threshold (0.3V minimum). Once the EN/UVLO pin is above its shutdown threshold (1V maximum), the LT8391A wakes up startup circuitry, generates bandgap reference, and powers up the internal $INTV_{CC}$ LDO. The $INTV_{CC}$ LDO supplies the internal control circuitry and gate drivers. Now the LT8391A enters undervoltage lock-out (UVLO) mode with a hysteresis current (2.5µA typical) pulled into the EN/UVLO pin. When the $INTV_{CC}$ pin is charged above its rising UVLO threshold (3.78V typical), the EN/UVLO pin passes its rising enable threshold (1.233V typical), and the junction temperature is less than its thermal shutdown (165°C typical), the LT8391A enters enable mode, in which the EN/UVLO hysteresis current is turned off and the voltage reference V_{REF} is being charged up from ground. From the time of entering enable mode to the time of V_{REF} passing its rising UVLO threshold (1.89V typical), the LT8391A is going through a power-on-reset (POR), waking up the entire internal control circuitry and settling to the right initial conditions. After the POR, the LT8391A is ready and waiting for the signals on the CTRL1, CTRL2, and PWM pins to start switching.

Start-Up and Fault Protection

Figure 8 shows the start-up and fault sequence for the LT8391A. During the POR state, the SS pin is hard pulled down with a 100Ω to ground. In a pre-biased condition, the SS pin has to be pulled below 0.2V to enter the INIT state, where the LT8391A wait 10µs so that the SS pin can be fully discharged to ground. After the 10µs, the LT8391A enters the UP/PRE state when the PWM_{ON} signal goes high. The PWM_{ON} high signal happens when both the CTRL1 and CTRL2 pins are above their rising dim-off thresholds (0.228V typical) and the external or internal PWM dimming is on.

During the UP/PRE state, the SS pin is charged up by a 12.5µA pull-up current while the switching is disabled and the PMWTG is turned off. Once the SS pin is charged above 0.25V, the LT8391A enters the UP/TRY state, where the PMWTG is turned on first while the switching is still

disabled. This is to check whether the voltage on the output capacitor is not too high for the LED string before any switching energy delivery. In the case of a higher voltage output capacitor connected to a lower voltage LED string, the excessive current flowing through the LED string and current sense resistor triggers the ISP/ISN over current (ISOC) signal and resets the LT8391A back into the POR state. So the LT8391A will hiccup with SS pin between 0V and 0.25V and go around the POR, INIT, UP/PRE, and UP/TRY states to slowly discharge the higher voltage output capacitor until its voltage gets closer to the lower voltage LED string. After 10µs in the UP/TRY state without triggering the ISOC signal, the LT8391A enters the UP/RUN state.
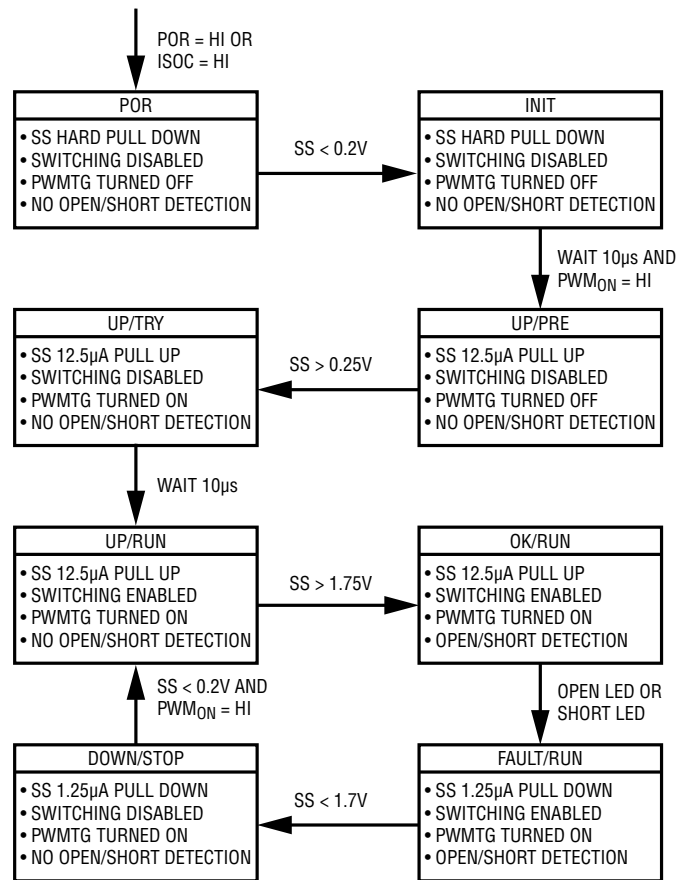

Figure 8. Start-Up and Fault Sequence

OPERATION

During the UP/RUN state, the switching is enabled and the start-up of the output voltage V_{OUT} is controlled by the voltage on the SS pin. When the SS pin voltage is less than 1V, the LT8391A regulates the FB pin voltage to the SS pin voltage instead of the 1V reference. This allows the SS pin to be used to program soft-start by connecting an external capacitor from the SS pin to GND. The internal 12.5µA pull-up current charges up the capacitor, creating a voltage ramp on the SS pin. As the SS pin voltage rises linearly from 0.25V to 1V (and beyond), the output voltage V_{OUT} rises smoothly to its final LED string voltage.

Once the SS pin is charged above 1.75V, the LT8391A enters the OK/RUN state, where the LED fault (both open LED and short LED) detection is activated. The open LED means that $V_{FB} > 0.95V$ and $V_{(ISP-ISN)} < 10mV$, and the short LED means that $V_{FB} < 0.25V$. Both the open LED and short LED faults are combined to the $\overline{FAULT}$ pin. When either fault happens, the LT8391A enters the FAULT/RUN state, where a 1.25µA pull-down current slowly discharges the SS pin with the other conditions the same as the OK/RUN state. Once the SS pin is discharged below 1.7V, the LT8391A enters the DOWN/STOP state, where the switching is disabled and the LED fault detection is deactivated with the previous fault latched. Once the SS pin is discharged below 0.2V and the PWM_{ON} signal is still high, the LT8391A goes back to the UP/RUN state.

In an open or short LED condition, the LT8391A can be set to hiccup, latch-off, or keep-running fault protection mode with a resistor between the SS and V_{REF} pins. Without any resistor, the LT8391A will hiccup with SS pin between 0.2V and 1.75V and go around the UP/RUN, OK/RUN, FAULT/RUN, and DOWN/STOP states until the fault condition is cleared. With a 499k resistor, the LT8391A will latch off until the EN/UVLO is toggled. With a 100k resistor, the LT8391A will keep running regardless of the fault.

APPLICATIONS INFORMATION

The front page shows a typical LT8391A application circuit. This Applications Information section serves as a guideline of selecting external components for typical applications. The examples and equations in this section assume continuous conduction mode unless otherwise specified.

Switching Frequency Selection

The LT8391A uses a constant frequency control scheme between 600kHz and 2MHz. Selection of the switching frequency is a trade off between efficiency and component size. Low frequency operation improves efficiency by reducing MOSFET switching losses, but requires larger inductor and capacitor values. For high power applications, consider operating at lower frequencies to minimize MOSFET heating from switching losses. For low power applications, consider operating at higher frequencies to minimize the total solution size.

In addition, the specific application also plays an important role in switching frequency selection. In a noise-sensitive system, the switching frequency is usually selected to keep the switching noise out of a sensitive frequency band.

Switching Frequency Setting

The switching frequency of the LT8391A can be set by the internal oscillator. With the SYNC/SPRD pin pulled to ground, the switching frequency is set by a resistor from the RT pin to ground. Table 1 shows R_T resistor values for common switching frequencies.

Table 1. Switching Frequency vs R_T Value (1% Resistor)

f_{OSC} (MHz)	R_T (k)
0.6	267
0.8	191
1.0	147
1.2	118
1.4	97.6
1.6	82.5
1.8	66.5
2.0	59.0

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Spread Spectrum Frequency Modulation

Switching regulators can be particularly troublesome for applications where electromagnetic interference (EMI) is a concern. To improve the EMI performance, the LT8391A implements a triangle spread spectrum frequency modulation scheme. With the SYNC/SPRD pin tied to $INTV_{CC}$, the LT8391A starts to spread its switching frequency 25% above the internal oscillator frequency. Figure 9 and Figure 10 show the noise spectrum comparison of the front page application between spread spectrum enabled and disabled.
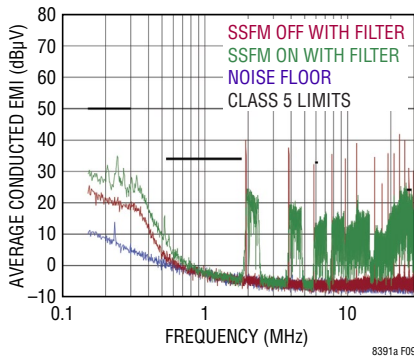

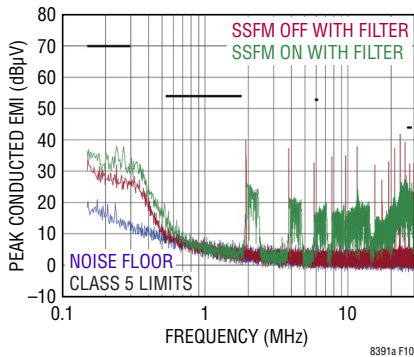**Figure 9. CISPR 25 Average Conducted EMI**

Figure 10. CISPR 25 Peak Conducted EMI

Frequency Synchronization

The LT8391A switching frequency can be synchronized to an external clock using the SYNC/SPRD pin. Driving the SYNC/SPRD with a 50% duty cycle waveform is always a good choice, otherwise maintain the duty cycle between 10% and 90%. Due to the use of a phase-locked loop (PLL) inside, there is no restriction between the synchronization frequency and the internal oscillator frequency.

The rising edge of the synchronization clock represents the beginning of a switching cycle, turning on switches A and C, or switches A and D.

Inductor Selection

The switching frequency and inductor selection are interrelated in that higher switching frequencies allow the use of smaller inductor and capacitor values. The inductor value has a direct effect on ripple current. The highest current ripple $\Delta I_L\%$ happens in the buck region at $V_{IN(MAX)}$, and the lowest current ripple $\Delta I_L\%$ happens in the boost region at $V_{IN(MIN)}$. For any given ripple allowance set by customers, the minimum inductance can be calculated as:

$$L_{BUCK} > \frac{V_{OUT} \bullet (V_{IN(MAX)} - V_{OUT})}{f \bullet I_{LED(MAX)} \bullet \Delta I_L\% \bullet V_{IN(MAX)}}$$

$$L_{BOOST} > \frac{V_{IN(MIN)}^2 \bullet (V_{OUT} - V_{IN(MIN)})}{f \bullet I_{LED(MAX)} \bullet \Delta I_L\% \bullet V_{OUT}^2}$$

where:

f is switching frequency

$\Delta I_L\%$ is allowable inductor current ripple

$V_{IN(MIN)}$ is minimum input voltage

$V_{IN(MAX)}$ is maximum input voltage

V_{OUT} is output voltage

$I_{LED(MAX)}$ is maximum LED current

Slope compensation provides stability in constant frequency current mode control by preventing subharmonic oscillations at certain duty cycles. The minimum inductance required for stability can be calculated as:

$$L > \frac{10 \bullet V_{OUT} \bullet R_{SENSE}}{f}$$

For high efficiency, choose an inductor with low core loss, such as ferrite. Also, the inductor should have low DC resistance to reduce the I^2R losses, and must be able to handle the peak inductor current without saturating. To minimize radiated noise, use a shielded inductor.

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R$_{SENSE}$ Selection and Maximum Output Current

R$_{SENSE}$ is chosen based on the required output current. The duty cycle independent maximum current sense thresholds (50mV in peak-buck and 50mV in peak-boost) set the maximum inductor peak current in buck region, buck-boost region, and boost region.

In boost region, the lowest maximum average load current happens at V$_{IN(MIN)}$ and can be calculated as:

$$I_{OUT(MAX\_BOOST)} = \left(\frac{50mV}{R_{SENSE}} - \frac{\Delta I_{L(BOOST)}}{2} \right) \bullet \frac{V_{IN(MIN)}}{V_{OUT}}$$

where $\Delta I_{L(BOOST)}$ is peak-to-peak inductor ripple current in boost region and can be calculated as:

$$\Delta I_{L(BOOST)} = \frac{V_{IN(MIN)} \bullet (V_{OUT} - V_{IN(MIN)})}{f \bullet L \bullet V_{OUT}}$$

In buck region, the lowest maximum average load current happens at V$_{IN(MAX)}$ and can be calculated as:

$$I_{OUT(MAX\_BUCK)} = \left(\frac{50mV}{R_{SENSE}} - \frac{\Delta I_{L(BUCK)}}{2} \right)$$

where $\Delta I_{L(BUCK)}$ is peak-to-peak inductor ripple current in buck region and can be calculated as:

$$\Delta I_{L(BUCK)} = \frac{V_{OUT} \bullet (V_{IN(MAX)} - V_{OUT})}{f \bullet L \bullet V_{IN(MAX)}}$$

The maximum current sense R$_{SENSE}$ in boost region is:

$$R_{SENSE(BOOST)} = \frac{2 \bullet 50mV \bullet V_{IN(MIN)}}{2 \bullet I_{LED(MAX)} \bullet V_{OUT} + \Delta I_{L(BOOST)} \bullet V_{IN(MIN)}}$$

The maximum current sense R$_{SENSE}$ in buck region is

$$R_{SENSE(BUCK)} = \frac{2 \bullet 50mV}{2 \bullet I_{LED(MAX)} + \Delta I_{L(BUCK)}}$$

The final R$_{SENSE}$ value should be lower than the calculated R$_{SENSE}$ in both buck and boost regions. A 20% to 30% margin is usually recommended.

Power MOSFET Selection

The LT8391A requires four external N-channel power MOSFETs, two for the top switches (switches A and D shown in Figure 1) and two for the bottom switches (switches B and C shown in Figure 1). Important parameters for the power MOSFETs are the breakdown voltage V$_{BR(DSS)}$, threshold voltage V$_{GS(TH)}$, on-resistance R$_{DS(ON)}$, reverse transfer capacitance C$_{RSS}$ and maximum current I$_{DS(MAX)}$.

To achieve 2MHz operation, the power MOSFET selection is critical. With typical 25ns shoot-through protection dead time, high performance power MOSFETs with low Q$_g$ and low R$_{DS(ON)}$ must be used.

Since the gate drive voltage is set by the 5V INTV$_{CC}$ supply, logic-level threshold MOSFETs must be used in LT8391A applications. Switching four MOSFETs at higher frequency like 2MHz, the substantial gate charge current from INTV$_{CC}$ can be estimated as:

$$I_{INTVCC} = f \bullet \left(Q_{gA} + Q_{gB} + Q_{gC} + Q_{gD} \right)$$

where:

f is the switching frequency

Q$_{gA}$, Q$_{gB}$, Q$_{gC}$, Q$_{gD}$ are the total gate charges of MOSFETs A, B, C, D at 5V V$_{GS}$.

Make sure the total required INTV$_{CC}$ current not exceeding the INTV$_{CC}$ current limit in the data sheet. Typically, MOSFETs with less than 15nC Q$_g$ are recommended.

The LT8391A uses the V$_{IN}$/V$_{OUT}$ ratio to transition between modes and regions. Bigger IR drop in the power path caused by improper MOSFET and inductor selection may prevent the LT8391A from smooth transition. Make sure that low R$_{DS(ON)}$ MOSFETs and low DCR inductor are used to satisfy:

$$I_{LED(MAX)} \leq \frac{0.025 \bullet V_{OUT}}{R_{A,B} + R_{C,D} + R_{SENSE} + R_L}$$

where:

R$_{A,B}$ is the maximum R$_{DS(ON)}$ of MOSFETs A or B at 25°C

R$_{C,D}$ is the maximum R$_{DS(ON)}$ of MOSFETs C or D at 25°C

R$_L$ is the maximum DCR resistor of inductor at 25°C

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The $R_{DS(ON)}$ and DCR increase at higher junction temperatures and the process variation have been included in the calculation above.

In order to select the power MOSFETs, the power dissipated by the device must be known. For switch A, the maximum power dissipation happens in boost region, when it remains on all the time. Its maximum power dissipation at maximum output current is given by:

$$P_{A(BOOST)} = \left(\frac{I_{LED(MAX)} \bullet V_{OUT}}{V_{IN}} \right)^2 \bullet \rho_T \bullet R_{DS(ON)}$$

where ρ_T is a normalization factor (unity at 25°C) accounting for the significant variation in on-resistance with temperature, typically 0.4%/°C as shown in Figure 11. For a maximum junction temperature of 125°C, using a value of $\rho_T = 1.5$ is reasonable.
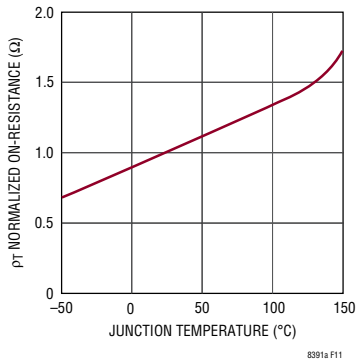

Figure 11. Normalized $R_{DS(ON)}$ vs Temperature

Switch B operates in buck region as the synchronous rectifier. Its power dissipation at maximum output current is given by:

$$P_{B(BUCK)} = \frac{V_{IN} - V_{OUT}}{V_{IN}} \bullet I_{LED(MAX)}^2 \bullet \rho_T \bullet R_{DS(ON)}$$

Switch C operates in boost region as the control switch. Its power dissipation at maximum current is given by:

$$P_{C(BOOST)} = \frac{(V_{OUT} - V_{IN}) \bullet V_{OUT}}{V_{IN}^2} \bullet I_{LED(MAX)}^2 \bullet \rho_T$$

$$\bullet R_{DS(ON)} + k \bullet V_{OUT}^3 \bullet \frac{I_{LED(MAX)}}{V_{IN}} \bullet C_{RSS} \bullet f$$

where C_{RSS} is usually specified by the MOSFET manufacturers. The constant k, which accounts for the loss caused by reverse recovery current, is inversely proportional to the gate drive current and has an empirical value of 1.7.

For switch D, the maximum power dissipation happens in boost region, when its duty cycle is higher than 50%. Its maximum power dissipation at maximum output current is given by:

$$P_{D(BOOST)} = \frac{V_{OUT}}{V_{IN}} \bullet I_{LED(MAX)}^2 \bullet \rho_T \bullet R_{DS(ON)}$$

For the same output voltage and current, typically switch A has the highest power dissipation in buck region at $V_{IN(MAX)}$ and switch C has the highest power dissipation in boost region at $V_{IN(MIN)}$.

From a known power dissipated in the power MOSFET, its junction temperature can be obtained using the following formula:

$$T_J = T_A + P \bullet R_{TH(JA)}$$

The junction-to-ambient thermal resistance $R_{TH(JA)}$ includes the junction-to-case thermal resistance $R_{TH(JC)}$ and the case-to-ambient thermal resistance $R_{TH(CA)}$. This value of T_J can then be compared to the original, assumed value used in the iterative calculation process.

Optional Schottky Diode (D_B, D_D) Selection

The optional Schottky diodes D_B (in parallel with switch B) and D_D (in parallel with switch D) conduct during the dead time between the conduction of the power MOSFET switches. They are intended to prevent the body diode of synchronous switches B and D from turning on and storing charge during the dead time. In particular, D_B significantly reduces reverse recovery current between switch B turn-off and switch A turn-on, and D_D significantly reduces reverse recovery current between switch D turn-off and switch C turn-on. They improve converter efficiency and reduce switch voltage stress. In order for the diode to be effective, the inductance between it and the synchronous switch must be as small as possible, mandating that these components be placed adjacently.

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C_{IN} and C_{OUT} Selection

Input and output capacitance is necessary to suppress voltage ripple caused by discontinuous current moving in and out the regulator. A parallel combination of capacitors is typically used to achieve high capacitance and low equivalent series resistance (ESR). Dry tantalum, special polymer, aluminum electrolytic and ceramic capacitors are all available in surface mount packages. Capacitors with low ESR and high ripple current ratings, such as OS-CON and POSCAP are also available.

Ceramic capacitors should be placed near the regulator input and output to suppress high frequency switching spikes. Ceramic capacitors, of at least 1μF, should also be placed from V_{IN} to GND and V_{OUT} to GND as close to the LT8391A pins as possible. Due to their excellent low ESR characteristics, ceramic capacitors can significantly reduce input ripple voltage and help reduce power loss in the higher ESR bulk capacitors. X5R or X7R dielectrics are preferred, as these materials retain their capacitance over wide voltage and temperature ranges. Many ceramic capacitors, particularly 0805 or 0603 case sizes, have greatly reduced capacitance at the desired operating voltage.

Input Capacitance C_{IN}

Discontinuous input current is highest in buck region due to the switch A toggling on and off. Make sure that the C_{IN} capacitor network has low enough ESR and is sized to handle the maximum RMS current. In buck region, the input RMS current is given by:

$$I_{RMS} \approx I_{LED(MAX)} \bullet \frac{V_{OUT}}{V_{IN}} \bullet \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

The formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{LED(MAX)}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief.

Output Capacitance C_{OUT}

Discontinuous current shifts from the input to the output in the boost region. Make sure that the C_{OUT} capacitor network is capable of reducing the output voltage ripple.

The effects of ESR and the bulk capacitance must be considered when choosing the right capacitor for a given output ripple voltage. The maximum steady state ripple due to charging and discharging the bulk capacitance is given by:

$$\Delta V_{CAP(BOOST)} = \frac{I_{LED} \bullet (V_{OUT} - V_{IN(MIN)})}{C_{OUT} \bullet V_{OUT} \bullet f}$$

$$\Delta V_{CAP(BUCK)} = \frac{V_{OUT} \bullet \left(1 - \dfrac{V_{OUT}}{V_{IN(MAX)}} \right)}{8 \bullet L \bullet f^2 \bullet C_{OUT}}$$

The maximum steady ripple due to the voltage drop across the ESR is given by:

$$\Delta V_{ESR(BOOST)} = \frac{V_{OUT} \bullet I_{LED(MAX)}}{V_{IN(MIN)}} \bullet ESR$$

$$\Delta V_{ESR(BUCK)} = \frac{V_{OUT} \bullet \left(1 - \dfrac{V_{OUT}}{V_{IN(MAX)}} \right)}{L \bullet f} \bullet ESR$$

INTV$_{CC}$ Regulator

An internal P-channel low dropout regulator produces 5V at the INTV$_{CC}$ pin from the V_{IN} supply pin. The INTV$_{CC}$ powers internal circuitry and gate drivers in the LT8391A. The INTV$_{CC}$ regulator can supply a peak current of 145mA and must be bypassed to ground with a minimum of 4.7μF ceramic capacitor. Good local bypass is necessary to supply the high transient current required by MOSFET gate drivers.

Higher input voltage applications with large MOSFETs being driven at higher switching frequencies may cause the maximum junction temperature rating for the LT8391A to be exceeded. The system supply current is normally dominated by the gate charge current. Additional external loading of the INTV$_{CC}$ also needs to be taken into account for the power dissipation calculation. The total LT8391A power dissipation in this case is $V_{IN} \bullet I_{INTVCC}$, and overall efficiency is lowered. The junction temperature can be estimated by using the equation:

$$T_J = T_A + P_D \bullet \theta_{JA}$$

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where θ_{JA} (in °C/W) is the package thermal resistance.

To prevent maximum junction temperature from being exceeded, the input supply current must be checked operating in continuous mode at maximum V_{IN}.

Top Gate MOSFET Driver Supply (C_{BST1}, C_{BST2})

The top MOSFET drivers, TG1 and TG2, are driven between their respective SW and BST pin voltages. The boost voltages are biased from floating bootstrap capacitors C_{BST1} and C_{BST2}, which are normally recharged through both the external and internal bootstrap diodes when the respective top MOSFET is turned off. External bootstrap diodes are recommended because the internal bootstrap diodes are not always strong enough to refresh top MOSFETs at 2MHz. Both capacitors are charged to the same voltage as the $INTV_{CC}$ voltage. The bootstrap capacitors C_{BST1} and C_{BST2}, need to store about 100 times the gate charge required by the top switches A and D. In most applications, a 0.1µF to 0.47µF, X5R or X7R dielectric capacitor is adequate.

Programming V_{IN} UVLO

A resistor divider from V_{IN} to the EN/UVLO pin implements V_{IN} undervoltage lockout (UVLO). The EN/UVLO enable falling threshold is set at 1.214V with 10mV hysteresis. In addition, the EN/UVLO pin sinks 2.5µA when the voltage on the pin is below 1.214V. This current provides user programmable hysteresis based on the value of R1. The programmable UVLO thresholds are:

$$V_{IN(UVLO+)} = 1.233V \cdot \frac{R1+R2}{R2} + 2.5\mu A \cdot R1$$

$$V_{IN(UVLO-)} = 1.220V \cdot \frac{R1+R2}{R2}$$

Figure 12 shows the implementation of external shutdown control while still using the UVLO function. The NMOS grounds the EN/UVLO pin when turned on, and puts the LT8391A in shutdown with quiescent current less than 2µA.

Programming LED Current

The LED current is programmed by placing an appropriate value current sense resistor, R_{LED}, in series with the LED
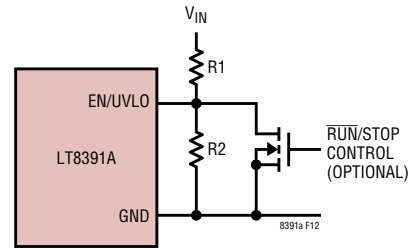

Figure 12. V_{IN} Undervoltage Lockout (UVLO)

string. The voltage drop across R_{LED} is (Kelvin) sensed by the ISP and ISN pins. The CTRL1 and CTRL2 pins should be tied to a voltage higher than 1.35V to get the full-scale 100mV (typical) threshold across the sense resistor. Either the CTRL1 or CTRL2 pin can be used to dim the LED current to zero, although relative accuracy decreases with the decreasing sense threshold. When either the CTRL1 or CTRL2 pin voltage is less than 1.15V, the LED current is:

$$I_{LED} = \frac{Min(V_{CTRL1}, V_{CTRL2}) - 250mV}{10 \cdot R_{LED}}$$

where $Min(V_{CTRL1}, V_{CTRL2})$ is the minimum value of CTRL1 and CTRL2 pin voltages. When $Min(V_{CTRL1}, V_{CTRL2})$ is between 1.15V and 1.35V, the LED current varies with the $Min(V_{CTRL1}, V_{CTRL2})$, but departs from the equation above by an increasing amount as $Min(V_{CTRL1}, V_{CTRL2})$ increases. Ultimately, when $Min(V_{CTRL1}, V_{CTRL2}) > 1.35V$, the LED current no longer varies. The typical $V_{(ISP-ISN)}$ threshold vs $Min(V_{CTRL1}, V_{CTRL2})$ is listed in Table 2.

Table 2. $V_{(ISP-ISN)}$ Threshold vs $Min(V_{CTRL1}, V_{CTRL2})$

$Min(V_{CTRL1}, V_{CTRL2})$ (V)	$V_{(ISP-ISN)}$ (mV)
1.15	90
1.20	94.5
1.25	98
1.30	99.5
1.35	100

When $Min(V_{CTRL1}, V_{CTRL2})$ is higher than 1.35V, the LED current is regulated to:

$$I_{LED} = \frac{100mV}{R_{LED}}$$

The CTRL1/CTRL2 pin should not be left open (tie to V_{REF} if not used). The CTRL1/CTRL2 pin can also be used in

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conjunction with a thermistor to provide overtemperature protection for the LED load, or with a resistor divider to V_{IN} to reduce output power and switching current when V_{IN} is low. The presence of a time varying differential voltage ripple signal across ISP and ISN at the switching frequency is expected. The amplitude of this signal is increased by higher LED load current, lower switching frequency, or smaller value output filter capacitor. Some level of ripple signal is acceptable, and the compensation capacitor on the V_C pin filters the signal so the average difference between ISP and ISN is regulated to the user-programmed value. The ripple voltage amplitude (peak-to-peak) in excess of 20mV should not cause misoperation, but may lead to noticeable offset between the average value and the user-programmed value.

Dimming Control

There are two methods to control the LED current for dimming using the LT8391A. One method uses the CTRL1 or CTRL2 pin to adjust the current regulated in the LEDs. A second method uses the PWM pin to modulate the LED current between zero and full current to achieve a precisely programmed average current.

Compared to the analog dimming method, the PWM dimming method offers much higher dimming ratio without any color shift. To make PWM dimming more accurate, the switch demand current is stored on the V_C node when the PWM signal is low. This feature minimizes recovery time when the PWM signal goes high. To further improve the recovery time, a high side PMOS PWM switch should be used in the LED current path to prevent the output capacitor from discharging during the PWM signal low phase.

The choice of switching frequency, inductor value, and loop compensation affects the minimum PWM on time, below which the LT8391A loses the LED current regulation. For the same application, the LT8391A achieves the highest PWM dimming ratio (up to 2000:1) in buck region, the medium PWM dimming ratio (up to 2000:1) in buck-boost region, and the lowest PWM dimming ratio (up to 1000:1) in boost region.

In either fixed frequency operation set by R_T resistor or spread spectrum frequency operation, the internal oscillator is synchronized to the PWM signal rising edge, thereby providing flicker-free PWM dimming performance. In external frequency synchronization operation, both SYNC and PWM signals must have synchronized rising edges to achieve flicker-free PWM dimming performance.

The LT8391A provides both external PWM dimming and internal PWM dimming. For external PWM dimming, choose R_P resistor less than 30k and apply external PWM clock signal on the PWM pin. For internal PWM dimming, choose R_P resistor to one of the five resistor values in Table 3 and apply analog DC voltage or a resistor divider from V_{REF} to the PWM pin. The R_P resistor sets the internal PWM dimming frequency, and the analog DC voltage on the PWM pin from 1V to 2V sets the internal PWM dimming duty ratio from 0% to 100% with a discrete 1/128 step size in Figure 13. A 1μF ceramic capacitor on the PWM pin is recommended to minimize the internal PWM dimming duty ratio jitter caused by switching noise.

Table 3. Internal PWM Dimming Frequency vs R_P Value (5% Resistor)

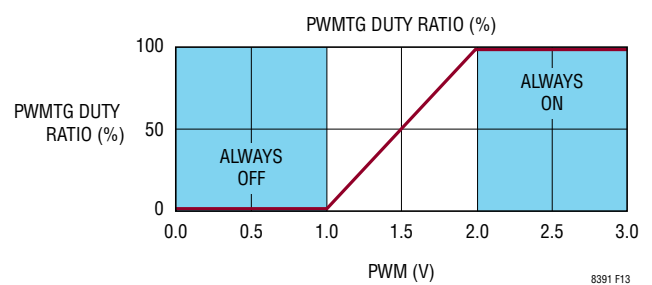| R_P (k)	f_{SW}	f_{SW} = 1MHz	f_{SW} = 1.5MHz	f_{SW} = 2MHz
≤ 30	External	External	External	External
51	f_{SW}/256	3.9kHz	5.9kHz	7.8kHz
82	f_{SW}/512	2.0kHz	2.9kHz	3.9kHz
130	f_{SW}/1024	1.0kHz	1.5kHz	2.0kHz
200	f_{SW}/2048	0.49kHz	0.73kHz	0.98kHz
300	f_{SW}/4096	0.24kHz	0.37kHz	0.49kHz

Figure 13. Internal PWM Dimming Duty Ratio vs PWM Voltage

High Side PMOS PWM Switch Selection

A high side PMOS PWM switch is recommended in most LT8391A applications to maximize the PWM dimming ratio and protect the LED string during fault conditions. Compared to a low side NMOS PWM switch, the high side PMOS PWM switch allows a single wire to the LED string

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and ground return path through chassis. The high side PMOS PWM switch is typically selected for drain-source voltage V_{DS}, gate-source threshold voltage $V_{GS(TH)}$, and continuous drain current I_D. For proper operations, V_{DS} rating should exceed the open LED regulation voltage set by the FB pin, the absolute value of $V_{GS(TH)}$ should be less than 3V, and I_D rating should be above $I_{LED(MAX)}$.

Programming Output Voltage and Thresholds

The LT8391A has a voltage feedback pin FB that can be used to program a constant-voltage output. The output voltage can be set by selecting the values of R3 and R4 (Figure 14) according to the following equation:

$$V_{OUT} = 1.00\,V \bullet \frac{R3 + R4}{R4}$$
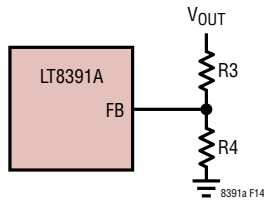
Figure 14. Feedback Resistor Connection

In addition, the FB pin also sets output overvoltage threshold, open LED threshold, and short LED threshold. For an LED driver application with small output capacitors, the output voltage usually overshoots a lot during an open LED event. Although the 1.00V FB regulation loop tries to regulate the output, the loop is usually too slow to prevent the output from overshooting. Once the FB pin hits its overvoltage threshold 1.05V, the LT8391A stops switching by turning off TG1, BG1, TG2, and BG2, and also turns off PWMTG to disconnect the LED string for protection. The output overvoltage threshold can be set as:

$$V_{OUT(OVP)} = 1.05\,V \bullet \frac{R3 + R4}{R4}$$

Make sure the expected V_{FB} during normal operation stays between the short LED rising threshold 0.3V and the open LED falling threshold 0.9V:

$$0.3\,V \le V_{LED} \bullet \frac{R4}{R3 + R4} \le 0.9\,V$$

These equations set the maximum LED string voltage with full open LED protection for the LT8391A to be 51V.

$\overline{FAULT}$ Pin

The LT8391A provides an open-drain status pin, $\overline{FAULT}$, which is pulled low during either open LED or short LED conditions. The open LED condition happens when the FB pin is above 0.95V and the voltage across $V_{(ISP-ISN)}$ is less than 10mV. The short LED condition happens when the FB pin is below 0.25V. The $\overline{FAULT}$ status is updated when the SS pin is above 1.75V and the PWM signal is high.

Soft-Start and Fault Protection

As shown in Figure 8 and explained in the Operation section, the SS pin can be used to program soft-start by connecting an external capacitor from the SS pin to ground. The internal 12.5µA pull-up current charges up the capacitor, creating a voltage ramp on the SS pin. As the SS pin voltage rises linearly from 0.25V to 1V (and beyond), the output voltage rises smoothly and transitions into LED current regulation. The soft-start range is defined to be the voltage range from 0V to the FB voltage in LED current regulation. The soft-start time can be calculated as:

$$t_{SS} = V_{LED} \bullet \frac{R4}{R3 + R4} \bullet \frac{C_{SS}}{12.5\,\mu A}$$

Make sure the C_{SS} is at least five to ten times larger than the compensation capacitor on the V_C pin. A 22nF ceramic capacitor is a good starting point.

The SS pin is also used as a fault timer. Once an open LED or a short LED fault is detected, a 1.25µA pull-down current source is activated. Using a single resistor from the SS pin to the V_{REF} pin, the LT8391A can be set to three different fault protection modes: hiccup (no resistor), latch-off (499k), and keep-running (100k).

With a 100k resistor in keep-running mode, the LT8391A continues switching normally, either regulating the programmed V_{OUT} during open LED fault or regulating the current during short LED fault. With a 499k resistor in latch-off mode, the LT8391A stops switching until the EN/UVLO pin is pulled low and high to restart. With no resistor in hiccup mode, the LT8391A enters low duty

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cycle auto-retry operation. The 1.25µA pull-down current discharges the SS pin to 0.2V and then 12.5µA pull-up current charges the SS pin up. If the fault condition has not been removed when the SS pin reaches 1.75V, the 1.25µA pull-down current turns on again, initiating a new hiccup cycle. This will continue until the fault is removed.

Loop Compensation

The LT8391A uses an internal transconductance error amplifier, the output of which, V_C, compensates the control loop. The external inductor, output capacitor, and the compensation resistor and capacitor determine the loop stability.

The inductor and output capacitor are chosen based on performance, size and cost. The compensation resistor and capacitor on the V_C pin are set to optimize control loop response and stability. For a typical LED application, a 2.2nF compensation capacitor on the V_C pin is adequate, and a series resistor should always be used to increase the slew rate on the V_C pin to maintain tighter regulation of LED current during fast transients on the input supply of the converter.

Efficiency Considerations

The power efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Although all dissipative elements in circuits produce losses, four main sources account for most of the losses in LT8391A circuits:

1. DC I^2R losses. These arise from the resistances of the MOSFETs, sensing resistor, inductor and PC board traces and cause the efficiency to drop at high output currents.

2. Transition loss. This loss arises from the brief amount of time switch A or switch C spends in the saturated region during switch node transitions. It depends upon the input voltage, load current, driver strength and MOSFET capacitance, among other factors.

3. $INTV_{CC}$ current. This is the sum of the MOSFET driver and control currents.

4. C_{IN} and C_{OUT} loss. The input capacitor has the difficult job of filtering the large RMS input current to the regulator in buck region. The output capacitor has the difficult job of filtering the large RMS output current in boost region. Both C_{IN} and C_{OUT} are required to have low ESR to minimize the AC I^2R loss and sufficient capacitance to prevent the RMS current from causing additional upstream losses in fuses or batteries.

5. Other losses. Schottky diode D_B and D_D are responsible for conduction losses during dead time and light load conduction periods. Inductor core loss occurs predominately at light loads. Switch A causes reverse recovery current loss in buck region, and switch C causes reverse recovery current loss in boost region.

When making adjustments to improve efficiency, the input current is the best indicator of changes in efficiency. If you make a change and the input current decreases, then the efficiency has increased. If there is no change in the input current, then there is no change in efficiency.

PC Board Layout Checklist

The basic PC board layout requires a dedicated ground plane layer. Also, for high current, a multilayer board provides heat sinking for power components.
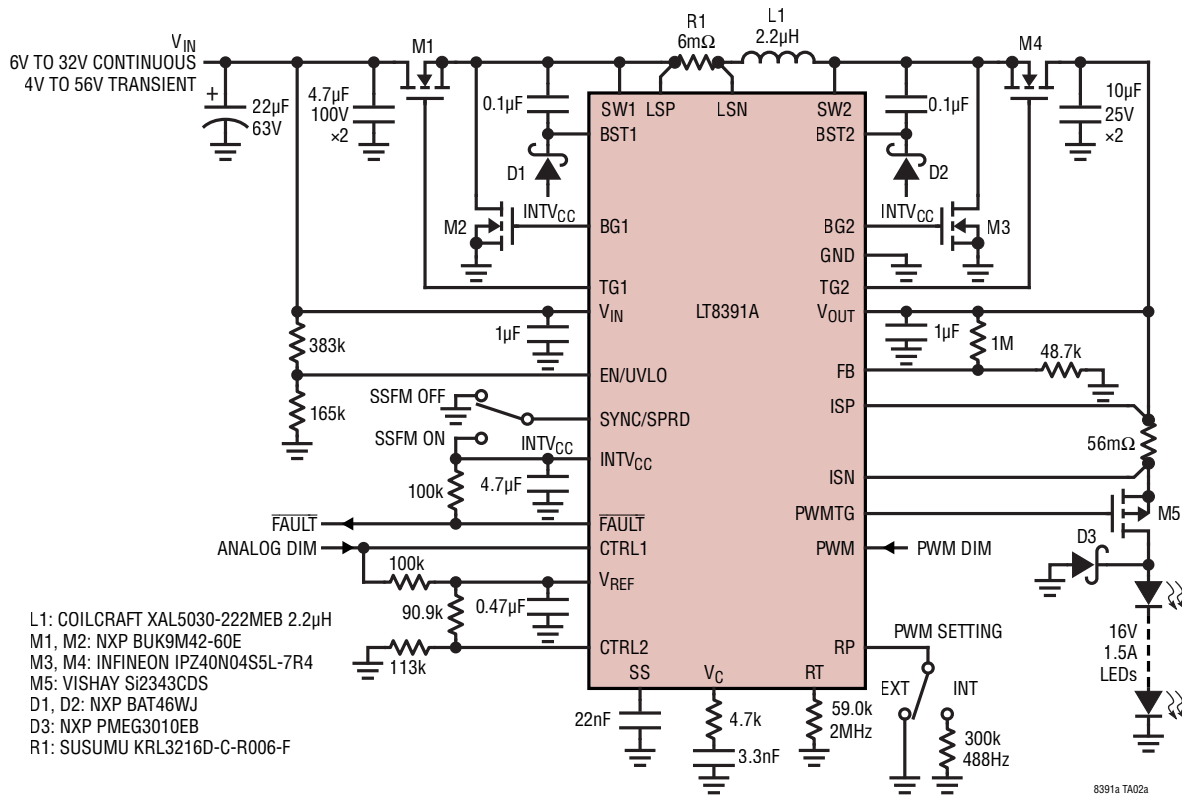
- The ground plane layer should not have any traces and it should be as close as possible to the layer with power MOSFETs.
- Place C_{IN}, switch A, switch B and D_B in one compact area. Place C_{OUT}, switch C, switch D and D_D in one compact area.
- Use immediate vias to connect the components to the ground plane. Use several large vias for each power component.
- Use planes for V_{IN} and V_{OUT} to maintain good voltage filtering and to keep power losses low.

APPLICATIONS INFORMATION

- Flood all unused areas on all layers with copper. Flooding with copper will reduce the temperature rise of power components. Connect the copper areas to any DC net (V_{IN} or GND).
- Separate the signal and power grounds. All small-signal components should return to the exposed GND pad from the bottom, which is then tied to the power GND close to the sources of switch B and switch C.
- Place switch A and switch C as close to the controller as possible, keeping the power GND, BG and SW traces short.
- Keep the high dV/dT SW1, SW2, BST1, BST2, TG1 and TG2 nodes away from sensitive small-signal nodes.
- The path formed by switch A, switch B, D_B and the C_{IN} capacitor should have short leads and PCB trace lengths. The path formed by switch C, switch D, D_D and the C_{OUT} capacitor also should have short leads and PCB trace lengths.
- The output capacitor (–) terminals should be connected as close as possible to the (–) terminals of the input capacitor.

- Connect the top driver bootstrap capacitor C_{BST1} closely to the BST1 and SW1 pins. Connect the top driver bootstrap capacitor C_{BST2} closely to the BST2 and SW2 pins.
- Connect the input capacitors C_{IN} and output capacitors C_{OUT} closely to the power MOSFETs. These capacitors carry the MOSFET AC current.
- Route LSP and LSN traces together with minimum PCB trace spacing. Avoid sense lines pass through noisy areas, such as switch nodes. The filter capacitor between LSP and LSN should be as close as possible to the IC. Ensure accurate current sensing with Kelvin connections at the R_{SENSE} resistor. A low ESL sense resistor is recommended.
- Connect the V_C pin compensation network close to the IC, between V_C and the signal ground. The capacitor helps to filter the effects of PCB noise and output voltage ripple voltage from the compensation loop.
- Connect the $INTV_{CC}$ bypass capacitor, C_{INTVCC}, close to the IC, between the $INTV_{CC}$ and the power ground. This capacitor carries the MOSFET drivers' current peaks.
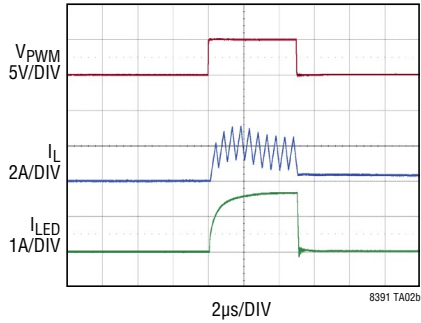
TYPICAL APPLICATIONS

### 94% Efficient 24W (16V 1.5A) 2MHz Buck-Boost LED Driver with Fault Protection

L1: COILCRAFT XAL5030-222MEB 2.2µH
M1, M2: NXP BUK9M42-60E
M3, M4: INFINEON IPZ40N04S5L-7R4
M5: VISHAY Si2343CDS
D1, D2: NXP BAT46WJ
D3: NXP PMEG3010EB
R1: SUSUMU KRL3216D-C-R006-F

8391a TA02a

TYPICAL APPLICATIONS

100Hz 2000:1 External PWM Dimming (V_IN = 32V)

8391 TA02b

100Hz 2000:1 External PWM Dimming (V_IN = 18V)

8391 TA02c
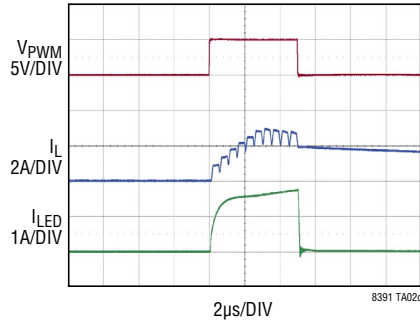
100Hz 800:1 External PWM Dimming (V_IN = 8V)

8391 TA02d
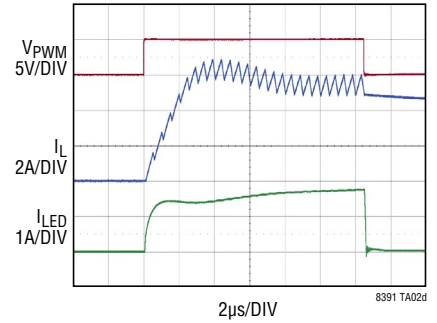
OPEN LED Protection: Hiccup Mode (R_SS = Open)

8391a TA02e
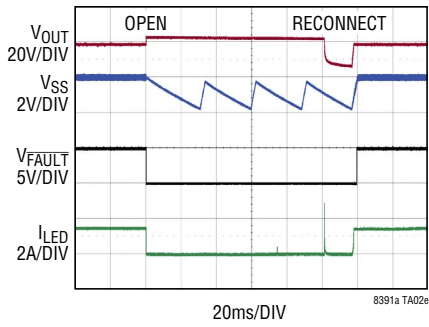
OPEN LED Protection: Latch-Off Mode (R_SS = 499k)

8391a TA02f
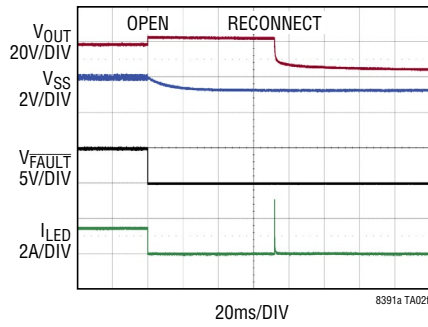
OPEN LED Protection: Keep-Running Mode (R_SS = 100k)

8391a TA02g

Rev. A

For more information www.analog.com
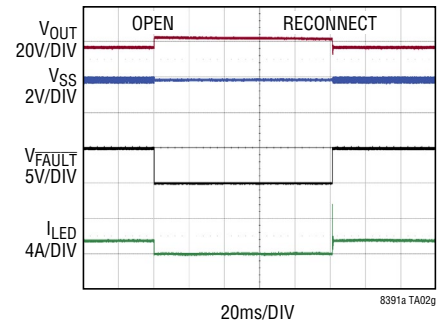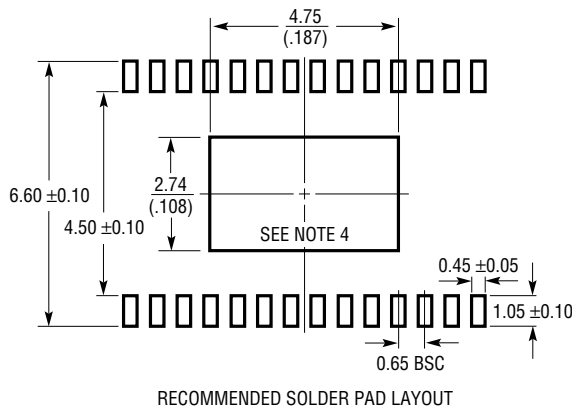
PACKAGE DESCRIPTION

FE Package
28-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1663 Rev L)
Exposed Pad Variation EB

4.75
(.187)

6.60 ±0.10
4.50 ±0.10

2.74
(.108)

SEE NOTE 4

0.45 ±0.05

1.05 ±0.10

0.65 BSC

RECOMMENDED SOLDER PAD LAYOUT

9.60 – 9.80*
(.378 – .386)

4.75
(.187)

28 27 26 25 24 23 22 21 20 19 18 17 16 15

EXPOSED
PAD HEAT SINK
ON BOTTOM OF
PACKAGE

2.74
(.108)

6.40
(.252)
BSC

1 2 3 4 5 6 7 8 9 10 11 12 13 14

4.30 – 4.50*
(.169 – .177)

0.25
REF

0° – 8°

0.09 – 0.20
(.0035 – .0079)

0.50 – 0.75
(.020 – .030)

1.20
(.047)
MAX

0.65
(.0256)
BSC

0.195 – 0.30
(.0077 – .0118)
TYP

0.05 – 0.15
(.002 – .006)

FE28 (EB) TSSOP REV L 0117

NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN MILLIMETERS
   (INCHES)
3. DRAWING NOT TO SCALE

4. RECOMMENDED MINIMUM PCB METAL SIZE
   FOR EXPOSED PAD ATTACHMENT

*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH
 SHALL NOT EXCEED 0.150mm (.006") PER SIDE

Rev. A

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PACKAGE DESCRIPTION

UFD Package
28-Lead Plastic QFN (4mm × 5mm)
(Reference LTC DWG # 05-08-1712 Rev C)
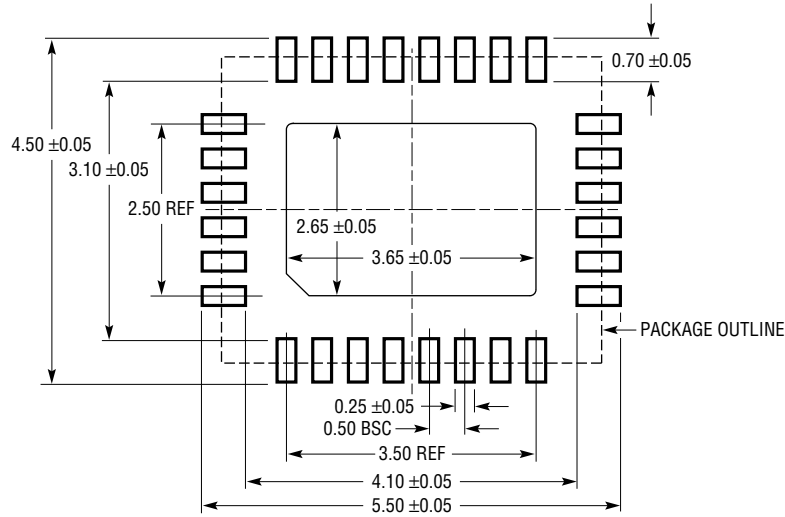
RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED

BOTTOM VIEW—EXPOSED PAD

(UFD28) QFN 0816 REV C
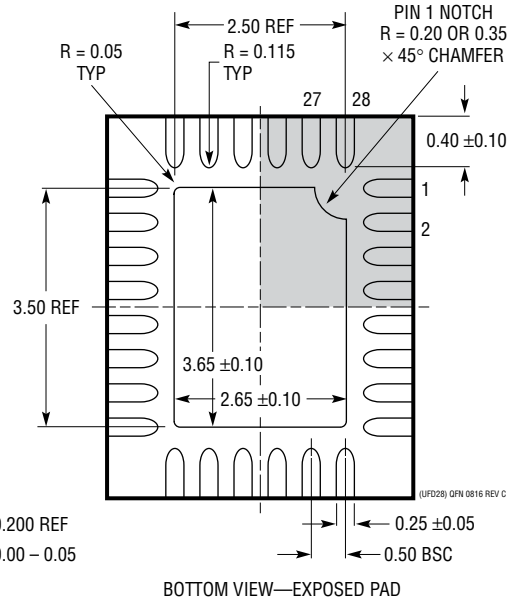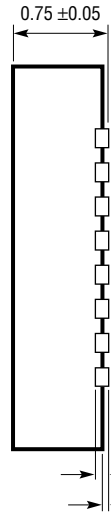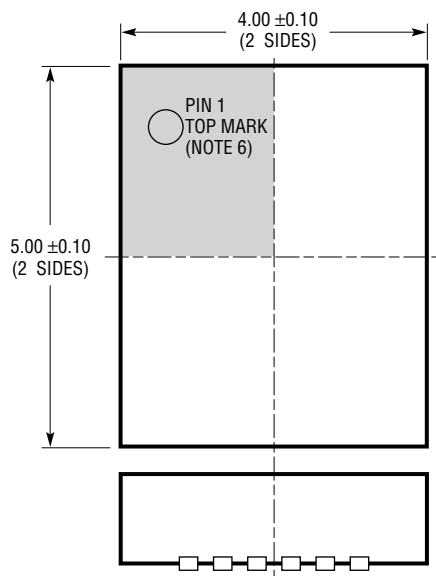
NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGHD-3).
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION
   ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	06/21	Added AEC-Q100 Qualified for Automotive Applications to Features section.	1
		Added LT8391J to Operating Junction Temperature Range section.	2
		Changed theta J_A to 43°C/W of UFD Package.	2
		Added "AUTOMOTIVE PRODUCTS**" and supplemental text to Ordering Information table.	3
		Updated Note 2.	7