2.5A Monolithic Active Cell Balancer with Telemetry Interface

FEATURES

- **2.5A Typical Average Cell Discharge Current**
- **Integrated 6A, 50V Power Switch**
- **Integrates Seamlessly with LTC680x Family: No Additional Software Required**
- **Selectable Current and Temperature Monitors**
- **Ultralow Quiescent Current in Shutdown**
- **Engineered for ISO 26262 Compliant Systems**
- **Isolated Balancing:**
  - **Can Return Charge to Top of Stack**
  - **Can Return Charge to Any Combination of Cells in Stack**
  - **Can Return Charge to 12V Battery for Alternator Replacement**
- Can Be Paralleled for Greater Discharge Capability
- All Quiescent Current in Operation Taken from Local Cell
- 16-Lead TSSOP Package

APPLICATIONS

- Active Battery Stack Balancing
- Electric and Hybrid Electric Vehicles
- Fail-Safe Power Supplies
- Energy Storage Systems

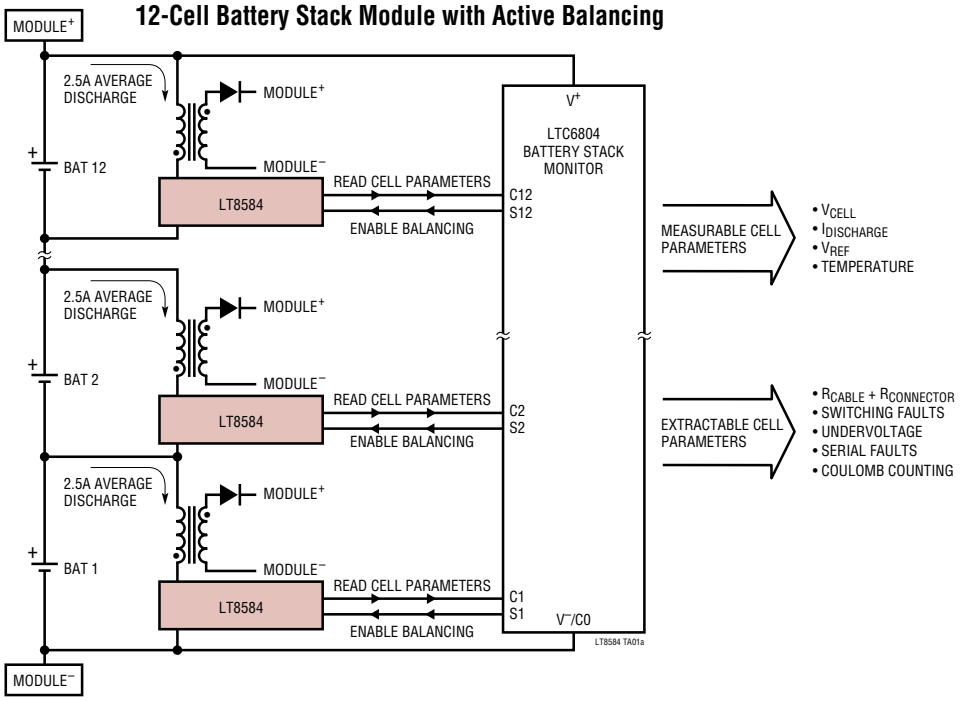
DESCRIPTION

The LT®8584 is a monolithic flyback DC/DC converter designed to actively balance high voltage stacks of batteries. The high efficiency of a switching regulator significantly increases the achievable balancing current while reducing heat generation. Active balancing also allows for capacity recovery in stacks of mismatched batteries, a feat unattainable with passive balance systems. In a typical system, greater than 99% of the total battery capacity can be recovered.

The LT8584 includes an integrated 6A, 50V power switch, reducing the design complexity of the application circuit. The part runs completely off of the cell which it is discharging, removing the need for complicated biasing schemes commonly required for external power switches. The enable pin (D_{IN}) of the part is designed to work seamlessly with the LTC680x family of battery stack voltage monitoring ICs. The LT8584 also provides system telemetry including current and temperature monitoring when used with the LTC680x family of parts. When the LT8584 is disabled, less than 20nA of total quiescent current is typically consumed from the battery.

TYPICAL APPLICATION

12-Cell Battery Stack Module with Active Balancing

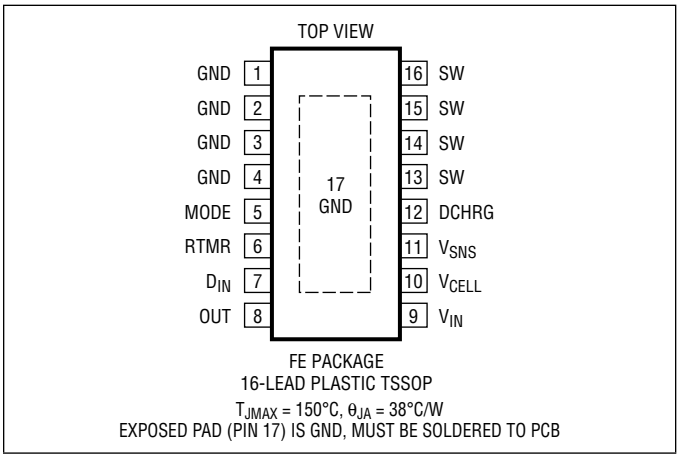


ABSOLUTE MAXIMUM RATINGS

(Note 1)

D_{IN} to GND Voltage ..... ±10V
V_{IN}, V_{CELL}, V_{SNS}, MODE, OUT,
DCHRG Voltage..... –0.3V to 9V
RTMR Voltage..... (Note 2)
SW Voltage (Note 3) ..... –0.4V to 50V
V_{IN} – V_{CELL} Voltage.....±200mV
V_{IN} – V_{SNS} Voltage .....±200mV
MODE – V_{IN} Voltage.....200mV
V_{SNS}, MODE Pin Current..... ±1mA
V_{CELL}, OUT Pin Current..... ±10mA
SW Pin Negative Current .....–2A
Operating Junction Temperature Range (Note 4)
LT8584E..... –40°C to 125°C
LT8584I..... –40°C to 125°C
LT8584H ..... –40°C to 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)..... 300°C

PIN CONFIGURATION



FE PACKAGE
16-LEAD PLASTIC TSSOP
T_{JMAX} = 150°C, θ_{JA} = 38°C/W
EXPOSED PAD (PIN 17) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT8584EFE#PBF	LT8584EFE#TRPBF	8584FE	16-Lead Plastic TSSOP	–40°C to 125°C
LT8584IFE#PBF	LT8584IFE#TRPBF	8584FE	16-Lead Plastic TSSOP	–40°C to 125°C
LT8584HFE#PBF	LT8584HFE#TRPBF	8584FE	16-Lead Plastic TSSOP	–40°C to 150°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 4.2V, D_{IN} = GND unless otherwise noted. (Note 4)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN} Recommended Voltage Range	Switching Nonswitching	● ●	2.5 2.45		5.3 5.3	V
V_{IN} Quiescent Current	Switching Nonswitching In Shutdown, D_{IN} = OUT In Shutdown, D_{IN} = OUT	 ● ●		45 2.5 1	 3 90 1	mA mA nA µA
V_{IN} UVLO		●	2.1		2.45	V
Switch DC Current Limit		●	6	6.3	6.8	A
Current Limit Blanking Time				450		ns
Switch V_{CESAT}	I_{SW} = 4A			200		mV
Switch Leakage Current	V_{SW} = 4.2V V_{SW} = 4.2V	 ●		5	70 4	nA µA
Switch Maximum On Time		●	30	50	70	µs
Switch Short Detection Timeout	Note 5	●	0.5	0.85	1.2	µs
Switch Clamp Voltage	I_{SW} = 2mA I_{SW} = 6A		42	45 50	48	V V
Switch Clamp Blanking Time	Note 6		80	200	360	ns
DCM Comparator Trip Voltage	$V_{SW} - V_{VIN}$	●	40	95	150	mV
DCM Comparator Propagation Delay	200mV Overdrive	●		100	180	ns
DCM Blanking Time				230		ns
MODE Threshold				1.7		V
D_{IN} Shutdown Threshold	High → Low, Referred to GND	●	1	1.2	1.4	V
D_{IN} Shutdown Threshold Hysteresis				100		mV
D_{IN} Data Threshold	High → Low, $V_{TH} = V_{OUT} - V_{DIN}$, MODE = 0V	●	0.3	0.7	0.9	V
D_{IN} Data Threshold Hysteresis	$V_{TH} = V_{OUT} - V_{DIN}$, MODE = 0V	●	20	80	160	mV
D_{IN} Pin Current	V_{DIN} = 0V V_{DIN} = –1V	●	–6 –18	–3 –14	–1 –6	µA µA
DCHRG Threshold	MODE Tied to V_{IN}	●	0.5	0.8	1.1	V
DCHRG Hysteresis	MODE Tied to V_{IN}			100		mV
DCHRG Pull-down Current	Pin Voltage = 0.4V	●	220	300		µA
DCHRG Pull-up Current	Pin Voltage = V_{IN} – 0.4V	●	220	300		µA
RMTR Pin High Voltage	R_{RTMR} = 50kΩ			1.22		V
RMTR Pin Low Voltage	R_{RTMR} = 50kΩ			0		V
V_{CELL} Switch R_{DSON}				55		Ω
V_{SNS} Dynamic Input Range	Gain Error ≤ 8%	●	–30		70	mV
V_{SNS} Average Input Range	Gain Error ≤ 3%	●	15		45	mV
V_{SNS} Amplifier Input Referred Offset	$V_{CELL} - V_{SNS}$ = 40mV	●	–1.1		1.1	mV
V_{SNS} Amplifier Gain	Over V_{SNS} Average Input Range	●	18.7	19	19.3	V/V
Handshake Voltage Error	Measured ± with Respect to: V_{MODE1} = 0.2V V_{MODE2} = 0.4V V_{MODE3} = 0.6V V_{MODE4} = 0.8V $V_{SW,ERR}$ = 1.2V V_{FAULT} = 1.4V V_{FAULT} = 1.4V	 ● ● ● ● ● ● 	 –13 –14 –18 –22 –31 –35 –28		 13 14 18 22 31 35 28	 mV mV mV mV mV mV mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 4.2V, D_{IN} = GND unless otherwise noted. (Note 4)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Handshake Voltage Line Regulation	From V_{VIN} = 2.5V to V_{VIN} = 4.2V			0.2	0.75	%/V
V_{TEMP} Temperature Coefficient (TC)	Note 7, °K = (V_{CELL} – V_{TEMP})/TC			2		mV/°K
V_{TEMP}	V_{TEMP} = V_{IN} – V_{OUT}, T_J = 25°C			0.658		V
OUT Pin Clamp Voltage	10mA Sourced from Pin	●	1.53	1.6		V
OUT Pin Amplifier Load Regulation	I_{OUT} = 10µA to 1mA	●	0	0.2	0.4	%/mA

TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. MODE = 0V. Refer to Timing Diagram for parameter definition. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_W	Decode Window Duration	R_{RTMR} = 10kΩ	●	1.76	1.86	1.96	ms
		R_{RTMR} = 50kΩ	●	8	8.4	8.8	ms
		R_{RTMR} = 100kΩ	●	15.6	16.4	17.2	ms
		R_{RTMR} = 200kΩ	●	29.3	31.5	33.7	ms
	Decode Window Range		●	1.76		33.7	ms
t_{RST}	D_{IN} Serial Communication Reset Time		●	10			µs
t_1	RTMR Start-Up Time	R_{RTMR} = 10kΩ	●		1.8	5	µs
t_2	D_{IN} Hold-Off Time		●	50			µs
t_3	D_{IN} High Time		●	50			µs
t_4	D_{IN} Low Time		●	50			µs
t_5	Discharger Activation Time	R_{RTMR} = 10kΩ			900		ns
t_6	Discharger Deactivation Time				2.1		µs
SR	D_{IN} Slew Rate		●	9			V/ms

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Do not apply a positive or negative voltage or current source to RTMR, otherwise permanent damage may occur.

Note 3: ABSMAX rating refers to the maximum DC + AC leakage spike. Do not exceed 40V_{DC} on any of the SW pins.

Note 4: The LT8584E is guaranteed to meet performance specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization, and correlation with statistical process controls. The LT8584I is guaranteed over the full –40°C to 125°C operating junction temperature range. The LT8584H is guaranteed over the full –40°C to 150°C operating junction temperature range.

Note 5: This is a measure of time duration from the onset of the switch turning on to the time the short-circuit protection circuit is disabled. If the current comparator trips during this duration, the switch error latch is set. This indicates that the connection to the transformer primary is most likely shorted.

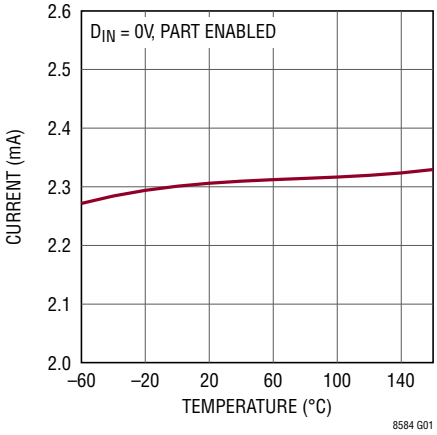
Note 6: This is a measure of time duration for the switch clamp to operate continuously without setting the switch error latch. If the switch clamp remains engaged longer than the switch clamp blanking time, the switch error latch is set and switching is disabled.

Note 7: The voltage proportional to temperature (V_{TEMP}) is measured on the OUT pin while in analog multiplexer MODE 3 or 4. V_{TEMP} must be subtracted from the V_{CELL} voltage that is measured while in analog mux MODE 1. Both measurements should be taken within 100ms of each other to reduce errors in absolute temperature calculation.

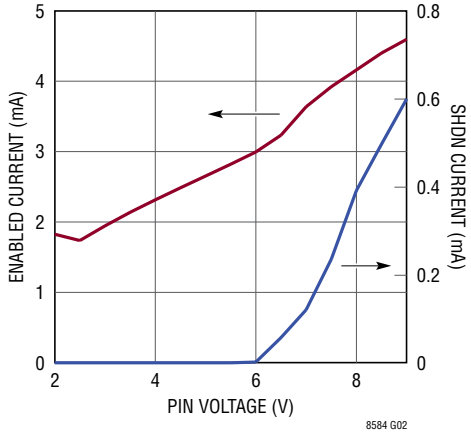
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{IN} = V_{CELL} = V_{SNS} = 4.2V, unless otherwise noted.

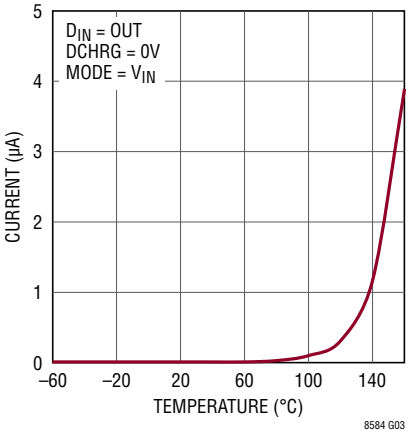
V_{IN} Pin Current Switching Disabled



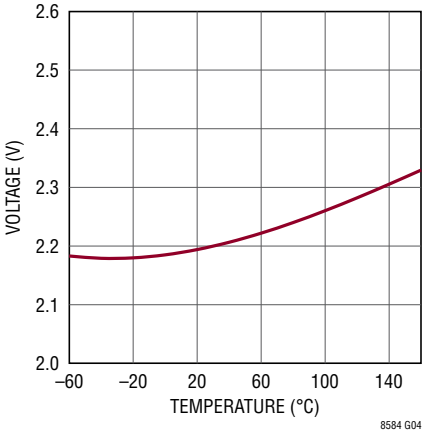
V_{IN} Pin Current



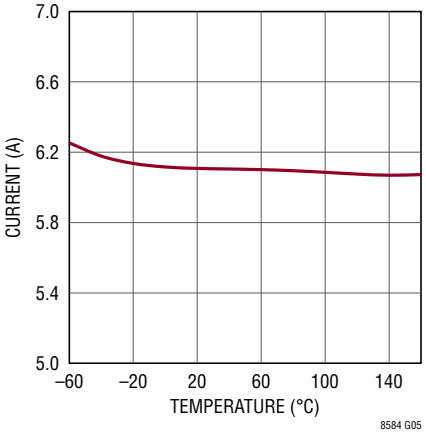
Total Input Leakage I_{VIN} + I_{VCELL} + I_{VSNS} + I_{SW}



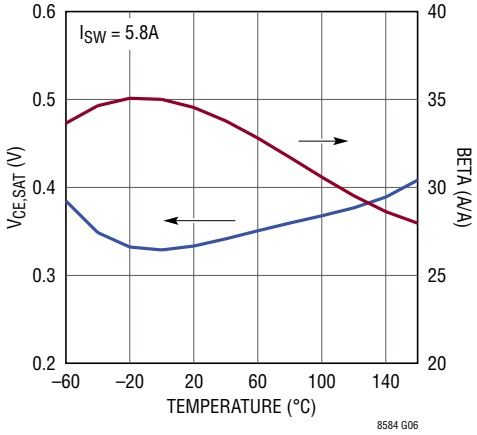
V_{IN} Internal UVLO



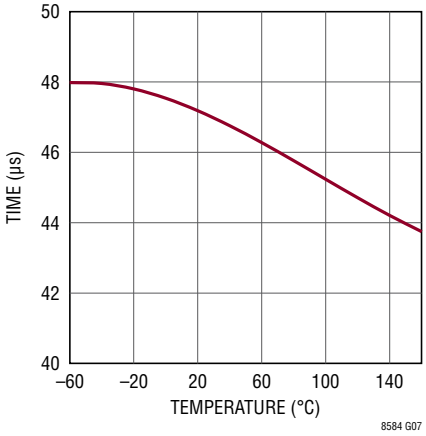
Switch Current Limit



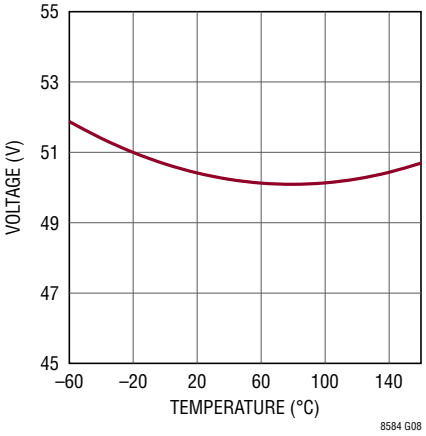
Switch Characteristics



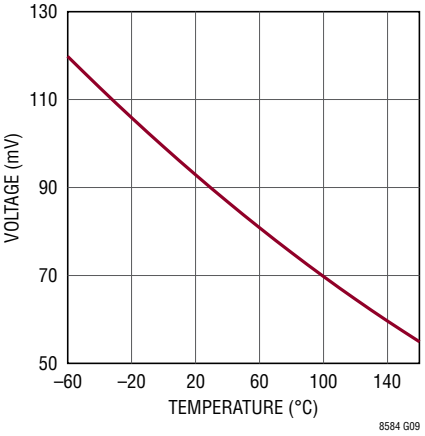
Switch Maximum On-Time



Switch Clamp Voltage (I_{SW} = 6A)



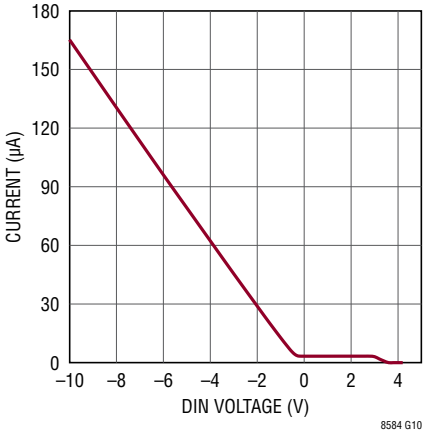
DCM Comparator Threshold



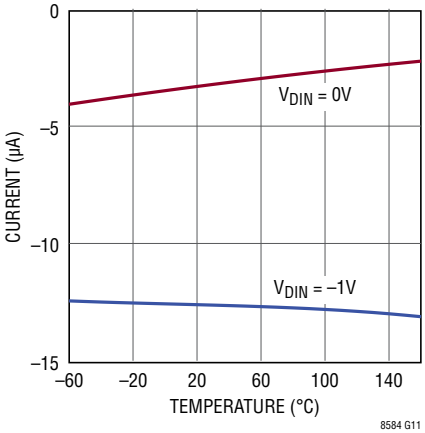
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{IN} = V_{CELL} = V_{SNS} = 4.2V, unless otherwise noted.

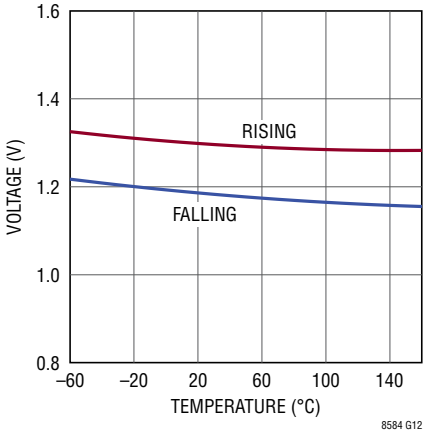
D_{IN} Pin Current



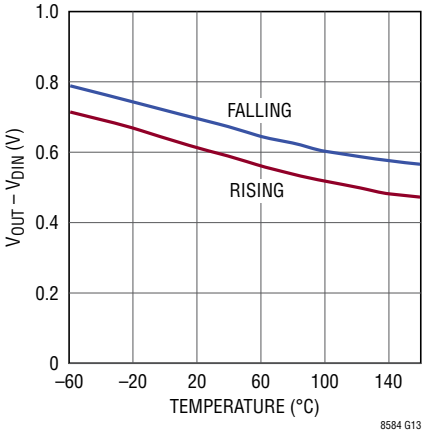
D_{IN} Pin Current



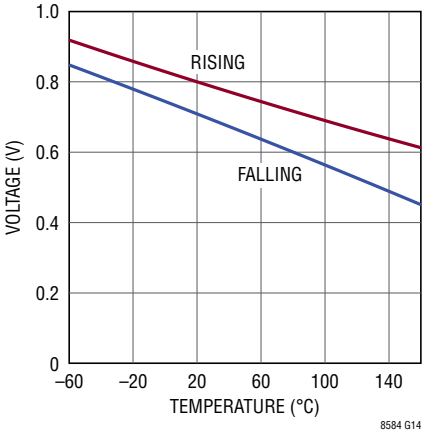
D_{IN} SHDN Threshold



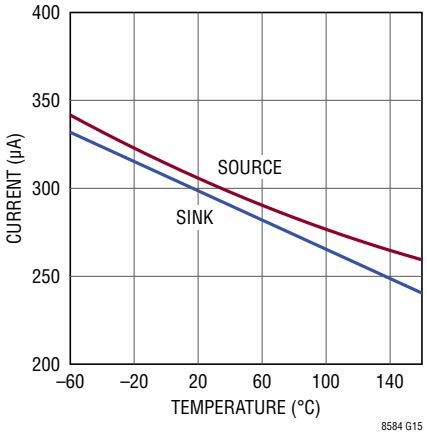
D_{IN} Data Threshold



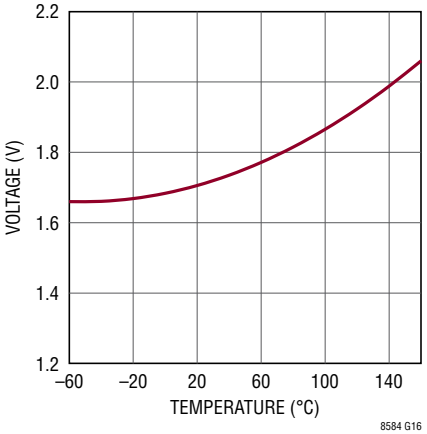
DCHRG Threshold (Simple Mode)



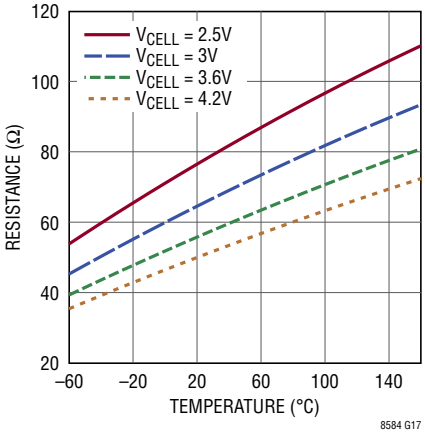
DCHRG Drive Current (Serial Mode)



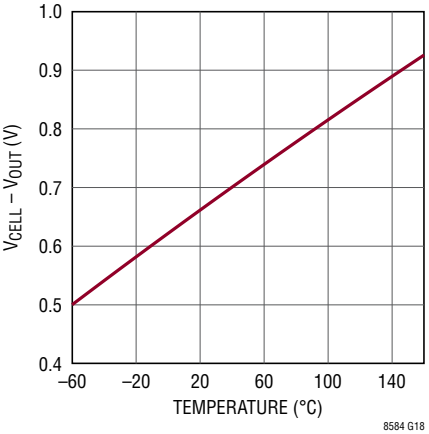
MODE Pin Threshold



V_{CELL} Switch $R_{DS(ON)}$



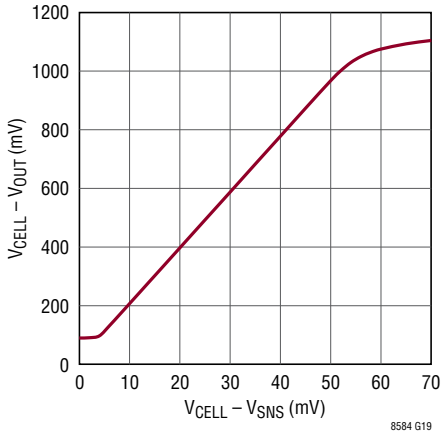
V_{TEMP}



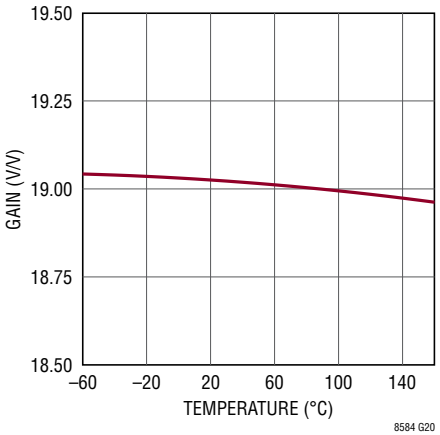
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{IN} = V_{CELL} = V_{SNS} = 4.2V, unless otherwise noted.

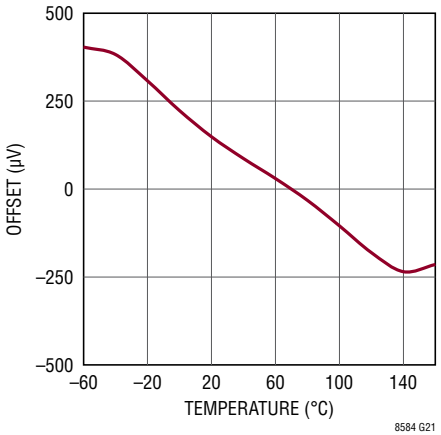
V_{SNS} Transfer Function



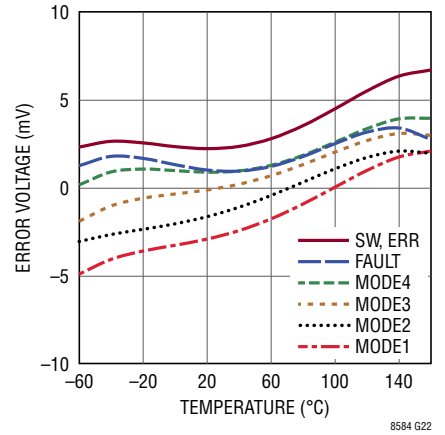
V_{SNS} Amplifier Gain



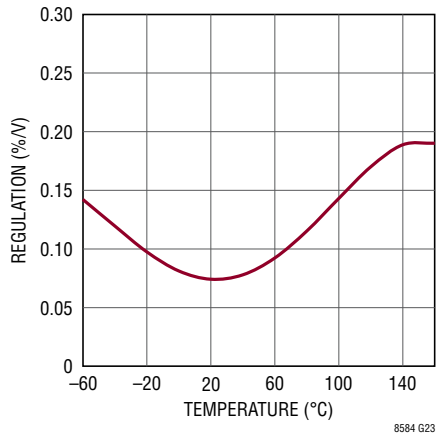
V_{SNS} Amplifier Input Referred Offset



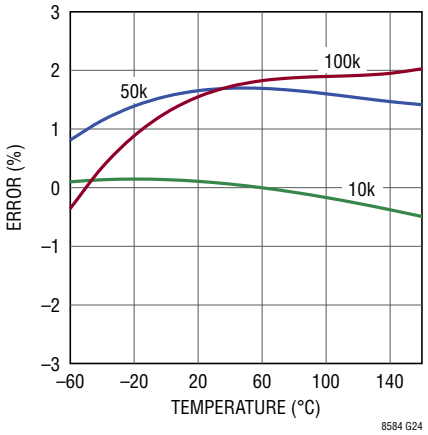
Handshake Voltage Error



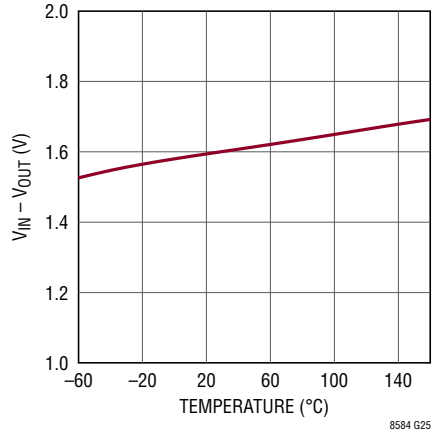
Handshake Voltage Line Regulation



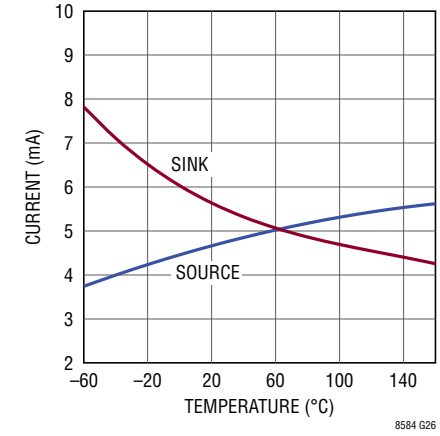
Decode Window Duration Error



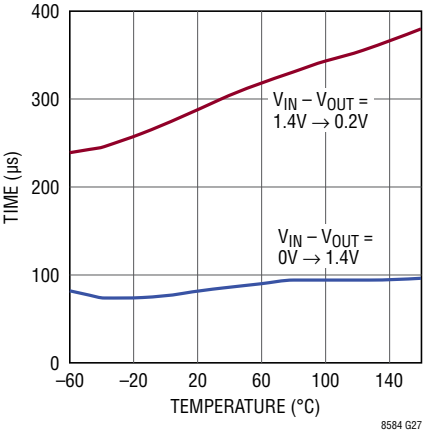
OUT Pin Clamp Voltage
I_{OUT} = 10mA



OUT Pin Amplifier Drive Current



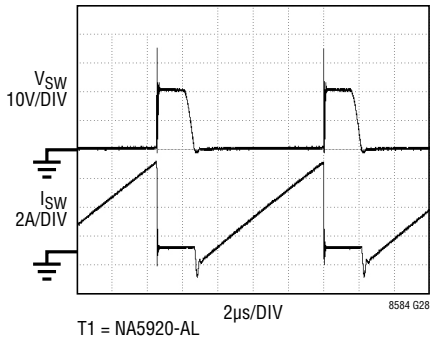
OUT Pin Amplifier
1% Settling Time, C_{OUT} = 220nF



TYPICAL PERFORMANCE CHARACTERISTICS

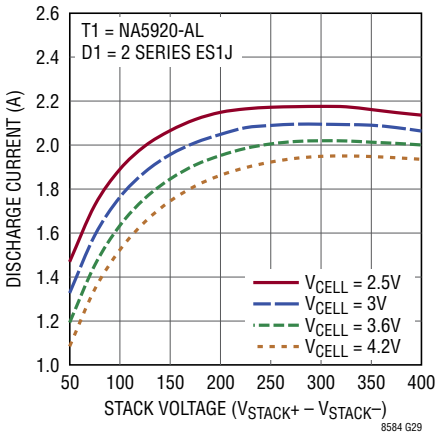
T_A = 25°C, V_{IN} = V_{CELL} = V_{SNS} = 4.2V, unless otherwise noted.

Switching Waveform

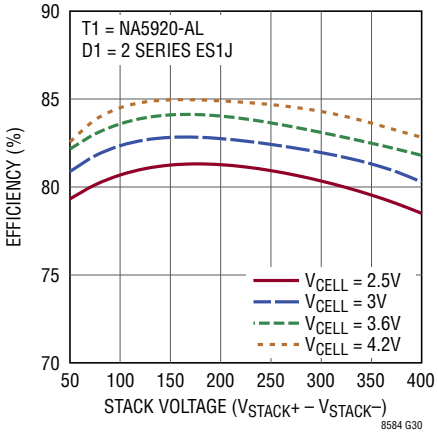


T1 = NA5920-AL
D1 = 2 SERIES ES1J
V_{CELL} = 4.2V
V_{STACK} = 400V

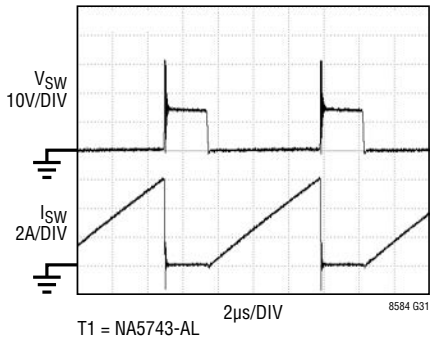
Average Discharge Current



Conversion Efficiency

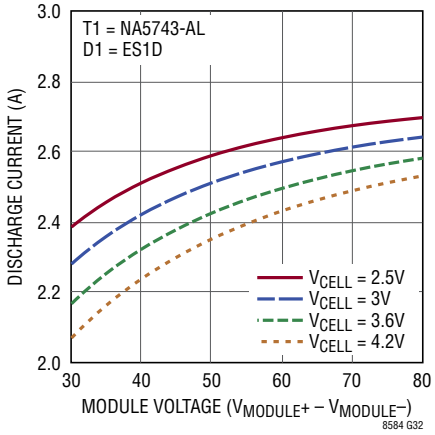


Switching Waveform

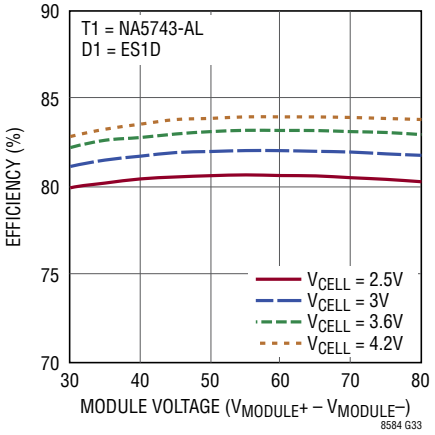


T1 = NA5743-AL
D1 = ES1D
V_{CELL} = 3.6V
V_{MODULE} = 40V
RCD SNUBBER = 4.99kΩ, 22nF

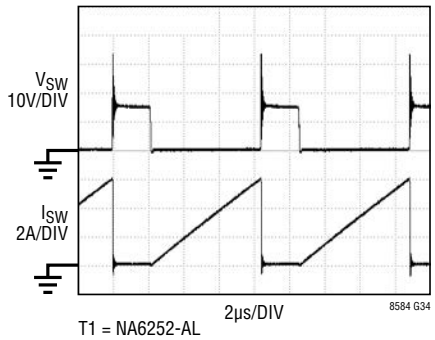
Average Discharge Current



Conversion Efficiency

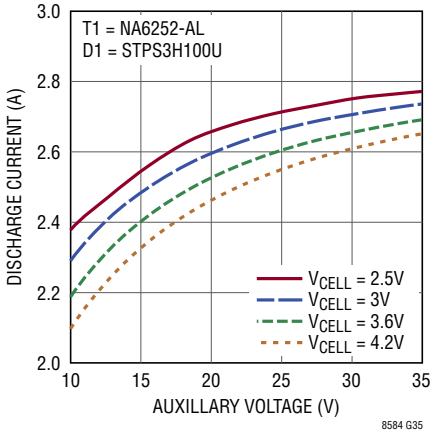


Switching Waveform

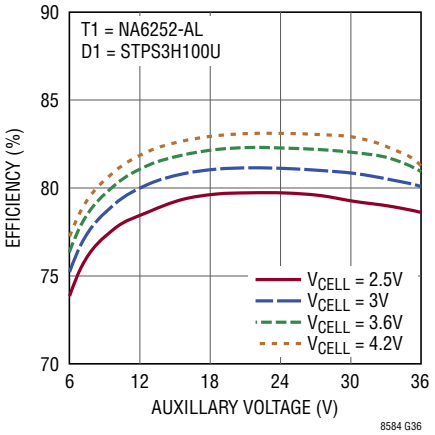


T1 = NA6252-AL
D1 = STPS3H100U
V_{CELL} = 4.2V
V_{AUX} = 13.8V
RCD SNUBBER = 4.99kΩ, 22nF

Average Discharge Current



Conversion Efficiency



PIN FUNCTIONS

GND (Pin1, Pin 2, Pin 3, Pin 4, Pin 17): Must be soldered directly to local ground plane.

MODE (Pin 5): Serial Enable Pin. Connect this pin to ground to enable serial interface for analog mux control. Connect this pin to V_{IN} to disable the analog mux. When the analog mux is disabled, the OUT pin defaults to V_{TEMP} measurement. Do not float this pin.

RTMR (Pin 6): Serial Interface Timer Pin. Place a resistor from this pin to ground to set the serial count duration window, t_W. See the Applications Information section for proper resistor selection.

D_{IN} (Pin 7): Data Input Pin. Take this pin to ground to initiate switching if MODE pin is connected to V_{IN}, or to select the desired analog mux state if MODE pin is tied to ground. This pin is designed to be directly driven from the LTC680x family's S pins.

OUT (Pin 8): Analog Output Pin. Connect this pin to an accurate voltage monitor to measure a voltage proportional to the internal IC temperature, V_{TEMP}, if MODE pin is connected to V_{IN}, or measure the output of the internal analog mux if MODE pin is connected to ground. In analog mux mode, the OUT pin allows voltage monitoring of the V_{CELL} pin, the V_{SNS} pin, or V_{TEMP}. This pin is designed to be directly connected to the LTC680x family's C pins. Must connect a compensation capacitor to this pin. See the Applications Information section for proper capacitor sizing and placement.

V_{IN} (Pin 9): Supply Pin. Connect this pin directly to the positive battery cell terminal. Must be bypassed with high grade (X5R or better) ceramic capacitor placed close to the transformer's primary winding connection.

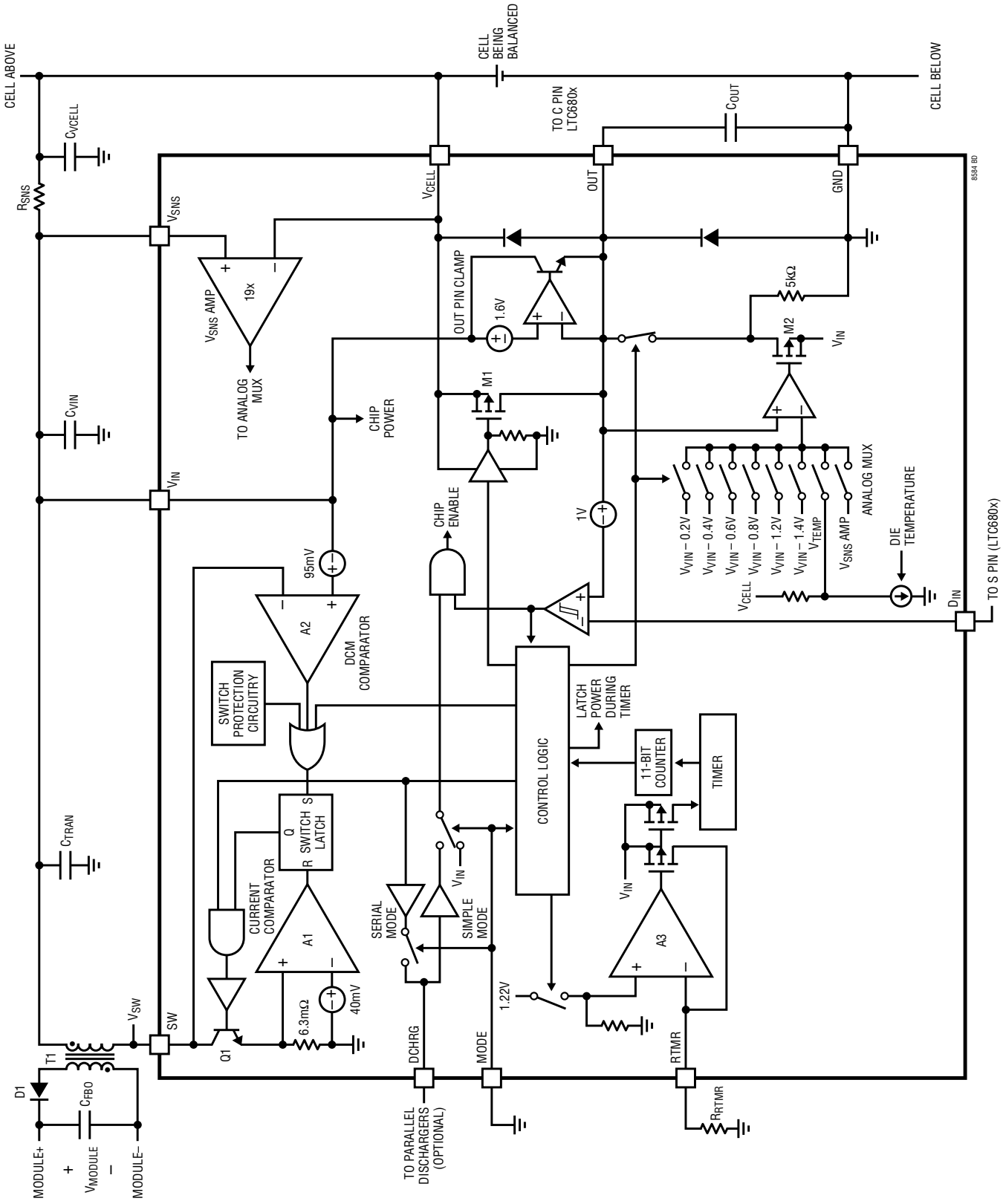
V_{CELL} (Pin 10): Cell Voltage Monitor Pin. This pin provides a Kelvin connection to the battery cell for accurate voltage monitoring. Connect this pin directly to the positive battery cell terminal. The recommended cell voltage is 2.5V to 5.3V.

V_{SNS} (Pin 11): Voltage Sense Pin. Connect this pin to the current sense resistor connected to the primary side of the transformer. Use this pin to measure average current discharged from battery cell (see the Block Diagram). MODE pin must be connected to ground and the internal analog mux must have the V_{SNS} pin selected to use this feature. Input current is determined as $(V_{VCELL} – V_{VSNS})/R_{SNS}$.

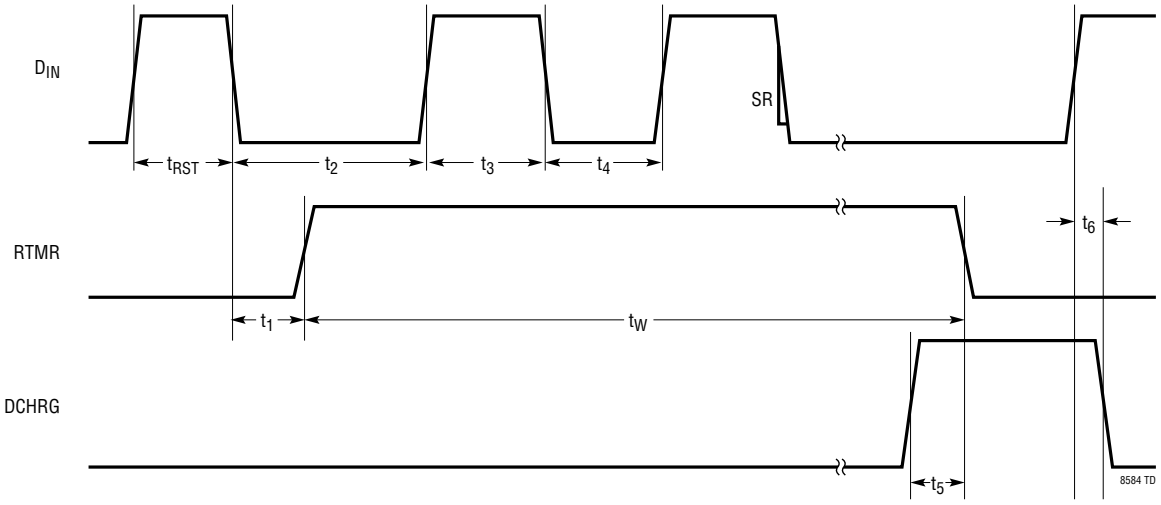
DCHRG (Pin 12): Discharge Pin. The Discharge pin can be configured as an input or output pin. Connect MODE pin to ground to configure DCHRG as an output pin where DCHRG is driven to V_{IN} during switching and driven to ground when switching is deactivated. The output configuration can be used to drive multiple LT8584's or other switching regulators in parallel, to boost discharge capability. Connect MODE pin high to configure DCHRG as an input. When configured as an input pin, drive DCHRG pin to V_{IN} to enable switching. Note in this mode that serial communication is disabled and the D_{IN} pin must be grounded to initiate switching.

SW (Pin 13, Pin 14, Pin 15, Pin 16): Switch Pin. This is the collector of the internal 6A NPN power switch. Minimize the metal trace area connected to this pin to minimize EMI. Connect the bottom side of the transformer primary to this pin.

BLOCK DIAGRAM



TIMING DIAGRAM



OPERATION

Many systems use multiple battery cells connected in series to increase the available capacity and voltage. In such systems, the individual battery cells must be constantly monitored to ensure that they operate within a controlled range. Otherwise, the battery's capacity and life span may be compromised. Linear Technology offers the LTC680x family series of multicell battery stack monitors (BSM) to accomplish this task.

The LTC680x monitors each individual cell in the stack and communicates this information through a proprietary serial bus to a central processing unit. As a cell begins to reach the upper charge limit, commands are issued to the LTC680x to turn on that cell's passive shunt, bypassing the charging current to that cell and allowing the current to continue to the rest of the cells. The passive shunt current and/or power capability constrains the maximum charging current for the battery stack. Using a passive shunt is also inefficient, and the shunted current produces considerable heat at higher charging currents.

The LT8584 solves the two limitations of passive shunting balancers by actively shunting the charging current and returning the energy back to the battery stack. Instead of the energy being lost as heat, it is reused to charge the rest of the batteries in the stack. The architecture of the LT8584 also solves the problem of reduced run time when one or more of the cells in the stack reaches the lower safety voltage threshold before the entire stack capacity is extracted. Only active balancing can redistribute the charge from the stronger cells (cells with higher voltage) to charge the weaker cells. This allows the weaker cells to continue to supply the load, extracting greater than 96% of entire stack capacity where passive balancing may only extract 80%.

The LT8584 has an integrated 6A switch designed to operate as a boundary mode flyback converter and provides 2.5A average discharge current. The average discharge current is also scalable by using multiple LT8584s to balance each cell. Note that each battery in the stack requires an LT8584 active cell balancer.

The LT8584 flyback topology allows the charge to return between any two points in the battery stack. Most applications use a module approach and return the charge to a local set of 12 series-connected cells monitored by a 12 channel BSM IC, where the output of the flyback converter is designated as V_{MODULE}. The entire battery stack is then constructed using several 12-cell modules connected in series. A second approach is to return the charge to the entire battery stack, where the flyback output is designated as V_{STACK}. A final option is to return the charge to an auxiliary power rail, designated as V_{AUX}.

The LT8584 has two modes of operation—selectable by the MODE pin—that can be integrated with the LTC680x or other battery stack system. In simple mode, the LT8584

OPERATION

discharger is toggled on/off using a logic input pin. In serial mode, the LT8584 allows the user to measure the discharge current and the die temperature, in addition to the cell voltage.

GENERAL FLYBACK OPERATION

The first cycle will commence approximately 2µs after LT8584 has been commanded to discharge a cell. The LT8584 is configured as a flyback converter operating in boundary mode (the edge of continuous operation), and has three basic states (see Figure 1).

1. Primary-Side Charging

When the switch latch is set, the internal NPN switch turns on, forcing ($V_{VIN} – V_{CESAT}$) across the primary winding. Consequently, current in the primary coil rises linearly at a rate of ($V_{VIN} – V_{CESAT}$)/L_{PRI}. The input voltage is mirrored on the secondary winding as –N • ($V_{VIN} – V_{CESAT}$) which reverse-biases the secondary-side series diode and prevents current flow in the secondary winding. Thus, energy is stored in the core of the transformer.

2. Secondary-Side Energy Transfer

When current limit is reached, the current limit comparator resets the switch latch and the device enters the second phase of operation, secondary-side energy transfer. The energy stored in the transformer core forward-biases the series diode and current flows into the output capacitor and/or battery. During this time, the output voltage plus the diode drop is reflected back to the primary coil.

3. Discontinuous Mode Detection

During secondary-side energy transfer to the output capacitor, ($V_{MODULE} + V_{DIODE}$)/N will appear across the primary winding. A transformer with no energy cannot support a DC voltage, so the voltage across the primary winding will decay to zero. In other words, the collector of the internal NPN, SW pins, will ring down from V_{VIN} + ($V_{MODULE} + V_{DIODE}$)/N to V_{VIN}. When the SW pin voltage falls below V_{VIN} + 95mV, the DCM comparator sets the switch latch and a new switch cycle begins. States 1-3 continue until the part is disabled.

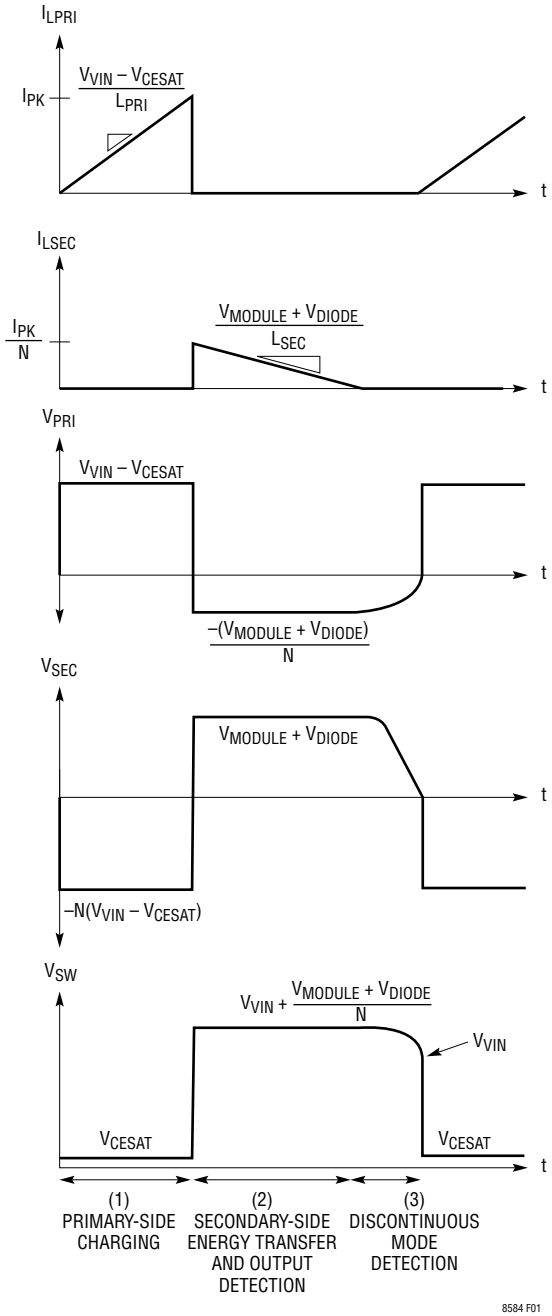


Figure 1. Simplified Discharging Waveforms

OPERATION

SWITCH PROTECTION

Several protection features are included to reduce the likelihood of permanent damage to the internal power NPN switch: the short-circuit detector, the high-impedance detector, the switch overvoltage protection (OVP), and internal undervoltage lockout (UVLO). These also alert the user when the integrity of the discharge converter has been compromised because of a fault. Switching is disabled during fault conditions.

Short-Circuit Detector

The short-circuit detector detects when the power NPN switch turns off prematurely due to a short in the primary-side winding. If the current comparator trips before the 850ns short detection timeout, the switch error latch will trip. The OUT pin is driven to $V_{VIN} - 1.2V$, $V_{SW,ERR}$, during a switch error. The part must be reset to clear the switch error fault.

High-Impedance Detector

The high-impedance detector monitors how long the power NPN switch has been on. If the switch remains on longer than 50µs, the switch maximum on-time, the switch error latch is set and the OUT pin is driven to $V_{VIN} - 1.2V$, $V_{SW,ERR}$. The part must be reset to clear the switch error fault.

Overvoltage Protection (OVP)

The OVP circuitry dynamically clamps the NPN collector's SW pins to 50V. This protects the internal power switch from entering breakdown and causing permanent damage. The clamp is also used as a primary-side snubber to absorb the leakage inductance energy. The 200ns switch clamp blanking time determines if the clamp is absorbing a leakage spike or if the switch is turning off while the secondary of the transformer is open. If the switch clamp is on longer than approximately 200ns, the switch error latch is set. The part must be reset to clear the switch error fault.

Internal Undervoltage Lockout (UVLO)

LT8584 protects itself during a UVLO condition by disabling switching. The OUT pin is driven to $V_{VIN} - 1.4V$, V_{FAULT}, during a UVLO condition. A UVLO fault is non-latching and dominates over a switch fault (Serial Mode requires V_{IN} to remain above 2V for a UVLO fault to be non-latching). Once the UVLO condition is cleared, the OUT pin reverts to normal operation and switching resumes. If the switch fault latch was tripped prior to the UVLO event, the OUT pin will indicate a switch fault, $V_{SW,ERR}$, only after the UVLO condition is cleared and switching would remain disabled.

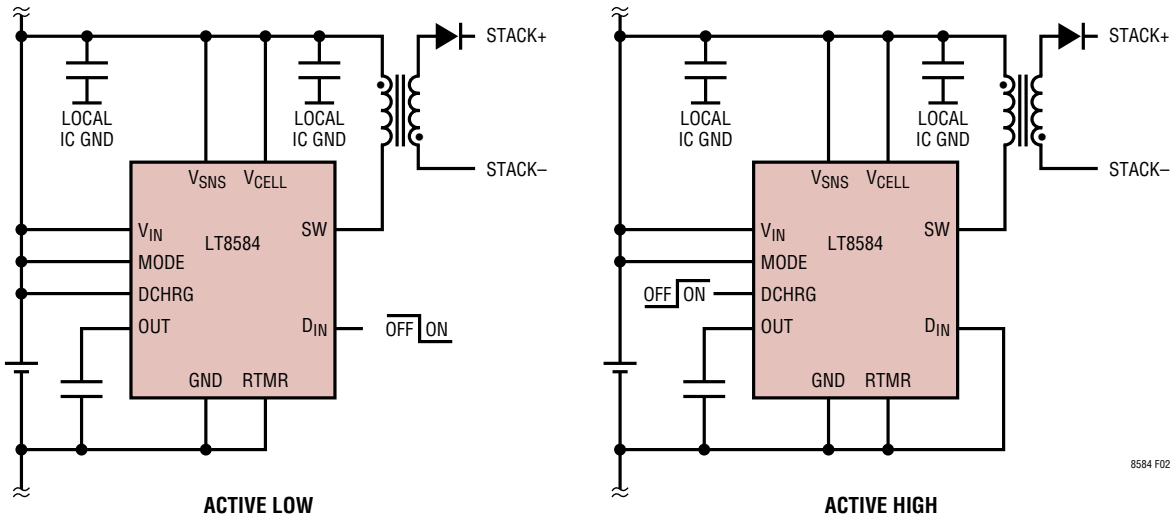


Figure 2. Simple Mode Configurations

OPERATION

SIMPLE MODE OPERATION

Connecting the MODE pin to the V_{IN} pin configures the LT8584 as a simple discharger with a simple on/off shutdown pin. Two shutdown options are provided to handle either an active high (DCHRG) or an active low input (D_{IN}), see Figure 2. Connect D_{IN} to ground and use DCHRG pin for an active high input, or connect DCHRG to V_{IN} and use D_{IN} as an active low input. The part will begin switching once the D_{IN} pin is low and DCHRG is high. Figure 3 shows the enable logic function. Never drive D_{IN} more than 0.4V below the local ground while operating in active-high simple mode.

Figure 3. Simple Mode Enable Logic

OUT Pin in Simple Mode

The OUT pin defaults to V_{TEMP}, a voltage proportional to the die temperature, and is measured with respect to the cell voltage such that $V_{TEMP} = V_{VCELL} – V_{OUT}$. This can be used to monitor the internal die temperature for system diagnostics. The OUT pin will also output two distinct indication voltage levels, $V_{VIN} – 1.4V$, V_{FAULT}, for an internal UVLO condition, or $V_{VIN} – 1.2V$, $V_{SW,ERR}$, for a switch error. V_{TEMP} is not allowed to exceed 1V (equivalent to 180°C)[1]. This makes both the fault and switch error voltages deterministic. The switch error latch is set when the power NPN switch has encountered a fault (see the Switch Protection section for more details).

[1] Not verified during production testing.

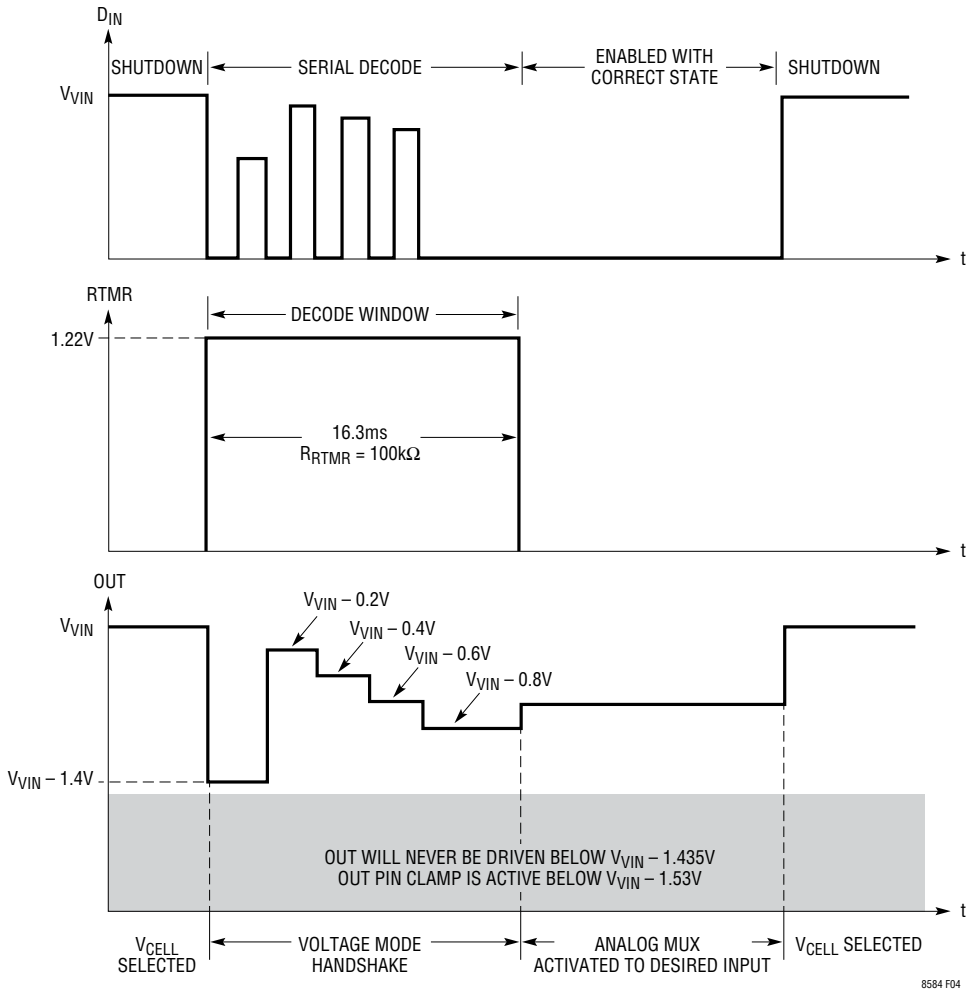


Figure 4. Serial Communication Decode

OPERATION

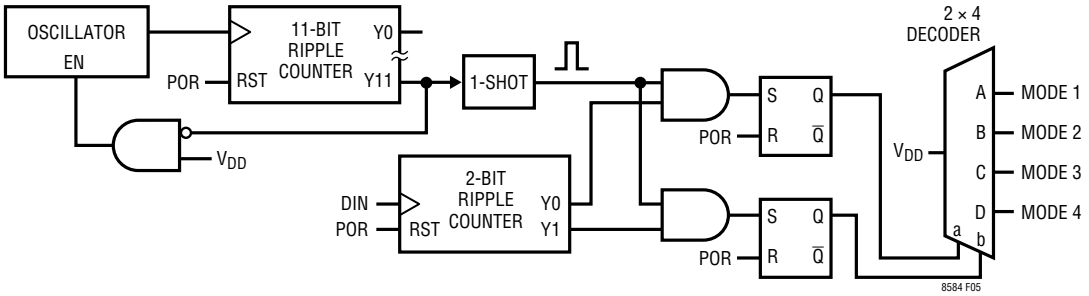


Figure 5. Serial Communication Architecture

SERIAL MODE OPERATION

Use serial mode if monitoring the discharging current and/or the die temperature are required. Connecting the MODE pin to GND enables serial communication. The D_{IN} pin is used to input serial data through a custom serial bus (see Figures 4 and 5).

Serial Mode Safety Features

The LT8584 provides the user with several levels of safety and verification. The LT8584 has built in switch protection that detects and halts power delivery during either a primary-side open or short, a secondary-side open or short, or an overvoltage on the primary or secondary. The LT8584 outputs the $V_{SW,ERR}$ handshake that can be read back by the battery stack monitor (BSM).

The LT8584 also detects communication errors including too many or too few D_{IN} pulses or a UVLO condition. The LT8584 outputs the V_{FAULT} handshake that can be read back by the BSM.

The LT8584 also provides critical cell parameters including temperature, discharge current, cell voltage, and cell and connection DC resistance. These are all read back by the BSM. As the cell starts to age, the cell impedance increases. This allows the user to perform preventative maintenance, keeping the system down time to a minimum.

Finally, the LT8584 handshake voltages are ±3% accurate independent references that can be used to verify that every channel in the BSM is measuring accurately.

Serial Architecture

Power to the part is latched on the first negative edge of D_{IN} signal and remains latched for the duration of the decode window, t_W. This allows the D_{IN} pin to be toggled for communicating serial data without resetting the part.

The LT8584 counts the number of negative edges seen on the D_{IN} pin. Note that the first edge, which initiates serial communication and latches the part, is not counted. There are four active modes the user can select as shown in Table 1. Handshaking is accomplished by reading the analog voltage on the OUT pin. Handshaking voltages are asserted on the negative edge of the D_{IN} signal, corresponding to the serial decode count.

Once the decode window expires and RTMR pin returns to ground, three actions are initiated: the OUT pin analog multiplexer switches to the desired measurement, the discharger turns on depending on selected mode in Table 1, and the input power latch disables. Note that the LT8584 can only be disabled after the decode window has expired and the D_{IN} pin has been taken high.

Table 1.Serial Mode States

PULSE COUNT	MODE	DISCHARGER STATE	MUX OUTPUT	HANDSHAKE VOLTAGE ($V_{VIN} - V_{OUT}$)
Part Disabled	0	Disabled	V_{CELL}	N/A
0	Fault	Disabled	V_{FAULT}	1.4
1	1	Enabled	V_{CELL}	0.2
2	2	Enabled	V_{SNS}	0.4
3	3	Enabled	V_{TEMP}	0.6
4	4	Disabled	V_{TEMP}	0.8
≥5	Fault	Disabled	V_{FAULT}	1.4

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Serial Timer Decode Window

The timer initiates on the first negative edge on the D_{IN} pin. RTMR pin remains high for the duration of the timer which signifies the decode window for the serial input counter. A resistor from the RTMR pin to ground sets the decode window duration. The duration can be accurately set from 1.9ms (R_{RTMR} = 10k) to 31ms (R_{RTMR} = 200k). The timer can be set outside this range, but the accuracy decreases. The serial input counter stops counting and latches the data once the RTMR pin goes low; after which, the OUT pin amplifier input MUX selects the desired measurement, and the discharger is set to the right state.

Serial Communication Fault Modes

The serial interface has several fault monitors that prevent entering undesired modes due to a communication error. The OUT pin is set to V_{VIN} – 1.4V to indicate the LT8584 is in fault. The part remains in fault from the onset of RTMR going high until the first count is detected. If no count is seen by the serial input counter during the decode window, the fault is latched. If the serial input counter counts higher than 4 negative edges, the fault latch is set.

A third latching fault occurs if an internal undervoltage lockout (UVLO) is detected during the decode window. This protects against undesired operation if data latches or the serial input counter were reset. The part must be reset by taking D_{IN} high to clear a fault.

D_{IN} Pin and Serial Bus Timing

Several internal passive filters are added to the data bus to prevent injected system noise corrupting serial communication. These filters have time constants that place constraints on the serial communication timing requirements (see the Timing Diagram). The LT8584 can reject up to 4µs of erroneous glitches on the D_{IN} pin in either direction. The power latch filter can also reject up to a 4µs glitch on D_{IN}.

The D_{IN} pin has built-in hysteresis of approximately 100mV. This allows the serial input counter to recognize both slow and fast edges without erroneous behavior. The discharger activation or deactivation time is typically less than 3µs and is a direct indication of the switch enable latch state.

OUT Pin Analog MUX

An internal multiplexer, MUX, selects between V_{CELL} and the OUT pin amplifier based on one of the selected Serial Modes shown in Table 1. The OUT pin amplifier has a 5kΩ internal load and has several inputs including: V_{TEMP}, the 19•V_{SNS} amplifier, and six handshake voltages. The internal MUX defaults to V_{CELL} in shutdown—consuming no power in the process—and provides a 55Ω nominal resistance from the V_{CELL} pin to the OUT pin. Figure 6 shows the connection of the OUT pin to a BSM and its internal analog MUX.

The MUX switches over to one of the handshake voltage levels once both the LT8584 and the decode window are activated. The OUT amplifier will indicate a fault at start-up until the serial input counter recognizes the first negative edge on D_{IN}. Subsequent negative edges on D_{IN} cause the MUX to select the handshake voltage corresponding to the number of edges counted. These voltage levels provide a means of verifying if the serial interface has recognized the correct count. Note that the OUT pin amplifier has an approximate 200µs one percent settling time when driving a 220nF load capacitance.

Once the RTMR pin goes low, the MUX selects the OUT pin mode corresponding to the number of serial input counts (see Table 1 for available modes). The part can also be placed in shutdown when RTMR is low and the decode window has expired.

V_{CELL} Measurement

The user can measure the cell voltage by measuring the voltage on the OUT pin either with the part disabled (discharger off) or with the part enabled in MODE 1 (discharger on), see Table 1. The LT8584 uses an internal PMOS switch with R_{DSON} = 55Ω to connect V_{CELL} to the OUT pin. Note that any current flowing into or out of the OUT pin will cause a measurement error due to the IR drop across the switch.

V_{SNS} 19× Amplifier

An amplifier is provided to allow the user to monitor the discharger current. This measurement can only be performed when the discharger is on (MODE 2). The differential voltage between V_{VCELL} and V_{VSNS} is amplified 19×.

OPERATION

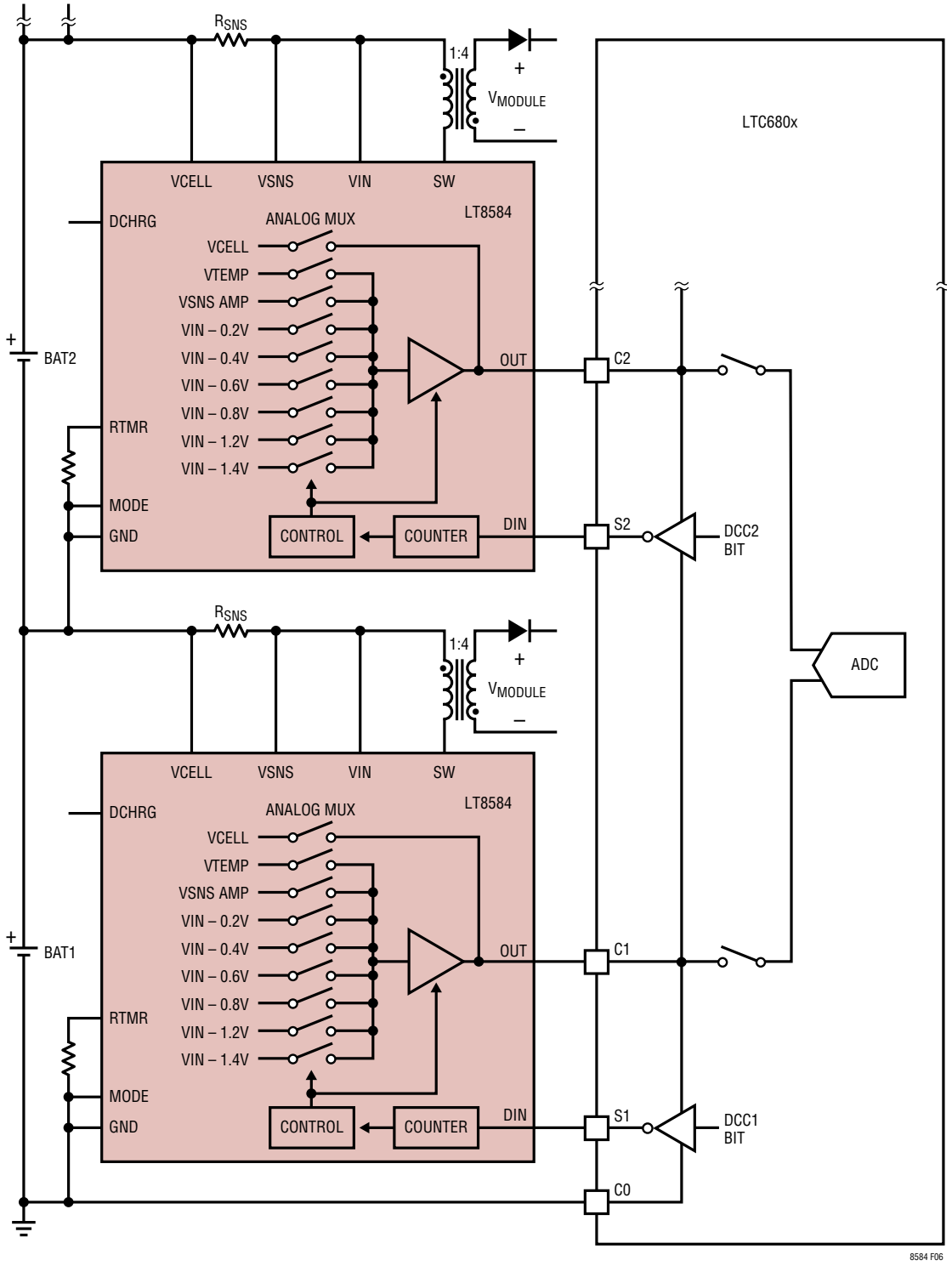


Figure 6. Serial Mode Analog MUX Connection

OPERATION

This reduces errors due to input offset in the measurement circuitry connected to the OUT pin. It also allows the use of low-value resistors, and thus, yields greater overall efficiency.

For accuracy, the V_{IN} pin should be tied to the V_{SNS} pin to include both the LT8584 bias current and the internal NPN base drive current. Tying the V_{IN} pin to the V_{SNS} pin changes the overall gain to 20x. Tying the V_{IN} pin to the V_{CELL} measures transformer current only and the overall gain remains 19x.

The V_{SNS} amplifier has a –30mV to 70mV dynamic input range. Internal filtering and circuit architecture allows accurate measurements even when the input current contains negative components. The V_{SNS} amplifier requires that the average input current remain positive. $V_{VIN} – V_{OUT}$ is not allowed to exceed 1V during V_{SNS} measurement to guarantee that both V_{FAULT} and $V_{SW,ERR}$ are deterministic. This sets the maximum average input range, $V_{VCELL} – V_{VSNS}$, to 50mV.

Die Temperature Output

The user can also monitor the die temperature by selecting either MODE 3 (discharger enabled) or MODE 4 (discharger disabled). The voltage $V_{VCELL} – V_{OUT}$, V_{TEMP}, is proportional to the absolute temperature in degrees Kelvin. Thus, the user needs to take two measurements to calculate the die temperature. Temperature data gives the user a second means to verify if the discharger is on as well as to monitor environmental conditions. V_{TEMP} is not allowed to exceed 1V (equivalent to 180°C)[1] to make both V_{FAULT} and $V_{SW,ERR}$ deterministic.

The following equation is used to determine the internal die temperature in degrees Celsius:

$$T_J(°C) = \frac{V_{TEMP} – 0.609}{0.00197}$$

where $V_{TEMP} = V_{VCELL} – V_{OUT}$ and expressed in volts. Although the absolute die temperature can deviate from the above equation by ±25°C, the relationship between V_{TEMP} and the change in die temperature is well defined. The offset error can be calibrated out using an accurate system temperature monitor like that in the LTC680x family of parts. There is also a small V_{VCELL} dependence on V_{TEMP} which can be corrected using the following expression:

$$T_{J,CORR}\ (°C) = T_{J,CAL} + (4.2V – V_{CELL}) \bullet 2°C$$

where $T_{J,CORR}$ is the corrected die temperature and $T_{J,CAL}$ is die temperature calculated from the previous equation.

Serial Mode Differential Measurements

All parameters including handshake voltages, V_{SNS}, and V_{TEMP} are extracted differentially by taking two sequential measurements and doing a subtraction. Figure 7 shows the method for extracting a given parameter, V_{PAR}, from the highlighted LT8584. The LT8584 directly below the LT8584 under measurement must be forced to select V_{CELL} (MODE 0) and becomes the negative reference for both sequential measurements.

Table 2. MODE Selection During Differential Measurements

	SERIAL MODE STATE	
DESIRED PARAMETER	**1ST MEASUREMENT**	**2ND MEASUREMENT**
Handshake Voltage	MODE 0	During Decode Window
V_{SNS}	MODE 1	MODE 2
V_{TEMP}, Balancer Enabled	MODE 1	MODE 3
V_{TEMP}, Balancer Disabled	MODE 0	MODE 4

Selecting V_{CELL} for the first measurement is performed by entering either MODE 0 (balancer disabled) or MODE 1 (balancer enabled). Use Table 2 to determine which V_{CELL} to reference for a given parameter. All measurements are taken after the decode window has expired, unless otherwise noted.

$$V_{PAR} = 1st\ Measurement – (2nd\ Measurement)$$
$$= V_{CELL} – (V_{CELL} – V_{PAR})$$

The LTC6803's channel above the channel under measurement will have a voltage higher than a standard cell, $V_{CELL} + V_{PAR}$, see Figure 7. The LT8584 was architected to protect the LTC6803's ADC inputs and to guarantee that they well never be stressed beyond their absolute maximum rating.

DCHRG Output

The DCHRG pin allows the LT8584 to operate several dischargers in parallel. The DCHRG pin goes high when the switch enable latch is set. The DCHRG pin can be used to directly drive the DCHRG pin of another LT8584 configured in simple mode (MODE pin connected to V_{IN}) or to directly drive the shutdown pin of another power converter. It has the ability to sink or source currents up to 300µA.

[1] Not verified during production testing.

OPERATION

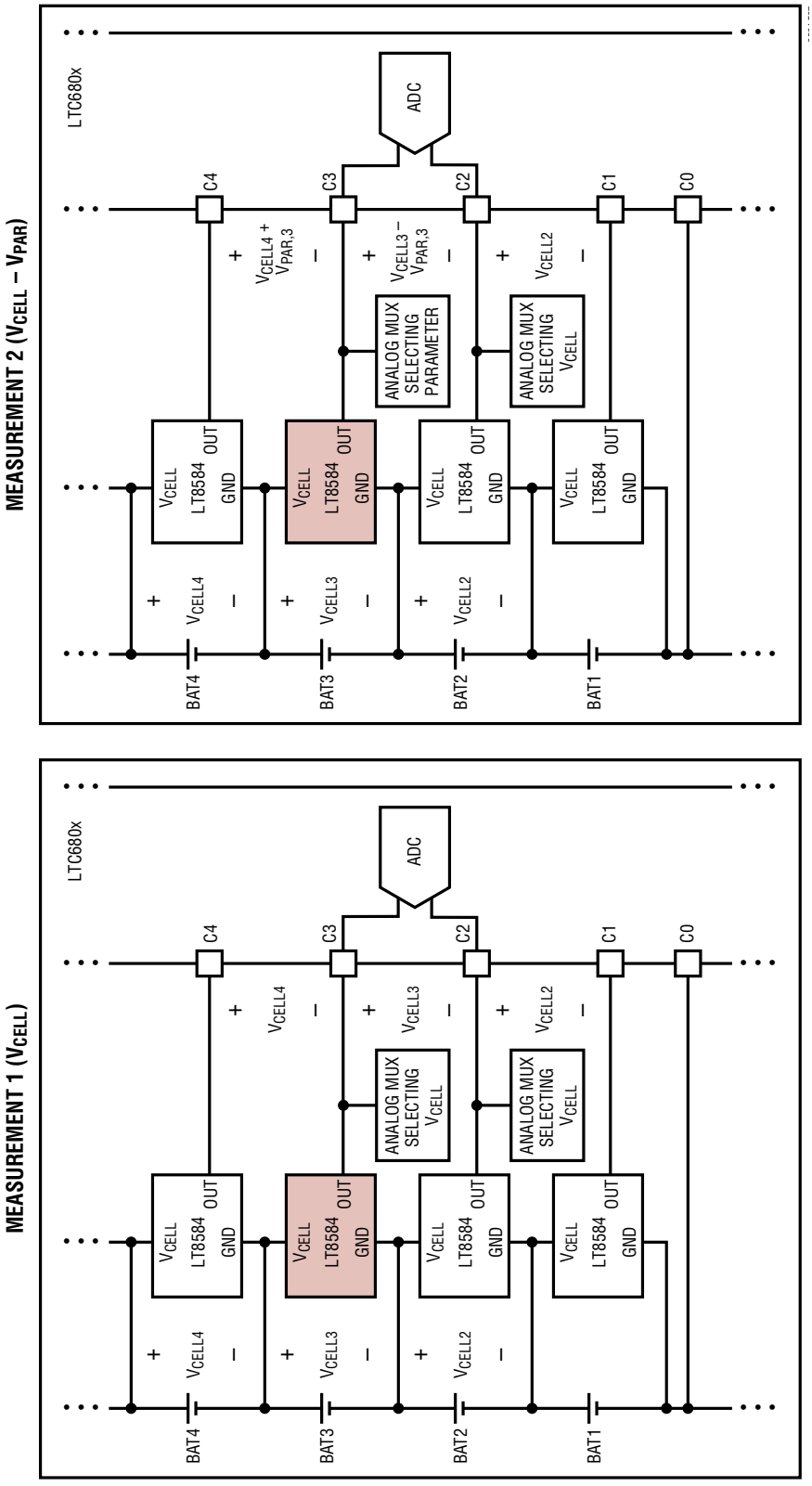


Figure 7. Serial Mode Differential Measurements

APPLICATIONS INFORMATION

The LT8584 can be used as a discharger for balancing the charge in battery or supercapacitor stack systems. The user can choose either simple mode or serial mode. The LT8584 can be driven from any battery stack monitor such as the LTC680x. Simple mode can be employed using either active high or active low logic, increasing its interface flexibility.

COMPONENT SELECTION

Few external components are required to achieve balancing. The only external components are the transformer, the output diode(s), the V_{IN} bypass capacitors, the R_{SNS} resistor (for measuring discharge current), the R_{RTMR} resistor (for serial mode), and in some cases, a RCD snubber.

The equations are shown for a module based approach described in the Operation section. V_{MODULE} becomes V_{STACK} in all equations for applications returning charge to the entire stack voltage, and V_{MODULE} becomes VAUX for all applications returning charge to an auxiliary power rail.

Transformer Design

The transformer design should yield overall converter efficiencies greater than 80%. This reduces heat dissipation and allows for a smaller converter PCB footprint. A proper transformer design balances core losses with winding losses. The LT8584 converter operates in DCM where the flux swing in the transformer is the greatest. This shifts most of the heat loss from winding loss to core loss. Reduce transformer core flux swing by lowering the air-gap permeability. A lower permeability requires more turns to achieve a desired primary inductance; thus, a balance can be achieved between core and winding losses. Recommended transformers are given in Table 3 that have been optimized for efficiency and size. Use the following guidelines when designing new transformers.

Reduce the transformer size by designing the boundary-mode operating frequency between 100kHz and 150kHz. The peak primary current is fixed at 6A by the chip. The transformer turns ratio, N, should be selected by optimizing the converter input RMS current, i.e. battery discharge current. The RMS input current can be estimated as:

$$I_{RMS,IN} = I_{PK} \bullet \sqrt{\frac{f_{BM} \bullet t_{ON}}{3}}$$

Note that negative switch current reduces the RMS input current by effectively reducing the boundary-mode frequency, f_{BM}, (see Figure 8). Reduce the overall reflected capacitance on the SW node by reducing the output diode and transformer interwinding parasitic capacitances.

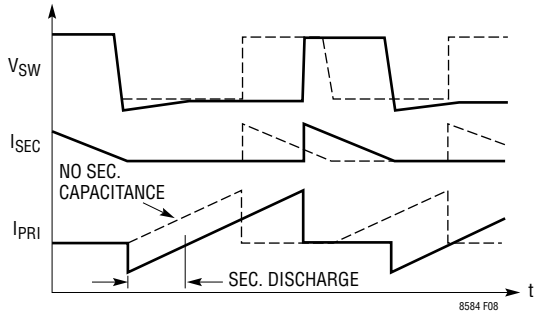


Figure 8. Effect of Secondary Winding Capacitance

Table 3. Recommended Transformers

MANUFACTURER	PART NUMBER	RECOMMENDED OUTPUT RANGE (V)	RCD SNUBBER REQUIRED	SIZE W × L × H (mm)	L_{PRI} (µH)	TURNS RATIO (PRI:SEC)
Coilcraft www.coilcraft.com	NA6252-AL NA5743-AL NA5920-AL*	10 to 35 30 to 80 100 to 400	Yes Yes No	15.24 × 12.7 × 11.43 15.24 × 12.7 × 11.43 15.24 × 12.7 × 11.43	4 4 4	11:15 1:4 1:24
Cooper Bussmann www.cooperindustries.com	CTX02-19175-R CTX02-19174-R CTX02-19176-R*	10 to 35 30 to 80 100 to 400	Yes Yes No	15 × 13 × 12 15 × 13 × 12 15 × 13 × 12	4 4 4	3:4 1:4 1:24
Würth www.we-online.com	750314019_R01 750314018_R02 750314020_R01*	10 to 35 30 to 80 100 to 400	Yes Yes No	15.24 × 13.34 × 11.43 15.24 × 13.34 × 11.43 15.24 × 13.34 × 11.43	4 4 4	3:4 1:4 1:24

* Switch error latch may trip when starting at voltages lower than the recommended output range.

APPLICATIONS INFORMATION

The RMS input current can be increased by increasing the ratio between the effective switch on-time, t_{ON}, and off-time, t_{OFF}. This off-time ratio is set by the transformer ratio, N. The following equation sets the switch off-time to approximately 1/3 of the switch on-time to optimize power transfer and efficiency.

$$N = \frac{\text{Secondary Turns}}{\text{Primary Turns}} = \frac{V_{MODULE}}{3 \bullet V_{IN}}$$

The off-time ratio should not be decreased much beyond 1/5; otherwise, secondary-side energy transfer time becomes too short, and the converter efficiency is reduced. Some applications may require a lower RMS current due to charging limitations or thermal dissipation limitations. Both can be reduced by increasing the turns ratio, N. Use the following equation to size the transformer's primary inductance:

$$L_{PRI} = \frac{1}{I_{PK} \bullet f_{BM} \bullet \left(\frac{1}{V_{IN}} + \frac{N}{V_{MODULE}} \right)}$$

Keep the primary inductance in the range of 2.2µH to 10µH. The lower limit guarantees proper detection of an open circuit in the transformer's secondary. The upper limit guarantees the high-impedance detector does not activate a false switch error during normal operation.

Leakage Inductance

Leakage inductance causes added voltage stress on the internal power NPN collector. The LT8584 uses an internal Zener clamp to absorb this leakage spike energy and clamp the switch node voltage to 50V. The leakage spike energy should be limited to improve efficiency. Figure 9 shows the waveform of the internal NPN switch.

Design the transformer to have minimum leakage inductance. Keep both transformer windings tightly wound around the core air gap. Using a bifilar winding or a sandwiched secondary decreases leakage inductance. Note that increased interwinding capacitance is a trade-off with lower leakage inductance. Several iterations may be required to optimize the transformer design.

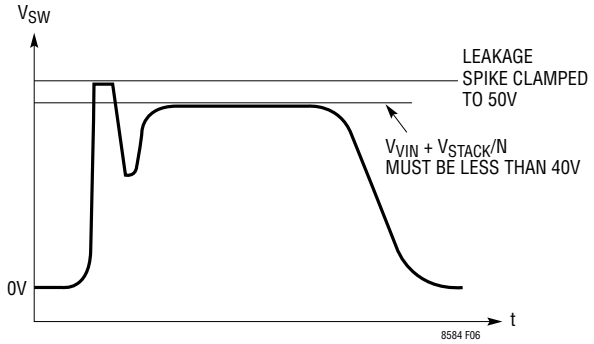


Figure 9. Internal Switch Voltage Waveform

Higher transformer turns ratios benefit from higher reflected capacitance that helps snub the leakage spike. N ratios less than 8 usually require an RCD snubber to help clamp this primary-side leakage spike and increase the converter efficiency. Good values for the resistor and capacitor are 4.99kΩ and 22nF, respectively.

Output Diode

The output diode(s) are selected based on the maximum repetitive reverse voltage (V_{RRM}) and the average forward current, $I_{F(AVG)}$. The output diode's V_{RRM} should at a minimum exceed $V_{MODULE} + N \bullet V_{VIN}$. The LT8584's internal OVP circuitry triggers at 50V, and V_{RRM} should therefore exceed $N \bullet (50 + V_{VIN})$ to prevent damage to the output diode during an OVP event. Note that the leakage spike will usually cause the OVP to trigger roughly 10% lower than the nominal reflected voltage on the primary. The output diode's $I_{F(AVG)}$ should exceed $I_{PK}/2N$, the average short-circuit current. The average diode current is also a function of the output voltage.

$$I_{F(AVG)} = \frac{I_{PK} \bullet V_{VIN}}{2 \bullet \left(V_{MODULE} + N \bullet V_{VIN} \right)}$$

The highest average diode current occurs at low output voltages and decreases as the output voltage increases. Reverse recovery time, reverse bias leakage, and junction capacitance should also be considered. All affect the overall charging efficiency. Excessive diode reverse recovery times can cause appreciable discharging of the output stack, thereby decreasing charge recovery. Choose a diode with a reverse recovery time of less than 75ns.

APPLICATIONS INFORMATION

Diode leakage current under high reverse bias bleeds the output battery/capacitor stack of charge. Choose a diode that has minimal reverse bias leakage current. Diode junction capacitance is reflected back to the primary, and energy is lost during negative NPN collection conduction. Choose a diode with minimal junction capacitance. Table 4 recommends several output diodes for various output voltages that have adequate reverse recovery times.

Flyback Output Capacitor

Every balancer flyback output must have a ceramic capacitor on its output. The output capacitor serves as a local, low impedance return path. It also aids during a connection failure, adding charge storage to allow the OVP circuit to detect an open. The capacitor should be sized to allow roughly 10 switch cycles when charging the output from ground to the nominal output voltage, $V_{OUTPUT,NOM}$. Use the following equation to size the output capacitor:

$$C_{FBO} \geq \frac{400 \bullet L_{PRIMARY}}{V^2_{OUTPUT,NOM}}$$

The voltage surge rating must exceed 50•N. The voltage surge rating is usually specified as a multiple of the maximum operating voltage. For capacitor maximum operating voltages less than 100V, the surge rating is 2.5x. For operating voltage between 100V and 630V, the surge rating is typically 1.5x; and for voltages higher than 1000V, the surge rating is 1.2x.

Bypass Capacitors

The LT8584 should be bypassed using 3 capacitors, C_{VIN}, C_{VCELL}, and C_{TRAN} (see Block Diagram), using a high-grade (X5R or better) ceramic capacitors. C_{VIN} should be placed close to the V_{IN} pin and should be sized between 1µF and 4.7µF. C_{TRAN} must be placed close to the transformer's primary winding connection and the IC local ground. The capacitance should range between 47µF and 100µF. Simple mode should have V_{SNS}, V_{CELL}, and D_{CHRG} shorted to V_{IN}, which provides an excellent landing for both the transformer primary and a single bypass cap (see the Recommended Layout section). C_{VIN} may be omitted in Simple Mode provided that the C_{TRAN} capacitor is in close proximity to the V_{IN} pin. C_{VCELL} is used for bulk capacitance and should be place close to the battery input connection. Ceramic capacitors are a good choice for bypassing due to their moderate density, low internal series impedance, and very low leakage current. Note that capacitor leakage current at a given operating voltage goes down with increasing capacitor voltage rating. Ceramic capacitors offer the lowest leakage current, while most electrolytic capacitors are quite leaky.

Table 4. Recommended Output Diodes

MANUFACTURER	RECOMMENDED TRANSFORMER TURNS RATIO (N) RANGE	PART NUMBER	$I_{F(AVG)}$ (A)	V_{RRM} (V)	t_{rr} (ns)	JUNCTION CAPACITANCE (pF)	PACKAGE
STMicroelectronics	1 to 2	STPS3H100U	3	100	N/A	90	SMB
		STPS2H100AY*	2	100	N/A	50	SMA
	2 to 4	STTH102AY*	1	200	20	12	SMA
	10 to 24	STTH112A	1	1200	75		SMA
Fairchild Semiconductor www.fairchildsemi.com	1 to 2	ES2B	2	100	20	18	SMB
	2 to 4	ES1D	1	200	15	7	SMA
	4 to 8	ES1G	1	400	35	10	SMA
	6 to 12	ES1J	1	600	35	8	SMA
Vishay www.vishay.com	1 to 2	SS2H10*	2	100	N/A	70	SMB
		U2B	2	100	20	16	SMB
	2 to 4	ES1D	1	200	15	10	SMA
		ES07D-M*	1.2	200	25	5	SMF
	10 to 20	US1M	1	1000	50	10	SMA

*AEC-Q101 Qualified

APPLICATIONS INFORMATION

Discharge Current Sense Resistor

The discharge current sense resistor, R_{SNS}, should only be used in serial mode. Omit this resistor and short V_{SNS} and V_{CELL} to V_{IN} in simple mode. The maximum sense voltage between V_{VSNS} and V_{VCELL} is 50mV. It is recommended to design for a nominal sense voltage of 30mV. It is not recommended to design for a nominal sense voltage below 20mV since the input offset voltage of the differential amplifier contributes more error at the lower range.

$$R_{SNS} = \frac{V_{VCELL} - V_{VSNS}}{I_{DIS,AV}} = \frac{30mV}{2.5A} = 12m\Omega$$

The internal amplifier amplifies the voltage difference between V_{VSNS} and V_{VCELL} 20× when V_{IN} is tied to V_{SNS}. The voltage is referenced from V_{CELL} such that:

$$V_{VCELL} - V_{OUT} = 20 \bullet (R_{SNS} \bullet I_{DIS,AV})$$

The measurement is the average discharge current, $I_{DIS,AV}$, and not the RMS value. The output, $V_{VIN} - V_{OUT}$, is clamped to a maximum of 1V.

Decode Window Resistor, R_{RTMR}

RTMR pin is used to set the duration of the decode window and is programmed by selecting the value of the resistor connected between RTMR and GND. This pin is used in serial mode only. Ground this pin when using simple mode. The decode window is programmable from 1.9ms to 31ms. Set the decode window duration 30% longer than the required time to set the LT8584 in MODE 4 and read back the handshake voltage. This allows the system to detect if there is a communication error. Set R_{RTMR} based on following equation:

$$R_{RTMR}\ (k\Omega) = 0.015 \bullet t^2_W + 5.9 \bullet t_W - 1.1$$

where R_{RTMR} is given in kΩ and t_W is given in ms.

The RTMR pin is driven to 1.22V approximately 2µs after the part is first enabled. This indicates the decode window is active. The RTMR pin is taken low after the decode window expires. The internal decoder states are latched on the falling edge of RTMR (see Figure 4). The OUT pin multiplexer then selects the correct input corresponding to the programmed mode (refer to Table 1).

OUT Pin Compensation and Filtering

The OUT pin must have external compensation, C_{OUT}, for all applications including both serial mode and simple mode. The external capacitor also provides necessary filtering for the input to the BSM. The OUT amplifier is internally compensated to handle capacitance ranging from 20nF to 220nF. Use 47nF for most applications to yield approximately 100µs 1% settling time. A faster amplifier response can be achieved by adding a zero using a resistor in series with the external filter capacitor. Use 4.7nF capacitor with a 60Ω series resistor to achieve a sub-100µs settling time. Note that in serial mode, the capacitors are placed between adjacent LT8584 OUT pins. This effectively doubles the compensation capacitance from the capacitor value used. The OUT amplifier also has internal filtering to both improve PSRR and handle large-signal steps or spikes that may be present on the supply lines.

Additional filtering may be required in noisy environments. Figure 10 shows a two-pole filter with the LT8584 operating in serial mode. The resistors must be kept small to minimize error due to non-zero input currents into the BSM. The LTC6804 is guaranteed to have 2µA or less input bias current during measurement. There are two resistors in any given measurement path. Thus, a 50Ω series resistor will introduce up to a 200µV error. D_{IN} pin current will also cause an error when enabling a particular LT8584, but the error term is canceled when making differential measurements.

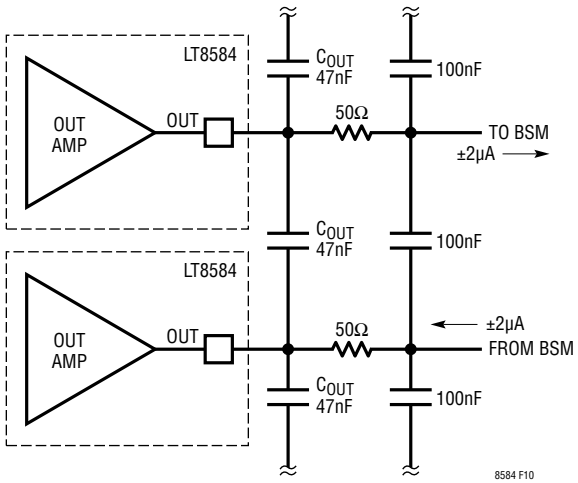


Figure 10. Optional OUT Pin Filtering

APPLICATIONS INFORMATION

HOT SWAP™ PROTECTION

Large currents are developed when hot swapping a battery with a LT8584 application due to the large input bulk capacitance coupled with the low ESR of the batteries. In most cases, the LT8584 should have no problem handling the overshoot voltage that follows the large inrush current. The downstream BSM, however, might encounter damage that requires additional steps and/or circuitry to protect against hot swapping. Several solutions use a two-path method incorporating a pre-charge resistive path and a shunt path (see Figure 11).

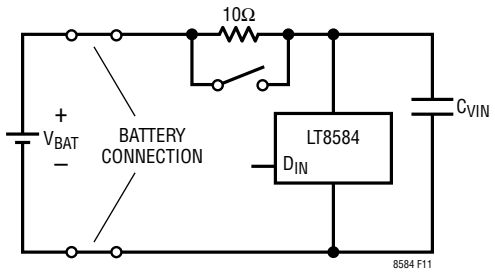


Figure 11. Dual Path Hot Swap Solution

For most applications, use the recommended Hot Swap Solution shown as Active Solution 1 in Figure 12 and in the Typical Application Section. Several other mechanical, active, and order-of-assembly solutions are also given as alternatives or as supplements.

Active Solution

An active solution has the added advantage of automatic hot swap protection; no additional steps are needed when connecting batteries. Two input protection solutions are shown with the first solution using only TVS diodes. D1 is selected to trigger around 6V and to take the brunt of the connection input pulse. The reverse leakage current is more significant in low-voltage TVS's. Table 5 gives several diodes for D1 that have adequate current and voltage characteristics while minimizing reverse leakage current. D2 provides secondary protection for the BSM inputs. These should be smaller than D1 since the LT8584's OUT pin limits current. Table 6 gives several diodes that are optimal for D2.

The second active solution has additional overvoltage protection via a fuse, F1, and a pre-charge MOSFET circuit. This method has the disadvantage of lower efficiency and higher cost. Use FETs for M1 in Figure 12 that have low $R_{DS,ON}$ to maximize converter efficiency and have less than a 1.25V V_{GS} threshold. Table 7 lists several recommended FETs for M1. C1 should be sized such that C1 ≥ C_{VIN}/500.

The third active solution protects the flyback output capacitors. All flyback outputs sum together and flow through D13. During a Hot Swap condition, D13 will reverse bias and prevent a large inrush current into the flyback output capacitors. The peak repetitive reverse voltage, V_{RRM}, should exceed the maximum module voltage, V_{MODULE}. Several recommended diodes for D13 are given in Table 8.

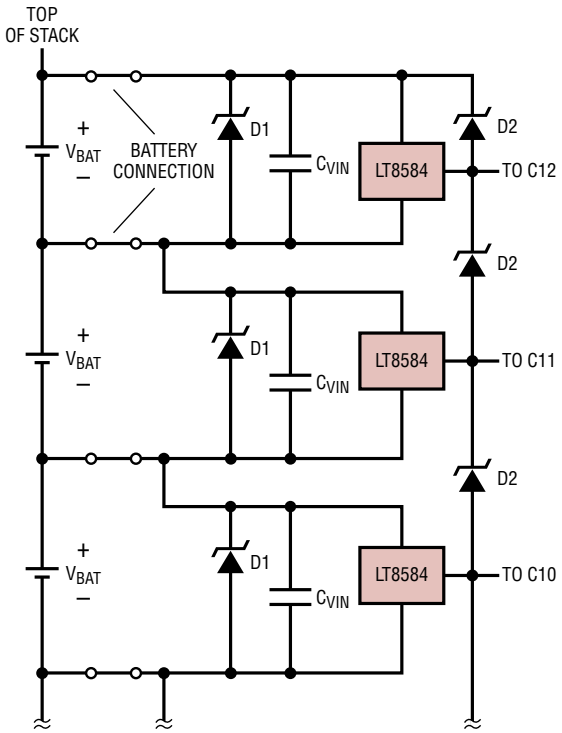
Mechanical Solution

A mechanical approach may result in a more cost effective solution. A 10Ω resistor is used to pre-charge the C_{VIN} capacitor to the battery voltage, limiting the inrush current. After the C_{VIN} cap is charged, a mechanical short is connected across the resistor and remains there during all normal operations. There are three recommended solutions for the mechanical short: 1.) use a > 3A rated jumper 2.) use a mechanical switch or 3.) use a staggered-pin battery connector. The staggered pin connection has the long pins connecting to LT8584 through the 10Ω resistor. The short pins connect directly to the LT8584, shorting out the 10Ω resistor. Normal insertion has a delay on the order of milliseconds between the long pin connecting and short pin connecting to the circuit, allowing C_{VIN} to charge up through a current limiting resistor before the mechanical short is made.

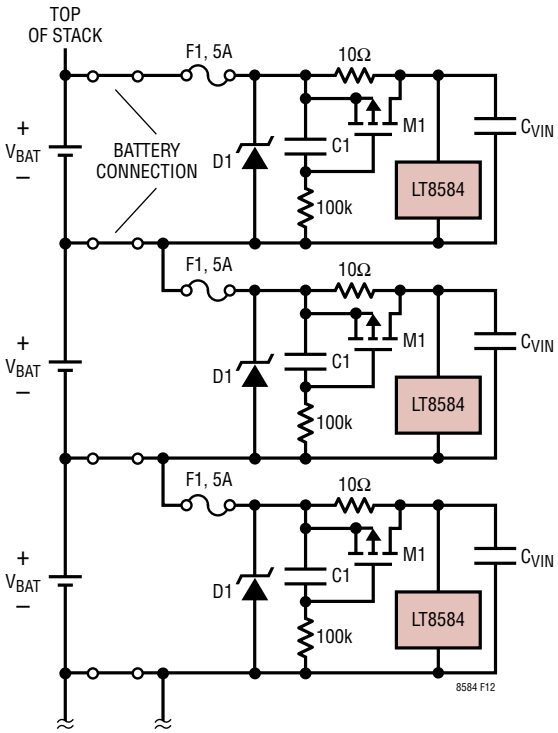
Order of Assembly

The order of assembly of the battery stack, the LT8584 balancers, and the BSM can also mitigate hot swapping issues. Having separate boards for both the LT8584 balancers and the BSM is recommended. This allows the LT8584 balancers to be built and connected during the battery stack assembly. The last step involves mating the battery stack and LT8584 assembly with the BSM board. Additional filters on the inputs into the BSM also reduce possible issues during final assembly, see the OUT Pin Compensation and Filtering section for more detail.

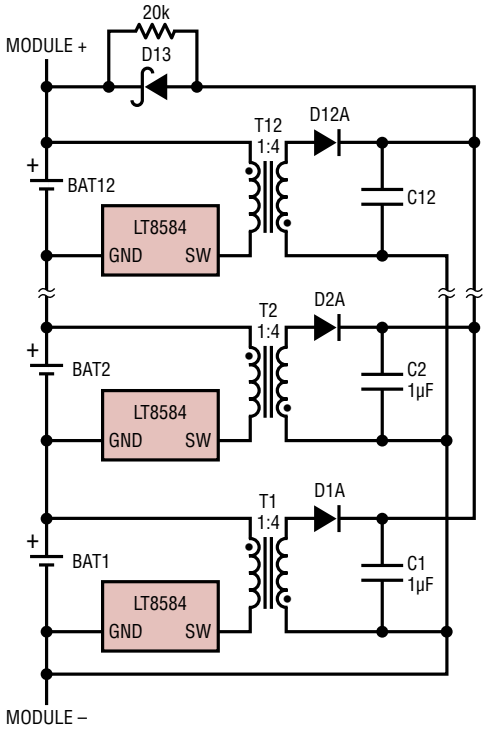
APPLICATIONS INFORMATION



ACTIVE SOLUTION 1



ACTIVE SOLUTION 2



FLYBACK OUTPUT HOT SWAP PROTECTION

Figure 12. Active Hot Swap Solutions

APPLICATIONS INFORMATION

Table 5. Recommended Transient Voltage Suppressors (TVS) for D1 in Figure 12

MANUFACTURER	PART NUMBER	REVERSE LEAKAGE (μA)	V_{P-P} AT I_{P-P}	PACKAGE
STMicroelectronics	SM2T6V8A	50 at 5V	9.2V at 19.6A	DO-216AA
	SM4T6V7AY*	20 at 5V	9.2V at 43.5A	SMA
	SMA6T6V7AY*	20 at 5V	9.1V at 68A	SMA
Vishay	VESD05A1-02V	1 at 5V	12V at 16A	SOD-523
	GSOT05*	10 at 5V	12 at 30A	SOT-23
NXP	PESD5V0S1UA	4 at 5V	13.5V at 25A	SOD-323
Infineon	ESD5V0S1U-03W	20 at 5V	14V at 40A	SOD323

*AEC-Q101 Qualified

Table 6. Recommended Transient Voltage Suppressors (TVS) for D2 in Figure 12

MANUFACTURER	PART NUMBER	REVERSE LEAKAGE (μA)	V_{P-P} AT I_{P-P}	PACKAGE
STMicroelectronics	ESDALC6V1-1M2	0.1 at 3V	9.2V at 6A	SOD882
Vishay	VBUS051BD-HD1	0.1 at 5V	16V at 3A	LLP1006-2L
	VESD05-02V	0.1 at 5V	20V at 6A	SOD-523
Diode Inc	T5V0S5-7	0.05 at 5V	15V at 5A	SOD-523
NXP	PESD9X5.0L*	0.2 at 5V	10V at 1A	SOD-882

*AEC-Q101 Qualified

Table 7. Recommended FETs for M1 in Figure 12

MANUFACTURER	PART NUMBER	$R_{DS,ON}$ (mΩ) AT V_{GS} = 2.5V	$I_{DS,MAX}$ (A)	PACKAGE
Fairchild Semiconductor www.fairchildsemi.com	FDS4465	10.5	13.5	SO-8
	FDS6576	20	11	SO-8
	FDMA905P	21	10	MicroFET 2x2
	FDMA910PZ	24	9.4	MicroFET 2x2
Vishay www.vishay.com	Si7623DN	9	35	PowerPAK 1212-8
	Si7615ADN	9.8	35	PowerPAK 1212-8
	SiS407DN	13.8	25	PowerPAK 1212-8
	SiA447DJ	19.4	12	PowerPAK SC-70

Table 8. Recommended Diodes for D13 in Figure 12

MANUFACTURER	PART NUMBER	$I_{F(AVG)}$ (A)	V_{RRM} (V)	PACKAGE
Diodes, Inc. www.diodes.com	SBR8U60P5	8	60	POWERDI5
	PDS760-13	7	60	POWERDI5
Vishay www.vishay.com	V8P10-M3	8	100	TO-277A
	SS10P6	7	60	TO-277A

APPLICATIONS INFORMATION

OPERATING PARALLELED LT8584s

Multiple LT8584s may be used if more discharge current is required. The LT8584 connected to a battery stack monitor (LTC6804 is recommended) becomes the master balancer. Connect its MODE pin to ground. Limit the maximum number of parallel slave balancers to 20. This gives a maximum discharge current of 50A. Other converters may also be used as a slave, including the LT3751 (must connect its V_{IN} to the cell above) and the LT3750. Connect all slave MODE pins to V_{IN}. This forces those parts into simple mode and makes their DCHRG pin an input pin.

Connect all slave DCHRG pins (SHDN pins if using other converters) to the master DCHRG pin. Figure 13 shows a 5A discharger circuit using two LT8584s.

Each part operates asynchronously from the other one. Use separate transformers for each LT8584 balancer.

The slave balancers operate only when the master balancer is operating. A fault on the master balancer will turn off all slave balancers. A fault in any of the slave balancers will not turn off any of the other balancers. Use an external sense resistor, R_{SNS}, and the V_{SNS} pin to determine if the average current is at the expected value.

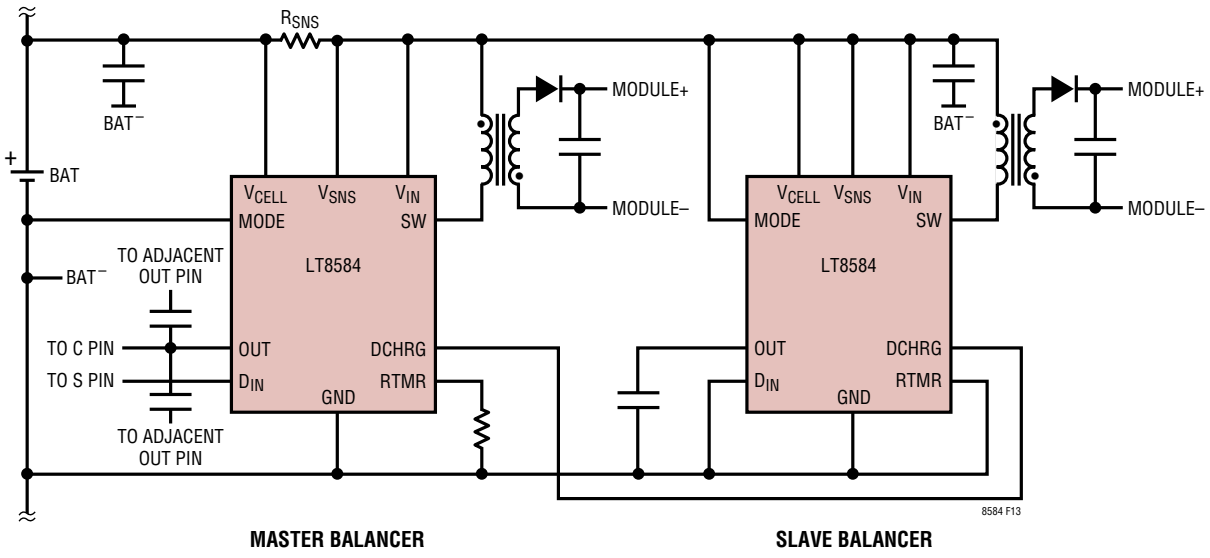


Figure 13. LT8584 Parallel Operation

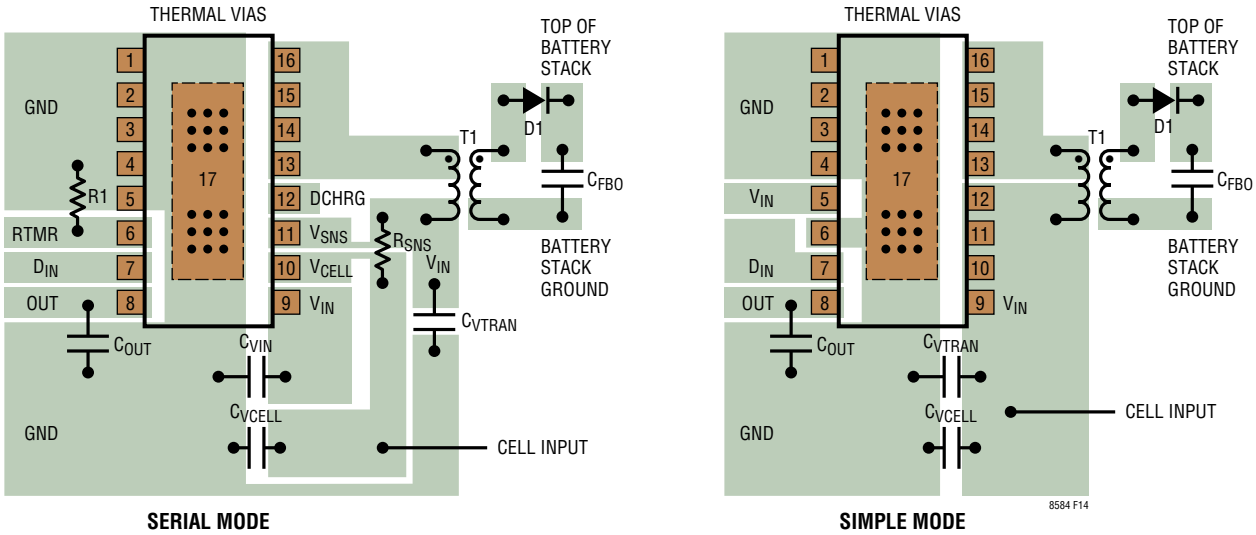


Figure 14. LT8584 Suggested Layout

APPLICATIONS INFORMATION

RECOMMENDED LAYOUT

The potentially high voltage operation of the LT8584 demands careful attention to the board layout, observing the following points:

1. Minimize the board trace area of the high voltage end of the secondary winding.
2. Keep the electrical path formed by C_{VTRAN}, the primary of T1, the SW node, and ground as short as possible. Increasing the length of this path effectively increases the leakage inductance of T1, resulting in excessive energy loss in the internal Zener clamp or RCD snubber.
3. Thermal vias should be added underneath the chip's exposed pad, pin 17, to enhance the LT8584's thermal performance. These vias should go directly to a local ground plane with a minimum area of 650mm^2.
4. Make Kelvin connections for V_{SNS}, V_{CELL}, and R_{SNS} to the battery cell when using the LT8584 in serial mode. The IR drop in the battery connection can be calibrated out using a software algorithm. Consult Application Engineering.
5. Care should be taken when routing V_{CELL}, V_{SNS} and V_{IN} connections. R_{TRACE} in Figure 15 should be minimized for better efficiency. R_{TRACE} should never exceed 19•R_{SNS}. This guarantees that the OUT pin amplifier headroom is sufficient enough for reporting the V_{SNS} amplifier output.
6. Minimize the total connection resistance from the battery terminals to the V_{CELL} and GND pins of the LT8584. It is recommended to keep the total resistance less than 60mΩ to improve converter efficiency. Excessive IR drops in the PCB traces or connector terminals could also cause the LT8584 to prematurely enter UVLO.

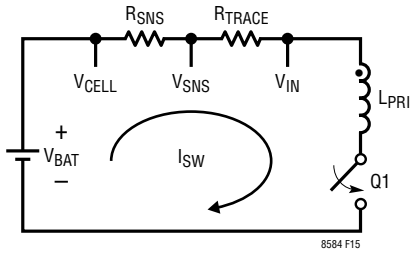


Figure 15. R_{TRACE} Minimization

CONNECTING TO A BATTERY STACK MONITOR

There are two methods used to connect the LT8584 balancer to a battery stack monitor (BSM): either a single-wire or two-wire. Both have advantages and disadvantages. Both methods may require Kelvin connections for the BSM supply rails depending upon the magnitude of IR drop across the connections to the battery stack. In most cases, keeping the individual connection resistances less than 60mΩ allows the BSM supply rails to share the return path through RW0 and RW12, see Figure 16.

The single-wire connection is recommended due to complete system visibility of the wire connection impedance. The single-wire is also cheaper and more reliable due to fewer wire connections. See the Typical Application section for proper Kelvin connection between adjacent LT8584 channels in single-wire mode.

Note that in the two-wire connection scheme, the ground connection impedance can not be determined when calculating wire impedance and will be invisible to the measurement system. On the flip side, the algorithms for computing two-wire connection impedance and back calculating V_{CELL} during discharging are more straightforward. The two-wire method also has the advantage of only losing visibility of a single cell during an open connection instead of two as in the single-wire method.

INTEGRATING WITH THE LTC680x FAMILY

The LTC680x family of parts are multi-cell battery stack monitors that are described in the Operation section of this data sheet. For more information, consult the LTC680x data sheets. Several operational flavors are available with their inherent differences shown in Table 9.

Table 9. LTC680x Feature Differences

PART	COMMUNICATION	COMPATIBLE MODES
LTC6802-1	Daisy Chained Serial	Simple Mode Only
LTC6802-2	Addressable Parallel	Simple Mode Only
LTC6804-1/LTC6803-1/ LTC6803-3	Daisy Chained Serial	Serial / Simple Mode
LTC6804-2/LTC6803-2/ LTC6803-4	Addressable Parallel	Serial / Simple Mode

APPLICATIONS INFORMATION

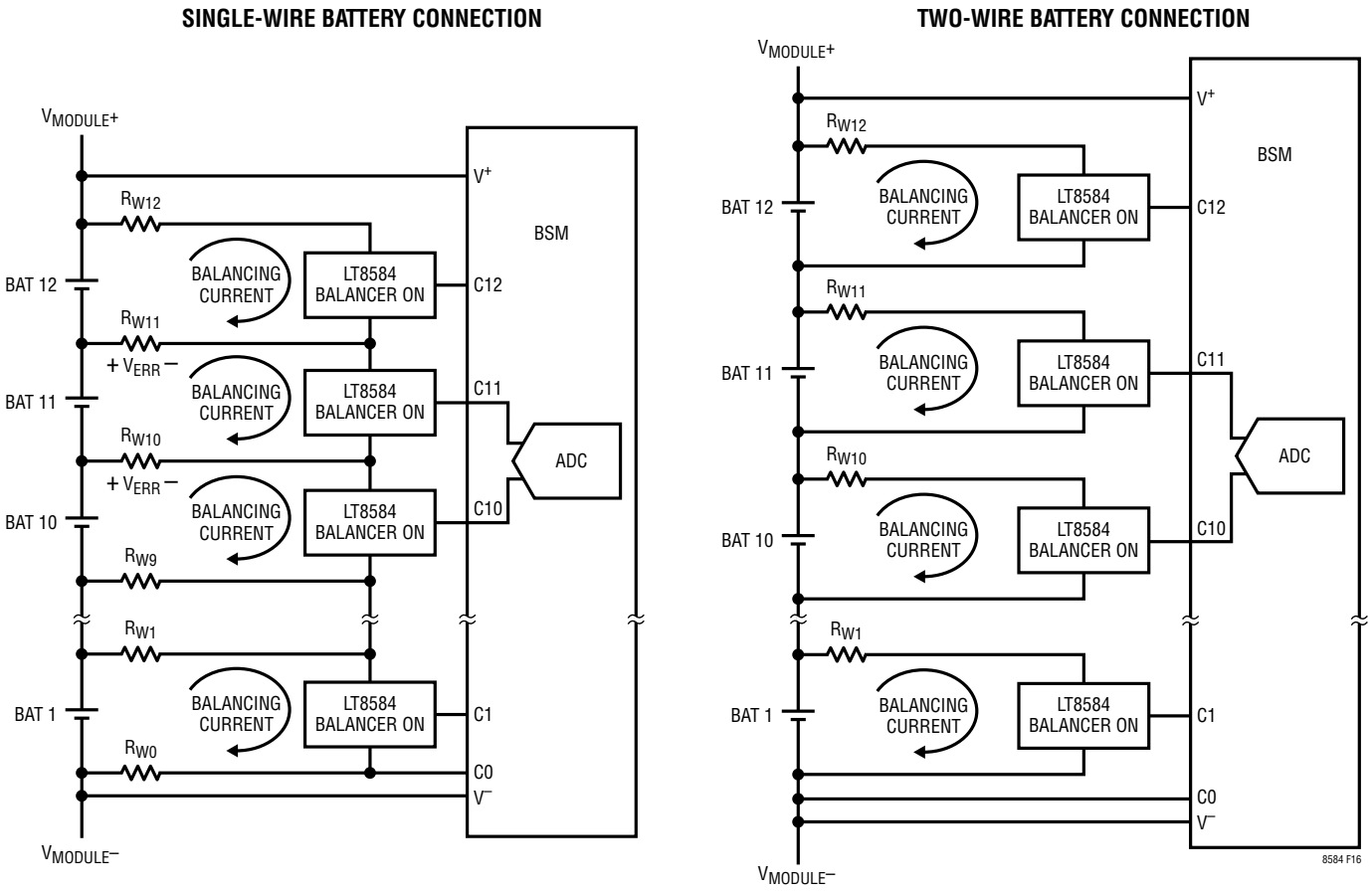


Figure 16. LT8584 Battery Connections

The LTC6803 and LTC6804 draw only 3µA of static current on the S pin, allowing the LT8584 to be enabled without noticeable measurement error. The LTC6804 offers improved ADC performance over the LTC6803 by reducing conversion time approximately 10x and reducing measurement error below 1.2mV. The LTC6804 also utilizes isoSPI with improved RF-immunity.

Enable Balancing in Simple Mode

Write a '1' to the corresponding DCCx bit in the configuration register of the LTC680x. This pulls its S pin low and activates the LT8584. Table 10 shows the required time to turn on one balancer where N = number of LTC680x in the system and f = frequency of the SCKI clock.

Table 10. Approximate Time to Enable One LT8584

STEP	TIME (s)	
	LTC6802-1/LTC6802-3 LTC6803-1/LTC6803-3	LTC6802-2/LTC6802-4 LTC6803-2/LTC6803-4
Send WRCFG Command, Write '1' to Enable Balancer	$\frac{(16+56 \cdot N)}{f}$	$\frac{72}{f}$

Note that the addressable serial interface is much faster when writing to a single channel in a multi-chip system.

APPLICATIONS INFORMATION

Enable Balancing in Serial Mode

In serial mode, the configuration register has to be written several times to toggle the DCCx bit and pipe data into the serial bus. The RTMR resistor needs to be set accordingly to guarantee that enough time is allocated to enter any one of the four serial modes and read back the handshake voltage on the OUT pin. There are speed limitations when sending information to the LT8584 (see the Timing Diagram). Use Table 11 to determine overall timing requirements.

Table 11. Turning on LT8584 in MODE 4

DCCx STATE	TIME (s)	
	LTC6803-1/ LTC6803-2	LTC6803-2/ LTC6803-4
1 – D_{IN} Low	$\frac{(16+56 \cdot N)}{f}$	$\frac{72}{f}$
0 – D_{IN} High		
1 – D_{IN} Low (MODE 1)		
0 – D_{IN} High		
1 – D_{IN} Low (MODE 2)		
0 – D_{IN} High		
1 – D_{IN} Low (MODE 3)		
0 – D_{IN} High		
1 – D_{IN} Low (MODE 4)		
Total	$\frac{(16+56 \cdot N) \cdot 9}{f}$	$\frac{648}{f}$

Filtering and ADC Measurements

The LTC680x has an internal multichannel differential ADC that measures the voltage between each consecutive pair of C pins. Figure 17 shows the ADC connected to C(N) and C(N+1), measuring the difference between the two adjacent LT8584's OUT pins. Most parameters require two measurements, one with the top LT8584 selecting V_{CELL} and another one with the top LT8584 selecting the desired parameter. The difference between these two measurements yields the desired parameter value. This is required since the LTC680x is not directly connected to the battery cells. See the Serial Mode Differential Measurements section for more detail.

Filter capacitors (typically 47nF) have to be placed between adjacent C pins to provide the required 16kHz lowpass filter for the ADC input path. This provides 30dB of noise reduction. No external filter resistors are needed since the

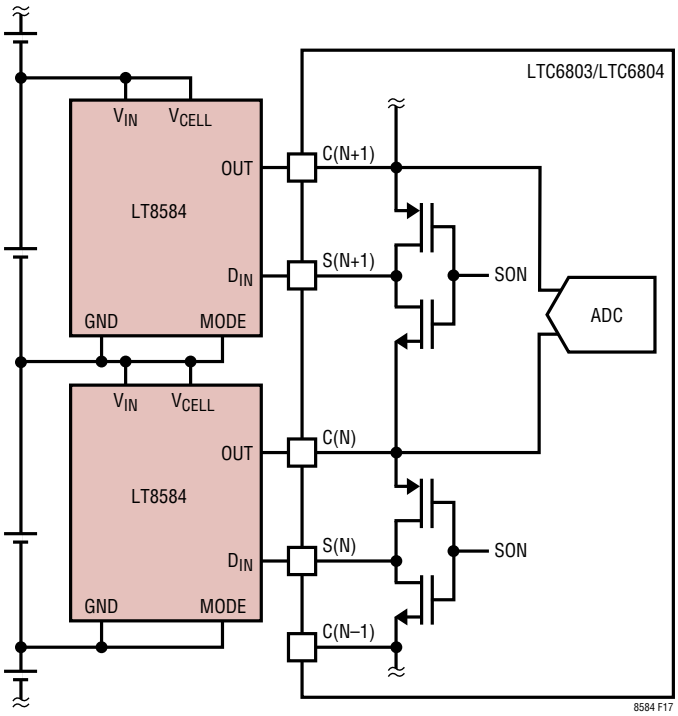


Figure 17. LTC6803/LTC6804 Simplified Connections

internal impedance from V_{CELL} to OUT is approximately 55Ω. Note that the effective capacitance on the OUT pin becomes 2× 47nF or 94nF. Figure 17 has omitted these capacitors for the sake of simplicity (see the Typical Applications for proper connection of the filter capacitors).

Adequate bypass capacitors need to be connected from V_{IN} to ground for each LT8584 to provide a low-impedance path for high-frequency switching noise. Ceramic capacitors work well for this purpose.

Several passive filters internal to the LT8584 are included to remove erroneous glitches on the D_{IN} pin that are up to 4µs in duration.

TEST CIRCUIT

Use the circuit in Figure 18 for testing the LT8584 in Serial Mode without using a BSM. The inverter directly driving the LT8584 should be placed close to the LT8584 and have less than 1V V_{GS} thresholds. Figure 19 shows typical serial communication waveforms using a 100kΩ timer resistor and a 2ms data period.

APPLICATIONS INFORMATION

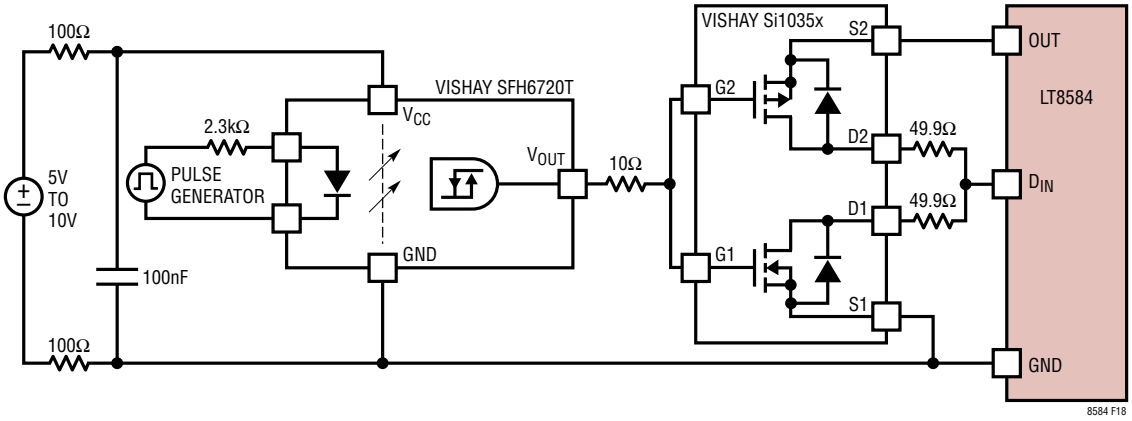


Figure 18. Serial Mode Test Circuit

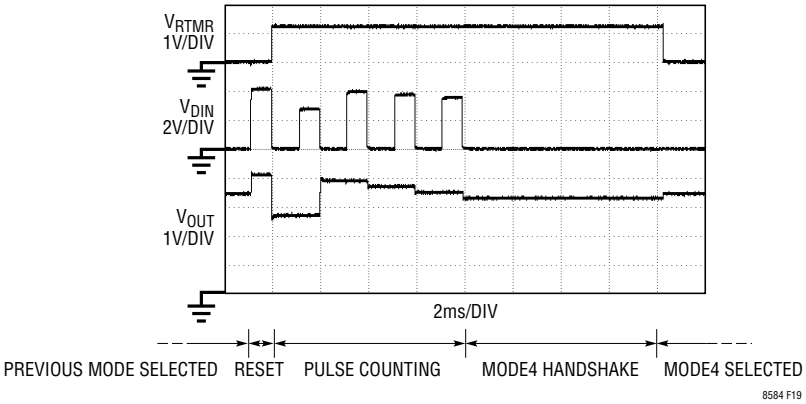
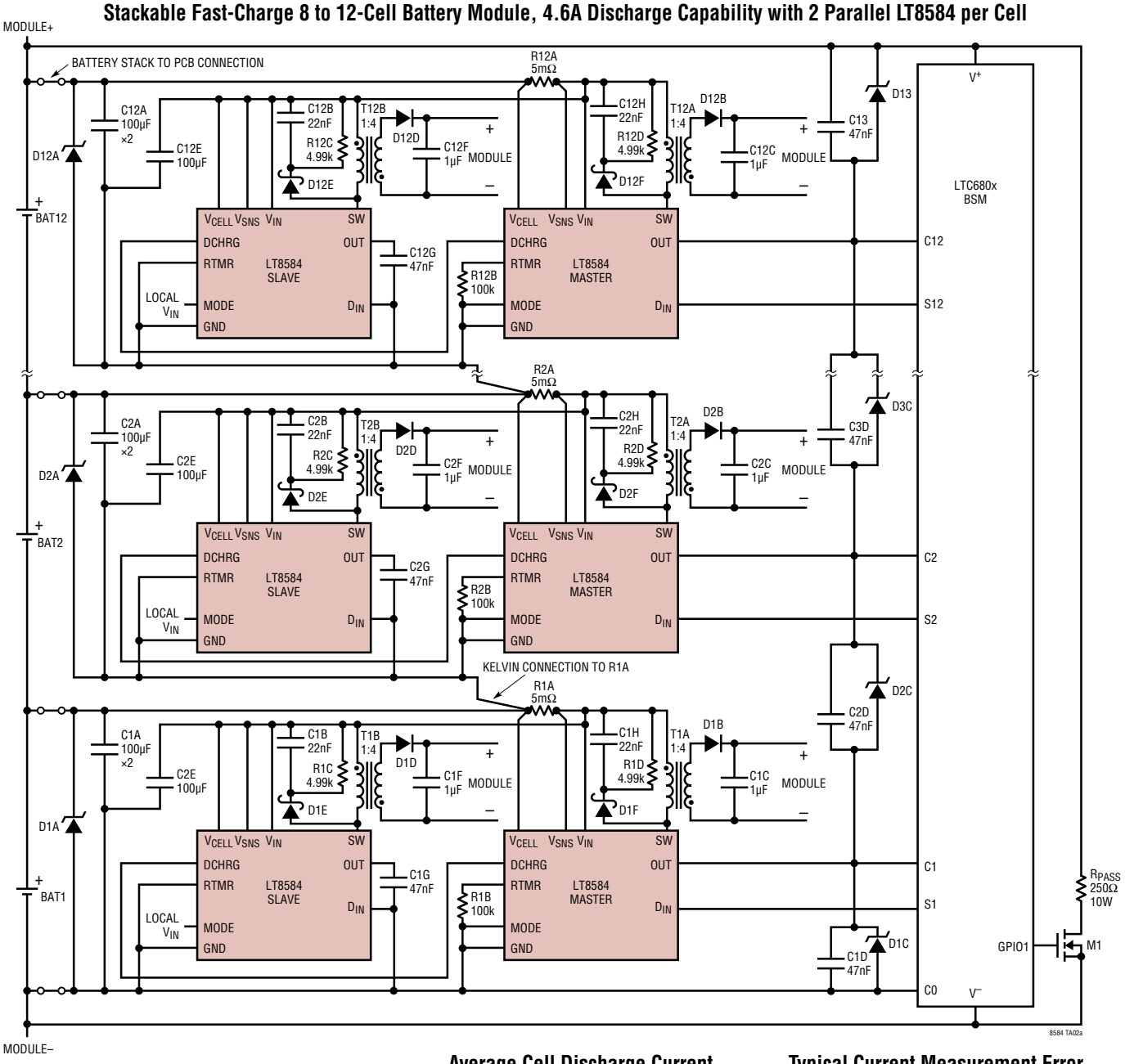


Figure 19. Typical Serial Mode Communication Waveforms

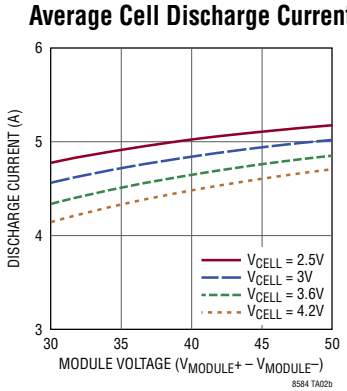
TYPICAL APPLICATIONS

Stackable Fast-Charge 8 to 12-Cell Battery Module, 4.6A Discharge Capability with 2 Parallel LT8584 per Cell

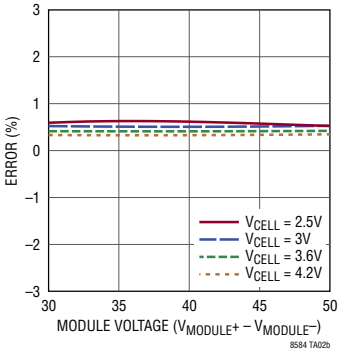


C1A-C12A: 6.3V X5R OR X7R CERAMIC CAPACITOR
C1B-C12B, C1H-C12H: 50V X5R OR X7R CERAMIC CAPACITOR
C1C-C12C: 100V X5R OR X7R CERAMIC CAPACITOR
C1D-C12D, C13: 50V NPO CERAMIC CAPACITOR
C1E-C12E: 6.3V X5R OR X7R CERAMIC CAPACITOR
C1F-C12F: 100V X5R OR X7R CERAMIC CAPACITOR
C1G-C12G: 6.3V X5R OR X7R CERAMIC CAPACITOR
D1A-D12A: STMICROELECTRONICS SMA6T6V7AY TVS DIODE
D1B-D12B: FAIRCHILD ES1D 200V, 1A ULTRAFAST RECTIFIER
D1C-D12C, D13: STMICROELECTRONICS ESDALC6V1-1M2 TVS
D1D-D12D: FAIRCHILD ES1D 200V, 1A ULTRAFAST RECTIFIER
D1E-D12E, D1F-D12F: FAIRCHILD SS16 60V, 1A
M1: FAIRCHILD FDMC86102L 100V, 5.5A
R1A-R12A: USE 1% 1206 RESISTORS
R1B-R12B, R1C-R12C, R1D-R12D: USE 1% 0603 RESISTORS
RPASS: 10W WIREWOUND
T1A-T12A, T1B-T12B: COILCRAFT NA5743-AL
U1: LINEAR TECHNOLOGY LTC680x FAMILY INCLUDING BUT NOT LIMITED TO LTC6802, LTC6803, LTC6804

Average Cell Discharge Current



Typical Current Measurement Error



TYPICAL APPLICATIONS

Stackable Fast-Charge 8 to 12-Cell Battery Module Application Notes

1. Channels 3 through 11 are omitted for clarity. These channels should be integrated similar to channel 2. Not all required components for the LTC680x are shown. Consult the LTC680x data sheet for recommended components and their connections.
2. Up to 20 LT8584 balancers may be connected in parallel to farther increase discharge current. The DCHRG pin can also drive an enable pin of a separate DC/DC converter like the LT3750 capacitor charger.
3. Multiple modules can be stacked in series to achieve a larger battery stack. Each module must contain an integer multiple of the total number of cells in the stack. For instance, an 80 cell stack should be constructed with 8 modules each having 10 cells. Use consecutive BSM channels starting with BSM channel 1when populating a module with less than 12 channels. Tie all unused LTC680x C pins to MODULE+.
4. Place one CnE capacitor close to the Master LT8584's transformer primary, and place the other CnE capacitor close to the Slave LT8584's transformer primary. The symbol 'n' denotes a particular channel ranging from 1 to 12.
5. Place RCD snubber composed of DnF, DnE, RnC, RnD, CnB, CnH, as close as possible to the respective transformer primary. The symbol 'n' denotes a particular channel ranging from 1 to 12.
6. R_{PASS} and M1 may be omitted for applications using only one module in the stack.
7. Each LT8584 channel should have no less than 650mm^2 of PCB pad footprint for proper heat sinking.
8. Consult Application Engineering for proper communication with LTC680x family of parts as well as a proper algorithm for extracting cell parameters.
9. Recommended for cells that operate within a 2.5V to 5.3V range.

Stackable 8 to 12-Cell Battery Module Application Notes

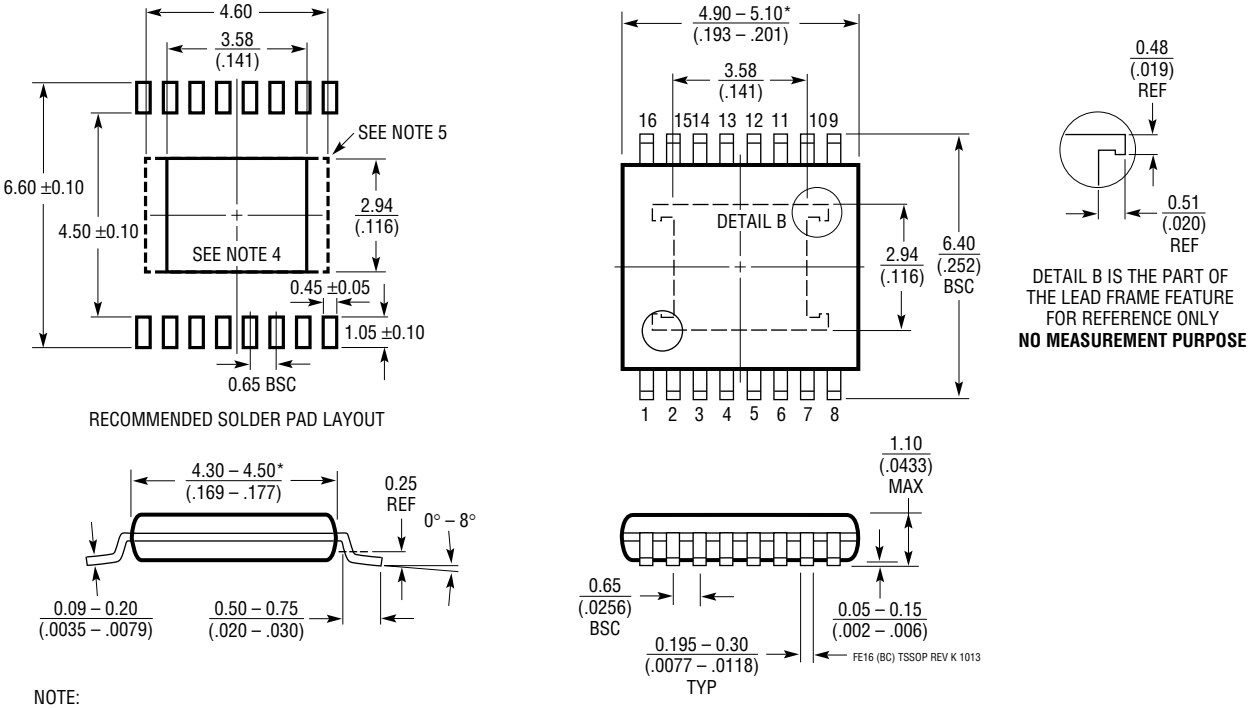
See the last page Typical Application.

1. Channels 4 through 11 are omitted for clarity. These channels should be integrated similar to channel 2. Not all required components for the LTC680x are shown. Consult the LTC680x data sheet for recommended components and their connections.
2. Multiple modules can be stacked in series to achieve a larger battery stack. Each module must contain an integer multiple of the total number of cells in the stack. For instance, an 80 cell stack should be constructed with 8 modules each having 10 cells. Use consecutive BSM channels starting with BSM channel 1 when populating a module with less than 12 channels. Tie all unused LTC680x C pins to MODULE+.
3. Place the CnB capacitor close to the LT8584's transformer primary. The RCD snubber composed of CnE, RnC and DnD should also be placed close the LT8584's transformer primary. The symbol 'n' denotes a particular channel ranging from 1 to 12.
4. The BSM V^+ pin may share cell 12's positive battery connection, and the BSM V^- pin may share cell 0's negative battery connection as long as the summation of each battery connection's PCB trace, wire, and interconnection resistance is less than 60mΩ.
5. R_{PASS} and M1 may be omitted for applications using only one module in the stack.
6. Each LT8584 channel should have no less than 650mm^2 of PCB pad footprint for proper heat sinking.
7. Consult Application Engineering for proper communication with LTC680x family of parts as well as a proper algorithm for extracting cell parameters.
8. Recommended for cells that operate within a 2.5V to 5.3V range.

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

FE Package
16-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1663 Rev K)
Exposed Pad Variation BC



NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{(\text{INCHES})}$
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT
5. BOTTOM EXPOSED PADDLE MAY HAVE METAL PROTRUSION IN THIS AREA. THIS REGION MUST BE FREE OF ANY EXPOSED TRACES OR VIAS ON PCB LAYOUT

*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	05/14	Clarified Features	1
		Clarified Electrical Characteristics	3
		Clarified Data Threshold graph	6
		Clarified OUT Pin Amplifier graph	7
		Clarified Operation description	11
		Clarified Operation description	15
		Clarified Applications Information	20, 24, 30
		Clarified Figures 17, 18	30, 31
B	8/14	Clarified Absolute Maximum Ratings	2
		Clarified Handshake Voltage Error Conditions	3
		Clarified D_{IN} Pin Function	9
		Clarified Block Diagram	10
		Clarified Figure 1	12
		Clarified Sense Resistor Formula	23
		Clarified Figure 16 in Applications Information	29