Active Rectifier Controller with Reverse Protection

FEATURES

- **AEC-Q100 Qualified for Automotive Applications**
- **Reverse Input Protection to –40V**
- **Improved Performance Compared to a Schottky Diode**
  - **Reduce Power Dissipation by >90%**
  - **Reduce Drop to 20mV**
- **Ultrafast Transient Response**
  - **Rectifies $6V_{P-P}$ Up to 50kHz**
  - **Rectifies $2V_{P-P}$ Up to 100kHz**
- **Wide Operating Voltage Range: 3V to 42V**
- **Low 20µA Quiescent Current in Operation**
- **Low 3.5µA Shutdown Current**
- Accurate 1.21V Enable Pin Threshold
- Small 10-Lead MSOP Package, 10-Lead 3mm × 2mm DFN Package and 3mm × 2mm Side-Wettable DFN Package

APPLICATIONS

- Automotive Battery Protection
- Industrial Supplies
- Portable Instrumentation

DESCRIPTION

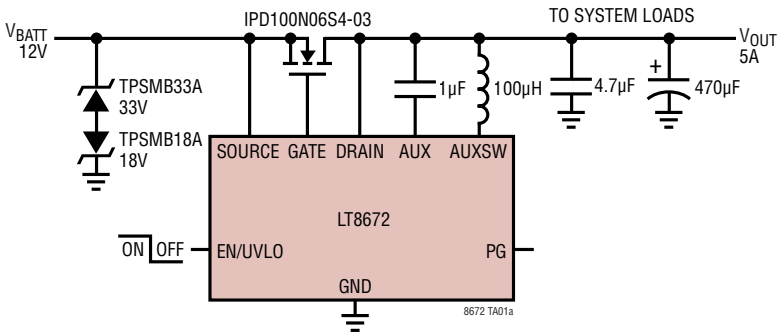
The LT®8672 is an active rectifier controller for reverse input protection. It drives an external N-channel MOSFET to replace a power Schottky diode. Its very low quiescent current and fast transient response meet the tough requirements in automotive applications where AC input signals of up to 100kHz are present. These signals are rectified with minimum power dissipation on the external FET, simplifying thermal management on the PCB.

With a drop of only 20mV, the LT8672 solution eases the minimum input voltage requirement during cold crank and start-stop, allowing simpler and more efficient circuits. If the input power source fails or is shorted, a fast turn-off minimizes reverse current transients. An available shutdown mode reduces the quiescent current to 3.5µA.

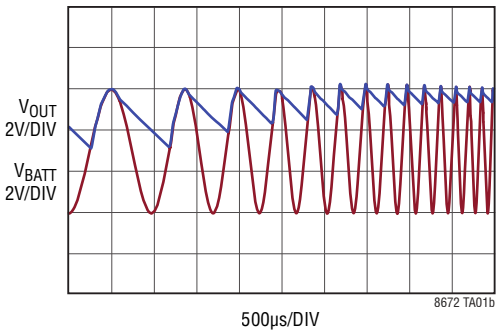
An integrated auxiliary boost regulator provides the required boost voltage to turn the external FET fully on. A power good pin signals when the external FET is ready to take load current.

TYPICAL APPLICATION

12V, 5A Automotive Reverse Battery Protection



Rectification of Input Ripple



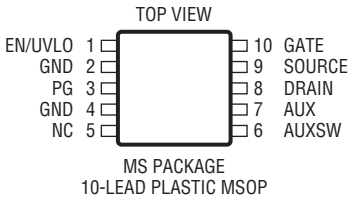
ABSOLUTE MAXIMUM RATINGS

(Notes 1 and 2)

DRAIN ..... –0.3V to 42V
SOURCE, EN/UVLO ..... –40V to 42V
DRAIN–SOURCE ..... –5V to 54V
AUX ..... V_{DRAIN} + 13V
GATE ..... V_{SOURCE} – 0.3V to V_{SOURCE} + 17V
GATE ..... V_{AUX} – 67V to V_{AUX} + 0.3V
PG ..... –0.3V to 5V

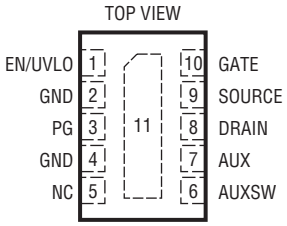
Operating Junction Temperature Range (Notes 3, 4)
E-, I-Grades ..... –40°C to 125°C
J-, H-Grades ..... –40°C to 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)
MS Package ..... 300°C

PIN CONFIGURATION



MS PACKAGE
10-LEAD PLASTIC MSOP

θ_{JA} = 160°C/W



DDB/DDBM PACKAGE
10-LEAD (3mm × 2mm) PLASTIC DFN

θ_{JA} = 76°C/W, θ_{JC} = 13.5°C/W
EXPOSED PAD (PIN 11) MUST BE SHORTED TO GND OR LEFT FLOATIN

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT8672EMS#PBF	LT8672EMS#TRPBF	LTGYT	10-Lead Plastic MSOP	–40°C to 125°C
LT8672IMS#PBF	LT8672IMS#TRPBF	LTGYT	10-Lead Plastic MSOP	–40°C to 125°C
LT8672JMS#PBF	LT8672JMS#TRPBF	LTGYT	10-Lead Plastic MSOP	–40°C to 150°C
LT8672HMS#PBF	LT8672HMS#TRPBF	LTGYT	10-Lead Plastic MSOP	–40°C to 150°C
MINI REEL				
LT8672EDDB#TRMPBF	LT8672EDDB#TRPBF	LGYS	10-Lead (3mm × 2mm) Plastic DFN	–40°C to 125°C
LT8672IDDB#TRMPBF	LT8672IDDB#TRPBF	LGYS	10-Lead (3mm × 2mm) Plastic DFN	–40°C to 125°C
LT8672JDDB#TRMPBF	LT8672JDDB#TRPBF	LGYS	10-Lead (3mm × 2mm) Plastic DFN	–40°C to 150°C
LT8672HDDB#TRMPBF	LT8672HDDB#TRPBF	LGYS	10-Lead (3mm × 2mm) Plastic DFN	–40°C to 150°C
AUTOMOTIVE PRODUCTS**				
LT8672EMS#WPBF	LT8672EMS#WTRPBF	LTGYT	10-Lead Plastic MSOP	–40°C to 125°C
LT8672IMS#WPBF	LT8672IMS#WTRPBF	LTGYT	10-Lead Plastic MSOP	–40°C to 125°C
LT8672JMS#WPBF	LT8672JMS#WTRPBF	LTGYT	10-Lead Plastic MSOP	–40°C to 150°C
LT8672HMS#WPBF	LT8672HMS#WTRPBF	LTGYT	10-Lead Plastic MSOP	–40°C to 150°C
LT8672EDDBM#WTRMPBF	LT8672EDDBM#WTRPBF	LHJR	10-Lead (3mm × 2mm) Plastic Side-Wettable DFN Package	–40°C to 125°C
LT8672IDDBM#WTRMPBF	LT8672IDDBM#WTRPBF	LHJR	10-Lead (3mm × 2mm) Plastic Side-Wettable DFN Package	–40°C to 125°C
LT8672JDDBM#WTRMPBF	LT8672JDDBM#WTRPBF	LHJR	10-Lead (3mm × 2mm) Plastic Side-Wettable DFN Package	–40°C to 150°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

**Versions of this part are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. These models are designated with a #W suffix. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{SOURCE} = V_{DRAIN} = 12V, unless otherwise noted. (Note 3)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Drain Voltage		●		2.85	3	V
Total System Quiescent Current	$V_{EN/UVLO}$ = 0V	 ●		3.5	5 15	µA µA
	$V_{EN/UVLO}$ = 2V, Active Rectifier Controller In Regulation (Note 4)	 ●		20 20	26 39	µA µA
EN/UVLO Pin Threshold High	Pin Voltage Rising	●	1.22	1.28	1.34	V
EN/UVLO Pin Threshold Low	Pin Voltage Falling	●	1.16	1.21	1.26	V
EN/UVLO Pin Hysteresis				70		mV
EN/UVLO Pin Current	$V_{EN/UVLO}$ = 2V		–0.1		0.1	µA
PG Pin Leakage	V_{PG} = 3.3V		–0.1		0.1	µA
PG Pull-Down Resistance	V_{PG} = 0.1V	●		650	2000	Ω
Auxiliary Boost Regulator						
Regulation Voltage V_{AUX} – V_{DRAIN}		●	10.2	11	11.8	V
Power NMOS Current Limit		●	75	100	120	mA
Power NMOS On-Resistance				2		Ω
Catch Diode Forward Voltage	I_{DIODE} = 100mA			0.8		V
AUXSW Pin Leakage	V_{AUXSW} = 12V		–0.2		0.2	µA
Active Rectifier Controller						
SOURCE–DRAIN Regulation Voltage		●	10	20	25	mV
SOURCE–DRAIN Fast Pull-Up Threshold		●	60	75	90	mV
DRAIN Current	With Gate Driver in Regulation			12		µA
SOURCE Current	With Gate Driver in Regulation Fault Condition, V_{SOURCE} = –40V			5	 –1	µA mA
Maximum Gate Drive (GATE–SOURCE)		●	10.2	11	11.8	V
Gate Pull-Up Current			–26	–50		mA
Gate Pull-Down Current			170	300		mA
Gate-Source Off Voltage for Reverse SOURCE	Fault Condition, V_{SOURCE} = –5V, I_{GATE} = 1mA Fault Condition, V_{SOURCE} = –40V, I_{GATE} = 1mA	● ●		0.01 0.01	0.3 0.3	V V
Gate Turn-Off Delay Time	Step (V_{SOURCE}–V_{DRAIN}) from 130mV to –70mV V_{GATE}–V_{SOURCE} < 1V, $C_{GATE–SOURCE}$ = 10nF	●		0.6	1.1	µs
Gate Turn-On Delay Time	Step (V_{SOURCE}–V_{DRAIN}) from –70mV to 130mV V_{GATE}–V_{SOURCE} > 5V , $C_{GATE–SOURCE}$ = 10nF	●		1.7	3.1	µs
Maximum Frequency of AC Input Signal to Be Rectified	AC Input Ripple < $6V_{P-P}$, $C_{GATE–SOURCE}$ = 10nF AC Input Ripple < $2V_{P-P}$, $C_{GATE–SOURCE}$ = 10nF	● ●	50 100			kHz kHz

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect the device reliability and lifetime.

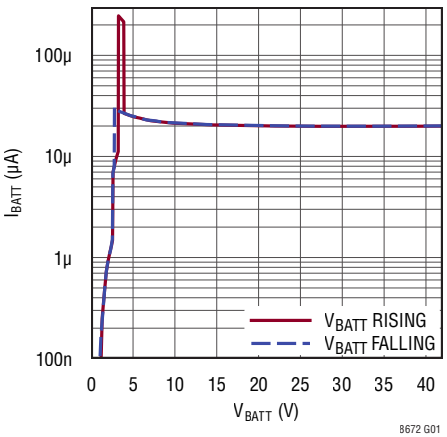
Note 2: Positive currents flow into pins, negative currents flow out of pins. Minimum and Maximum values refer to absolute values.

Note 3: The LT8672E is guaranteed to meet performance specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT8672I is guaranteed over the full –40°C to 125°C operating junction temperature range. The LT8672J and the LT8672H are guaranteed over the full –40°C to 150°C operating junction temperature range. Operating lifetime is derated at junction temperatures greater than 125°C.

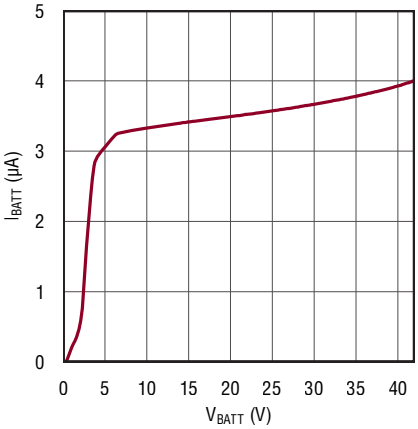
Note 4: Total system current with active rectifier controller in regulation.

TYPICAL PERFORMANCE CHARACTERISTICS

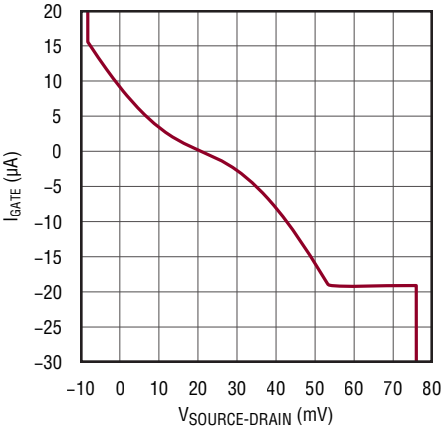
Total Input Current in Regulation



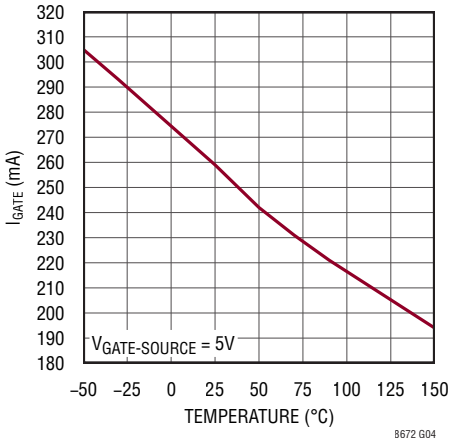
Total Input Current in Shutdown



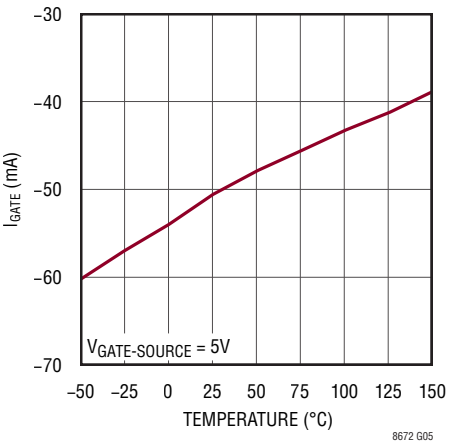
GATE Current vs Forward Voltage Drop



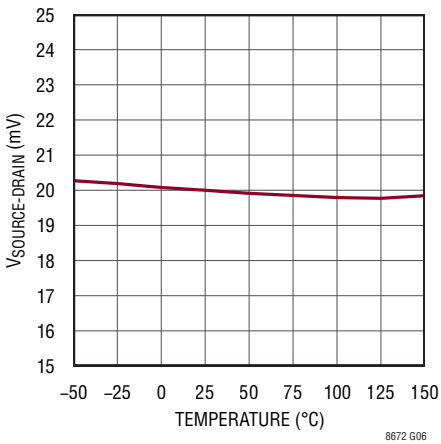
Fast Pull-Down Current



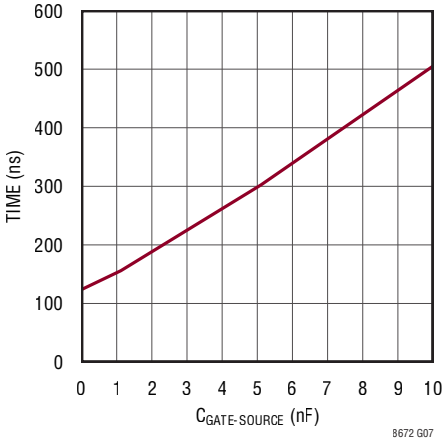
Fast Pull-Up Current



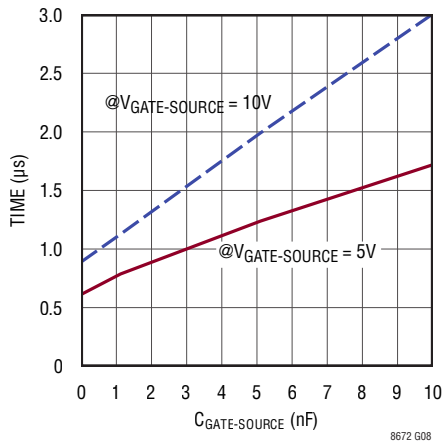
Forward Regulation Voltage



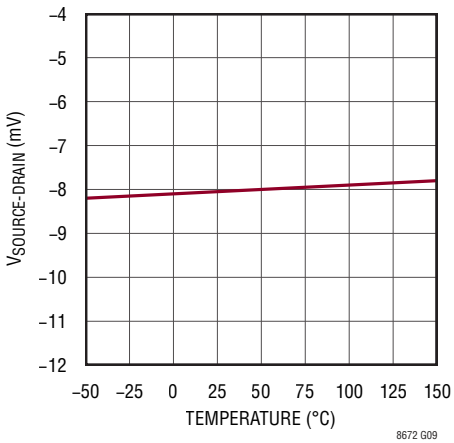
GATE Turn-Off Time vs GATE Capacitance



GATE Turn-On Time vs GATE Capacitance

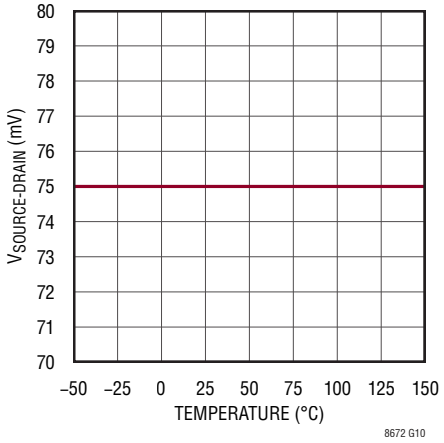


Fast Pull-Down Threshold

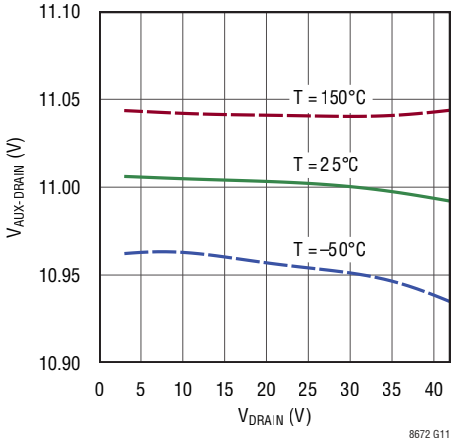


TYPICAL PERFORMANCE CHARACTERISTICS

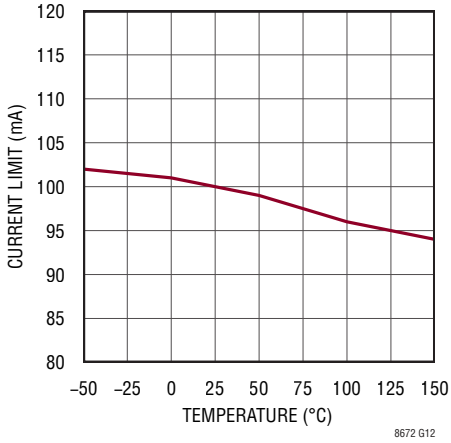
Fast Pull-Up Threshold



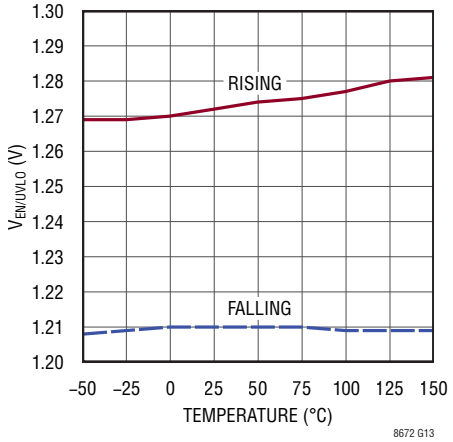
AUX–DRAIN Regulation Voltage



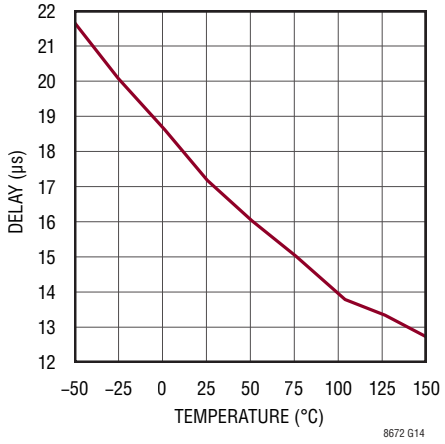
Auxiliary Boost Regulator Current Limit



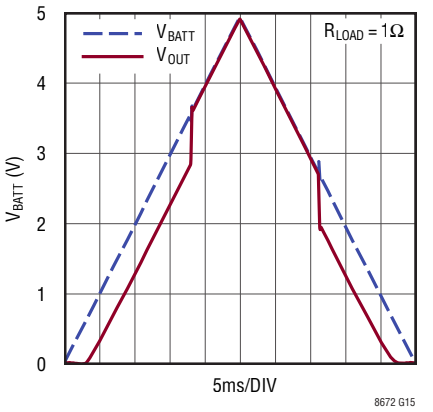
EN/UVLO Pin Thresholds



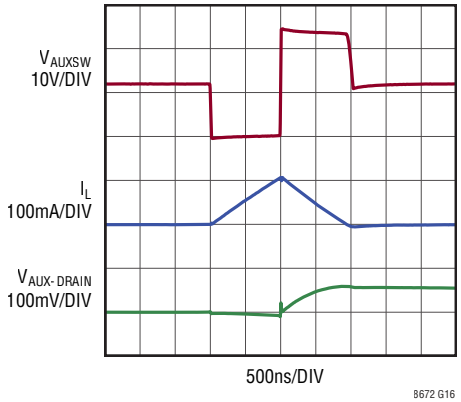
Fast Pull-Up to PG Low Delay



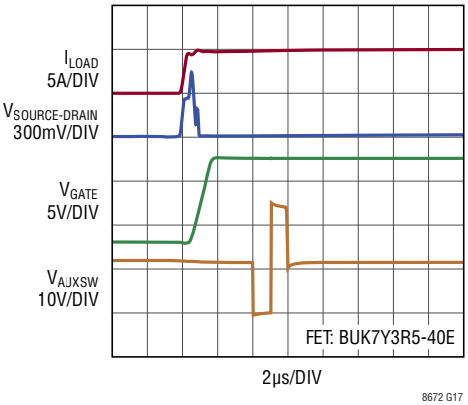
Dropout Performance



Auxiliary Boost Regulator Switching Waveforms



Auxiliary Boost Regulator Response to Fast Pull-Up



PIN FUNCTIONS

EN/UVLO (Pin 1): The LT8672's active rectifier controller and the auxiliary boost regulator are shut down when this pin is below 1.21V. Tie to DRAIN if this shutdown feature is not used.

GND (Pin 2): This pin has no function in the application and should be connected to ground.

PG (Pin 3): The PG pin is the open drain output of an internal monitor circuitry. PG pulls low if any of the following criteria is met: the part is in shutdown, the AUX voltage has not reached its regulation value during start-up or the gate driver's fast pull-up path is active for more than 17µs. If the PG pin is used to control the output load, it can protect the MOSFET from being overloaded under these conditions. PG output is valid when DRAIN is above the minimum input voltage.

GND (Pin 4): This is the ground of all the internal circuitry. Tie directly to the local GND plane.

NC (Pin 5): This pin is not connected internally. Connect it to ground or leave it floating.

AUXSW (Pin 6): Output of the Internal Power Switch of the Auxiliary Boost Regulator. This node should be kept small on the PCB for good performance and low EMI. Connect the boost inductor between this pin and the DRAIN pin.

AUX (Pin 7): Auxiliary Boost Regulator Output. This pin is used to provide a drive voltage, higher than the input voltage, to the gate driver of the active rectifier controller. Connect a 1µF capacitor between this pin and the DRAIN pin as close as possible to the IC. Do not place a capacitor to any other node than DRAIN on this pin.

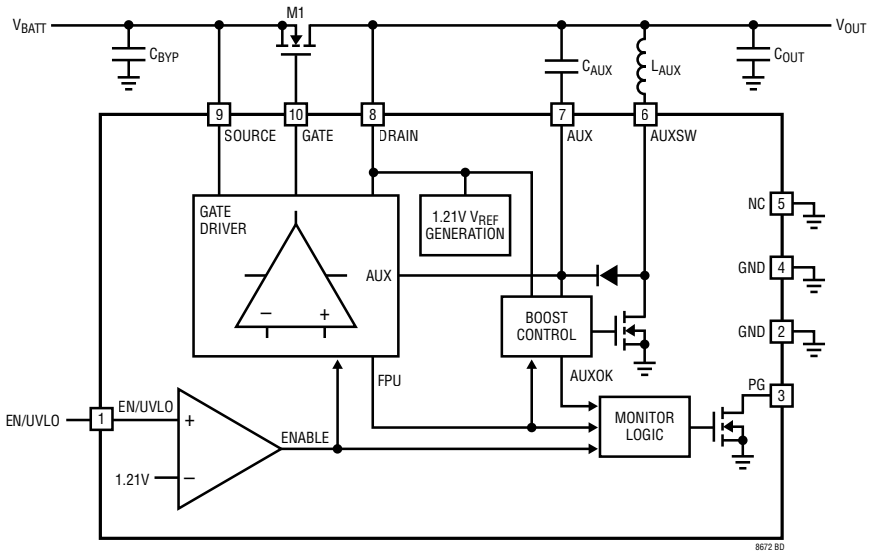
DRAIN (Pin 8): Drain Voltage Sense and Supply Voltage. The voltage sensed at this pin is used to control the external MOSFET gate. It also provides current to the LT8672's internal circuitry. Connect this pin as close as possible to the drain of the external N-channel MOSFET. This pin must be locally bypassed with at least 4.7µF.

SOURCE (Pin 9): Source Connection. SOURCE is the return path of the gate fast pull-down. The voltage sensed at this pin is also used to control the MOSFET gate. Connect this pin as close as possible to the source of the external N-channel MOSFET.

GATE (Pin 10): Gate Drive Output. This pin drives the gate of the external N-channel MOSFET. Connect this pin to the gate of the MOSFET.

Exposed Pad (Pin 11, DFN Only): The exposed pad must either be left floating or be connected to the GND pin.

BLOCK DIAGRAM



OPERATION

The LT8672 is an active rectifier controller including an integrated auxiliary boost regulator for fast turn on of the external N-channel MOSFET. Operation is best understood by referring to the Block Diagram.

Active Rectifier Controller

The active rectifier controller controls an external N-channel MOSFET (M1) to form an ideal diode. The GATE amplifier senses across DRAIN and SOURCE and drives the gate of the MOSFET to regulate the forward voltage to 20mV. As the load current increases, GATE is driven higher until a point is reached where the MOSFET is fully on. If the load current is reduced, the GATE amplifier drives the MOSFET gate lower to maintain a 20mV drop. If the voltage V_{DRAIN} is reduced to a point where a forward drop of 20mV cannot be supported, the GATE amplifier drives the MOSFET off.

During fast SOURCE–DRAIN transients such as fast varying input (SOURCE) signals where the regulating 20mV loop is too slow, fast pull-up (FPU) and fast pull-down (FPD) current paths turn on and off the external MOSFET quickly. This rectifies the input signal the same way a diode would do but with much less power dissipation.

The SOURCE and GATE pins are protected against reverse input voltages of up to –40V. GATE is pulled to SOURCE when SOURCE goes negative, turning off the MOSFET and isolating DRAIN from the negative input.

The gate voltage for the external MOSFET is provided by the auxiliary boost regulator, which regulates its output AUX to 11V above DRAIN.

The EN/UVLO pin can be used to shut down the active rectifier controller and auxiliary boost regulator. By setting EN/UVLO low, total system input current is reduced to less than 3.5µA. The conduction path on the external MOSFET would only be through its body diode.

Note that it typically takes 7ms for the internal supply voltages to stabilize once the DRAIN voltage exceeds the minimum voltage of 2.85V.

Auxiliary Boost Regulator

The auxiliary boost regulator uses a hysteretic control scheme in conjunction with a constant low side current limit of 100mA. When the AUX–DRAIN voltage is below its nominal value of typically 11V, the low side power switch is turned on. The L_{AUX} inductor current rises, until it reaches the low side current limit of 100mA, at which point the low side switch is turned off and the inductor discharges into C_{AUX} until its current falls to zero. Then, the low side switch turns on again, unless the AUX–DRAIN voltage has risen above its nominal value. In this case, all high power circuitry is shut off in order to reduce the quiescent current.

This control scheme results in a switching frequency which depends on inductor value and DRAIN voltage.

Power Good Pin (PG)

The open drain power good pin PG goes high impedance when no fault is present. This indicates the external MOSFET is operating properly.

APPLICATIONS INFORMATION

Active Rectifier Controller

Blocking diodes are commonly placed in series with supply inputs to protect against supply reversal. The LT8672 replaces diodes in these applications with a MOSFET to reduce both the voltage drop and power loss associated with a passive solution. The curve shown in Figure 1 illustrates the dramatic improvement in power loss achieved in a practical application. This represents significant savings in board area by greatly reducing power dissipation in the pass device. At low input voltages, the improvement in forward voltage loss is readily appreciated where headroom is tight, as shown in Figure 2.

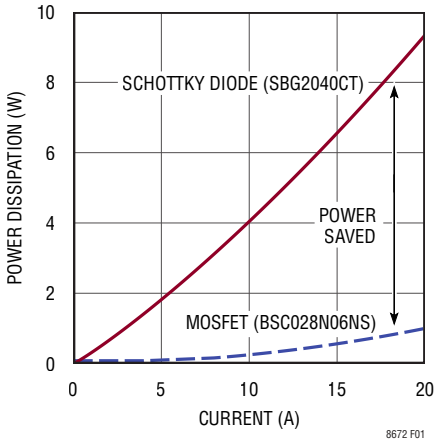


Figure 1. Power Dissipation Comparison Between MOSFET and Schottky Diode

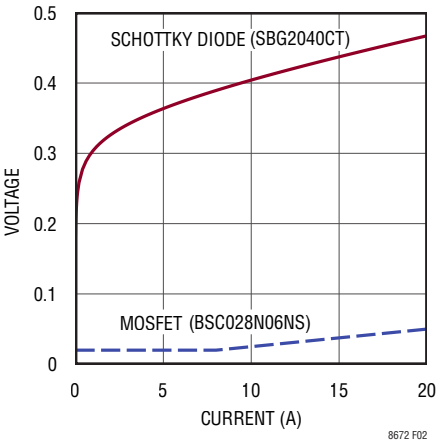


Figure 2. Forward Voltage Drop Comparison Between MOSFET and Schottky Diode

The LT8672 operates from 3V to 42V and withstands an absolute maximum range of –40V to 42V without damage. In automotive applications the LT8672 operates through load dump, cold crank and two-battery jumps, and it survives reverse battery connections while also protecting the load. Furthermore, due to its fast response to changes in the external MOSFET's forward voltage, it can rectify input ripple with amplitudes as high as $6V_{P-P}$ up to 50kHz. Rectification up to 100kHz is possible with amplitudes as high as $2V_{P-P}$. The fast gate drive capability of the LT8672 prevents the external MOSFET from overheating during these demanding conditions since its body diode conducts current only for a very small portion of the ripple period.

The LT8672 does not require any bypass capacitor at the SOURCE pin (C_{BYP} in the Block Diagram). Should such a capacitor be needed for other reasons, for example as part of an up-front EMI filter, its capacitance must not exceed 60nF; otherwise, the gate driver's stability may be impaired. This applies to the total capacitance connected to SOURCE on the PCB.

It is important to note that the EN/UVLO pin, while disabling the LT8672 and reducing its current consumption to 3.5µA, does not disconnect the load from the input since the MOSFET's body diode is ever-present.

Shutdown Mode/Undervoltage Lockout

In shutdown, the LT8672 pulls GATE low to SOURCE, turning off the MOSFET and reducing current consumption to 3.5µA. Shutdown does not interrupt forward current flow; a path is still present through M1's body diode. When enabled, the LT8672 operates as an active rectifier. If shutdown is not needed, connect EN/UVLO to DRAIN. EN/UVLO may be driven with a 3.3V or 5V logic signal. To disable the part, EN/UVLO must be pulled down below 1.21V.

APPLICATIONS INFORMATION

Adding a resistive divider from SOURCE to EN/UVLO, as shown in Figure 3, programs the LT8672 to disable itself when V_{BATT} is below a threshold voltage $V_{BATT(EN/UVLO)}$, given by:

$$R1 = R2\left(\frac{V_{BATT(EN/UVLO)}}{1.21V} - 1\right)$$

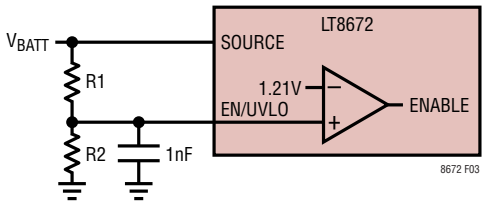


Figure 3. EN/UVLO Pin Allows Programmable Undervoltage Lockout

Note that due to the comparator's hysteresis, the LT8672 will not be enabled until V_{BATT} rises slightly above $V_{BATT(EN/UVLO)}$. If EN/UVLO is connected using a high ohmic resistor, it is subject to capacitive coupling from nearby clock lines or traces exhibiting high dV/dt. Bypass EN/UVLO to GND with 1nF to eliminate injection.

This capacitor, if sized accordingly, will also prevent negative voltage transients on V_{BATT} from inadvertently disabling the LT8672.

Input Short-Circuit Faults and Negative Transients

For fast negative input transients, the LT8672 relies on its fast pull-down (FPD) comparator. But since the FPD threshold is negative, reverse current is built up in the external MOSFET prior to an FPD turn-off. This process resembles the reverse recovery of a diode, although cause and timing differ. Since there is always a parasitic or, in case of an up front EMI filter, intended inductance in front of SOURCE, the reverse current stores energy in this inductance. This energy pulls the SOURCE node negative, once the external MOSFET is finally turned off. A zero impedance short-circuit directly across the input and ground is especially troublesome because it permits the highest possible reverse current to build up.

This negative transient on SOURCE may potentially be destructive to the LT8672, since the voltage on the SOURCE pin is limited to –40V. To prevent damage to the LT8672, protect the SOURCE pin as shown in Figure 4 by clamping to the ground node with two TVS diodes. Negative spikes, seen after the MOSFET turns off during an FPD event, are clamped by D2. The example, an 18V TVS, is a good choice for automotive applications, where a reversed battery could produce a reverse voltage of up to 14.4V, at which D2 should not conduct any current. D2 is not required if reverse-input protection is not needed.

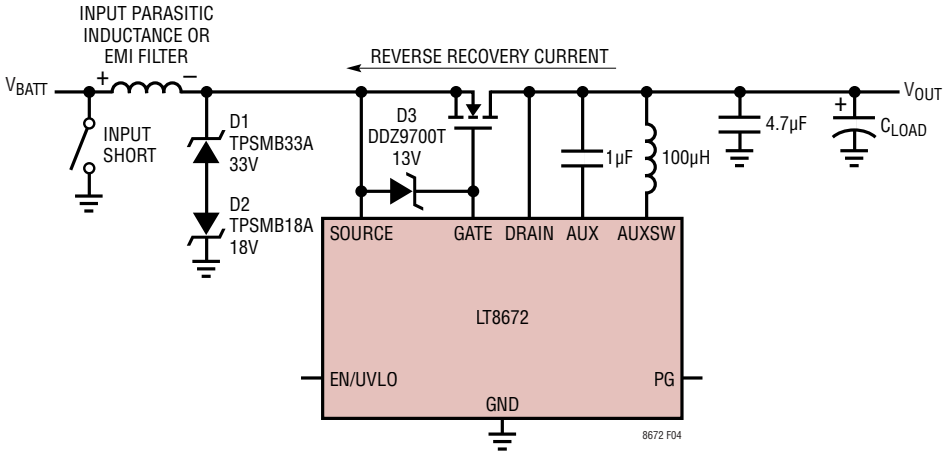


Figure 4. Reverse Recovery Produces an Inductive Spike at the SOURCE Pin. The Polarity of Step Recovery Is Shown Across the Parasitic Inductance (See Text for D3)

APPLICATIONS INFORMATION

D1 protects SOURCE in the positive direction during load steps and overvoltage conditions. The example, a 33V TVS, is a good choice for automotive applications, where a load dump could produce an overvoltage at which D1 should not conduct any current.

If neither D1 nor any reverse current protection (D2) is needed, a diode is still required at SOURCE to protect the LT8672 from negative inductive spikes caused by any parasitic input inductance.

For input voltages 4V greater than $V_{GS(MAX)}$ of the external MOSFET, a direct short (minimal inductance of less than a few nH) at the SOURCE node on the PCB could temporarily increase the V_{GS} of the external MOSFET above its $V_{GS(MAX)}$. If such a short is to be expected, D3 is needed to protect the external MOSFET.

Any leakage current in D3 will increase the total quiescent current accordingly. In addition, D3's leakage current should not exceed 5µA, as it would otherwise create an offset at the gate driver's input, increasing the SOURCE–DRAIN regulation voltage.

Rectification of Fast Input Ripple

The LT8672 is specifically designed to address the challenging specifications for battery connected automotive electronic control units (ECUs). For example, according to automotive norms ISO16750 or LV124 an ECU may be subjected to an AC ripple superimposed on its supply, with frequencies of up to 30kHz and amplitudes of up to $6V_{P-P}$.

Due to its gate driver's high output current and short delay times, the LT8672 is able to control the external MOSFET rapidly enough even at these frequencies to keep power dissipation and reverse current conduction to a minimum. In addition, this significantly reduces the ripple current in the output capacitor.

Figure 5, Figure 6 and Figure 7 show input and output waveforms for various input ripple frequencies.

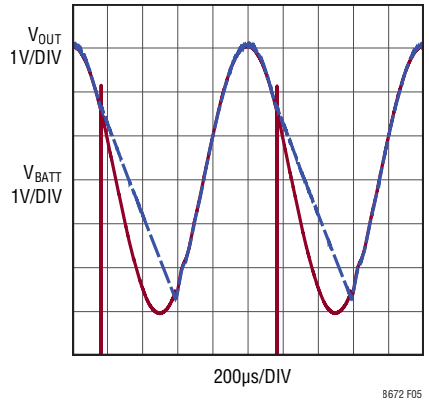


Figure 5. Rectification of Input Ripple Waveform (f = 1kHz, 5A Load Current)

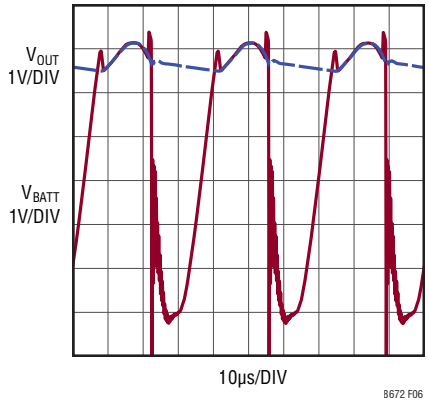


Figure 6. Rectification of Input Ripple Waveform (f = 30kHz, 5A Load Current)

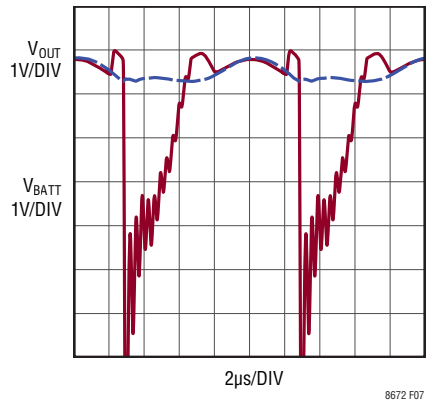


Figure 7. Rectification of Input Ripple Waveform (f = 100kHz, 5A Load Current)

APPLICATIONS INFORMATION

MOSFET Selection

All load current passes through an external MOSFET, M1. The important characteristics of the MOSFET are on-resistance, $R_{DS(ON)}$, the maximum drain-source voltage, B_{VDSS}, the gate threshold voltage $V_{GS(TH)}$ and the total gate charge Q_{GTOT}.

Gate drive is compatible with standard threshold and logic-level MOSFETs over the entire operating range of 3V to 42V. For logic-level MOSFETs, $V_{GS(MAX)}$ should be ±15V or higher.

The maximum allowable drain-source voltage, B_{VDSS}, must be higher than the power supply voltage. If the input is grounded, the full supply voltage will appear across the MOSFET. If the input is reversed and the output is held up by a charged capacitor, battery or power supply, the sum of the input and output voltages will appear across the MOSFET and require a $B_{VDSS} > V_{OUT} + |V_{BATT}|$.

The MOSFET's on-resistance, $R_{DS(ON)}$, directly affects the forward voltage drop and power dissipation. Desired forward voltage drop should be less than that of a diode for reduced power dissipation; 60mV is a good starting point. Choose a MOSFET which has:

$$R_{DS(ON)} < \frac{\text{Forward Voltage Drop}}{I_{LOAD}}$$

The resulting power dissipation is

$$P_d = I_{LOAD}^2 \bullet R_{DS(ON)}$$

For fast gate drive operation choose a MOSFET with the smallest total gate charge Q_{GTOT} that also satisfies the B_{VDSS} and $R_{DS(ON)}$ requirements. A MOSFET with smaller Q_{GTOT} not only reduces reverse current during the turn-off phase but also stays cooler during rectification of high amplitude ripple on the input.

If the MOSFET has an integrated gate protection, its leakage should not exceed 5µA, as this would otherwise create an offset at the gate driver's input, increasing the SOURCE–DRAIN regulation voltage.

When the LT8672 rectifies an AC ripple voltage, the average current through the external MOSFET still equals the load current, but the peak current is much higher. Since the MOSFET's power dissipation is proportional to the square of this current as described above, the average power dissipation during rectification exceeds the power dissipation in steady state. The actual peak current depends on the external components and their parasitics. Figure 8 shows a simple model which can be used to estimate the peak current by computer simulation. R_{BATT} represents the impedance of the voltage source V_{BATT}, the inductor models the combined inductance of the cable and, if present, the EMI filter inductor. The ideal diode has no resistance and a forward voltage of 0V. $R_{DS(ON)}$ represents the on-resistance of the external MOSFET, while C_{LOAD} and R_{ESR} represent the electrolytic capacitor and its equivalent series resistance.

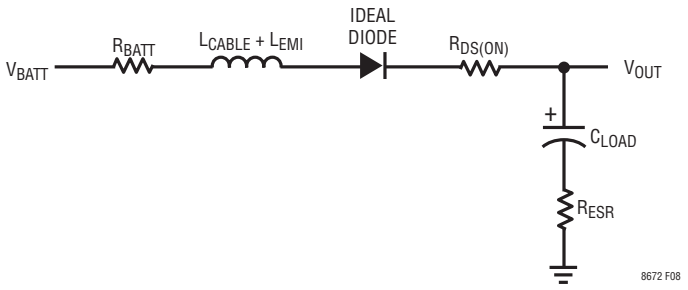


Figure 8. Simplified Application Model Including All Relevant Parasitics

APPLICATIONS INFORMATION

For example, an application with C_{LOAD} = 470µF, R_{ESR} = 16mΩ, $R_{DS(ON)}$ = 5mΩ, L_{CABLE} + L_{EMI} = 1µH, and R_{BATT} = 50mΩ dissipates 0.5W of power in steady state with a load current of 10A. But this power increases to 1.13W when a 6V_{P-P} AC-ripple with a frequency of 10kHz is superimposed on V_{BATT}. Removing any inductance raises this power even further to 1.3W, while the RMS current in C_{LOAD} reaches 12.6A.

This model can also be used to select an electrolytic capacitor which can handle the corresponding RMS current for the duration of the AC-ripple.

Electrolytic Capacitor and Ripple Voltage

During rectification, the electrolytic capacitor C_{LOAD} reduces the ripple voltage seen by the load. Figure 9 shows the corresponding waveforms for the rectification of a sinusoidal SOURCE ripple voltage.

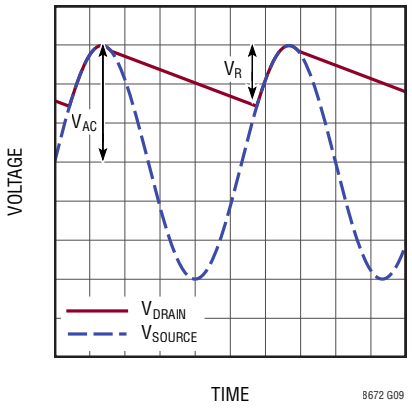


Figure 9. Waveforms For Rectification Of a Sinusoidal SOURCE Ripple Voltage

The load is exposed to the remaining ripple voltage V_R, which depends on C_{LOAD}, ripple frequency, ripple amplitude, and load current. This ripple voltage decreases with frequency and is approximately:

$$V_R = \frac{4V_{AC} \bullet I_{LOAD}}{4V_{AC} \bullet f \bullet C_{LOAD} + I_{LOAD}}$$

where V_{AC} is the ripple amplitude in V, f the ripple frequency in Hz, C_{LOAD} the capacitance of the electrolytic capacitor in F, and I_{LOAD} the load current in A. Note that any ripple caused by the equivalent series resistance of C_{LOAD} will increase V_R accordingly, in particular at high frequencies.

Since the power supply rejection of the load usually degrades with frequency, it is often desirable to limit V_R at a given frequency f. Using the above equation, the necessary minimum capacitance C_{LOAD} can be calculated from:

$$C_{LOAD} = \frac{4V_{AC} - V_R}{4V_{AC} \bullet V_R \bullet f} \bullet I_{LOAD}$$

For example, if the ripple voltage V_R is to be kept below 2V at f = 5kHz, V_{AC} = 3V (6V_{P-P}), and a load current of I_{LOAD} = 5A, then C_{LOAD} = 417µF.

When selecting an electrolytic capacitor also keep in mind the high peak currents at high frequencies as discussed in the previous section.

Automotive Cold Crank

During the so-called "cold crank" (e.g. LV124 E-11) a car's battery voltage may drop to 3.2V. As a result, the high voltage drop of traditional reverse protection schemes using passive rectifiers like Schottky diodes require the supplied circuitry to work at minimum input voltages as low as 2.5V. Buck-boost regulators may then be needed instead of simpler and more efficient buck regulators in order to provide a stable 3V supply often required by many microcontrollers.

The LT8672's minimum input operating voltage of 3V allows the active rectifier to operate through the cold crank pulse with minimum drop between input and output. This allows use of a buck regulator with a minimum operating voltage of 3V and low dropout characteristics like the LT8650S to generate a 3V supply.

Figure 10 shows input and output waveforms during a cold crank pulse, comparing the LT8672 active rectifier controller to a Schottky diode.

APPLICATIONS INFORMATION

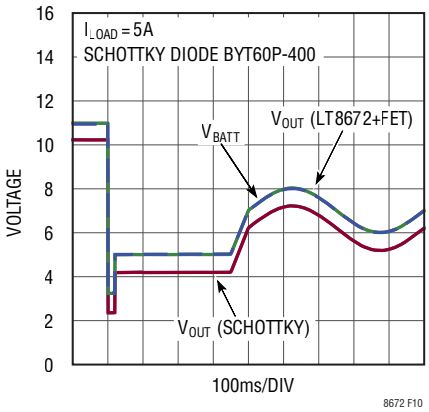


Figure 10. Automotive Cold Crank Waveforms

Auxiliary Boost Regulator

The auxiliary boost regulator provides a boosted voltage to the gate driver to enhance the external MOSFET fully with at least 10V of gate drive.

It uses a hysteretic control scheme in conjunction with a constant low side current limit of 100mA. This control scheme results in a switching frequency with a maximum value which depends on inductor value and DRAIN voltage.

Recommended boost regulator external passive components are a 1µF/16V ceramic capacitor and a 47µH to 100µH inductor. The inductor's saturation current should be at least 120mA and its ESR should not exceed 10Ω, therefore small chip inductors like CBC2518T470K or CBC2518T101K from Taiyo Yuden or those from the XPL2010 series from Coilcraft are good options.

The boost regulator maximum output current available to the gate driver on the AUX pin can be approximated by the following equation:

$$I_{AUX(MAX)} = 50 \bullet \frac{V_{DRAIN} - 1}{V_{DRAIN} + 11.8}$$

where $I_{AUX(MAX)}$ is the maximum boost regulator output current in mA and V_{DRAIN} is the DRAIN pin voltage in volts.

This maximum available AUX current is achieved at the boost regulator's maximum switching frequency which can be approximated by following equation:

$$f_{AUXSW(MAX)} = \frac{1180 \bullet (V_{DRAIN} - 0.2)}{(V_{DRAIN} + 11.6) \bullet (10L_{AUX} + 3V_{DRAIN} - 0.6)}$$

where $f_{AUXSW(MAX)}$ is the maximum switching frequency in MHz, V_{DRAIN} is the DRAIN pin voltage in volts and L_{AUX} is the boost regulator inductor in µH.

However, depending on the total average current required by the gate driver on the AUX pin to switch the external MOSFET on and off periodically, the boost regulator might enter discontinuous mode and switch at a lower frequency given by the following equation:

$$f_{AUXSW} = \frac{2.9 \bullet I_{AUX}}{L_{AUX}}$$

where f_{AUXSW} is the switching frequency in MHz, I_{AUX} is the average current required by the gate driver in mA and L_{AUX} is the boost regulator inductor in µH.

During rectification of input ripple, fully charging and discharging the gate capacitance of the external MOSFET requires an average AUX current

$$I_{AUX} = \frac{f \bullet Q_G}{1000}$$

where f is the ripple frequency in kHz, Q_G is the total gate charge of the external MOSFET in nC, and I_{AUX} is the AUX current in mA drawn by the gate driver. For example, rectification of a $6V_{P-P}$–50kHz input ripple superimposed on the 12V battery voltage, using an external MOSFET with 100nC of total gate charge under full load conditions, requires an average turn on gate current of 5mA which the gate driver takes from the AUX pin. Under these conditions, the boost regulator runs with a switching frequency of 145kHz using a 100µH inductor. The maximum available AUX current is approximately 23mA with the boost regulator switching at about 595kHz.

When the active rectifier is in steady state conditions, the AUX pin current required by the gate driver is approximately 1µA and the boost regulator is most of the time in sleep

APPLICATIONS INFORMATION

mode waking up only from time to time to maintain the AUX pin voltage 11V above DRAIN.

Figure 11, Figure 12 and Figure 13 show typical waveforms with 1µA, 5mA, and 10mA of AUX load current.

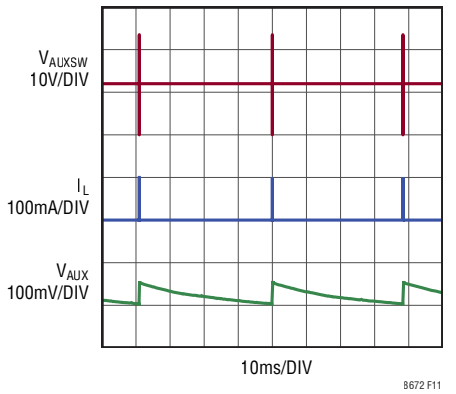


Figure 11. Auxiliary Boost Regulator Waveforms for 1µA Load on AUX (Steady State in Regulation)

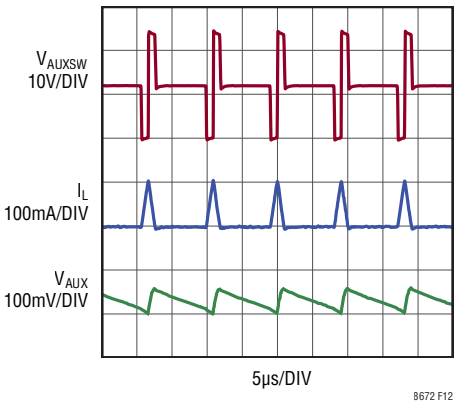


Figure 12. Auxiliary Boost Regulator Waveforms for 5mA Load on AUX

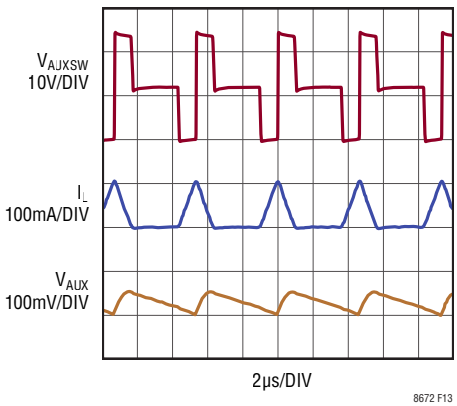


Figure 13. Auxiliary Boost Regulator Waveforms for 10mA Load on AUX

Power Good Pin

The power good pin is the output of internal monitoring circuitry, which signals when the external MOSFET is able to pass the full load current with a voltage of less than 75mV between its source and drain. PG only goes high if the LT8672 is enabled, and the AUX voltage has reached its regulation value during start-up, and if the gate driver's fast pull-up path is not engaged for more than 17µs. This allows detection of a number of system faults.

For example, the gate of the external MOSFET may be shorted to ground or source. It would then be impossible to turn it on, which would keep the gate driver's fast pull-up path active indefinitely, thereby pulling PG low. The fast pull-up path would never be active for so long in a correctly working system, because charging the external MOSFET's gate requires much less time.

An insufficient AUX voltage (for example during start-up or due to a system fault) may be able to deliver sufficient gate-source voltage to the external MOSFET for small load currents, but not for high load currents. Therefore PG is pulled low if AUX remains too low during start-up.

PG is valid (and pulls low) even in shutdown. Although this may increase the overall shutdown current through the external pull-up resistor on PG, it keeps the system correctly informed about the shutdown status of the LT8672 and that it cannot enhance the external MOSFET.

Thus, if PG is used to control the load current in the external MOSFET, its body diode can be prevented from conducting large currents for a prolonged period of time. This significantly reduces the amount of heat generated by the external MOSFET even in fault conditions.

The fast pull-up path is active when the external MOSFET's forward voltage exceeds 75mV, therefore it is recommended to choose a MOSFET large enough not to exceed this threshold with maximum load current. If the PG flag is ignored in the application, the MOSFET can be pushed to higher forward voltages provided that its power dissipation is kept within safe levels.

APPLICATIONS INFORMATION

The PG output is valid when DRAIN is above the minimum input voltage. Figure 14 and Figure 15 show power good pin waveforms under several "MOSFET Not Ready" conditions.

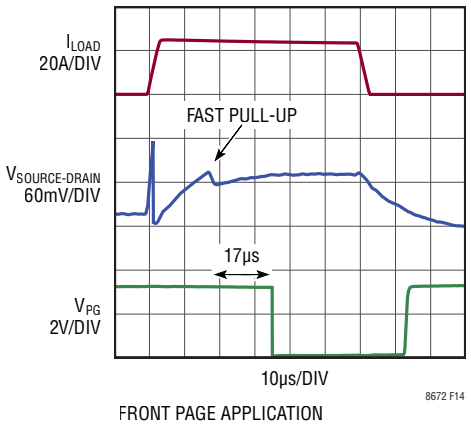


Figure 14. PG Waveform Showing How PG Responds to a Very Long Fast Pull-Up Condition

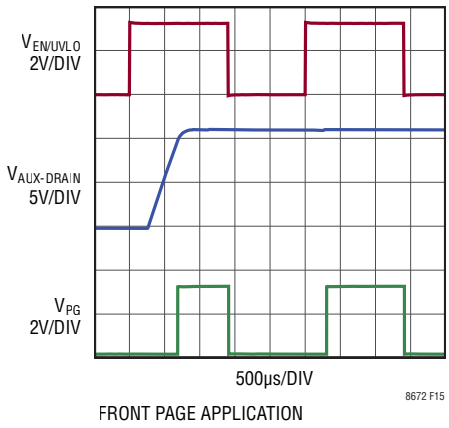


Figure 15. PG Waveform Showing How PG Behaves During Start-Up and How It Depends on EN/UVLO

Layout Considerations

Connect the SOURCE and DRAIN pins as close as possible to the MOSFET source and drain pins. Keep the traces to the MOSFET wide and short to minimize resistive losses as shown in Figure 16 and Figure 17. Place surge suppressors and necessary transient protection components close to the LT8672 using short lead lengths. Keep more than minimum distance from GATE traces to other nodes to prevent leakage that could turn the MOSFET on. Only SOURCE and DRAIN traces are allowed to run beside GATE traces. Use no-clean flux to minimize PCB contamination.

Note that the integrated boost regulator causes switched currents to flow in C_{AUX} and C_{OUT} and in the pins AUX, AUXSW, and GND. The loops formed by C_{AUX} and C_{OUT} should be minimized by placing these capacitors as close as possible to the LT8672 as shown in Figure 16 and Figure 17. C_{OUT} can be split into two capacitors C_{OUT1} (close to the LT8672) and C_{OUT2} (further away), provided that C_{OUT1} has a capacitance of at least 1µF.

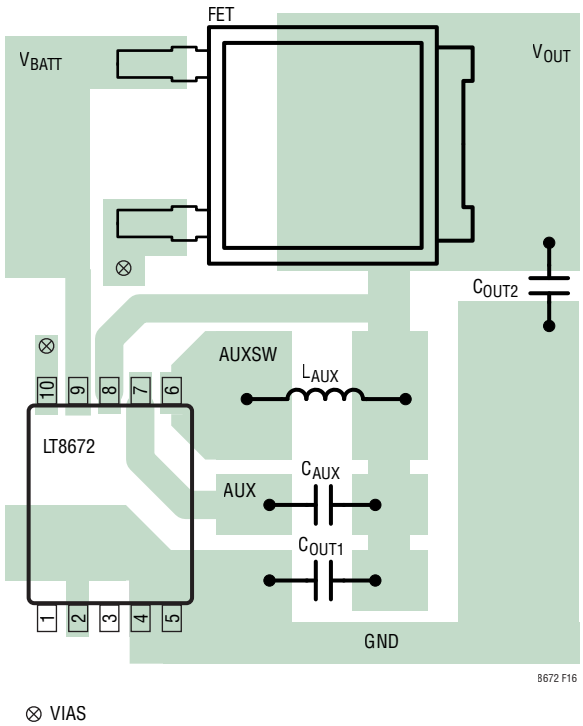


Figure 16. Recommended PCB Layout for the LT8672 (MSOP)

APPLICATIONS INFORMATION

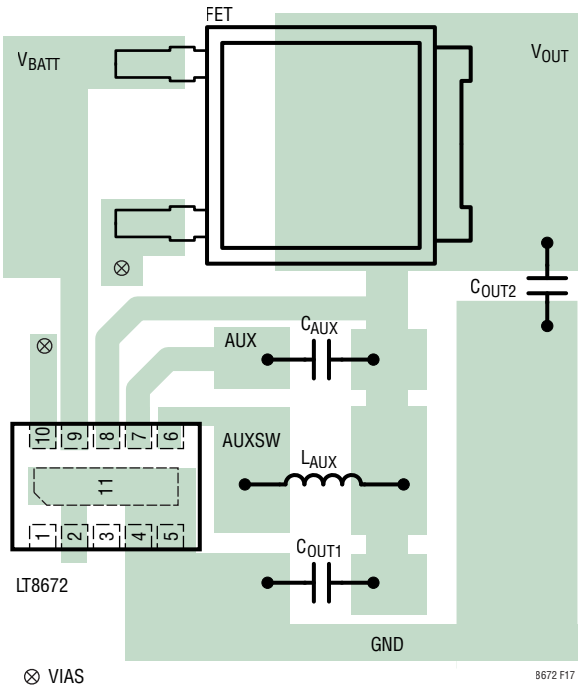
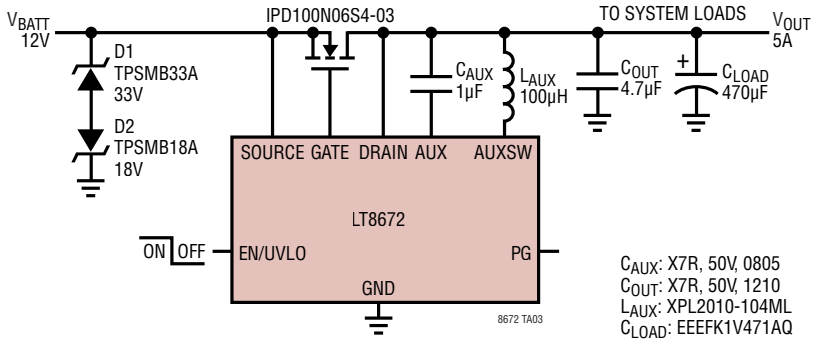


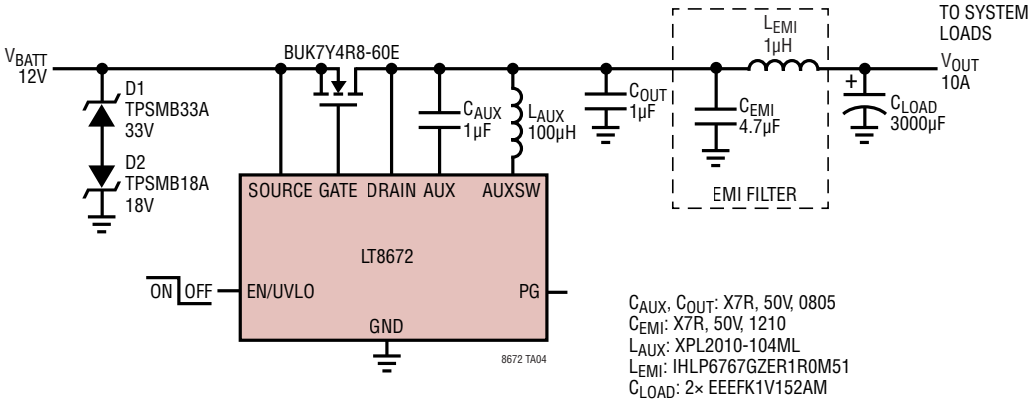
Figure 17. Recommended PCB Layout for the LT8672 (DFN)

TYPICAL APPLICATIONS

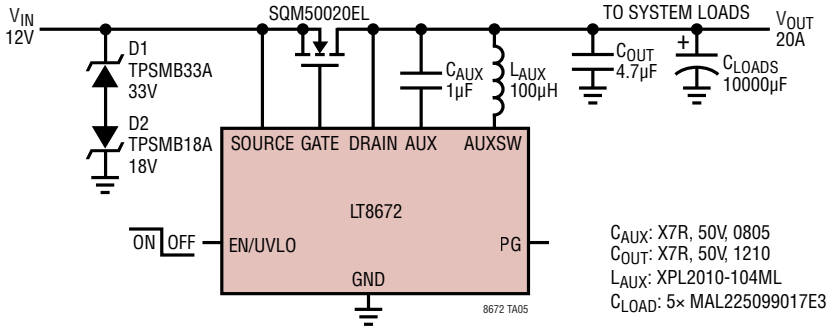
Active Rectifier for 12V Automotive Applications



Active Rectifier for 12V Automotive Applications with EMI Filter at DRAIN

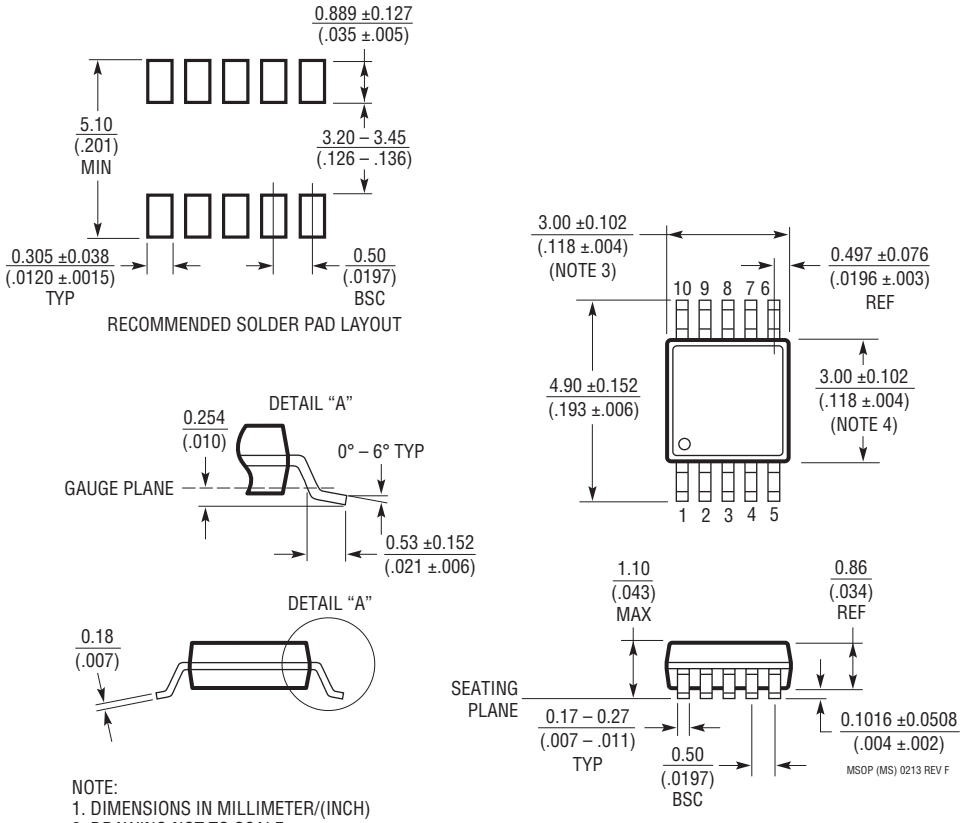


Active Rectifier for 12V Automotive Applications with High Load



PACKAGE DESCRIPTION

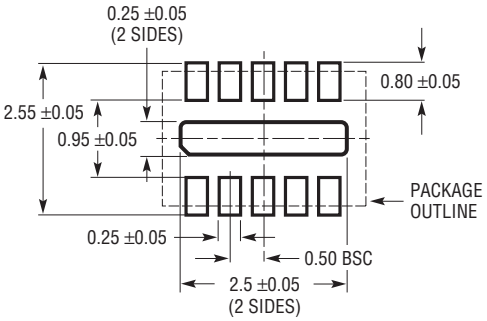
MS Package
10-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1661 Rev F)



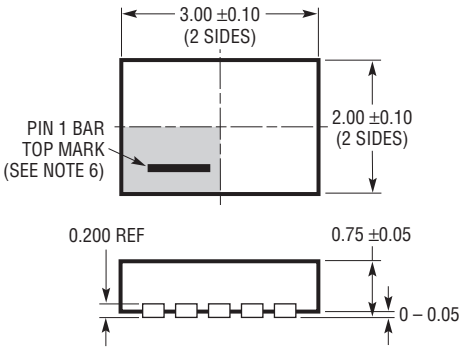
NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

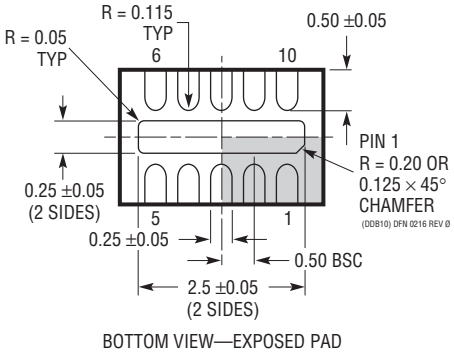
PACKAGE DESCRIPTION

DDB Package
10-Lead Plastic DFN (3mm × 2mm) COL
(Reference LTC DWG # 05-08-1531 Rev Ø)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



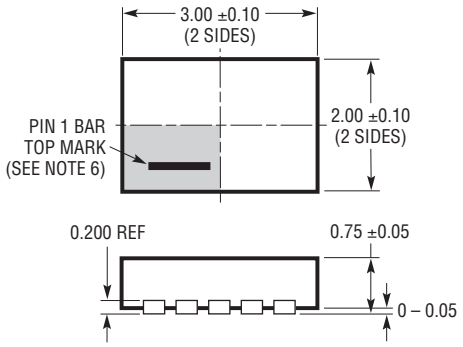


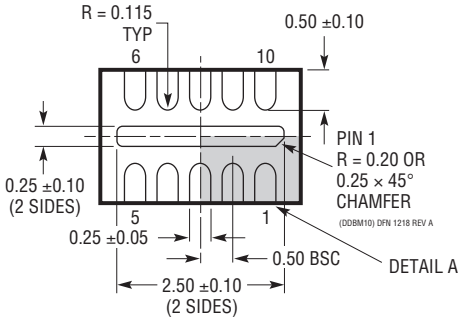
BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING CONFORMS TO VERSION (WECD-1) IN JEDEC PACKAGE OUTLINE M0-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

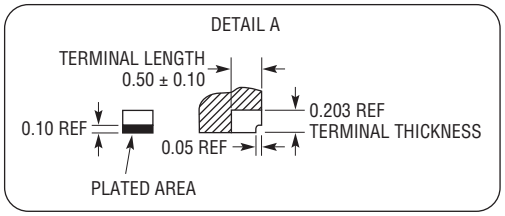
DDBM Package
10-Lead Plastic SIDE WETTABLE DFN (3mm × 2mm)
(Reference LTC DWG # 05-08-1655 Rev A)

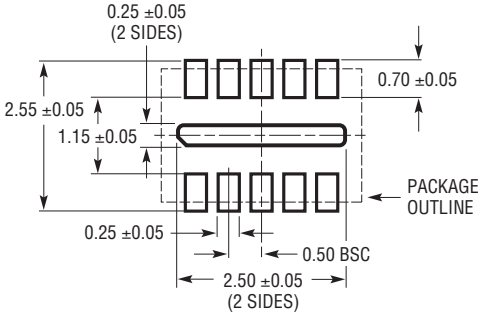




BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING CONFORMS TO VERSION (WECD-1) IN JEDEC PACKAGE OUTLINE M0-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE





RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	04/18	Added DFN package option	1, 2, 6
		Clarified Figure 16 and Figure 17	16
		Added Figure 17	17
		Added DFN package drawing	20
B	09/18	Clarified Gate Turn-On and Turn-Off Delay Time	3
C	10/18	Added J-Grade temperature option	2, 3
		Clarified θ_{JC}	2
D	04/19	Added J-Grade side-wettable plank option DFN package with W Flow (LT8672JDDBM#WTRPBF)	2
		Added side-wettable flank DFN package drawing	20