80V Synchronous 4-Switch Buck-Boost DC/DC Controller with Bidirectional Capability

FEATURES

- **Single Inductor Allows V_{IN} Above, Below, or Equal to V_{OUT}**
- **Six Independent Forms of Regulation**
  - **V_{IN} Current (Forward and Reverse)**
  - **V_{OUT} Current (Forward and Reverse)**
  - **V_{IN} and V_{OUT} Voltage**
- **Forward and Reverse Discontinuous Conduction Mode Supported**
- **Supports MODE and DIR Pin Changes While Switching**
- **V_{INCHIP} Range 2.8V (Need $EXTV_{CC}$ > 6.4V) to 80V**
- **V_{OUT} Range: 1.3V to 80V**
- **Synchronous Rectification: Up to 99% Efficiency**
- Available in 40-Lead (5mm × 8mm) QFN with High Voltage Pin Spacing and 64-Lead (10mm × 10mm) eLQFP
- AEC-Q100 in Progress

APPLICATIONS

- High Voltage Buck-Boost Converters
- Bidirectional Charging System
- Automotive 48V Systems

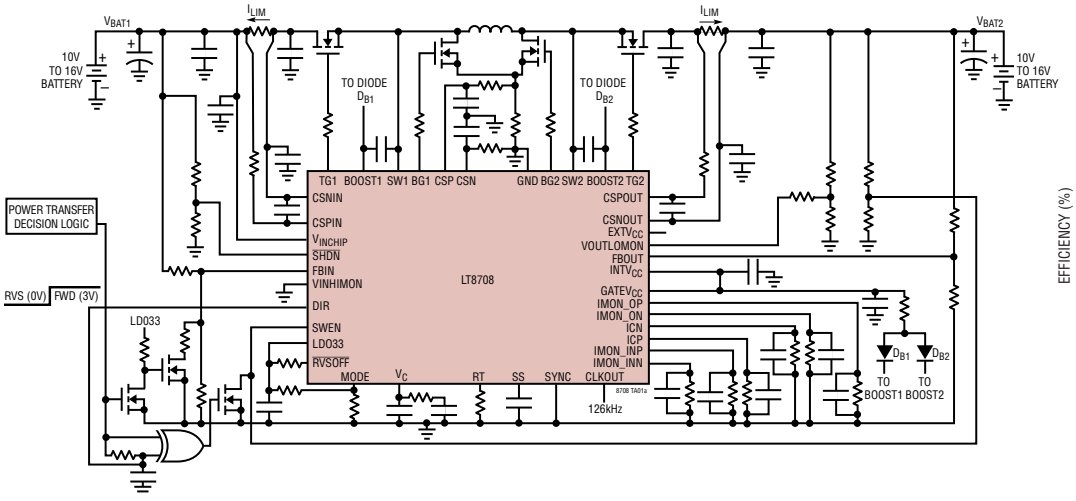
DESCRIPTION

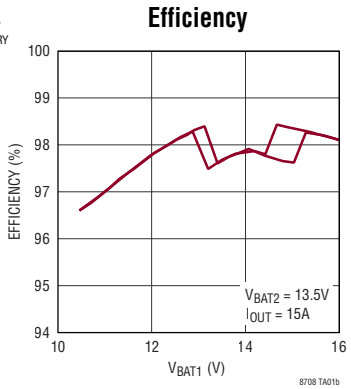
The LT®8708 is a high performance buck-boost switching regulator controller that operates from an input voltage that can be above, below or equal to the output voltage. Features are included to simplify bidirectional power conversion in battery/capacitor backup systems and other applications that may need regulation of V_{OUT}, V_{IN}, I_{OUT}, and/or I_{IN}. Forward and reverse current can be monitored and limited for the input and output sides of the converter. All four current limits (forward input, reverse input, forward output and reverse output) can be set independently using four resistors on the PCB.

The MODE pin can select between discontinuous conduction mode (DCM), continuous conduction mode (CCM), hybrid conduction mode (HCM) and Burst Mode® operation. In combination with the DIR (direction) pin, the chip can be configured to process power only from V_{IN} to V_{OUT} or only from V_{OUT} to V_{IN}. With a wide 2.8V to 80V input and 1.3V to 80V output range, the LT8708 is compatible with most solar, automotive, telecom and battery-powered systems.

TYPICAL APPLICATION

12V Bidirectional Dual Battery System with FHCM and RHCM





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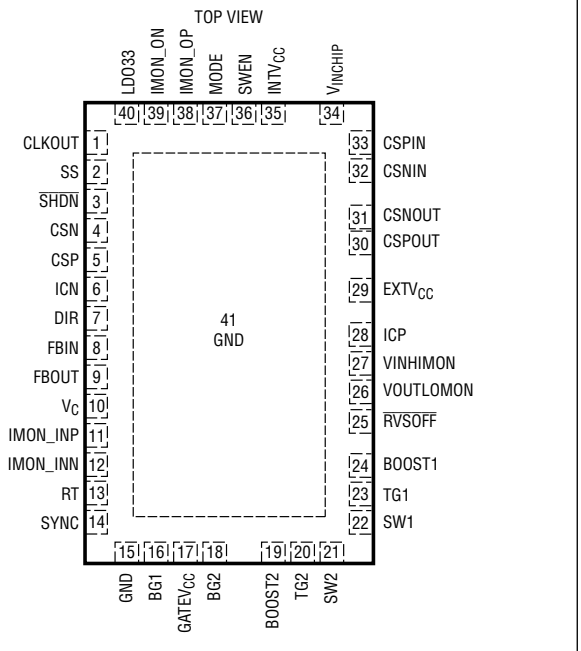
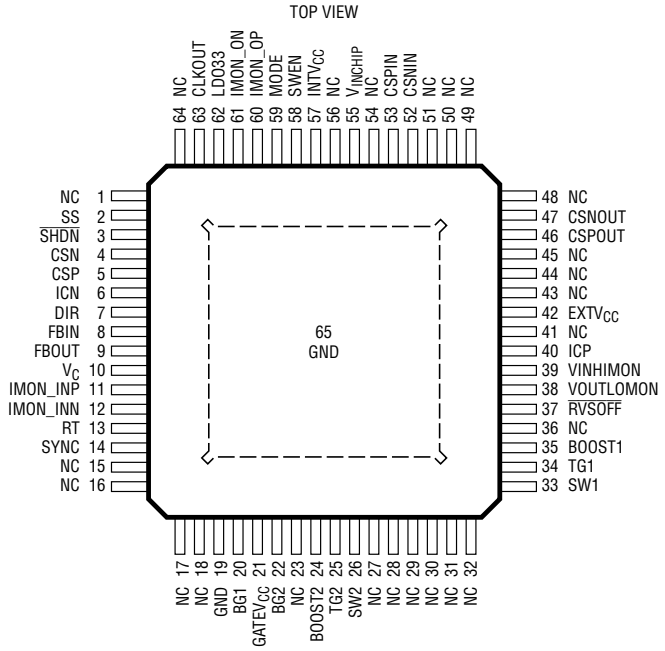
ABSOLUTE MAXIMUM RATINGS (Note 1)

$V_{CSP} – V_{CSN}$, $V_{CSPIN} – V_{CSNIN}$, $V_{CSPOUT} – V_{CSNOUT}$ ..... –0.3V to 0.3V
CSP, CSN Voltage ..... –0.3V to 3V
V_C Voltage (Note 2) ..... –0.3V to 2.2V
RT, FBOUT, SS Voltage ..... –0.3V to 5V
IMON_INP, IMON_INN, IMON_OP, IMON_ON, ICP, ICN Voltage ..... –0.3V to 5V
SYNC Voltage ..... –0.3V to 5.5V
$INTV_{CC}$, $GATEV_{CC}$ Voltage ..... –0.3V to 7V
$V_{BOOST1} – V_{SW1}$, $V_{BOOST2} – V_{SW2}$ ..... –0.3V to 7V
SWEN, $\overline{RVSOFF}$ Voltage ..... –0.3V to 7V
SWEN Current 0.5mA
$\overline{RVSOFF}$ Current 1mA
FBIN, $\overline{SHDN}$ Voltage ..... –0.3V to 30V
VINHIMON Voltage ..... –0.3V to 30V
VOUTLOMON Voltage ..... –0.3V to 5V
DIR, MODE Voltage ..... –0.3V to 5V
CSNIN, CSPIN, CSPOUT, CSNOUT Voltage –0.3V to 80V
V_{INCHIP}, $EXTV_{CC}$ Voltage ..... –0.3V to 80V
SW1, SW2 Voltage ..... 81V (Note 6)
BOOST1, BOOST2 Voltage ..... –0.3V to 87V
BG1, BG2, TG1, TG2 ..... (Note 5)
LDO33, CLKOUT ..... (Note 8)
Operating Junction Temperature Range
LT8708E (Notes 3, 8) ..... –40°C to 125°C
LT8708I (Notes 3, 8) ..... –40°C to 125°C
LT8708H (Notes 3, 8) ..... –40°C to 150°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



UHG PACKAGE
40-LEAD (5mm × 8mm) PLASTIC QFN
T_{JMAX} = 150°C, θ_{JA} = 36°C/W, θ_{JC} = 3.8°C/W
EXPOSED PAD (PIN 41) IS GND, MUST BE SOLDERED TO PCB



LWE PACKAGE
64-LEAD (10mm × 10mm) PLASTIC LQFP
T_{JMAX} = 150°C, θ_{JA} = 17°C/W, θ_{JC} = 2.5°C/W
EXPOSED PAD (PIN 65) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT8708EUHG#PBF	LT8708EUHG#TRPBF	8708	40-Lead (5mm × 8mm) Plastic QFN	–40°C to 125°C
LT8708IUHG#PBF	LT8708IUHG#TRPBF	8708	40-Lead (5mm × 8mm) Plastic QFN	–40°C to 125°C
LT8708HUHG#PBF	LT8708HUHG#TRPBF	8708	40-Lead (5mm × 8mm) Plastic QFN	–40°C to 150°C
AUTOMOTIVE PRODUCTS**				
LT8708EUHG#WPBF	LT8708EUHG#WTRPBF	8708	40-Lead (5mm × 8mm) Plastic QFN	–40°C to 125°C
LT8708IUHG#WPBF	LT8708IUHG#WTRPBF	8708	40-Lead (5mm × 8mm) Plastic QFN	–40°C to 125°C
LT8708HUHG#WPBF	LT8708HUHG#WTRPBF	8708	40-Lead (5mm × 8mm) Plastic QFN	–40°C to 150°C

TRAY	PART MARKING*	PACKAGE DESCRIPTION	MSL RATING	TEMPERATURE RANGE
LT8708ELWE#PBF	LT8708LWE	64-Lead (10mm × 10mm) Plastic eLQFP	3	–40°C to 125°C
LT8708ILWE#PBF	LT8708LWE	64-Lead (10mm × 10mm) Plastic eLQFP	3	–40°C to 125°C
LT8708HLWE#PBF	LT8708LWE	64-Lead (10mm × 10mm) Plastic eLQFP	3	–40°C to 150°C
AUTOMOTIVE PRODUCTS**				
LT8708ELWE#WPBF	LT8708LWE	64-Lead (10mm × 10mm) Plastic eLQFP	3	–40°C to 125°C
LT8708ILWE#WPBF	LT8708LWE	64-Lead (10mm × 10mm) Plastic eLQFP	3	–40°C to 125°C
LT8708HLWE#WPBF	LT8708LWE	64-Lead (10mm × 10mm) Plastic eLQFP	3	–40°C to 150°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

**Versions of this part are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. These models are designated with a #W suffix. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{INCHIP} = 12V, $\overline{SHDN}$ = 3V, DIR = 3.3V unless otherwise noted (Note 3).

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Voltage Supplies and Regulators						
V_{INCHIP} Operating Voltage Range	$EXTV_{CC}$ = 0V $EXTV_{CC}$ = 7.5V	● ●	5.5 2.8		80 80	V V
V_{INCHIP} Quiescent Current	Not Switching, V_{EXTVCC} = 0V SWEN = 3.3V SWEN = 0V			3.9 2.45	6.5 4.5	 mA mA
V_{INCHIP} Quiescent Current in Shutdown	$V_{\overline{SHDN}}$ = 0V			0	1	µA
$EXTV_{CC}$ Switchover Voltage	I_{INTVCC} = –20mA, V_{EXTVCC} Rising	●	6.15	6.4	6.6	V
$EXTV_{CC}$ Switchover Hysteresis				0.2		V
$INTV_{CC}$ Current Limit	Maximum Current Draw from $INTV_{CC}$ and LDO33 Pins Combined. Regulated from V_{INCHIP} or $EXTV_{CC}$ (12V) $INTV_{CC}$ = 5.25V $INTV_{CC}$ = 4.4V	 ● ●	 90 28	 127 42	 165 55	 mA mA
$INTV_{CC}$ Voltage	Regulated from V_{INCHIP}, I_{INTVCC} = 20mA Regulated from $EXTV_{CC}$ (12V), I_{INTVCC} = 20mA	● ●	6.1 6.1	6.3 6.3	6.5 6.5	V V
$INTV_{CC}$ Load Regulation	I_{INTVCC} = 0mA to 50mA			–0.5	–1.5	%
$INTV_{CC}$, $GATEV_{CC}$ Undervoltage Lockout	$INTV_{CC}$ Falling, $GATEV_{CC}$ Connected to $INTV_{CC}$	●	4.45	4.65	4.85	V

ELECTRICAL CHARACTERISTICS

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PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$INTV_{CC}$, $GATEV_{CC}$ Undervoltage Lockout Hysteresis	$GATEV_{CC}$ Connected to $INTV_{CC}$			170		mV
$INTV_{CC}$ Regulator Dropout Voltage	$V_{INCHIP} – V_{INTVCC}$, I_{INTVCC} = 20mA			220		mV
LDO33 Pin Voltage	5mA from LDO33 Pin	●	3.23	3.295	3.35	V
LDO33 Pin Load Regulation	I_{LDO33} = 0.1mA to 5mA			–0.25	–1	%
LDO33 Pin Current Limit	SYNC = 3V	●	12	17.25	22	mA
LDO33 Pin Undervoltage Lockout	LDO33 Falling		2.96	3.04	3.12	V
LDO33 Pin Undervoltage Lockout Hysteresis				35		mV
Switching Regulator Control						
Maximum Current Sense Threshold ($V_{CSP} – V_{CSN}$)	Boost Mode, Minimum M3 Switch Duty Cycle	●	76	93	110	mV
Maximum Current Sense Threshold ($V_{CSN} – V_{CSP}$)	Buck Mode, Minimum M2 Switch Duty Cycle	●	68	82	97	mV
Maximum Current Sense Threshold ($V_{CSN} – V_{CSP}$)	Boost Mode, Minimum M3 Switch Duty Cycle	●	79	93	108	mV
Maximum Current Sense Threshold ($V_{CSP} – V_{CSN}$)	Buck Mode, Minimum M2 Switch Duty Cycle	●	72	84	96	mV
Gain from V_C to Maximum Current Sense Voltage ($V_{CSP} – V_{CSN}$) (A5 in the Block Diagram)	Boost Mode Buck Mode			135 –135		mV/V mV/V
$\overline{SHDN}$ Input Voltage High	$\overline{SHDN}$ Rising to Enable the Device QFN LWE	 ● ●	 1.175 1.175	 1.221 1.221	 1.275 1.29	 V V
$\overline{SHDN}$ Input Voltage High Hysteresis				40		mV
$\overline{SHDN}$ Input Voltage Low	Device Disabled, Low Quiescent Current (LT8708E, LT8708I) (LT8708H)	 ● ●			 0.35 0.3	 V V
$\overline{SHDN}$ Pin Bias Current	$V_{\overline{SHDN}}$ = 3V $V_{\overline{SHDN}}$ = 12V			0 14	1 22	µA µA
SWEN Rising Threshold Voltage		●	1.156	1.208	1.256	V
SWEN Threshold Voltage Hysteresis				22		mV
SWEN Output Voltage Low	I_{SWEN} = 200µA $\overline{SHDN}$ = 0V or V_{INCHIP} = 0V $\overline{SHDN}$ = 3V	 ● ●		 0.9 0.2	 1.1 0.5	 V V
SWEN Internal Pull-Down Release Voltage	$\overline{SHDN}$ = 3V	●	0.75	0.8		V
MODE Pin Continuous Conduction Mode (CCM) Threshold		●	0.4			V
MODE Pin Hybrid DCM/CCM Mode (HCM) Range		●	0.8		1.2	V
MODE Pin Discontinuous Conduction Mode (DCM) Range		●	1.6		2.0	V
MODE Pin Burst Mode Operation Threshold		●			2.4	V
DIR Pin Forward Operation Threshold		●	1.6			V
DIR Pin Reverse Operation Threshold		●			1.2	V
$\overline{RVSOFF}$ Output Voltage Low	$I_{\overline{RVSOFF}}$ = 200µA	●		0.08	0.5	V
$\overline{RVSOFF}$ Falling Threshold Voltage		●	1.155	1.209	1.275	V
$\overline{RVSOFF}$ Threshold Voltage Hysteresis				165		mV
Soft-Start Charging Current	V_{SS} = 0V		13	19	25	µA
ICN Rising Threshold for FDCM Operation	MODE = 1V (HCM), DIR = 3.3V	●	235	255	280	mV
ICN Falling Threshold for CCM Operation	MODE = 1V (HCM), DIR = 3.3V	●	185	205	235	mV
IMON_INP Rising Threshold for RDCM Operation	MODE = 1V (HCM), DIR = 0V	●	235	255	280	mV
IMON_INP Falling Threshold for CCM Operation	MODE = 1V (HCM), DIR = 0V	●	185	205	235	mV

ELECTRICAL CHARACTERISTICS

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PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Voltage Regulation Loops (Refer to Block Diagram to Locate Amplifiers)						
Regulation Voltage for FBOUT	Regulate V_C to 1.2V	●	1.193	1.207	1.222	V
Regulation Voltage for FBIN	Regulate V_C to 1.2V	●	1.184	1.205	1.226	V
Line Regulation for FBOUT and FBIN Error Amp Reference Voltage	V_{INCHIP} = 12V to 80V. Not Switching			0.002	0.005	%/V
FBOUT Pin Bias Current	Current Out of Pin			15		nA
FBOUT Error Amp EA4 g_m				345		µmho
FBOUT Error Amp EA4 Voltage Gain				245		V/V
VOUTLOMON Voltage Activation Threshold	Falling	●	1.185	1.207	1.225	V
VOUTLOMON Threshold Voltage Hysteresis				24		mV
VOUTLOMON Pin Bias Current	$V_{VOUTLOMON}$ =1.24V, Current Into Pin $V_{VOUTLOMON}$ =1.17V, Current Into Pin	 ●	 0.8	0.01 1	 1.2	µA µA
FBIN Pin Bias Current	Current Out of Pin			10		nA
FBIN Error Amp EA3 g_m				235		µmho
FBIN Error Amp EA3 Voltage Gain				150		V/V
VINHIMON Voltage Activation Threshold	Rising	●	1.185	1.207	1.23	V
VINHIMON Threshold Voltage Hysteresis				24		mV
VINHIMON Pin Bias Current	$V_{VINHIMON}$ = 1.17V, Current Out of Pin $V_{VINHIMON}$ = 1.24V, Current Out of Pin	 ●	 0.8	0.03 1	 1.2	µA µA
Current Regulation Loops (Refer to Block Diagram to Locate Amplifiers)						
Regulation Voltages for IMON_INP and IMON_OP	V_C = 1.2V	●	1.185	1.209	1.231	V
Regulation Voltages for IMON_INN and IMON_ON	V_C =1.2V	●	1.185	1.21	1.24	V
Line Regulation for IMON_INP, IMON_INN, IMON_OP and IMON_ON Error Amp Reference Voltage	V_{INCHIP} = 12V to 80V			0.002	0.005	%/V
CSPIN Bias Current	V_{CSPIN} = 12V V_{CSPIN} = 1.5V			0.01 0.01		µA µA
CSNIN Bias Current	BOOST Capacitor Charge Control Block Not Active V_{SWEN} = 3.3V, V_{CSPIN} = V_{CSNIN} = 12V V_{SWEN} = 3.3V, V_{CSPIN} = V_{CSNIN} = 1.5V V_{SWEN} = 0V			 84 4.25 0.01		 µA µA µA
CSPIN, CSNIN Common Mode Operating Voltage Range		●	0		80	V
CSPIN, CSNIN Differential Mode Operating Voltage Range		●	–100		100	mV
IMON_INP Output Current	V_{CSPIN} – V_{CSNIN} = 50mV, V_{CSNIN} = 5V V_{CSPIN} – V_{CSNIN} = 50mV, V_{CSNIN} = 5V V_{CSPIN} – V_{CSNIN} = 5mV, V_{CSNIN} = 5V V_{CSPIN} – V_{CSNIN} = 5mV, V_{CSNIN} = 5V	 ● ●	67 64.5 22.5 20	70 70 25 25	73 75.5 27.5 30	µA µA µA µA
IMON_INN Output Current	V_{CSNIN} – V_{CSPIN} = 50mV, V_{CSNIN} = 5V V_{CSNIN} – V_{CSPIN} = 50mV, V_{CSNIN} = 5V V_{CSNIN} – V_{CSPIN} = 5mV, V_{CSNIN} = 5V V_{CSNIN} – V_{CSPIN} = 5mV, V_{CSNIN} = 5V	 ● ●	66 65 19 18	70 70 25 25	74 75 30.5 32	µA µA µA µA
IMON_INP and IMON_INN Max Output Current		●	120			µA
IMON_INP Error Amp EA5 g_m				190		µmho
IMON_INP Error Amp EA5 Voltage Gain				130		V/V
IMON_INN Error Amp EA1 g_m	FBIN = 0V, FBOUT = 3.3V			190		µmho

ELECTRICAL CHARACTERISTICS

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PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
IMON_INN Error Amp EA1 Voltage Gain	FBIN = 0V, FBOUT = 3.3V			130		V/V
CSPOUT Bias Current	V_{CSPOUT} = 12V V_{CSPOUT} = 1.5V			0.01 0.01		µA µA
CSNOUT Bias Current	BOOST Capacitor Charge Control Block Not Active V_{SWEN} = 3.3V, V_{CSPOUT} = V_{CSNOUT} = 12V V_{SWEN} = 3.3V, V_{CSPOUT} = V_{CSNOUT} = 1.5V V_{SWEN} = 0V			 83 4.25 0.01		 µA µA µA
CSPOUT, CSNOUT Common Mode Operating Voltage Range		●	0		80	V
CSPOUT, CSNOUT Differential Mode Operating Voltage Range		●	–100		100	mV
IMON_OP, ICP Output Current	V_{CSPOUT} – V_{CSNOUT} = 50mV, V_{CSNOUT} = 5V V_{CSPOUT} – V_{CSNOUT} = 50mV, V_{CSNOUT} = 5V V_{CSPOUT} – V_{CSNOUT} = 5mV, V_{CSNOUT} = 5V V_{CSPOUT} – V_{CSNOUT} = 5mV, V_{CSNOUT} = 5V (QFN) V_{CSPOUT} – V_{CSNOUT} = 5mV, V_{CSNOUT} = 5V (LWE) V_{CSPOUT} – V_{CSNOUT} = –5mV, V_{CSNOUT} = 5V V_{CSPOUT} – V_{CSNOUT} = –5mV, V_{CSNOUT} = 5V	 ● ● ● ●	67 65 22.5 20.5 20.5 12.5 10.5	70 70 25 25 25 15 15	73 76 27.5 29 30 17.5 19.5	µA µA µA µA µA µA µA
IMON_ON, ICN Output Current	V_{CSNOUT} – V_{CSPOUT} = 50mV, V_{CSNOUT} = 5V V_{CSNOUT} – V_{CSPOUT} = 50mV, V_{CSNOUT} = 5V V_{CSNOUT} – V_{CSPOUT} = 5mV, V_{CSNOUT} = 5V V_{CSNOUT} – V_{CSPOUT} = 5mV, V_{CSNOUT} = 5V V_{CSNOUT} – V_{CSPOUT} = –5mV, V_{CSNOUT} = 5V V_{CSNOUT} – V_{CSPOUT} = –5mV, V_{CSNOUT} = 5V	 ● ● ●	67 65 22.5 20.5 12.5 10.5	70 70 25 25 15 15	73 75 27.5 29 17.5 19.5	µA µA µA µA µA µA
IMON_OP, IMON_ON, ICP and ICN Max Output Current		●	120			µA
IMON_OP Error Amp EA6 g_m				190		µmho
IMON_OP Error Amp EA6 Voltage Gain				130		V/V
IMON_ON Error Amp EA2 gm	FBIN = 0V, FBOUT = 3.3V			190		µmho
IMON_ON Error Amp EA2 Voltage Gain	FBIN = 0V, FBOUT = 3.3V			130		V/V
NMOS Gate Drivers						
TG1, TG2 Rise Time	C_{LOAD} = 3300pF (Note 4)			20		ns
TG1, TG2 Fall Time	C_{LOAD} = 3300pF (Note 4)			20		ns
BG1, BG2 Rise Time	C_{LOAD} = 3300pF (Note 4)			20		ns
BG1, BG2 Fall Time	C_{LOAD} = 3300pF (Note 4)			20		ns
TG1 Off to BG1 On Delay	C_{LOAD} = 3300pF Each Driver			90		ns
BG1 Off to TG1 On Delay	C_{LOAD} = 3300pF Each Driver			80		ns
TG2 Off to BG2 On Delay	C_{LOAD} = 3300pF Each Driver			90		ns
BG2 Off to TG2 On Delay	C_{LOAD} = 3300pF Each Driver			80		ns
Minimum On-Time for Main Switch in Boost Operation ($t_{ON(M3,MIN)}$)	Switch M3, C_{LOAD} = 3300pF			200		ns
Minimum On-Time for Synchronous Switch in Buck Operation ($t_{ON(M2,MIN)}$)	Switch M2, C_{LOAD} = 3300pF			200		ns
Minimum Off-Time for Main Switch in Steady-State Boost Operation	Switch M3, C_{LOAD} = 3300pF			230		ns
Minimum Off-Time for Synchronous Switch in Steady-State Buck Operation	Switch M2, C_{LOAD} = 3300pF			230		ns

ELECTRICAL CHARACTERISTICS

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PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Oscillator						
Switch Frequency Range	SYNCing or Free Running		100		400	kHz
Switching Frequency, F_{OSC}	R_T = 365k R_T = 215k R_T = 124k	● ● ●	102 170 310	120 202 350	142 235 400	kHz kHz kHz
SYNC High Level for Synchronization		●	1.3			V
SYNC Low Level for Synchronization		●			0.5	V
SYNC Clock Pulse Duty Cycle	V_{SYNC} = 0V to 2V		20		80	%
Recommended Min SYNC Ratio F_{SYNC}/F_{OSC}				3/4		
CLKOUT Output Voltage High	$V_{LDO33} – V_{CLKOUT}$, 1mA Out of CLKOUT Pin, I_{LDO33} = 0µA			100	250	mV
CLKOUT Output Voltage Low	1mA Into CLKOUT Pin			25	100	mV
CLKOUT Duty Cycle	T_J = –40°C T_J = 25°C T_J = 125°C			22.7 44.1 77		% % %

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PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
CLKOUT Rise Time	C_{LOAD} = 200pF			20		ns
CLKOUT Fall Time	C_{LOAD} = 200pF			20		ns
CLKOUT Phase Delay	SYNC Rising to CLKOUT Rising, f_{OSC} = 100kHz	●	160	180	200	degrees

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Do not force voltage on the V_C pin.

Note 3: The LT8708E is guaranteed to meet performance specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT8708I is guaranteed over the full –40°C to 125°C junction temperature range. The LT8708H is guaranteed over the full –40°C to 150°C operating junction temperature range.

Note 4: Rise and fall times are measured using 10% and 90% levels. Delay times are measured using 50% levels.

Note 5: Do not apply a voltage or current source to these pins. They must be connected to capacitive loads only, otherwise permanent damage may occur.

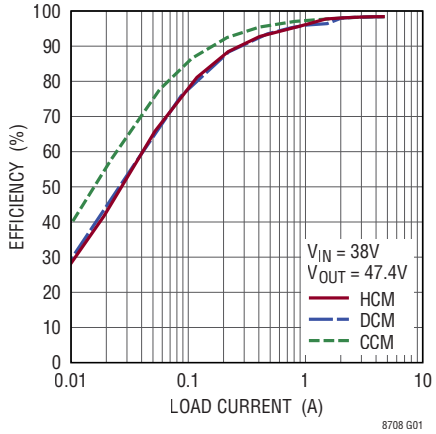
Note 6: Negative voltages on the SW1 and SW2 pins are limited, in an application, by the body diodes of the external NMOS devices, M2 and M3, or parallel Schottky diodes when present. The SW1 and SW2 pins are tolerant of these negative voltages in excess of one diode drop below ground, guaranteed by design.

Note 7: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed the maximum operating junction temperature when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

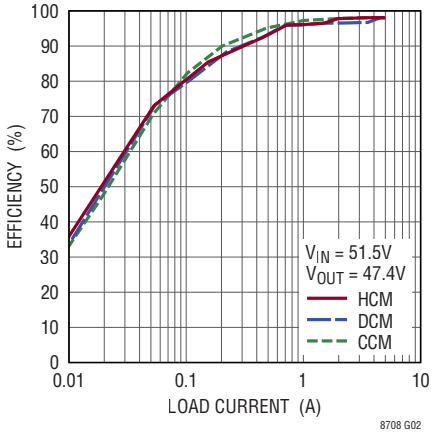
Note 8: Do not force voltage or current into these pins.

TYPICAL PERFORMANCE CHARACTERISTICS

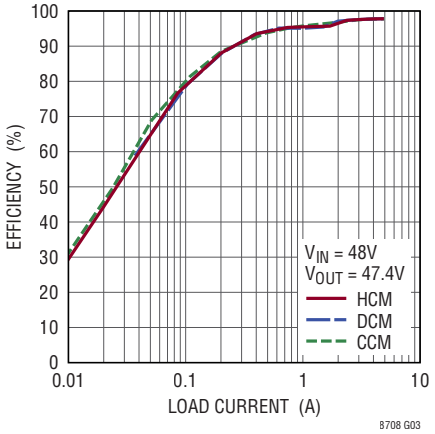
Efficiency vs Output Current (Boost Region – page 59)



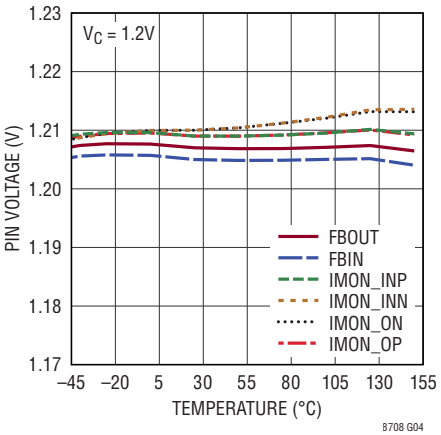
Efficiency vs Output Current (Buck Region – page 59)



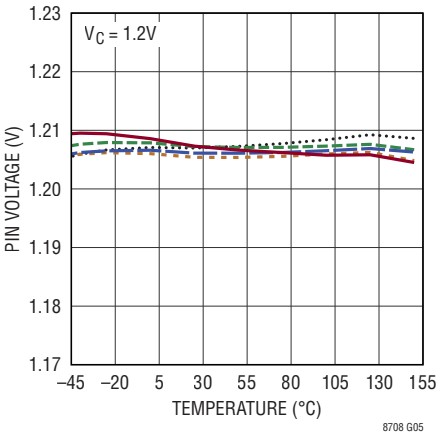
Efficiency vs Output Current (Buck–Boost Region – page 59



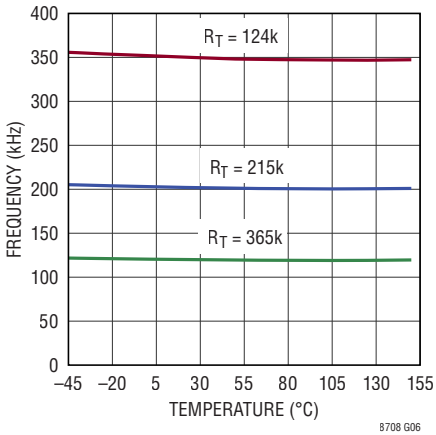
Feedback Voltages



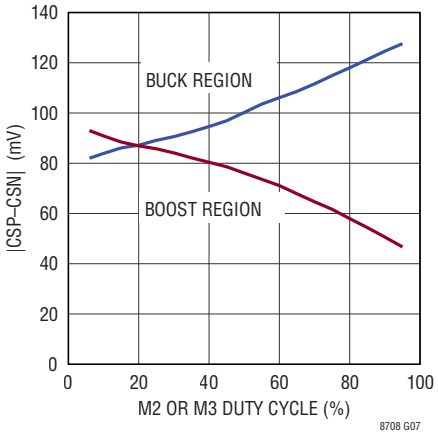
Feedback Voltages (Five Parts)



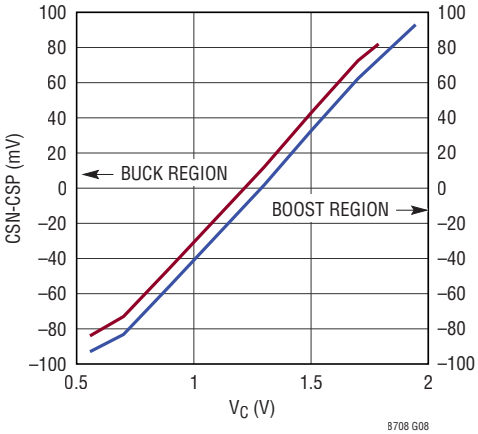
Oscillator Frequency



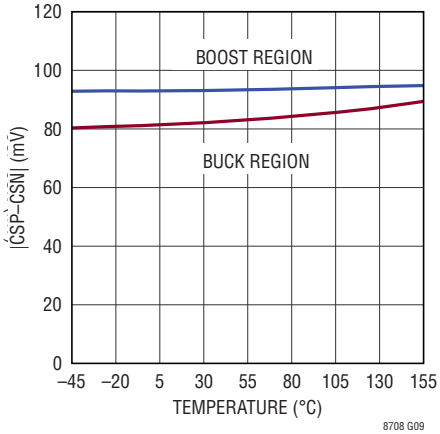
Maximum Inductor Current Sense Voltage vs Duty Cycle



Inductor Current Sense Voltage at Minimum Duty Cycle

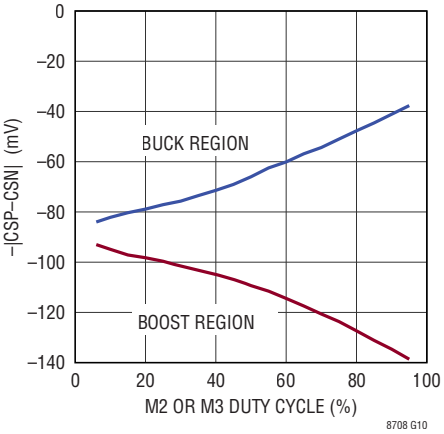


Maximum Inductor Current Sense Voltage at Minimum Duty Cycle

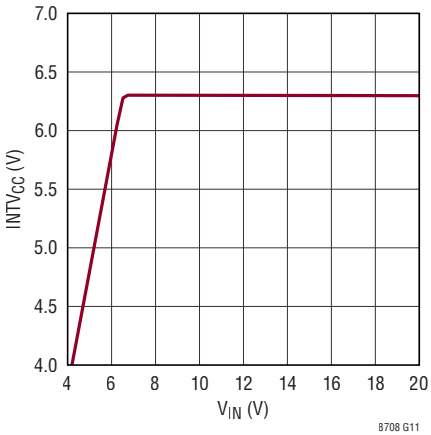


TYPICAL PERFORMANCE CHARACTERISTICS

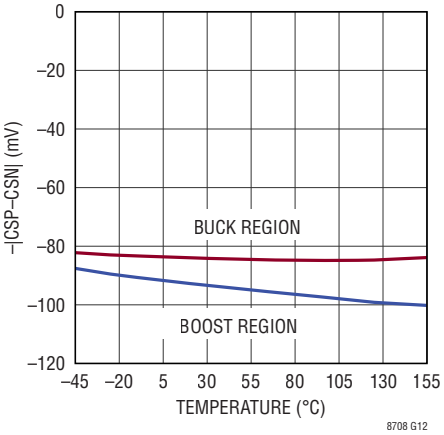
Minimum Inductor Current Sense Voltage vs Duty Cycle



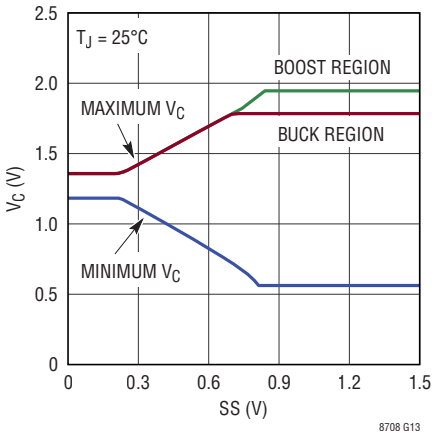
$INTV_{CC}$ Line Regulation ($EXTV_{CC}$ = 0V)



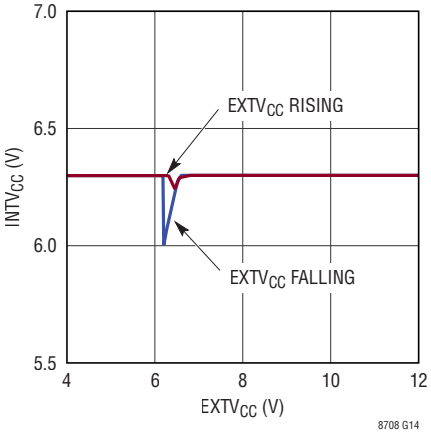
Minimum Inductor Current Sense Voltage at Minimum Duty Cycle



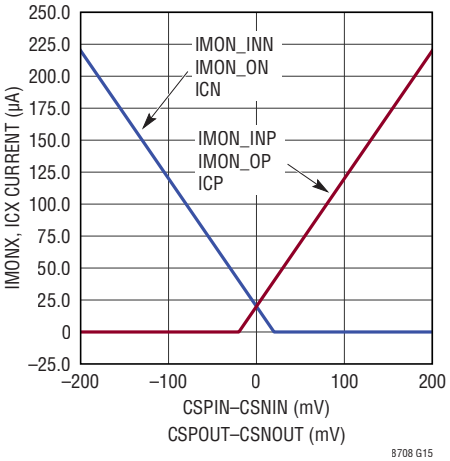
Maximum and Minimum V_C vs SS



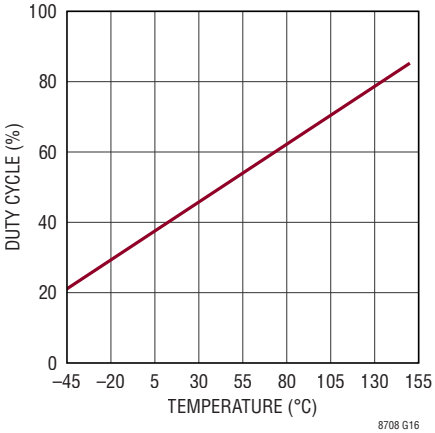
$INTV_{CC}$ Line Regulation (V_{IN} = 12V)



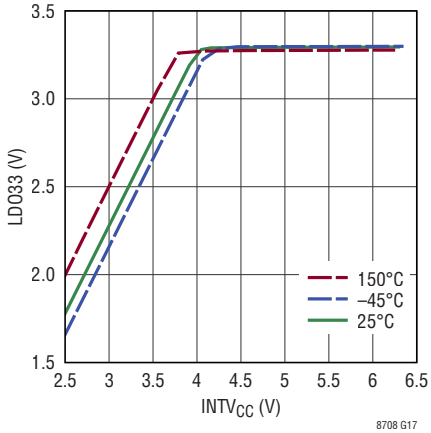
IMONx, ICx Output Current



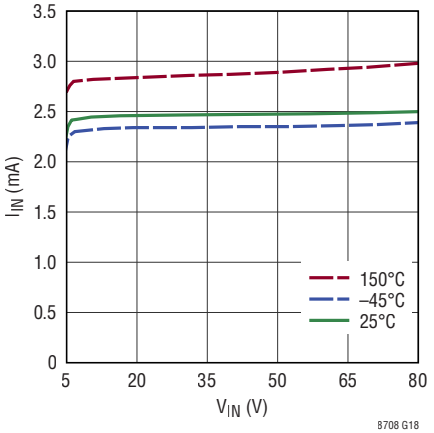
CLKOUT Duty Cycle



LDO33 Pin Regulation (I_{LDO33} = 1mA)

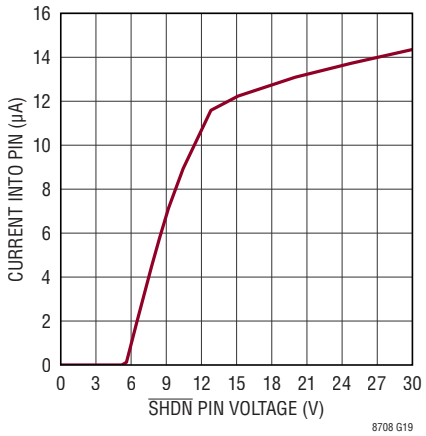


V_{IN} Supply Current vs Voltage (Not Switching)

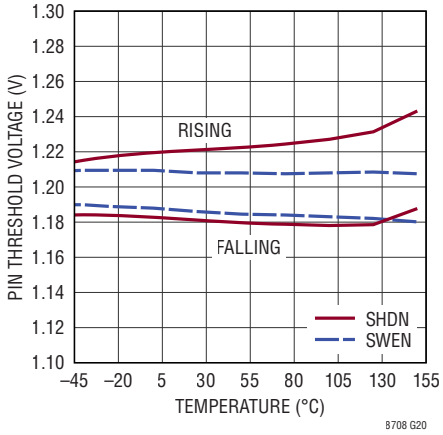


TYPICAL PERFORMANCE CHARACTERISTICS

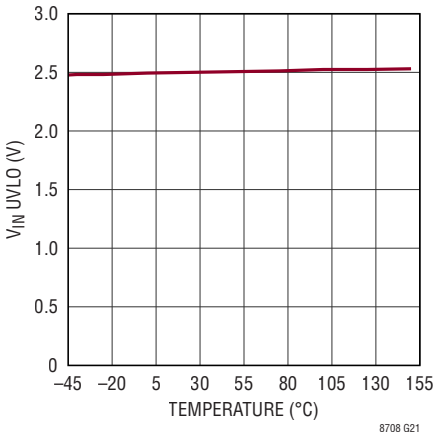
$\overline{SHDN}$ Pin Current



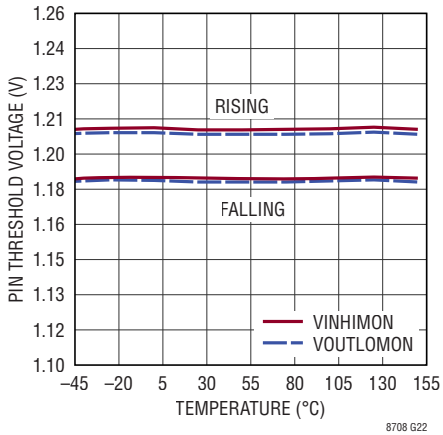
$\overline{SHDN}$ and SWEN Pin Thresholds vs Temperature



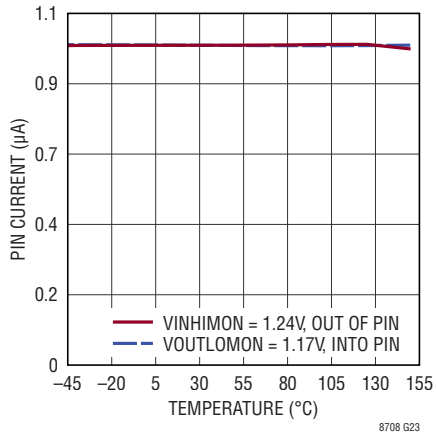
Internal V_{IN} UVLO



VINHIMON and VOUTLOMON Pin Thresholds vs Temperature

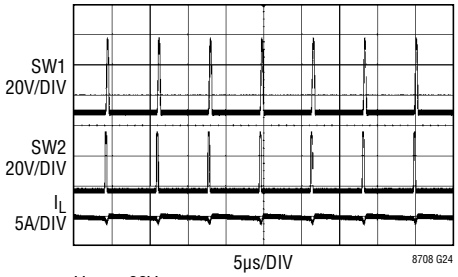


VINHIMON and VOUTLOMON Pin Hysteresis Current vs Temperature



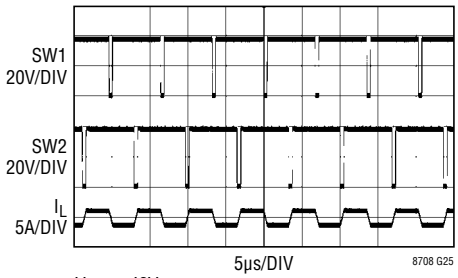
TYPICAL PERFORMANCE CHARACTERISTICS

Discontinuous Mode (page 59)



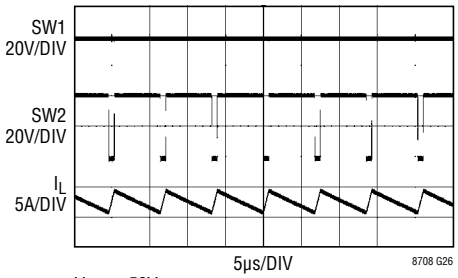
V_{BAT} = 38V
V_{LOAD} = 47.4V

Continuous Mode (page 59)



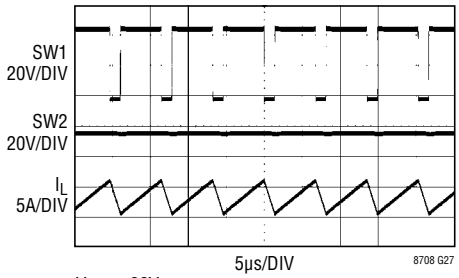
V_{BAT} = 48V
V_{LOAD} = 47.4V

Continuous Mode (page 59)



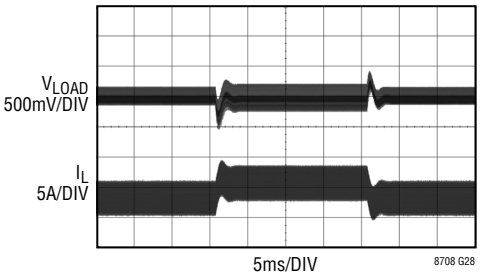
V_{BAT} = 52V
V_{LOAD} = 47.4V

Continuous Mode (page 59)



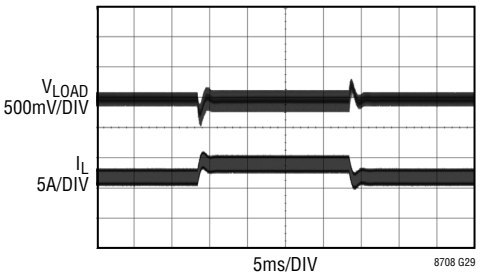
V_{BAT} = 38V
V_{LOAD} = 47.4V

Load Step (page 59)



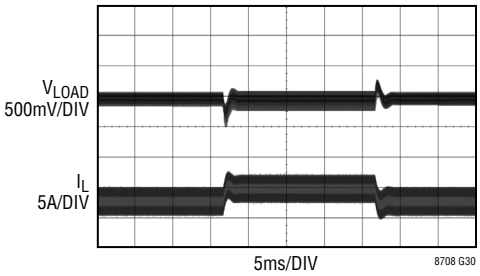
V_{BAT} = 38V
V_{LOAD} = 47.4V
LOAD STEP = 2A TO 4A

Load Step (page 59)



V_{BAT} = 52V
V_{LOAD} = 47.4V
LOAD STEP = 2A TO 4A

Load Step (page 59)



V_{BAT} = 48V
V_{LOAD} = 47.4V
LOAD STEP = 2A TO 4A

PIN FUNCTIONS (QFN/eLQFP)

CLKOUT (Pin 1/Pin 63): Clock Output Pin. Use this pin to synchronize one or more compatible switching regulator ICs to the LT8708. CLKOUT toggles at the same frequency as the internal oscillator or as the SYNC pin, but is approximately 180° out of phase. CLKOUT may also be used as a temperature monitor since the CLKOUT duty cycle varies linearly with the part's junction temperature. The CLKOUT pin can drive capacitive loads up to 200pF.

SS (Pin 2/Pin 2): Soft-Start Pin. Place at least 220nF of capacitance here. Upon start-up, this pin will be charged by an internal resistor to 3.3V.

$\overline{\text{SHDN}}$ (Pin 3/Pin 3): Shutdown Pin. Tie high to enable chip. Ground to shut down and reduce quiescent current to a minimum. Don't float this pin.

CSN (Pin 4/Pin 4): The (–) Input to the Inductor Current Sense and DCM Detect Comparator.

CSP (Pin 5/Pin 5): The (+) Input to the Inductor Current Sense and DCM Detect Comparator. The V_C pin voltage and built-in offsets between CSP and CSN pins, in conjunction with the R_{SENSE} value, set the inductor current trip threshold.

ICN (Pin 6/Pin 6): Negative V_{OUT} Current Monitor. The current out of this pin is 20µA plus a current proportional to the negative average V_{OUT} current. See the Applications Information section for more information.

DIR (Pin 7/Pin 7): Direction pin when MODE is set for DCM (discontinuous conduction mode) or HCM (hybrid conduction mode) operation. Otherwise this pin is ignored. Connect the pin to GND to process power from the V_{OUT} to V_{IN}. Connect the pin to LDO33 to process power from the V_{IN} to V_{OUT}.

FBIN (Pin 8/Pin 8): V_{IN} Feedback Pin. This pin is connected to the input of error amplifier EA3 and is used to detect and/or regulate low V_{IN} voltage.

FBOUT (Pin 9/Pin 9): V_{OUT} Feedback Pin. This pin is connected to the input of error amplifier EA4 and is used to detect and/or regulate high V_{OUT} voltage.

V_C (Pin 10/Pin 10): Error Amplifier Output Pin. Tie external compensation network to this pin.

IMON_INP (Pin 11/Pin 11): Positive V_{IN} Current Monitor and Limit Pin. The current out of this pin is 20µA plus a current proportional to the positive average V_{IN} current. IMON_INP also connects to error amplifier EA5 and can be used to limit the maximum positive V_{IN} current. See the Applications Information section for more information.

IMON_INN (Pin 12/Pin 12): Negative V_{IN} Current Monitor and Limit Pin. The current out of this pin is 20µA plus a current proportional to the negative average V_{IN} current. IMON_INN also connects to error amplifier EA1 and can be used to limit the maximum negative V_{IN} current. See the Applications Information section for more information.

RT (Pin 13/Pin 13): Timing Resistor Pin. Adjusts the switching frequency. Place a resistor from this pin to ground to set the frequency. Do not float this pin.

SYNC (Pin 14/Pin 14): To synchronize the switching frequency to an outside clock, simply drive this pin with a clock. The high voltage level of the clock needs to exceed 1.3V, and the low level should be less than 0.5V. Drive this pin to less than 0.5V to revert to the internal free-running clock. See the Applications Information section for more information.

BG1, BG2 (Pin 16/Pin 20, Pin 18/Pin 22): Bottom Gate Drive. Drives the gate of the bottom N-channel MOSFETs between ground and $GATEV_{CC}$.

$GATEV_{CC}$ (Pin 17/Pin 21): Power supply for bottom gate drivers. Must be connected to the $INTV_{CC}$ pin. Do not power from any other supply. Locally bypass to GND.

BOOST1, BOOST2 (Pin 24/Pin 35, Pin 19/Pin 24): Boosted Floating Driver Supply. The (+) terminal of the bootstrap capacitor connects here. The BOOST1 pin swings from a diode voltage below $GATEV_{CC}$ up to V_{IN} + $GATEV_{CC}$. The BOOST2 pin swings from a diode voltage below $GATEV_{CC}$ up to V_{OUT} + $GATEV_{CC}$.

TG1, TG2 (Pin 23/Pin 34, Pin 20/Pin 25): Top Gate Drive. Drives the top N-channel MOSFETs with voltage swings equal to $GATEV_{CC}$ superimposed on the switch node voltages.

SW1, SW2 (Pin 22/Pin 33, Pin 21/Pin 26): Switch Nodes. The (–) terminals of the bootstrap capacitors connect here.

PIN FUNCTIONS (QFN/eLQFP)

$\overline{\text{RVSOFF}}$ (Pin 25/Pin 37): Reverse Conduction Disable Pin. This is an input/output open-drain pin that requires a pull up resistor. Pulling this pin low disables reverse current operation. See the Uni and Bidirectional Conduction section for more information.

VOUTLOMON (Pin 26/Pin 38): V_{OUT} Low Voltage Monitor Pin. Connect a ±1% resistor divider between V_{OUT}, VOUTLOMON and GND to set an undervoltage level on V_{OUT}. When V_{OUT} is lower than this level, reverse conduction is disabled to prevent drawing current from V_{OUT}. See the Applications Information section for more information.

VINHIMON (Pin 27/Pin 39): V_{IN} High Voltage Monitor Pin. Connect a ±1% resistor divider between V_{IN}, VINHIMON and GND in order to set an overvoltage level on V_{IN}. When V_{IN} is higher than this level, reverse conduction is disabled to prevent current flow into V_{IN}. See the Applications Information section for more information.

ICP (Pin 28/Pin 40): Positive V_{OUT} Current Monitor Pin. The current out of this pin is 20µA plus a current proportional to the positive average V_{OUT} current. See the Applications Information section for more information.

$EXTV_{CC}$ (Pin 29/Pin 42): External V_{CC} Input. When $EXTV_{CC}$ exceeds 6.4V (typical), $INTV_{CC}$ will be powered from this pin. When $EXTV_{CC}$ is lower than 6.4V, the $INTV_{CC}$ will be powered from V_{INCHIP}.

CSPOUT (Pin 30/Pin 46): The (+) Input to the V_{OUT} Current Monitor Amplifier. This pin and the CSNOUT pin measure the voltage across the sense resistor, R_{SENSE2}, to provide the V_{OUT} current signals. Connect this pin to V_{OUT} when not in use. See Applications Information section for proper use of this pin.

CSNOUT (Pin 31/Pin 47): The (–) Input to the V_{OUT} Current Monitor Amplifier. Connect this pin to V_{OUT} when not in use. See Applications Information section for proper use of this pin.

CSNIN (Pin 32/Pin 52): The (–) Input to the V_{IN} Current Monitor Amplifier. This pin and the CSPIN pin measure the voltage across the sense resistor, R_{SENSE1}, to provide the V_{IN} current signals. Connect this pin to V_{IN} when not in use. See Applications Information section for proper use of this pin.

CSPIN (Pin 33/Pin 53): The (+) Input to the V_{IN} Current Monitor Amplifier. Connect this pin to V_{IN} when not in use. See Applications Information section for proper use of this pin.

V_{INCHIP} (Pin 34/Pin 55): Main Input Supply Pin for the LT8708. It must be locally bypassed to ground.

$INTV_{CC}$ (Pin 35/Pin 57): 6.3V Regulator Output. Must be connected to the $GATEV_{CC}$ pin. $INTV_{CC}$ is powered from $EXTV_{CC}$ when the $EXTV_{CC}$ voltage is higher than 6.4V, otherwise $INTV_{CC}$ is powered from V_{INCHIP}. Bypass this pin to ground with a minimum 4.7µF ceramic capacitor.

SWEN (Pin 36/Pin 58): Switching Regulator Enable Pin. Tie high through a resistor to enable the switching. Ground to disable switching. This pin is pulled down during shutdown, a thermal lockout or when an internal UVLO (undervoltage lockout) is detected. Don't float this pin. See the Start-Up: SWEN Pin section for more details.

MODE (Pin 37/Pin 59): Conduction Mode Select Pin. The voltage applied to this pin sets the conduction mode of the controller. Apply less than 0.4V to enable continuous conduction mode (CCM). Apply 0.8V to 1.2V to enable the hybrid conduction mode (HCM). Apply 1.6V to 2.0V to enable the discontinuous conduction mode (DCM). Apply more than 2.4V to enable Burst Mode operation.

IMON_OP (Pin 38/Pin 60): Positive V_{OUT} Current Monitor and Limit Pin. The current out of this pin is 20µA plus a current proportional to the positive average V_{OUT} current. IMON_OP also connects to error amplifier EA6 and can be used to limit the maximum positive V_{OUT} current. See the Applications Information section for more information.

IMON_ON (Pin 39/Pin 61): Negative V_{OUT} Current Monitor and Limit Pin. The current out of this pin is 20µA plus a current proportional to the negative average V_{OUT} current. IMON_ON also connects to error amplifier EA2 and can be used to limit the maximum negative V_{OUT} current. See the Applications Information section for more information.

LDO33 (Pin 40/Pin 62): 3.3V Regulator Output. Bypass this pin to ground with a minimum 0.1µF ceramic capacitor.

GND (Pin 15/Pin 19, Exposed Pad Pin 41/Pin 65): Ground. Tie directly to local ground plane.

BLOCK DIAGRAM

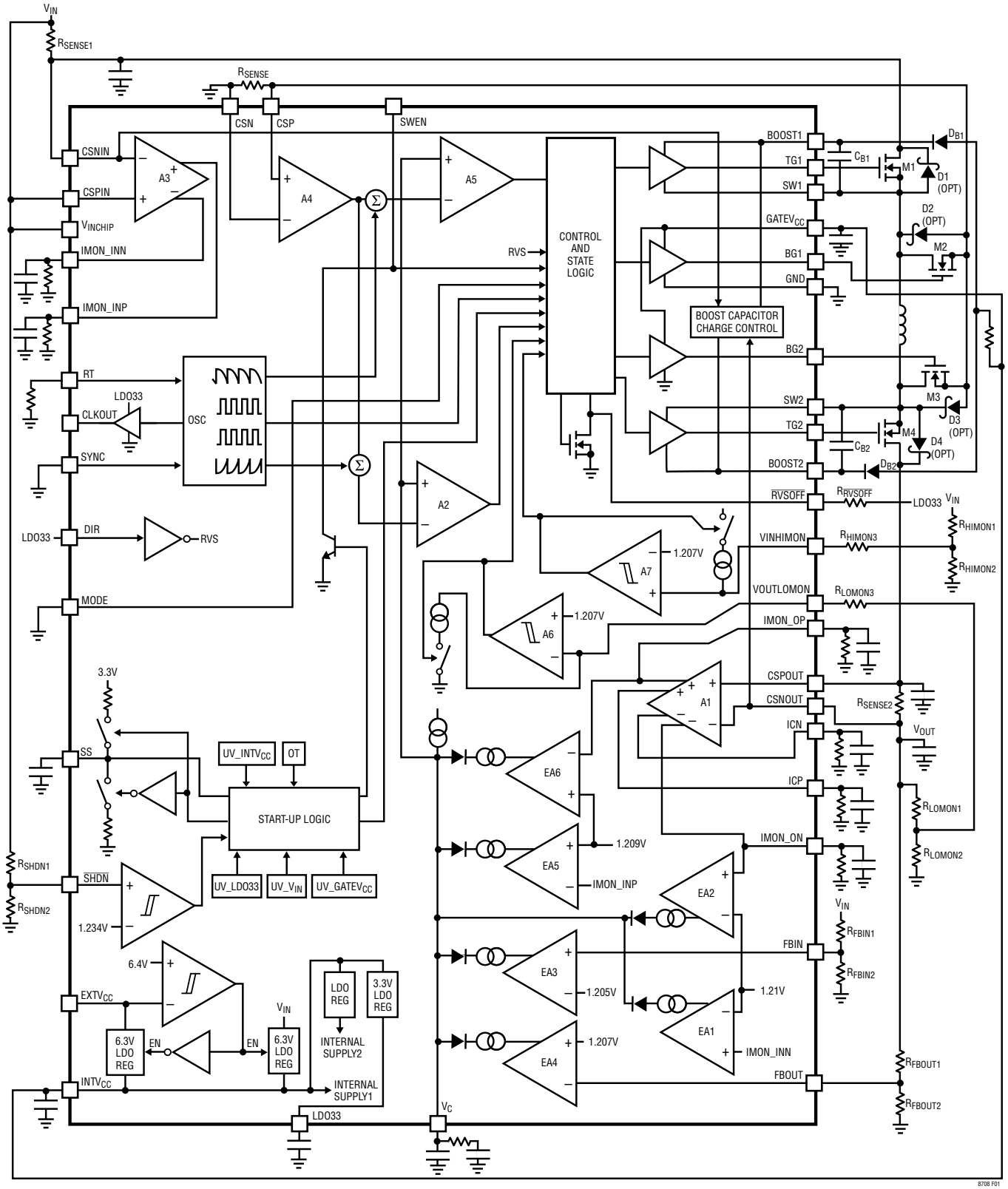


Figure 1. Block Diagram

OPERATION

TYPOGRAPHICAL CONVENTIONS

The LT8708 is a high performance 4-switch buck-boost controller that includes features to facilitate bidirectional current and power flow. Using the LT8708, an application can command power to be delivered from V_{IN} to V_{OUT} or from V_{OUT} to V_{IN} as needed. Some terms, listed below, are used throughout this data sheet in reference to the direction of current and power flow. In order to clarify these direction-based concepts, these terms are defined as follows:

V_{IN} and I_{IN}: The V_{IN} side of circuits drawn in this data sheet will always be on the left. V_{IN} is connected to the SW1 side of the buck-boost inductor through M1. I_{IN} is the V_{IN} current.

V_{OUT} and I_{OUT}: The V_{OUT} side of circuits drawn in this data sheet will always be on the right. V_{OUT} is connected to the SW2 side of the buck-boost inductor through M4. I_{OUT} is the V_{OUT} current.

Supply (Input): Power Source. The power source is most commonly applied to V_{IN}. However, V_{OUT} can be a Supply (or Input) when power is being delivered from V_{OUT} to V_{IN}.

Load (Output): Devices that are consuming the power. The Load is most commonly connected to V_{OUT}. However, V_{IN} can connect to the Load (or Output) when power is being delivered from V_{OUT} to V_{IN}.

Forward Conduction: Current or power flowing from the V_{IN} or SW1 node (or side) to the V_{OUT} or SW2 node (or side) of the circuit. This is generally left to right on schematics.

Reverse Conduction: Current or power flowing from the V_{OUT} or SW2 node (or side) to the V_{IN} or SW1 node (or side) of the circuit. This is general right to left on schematics.

Positive Current: Current that flows from the SW1 side of the buck-boost inductor to the SW2 side. Also refers to current that flows from V_{IN} and/or into V_{OUT}.

Reverse Current: Current that flows from the SW2 side of the buck-boost inductor to the SW1 side. Also refers to current that flows from V_{OUT} and/or into V_{IN}.

Refer to the Block Diagram (Figure 1) when reading the following sections about the operation of the LT8708.

START-UP

Figure 2 illustrates the start-up sequence for the LT8708.

Start-Up: $\overline{SHDN}$ Pin

The master shutdown pin for the chip is $\overline{SHDN}$. When driven below 0.35V (LT8708E, LT8708I) or 0.3V (LT8708H), the chip is disabled (CHIP OFF state) and quiescent current is minimal. Increasing the $\overline{SHDN}$ voltage can increase quiescent current but will not enable the chip until $\overline{SHDN}$ is driven above 1.221V (typical) after which the $INTV_{CC}$ and LDO33 regulators are enabled (SWITCHER OFF 1 state). External devices powered by LDO33 can become active at this time if enough voltage is available on V_{INCHIP} or $EXTV_{CC}$ to raise $INTV_{CC}$, and thus LDO33, to an adequate voltage.

Start-Up: SWEN Pin

The SWEN pin is used to enable the switching regulator after the chip has also been enabled by driving $\overline{SHDN}$ high. SWEN must be pulled high through a resistor to enable the switching regulator. The typical activation threshold is 1.208V as shown in the Electrical Characteristics section. When the SWEN pin voltage is below the activation threshold, the CSP-CSN, CSPIN-CSNIN and CSPOUT-CSNOUT current sense circuits on the chip are disabled.

SWEN has an internal pull-down that is activated when the switching regulator is unable to operate (see CHIP OFF and SWITCHER OFF 1 states in Figure 2). After the chip is able to operate and SWEN is internally pulled down below 0.8V (typical), the internal SWEN pull-down is disabled and start-up can proceed past the SWITCHER OFF1 state.

LDO33 or $INTV_{CC}$ are convenient nodes to pull SWEN up to. Choose a pull-up resistor value that limits the current to less than 200µA when SWEN is pulled low. The SWEN pin can also be digitally driven through a current limiting resistor. Note in the Electrical Characteristics section, the SWEN output low voltage is 0.9V (typical) when $\overline{SHDN}$ is low and/or V_{INCHIP} is unpowered. The SWEN output low is 0.2V when $\overline{SHDN}$ is 3V and V_{INCHIP} is powered.

OPERATION

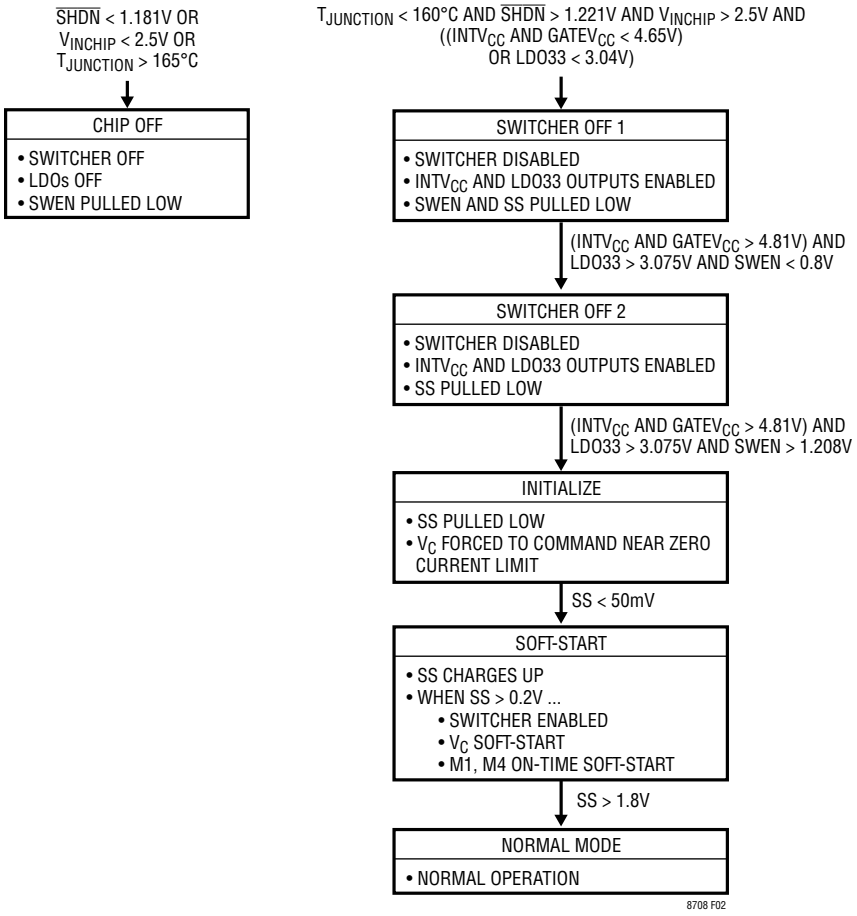


Figure 2. Start-Up Sequence (All Values are Typical)

Start-Up: Soft-Start of Switching Regulator

In the INITIALIZE state, the SS (soft-start) pin is pulled low to prepare for soft-starting the switching regulator. After SS has been discharged to less than 50mV, the SOFT-START state begins. In this state, as SS gradually rises, the soft-start circuitry provides a gradual ramp of V_C and the inductor current in the appropriate direction (refer to the V_C vs SS Voltage graph in the Typical Performance Characteristics section). This prevents abrupt surges of inductor current and helps the output voltage ramp smoothly into regulation. See the Switch Control: Soft-Start section for information about the power switch control during soft-start.

During soft-start, an integrated 180k (typical) resistor pulls SS up to 3.3V. The rising ramp rate of the SS pin voltage is set by this 180k resistor and the external capacitor connected to this pin. When SS reaches 1.8V (typical), the LT8708 exits soft-start and enters normal operation. Typical values for the external soft-start capacitor range from 220nF to 2µF. A minimum of 220nF is recommended.

CONTROL OVERVIEW

The LT8708 is a current mode controller that provides an output voltage above, below or equal to the input voltage. It also provides bidirectional current monitoring and regulation capabilities at both the input and the output.

The ADI proprietary control architecture employs an inductor current-sensing resistor (R_{SENSE}) in buck, boost or buck-boost regions of operation. The inductor current is controlled by the voltage on the V_C pin, which is the combined output of six internal error amplifiers EA1 – EA6.

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These amplifiers can be used to limit or regulate their respective voltages or currents as shown in Table 1.

Table 1. Error Amplifiers (EA1 – EA6)

AMPLIFIER NAME	PIN NAME	USED TO LIMIT OR REGULATE
EA1	IMON_INN	Negative I_{IN}
EA2	IMON_ON	Negative I_{OUT}
EA3	FBIN	V_{IN} Voltage
EA4	FBOUT	V_{OUT} Voltage
EA5	IMON_INP	Positive I_{IN}
EA6	IMON_OP	Positive I_{OUT}

The V_C voltage typically has a min-max range of about 1.2V. The maximum V_C voltage commands the most positive inductor current and, thus, commands the most power flow from V_{IN} to V_{OUT}. The minimum V_C voltage commands the most negative inductor current and, thus, commands the most power flow from V_{OUT} to V_{IN}.

In a simple example of V_{OUT} regulation, the FBOUT pin receives the V_{OUT} voltage feedback signal which is compared to the internal reference voltage using EA4. Low V_{OUT} voltage raises V_C and, thus, more current flows into V_{OUT}. Conversely, higher V_{OUT} reduces V_C, thus, reducing the current into V_{OUT} or even drawing current and power from V_{OUT}.

Note that the current and power flow can also be restricted to one direction, as needed, by the selected conduction mode discussed in the Uni and Bidirectional Conduction section.

As mentioned previously, the LT8708 also provides bidirectional current regulation capabilities at both the input and the output. The V_{OUT} current can be regulated or limited in the forward and reverse directions (EA6 and EA2, respectively). The V_{IN} current can also be regulated or limited in the forward direction and reverse directions (EA5 and EA1, respectively).

In a common application, V_{OUT} might be regulated using EA4, while the remaining error amplifiers are monitoring for excessive input or output current or an input undervoltage condition. In other applications, such as a battery backup system, a battery connected to V_{OUT} might be charged with constant current (EA6) to a maximum voltage (EA4) and also reversed, at times, to supply power back to V_{IN} using the other error amplifiers to regulate V_{IN} and limit the maximum current.

POWER SWITCH CONTROL

The following discussions about the power switch control assume that the LT8708 is operating in the continuous conduction mode (see Bidirectional Conduction: CCM). Other conduction modes have slight differences that are discussed later in their respective Conduction sections.

Figure 3 shows a simplified diagram of how the four power switches are connected to the inductor, V_{IN}, V_{OUT} and ground. Figure 4 shows the regions of operation for the LT8708 as a function of $V_{OUT} – V_{IN}$ or switch duty cycle (DC). The power switches are properly controlled so the transfer between modes is continuous.

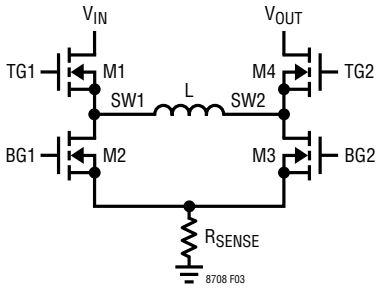


Figure 3. Simplified Diagram of the Buck-Boost Switches

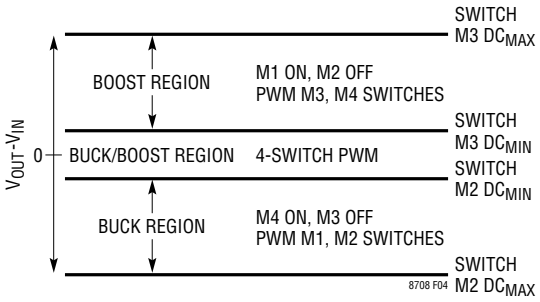


Figure 4. Operating Regions vs $V_{OUT} – V_{IN}$

OPERATION

Switch Control: Buck Region (V_{IN} >> V_{OUT})

When V_{IN} is significantly higher than V_{OUT}, the part will run in the buck region. In this region M3 is always off and switch M4 is always on. At the start of every cycle, synchronous switch M2 is turned on first. Inductor current is sensed by amplifier A4 while switch M2 is on. A slope compensation ramp is added to the sensed voltage which is then compared by A5 to a reference that is proportional to V_C. After the sensed inductor current falls below the reference, switch M2 is turned off and switch M1 is turned on for the remainder of the cycle. Switches M1 and M2 will alternate, behaving like a typical synchronous buck regulator. Figure 5 shows the switching waveforms in the buck region.

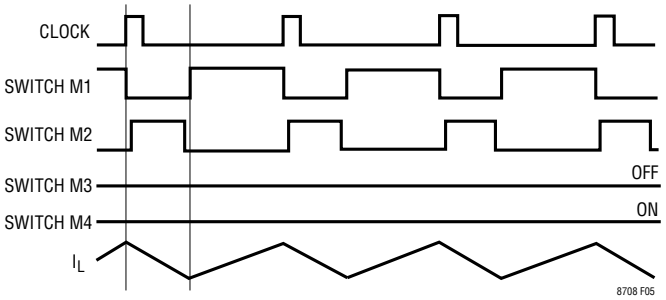


Figure 5. Buck Region (V_{IN} >> V_{OUT})

The part will continue operating in the buck region over a range of switch M2 duty cycles. The duty cycle of switch M2 in the buck region is given by:

$$DC_{(M2,BUCK)} = \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \bullet 100\%$$

As V_{IN} and V_{OUT} get closer to each other, the duty cycle decreases until the minimum duty cycle of the converter, in the buck region, reaches $DC_{(ABSMIN,M2,BUCK)}$. If the duty cycle becomes lower than $DC_{(ABSMIN,M2,BUCK)}$ the part will move to the buck-boost region.

$$DC_{(ABSMIN,M2,BUCK)} \cong t_{ON(M2,MIN)} \bullet f \bullet 100\%$$

where:

$t_{ON(M2,MIN)}$ is the minimum on-time for the synchronous switch in buck operation (200ns typical, see Electrical Characteristics).

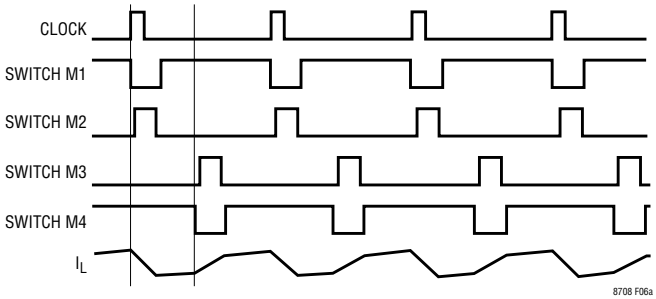
f is the switching frequency.

When V_{IN} is much higher than V_{OUT}, the duty cycle of switch M2 will increase, causing the M2 switch off-time to decrease. The M2 switch off-time should be kept above 230ns (typical, see Electrical Characteristics) to maintain steady-state operation and avoid duty cycle jitter, increased output ripple and reduction in maximum output current.

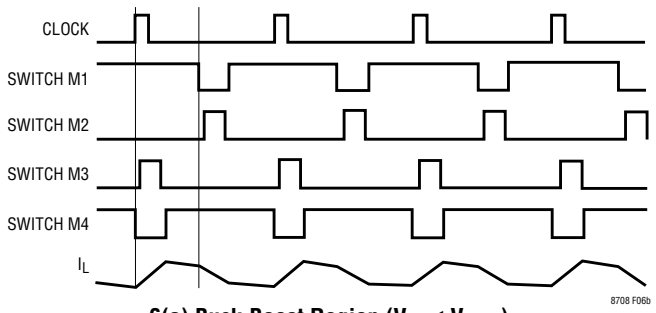
Switch Control: Buck-Boost (V_{IN} ≅ V_{OUT})

When V_{IN} is close to V_{OUT}, the controller operates in the buck-boost region. Figure 6 shows typical waveforms in this region. Every cycle, if the controller starts with switches M2 and M4 turned on, the controller first operates as if in the buck region. When A5 trips, switch M2 is turned off and M1 is turned on until the middle of the clock cycle. Next, switch M4 turns off and M3 turns on. The LT8708 then operates as if in boost mode until A2 trips. Finally, switch M3 turns off and M4 turns on until the end of the cycle.

If the controller starts with switches M1 and M3 turned on, the controller first operates as if in the boost region. When A2 trips, switch M3 is turned off and M4 is turned on until the middle of the clock cycle. Next, switch M1



6(a) Buck-Boost Region (V_{IN} ≥ V_{OUT})



6(a) Buck-Boost Region (V_{IN} ≤ V_{OUT})

Figure 6. Buck-Boost Region

OPERATION

turns off and M2 turns on. The LT8708 then operates as if in buck mode until A5 trips. Finally, switch M2 turns off and M1 turns on until the end of the cycle.

Switch Control: Boost Region (V_{IN} << V_{OUT})

When V_{OUT} is significantly higher than V_{IN}, the part operates in the boost region. In this region switch M1 is always on and switch M2 is always off. At the start of every cycle, switch M3 is turned on first. Inductor current is sensed by amplifier A4 while switch M3 is on. A slope compensation ramp is added to the sensed voltage which is then compared (A2) to a reference that is proportional to V_C. After the sensed inductor current rises above the reference voltage, switch M3 is turned off and switch M4 is turned on for the remainder of the cycle. Switches M3 and M4 will alternate, behaving like a typical synchronous boost regulator.

The part will continue operating in the boost region over a range of switch M3 duty cycles. The duty cycle of switch M3 in the boost region is given by:

$$DC_{(M3,BOOST)} = \left(1 - \frac{V_{IN}}{V_{OUT}}\right) \bullet 100\%$$

As V_{IN} and V_{OUT} get closer to each other, the duty cycle decreases until the minimum duty cycle of the converter, in the boost region, reaches $DC_{(ABSMIN,M3,BOOST)}$. If the duty cycle becomes lower than $DC_{(ABSMIN,M3,BOOST)}$, the part will move to the buck-boost region.

$$DC_{(ABSMIN,M3,BOOST)} \cong t_{ON(M3,MIN)} \bullet f \bullet 100\%$$

where:

$t_{ON(M3,MIN)}$ is the minimum on-time for the main switch in boost operation (200ns typical, see Electrical Characteristics).

f is the switching frequency.

When V_{OUT} is much higher than V_{IN}, the duty cycle of switch M3 will increase, causing the M3 switch off-time to decrease. The M3 switch off-time should be kept above 230ns (typical, see Electrical Characteristics) to maintain steady-state operation and avoid duty cycle jitter, increased output ripple and reduction in maximum output current.

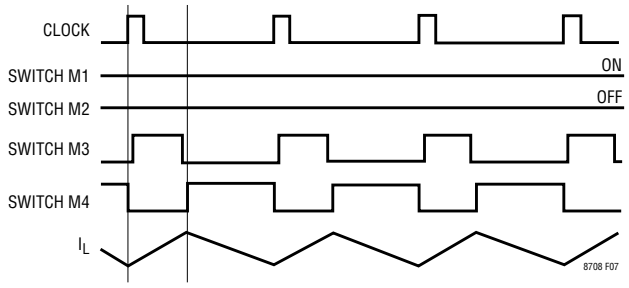


Figure 7. Boost Region (V_{IN} << V_{OUT})

Switch Control: Soft-Start

During soft-start, the LT8708 operates in the same three regions discussed above (buck, buck-boost and boost). However, a few differences in switch control happen during soft-start.

First, M1 and M4 are not turned on simultaneously while SS ramps up to 0.8V (typical). When M1 and M4 would normally both be on, they are instead turned off, leaving all four switches off. After SS rises above 0.8V, during the time when M1 and M4 would normally both be on, they are turned on briefly instead. This brief amount of time increases as SS rises until M1 & M4 are allowed to remain on as long as the normal switching sequence requires.

Second, M2 and M3 will occasionally turn on together for one cycle to refresh both boost capacitors. This refresh cycle happens because M1 and M4 switch more frequently during soft-start than in normal operation. As such, the Boost Capacitor Charge Control block (see Figure 1) cannot always keep the boost capacitors charged. M2 and M3 are turned on when either BOOSTx-SWx voltage drops below 5V (typical). Note that during the refresh cycle, the inductor current slope is nearly zero, thus the boost capacitors can be refreshed without much disturbance to the ongoing switching operations.

UNI AND BIDIRECTIONAL CONDUCTION

The LT8708 has one bidirectional and three unidirectional current conduction modes, primarily selected by the MODE pin. The bidirectional mode (CCM: continuous conduction mode) allows current and power to flow from V_{IN} to V_{OUT}, or vice versa, under control of the V_C pin. The unidirectional modes (DCM: discontinuous

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conduction mode, HCM: hybrid current mode and Burst Mode operation) only allow current and power to flow in one direction. Unidirectional settings override the V_C pin's attempt to direct current and power opposite to the selected direction.

The DIR pin selects the allowed power direction when using the DCM and HCM unidirectional modes. The Burst Mode operation only operates in the forward direction and is not affected by the DIR pin. In DCM and HCM modes, driving DIR > 1.6V (typical) selects forward operation which only allows power flow from V_{IN} to V_{OUT}. Driving DIR < 1.2V (typical) selects reverse operation which only allows power flow from V_{OUT} to V_{IN}.

Next, a low state on the $\overline{\text{RVSOFF}}$ pin inhibits reverse current and power flow. $\overline{\text{RVSOFF}}$ is an open-drain pin that requires a pull-up resistor. LDO33 or $INTV_{CC}$ are convenient nodes to pull $\overline{\text{RVSOFF}}$ up to. Normally, $\overline{\text{RVSOFF}}$ is only pulled low in response to a low V_{OUT} voltage (via the VOUTLOMON comparator) or a high V_{IN} voltage (via the VINHIMON comparator). However, external devices are permitted to pull $\overline{\text{RVSOFF}}$ low as needed. More information is available in the VINHIMON, VOUTLOMON and $\overline{\text{RVSOFF}}$ section.

Table 2 summarizes selection of the various conduction modes. See the Electrical Characteristics for the voltage thresholds of the DIR, VINHIMON, VOUTLOMON and $\overline{\text{RVSOFF}}$ pins.

Table 2. Conduction Configurations

MODE PIN	DIR PIN STATE	$\overline{\text{RVSOFF}}$ PIN STATE	CONDUCTION MODE	POSSIBLE DIRECTION
<0.4V	–	Hi	CCM	Forward and Reverse
		Lo	DCM	Forward
0.8V to 1.2V	Hi	–	HCM	Forward
	Lo	Hi		Reverse
		Lo	–	None
1.6V to 2.0V	Hi	–	DCM	Forward
	Lo	Hi		Reverse
		Lo	–	None
>2.4V	–	Hi	Burst Mode Operation	Forward
		Lo	–	None

The conduction configuration can be changed during operation, as needed, with the following restrictions:

1. Before transitioning from MODE = Burst Mode operation to MODE = CCM, the DIR pin must be driven to the Hi (Forward) state.
2. Avoid control pulses on the MODE and DIR pins narrower than 15 LT8708 clock cycles.

   Note: The V_C pin may be railed at the moment the DIR pin or MODE pin changes state. The railed V_C voltage corresponds to zero current in one direction and maximum current in the other. Therefore, if a small value R_{SENSE} resistor is used, the chip may momentarily command high inductor current immediately after the DIR or MODE pin change. An undersized inductor may become saturated in this case. An edge detector on the DIR and/or MODE pin can be used to reset the chip, forcing a soft-start and limiting the initial current. See the 48V to 14V Bidirectional Dual Battery System with FHCM & RHCM in the Typical Applications section as an example.

More details about each of the four conduction modes are provided in the following sub-sections.

Bidirectional Conduction: CCM

The continuous conduction mode allows the inductor current to flow in the forward or reverse direction, depending on the V_C voltage. When CCM is selected, high V_C voltage causes current and power to flow from V_{IN} to V_{OUT} and low V_C voltage causes current and power to flow from V_{OUT} to V_{IN}. At very light load currents the inductor current may ripple positive and negative as the appropriate average current is delivered to the appropriate output.

Unidirectional Conduction: DCM

The discontinuous conduction mode restricts the inductor current so that it can only flow in one direction, positive towards V_{OUT} (Forward DCM) or negative towards V_{IN} (Reverse DCM). The forward/reverse selection is made by driving the DIR pin as desired.

When FDCM is selected, higher V_C voltage increases the power flowing from V_{IN} to V_{OUT}. Lower V_C voltage reduces or stops the flow. When RDCM is selected, lower

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V_C voltage increases the power flowing from V_{OUT} into V_{IN}. Higher V_C voltage reduces or stops the flow.

Forward (or reverse) DCM affects the power switches as follows. Under light loading conditions, in FDCM (or RDCM), synchronous switch M4 (or M1) is turned off whenever instantaneous reverse (or forward) current in the inductor is detected. This is to prevent drawing current from V_{OUT} (or V_{IN}) and feeding current into V_{IN} (or V_{OUT}). Under very light loads, the current comparator may also remain tripped for several cycles and force switches M1 (or M2) and M3 (or M4) to stay off for the same number of cycles i.e., skipping pulses. Synchronous switch M2 (or M3) will remain on during the skipped cycles, but since switch M4 (or M1) is off, the inductor current will not reverse directions.

Unidirectional Conduction: HCM

Large inductor current ripple can sometimes result in high power dissipation of the M4 (or M1) junction diode during the FDCM (or RDCM) operation described above. This can happen, for example, when $V_{IN} >> V_{OUT}$ and the average V_{OUT} current is relatively high, but M4 is turned off to block negative components of the AC inductor current. The hybrid current mode (or HCM) is an alternative to DCM that often reduces the maximum M4 (or M1) heating in such cases.

The hybrid current mode is a mixture of the light load DCM operation and CCM operation, but only allows average current flow in one direction. As such, it is possible to have the lower portions of the inductor current ripple flow opposite to the selected direction while the average current remains in the selected direction. The DIR pin is used to select the desired forward (or FHCM) or reverse (or RHCM) direction of average current flow.

HCM works by measuring the average forward V_{OUT} current and the average reverse V_{IN} current indicated on ICN and IMON_INP, respectively. In FHCM (or RHCM), light load is detected when ICN (or IMON_INP) is above 255mV (typical). As a result, M4 (or M1) is turned off to prevent average current flow opposite to the desired direction. Heavy load is detected when ICN (or IMON_INP) is below 205mV (typical). As a result, CCM operation is enabled, allowing M4 (or M1) to turn on and reduce the diode's power dissipation.

NOTE: In FHCM operation connect a 17.4k resistor from ground to the ICN pin, and in RHCM operation, connect a 17.4k resistor from ground to the IMON_INP pin.

Unidirectional Conduction: Burst Mode

In Burst Mode operation, a V_C voltage is set, with about 25mV of hysteresis, below which switching activity is inhibited and above which switching activity is re-enabled. A typical example is when, at light output currents, V_{OUT} rises and forces the V_C pin below the threshold that temporarily inhibits switching. After V_{OUT} drops slightly and V_C rises ~25mV, the switching is resumed, initially in the buck-boost region. Burst Mode operation can increase efficiency at light load currents by eliminating unnecessary switching activity and related power losses. In Burst Mode operation, inductor current is only allowed in the forward direction, regardless of the voltage on the DIR pin. Burst Mode operation handles reverse-current detection similar to forward DCM. The M4 switch is turned off when reverse inductor current is detected.

ERROR AMPLIFIERS

The six internal error amplifiers combine to drive V_C according to Table 3, with the highest priority being at the top.

Table 3. Error Amp Priorities

TYPICAL CONDITION			PURPOSE
if	IMON_INN > 1.21V or	then V_C Rises	to Reduce Negative I_{IN}
	IMON_ON > 1.21V		to Reduce Negative I_{OUT}
else if	FBIN < 1.205V or	then V_C Falls	to Reduce Positive I_{IN} or Increase Negative I_{IN}
	FBOUT > 1.207V or		to Reduce Positive I_{OUT} or Increase Negative I_{OUT}
	IMON_INP > 1.209V or		to Reduce Positive I_{IN}
	IMON_OP > 1.209V		to Reduce Positive I_{OUT}
else		V_C Rises	Default

Note that certain error amplifiers are disabled under the conditions shown in Table 4. A disabled error amplifier is unable to affect V_C and can be treated as if its associated row is removed from Table 3.

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Table 4. Automatically Disabled Error Amp Conditions

ERROR AMP	PIN NAME	VOUTLOMON ASSERTED	VINHIMON ASSERTED	RDCM or RHCM	
				–	$\overline{\text{RVSOFF}}$ <1.207V
EA1	IMON_INN				4*
EA2	IMON_ON				4*
EA3	FBIN		2*		4*
EA4	FBOUT	1*		3*	4*
EA5	IMON_INP				4*
EA6	IMON_OP				4*

A 1* – 4* indicates that the error amplifier listed for that row is disabled under that column's condition. The purposes of disabling the respective amplifiers are listed below.

1* This improves transient response when VOUTLOMON deasserts.

2* This improves transient response when VINHIMON deasserts.

3* Since power can only transfer from V_{OUT} to V_{IN}, this prevents higher FBOUT/V_{OUT} voltages from interfering with the FBIN/V_{IN} voltage regulation.

4* No switching occurs in this condition. Disabling the error amplifiers improves transient response when resuming switching operation.

Some applications don't require the use of all six error amplifiers. When unused, the respective input pin(s) should be driven so that they don't interfere with the operation of the remaining amplifiers. Use Table 5 as a guide.

Table 5. Disabling Unused Amplifiers

AMPLIFIER NAME	PIN NAME	TIE TO DISABLE	EXAMPLE DISABLED PIN CONNECTION
EA1	IMON_INN	< 0.9V	GND
EA2	IMON_ON		
EA3	FBIN	> 1.5V	LDO33
EA4	FBOUT	< 0.9V	GND
EA5	IMON_INP		
EA6	IMON_OP		

V_{OUT} REGULATION AND SENSING

Two pins, FBOUT and VOUTLOMON, are provided to sense the V_{OUT} voltage and issue the appropriate response to the switching regulator.

V_{OUT}: Regulation

V_{OUT} is regulated, subject to the priorities in Table 3, using a resistor divider between V_{OUT}, FBOUT and ground. FBOUT connects to the EA4 amplifier to drive V_C. When FBOUT rises near or above the EA4 reference (1.207V typical), V_C typically falls, commanding less current into V_{OUT}. The V_{OUT} regulation voltage is given by the equation:

$$V_{OUT} = 1.207V \bullet \left(1 + \frac{R_{FBOUT1}}{R_{FBOUT2}}\right)$$

where:

R_{FBOUT1} and R_{FBOUT2} are shown in Figure 1.

V_{OUT}: Above Regulation

When the FBOUT pin and EA4 detect that V_{OUT} is significantly above regulation, V_C typically falls to its minimum voltage. The LT8708 responds to the minimum V_C voltage according to the conduction mode enabled by MODE, DIR and $\overline{\text{RVSOFF}}$. If reverse conduction is not allowed (FDCM, FHCM and Burst Mode operation) then switching will stop and current won't be delivered to V_{IN}. If reverse conduction is allowed (CCM, RDCM and RHCM), then current and power will flow from V_{OUT} to V_{IN}.

V_{OUT}: Below Regulation and Undervoltage

When the FBOUT pin and EA4 detect V_{OUT} is below regulation, V_C typically rises. If forward conduction is enabled (CCM, FDCM, FHCM and Burst mode), then current and power will flow from V_{IN} to V_{OUT}.

A resistor divider between V_{OUT}, VOUTLOMON and ground is used to detect V_{OUT} undervoltage. This function prevents reverse conduction, from V_{OUT} to V_{IN}, from drawing V_{OUT} down lower than desired. When undervoltage is detected by VOUTLOMON, $\overline{\text{RVSOFF}}$ is pulled low to disable reverse current and power. This function can be used as a UVLO (undervoltage lockout), for example, when a battery or supercapacitor, connected to V_{OUT}, is supplying power to V_{IN}. See the VINHIMON, VOUTLOMON and $\overline{\text{RVSOFF}}$ section for more detailed information.

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V_{IN} REGULATION AND SENSING

Two pins, FBIN and VINHIMON, are provided to sense the V_{IN} voltage and issue the appropriate response to the switching regulator.

V_{IN}: Regulation

Subject to the priorities in Table 3, a resistor divider between V_{IN}, FBIN and ground can be used to regulate V_{IN} or serve an undervoltage lockout function. A few application examples are as follows:

- For V_{IN} supplies with high source impedance (i.e., a solar panel), V_{IN} regulation can prevent the supply voltage from dropping too low under high V_{OUT} load conditions.
- For V_{IN} supplies with low source impedance (i.e., batteries and voltage supplies), the FBIN pin can be used to stop switching activity when the V_{IN} supply voltage gets too low for proper system operation.
- V_{IN} can also be regulated to a maximum voltage when power is flowing from V_{OUT} to V_{IN}, such as in a battery backup application.

When FBIN falls near or below the EA3 reference (1.205V typical), the V_C voltage falls and reduces current draw from V_{IN}. The V_{IN} regulation voltage is given by the equation:

$$V_{IN} = 1.205V \bullet \left(1 + \frac{R_{FBIN1}}{R_{FBIN2}}\right)$$

where:

R_{FBIN1} and R_{FBIN2} are shown in Figure 1.

V_{IN}: Above Regulation and Overvoltage

When the FBIN pin and EA3 detect V_{IN} is above regulation, V_C is allowed to rise. If forward conduction is enabled (CCM, FDCM, FHCM and Burst Mode operation), then current and power can flow from V_{IN} to V_{OUT}. If only reverse conduction is enabled (RDCM and RHCM), then switching will stop and current won't be delivered into V_{IN}. NOTE: This above-regulation condition is required to allow forward conduction in an application.

A resistor divider between V_{IN}, VINHIMON and ground is used to detect V_{IN} overvoltage. This function prevents reverse conduction, from V_{OUT} to V_{IN}, from forcing V_{IN} higher than desired. When overvoltage is detected by VINHIMON, $\overline{RVSOFF}$ is pulled low to disable reverse current and power. This function can be used as an OVLO (over voltage lockout), for example, when a battery, connected to V_{IN}, is being charged from V_{OUT}. See the VINHIMON, VOUTLOMON and $\overline{RVSOFF}$ section for more detailed information.

V_{IN}: Below Regulation

When the FBIN pin and EA3 detect that V_{IN} is significantly below regulation, V_C may fall to its minimum voltage. The LT8708 responds to the minimum V_C voltage according to the conduction mode enabled by MODE, DIR and $\overline{RVSOFF}$. If only forward conduction is allowed (FDCM, FHCM and Burst Mode operation) then switching will stop and current won't be drawn from V_{OUT}. If reverse conduction is allowed (CCM, RDCM and RHCM), then current and power will flow from V_{OUT} to V_{IN}.

UVLO functions are available to detect low V_{IN} voltage. These functions are discussed in the Voltage Lockouts section.

CURRENT MONITORING AND LIMITING

Monitoring and Limiting: IMON Pins

The LT8708 can monitor V_{IN} and V_{OUT} current (I_{IN} and I_{OUT}) in both the positive and negative directions. The CSPIN and CSNIN pins connect across a current sense resistor to monitor I_{IN}. External resistors are connected from the IMON_INP and IMON_INN pins to GND. Their resulting voltages are linearly proportional to positive I_{IN} and negative I_{IN} respectively. See amplifier A3 in the Block Diagram.

Similarly, an I_{OUT} sense resistor, measured by CSPOUT and CSNOUT, is used to monitor the V_{OUT} current. External resistors are connected from the IMON_OP and IMON_ON pins to GND. Their resulting voltages are linearly proportional to positive I_{OUT} and negative I_{OUT} respectively. See amplifier A1 in the Block Diagram.

OPERATION

The I_{IN} and I_{OUT} currents can be limited and regulated to independent maximum positive values. When I_{IN} causes IMON_INP to rise near or above 1.209V (typical), EA5 typically causes V_C to pull down and limit/regulate the maximum current. Similarly, when I_{OUT} causes IMON_OP to rise near or above 1.209V (typical), EA6 typically causes V_C to pull down and limit/regulate the maximum current. See Table 3 for error amplifier priorities.

The I_{IN} and I_{OUT} currents can also be limited and regulated to independent maximum negative values. When I_{IN} causes IMON_INN to rise near or above 1.21V (typical), EA1 causes V_C to pull up and limit the maximum current. Similarly, when I_{OUT} causes IMON_ON to rise near or above 1.21V (typical), EA2 causes V_C to pull up and limit the maximum current.

The I_{IN} and I_{OUT} current limits can provide many benefits. They can be used to prevent overloading the input supply, allow for constant-current battery and supercapacitor charging and can also serve as short-circuit protection for constant-voltage regulators. See the Applications Information section for more information about the current monitors and the current regulation and limiting.

Monitoring: ICP and ICN Pins

ICP and ICN are additional current monitor pins with output currents typically equal to those of IMON_OP and IMON_ON, respectively.

In contrast to IMON_OP, ICP is internally pulled to ~0.6V (typical) when V_C is at its minimum and the conduction mode is either RDCM or RHCM. Also, in contrast to IMON_ON, ICN is internally pulled to ~0.6V (typical) when V_C is at its maximum and the conduction mode is FDCM, FHCM or Burst Mode operation.

Always connect a 17.4k resistor from ICP to ground and from ICN to ground.

$INTV_{CC}$/$EXTV_{CC}$/$GATEV_{CC}$/LDO33 POWER

Power for the top and bottom MOSFET drivers, the LDO33 pin and most internal circuitry is derived from the $INTV_{CC}$ pin. $INTV_{CC}$ is regulated to 6.3V (typical) from either the V_{INCHIP} or $EXTV_{CC}$ pin. When the $EXTV_{CC}$ pin is left open or tied to a voltage less than 6.2V (typical), an internal low dropout regulator regulates $INTV_{CC}$ from V_{INCHIP}. If $EXTV_{CC}$ is taken above 6.4V (typical), another low dropout regulator will instead regulate $INTV_{CC}$ from $EXTV_{CC}$. Regulating $INTV_{CC}$ from $EXTV_{CC}$ allows the power to be derived from the lowest supply voltage (highest efficiency) such as the LT8708 switching regulator output (see $INTV_{CC}$ Regulators and $EXTV_{CC}$ Connection in the Applications Information section for more details).

The $GATEV_{CC}$ pin directly powers the bottom MOSFET drivers for switches M2 and M3 (see Figure 3). $GATEV_{CC}$ should always be connected to $INTV_{CC}$ and should not be powered or connected to any other source. Undervoltage lockouts (UVLOs) monitoring $INTV_{CC}$ and $GATEV_{CC}$ disable the switching regulator when the pins are below 4.65V (typical).

The LDO33 pin can provide power to external components such as a microcontroller and/or can provide an accurate bias voltage. Load current is limited to 17.25mA (typical). As long as $\overline{SHDN}$ is high, the LDO33 output is linearly regulated from the $INTV_{CC}$ pin and is not affected by the $INTV_{CC}$ or $GATEV_{CC}$ UVLOs or the SWEN pin voltage. LDO33 remains regulated as long as $\overline{SHDN}$ is high and sufficient voltage is available on $INTV_{CC}$ (typically > 4.0V). An undervoltage lockout monitoring LDO33 will disable the switching regulator when LDO33 is below 3.04V (typical).

CLKOUT AND TEMPERATURE SENSING

The CLKOUT pin toggles at the LT8708's internal clock frequency whether the internal clock is synchronized to an external source or is free-running based on the external R_T resistor. The CLKOUT pin can be used to synchronize other devices to the LT8708's switching frequency. Also, the duty cycle of CLKOUT is proportional to the die temperature and can be used to monitor the die for thermal issues.

APPLICATIONS INFORMATION

This Applications Information section provides additional details for setting up an application using the LT8708. Topics include verifying the power flow conditions, selection of various external components including the switching MOSFETs, sensing resistors, filter capacitors, diodes and the primary inductor among others. In addition, more information is provided about voltage lockouts, current monitoring, PCB layout and efficiency considerations. This section wraps up with a design example to illustrate the use of the various design equations presented here.

VERIFY THE POWER FLOW CONDITIONS

Due to the configurability of the LT8708, a methodical approach should be used to verify that power will flow, as intended, under all relevant conditions. Table 6(a) and 6(b) are provided to help with this verification.

First, using Table 6(a), note which V_{IN} and V_{OUT} combinations are used in the application. For example, print a copy of Table 6(a) and highlight or circle the applicable cells.

In Table 6(a):

- V_{IN_FBIN} is the V_{IN} voltage when FBIN is at 1.205V (typ)
- V_{OUT_FBOUT} is the V_{OUT} voltage when FBOUT is at 1.207V (typ)
- $V_{IN\_VINHIMON}$ is the V_{IN} voltage when $V_{INHIMON}$ at 1.207V (typ)
- $V_{OUT\_VOUTLOMON}$ is the V_{OUT} voltage when $V_{OUTLOMON}$ is at 1.207V (typ)

If one or more of the FBIN, FBOUT, VINHIMON and VOUTLOMON pins are tied to their inactive states (see Table 5 and the VINHIMON, VOUTLOMON and $\overline{\text{RVSOFF}}$ section), the associated row(s) or column(s) will not apply to the application. For example, if FBIN is tied to LDO33 to deactivate that pin function, then the $V_{IN} < V_{IN\_FBIN}$ row of Table 6(a) is not applicable and no cells in that row should be circled.

Next, for each cell identified in Table 6(a), check that the operating condition described in Table 6(b) meets the application's requirements.

Table 6. Power Flow Verification Table

6(a)

V_{OUT}/V_{IN}	$V_{OUT} < V_{OUT\_VOUTLOMON}$	$V_{OUT} > V_{OUT\_VOUTLOMON}$ & $V_{OUT} < V_{OUT\_FBOUT}$	$V_{OUT} > V_{OUT\_FBOUT}$
$V_{IN} < V_{IN\_FBIN}$	No Power Transfer	B	B
$V_{IN} > V_{IN\_FBIN}$ & $V_{IN} < V_{IN\_VINHIMON}$	A	D	C
$V_{IN} > V_{IN\_VINHIMON}$	A	D	No Power Transfer

6(b)

<table>
<tr><th></th><th>MODE = BURST</th><th>MODE = CCM</th><th>MODE = DCM/HCM, DIR = FWD</th><th>MODE = DCM/HCM, DIR = RVS</th></tr>
<tr><td>A</td><td colspan="3">Power Flows from V_{IN} to V_{OUT}</td><td>No Power Flow</td></tr>
<tr><td>B</td><td rowspan="2">No Power Flow</td><td rowspan="2">Power Flows from V_{OUT} to V_{IN}</td><td rowspan="2">No Power Flow</td><td>Power Flows from V_{OUT} to V_{IN}</td></tr>
<tr><td>C</td><td rowspan="2">No Power Flow</td></tr>
<tr><td>D</td><td colspan="3">Power Flows from V_{IN} to V_{OUT}</td></tr>
</table>

Note: Table 6(a) and Table 6(b) assume that the $\overline{\text{RVSOFF}}$ pin is not driven low by an external device.

See the Design Example section for a further example of using these tables.

OPERATING FREQUENCY SELECTION

The LT8708 uses a constant frequency architecture between 100kHz and 400kHz. The frequency can be set using the internal oscillator or can be synchronized to an external clock source. Selection of the switching frequency is a trade-off between efficiency and component size. Low frequency operation increases efficiency by reducing MOSFET switching losses, but requires more inductance and/or capacitance to maintain low output ripple voltage. For high power applications, consider operating at lower frequencies to minimize MOSFET heating from switching losses. The switching frequency can be set by placing an appropriate resistor from the RT pin to ground and tying the SYNC pin low. The frequency can also be synchronized to an external clock source driven into the SYNC pin. The following sections provide more details.

APPLICATIONS INFORMATION

INTERNAL OSCILLATOR

The operating frequency of the LT8708 can be set using the internal free-running oscillator. When the SYNC pin is driven low (< 0.5V), the operating frequency is set by the value of the resistor from the RT pin to ground. An internally trimmed timing capacitor resides inside the IC. The oscillator frequency is calculated using the following formula:

$$f_{OSC} = \left(\frac{43{,}750}{R_T + 1} \right) kHz$$

where:

f_{OSC} is in kHz and R_T is in kΩ.

Conversely, R_T (in kΩ) can be calculated from the desired frequency (in kHz) using:

$$R_T = \left(\frac{43{,}750}{f_{OSC}} - 1 \right) k\Omega$$

SYNC PIN AND CLOCK SYNCHRONIZATION

The operating frequency of the LT8708 can be synchronized to an external clock source. To synchronize to the external source, simply provide a digital clock signal into the SYNC pin. The LT8708 will operate at the SYNC clock frequency.

The duty cycle of the SYNC signal must be between 20% and 80% for proper operation. Also, the frequency of the SYNC signal must meet the following two criteria:

1. SYNC may not toggle outside the frequency range of 100kHz to 400kHz unless it is stopped low to enable the free-running oscillator.
2. The SYNC pin frequency can always be higher than the free-running oscillator set frequency, f_{OSC}, but should not be less than 25% below f_{OSC}.

After SYNC begins toggling, it is recommended that switching activity is stopped before the SYNC pin stops toggling. Excess inductor current can result when SYNC stops toggling as the LT8708 transitions from the external SYNC clock source to the internal free-running oscillator clock. Switching activity can be stopped by driving either the SWEN or $\overline{SHDN}$ pin low.

CLKOUT PIN AND CLOCK SYNCHRONIZATION

The CLKOUT pin can drive up to 200pF and toggles at the LT8708's internal clock frequency whether the internal clock is synchronized to the SYNC pin or is free-running based on the external R_T resistor. The rising edge of CLKOUT is approximately 180° out of phase from the internal clock's rising edge or the SYNC pin's rising edge if it is toggling. CLKOUT starts toggling when the INITIALIZE state is entered (see Figure 2).

The CLKOUT pin can be used to synchronize other devices to the LT8708's switching frequency. For example, the CLKOUT pin can be tied to the SYNC pin of another LT8708 regulator which will operate approximately 180°out of phase of the master LT8708. The frequency of the master LT8708 can be set by the external R_T resistor or by toggling the SYNC pin. Note that the R_T pin of the slave LT8708 must have a resistor tied to ground. In general, use the same value R_T resistor for all of the synchronized LT8708s.

The duty cycle of CLKOUT is proportional to the die temperature and can be used to monitor the die for thermal issues. See the Junction Temperature Measurement section for more information.

INDUCTOR CURRENT SENSING AND SLOPE COMPENSATION

The LT8708 operates using inductor current mode control. As described previously in the Power Switch Control section, the LT8708 measures the peak of the inductor current waveform in the boost region and the valley of the inductor current waveform in the buck region. The inductor current is sensed across the R_{SENSE} resistor with pins CSP and CSN. During any given cycle, the peak (boost region) or valley (buck region) of the inductor current is controlled by the V_C pin voltage.

Slope compensation provides stability in constant-frequency current mode control architectures by preventing subharmonic oscillations at high duty cycles. This is accomplished internally by adding a compensating ramp to the inductor current signal in the boost region, or subtracting a ramp from the inductor current signal in the buck region. At higher duty cycles, this results in a reduction of maximum inductor current in the boost region, and an increase

APPLICATIONS INFORMATION

of the maximum inductor current in the buck region. For example, refer to the Maximum Inductor Current Sense Voltage vs Duty Cycle graph in the Typical Performance Characteristics section. The graph shows that, with V_C at its maximum voltage, the maximum peak inductor sense voltage V_{RSENSE} is between 47mV and 93mV depending on the duty cycle. It also shows that the maximum inductor valley current in the buck region is 82mV increasing to ~130mV at higher duty cycles.

R_{SENSE} SELECTION AND MAXIMUM CURRENT

The R_{SENSE} resistance must be chosen properly to achieve the desired amount of output current (forward conduction) and input current (reverse conduction). Too much resistance can limit the input/output current below the application requirements. Start by determining the maximum allowed R_{SENSE} resistances in the forward and reverse boost regions ($R_{SENSE(MAX,BOOST,FWD)}$ and $R_{SENSE(MAX,BOOST,RVS)}$). Follow this by finding the maximum allowed R_{SENSE} resistances in the forward and reverse buck regions ($R_{SENSE(MAX,BUCK,FWD)}$ and $R_{SENSE(MAX,BUCK,RVS)}$). The selected R_{SENSE} resistance must be less than all four values.

R_{SENSE} Selection: Max R_{SENSE} in the Boost Region

Forward Conduction: In this section $R_{SENSE(MAX,BOOST,FWD)}$ is calculated which is the maximum allowed R_{SENSE} resistance when operating in the boost region with forward conduction (V_{IN} to V_{OUT}). Skip this section and assume $R_{SENSE(MAX,BOOST,FWD)} = \infty$ when this operating condition does not apply to the application.

In the boost region, the maximum positive V_{OUT} current capability is the lowest when V_{IN} is at its minimum and V_{OUT} is at its maximum. Therefore, R_{SENSE} must be chosen to meet the output current requirements under these conditions.

Start by finding the maximum boost region duty cycle which occurs when V_{IN} is minimum and V_{OUT} is maximum using:

$$DC_{(MAX,M3,BOOST)} \cong \left(1-\frac{V_{IN(MIN,BOOST)}}{V_{OUT(MAX,BOOST)}}\right)\bullet 100\%$$

For example, an application with a V_{IN} range of 12V to 48V and V_{OUT} set to 36V will have:

$$DC_{(MAX,M3,BOOST)} \cong \left(1-\frac{12V}{36V}\right)\bullet 100\% = 67\%$$

Referring to the Maximum Inductor Current Sense Voltage graph in the Typical Performance Characteristics section, the maximum R_{SENSE} voltage at 67% duty cycle is 68mV, or:

$$V_{RSENSE(MAX,BOOST,MAXDC)} \cong 68mV$$

for V_{IN} = 12V, V_{OUT} = 36V.

Next, the inductor ripple current in the boost region must be determined. If the main inductor L is not known, the maximum ripple current $\Delta I_{L(MAX,BOOST)}$ can be estimated by choosing $\Delta I_{L(MAX,BOOST)}$ to be 30% to 50% of the maximum peak inductor current in the boost region as follows:

$$\Delta I_{L(MAX,BOOST)} \cong \frac{V_{OUT(MAX,BOOST)}\bullet I_{OUT(MAX,FWD)}}{V_{IN(MIN,BOOST)}\bullet\left(\frac{100\%}{\%Ripple}-0.5\right)} A$$

where:

$I_{OUT(MAX,FWD)}$ is the maximum V_{OUT} load current required in the boost region.

%Ripple is 30% to 50%

For example, using $V_{OUT(MAX)}$ = 36V, $V_{IN(MIN)}$ = 12V, $I_{OUT(MAX,FWD)}$ = 2A and %Ripple = 40% we can calculate:

$$\Delta I_{L(MAX,BOOST)} \cong \frac{36V\bullet 2A}{12V\bullet\left(\frac{100\%}{40\%}-0.5\right)} = 3A$$

APPLICATIONS INFORMATION

Otherwise, if the inductance is already known then $\Delta I_{L(MAX,BOOST,FWD)}$ can be more accurately calculated as follows:

$$\Delta I_{L(MAX,BOOST)} = \frac{\left(\frac{DC_{(MAX,M3,BOOST)}}{100\%}\right) \bullet V_{IN(MIN,BOOST)}}{f \bullet L} A$$

where:

$DC_{(MAX,M3,BOOST)}$ is the maximum duty cycle percentage in the boost region as calculated previously

f is the switching frequency

L is the inductance of the main inductor

After the maximum ripple current is known, the maximum allowed R_{SENSE} in the boost region while in forward conduction (V_{IN} to V_{OUT}) can be calculated as follows:

$$R_{SENSE(MAX,BOOST,FWD)} = \frac{2 \bullet V_{RSENSE(MAX,BOOST,MAXDC)} \bullet V_{IN(MIN,BOOST)}}{\left(2 \bullet I_{OUT(MAX,FWD)} \bullet V_{OUT(MAX,BOOST)}\right) + \left(\Delta I_{L(MAX,BOOST)} \bullet V_{IN(MIN,BOOST)}\right)} \Omega$$

where:

$V_{RSENSE(MAX,BOOST,MAXDC)}$ is the maximum inductor current sense voltage as discussed in the previous section.

Using values from the previous examples:

$$R_{SENSE(MAX,BOOST,FWD)} = \frac{2 \bullet 68mV \bullet 12V}{(2 \bullet 2A \bullet 36V) + (3A \bullet 12V)} = 9.1m\Omega$$

Reverse Conduction: In this section $R_{SENSE(MAX,BOOST,RVS)}$ is calculated which is the maximum allowed R_{SENSE} resistance when operating in the boost region with reverse conduction (V_{OUT} to V_{IN}). Skip this section and assume $R_{SENSE(MAX,BOOST,RVS)} = \infty$ when this operating condition does not apply to the application.

In the boost region, the maximum reverse V_{IN} current capability is the lowest when operating at the minimum duty cycle. See Switch Control: Boost Region (V_{IN} << V_{OUT}) section for the equation to calculate the minimum duty cycle $DC_{(ABSMIN, M3, BOOST)}$.

Before calculating the maximum R_{SENSE} resistance allowed during reverse operation, however, the inductor ripple current must be determined. If the main inductor L is not known, the ripple current $\Delta I_{L(MIN,BOOST)}$ can be estimated by choosing $\Delta I_{L(MIN,BOOST)}$ to be 10% of the minimum peak inductor current in the boost region as follows:

$$\Delta I_{L(MIN,BOOST)} \cong \frac{I_{IN(MAX,RVS)}}{\left(\frac{100\%}{10\%} - 0.5\right)} A$$

where:

$I_{IN(MAX,RVS)}$ is the maximum V_{IN} load current required in the boost region in the reverse direction

If the inductance is already known then $\Delta I_{L(MIN,BOOST)}$ can be calculated as follows:

$$\Delta I_{L(MIN,BOOST)} = \frac{\left(\frac{DC_{(ABSMIN,M3,BOOST)}}{100\%}\right) \bullet V_{IN(MIN,BOOST)}}{f \bullet L} A$$

where:

$DC_{(ABSMIN,M3,BOOST)}$ is the minimum duty cycle percentage in the boost region (see Switch Control: Boost Region (V_{IN} << V_{OUT}) section)

f is the switching frequency

L is the inductance of the main inductor

Now that the inductor ripple current is known, the maximum allowed R_{SENSE} in the boost region while in reverse conduction can be calculated as follows:

$$R_{SENSE(MAX,BOOST,RVS)} = \frac{2 \bullet \left| V_{RSENSE(MIN,BOOST,MINDC)} \right|}{\left(2 \bullet I_{IN(MAX,RVS)}\right) - \Delta I_{L(MIN,BOOST)}} \Omega$$

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where:

$V_{RSENSE(MIN,BOOST,MINDC)}$ is the minimum inductor current sense voltage in the boost region at the minimum duty cycle. Typical value is –93mV.

Negative result from the above equation indicates that any R_{SENSE} value can meet the requirement. Substitute the calculated result with ∞ and move onto the next section.

R_{SENSE} Selection: Max R_{SENSE} in the Buck Region

Forward Conduction: In this section $R_{SENSE(MAX,BUCK,FWD)}$ is calculated which is the maximum allowed R_{SENSE} resistance when operating in the buck region with forward conduction (V_{IN} to V_{OUT}).

In the buck region, the maximum V_{OUT} current capability is the lowest when operating at the minimum duty cycle. See Switch Control: Boost Region (V_{IN} << V_{OUT}) section for the equation to calculate the minimum duty cycle $DC_{(ABSMIN, M2,BUCK)}$.

Before calculating the maximum R_{SENSE} resistance, however, the inductor ripple current must be determined. If the main inductor L is not known, the ripple current $\Delta I_{L(MIN,BUCK)}$ can be estimated by choosing $\Delta I_{L(MIN,BUCK)}$ to be 10% of the maximum peak inductor current in the buck region as follows:

$$\Delta I_{L(MIN,BUCK)} \cong \frac{I_{OUT(MAX,FWD)}}{\left(\frac{100\%}{10\%} - 0.5\right)} A$$

where:

$I_{OUT(MAX,FWD)}$ is the maximum V_{OUT} load current required in the buck region in the forward direction.

If the inductance is already known then $\Delta I_{L(MIN,BUCK)}$ can be calculated as follows:

$$\Delta I_{L(MIN,BUCK)} = \frac{\left(\frac{DC_{(ABSMIN,M2,BUCK)}}{100\%}\right) \bullet V_{OUT(MIN,BUCK)}}{f \bullet L} A$$

where:

$DC_{(ABSMIN,M2,BUCK)}$ is the minimum duty cycle percentage in the buck region as calculated previously

f is the switching frequency

L is the inductance of the main inductor

After the inductor ripple current is known, the maximum allowed R_{SENSE} in the buck region while in forward conduction can be calculated as follows:

$$R_{SENSE(MAX,BUCK,FWD)} = \frac{2 \bullet V_{RSENSE(MAX,BUCK,MINDC)}}{\left(2 \bullet I_{OUT(MAX,FWD)}\right) - \Delta I_{L(MIN,BUCK)}} \Omega$$

where:

$V_{RSENSE(MAX,BUCK,MINDC)}$ is the maximum inductor current sense voltage at the minimum duty cycle. Typical value is 82mV.

Negative result from the above equation indicates that any R_{SENSE} value can meet the requirement. Substitute the calculated result with ∞ and move onto the next section.

Reverse Conduction: In this section $R_{SENSE(MAX, BUCK, RVS)}$ is calculated which is the maximum allowed R_{SENSE} resistance when operating in the buck region with reverse conduction (V_{OUT} to V_{IN}). Skip this section and assume $R_{SENSE(MAX, BUCK, RVS)} = \infty$ when this operating condition does not apply to the application.

In the buck region, the maximum reverse V_{IN} current capability is the least when V_{IN} is at its maximum and V_{OUT} is at its minimum for buck operation. Therefore R_{SENSE} must be chosen to meet the V_{IN} current requirements under these conditions.

Start by finding the buck region duty cycle when V_{IN} is minimum and V_{OUT} is maximum using:

$$DC_{(MAX,M2,BUCK)} \cong \left(1 - \frac{V_{OUT(MIN,BUCK)}}{V_{IN(MAX,BUCK)}}\right) \bullet 100\%$$

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Next, the inductor ripple current in the buck region must be determined. If the main inductor L is not known, the maximum ripple current $\Delta I_{L(MAX,BUCK)}$ can be estimated by choosing $\Delta I_{L(MAX,BUCK)}$ to be 30% to 50% of the maximum peak inductor current in the buck region as follows:

$$\Delta I_{L(MAX,BUCK)} \cong \frac{V_{IN(MAX,BUCK)} \bullet I_{IN(MAX,RVS)}}{V_{OUT(MIN,BUCK)} \bullet \left(\frac{100\%}{\%Ripple} - 0.5\right)} A$$

where:

$I_{IN(MAX,RVS)}$ is the maximum V_{IN} load current in the reverse direction required in the buck region.

%Ripple is 30% to 50%

Otherwise, if the inductance is already known then $\Delta I_{L(MAX,BUCK)}$ can be more accurately calculated as follows:

$$\Delta I_{L(MAX,BUCK)} \cong \frac{\left(\frac{DC_{(MAX,M2,BUCK)}}{100\%}\right) \bullet V_{OUT(MIN,BUCK)}}{f \bullet L} A$$

where:

$DC_{(MAX,M2,BUCK)}$ is the maximum duty cycle percentage in the buck region as calculated previously

f is the switching frequency

L is the inductance of the main inductor

After the maximum ripple current is known, the maximum allowed R_{SENSE} in the buck region while in reverse conduction can be calculated as follows:

$$R_{SENSE(MAX,BUCK,RVS)} = \frac{2 \bullet \left| V_{RSENSE(MIN,BUCK,MAXDC)} \right| \bullet V_{OUT(MIN,BUCK)}}{\left(2 \bullet \left| I_{IN(MAX,RVS)} \right| \bullet V_{IN(MAX,BUCK)}\right) + \left(\Delta I_{L(MAX,BUCK)} \bullet V_{OUT(MIN,BUCK)}\right)} \Omega$$

where:

$V_{RSENSE(MIN,BUCK,MAXDC)}$ is the minimum inductor current sense voltage at the maximum duty cycle. This value is determined in a similar manner to $V_{RSENSE(MAX,BOOST,MAXDC)}$ discussed previously in the R_{SENSE} Selection: Max R_{SENSE} in the Boost Region (Forward Conduction) section.

R_{SENSE} Selection: Final R_{SENSE} Value

The final R_{SENSE} value should be lower than all four maximum R_{SENSE} values, $R_{SENSE(MAX,BOOST,FWD)}$, $R_{SENSE(MAX,BOOST,RVS)}$, $R_{SENSE(MAX,BUCK,FWD)}$ and $R_{SENSE(MAX,BUCK,RVS)}$. A margin of 20% to 30% is recommended.

Figure 8 shows approximately how the maximum positive I_{OUT} and inductor currents would vary with V_{IN}/V_{OUT} while all other operating parameters remain constant (frequency = 120kHz, inductance = 10µH, R_{SENSE} = 1mΩ). This graph is normalized and accounts for changes in maximum current due to the slope compensation ramps and the effects of changing ripple current. The curve is theoretical but can be used as a guide to predict relative changes in maximum currents over a range of V_{IN}/V_{OUT} voltages. Similarly, when in reverse conduction, Figure 9 shows approximately how the maximum negative I_{IN} and inductor currents would vary with V_{IN}/V_{OUT}.

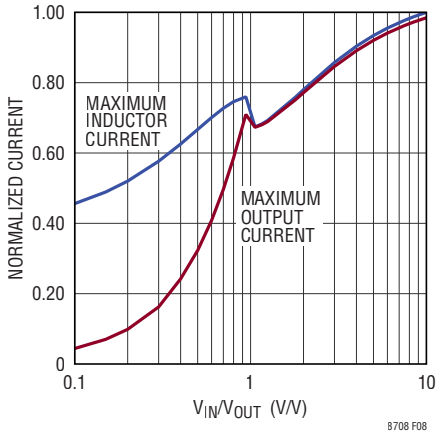

Figure 8. Currents vs V_{IN}/V_{OUT} Ratio in Forward Conduction

APPLICATIONS INFORMATION

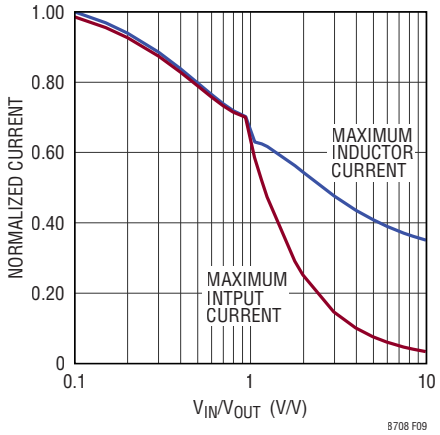

Figure 9. Currents vs V_{IN}/V_{OUT} Ratio in Reverse Conduction

R_{SENSE} FILTERING

Certain applications may require filtering of the inductor current sense signals due to excessive switching noise that can appear across R_{SENSE}. Higher operating voltages, higher values of R_{SENSE}, and more capacitive MOSFETs will all contribute additional noise across R_{SENSE} when the SW pins transition. The CSP/CSN sense signals can be filtered by adding one of the RC networks shown in Figure 10. Most PC board layouts can be drawn to accommodate either network on the same board. The network should be placed as close as possible to the IC. The network in Figure 10b can reduce common mode noise seen by the CSP/CSN pins of the LT8708 at the expense of some increased ground trace noise as current passes through the capacitors. A short direct path from the capacitor grounds to the IC ground should be used on the PC board. Resistors greater than 10Ω should be avoided as these can increase offset voltages at the CSP/CSN pins. The RC product should be kept to less than 30ns.

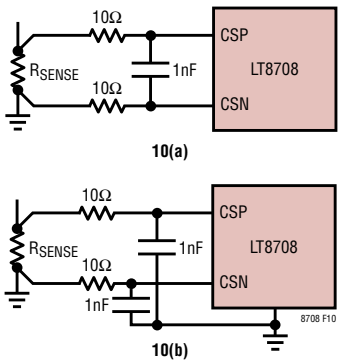

Figure 10. Inductor Current Sense Filter

INDUCTOR (L) SELECTION

For high efficiency, choose an inductor with low core loss, such as ferrite. Also, the inductor should have low DC resistance to reduce the I^2R losses, and must be able to handle the peak inductor current without saturating. To minimize radiated noise, use a toroid, pot core or shielded bobbin inductor.

The operating frequency and inductor selection are interrelated in that higher operating frequencies allow the use of smaller inductor and capacitor values. The following sections discuss several criteria to consider when choosing an inductor value. For optimal performance, choose an inductor that meets all of the following criteria.

L Selection: Load Current in Buck and Boost Regions

Small inductances result in increased ripple currents and thus, due to the positive and negative inductor current limits, decrease the maximum average forward I_{OUT} in the boost region and the maximum average reverse I_{IN} in the buck region.

In order to provide adequate forward I_{OUT} at low V_{IN} voltages in the boost region, L should be at least:

$$L_{(MIN1,BOOST)} \cong \frac{V_{IN(MIN,BOOST)} \bullet \left(\frac{DC_{(MAX,M3,BOOST)}}{100\%}\right)}{2 \bullet f \bullet \left(\frac{V_{RSENSE(MAX,BOOST,MAXDC)}}{R_{SENSE}} - \frac{I_{OUT(MAX,FWD)} \bullet V_{OUT(MAX,BOOST)}}{V_{IN(MIN,BOOST)}}\right)} H$$

where:

$DC_{(MAX,M3,BOOST)}$ is the maximum duty cycle percentage of the M3 switch (see R_{SENSE} Selection: Max R_{SENSE} in the Boost Region section)

f is the switching frequency

$V_{RSENSE(MAX,BOOST,MAXDC)}$ is the maximum current sense voltage in the boost region at maximum duty cycle (see R_{SENSE} Selection: Max R_{SENSE} in the Boost Region section)

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$I_{OUT(MAX,FWD)}$ is the maximum forward V_{OUT} current in boost region

To provide adequate reverse I_{IN} current at low V_{OUT} voltages in the buck region, L should be at least:

$$L_{(MIN1,BUCK)} \cong \frac{V_{OUT(MIN,BUCK)} \bullet \left(\frac{DC_{(MAX,M2,BUCK)}}{100\%}\right)}{2 \bullet f \bullet \left(\frac{|V_{RSENSE(MIN,BUCK,MAXDC)}|}{R_{SENSE}} - \frac{I_{IN(MAX,RVS)} \bullet V_{IN(MAX,BUCK)}}{V_{OUT(MIN,BUCK)}}\right)} \Omega$$

where:

$DC_{(MAX,M2,BUCK)}$ is the maximum duty cycle percentage of the M2 switch (see R_{SENSE} Selection: Max R_{SENSE} in the Buck Region section)

f is the switching frequency

$V_{RSENSE(MIN,BUCK,MAXDC)}$ is the minimum current sense voltage in the buck region at maximum duty cycle (see R_{SENSE} Selection: Max R_{SENSE} in the Buck Region section)

$I_{IN(MAX,RVS)}$ is the maximum reverse V_{IN} current in buck region

Negative values of $L_{(MIN1,BOOST)}$ or $L_{(MIN1,BUCK)}$ indicate that the load current can't be delivered because the inductor current limit is too low. If $L_{(MIN1,BOOST)}$ or $L_{(MIN1,BUCK)}$ is too large or is negative, consider reducing the R_{SENSE} resistor value to increase the inductor current limit.

L Selection: Subharmonic Oscillations

The LT8708's internal slope compensation circuits will prevent subharmonic oscillations that can otherwise occur when V_{IN}/V_{OUT} is less than 0.5 or greater than 2. The slope compensation circuits will prevent these oscillations provided that the inductance exceeds a minimum value (see the earlier section Inductor Current Sensing and Slope Compensation for more information). Choose an inductance greater than all of the relevant $L_{(MIN)}$ limits discussed below. Negative calculation results can be interpreted as zero.

In the boost region, if V_{OUT} can be greater than twice V_{IN}, calculate $L_{(MIN2,BOOST)}$ as follows:

$$L_{(MIN2,BOOST)} = \frac{\left[V_{OUT(MAX,BOOST)} - \left(\frac{V_{IN(MIN,BOOST)} \bullet V_{OUT(MAX,BOOST)}}{V_{OUT(MAX,BOOST)} - V_{IN(MIN,BOOST)}}\right)\right] \bullet R_{SENSE}}{0.08 \bullet f} H$$

In the buck region, if V_{IN} can be greater than twice V_{OUT}, calculate $L_{(MIN2,BUCK)}$ as follows:

$$L_{(MIN2,BUCK)} = \frac{\left[V_{IN(MAX,BUCK)} \bullet \left(1 - \frac{V_{OUT(MIN,BUCK)}}{V_{IN(MAX,BUCK)} - V_{OUT(MIN,BUCK)}}\right)\right] \bullet R_{SENSE}}{0.08 \bullet f} H$$

L Selection: Maximum Current Rating

The inductor must have a rating greater than its maximum operating current to prevent inductor saturation resulting in efficiency loss. The maximum forward inductor current in the boost region is:

$$I_{L(MAX,BOOST,FWD)} \cong I_{OUT(MAX,FWD)} \bullet \frac{V_{OUT(MAX,BOOST)}}{V_{IN(MIN,BOOST)}} + \left(\frac{V_{IN(MIN,BOOST)} \bullet \left(\frac{DC_{(MAX,M3,BOOST)}}{100\%}\right)}{2 \bullet L \bullet f}\right) A$$

where:

$DC_{(MAX,M3,BOOST)}$ is the maximum duty cycle percentage of the M3 switch (see R_{SENSE} Selection and Maximum Current section).

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The maximum reverse inductor current in the boost region for applications in which $V_{OUT(MAX)} \geq 2 \bullet V_{IN(MAX)}$ is:

$$I_{L(MAX,BOOST,RVS)} \cong I_{IN(MAX,RVS)} + \left(\frac{V_{IN(MAX,BOOST)}}{4 \bullet L \bullet f} \right) A$$

For applications in which $V_{OUT(MAX)} < 2 \bullet V_{IN(MAX)}$, the maximum reverse inductor current is smaller than the value given by the above equation. The following equation can be used to calculate the reverse inductor current for given combinations of V_{IN} and V_{OUT}.

$$I_{L(MAX,BOOST,RVS)} \cong I_{IN(MAX,RVS)} + \left(\frac{V_{IN} \bullet (V_{OUT} - V_{IN})}{2 \bullet L \bullet f \bullet V_{OUT}} \right) A$$

where:

$V_{OUT} > V_{IN}$

The maximum positive inductor current in the buck region for applications in which $V_{IN(MAX)} \geq 2 \bullet V_{OUT(MAX)}$ is:

$$I_{L(MAX,BUCK,FWD)} \cong I_{OUT(MAX,FWD)} + \left(\frac{V_{OUT(MAX,BUCK)}}{4 \bullet L \bullet f} \right) A$$

For applications with $V_{IN(MAX)} < 2 \bullet V_{OUT(MAX)}$, the maximum forward inductor current is smaller than the value given by the above equation. The following equation can be used to calculate the forward inductor current for given combinations of V_{IN} and V_{OUT}.

$$I_{L(BUCK,FWD)} \cong I_{OUT(MAX,FWD)} + \left(\frac{V_{OUT} \bullet (V_{IN} - V_{OUT})}{2 \bullet L \bullet f \bullet V_{IN}} \right) A$$

where:

$V_{IN} > V_{OUT}$

The maximum reverse inductor current when operating in the buck region is:

$$I_{L(MAX,BUCK,RVS)} \cong I_{IN(MAX,RVS)} \bullet \frac{V_{IN(MAX,BUCK)}}{V_{OUT(MIN,BUCK)}} + \left(\frac{V_{OUT(MIN,BUCK)} \bullet \frac{DC_{(MAX,M2,BUCK)}}{100\%}}{2 \bullet L \bullet f} \right) A$$

where:

$DC_{(MAX,M2,BUCK)}$ is the maximum duty cycle percentage of the M2 switch in the buck region (see R_{SENSE} Selection: Max R_{SENSE} in the Buck Region section).

Note that the inductor current can be higher when there are load transients or the load current exceeds the expected maximum amount. It can also be higher during start-up if inadequate soft-start capacitance is used, or during output shorts. Consider using the I_{IN} and/or I_{OUT} current limiting to help prevent the inductor current from becoming excessive. I_{IN} and I_{OUT} current limiting are discussed later in the I_{IN} and I_{OUT} Current Monitoring and Limiting section. Careful board evaluation of the maximum inductor current is recommended.

POWER MOSFET SELECTION

The LT8708 requires four external N-channel power MOSFETs, two for the top switches (switches M1 and M4, shown in Figure 3) and two for the bottom switches (switches M2 and M3, shown in Figure 3). Important parameters for the power MOSFETs are the breakdown voltage $V_{BR,DSS}$, threshold voltage $V_{GS,TH}$, on-resistance $R_{DS(ON)}$, output capacitance C_{OSS}, and maximum current $I_{DS(MAX)}$. The gate drive voltage is set by the 6.3V $GATEV_{CC}$ supply. Consequently, logic-level threshold MOSFETs must be used in LT8708 applications.

APPLICATIONS INFORMATION

It is very important to consider power dissipation when selecting power MOSFETs. The most efficient circuit will use MOSFETs that dissipate the least amount of power. Power dissipation must be limited to avoid overheating that might damage the devices. In forward conduction, the M1 and M3 switches will have the highest power dissipation, while M2 and M4 will have the highest power dissipation in reverse conduction. In some cases it can be helpful to use two or more MOSFETs in parallel to reduce power dissipation in each device. This is most helpful when power is dominated by I^2R losses while the MOSFET is "on". The additional capacitance of connecting MOSFETs in parallel can sometimes slow down switching edge rates and consequently increase total switching power losses.

The following sections provide guidelines for calculating power consumption of the individual MOSFETs. From a known power dissipation, the MOSFET junction temperature can be obtained using the following formula:

$$T_J = T_A + P \bullet R_{TH(JA)}$$

where:

T_J is the junction temperature of the MOSFET

T_A is the ambient air temperature

P is the power dissipated in the MOSFET

$R_{TH(JA)}$ is the MOSFET's thermal resistance from the junction to the ambient air. Refer to the manufacturer's data sheet.

$R_{TH(JA)}$ normally includes the $R_{TH(JC)}$ for the device plus the thermal resistance from the case to the ambient temperature $R_{TH(CA)}$. Compare the calculated value of T_J to the manufacturer's data sheets to help choose MOSFETs that will not overheat.

The power dissipation of the external N-channel MOSFETs comes from two primary components: (1) I^2R power when the switch is fully "on" and inductor current is flowing between the drain and source connections and (2) power dissipated while the switch is turning "on" and "off" and (B) charging and discharging the SW1 or SW2 node capacitance, which is dominated by the output capacitance of the external MOSFETs. Use Table 7 to determine which power components are applicable in the various regions of operation.

Table 7. NMOS Power in Various Operating Regions

OPERATING REGION		M1	M2	M3	M4
Pos. I_L	Buck	$P_{I^2R} + P_{SW}$	P_{I^2R}	0	P_{I^2R}
	Boost	P_{I^2R}	0	$P_{I^2R} + P_{SW}$	
	Buck-Boost	$P_{I^2R} + P_{SW}$	P_{I^2R}	$P_{I^2R} + P_{SW}$	
Neg. I_L	Buck	P_{I^2R}	$P_{I^2R} + P_{SW}$	0	P_{I^2R}
	Boost		0	P_{I^2R}	$P_{I^2R} + P_{SW}$
	Buck-Boost		$P_{I^2R} + P_{SW}$	P_{I^2R}	$P_{I^2R} + P_{SW}$

The MOSFET power components listed above can be approximated using the following equations. Note that I_{IN} can be substituted for I_{OUT} using:

$$I_{IN} \cong \frac{V_{OUT}}{V_{IN}} \bullet I_{OUT} \quad \text{where necessary.}$$

I^2R Component Equations:

$$P_{I^2R[M1,BUCK]} \text{ or } P_{I^2R[M4,BOOST]} \cong \frac{V_{OUT}}{V_{IN}} \bullet I_{OUT}{}^2 \bullet R_{DS(ON)} \bullet \rho_\tau \, W$$

$$P_{I^2R[M1,BOOST]} \cong \left(\frac{V_{OUT}}{V_{IN}} \bullet I_{OUT}\right)^2 \bullet R_{DS(ON)} \bullet \rho_\tau$$

$$P_{I^2R[M2,BUCK]} \cong \frac{V_{IN} - V_{OUT}}{V_{IN}} \bullet I_{OUT}{}^2 \bullet R_{DS(ON)} \bullet \rho_\tau \, W$$

$$P_{I^2R[M3,BOOST]} \cong \frac{V_{OUT} - V_{IN}}{V_{IN}{}^2} \bullet V_{OUT} \bullet I_{OUT}{}^2 \bullet R_{DS(ON)} \bullet \rho_\tau \, W$$

$$P_{I^2R[M4,BUCK]} \cong I_{OUT}{}^2 \bullet R_{DS(ON)} \bullet \rho_\tau \, W$$

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Switching Component Equations for M1 and M2:

$$P_{SW[M1,BUCK]} \text{ or } P_{SW[M2,BUCK]} \cong P_{SWA} + P_{SWB} \cong (V_{IN} \bullet |I_{OUT}| \bullet f \bullet t_{RF1}) + (0.5 \bullet C_{OSS(M1+M2)} \bullet V_{IN}^2 \bullet f)\ W$$

Switching Component Equations for M3 and M4:

$$P_{SW[M3,BOOST]} \text{ or } P_{SW[M4,BOOST]} \cong P_{SWA} + P_{SWB} \cong \left(V_{OUT}^2 \bullet |I_{OUT}| \bullet f \bullet \frac{t_{RF2}}{V_{IN}} \right) + (0.5 \bullet C_{OSS(M3+M4)} \bullet V_{OUT}^2 \bullet f)\ W$$

where:

t_{RF1} is the average of the SW1 pin rise and fall times. Typical values are 20 – 40ns depending on the MOSFET capacitance and V_{IN} voltage.

t_{RF2} is the average of the SW2 pin rise and fall times and, similar to t_{RF1}, is typically 20ns – 40ns depending on the MOSFET capacitance and V_{OUT} voltage.

$R_{DS(ON)}$ is the "on" resistance of the MOSFET at 25°C

ρ_T is a normalization factor (unity at 25°C) accounting for the significant variation in MOSFET on-resistance with temperature, typically about 0.4%/°C, as shown in Figure 11. For a maximum junction temperature of 125°C, using a value = 1.5 is reasonable.

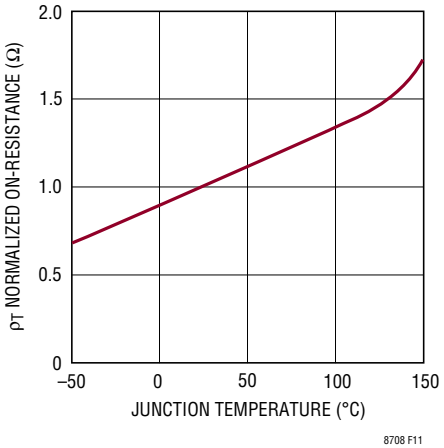

Figure 11. Normalized MOSFET RDS(ON) vs Temperature

Switch M1: For positive conduction, the maximum power dissipation in M1 occurs either in the buck region when V_{IN} is highest, V_{OUT} is highest, and switching power losses are greatest, or in the boost region when V_{IN} is smallest, V_{OUT} is highest and M1 is always on.

In most cases of negative conduction, the M1 switching power dissipation is quite small and I^2R power losses dominate. In negative conduction, M1 I^2R power is greatest in the boost region due to the lower V_{IN} and higher V_{OUT} that cause the M1 switch to be "on" for the most amount of time.

Switch M2: In most cases of positive conduction, the M2 switching power dissipation is quite small and I^2R power losses dominate. In positive conduction, M2 I^2R power is greatest in the buck region due to the higher V_{IN} and lower V_{OUT} that cause M2 to be "on" for the most amount of time.

For negative conduction, the maximum power dissipation in M2 occurs in the buck region when V_{IN} is highest and V_{OUT} is lowest.

Switch M3: If the inductor current is positive, the maximum power dissipation in M3 occurs when V_{IN} is lowest and V_{OUT} is highest.

In most cases of negative conduction, the M3 switching power dissipation is quite small and I^2R power losses dominate. In negative conduction, M3 I^2R power is greatest in the boost region due to the lower V_{IN} and higher V_{OUT} that cause the M3 switch to be "on" for the most amount of time.

Switch M4: If the inductor current is positive, in most cases the switching power dissipation in the M4 switch is quite small and I^2R power losses dominate. I^2R power is greatest in the boost region due to the lower V_{IN} and higher V_{OUT} that cause M4 switch to be "on" for the most amount of time.

If the inductor current is negative, the maximum power dissipation in the M4 switch occurs either in the boost region when V_{IN} is highest, V_{OUT} is highest, and switching power losses are greatest, or in the buck region when V_{IN} is highest, V_{OUT} is lowest and M4 is always on.

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Gate Resistors: In some cases it can be beneficial to add 1Ω to 10Ω of resistance between some of the NMOS gate pins and their respective gate driver pins on the LT8708 (i.e., TG1, BG1, TG2, BG2). Due to parasitic inductance and capacitance, ringing can occur on SW1 or SW2 when low capacitance MOSFETs are turned on/off too quickly. The ringing can be of greatest concern when operating the MOSFETs or the LT8708 near the rated voltage limits. Additional gate resistance slows the switching speed, minimizing the ringing.

Excessive gate resistance can have two negative side effects on performance:

1. Slowing the switch transition times can also increase power dissipation in the switch. This is described above.
2. Capacitive coupling from the SW1 or SW2 pin to the switch gate node can turn it on when it's supposed to be off, thus increasing power dissipation. With too much gate resistance, this would happen to the M2 switch when SW1 is rising with positive inductor current and to the M3 switch when SW2 is rising with negative inductor current.

Careful board evaluation should be performed when optimizing the gate resistance values. SW1 and SW2 pin ringing can be affected by the inductor current levels, therefore board evaluation should include measurements at a wide range of load currents, V_{IN} and V_{OUT}. When performing PCB measurements of the SW1 and SW2 pins, be sure to use a very short ground post from the PCB ground to the scope probe ground sleeve in order to minimize false inductive voltage readings.

C_{IN} AND C_{OUT} SELECTION

V_{IN} and V_{OUT} capacitance is necessary to suppress voltage ripple caused by discontinuous current moving in and out of the regulator. A parallel combination of capacitors is typically used to achieve high capacitance and low ESR (equivalent series resistance). Dry tantalum, special polymer, aluminum electrolytic and ceramic capacitors are all available in surface mount packages. Capacitors with low ESR and high ripple current ratings, such as OS-CON and POSCAP are also available.

Ceramic capacitors should be placed near the regulator input and output to suppress high frequency switching spikes. A ceramic capacitor, of at least 1µF at the maximum V_{INCHIP} operating voltage, should also be placed from V_{INCHIP} to GND as close to the LT8708 pins as possible. Due to their excellent low ESR characteristics ceramic capacitors can significantly reduce input ripple voltage and help reduce power loss in the higher ESR bulk capacitors. X5R or X7R dielectrics are preferred, as these materials retain their capacitance over wide voltage and temperature ranges. Many ceramic capacitors, particularly 0805 or 0603 case sizes, have greatly reduced capacitance at the desired operating voltage.

V_{IN} Capacitance: Discontinuous V_{IN} current is highest in the buck region due to the M1 switch toggling on and off. Make sure that the C_{IN} capacitor network has low enough ESR and is sized to handle the maximum RMS current. For buck operation, the V_{IN} RMS current is given by:

$$I_{(IN,RMS)} \cong I_{OUT} \bullet \frac{V_{OUT}}{V_{IN}} \bullet \sqrt{\frac{V_{IN}}{V_{OUT}} - 1} \quad A$$

This formula has a maximum at $V_{IN} = 2 \bullet V_{OUT}$, where $I_{(IN,RMS)} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief.

C_{IN} is necessary to reduce the V_{IN} voltage ripple caused by discontinuities and ripple of I_{IN}. The effects of ESR and the bulk capacitance must be considered when choosing the correct capacitor for a given V_{IN} ripple.

The V_{IN} ripple due to the voltage drop across the bulk cap ESR_{BULK}, without having any ceramic capacitance in parallel, is approximately:

$$\Delta V_{(IN,BUCK,BULK)} \cong I_{OUT} \bullet ESR_{BULK} \; V$$

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When low ESR ceramic capacitance is added in parallel with the bulk capacitor, the V_{IN} ripple is approximately:

$$\Delta V_{(IN,BUCK,CERAM)} \cong I_{OUT} \bullet \frac{V_{OUT}}{V_{IN}} \bullet ESR_{CERAM} \bullet \left(1 - \exp\left(\frac{-V_{OUT}}{V_{IN} \bullet f \bullet ESR_{CERAM} \bullet C_{IN-CERAM}}\right)\right) V$$

Add enough ceramic capacitance to make sure $\Delta V_{(IN,BUCK,CERAM)}$ is adequate for the application. In a properly designed application, $\Delta V_{(IN,BUCK,CERAM)}$ should be much smaller than $\Delta V_{(IN,BUCK,BULK)}$.

V_{OUT} Capacitance: Discontinuous V_{OUT} current is highest in the boost region due to the M4 switch toggling on and off. Make sure that the C_{OUT} capacitor network has low enough ESR and is sized to handle the maximum RMS current. For boost operation, the V_{OUT} RMS current is given by:

$$I_{(OUT,RMS)} \cong I_{OUT} \bullet \sqrt{\frac{V_{OUT}}{V_{IN}} - 1} \quad A$$

This formula has a maximum when V_{IN} is minimum and V_{OUT} is maximum.

C_{OUT} is necessary to reduce the V_{OUT} ripple caused by discontinuities and ripple of I_{OUT}. The effects of ESR and the bulk capacitance must be considered when choosing the right capacitor for a given V_{OUT} ripple.

The V_{OUT} ripple due to the voltage drop across the bulk cap ESR without having any ceramic caps in parallel is approximately:

$$\Delta V_{(OUT,BOOST,BULK)} \cong \frac{V_{OUT} \bullet I_{OUT}}{V_{IN}} \bullet ESR_{BULK}$$

$$\Delta V_{(OUT,BUCK,BULK)} \cong I_{RIPPLE} \bullet ESR_{BULK}$$

With enough ceramic caps added in parallel, the steady state V_{OUT} ripple due to charging and discharging the ceramic C_{OUT} is given by the following equations:

$$\Delta V_{(OUT,BOOST,CERAM)} \cong I_{OUT} \bullet ESR_{CERAM} \bullet \left(1 - \exp\left(\frac{V_{IN} - V_{OUT}}{V_{OUT} \bullet f \bullet ESR_{CERAM} \bullet C_{OUT-CERAM}}\right)\right) V$$

for $V_{OUT} > V_{IN}$, and

$$\Delta V_{(OUT,BUCK,CERAM)} \cong \frac{V_{OUT} \bullet \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}{8 \bullet L \bullet f^2 \bullet C_{OUT-CERAM}} V$$

for $V_{OUT} < V_{IN}$

Add enough ceramic caps to make sure $\Delta V_{(OUT,BOOST,CERAM)}$ and $\Delta V_{(OUT,BUCK,CERAM)}$ are adequate for the application. In a properly designed application, $\Delta V_{(OUT,BOOST,CERAM)}$ and $\Delta V_{(OUT,BUCK,CERAM)}$ should be much smaller than $\Delta V_{(OUT,BOOST,BULK)}$ and $\Delta V_{(OUT,BUCK,BULK)}$, respectively.

SCHOTTKY DIODE (D1, D2, D3, D4) SELECTION

During forward conduction the Schottky diodes, D2 and D4, shown in Figure 1, conduct during the dead time between the conduction of the power MOSFET switches. They help to prevent the body diodes of synchronous switches M2 and M4 from turning on and storing charge. For example, D4 can significantly reduce reverse-recovery current when M3 turns on, which improves converter efficiency, reduces switch M3 power dissipation, and reduces noise in the inductor current sense resistor (R_{SENSE}). Similarly, during reverse conduction, D1 and D3 conduct during the dead time between the conduction of the power MOSFET switches. In order for the diodes to be effective, the inductance between them and the synchronous switch must be as small as possible, mandating that these components be placed very close to the MOSFETs.

APPLICATIONS INFORMATION

For applications with high input or output voltages (typically >40V) avoid Schottky diodes with excessive reverse-leakage currents, particularly at high temperatures. Some ultra-low V_F diodes will trade-off increased high temperature leakage current for reduced forward voltage. Diodes D1 and D2 can have reverse voltages in excess of V_{IN} and D3 and D4 can have reverse voltages in excess of V_{OUT}. The combination of high reverse voltage and current can lead to self-heating of the diode. Besides reducing efficiency, this can increase leakage current which increases temperatures even further. Choose packages with lower thermal resistance (θ_{JA}) to minimize self heating of the diodes.

TOPSIDE MOSFET DRIVER SUPPLY (C_{B1}, D_{B1}, C_{B2}, D_{B2})

The top MOSFET drivers (TG1 and TG2) are driven digitally between their respective SW and BOOST pin voltages. The BOOST voltages are biased from floating booststrap capacitors C_{B1} and C_{B2}, which are normally recharged through external silicon diodes D_{B1} and D_{B2} when the respective top MOSFET is turned off. The capacitors are charged to about 6.3V (about equal to $GATEV_{CC}$) forcing the $V_{BOOST1-SW1}$ and $V_{BOOST2-SW2}$ voltages to be about 6.3V. The boost capacitors C_{B1} and C_{B2} need to store about 100 times the gate charge required by the top switches M1 and M4. In most applications, a 0.1µF to 0.47µF, X5R or X7R dielectric capacitor is adequate. The bypass capacitance from $GATEV_{CC}$ to GND should be at least 10 times the C_{B1} or C_{B2} capacitance.

Top Driver: Boost Cap Charge Control Block

When the LT8708 operates exclusively in the boost or buck region, M1 or M4 respectively may be "on" continuously. This prevents the respective bootstrap capacitor, C_{B1} or C_{B2}, from being recharged through the silicon diode, D_{B1} or D_{B2}. The Boost Cap Charge Control block (see Figure 1) keeps the appropriate bootstrap capacitor charged in these cases. In the boost region, when M1 is always on, current is drawn, as needed, from the CSNOUT and/or BOOST2 pins to charge the C_{B1} capacitor. In the buck region, when M4 is always on, current is drawn, as needed, from the CSNIN and/or BOOST1 pins to charge the C_{B2} capacitor. Because of this function, CSPIN and CSNIN should be connected across R_{SENSE1} in series with the M1 drain. Connect both pins to the M1 drain if they are not being used. Also, CSPOUT and CSNOUT should be connected across R_{SENSE2} in series with the M4 drain or connect both to the M4 drain if not being used.

Top Driver: Boost Diodes D_{B1} and D_{B2}

Although Schottky diodes have the benefit of low forward voltage drops, they can exhibit high reverse current leakage and have the potential for thermal runaway under high voltage and temperature conditions. Silicon diodes are thus recommended for diodes D_{B1} and D_{B2}. Make sure that D_{B1} and D_{B2} have reverse breakdown voltage ratings higher than $V_{IN(MAX)}$ and $V_{OUT(MAX)}$ and have less than 1mA of reverse-leakage current at the maximum operating junction temperature. Make sure that the reverse-leakage current at high operating temperatures and voltages won't cause thermal runaway of the diode.

In some cases it is recommended that up to 5Ω of resistance is placed in series with D_{B1} and D_{B2}. The resistors reduce surge currents in the diodes and can reduce ringing at the SW and BOOST pins of the IC. Since SW pin ringing is highly dependent on PCB layout, SW pin edge rates and the type of diodes used, careful measurements directly at the SW pins of the IC are recommended. If required, a single resistor can be placed between $GATEV_{CC}$ and the common anodes of D_{B1} and D_{B2} (as in the front page application) or by placing separate resistors between the cathodes of each diode and the respective BOOST pins. Excessive resistance in series with D_{B1} and D_{B2} can reduce the BOOST-SW capacitor voltage when the M2 or M3 on-times are very short and should be avoided.

VINHIMON, VOUTLOMON AND $\overline{RVSOFF}$

During reverse conduction, current and power are drawn from V_{OUT} and delivered to V_{IN}. This has the potential to draw V_{OUT} lower than desired or drive V_{IN} higher than desired, depending on the supplies and loads. The VINHIMON and VOUTLOMON pins are used to detect either of these conditions and disable reverse conduction by pulling $\overline{RVSOFF}$ low.

APPLICATIONS INFORMATION

The purpose of the VINHIMON and VOUTLOMON functions becomes clearer when considering the priorities of the error amplifiers (see Table 3). A few important cases should be considered.

1. **V_{IN} and V_{OUT} are both above regulation**: In this case FBIN is greater than 1.205V while FBOUT is greater than 1.207V. Normally this condition causes V_C to fall due to FBOUT being above 1.207V. The LT8708 responds by increasing the reverse current and power being fed into V_{IN}.

   This can be an undesirable response, for example, if V_{IN} is connected to a battery being charged from V_{OUT}. The solution is to use VINHIMON to detect the maximum V_{IN} and disable reverse conduction by pulling $\overline{RVSOFF}$ low.

2. **V_{IN} and V_{OUT} are both below regulation**: In this case FBIN is below 1.205V while FBOUT is below 1.207V. Normally this condition causes V_C to fall due to FBIN being below 1.205V. The LT8708 responds by increasing the reverse current and power being drawn from V_{OUT}.

   This can be an undesirable response, for example, if V_{OUT} is connected to a battery or supercapacitor supplying power to V_{IN}. The solution is to use VOUTLOMON to detect the minimum V_{OUT} and disable reverse conduction by pulling $\overline{RVSOFF}$ low.

If VINHIMON rises above its activation threshold or VOUTLOMON falls below its activation threshold (see Electrical Characteristics), the LT8708 will pull the $\overline{RVSOFF}$ pin low and not allow M4 switch to turn on if the inductor current is negative. In addition to the 24mV (typical) voltage hysteresis, the VINHIMON pin will source 1µA (typical) current and the VOUTLOMON pin will sink 1µA (typical) current as current hysteresis.

There are two ways to configure the VINHIMON and VOUTLOMON pins. Method (1) uses dedicated resistor dividers for VINHIMON and VOUTLOMON respectively, while method (2) uses common resistor dividers for VINHIMON and FBIN as well as for VOUTLOMON and FBOUT, allowing improved tracking with the FBOUT and FBIN regulation voltages, respectively.

1. Connect a resistor divider between V_{IN}, VINHIMON and GND to configure the V_{IN} overvoltage threshold. Connect a resistor divider between V_{OUT}, VOUTLOMON and GND to configure the V_{OUT} undervoltage threshold. (see Figure 12). Use the following equations to calculate the resistor values:

$$R_{HIMON1} = \frac{V_{OVIN^+} - 1.207}{I_{FBDIV}}$$

$$R_{HIMON2} = \frac{1.207}{I_{FBDIV}}$$

$$R_{HIMON3} = \left(\frac{1.207 - V_{HYSMON}}{I_{HYSMON}}\right) - \left(\frac{R_{HIMON1} \bullet R_{HIMON2}}{R_{HIMON1} + R_{HIMON2}}\right) - \left(\frac{V_{OVIN^-} \bullet R_{HIMON2}}{I_{HYSMON} \bullet (R_{HIMON1} + R_{HIMON2})}\right)$$

$$R_{LOMON1} = \frac{V_{UVOUT^-} - 1.207}{I_{FBDIV}}$$

$$R_{LOMON2} = \frac{1.207}{I_{FBDIV}}$$

$$R_{LOMON3} = \left(\frac{V_{UVOUT^+} \bullet R_{LOMON2}}{I_{HYSMON} \bullet (R_{LOMON1} + R_{LOMON2})}\right) - \left(\frac{R_{LOMON1} \bullet R_{LOMON2}}{R_{LOMON1} + R_{LOMON2}}\right) - \left(\frac{1.207 + V_{HYSMON}}{I_{HYSMON}}\right)$$

where:

I_{FBDIV} is the desired current through the resistor string. 50µA – 100µA is a good value.

V_{OVIN}+ and V_{OVIN}– are the rising and falling V_{IN} overvoltage thresholds.

V_{UVOUT}+ and V_{UVOUT}– are the rising and falling V_{OUT} undervoltage thresholds.

$R_{HIMON1-3}$ and $R_{LOMON1-3}$ are shown in Figure 12.

V_{HYSMON} is the VINHIMON and VOUTLOMON hysteresis voltage. Typical value is 24mV.

I_{HYSMON} is the VINHIMON and VOUTLOMON hysteresis current. Typical value is 1µA.

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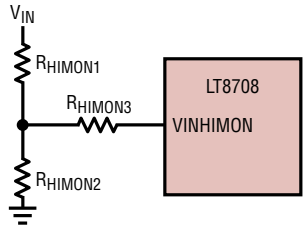
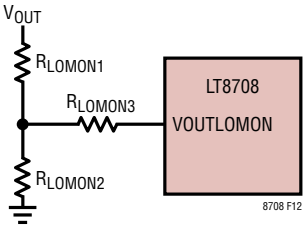


(a) Resistor Divider for VINHIMON



(b) Resistor Divider for VOUTLOMON

Figure 12.

2. Connect a resistor divider between V_{IN}, FBIN, VINHIMON and GND to configure the V_{IN} regulation and overvoltage thresholds (see Figure 13). Connect a resistor divider between V_{OUT}, VOUTLOMON, FBOUT and GND to configure the V_{OUT} regulation and undervoltage thresholds (see Figure 14).

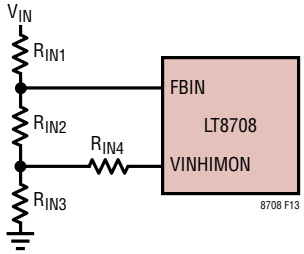


Figure 13. Single Divider for VINHIMON and FBIN

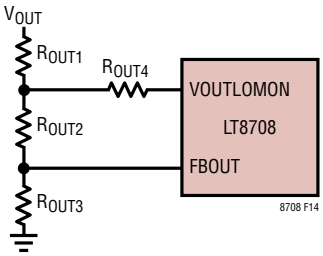


Figure 14. Single Divider for VOUTLOMON and FBOUT

Use the following equations to calculate the resistor values:

$$R_{IN3} = \frac{1.207 \bullet V_{IN}}{V_{OVIN^+} \bullet I_{FBDIV}}$$

$$R_{IN1} = V_{OVIN^+} \bullet R_{IN3} \bullet \left(\frac{1}{1.207} - \frac{1}{V_{IN}} \right)$$

$$R_{IN2} = \frac{(V_{OVIN^+} - V_{IN})}{V_{IN}} \bullet R_{IN3}$$

$$R_{IN4} = \left(\frac{[(R_{IN1} + R_{IN2}) \bullet I_{HYSMON} + V_{OVIN^+} - V_{OVIN^-}] \bullet 1.207}{V_{OVIN^+} \bullet I_{HYSMON}} \right) - \left(\frac{V_{HYSMON}}{I_{HYSMON}} \right) - \left(\frac{(V_{OVIN^+} - 1.207) \bullet R_{IN3}}{V_{OVIN^+}} \right)$$

$$R_{OUT3} = \frac{1.207}{I_{FBDIV}}$$

$$R_{OUT1} = V_{OUT} \bullet R_{OUT3} \bullet \left(\frac{1}{1.207} - \frac{1}{V_{UVOUT^-}} \right)$$

$$R_{OUT2} = \frac{(V_{OUT} - V_{UVOUT^-})}{V_{UVOUT^-}} \bullet R_{OUT3}$$

$$R_{OUT4} = \left(\frac{(R_{OUT1} \bullet I_{HYSMON} + V_{UVOUT^+} - V_{UVOUT^-}) \bullet 1.207}{V_{UVOUT^-} \bullet I_{HYSMON}} \right) - \left(\frac{V_{HYSMON}}{I_{HYSMON}} \right) - \left(\frac{(V_{UVOUT^-} - 1.207) \bullet R_{OUT3}}{V_{UVOUT^-}} \right)$$

where:

I_{FBDIV} is the desired current through the resistor string. 50µA – 100µA is a good value.

V_{IN} and V_{OUT} are the desired regulation voltages.

V_{OVIN+} and V_{OVIN-} are the rising and falling V_{IN} overvoltage thresholds.

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V_{UVOUT+} and V_{UVOUT-} are the rising and falling V_{OUT} undervoltage thresholds.

R_{IN1-4} and R_{OUT1-4} are shown in Figure 13 and Figure 14.

V_{HYSMON} is the VINHIMON and VOUTLOMON hysteresis voltage. Typical value is 24mV.

I_{HYSMON} is the VINHIMON and VOUTLOMON hysteresis current. Typical value is 1µA.

If unused, tie VINHIMON to GND and/or VOUTLOMON to LDO33.

Note: after the resistor values are selected, make sure to check that the FBIN and VOUTLOMON voltages are below their ABSMAX values when V_{IN} and V_{OUT} are at their maximum, respectively.

I_{IN} AND I_{OUT} CURRENT MONITORING AND LIMITING

The LT8708 has independent I_{IN} and I_{OUT} current monitors that can monitor and limit the respective currents in both positive and negative directions. Figure 15 and Figure 16 illustrate the operation of the current monitor circuits.

The remaining discussion refers to the I_{IN} current monitor circuit of Figure 15. All discussion and equations are also applicable to the I_{OUT} current monitor circuit, substituting pin and device names as appropriate.

Current Monitoring: The IMON_INP and IMON_INN pins can be used to monitor I_{IN} in the forward and reverse directions, respectively. When configured as shown in Figure 15, the IMON_INP and IMON_INN voltages are proportional to I_{IN}. V_{IMON_INP} is proportional to the positive I_{IN} current, increasing as I_{IN} becomes more positive. V_{IMON_INN} is proportional to the negative I_{IN} current, increasing as I_{IN} becomes more negative.

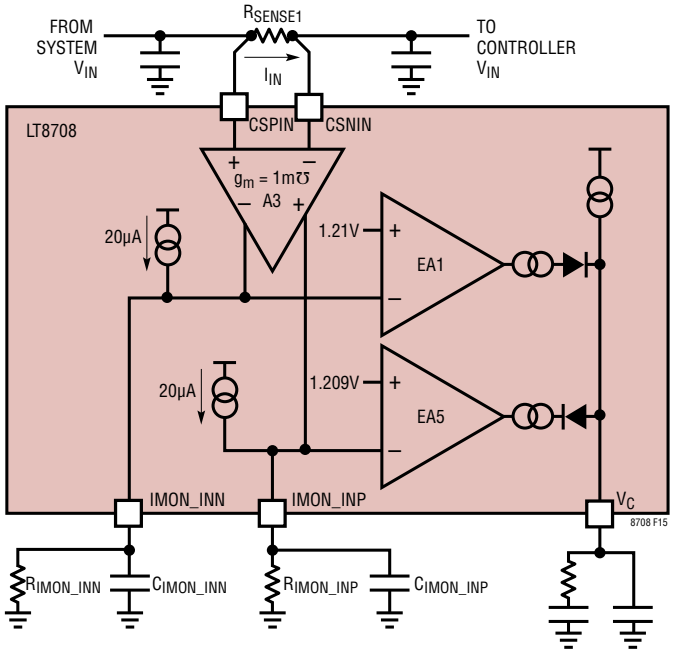

Figure 15. I_{IN} Current Monitor and Limit

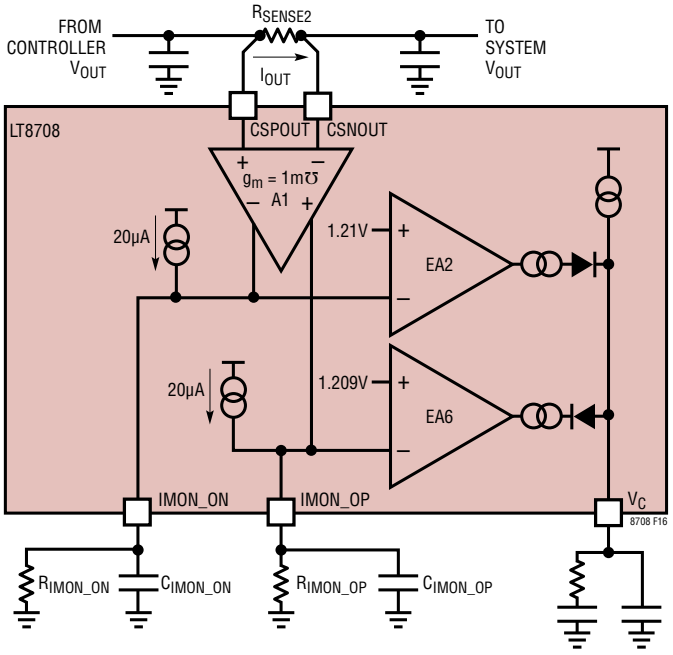

Figure 16. I_{OUT} Current Monitor and Limit

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Transconductance amplifier A3 performs this monitoring function. A3 converts the current sense voltage, $V_{CSPIN-CSNIN}$, into two currents:

$$+V_{CSPIN-CSNIN} \bullet 1m\frac{A}{V}$$

and

$$-V_{CSPIN-CSNIN} \bullet 1m\frac{A}{V}$$

These currents are added to 20µA offsets and then forced into R_{IMON_INP} and R_{IMON_INN}, respectively.

Due to the 20µA offset currents, V_{IMON_INP} and V_{IMON_INN} are not 0V when I_{IN} is 0A. Instead, $V_{IMON\_INP(0)}$ = 20µA•R_{IMON_INP} Volts and $V_{IMON\_INN(0)}$ = 20µA•R_{IMON_INN} Volts (typical) when I_{IN} = 0 Amps. As I_{IN} becomes increasingly negative, V_{IMON_INP} reduces below $V_{IMON\_INP(0)}$ until V_{IMON_INP} = 0V. Similarly, as I_{IN} becomes increasingly positive, V_{IMON_INN} reduces below $V_{IMON\_INN(0)}$ until V_{IMON_INN} = 0V. I_{MON_INP} and I_{MON_INN} will not be driven below ground as their output currents can only be positive or zero.

The complete transfer functions for IMON_INP and IMON_INN are given in the equations below:

$$V_{IMON\_INP} = \left(1m\frac{A}{V} \bullet R_{SENSE1} \bullet I_{IN} + 20\mu A\right) \bullet R_{IMON\_INP}$$

$$V_{IMON\_INN} = \left(-1m\frac{A}{V} \bullet R_{SENSE1} \bullet I_{IN} + 20\mu A\right) \bullet R_{IMON\_INN}$$

The differential voltage $V_{CSPIN-CSNIN}$ should remain between –100mV and 100mV due to the limited current that can be driven out of IMON_INP and IMON_INN. If the instantaneous $V_{CSPIN-CSNIN}$ exceeds these limits but the average $V_{CSPIN-CSNIN}$ is within the limits, consider including the current sense filter described in the next section.

In addition, IMON_INP and IMON_INN should be filtered with capacitors C_{IMON_INP} and C_{IMON_INN} due to I_{IN} ripple and discontinuities that can occur in various regions of operation. A few nF of capacitance is usually sufficient.

Current Limiting: As shown in Figure 15, IMON_INP voltage that exceeds 1.209V (typical) causes V_C to reduce, thus limiting the forward I_{IN} and inductor currents. IMON_INN voltage that exceeds 1.21V (typical) causes V_C to increase, thus limiting the reverse I_{IN} and inductor currents (see the Error Amplifiers section).

The forward I_{IN} limit, $I_{(IN,FWD,LIMIT)}$, can be set as needed by choosing the appropriate R_{SENSE1} and R_{IMON_INP} resistors using the following equation:

$$R_{IMON\_INP} = \frac{1.209}{I_{(IN,FWD,LIMIT)} \bullet 1m\frac{A}{V} \bullet R_{SENSE1} + 20\mu A}\Omega$$

For example, if R_{SENSE1} is chosen to be 12.5mΩ and the desired forward I_{IN} current limit is 4A then:

$$R_{IMON\_INP} = \frac{1.209}{4A \bullet 1m\frac{A}{V} \bullet 12.5m\Omega + 20\mu A} = 17.3k\Omega$$

Similarly, the reverse I_{IN} limit, $I_{(IN,RVS,LIMIT)}$, can be set as needed by choosing the appropriate R_{SENSE1} and R_{IMON_INN} resistors using the following equation:

$$R_{IMON\_INN} = \frac{1.21}{I_{(IN,RVS,LIMIT)} \bullet 1m\frac{A}{V} \bullet R_{SENSE1} + 20\mu A}\Omega$$

C_{IMON_INP} and C_{IMON_INN} capacitors of at least a few nF are necessary to maintain loop stability when IMON_INP and IMON_INN, respectively, are used to operate the LT8708 at constant current limit.

Review the Electrical Characteristics and the IMON Output Currents graph in the Typical Performance Characteristics section to understand the operational limits of the IMON_OP, IMON_ON, IMON_INP and IMON_INN currents.

External currents can be summed to the IMON pins to adjust I_{IN} and/or I_{OUT} limit in both directions while switching. When the IMON_OP and IMON_ON pins are used in

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this way, ICP and ICN can be used to monitor the I_{OUT} current in the forward and reverse directions respectively (see the Current Monitoring, Regulation and Limiting: ICP and ICN Pins section).

Current Sense Filter: The + and – outputs of current sense amplifiers A1 and A3 are rated to provide a range of –20µA to +100µA. For example, IMON_INP, which primarily reports forward I_{IN} current, may not provide the expected output current when $V_{CSPIN-CSNIN}$ exceeds 100mV. In addition, the IMON_INP pin will not provide the expected output current when $V_{CSPIN-CSNIN}$ is below –20mV.

Currents that flow through the current sense resistors (R_{SENSE1}, R_{SENSE2} in Figure 17) are often discontinuous and can contain significant AC content during each switching cycle. One example is the forward I_{IN} in the buck region. If the I_{IN} current presents an average differential ($V_{CSPIN-CSNIN}$) less than 100mV, but contains AC peaks exceeding 100mV, the IMON_INP current may clip. To prevent clipping, the current sense filter shown in Figure 17, can be added. The filter will reduce the peak differential ($V_{CSPIN-CSNIN}$) to <100mV while keeping the same average, thus allowing the correct result to be presented on IMON_INP. As another example, consider the reverse I_{OUT} measured by IMON_ON. If the current presents an average differential ($V_{CSNOUT-CSPOUT}$) less than 100mV, but contains AC peaks exceeding 100mV, the current sense filter can be used to reduce the peaks below 100mV while keeping the same average.

The –20µA output current limits for amplifiers A1 and A3 are often most important when using the HCM mode (see the Unidirectional Conduction: HCM section). The current sense amplifier outputs may clip at the –20µA limits when the average sensed current is low but contains high AC content. Clipping may distort the ICN or IMON_INP voltages that are used to select between heavy and light load HCM operation. Once again, the current sense filter can be used to reduce the AC content appearing at the amplifier inputs.

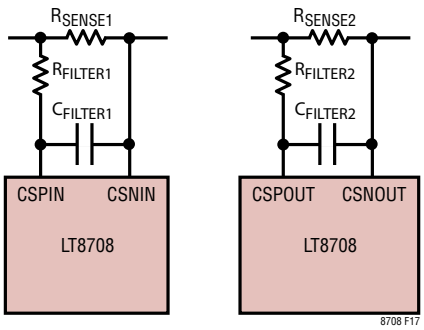

Figure 17. CSPIN/CSNIN and CSPOUT/CSNOUT Current Sense Filter

Current sense filter(s) should be connected as shown in Figure 16. Note that resistance in series with CSNIN and CSNOUT is not recommended. As described in the Topside MOSFET Driver Supply (CB1, DB1, CB2, DB2) section, the CSNIN and CSNOUT pins are also connected to the Boost Cap Charge Control block (also see Figure 1) and can draw current under certain conditions. In addition, the same CSNIN and CSNOUT current sense pins can draw bias current under normal operating conditions, while CSPIN and CSPOUT draw zero (typical) bias current. A time constant lower than 10µs is recommended for the filter(s).

Also, because of their use with the Boost Cap Charge Control block, tie the CSPIN and CSNIN pins to V_{IN} and tie the IMON_INP and IMON_INN pins to ground when the input current sensing is not in use. Similarly, the CSPOUT and CSNOUT pins should be tied to V_{OUT}, the IMON_OP, IMON_ON pins should be grounded when not in use.

LOOP COMPENSATION

The loop stability is affected by a number of factors including the inductor value, output capacitance, load current, V_{IN}, V_{OUT} and the V_C resistor and capacitors. The LT8708 uses internal transconductance error amplifiers driving V_C to help compensate the control loop. For most applications a 3.3nF series capacitor at V_C is a good value. The parallel capacitor (from V_C to GND) is typically 1/10th the value of the series capacitor to filter high frequency noise. A larger V_C series capacitor value may be necessary if the output capacitance is reduced. A good starting value for the V_C series resistor is 20k. Lower resistance will improve stability but will slow the loop response. Use a trim pot instead of a fixed resistor for initial bench evaluation to determine the optimum value.

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Also note that C_{IMON_INP} and C_{IMON_INN} capacitors of at least a few nF are necessary to maintain loop stability when IMON_INP and IMON_INN, respectively, are used to operate the LT8708 at constant current limit.

$INTV_{CC}$ REGULATORS AND $EXTV_{CC}$ CONNECTION

The LT8708 features two PNP LDOs (low dropout regulators) that regulate the 6.35V (typical) $INTV_{CC}$ pin from either the V_{INCHIP} or $EXTV_{CC}$ supply pin. $INTV_{CC}$ powers the MOSFET gate drivers via the required $GATEV_{CC}$ connection and also powers the LDO33 pin regulator and much of the LT8708's internal control circuitry. The $INTV_{CC}$ LDO selection is determined automatically by the $EXTV_{CC}$ pin voltage. When $EXTV_{CC}$ is lower than 6.2V (typical), $INTV_{CC}$ is regulated from the V_{INCHIP} pin LDO. After $EXTV_{CC}$ rises above 6.4V (typical), $INTV_{CC}$ is regulated by the $EXTV_{CC}$ pin LDO instead.

Overcurrent protection circuitry typically limits the maximum current draw from either LDO to 127mA. When $GATEV_{CC}$ and $INTV_{CC}$ are below 4.65V, during start-up or during an overload condition, the typical current limit is reduced to 42mA. The $INTV_{CC}$ pin must be bypassed to ground with a minimum 4.7µF ceramic capacitor placed as close as possible to the $INTV_{CC}$ and GND pins. An additional ceramic capacitor should be placed as close as possible to the $GATEV_{CC}$ and GND pins to provide good bypassing to supply the high transient current required by the MOSFET gate drivers. 1µF to 4.7µF is recommended.

Power dissipated in the $INTV_{CC}$ LDOs must be minimized to improve efficiency and prevent overheating of the LT8708. Since LDO power dissipation is proportional to the supply voltage and V_{INCHIP} can be as high as 80V in some applications, the $EXTV_{CC}$ pin is available to regulate $INTV_{CC}$ from a lower supply voltage. The $EXTV_{CC}$ pin is connected to V_{OUT} in many applications since V_{OUT} is often regulated to a much lower voltage than the maximum V_{INCHIP}. During start-up, power for the MOSFET drivers, control circuits and the LDO33 pin is usually derived from V_{INCHIP} until V_{OUT}/$EXTV_{CC}$ rises above 6.4V, after which the power is derived from V_{OUT}/$EXTV_{CC}$. This works well, for example, in a case where V_{OUT} is regulated to 12V and the maximum V_{INCHIP} voltage is 40V. $EXTV_{CC}$ can be floated or grounded when not in use or can also be connected to an external power supply if available.

The following list summarizes the three possible connections for $EXTV_{CC}$:

1. $EXTV_{CC}$ left open (or grounded). This will cause $INTV_{CC}$ to be powered from V_{INCHIP} through the internal 6.3V regulator at the cost of a small efficiency penalty.
2. $EXTV_{CC}$ connected directly to V_{OUT} (V_{OUT} > 6.4V). This is the normal connection for the regulator and usually provides the highest efficiency.
3. $EXTV_{CC}$ connected to an external supply. If an external supply is available greater than 6.4V (typical) it may be used to power $EXTV_{CC}$.

Powering $INTV_{CC}$ from $EXTV_{CC}$ can also provide enough gate drive when V_{INCHIP} drops as low as 2.8V. This allows the part to operate with a reduced V_{INCHIP} voltage after V_{OUT} gets into regulation.

The maximum current drawn through the $INTV_{CC}$ LDO occurs under the following conditions:

1. Large (capacitive) MOSFETs are being driven at high frequencies.
2. V_{IN} and/or V_{OUT} is high, thus requiring more charge to turn the MOSFET gates on and off.
3. The LDO33 pin output current is high.
4. In some applications, LDO current draw is maximum when the part is operating in the buck-boost region where V_{IN} is close to V_{OUT} since all four MOSFETs are switching.

To check for overheating find the operating conditions that consume the most power in the LT8708 (P_{LT8708}). This will often be under the same conditions just listed that maximize LDO current. Under these conditions monitor the CLKOUT pin duty cycle to measure the approximate die temperature. See the Junction Temperature Measurement section for more information.

LDO33 REGULATOR

The LT8708 includes a low dropout regulator (LDO) to regulate the LDO33 pin to 3.3V. This pin can be used to power external circuitry such as a microcontroller or other desired peripherals. The input supply for the LDO33 pin regulator is $INTV_{CC}$. Therefore $INTV_{CC}$ must have sufficient

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voltage, typically > 4.0V, to properly regulate LDO33. The LDO33 and $INTV_{CC}$ regulators are enabled by the $\overline{SHDN}$ pin and are not affected by SWEN. The LDO33 pin regulator has overcurrent protection circuitry that typically limits the output current to 17.25mA. An undervoltage lockout monitors LDO33 and disables switching activity when LDO33 falls below 3.04V (typical). LDO33 should be bypassed locally with 0.1µF or more.

VOLTAGE LOCKOUTS

The LT8708 contains several voltage detectors to make sure the chip is under proper operating conditions. Table 8 summarizes the pins that are monitored and also indicates the state that the LT8708 will enter if an under or over voltage condition is detected.

Table 8. Voltage Lockout Conditions

PIN(S)	APPROXIMATE VOLTAGE CONDITION	CHIP STATE (Figure 2)	READ SECTION
V_{INCHIP}	<2.5V	CHIP OFF	Operation: Start-Up
$\overline{SHDN}$	<1.18V		
$INTV_{CC}$ and $GATEV_{CC}$	<4.65V	SWITCHER OFF 1	
SWEN	<1.18V		
LDO33	<3.04V		
VINHIMON	>1.207V	–	Applications Information: VINHIMON, VOUTLOMON and $\overline{RVSOFF}$
VOUTLOMON	<1.207V		
$\overline{RVSOFF}$	<1.209V		
FBIN	<1.205V		Voltage Lockouts

The conditions are listed in order of priority from top to bottom. If multiple over/undervoltage conditions are detected, the chip will enter the state listed highest on the table.

Due to their accurate thresholds, configurable undervoltage lockouts (UVLOs) can be implemented using the $\overline{SHDN}$ and SWEN and in some cases, FBIN pin. The UVLO function sets the turn on/off of the LT8708 at a desired minimum voltage. For example, a resistor divider can be connected between V_{IN}, $\overline{SHDN}$ and GND as shown in Figure 1. From the Electrical Characteristics, $\overline{SHDN}$ has typical rising and falling thresholds of 1.221V and 1.181V, respectively. The falling threshold for turning-off switching activity can be chosen using:

$$R_{SHDN1} = \frac{R_{SHDN2} \bullet (V_{(IN,CHIPOFF,FALLING)} - 1.181)}{1.181} \Omega$$

For example, choosing R_{SHDN2} = 20k and a falling V_{IN} threshold of 5.42V results in:

$$R_{SHDN1} = \frac{20k \bullet (5.42 - 1.181)}{1.181} \cong 71.5k\Omega$$

The rising threshold for enabling switching activity would be:

$$V_{(IN,CHIPOFF,RISING)} = V_{(IN,CHIPOFF,FALLING)} \bullet \frac{1.221}{1.181}$$

or 5.6V in this example.

Similar calculations can be used to select a resistor divider connected to SWEN that would stop switching activity during an undervoltage condition. Make sure that the divider doesn't cause SWEN to exceed 7V (ABSMAX rating) under maximum supply voltage conditions. See the Start-Up: SWEN Pin section for additional information.

The same technique described in the V_{IN}: Regulation section can be used to create an undervoltage lockout if the LT8708 is in forward non-CCM mode, where forcing V_C low will stop all switching activity. Note that this does not reset the soft-start function, therefore resumption of switching activity will not be accompanied by a soft-start.

JUNCTION TEMPERATURE MEASUREMENT

The duty cycle of the CLKOUT signal is linearly proportional to the die junction temperature, T_J. Measure the duty cycle of the CLKOUT signal and use the following equation to approximate the junction temperature:

$$T_J \cong \frac{DC_{CLKOUT} - 34.4\%}{0.325\%} °C$$

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where DC_{CLKOUT} is the CLKOUT duty cycle in % and T_J is the die junction temperature in °C. The actual die temperature can deviate from the above equation by ±10°C.

THERMAL SHUTDOWN

If the die junction temperature reaches approximately 165°C, the part will go into thermal shutdown. The power switches will be turned off and the $INTV_{CC}$ and LDO33 regulators will be turned off (see Figure 2). The part will be re-enabled when the die temperature has dropped by ~5°C (nominal). After re-enabling, the part will start in the SWITCHER OFF 1 state as shown in Figure 2. The part will then INITIALIZE, perform a SOFT-START, then enter NORMAL OPERATION as long as the die temperature remains below approximately 165°C.

EFFICIENCY CONSIDERATIONS

The efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Although all dissipative elements in the circuit produce losses, three main sources account for most of the losses in LT8708 circuits. These and a few additional loss components are listed below:

1. Switching losses. These losses arise from the brief amount of time the switches (M1 – M4) spend in the saturated region during switch node transitions. Power loss depends upon the input voltage, load current, driver strength and MOSFET capacitance, among other factors. See the Power MOSFET Selection section for more details.
2. DC I^2R losses. These arise from the resistances of the MOSFETs (M1 – M4), sensing resistors, inductor and PC board traces and cause the efficiency to drop at high currents.
3. $INTV_{CC}$ current. This is the sum of the MOSFET driver current, LDO33 pin current and control currents. The $INTV_{CC}$ regulator's input voltage times the current represents lost power. This loss can be reduced by supplying $INTV_{CC}$ current through the $EXTV_{CC}$ pin from a high efficiency source, such as the output or alternate supply if available. Also, lower capacitance MOSFETs can reduce $INTV_{CC}$ current and power loss.
4. C_{IN} and C_{OUT} loss. The C_{IN} capacitor has the difficult job of filtering the large RMS input current to the regulator in buck mode. The C_{OUT} capacitor has the more difficult job of filtering the large RMS output current in boost mode. Both C_{IN} and C_{OUT} are required to have low ESR to minimize the AC I^2R loss and have sufficient capacitance to prevent the RMS current from causing additional upstream losses in fuses or batteries.
5. Other losses. Schottky diodes D1, D2, D3 and D4 are responsible for conduction losses during dead time and light load conduction periods. Inductor core loss occurs predominately at light loads.

Hybrid conduction mode (HCM) can be used to improve the efficiency when large inductor current ripples are present in DCM. See the Unidirectional Conduction: HCM section for details.

When making adjustments to improve efficiency, the input current is the best indicator of changes in efficiency. If one makes a change and the input current decreases, then the efficiency has increased. If there is no change in input current, then there is no change in efficiency.

CIRCUIT BOARD LAYOUT CHECKLIST

The basic circuit board layout requires a dedicated ground plane layer. Also, for high current, a multilayer board provides heat sinking for power components.

- The ground plane layer should not have any traces and should be as close as possible to the layer with the power MOSFETs.
- The high di/dt path formed by switch M1, switch M2, D1, R_{SENSE} and the C_{IN} capacitor should be compact with short leads and PC trace lengths. The high di/dt path formed by switch M3, switch M4, D2 and the C_{OUT} capacitor also should be compact with short leads and PC trace lengths. Two layout examples are shown in Figure 18 (a) and (b).

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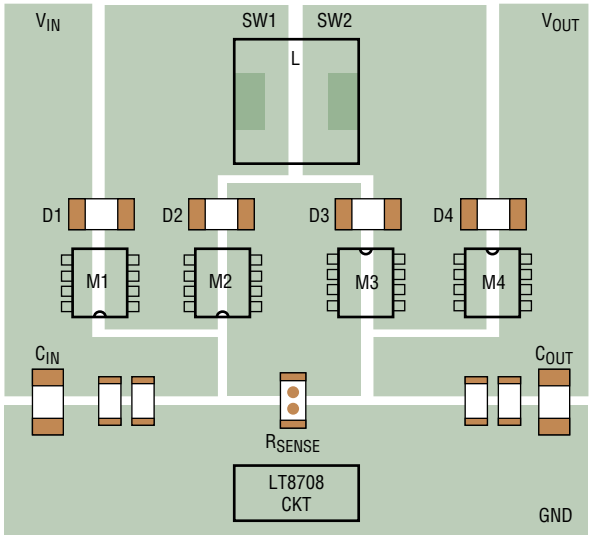
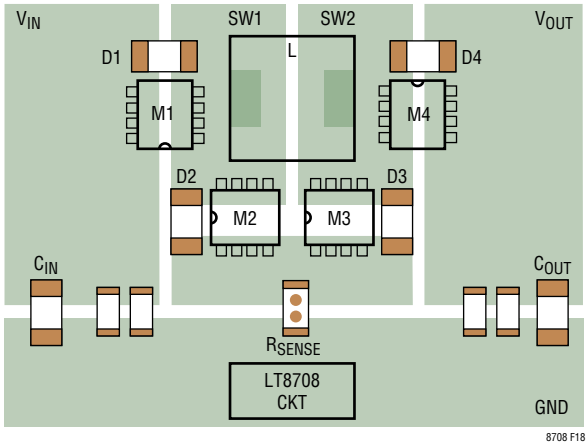


18(a)



18(b)

Figure 18. Switches Layout

- Avoid running signal traces parallel to the traces that carry high di/dt current because they can receive inductively coupled voltage noise. This includes the SW1, SW2, TG1 and TG2 traces to the controller.
- Use immediate vias to connect the components (including the LT8708's GND pins) to the ground plane. Use several vias for each power component.
- Minimize parasitic SW pin capacitance by removing GND, V_{IN} and V_{OUT} copper from underneath the SW1 and SW2 regions.
- Except under the SW pin regions, flood all unused areas on all layers with copper. Flooding with copper will reduce the temperature rise of power components. Connect the copper areas to a DC net (i.e., quiet GND) with many vias. The more vias the board has, the better heat conduction it has.
- Partition the power ground from the signal ground. The small-signal component grounds should not return to the IC GND through the power ground path.
- Place switch M2 and switch M3 as close to the controller as possible, keeping the GND, BG and SW traces short.
- Minimize inductance from the sources of M2 and M3 to R_{SENSE} by making the trace short and wide.
- Keep the high dv/dt nodes SW1, SW2, BOOST1, BOOST2, TG1 and TG2 away from sensitive small-signal nodes.
- The output capacitor (–) terminals should be connected as closely as possible to the (–) terminals of the input capacitor.
- Connect the top driver boost capacitor C_{B1} closely to the BOOST1 and SW1 pins. Connect the top driver boost capacitor C_{B2} closely to the BOOST2 and SW2 pins.
- Connect the C_{IN} and C_{OUT} capacitors closely to the power MOSFETs. These capacitors carry the MOSFET AC current in the boost and buck regions.
- Connect the FBOUT, FBIN, VINHIMON and VOUTLOMON pin resistor dividers to the (+) terminals of C_{OUT} and C_{IN}, respectively. Small FBOUT/FBIN/VINHIMON/VOUTLOMON bypass capacitors may be connected closely to the LT8708's GND pin if needed. The resistor connections should not be along the high current or noise paths.
- Route current sense traces (CSP/CSN, CSPIN/CSNIN, CSPOUT/CSNOUT) together with minimum PC trace

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spacing. Avoid having sense lines pass through noisy areas, such as switch nodes. The optional filter network capacitor between CSP and CSN should be as close as possible to the IC. Ensure accurate current sensing with Kelvin connections at the R_{SENSE} resistors.

- Connect the V_C pin compensation network closely to the IC, between V_C and the signal ground pins. The capacitor helps to filter the effects of PCB noise and output voltage ripple voltage from the compensation loop.
- Connect the $INTV_{CC}$ and $GATEV_{CC}$ bypass capacitors close to the IC. The capacitors carry the MOSFET drivers' current peaks.
- Run the trace from the LT8708's SW1/SW2 pin to the drain of M2/M3 in parallel with the trace from the $GATEV_{CC}$ capacitor's GND to the C_{IN} GND. Route the traces (as much as possible) directly above/below one another on adjacent layers and in such a way that they carry currents in opposite directions.
- Attention is required when making the PCB layout for R_{SENSE1} and R_{SENSE2}, especially for sense resistor values smaller than 5mΩ. Improper PCB layout can yield significant errors in the sense voltage.

HOT PLUGGING CONSIDERATIONS

When connecting a battery to an LT8708 application, there can be significant inrush current due to charge equalization between the partially charged battery stack and the charger output capacitors. To a lesser extent a similar effect can occur when connecting a powered DC supply to the input or output. The magnitude of the inrush current depends on (1) the battery or supply voltage, (2) ESR of the input or output capacitors, (3) initial voltage of the capacitors, and (4) cable impedance. Excessive inrush current can lead to sparking that can compromise connector integrity and/or voltage overshoot that can cause electrical overstress on LT8708 pins.

Excessive inrush current can be mitigated by first connecting the battery or supply to the charger through a resistive path, followed quickly by a short circuit. This can be accomplished using staggered length pins in a multi-pin connector. Alternatively, consider the use of a Hot Swap controller such as the LT1641, LT4256, etc. to make a current limited connection.

DESIGN EXAMPLE

V_{IN} = 8V to 25V

V_{IN_FBIN} = 12V (V_{IN} regulation voltage set by FBIN loop)

V_{OUT_FBOUT} = 12V (V_{OUT} regulation voltage set by FBOUT loop)

$I_{OUT(MAX,FWD)}$ = 5A

$I_{IN(MAX,RVS)}$ = 3A

f = 150kHz

This design operates in CCM.

Maximum ambient temperature = 60°C

Power Flow Verification: Determine which conditions in Table 6(a) apply to this application. In this design example, the VINHIMON and VOUTLOMON are disabled, therefore the conditions highlighted in blue in the copy of Table 6(a) apply to this application.

Table 9. A Copy of Table 6(a)

	$V_{OUT} < V_{OUT\_VOUTLOMON}$	$V_{OUT} > V_{OUT\_VOUTLOMON}$ & $V_{OUT} < V_{OUT\_FBOUT}$	$V_{OUT} > V_{OUT\_FBOUT}$
$V_{IN} < V_{IN\_FBIN}$	No Power Transfer	B	B
$V_{IN} > V_{IN\_FBIN}$ & $V_{IN} < V_{IN\_VINHIMON}$	A	D	C
$V_{IN} > V_{IN\_VINHIMON}$	A	D	No Power Transfer

Next, check each of these highlighted cells using Table 6(b) with MODE = CCM. A copy of Table 6(b) is shown below:

9(b). A Copy of Table 6(b)

	MODE = BURST	MODE = CCM	MODE = DCM/HCM, DIR = FWD	MODE = DCM/HCM, DIR = RVS
A	Power Flows from V_{IN} to V_{OUT}			No Power Flow
B	No Power Flow	Power Flows from V_{OUT} to V_{IN}	No Power Flow	Power Flows from V_{OUT} to V_{IN}
C				No Power Flow
D	Power Flows from V_{IN} to V_{OUT}			

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Verify expected operation by combining Table 6(a) and Table 6(b):

- When $V_{IN} < V_{IN\_FBIN}$ (12V) and $V_{OUT} > V_{OUT\_FBOUT}$ (12V)
  B – power is transferred from V_{OUT} to V_{IN}
- When $V_{IN} < V_{IN\_FBIN}$ (12V) and $V_{OUT} < V_{OUT\_FBOUT}$ (12V)
  B – power is transferred from V_{OUT} to V_{IN}
- When $V_{IN} > V_{IN\_FBIN}$ (12V) and $V_{OUT} > V_{OUT\_FBOUT}$ (12V)
  C – power is transferred from V_{OUT} to V_{IN}
- When $V_{IN} > V_{IN\_FBIN}$ (12V) and VOUT $< V_{OUT\_FBOUT}$ (12V)
  D – power is transferred from V_{IN} to V_{OUT}

The results above are as expected for this design example.

R_T Selection: Choose the R_T resistor for the free-running oscillator frequency using:

$$R_T = \left(\frac{43{,}750}{f_{OSC}} - 1\right)k\Omega = \left(\frac{43{,}750}{150} - 1\right) = 290.7k\Omega$$

We will choose 294k for R_T resistor.

R_{SENSE} Selection: Start by calculating the maximum and minimum duty cycle in the boost region:

$$DC_{(MAX,M3,BOOST)} \cong \left(1 - \frac{V_{IN(MIN,BOOST)}}{V_{OUT(MAX,BOOST)}}\right) \bullet 100\%$$

$$= \left(1 - \frac{8V}{12V}\right) \bullet 100\% = 33\%$$

$$DC_{(ABSMIN,M3,BOOST)} \cong t_{ON(M3,MIN)} \bullet f \bullet 100\%$$

$$= 200ns \bullet 150kHz \bullet 100\% = 3\%$$

Next, from the Maximum Inductor Current Sense Voltage vs Duty Cycle graph in the Typical Performance Characteristics section:

$$V_{RSENSE(MAX,BOOST,MAXDC)} \cong 83mV$$

$$V_{RSENSE(MIN,BOOST,MINDC)} \cong 93mV$$

Next, estimate the inductor current ripples at maximum and minimum boost duty cycles:

$$\Delta I_{L(MAX,BOOST)} \cong \frac{V_{OUT(MAX,BOOST)} \bullet I_{OUT(MAX,FWD)}}{V_{IN(MIN,BOOST)} \bullet \left(\frac{100\%}{\%Ripple} - 0.5\right)} A$$

$$= \frac{12V \bullet 5A}{8V \bullet \left(\frac{100\%}{40\%} - 0.5\right)} = 3.75A$$

$$\Delta I_{L(MIN,BOOST)} \cong \frac{I_{IN(MAX,RVS)}}{\left(\frac{100\%}{10\%} - 0.5\right)} A$$

$$= \frac{3A}{\left(\frac{100\%}{10\%} - 0.5\right)} = 0.32A$$

Now calculate the maximum R_{SENSE} values in the boost region:

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$$R_{SENSE(MAX,BOOST,FWD)} = \frac{2 \bullet V_{RSENSE(MAX,BOOST,MAXDC)} \bullet V_{IN(MIN,BOOST)}}{\left(2 \bullet I_{OUT(MAX,FWD)} \bullet V_{OUT(MAX,BOOST)}\right) + \left(\Delta I_{L(MAX,BOOST)} \bullet V_{IN(MIN,BOOST)}\right)} \Omega$$

$$= \frac{2 \bullet 83mV \bullet 8V}{(2 \bullet 5A \bullet 12V) + (3.75A \bullet 8V)} = 8.85m\Omega$$

$$R_{SENSE(MAX,BOOST,RVS)} = \frac{2 \bullet |V_{RSENSE(MIN,BOOST,MINDC)}|}{\left(2 \bullet |I_{IN(MAX,RVS)}|\right) - \Delta I_{L(MIN,BOOST)}} \Omega$$

$$= \frac{2 \bullet 93mV}{(2 \bullet 3A) - 0.32A} = 32.7m\Omega$$

Next, calculate the maximum and minimum duty cycle in the buck region:

$$DC_{(ABSMIN,M2,BUCK)} \cong t_{ON(M2,MIN)} \bullet f \bullet 100\%$$

$$= 200ns \bullet 150kHz \bullet 100\% = 3\%$$

$$DC_{(MAX,M2,BUCK)} \cong \left(1 - \frac{V_{OUT(MIN,BUCK)}}{V_{IN(MAX,BUCK)}}\right) \bullet 100\%$$

$$= \left(1 - \frac{12V}{25V}\right) \bullet 100\% = 52\%$$

Next, from the Maximum Inductor Current Sense Voltage vs Duty Cycle graph in the Typical Performance Characteristics section:

$$V_{RSENSE(MAX,BUCK,MINDC)} \cong 100mV$$

$$V_{RSENSE(MIN,BUCK,MAXDC)} \cong 82mV$$

Next, estimate the inductor current ripples at maximum and minimum buck duty cycles:

$$\Delta I_{L(MIN,BUCK)} \cong \frac{I_{OUT(MAX,FWD)}}{\left(\frac{100\%}{10\%} - 0.5\right)} A = \frac{5A}{\left(\frac{100\%}{10\%} - 0.5\right)}$$

$$= 0.526A$$

$$\Delta I_{L(MAX,BUCK)} \cong \frac{V_{IN(MAX,BUCK)} \bullet I_{IN(MAX,RVS)}}{V_{OUT(MIN,BUCK)} \bullet \left(\frac{100\%}{\%Ripple} - 0.5\right)} A$$

$$= \frac{25V \bullet 3A}{12V \bullet \left(\frac{100\%}{40\%} - 0.5\right)} = 3.125A$$

Now calculate the maximum R_{SENSE} values in the buck region:

$$R_{SENSE(MAX,BUCK,FWD)} = \frac{2 \bullet V_{RSENSE(MAX,BUCK,MINDC)}}{\left(2 \bullet I_{OUT(MAX,FWD)}\right) - \Delta I_{L(MIN,BUCK)}} \Omega$$

$$= \frac{2 \bullet 100mV}{(2 \bullet 5A) - 0.53A} = 21.1m\Omega$$

$$R_{SENSE(MAX,BUCK,RVS)} = \frac{2 \bullet |V_{RSENSE(MIN,BUCK,MAXDC)}| \bullet V_{OUT(MIN,BUCK)}}{\left(2 \bullet |I_{IN(MAX,RVS)}| \bullet V_{IN(MAX,BUCK)}\right) + \left(\Delta I_{L(MAX,BUCK)} \bullet V_{OUT(MIN,BUCK)}\right)} \Omega$$

$$= \frac{2 \bullet 82mV \bullet 12V}{(2 \bullet 3A \bullet 25V) + (3.125A \bullet 12V)} = 10.5m\Omega$$

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Choose the smallest calculated R_{SENSE} and add an additional 30% margin, choose R_{SENSE} to be 10.5mΩ/1.3 = 8.1mΩ

Inductor Selection: With R_{SENSE} known, we can now determine the minimum inductor value that will provide adequate load current in the boost region using:

$$L_{(MIN1,BOOST)} \cong \frac{V_{IN(MIN,BOOST)} \bullet \left(\frac{DC_{(MAX,M3,BOOST)}}{100\%}\right)}{2 \bullet f \bullet \left(\frac{V_{RSENSE(MAX,BOOST,MAXDC)}}{R_{SENSE}} - \frac{I_{OUT(MAX,BOOST)} \bullet V_{OUT(MAX,BOOST)}}{V_{IN(MIN,BOOST)}}\right)} H$$

$$= \frac{8V \bullet \left(\frac{33\%}{100\%}\right)}{2 \bullet 150kHz \bullet \left(\frac{83mV}{8.1m\Omega} - \frac{5A \bullet 12V}{8V}\right)} = 3.2\mu H$$

To avoid subharmonic oscillations in the inductor current, choose the minimum inductance according to:

$$L_{(MIN2,BOOST)} = \frac{\left[V_{OUT(MAX,BOOST)} - \left(\frac{V_{IN(MIN,BOOST)} \bullet V_{OUT(MAX,BOOST)}}{V_{OUT(MAX,BOOST)} - V_{IN(MIN,BOOST)}}\right)\right] \bullet R_{SENSE}}{0.08 \bullet f} H$$

$$= \frac{\left[12V - \left(\frac{8V \bullet 12V}{12V - 8V}\right)\right] \bullet 8.1m\Omega}{0.08 \bullet 150kHz} = -8.1\mu H$$

$$L_{(MIN1,BUCK)} = \frac{\left[V_{IN(MAX,BUCK)}\left(1 - \frac{V_{OUT(MAX,BUCK)}}{V_{IN(MAX,BUCK)} - V_{OUT(MIN,BUCK)}}\right)\right] \bullet R_{SENSE}}{0.08 \bullet f} H$$

$$= \frac{\left[25V \bullet \left(1 - \frac{12V}{25V - 12V}\right)\right] \bullet 8.1m\Omega}{0.08 \bullet 150kHz} = 1.3\mu H$$

The inductance must be higher than all of the minimum values calculated above. We will choose a 10µH standard value inductor for improved margin.

MOSFET Selection: The MOSFETs are selected based on voltage rating, C_{OSS} and $R_{DS(ON)}$ value. It is important to ensure that the part is specified for operation with the available gate voltage amplitude. In this case, the amplitude is 6.3V and MOSFETs with an $R_{DS(ON)}$ value specified at V_{GS} = 4.5V can be used.

Select M1 and M2: With 25V maximum input voltage, MOSFETs with a rating of at least 30V are used. As we do not yet know the actual thermal resistance (circuit board design and airflow have a major impact) we assume that the MOSFET thermal resistance from junction to ambient is 50°C/W.

If we design for a maximum junction temperature, $T_{J(MAX)}$ = 125°C, the maximum allowable power dissipation can be calculated. First, calculate the maximum power dissipation:

$$PD_{(MAX)} = \frac{T_{J(MAX)} - T_{A(MAX)}}{R_{TH(JA)}}$$

$$PD_{(MAX)} = \frac{125°C - 60°C}{50\frac{°C}{W}} = 1.3W$$

Since maximum I^2R power in the boost region with positive inductor current happens when V_{IN} is minimum, we can determine the maximum allowable $R_{DS(ON)}$ for the boost region using (see Table 7):

$$PM1 = P_I{}^2{}_R \cong \left[\left(\frac{V_{OUT}}{V_{IN}} \bullet I_{OUT(MAX,FWD)}\right)^2 \bullet R_{DS(ON)} \bullet \rho_\tau\right] W$$

and therefore

$$R_{DS(ON)} < \frac{13W}{\left[\left(\frac{12V}{8V} \bullet 5A\right]^2 \bullet 1.5\right)} = 15.4m\Omega$$

The Fairchild FDMS7672 meets the specifications with a maximum $R_{DS(ON)}$ of ~6.9mΩ at V_{GS} = 4.5V (~10mΩ at 125°C).

The maximum dissipation in M2 occurs at maximum V_{IN} voltage when the circuit is operating in the buck region

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in the reverse direction. Using the 6.9mΩ Fairchild FDMS7672, the dissipation is (see Table 7):

$$P_{M2} \cong I^2R + P_{SWITCHING}$$

$$\cong \left(\frac{V_{IN} - V_{OUT}}{V_{IN}} \bullet I_{OUT(MAX,RVS)}^2 \bullet R_{DS(ON)} \bullet \rho_\tau \right)$$

$$+ \left(V_{IN} \bullet I_{OUT(MAX,RVS)} \bullet f \bullet t_{RF1} \right)$$

$$+ \left(0.5 \bullet C_{OSS(M1+M2)} \bullet V_{IN}^2 \bullet f \right) W$$

$$P_{(M2,MAX)} \cong$$

$$\left(\frac{25V - 12V}{25V} \bullet (3A)^2 \bullet 6.9m\Omega \bullet 1.5 \right)$$

$$+ (25V \bullet 3A \bullet 150kHz \bullet 20ns)$$

$$+ [(0.5 \bullet (685P + 685P) \bullet 25V \bullet 25V \bullet 150k)]$$

$$= 0.13W + 0.225W + 0.064W = 0.419W$$

To check the power dissipation in the buck region with V_{IN} maximum and V_{OUT} minimum, choose the equation from Table 7 with positive inductor current in buck mode which yields:

$$P_{M1} \cong I^2R + P_{SWITCHING}$$

$$\cong \left[\left(\frac{V_{OUT}}{V_{IN}} \bullet I_{OUT(MAX,FWD)} \right)^2 \bullet R_{DS(ON)} \bullet \rho_\tau \right]$$

$$+ \left(V_{IN} \bullet I_{OUT(MAX,FWD)} \bullet f \bullet t_{RF1} \right)$$

$$+ \left(0.5 \bullet C_{OSS(M1+M2)} \bullet V_{IN}^2 \bullet f \right) W$$

$$P_{(M1,MAX)} \cong$$

$$\left[\left(\frac{12V}{25V} \bullet 5A \right)^2 \bullet 6.9m\Omega \bullet 1.5 \right]$$

$$+ (25V \bullet 5A \bullet 150k \bullet 20ns)$$

$$+ [(0.5 \bullet (685P + 685P) \bullet 25V \bullet 25V \bullet 150k)]$$

$$= 0.06W + 0.38W + 0.064W = 0.504W$$

The maximum switching power of 0.38W can be reduced by choosing a slower switching frequency. Since this calculation is approximate, measure the actual rise and fall times on the PCB to obtain a better power estimate.

Select M3 and M4: With 12V output voltage we need MOSFETs with 20V or higher rating.

The highest dissipation of M3 and M4 occurs in the boost region. For switch M3, the max dissipation occurs when the I_{OUT} is highest in the forward direction and V_{IN} is at the minimum 8V (see Table 7):

$$P_{M3} \cong I^2R + P_{SWITCHING}$$

$$\cong \left(\frac{(V_{OUT} - V_{IN}) \bullet V_{OUT}}{V_{IN}^2} \bullet I_{OUT(MAX,FWD)}^2 \bullet R_{DS(ON)} \bullet \rho_\tau \right)$$

$$+ \left(V_{OUT}^2 \bullet I_{OUT(MAX,FWD)} \bullet f \bullet \frac{t_{RF2}}{V_{IN}} \right)$$

$$+ \left(0.5 \bullet C_{OSS(M3+M4)} \bullet V_{OUT}^2 \bullet f \right) W$$

For switch M4, the max dissipation occurs when the I_{IN} is highest in the reverse direction and V_{IN} is highest in the boost region (see Table 7):

$$P_{M4} \cong I^2R + P_{SWITCHING}$$

$$\cong \left(\frac{V_{IN}}{V_{OUT}} \bullet I_{IN(MAX,RVS)}^2 \bullet R_{DS(ON)} \bullet \rho_\tau \right)$$

$$+ \left(V_{OUT} \bullet I_{IN(MAX,RVS)} \bullet f \bullet t_{RF2} \right)$$

$$+ \left(0.5 \bullet C_{OSS(M3+M4)} \bullet V_{OUT}^2 \bullet f \right) W$$

and

$$\frac{V_{IN(MAX,BOOST)}}{V_{OUT(MAX,BOOST)}} = 1 - DC_{(ABSMIN,M3,BOOST)}$$

therefore,

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$$P_{M4} \cong P_{I^2R} + P_{SWITCHING}$$
$$= \left[(1-DC_{(ABSMIN,M3,BOOST)}) \bullet I_{IN(MAX,RVS)}{}^2 \bullet R_{DS(ON)} \bullet \rho_{\tau}\right]$$
$$+\left(V_{OUT} \bullet I_{IN(MAX,RVS)} \bullet f \bullet t_{RF2}\right)$$
$$+\left(0.5 \bullet C_{OSS(M3+M4)} \bullet V_{OUT}{}^2 \bullet f\right) W$$

The Fairchild FDMS7672 can also be used for M3 and M4. Assuming 20ns rise and fall times, the calculated power loss is then 0.48W for M3 and 0.21W for M4.

Select R_{SENSE2}, R_{IMON_OP} and R_{IMON_ON}: The $I_{OUT(MAX,FWD)}$ = 5A and $I_{IN(MAX,RVS)}$ = 3A, with a 20% margin, the I_{OUT} current limit is set to 6A in the forward and the I_{IN} current limit is set to 3.6A in the reverse directions, respectively.

Choose R_{IMON_OP} to be 17.4k, so that the $V_{CSPOUT-CSNOUT}$ limit becomes 50mV, and the R_{SENSE2} is calculated to be:

$$R_{SENSE2} = \frac{50mV}{6A} \cong 8m\Omega$$

Using the equation given in the I_{IN} and I_{OUT} Current Monitoring and Limiting section, R_{IMON_ON} is calculated to be:

$$R_{IMON\_ON} = \frac{1.21}{I_{(OUT,RVS,LIMIT)} \bullet 1m\frac{A}{V} \bullet R_{SENSE2} + 20\mu A}\Omega$$
$$= \frac{1.21}{3.6A \bullet 1m\frac{A}{V} \bullet 8m\Omega + 20\mu A} = 24.9k\Omega$$

V_{OUT} Voltage: V_{OUT} voltage is 12V. Select R_{FBOUT2} as 20k. R_{FBOUT1} is:

$$R_{FBOUT1} = \left(\frac{V_{OUT}}{1.207V} - 1\right) \bullet R_{FBOUT2}$$

Select R_{FBOUT1} as 178k. Both R_{FBOUT1} and R_{FBOUT2} should have a tolerance of no more than 1%.

V_{IN} Voltage: Input voltage is 12V. Select R_{FBIN2} as 20k. R_{FBIN1} is:

$$R_{FBIN1} = \left(\frac{V_{IN}}{1.207V} - 1\right) \bullet R_{FBIN2}$$

Select R_{FBIN1} as 178k. Both R_{FBIN1} and R_{FBIN2} should have a tolerance of no more than 1%.

Capacitors: A low ESR (5mΩ) capacitor network with 30µF ceramic capacitors for C_{IN} is selected. In this mode, the maximum ripple is:

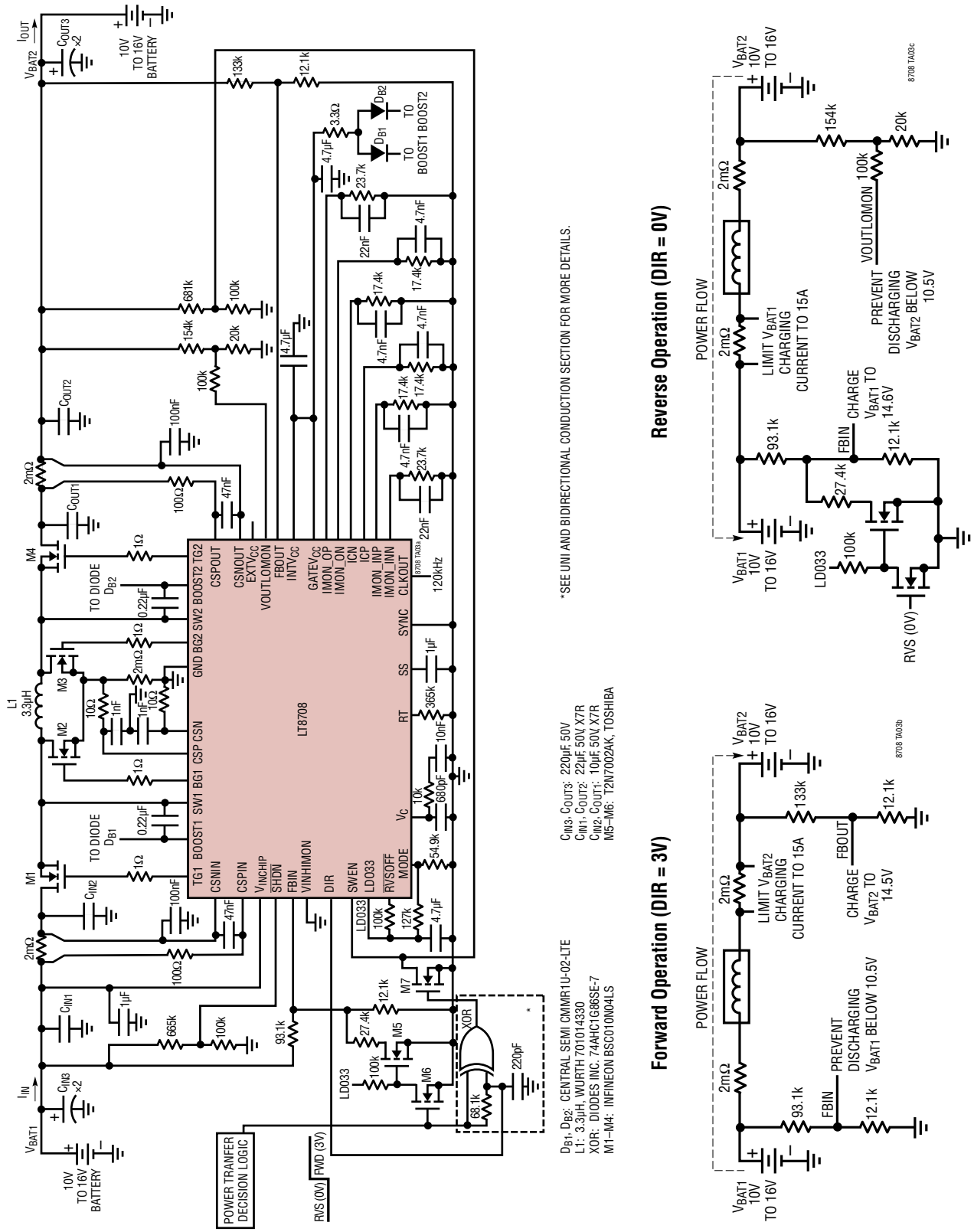
$$\Delta V_{(BUCK,CAP)} \cong$$
$$I_{OUT(MAX,FWD)} \bullet \frac{V_{OUT}}{V_{IN}} \bullet ESR_{CERAM} \bullet$$
$$\left(1 - \exp\left(\frac{-V_{OUT}}{V_{IN} \bullet f \bullet ESR_{CERAM} \bullet C_{IN-CERAM}}\right)\right)$$
$$\cong 5A \bullet \frac{12V}{24V} \bullet 5m\Omega$$
$$\bullet \left(1 - \exp\left(\frac{-12V}{24V \bullet 150kHz \bullet 5m\Omega \bullet 30\mu F}\right)\right)$$
$$= 12.5mV$$

Having 5mΩ of ESR with 66µF ceramic capacitor for the C_{OUT} network sets the maximum output voltage ripple at:

$$\Delta V_{(Boost,CAP)} \cong$$
$$I_{OUT(MAX,FWD)} \bullet ESR_{CERAM} \bullet$$
$$\left(1 - \exp\left(\frac{V_{IN} - V_{OUT}}{V_{OUT} \bullet f \bullet ESR_{CERAM} \bullet C_{OUT-CERAM}}\right)\right)$$
$$\cong 5A \bullet 5m\Omega$$
$$\bullet \left(1 - \exp\left(\frac{8V - 12V}{12V \bullet 150kHz \bullet 5m\Omega \bullet 66\mu F}\right)\right)$$
$$= 25mV$$

TYPICAL APPLICATIONS

12V Bidirectional Dual Battery System with FHCM & RHCM



APPLICATIONS INFORMATION

12V Bidirectional Dual Battery System with FHCM & RHCM Details

V_{BAT1} Charge Voltage = 14.6V (FBIN in RHCM)

V_{BAT2} Charge Voltage = 14.5V (FBOUT in FHCM)

V_{BAT1_DEAD} = 9V (Falling) or 9.4V (Rising)

V_{BAT2_DEAD} = 9.25V (Falling) or 9.4V (Rising)

V_{BAT1_UV} to Stop Discharging = 10.5V (FBIN in FHCM)

V_{BAT2_UV} to Stop Discharging = 10.5V (VOUTLOMON Falling) or 11.7V (VOUTLOMON Rising)

V_{BAT1} Charging Current Limit = 15A (IMON_INN)

V_{BAT2} Charging Current Limit = 15A (IMON_OP)

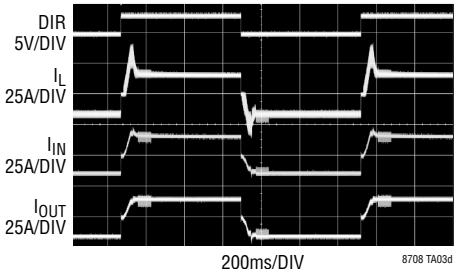
Frequency = 120kHz

Table of Operation Modes and Power Flow Directions

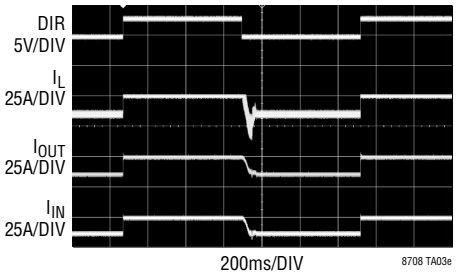
CONDITIONS			RESULTS		
V_{BAT1}	V_{BAT2}	DIR	POWER FLOW	CHIP OPERATES IN	$\overline{RVSOFF}$*
<V_{BAT1_DEAD}	–	–	No Power Flow	Shutdown	–
–	<V_{BAT2_DEAD}			No Switching	
<V_{BAT1_UV}	>V_{BAT2_DEAD}	Hi		FHCM	
>V_{BAT1_UV}	>14.5V				
	>V_{BAT2_DEAD} and <14.5V		Power Flows from V_{BAT1} to V_{BAT2} (V_{BAT2} Charging)		
>V_{BAT1_DEAD}	>V_{BAT2_DEAD} and <V_{BAT2_UV}	Lo	No Power Flow	RHCM	Lo
>14.6V	>V_{BAT2_UV}				Hi
>V_{BAT1_DEAD} and <14.6V	>V_{BAT2_UV}		Power Flows from V_{BAT2} to V_{BAT1} (V_{BAT1} Charging)		

*For use with LT8708-1(s)

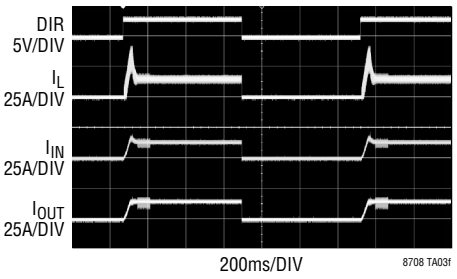
Direction Change with V_{BAT1} = 13.5V and V_{BAT2} = 13.5V



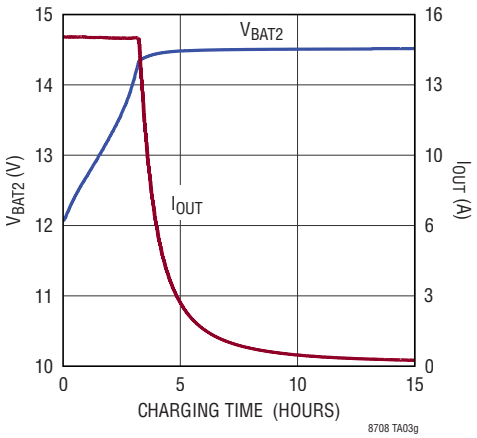
Direction Change with V_{BAT1} = 13.5V and V_{BAT2} = 16V



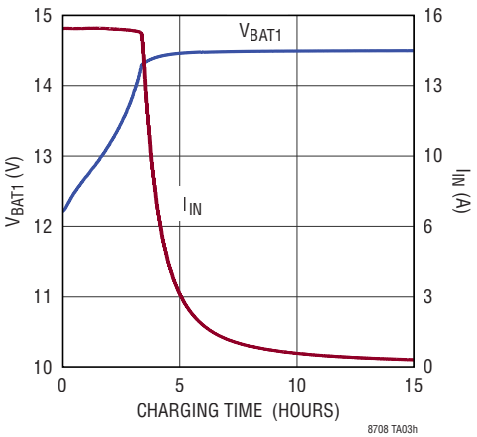
Direction Change with V_{BAT1} = 16V and V_{BAT2} = 13.5V



V_{BAT1} Charging Lead Acid Battery V_{BAT2}



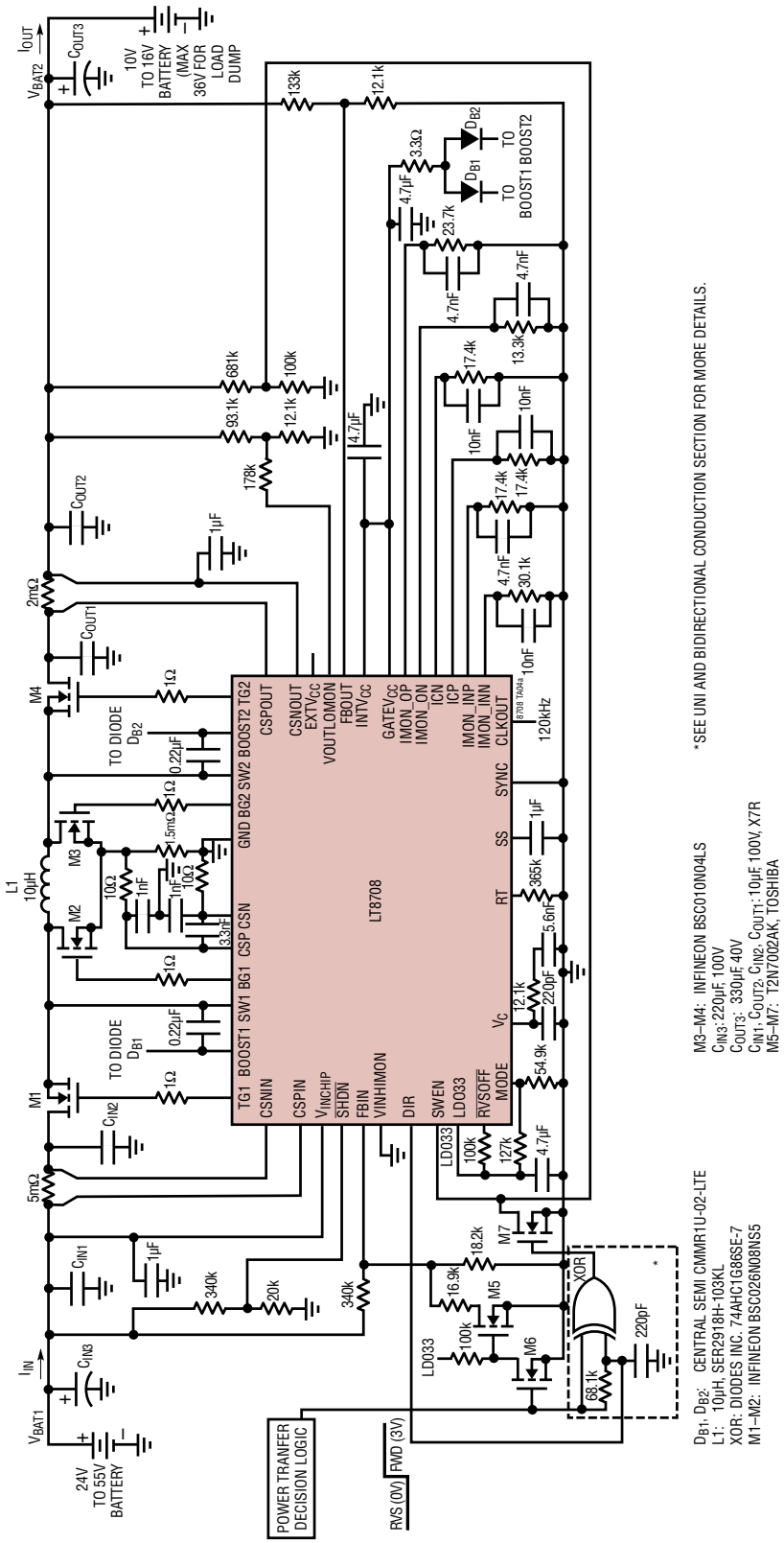
V_{BAT2} Charging Lead Acid Battery V_{BAT1}



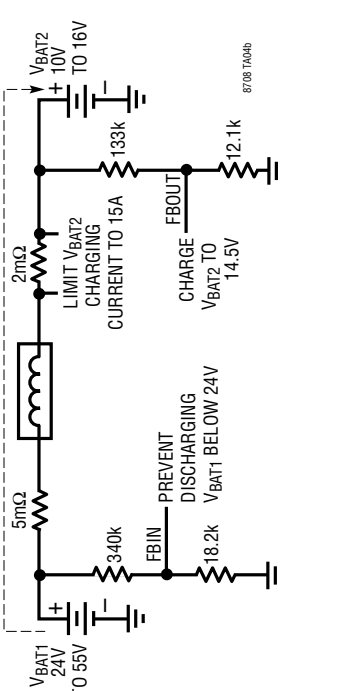
Rev. B

APPLICATIONS INFORMATION

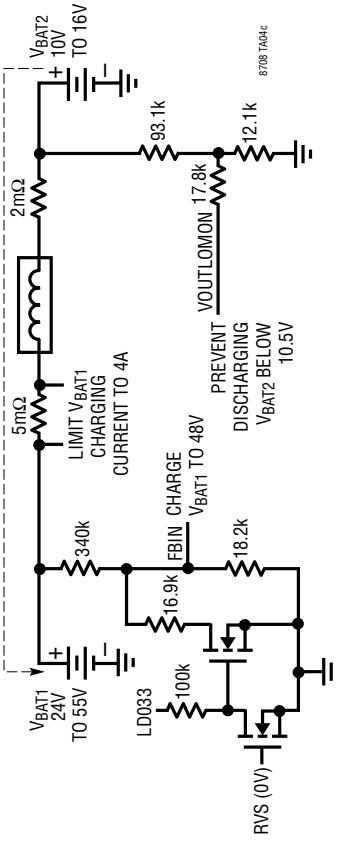
48V to 12V Bidirectional Dual Battery System with FHCM & RHCM



Forward Operation (DIR = 3V)



Reverse Operation (DIR = 0V)



APPLICATIONS INFORMATION

48V to 14V Bidirectional Dual Battery System with FHCM & RHCM Details

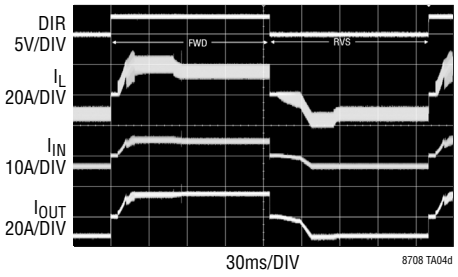
V_{BAT1} Charge Voltage = 48V (FBIN in RHCM)
V_{BAT2} Charge Voltage = 14.5V (FBOUT in FHCM)
V_{BAT1_DEAD} = 21.3V (Falling) or 22.2V (Rising)
V_{BAT2_DEAD} = 9.25V (Falling) or 9.4V (Rising)
V_{BAT2_UV} to Stop Discharging = 10.5V (VOUTLOMON Falling) or 12.3V (VOUTLOMON Rising)
V_{BAT1} Charging Current Limit = 4A (IMON_INN)
V_{BAT2} Charging Current Limit = 15A (IMON_OP)
Frequency = 120kHz

Table of Operation Modes and Power Flow Directions

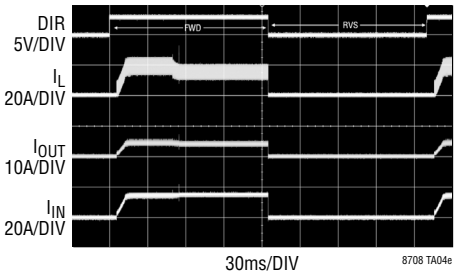
CONDITIONS			RESULTS		
V_{BAT1}	**V_{BAT2}**	**DIR**	**POWER FLOW**	**CHIP OPERATES IN**	**$\overline{RVSOFF}$***
<V_{BAT1_DEAD}	–	–	No Power Flow	Shutdown	–
–	<V_{BAT2_DEAD}			No Switching	
<V_{BAT1_UV}	> V_{BAT2_DEAD}	Hi		FHCM	
>V_{BAT1_UV}	>14.5V				
	>V_{BAT2_DEAD} and <14.5V		Power Flows from V_{BAT1} to V_{BAT2} (V_{BAT2} Charging)		
>V_{BAT1_DEAD}	>V_{BAT2_DEAD} and <V_{BAT2_UV}	Lo	No Power Flow	RHCM	Lo
>48V	>V_{BAT2_UV}				Hi
>V_{BAT1_DEAD} and <48V	>V_{BAT2_UV}		Power Flows from V_{BAT2} to V_{BAT1} (V_{BAT1} Charging)		

*For use with LT8708-1(s)

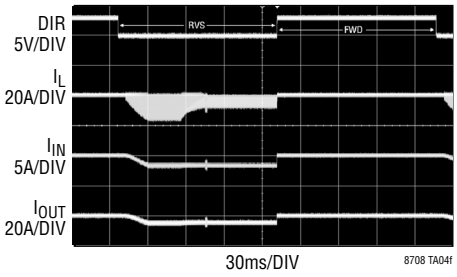
Direction Change with V_{BAT1} = 47.5V and V_{BAT2} = 14V



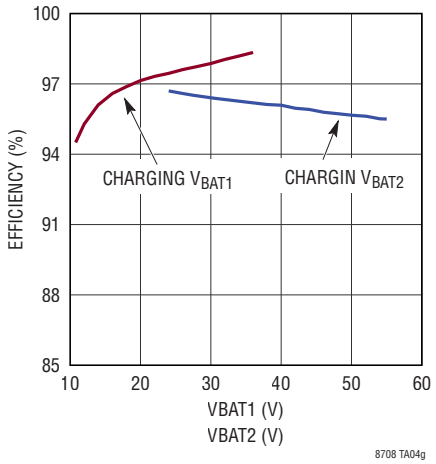
Direction Change with V_{BAT1} = 55V and V_{BAT2} = 14V



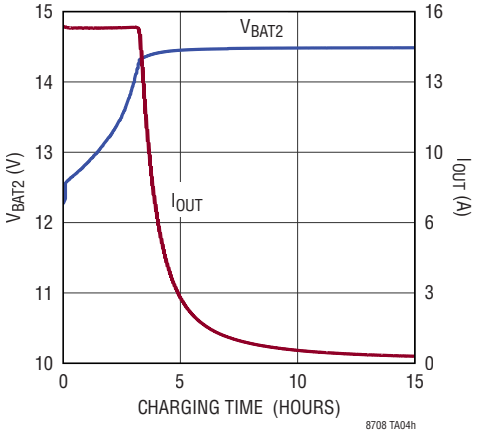
Direction Change with V_{BAT1} = 47.5V and V_{BAT2} = 36V



Efficiency

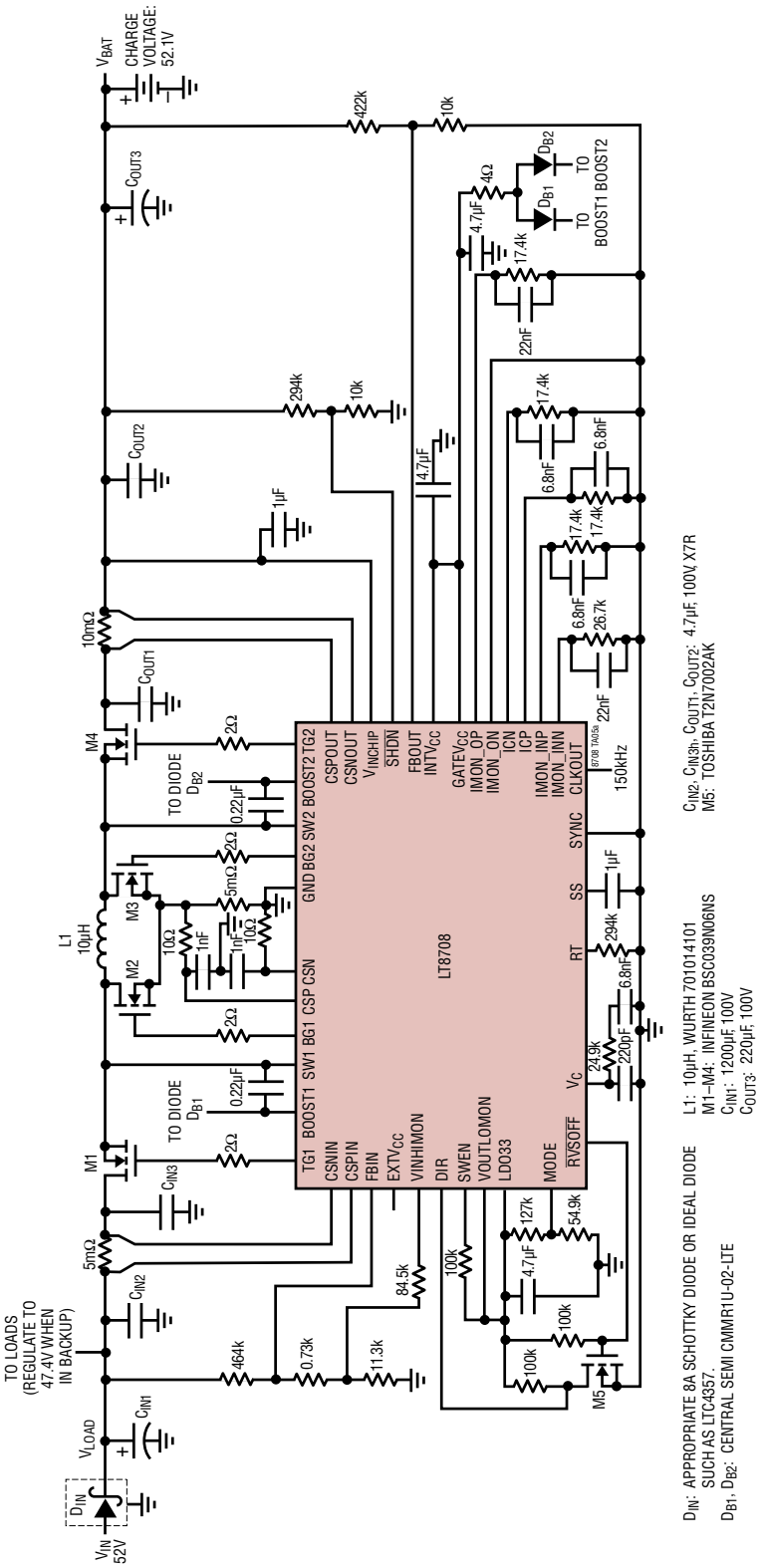


V_{BAT1} Charging Lead Acid Battery V_{BAT2}



APPLICATIONS INFORMATION

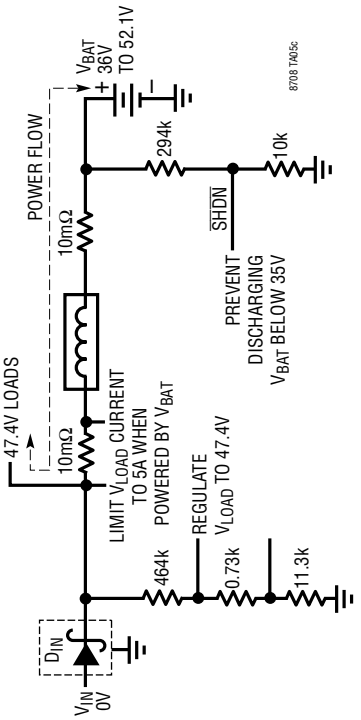
52V Battery Backup Supply Using FHCM and RHCM



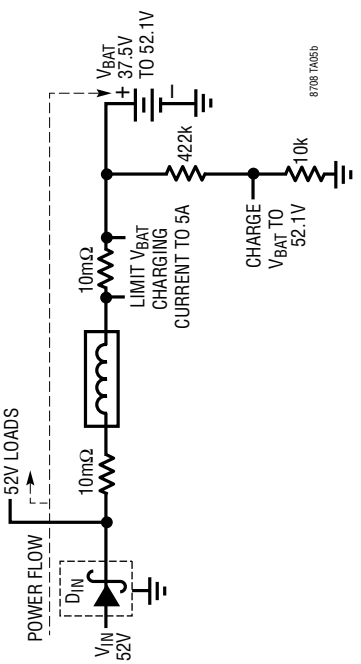
DIN: APPROPRIATE 8A SCHOTTKY DIODE OR IDEAL DIODE SUCH AS LTC4357.
DB1, DB2: CENTRAL SEMI CMMR1U-02-LTE

L1: 10µH, WURTH 7010141O1
M1–M4: INFINEON BSC039N06NS
M5: TOSHIBA T2N7002AK
CIN1: 1200µF 100V
COUT3: 220µF, 100V
CIN2, CIN3, COUT1, COUT2: 4.7µF, 100V, X7R

When V_{IN} Is Not Applied, V_{LOAD} Is Regulated to 47.4V Until V_{BAT} Drops Below 36V



When V_{IN} Is Applied, V_{BAT} Is Charged to 52.1V



APPLICATIONS INFORMATION

52V Battery Backup Supply Using FHCM and RHCM Detail

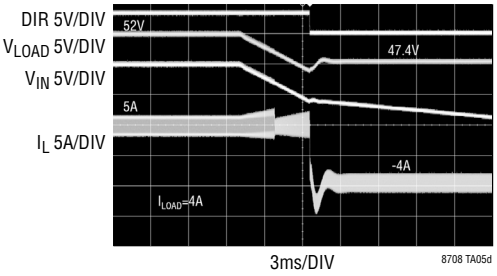
V_{BAT} Charge Voltage = 52.1V (FBOUT in FHCM)
V_{LOAD} Regulation Voltage = 47.4V (FBIN in RHCM)
V_{BAT_DEAD} = 36V (Falling) or 37.5V (Rising)
Frequency = 150kHz
V_{LOAD} Rising to Activate V_{BAT} Charging = 50.2V (VINHIMON Rising Activating FHCM)
V_{LOAD} Falling to Activate Backup Operation = 45.9V (VINHIMON Falling Activating RHCM)
V_{BAT} Charging Current Limit = 5A (IMON_OP)
V_{LOAD} Current Limit = 5A (IMON_INN)

Table of Operation Modes and Power Flow Directions

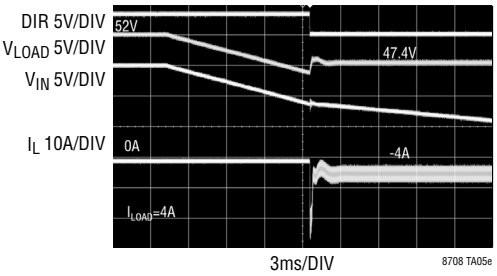
CONDITIONS		RESULTS			
V_{LOAD}	**V_{BAT}**	**POWER FLOW**	**CHIP OPERATES IN**	**$\overline{RVSOFF}$**	**DIR**
–	<V_{BAT_DEAD}	No Power Flow	Shutdown	–	–
>50.2V*	>52.1V				
Fell Into (47.4V to 50.2V) Range*	V_{BAT_DEAD} to 52.1V	Power Flows from V_{IN} to V_{BAT} (V_{BAT} Charging)	FHCM	Lo	Hi
	>52.1V	No Power Flow			
Fell Into (45.9V to 47.4V) Range*	>V_{BAT_DEAD}				
Rose Into (47.4V to 50.2V) Range*			RHCM	Hi	Lo
Rose Into (45.9V to 47.4V) Range		Power Flows from V_{BAT} to V_{LOAD} (Backup Operation)			
<45.9V					

*V_{LOAD} is powered from V_{IN}.

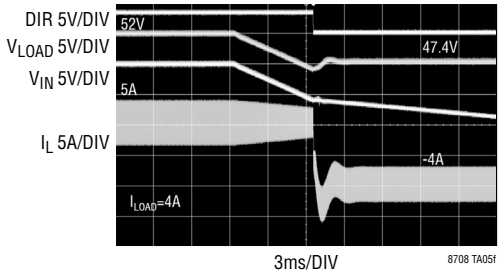
Transient Behavior Upon V_{IN} Dropout, V_{BAT} = 52V



Transient Behavior Upon V_{IN} Dropout, V_{BAT} = 53V

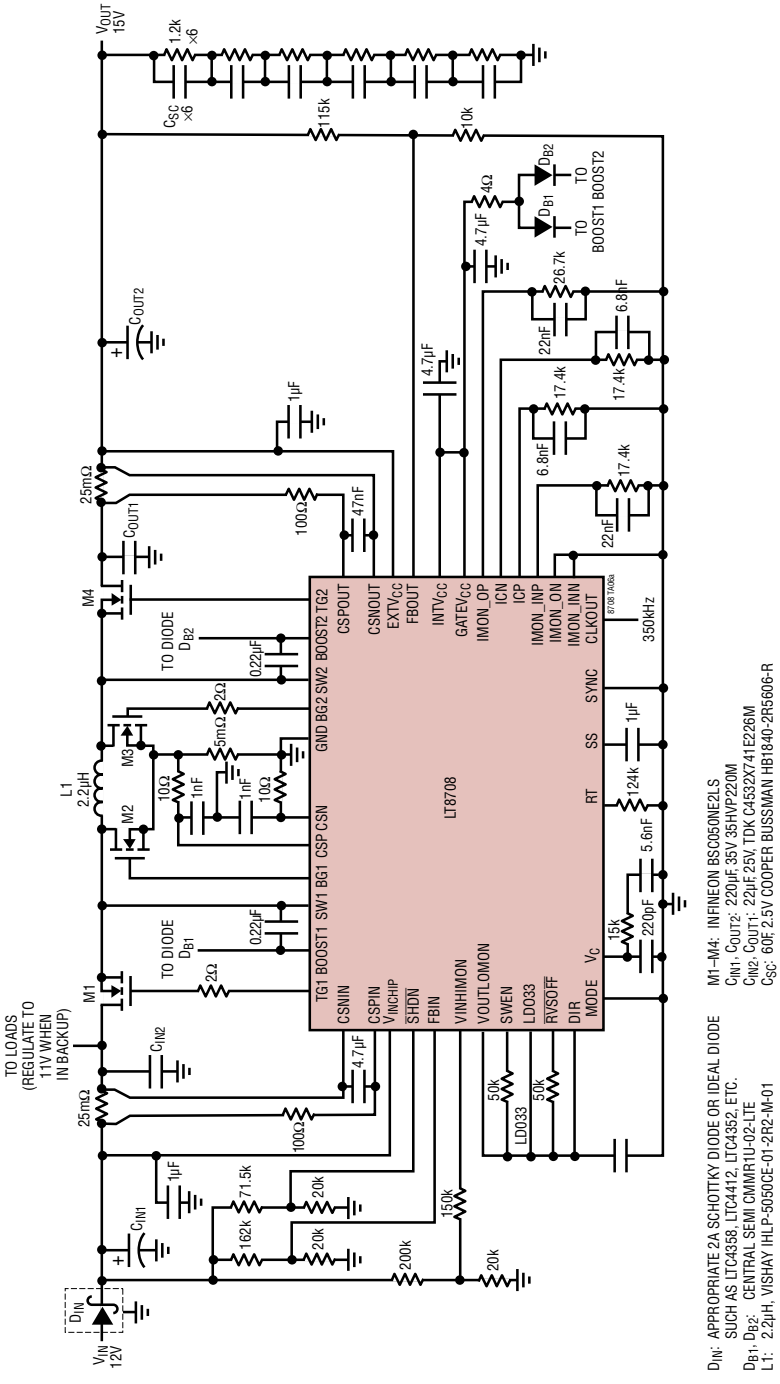


Transient Behavior Upon V_{IN} Dropout, V_{BAT} = 38V



APPLICATIONS INFORMATION

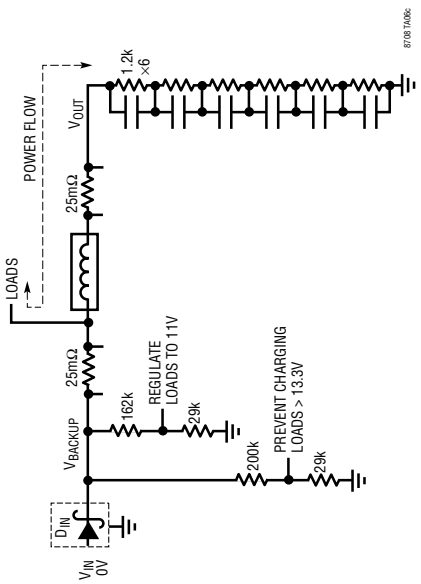
Supercapacitor Backup Supply Using CCM



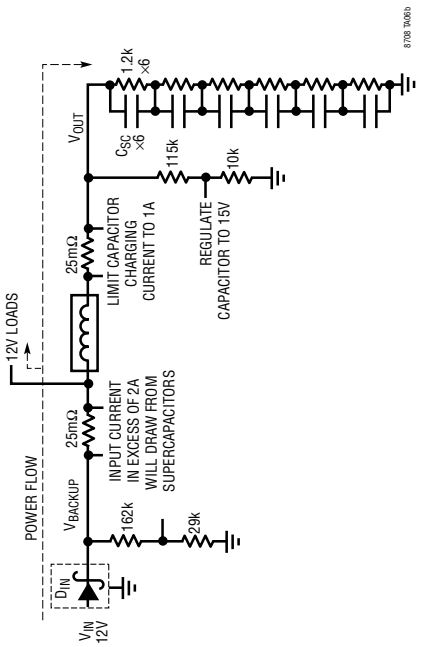
DIN: APPROPRIATE 2A SCHOTTKY DIODE OR IDEAL DIODE SUCH AS LTC4358, LTC4412, LTC4352, ETC.
DB1, DB2: CENTRAL SEMI CMMR1U-02-LTE
L1: 2.2µH, VISHAY IHLP-5050CE-01-2R2-M-01

M1–M4: INFINEON BSC050NE2LS
CIN1, COUT2: 220µF, 35V 35HVP220M
CIN2, COUT1: 22µF 25V, TDK C4532X741E226M
CSC: 60F, 2.5V COOPER BUSSMAN HB1840-2R5606-R

When V_{IN} Is Not Applied, V_{LOAD} Is Regulated to 11V



When V_{IN} Is Applied, V_{OUT} Is Charged to 15V



APPLICATIONS INFORMATION

Supercapacitor Backup Supply Using CCM Detail

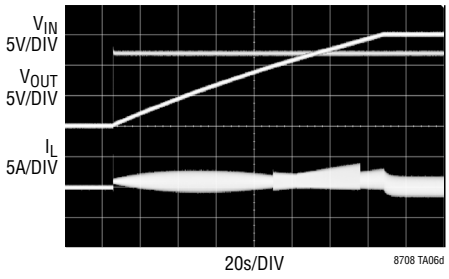
V_{OUT} Charge Voltage = 15V (FBOUT)
V_{BACKUP} Regulation Voltage = 11V (FBIN)
V_{IN_MIN} = 5.42V (Falling) or 5.65V (Rising)
Frequency = 350kHz
V_{BACKUP} Overvoltage Rising Threshold in Backup Operation = 13.3V (VINHIMON Rising)
V_{BACKUP} Overvoltage Falling Threshold in Backup Operation = 12.9V (VINHIMON Falling)
V_{OUT} Charging Current Limit = 1A (IMON_OP)
V_{IN} Current Limit = 2A (IMON_INP)

Table of Operation Modes and Power Flow Directions

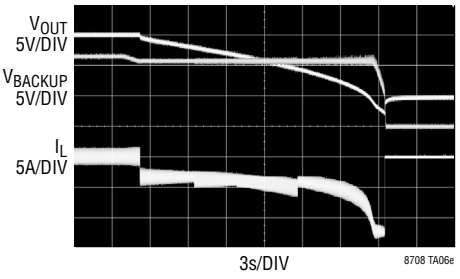
V_{BACKUP}	V_{OUT}	POWER FLOW	CHIP OPERATES IN	$\overline{RVSOFF}$*
$<V_{IN\_MIN}$	–	NO POWER FLOW	Shutdown	–
>13.3V	>15V	NO POWER FLOW	CCM	Lo
	<15V	Power Flows from V_{IN} to V_{OUT} (V_{OUT} Charging)		
Fell Into (12.9V to 13.3V) Range	>15V	No Power Flow		
Rose Into (12.9V to 13.3V) Range	<15V	Power Flows from V_{OUT} to LOADS (Backup Operation)		Hi
>11V and <12.9V	>15V	Power Flows from V_{IN} to V_{OUT} (V_{OUT} Charging)		
<11V and $>V_{IN\_MIN}$	–	Power Flows from V_{OUT} to LOADS (Backup Operation)		

*For use with LT8708-1(s)

Charging V_{OUT} to 15V with 1A Current

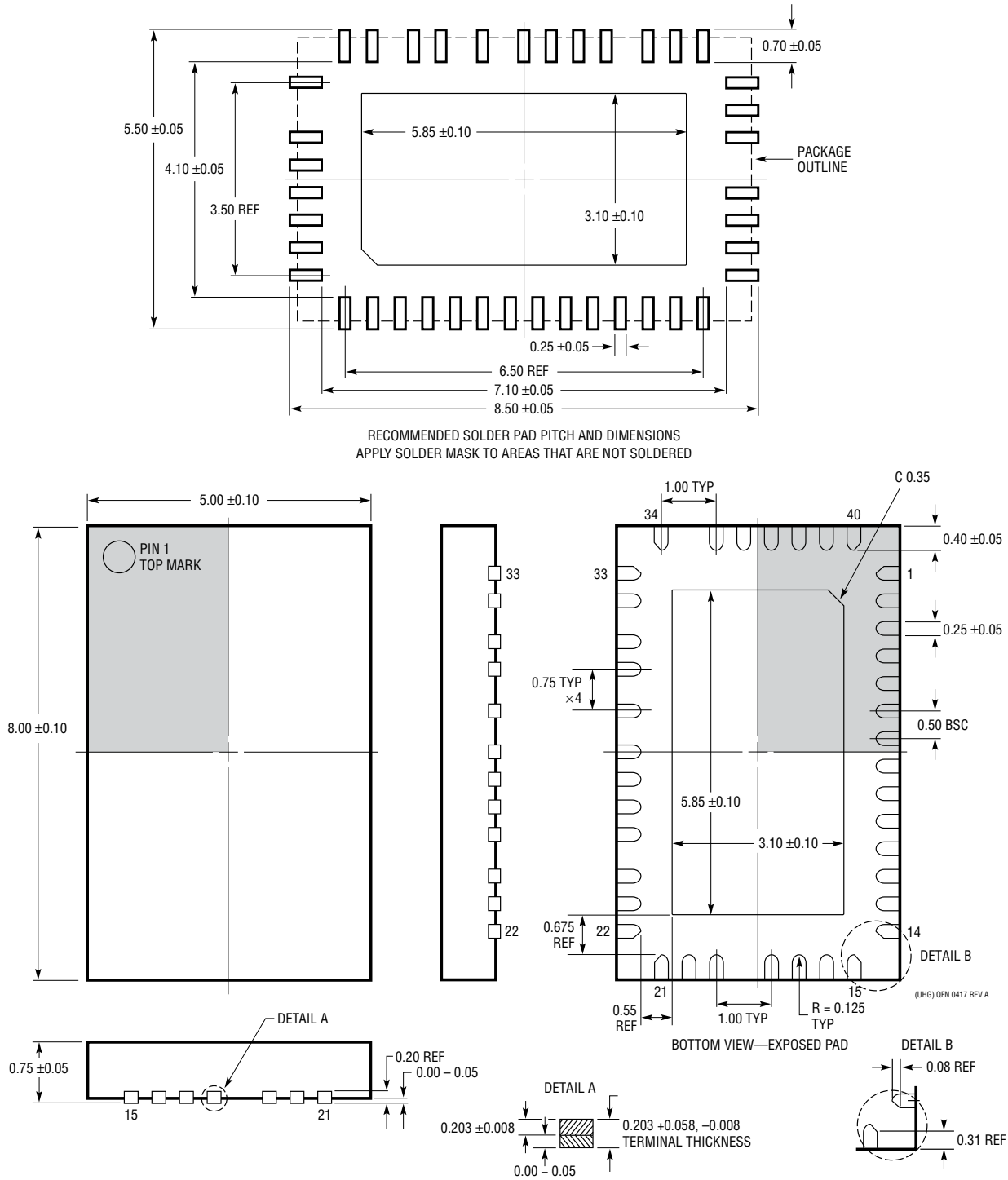


Transient Behavior Upon V_{IN} Dropout (I_{LOAD} = 4A)



PACKAGE DESCRIPTION

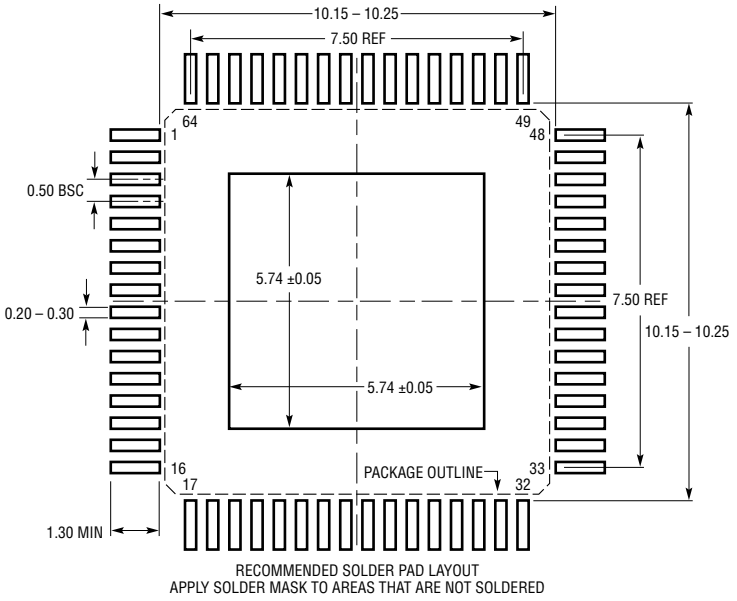
UHG Package
40-Lead Plastic QFN (5mm × 8mm)
(Reference LTC DWG # 05-08-1528 Rev A)

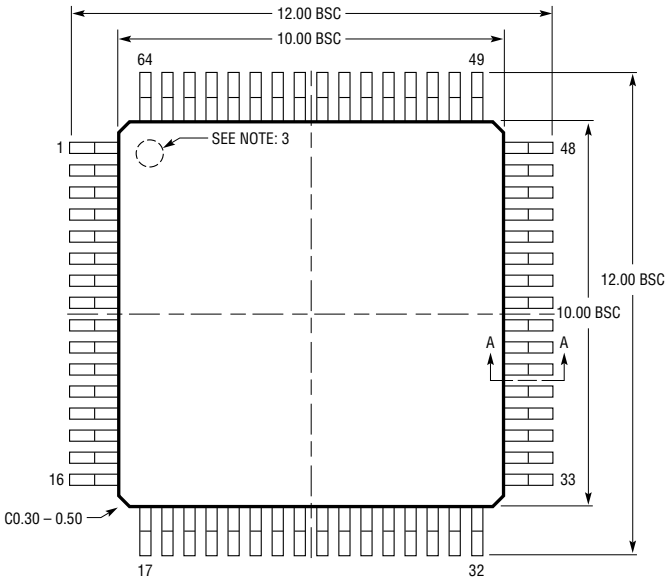


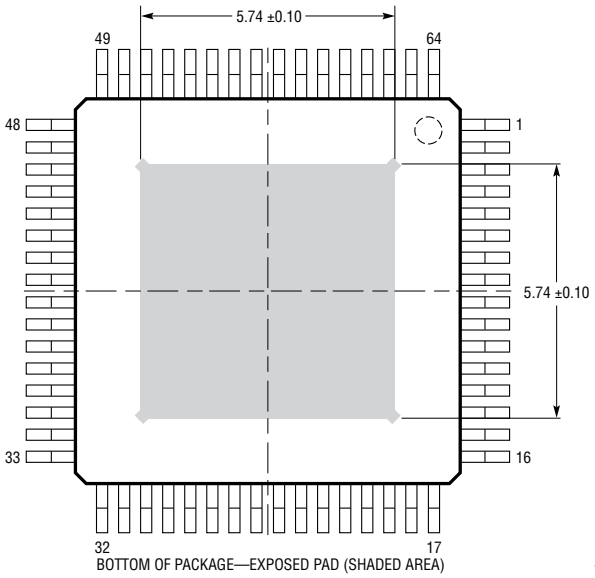
NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS. COPLANARITY SHALL NOT EXCEED 0.08MM.
3. WARPAGE SHALL NOT EXCEED 0.10MM.
4. PACKAGE LENGTH / PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC(S).
5. REFER JEDEC M0-220.

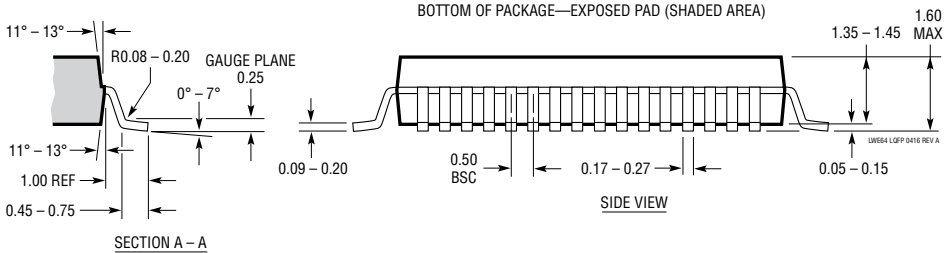
PACKAGE DESCRIPTION

LWE Package
64-Lead Plastic Exposed Pad LQFP (10mm × 10mm)
(Reference LTC DWG #05-08-1982 Rev A)









NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DIMENSIONS OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.25mm (10 MILS) BETWEEN THE LEADS AND MAX 0.50mm (20 MILS) ON ANY SIDE OF THE EXPOSED PAD, MAX 0.77mm (30 MILS) AT CORNER OF EXPOSED PAD, IF PRESENT
3. PIN-1 INDENTIFIER IS A MOLDED INDENTATION, 0.50mm DIAMETER
4. DRAWING IS NOT TO SCALE

Rev. B

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	01/20	Added eLQFP package option.	1, 3, 4, 6, 13, 14, 64, 65
		Added two arrows and corrected the 2nd y-axis of 8708 G08.	9
		Corrected the body connection of M1, changed EA7 to A7.	15
		Changed $R_{ESENSE1}$ to R_{SENSE1}.	43
		Corrected calculations.	51, 52
B	10/21	Removed TR from eLQFP package option in the Ordering Information section. The eLQFP package ships in trays.	4