Negative Input Synchronous Multi-Topology DC/DC Controller

FEATURES

- **Wide Negative Input Range: –4.5V to –80V**
- **Rail-to-Rail Output Current Monitor and Control**
- **Input Voltage Regulation for High Impedance Inputs**
- **Power Good Indication Pin**
- **MODE Pin for Forced CCM (Continuous Conduction Mode) or Pulse-Skipping/DCM (Discontinuous Conduction Mode) Operation**
- Switching Frequency Up to 750kHz
- Easily Configurable as a Buck, Boost, Buck-Boost, or Inverting Converter with a Single Feedback Pin
- Can be Synchronized to an External Clock
- High Gain EN/FBIN Pin Accepts Slowly Varying Input Signals
- 20-Lead TSSOP Package

APPLICATIONS

- High Power Negative Input, Negative Output Power Supplies
- High Power Negative Input, Positive Output Power Supplies
- Telecom Equipment Power Supplies
- Cathodic Protection Power Supplies

DESCRIPTION

The LT®8709 is a synchronous PWM controller for negative-to-negative or negative-to-positive DC/DC conversion, with rail-to-rail output current monitor and control. The LT8709 is ideal for many local power supply designs. It can be easily configured in buck, boost, buck-boost, and inverting topologies with negative input voltages.

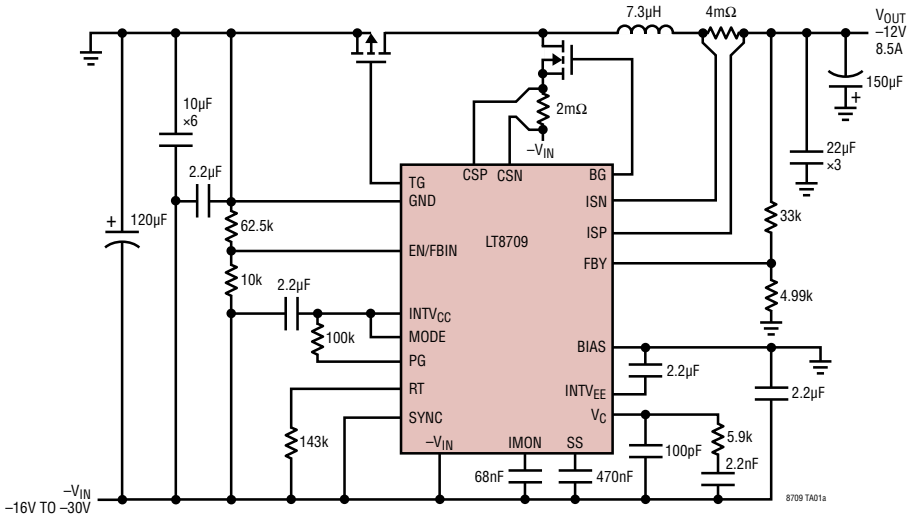
In addition, the LT8709's rail-to-rail output current sense allows the part to be configured in current limited applications such as battery or capacitor charging. The PG pin is used for power good indication.

The LT8709's switching frequency range can be set between 100kHz and 750kHz. The part may be clocked internally at a frequency set by the resistor from the RT pin to the $–V_{IN}$ pin, or it may be synchronized to an external clock.

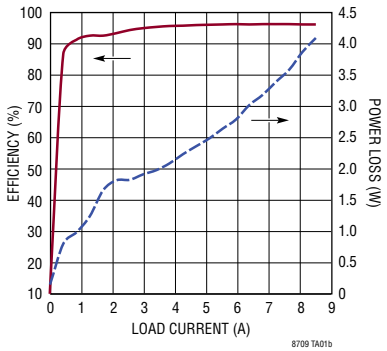
The LT8709 also features innovative EN/FBIN pin circuitry that allows for slowly varying input signals and an adjustable undervoltage lockout function. The pin is also used for input voltage regulation to avoid collapsing a high impedance input supply. Additional features such as frequency foldback, thermal shutdown and soft-start are integrated. The LT8709 is available in a 20-lead TSSOP package.

TYPICAL APPLICATION

250kHz, –16V to –30V Input to –12V/8.5A Output Buck



Efficiency and Power Loss vs Load Current ($–V_{IN}$ = –24V)

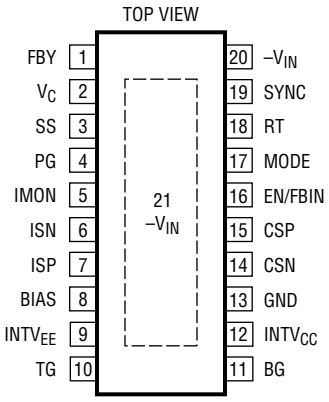


ABSOLUTE MAXIMUM RATINGS

(Note 1)

GND Voltage with Reference to $-V_{IN}$ ..... –0.3V to 80V
BIAS Voltage with Reference to $-V_{IN}$ ..... –0.3V to 80V
BG Voltage with Reference to $-V_{IN}$ ..... (Note 5)
TG Voltage with Reference to BIAS ..... (Note 5)
RT Voltage with Reference to $-V_{IN}$ ..... –0.3V to 5V
SS Voltage with Reference to $-V_{IN}$ ..... –0.3V to 3V
FBY Voltage with Reference to GND ..... –3V to 0.3V
V_C Voltage with Reference to $-V_{IN}$ ..... –0.3V to 2V
EN/FBIN Voltage with Reference to $-V_{IN}$ .... –0.3V to 80V
SYNC Voltage with Reference to $-V_{IN}$ ..... –0.3V to 5.5V
PG Voltage with Reference to $-V_{IN}$ ..... –0.3V to 7V
PG Current ..... ±1mA
MODE Voltage with Reference to $-V_{IN}$ ..... –0.3V to 40V
$INTV_{CC}$ Voltage with Reference to $-V_{IN}$ ..... –0.3V to 7V
$INTV_{EE}$ Voltage with Reference to BIAS ..... (Note 5)
CSP Voltage with Reference to $-V_{IN}$ ..... –0.3V to 2V
CSN Voltage with Reference to $-V_{IN}$ ..... –0.3V to 2V
ISP Voltage ..... ISN – 0.4V to ISN + 2V
ISN Voltage with Reference to $-V_{IN}$ ..... –0.3V to 80V
IMON Voltage with Reference to $-V_{IN}$ ..... –0.3V to 2.5V
Operating Junction Temperature Range
  LT8709E ..... –40°C to 125°C
  LT8709I ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



FE PACKAGE
20-LEAD PLASTIC TSSOP

T_{JMAX} = 125°C, θ_{JA} = 38°C/W, θ_{JC} = 10°C/W
EXPOSED PAD (PIN 21) IS $-V_{IN}$, MUST BE SOLDERED TO PCB

ORDER INFORMATION

(http://www.linear.com/product/LT8709#orderinfo)

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT8709EFE#PBF	LT8709EFE#TRPBF	LT8709FE	20-Lead Plastic TSSOP	–40°C to 125°C
LT8709IFE#PBF	LT8709IFE#TRPBF	LT8709FE	20-Lead Plastic TSSOP	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/

For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications for each channel are at T_A = 25°C. $V_{GND} - V_{-VIN}$ = 12V, $V_{EN/FBIN} - V_{-VIN}$ = 12V, $V_{BIAS} - V_{-VIN}$ = 12V, unless otherwise noted. Pin voltages have the following relations: FBY is relative to the GND pin, TG and $INTV_{EE}$ to the BIAS pin, and all other pins to the $-V_{IN}$ pin, unless otherwise stated. Pin currents have the following relations: positive current is denoted as current flowing into the pin; negative current is denoted as current flowing out of the pin, unless otherwise stated. (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Operating Input Voltage	$V_{GND} - V_{-VIN}$ OR $V_{BIAS} - V_{-VIN}$ $V_{GND} - V_{-VIN}$, if $V_{BIAS} - V_{-VIN} \geq 4.5V$	● 	 0	4.25	4.5	V V
Quiescent Current, I_{GND}, Not Switching	$V_{BIAS} - V_{-VIN}$ = 8V, $V_{ISN} - V_{-VIN}$ = 8V $V_{BIAS} - V_{-VIN}$ = 6.3V, $V_{BIAS} - V_{INTVEE}$ = 6.3V			4 5.5	5.5 7.5	mA mA
Quiescent Current in Shutdown, I_{GND}	$V_{EN/FBIN}$ = 0V			0	1	µA
EN/FBIN Minimum Input Voltage High, Releases SS	EN/FBIN Rising	●	1.64	1.7	1.76	V
EN/FBIN Minimum Input Voltage High, Chip-On but SS Held Low	EN/FBIN Rising EN/FBIN Falling	● ●	1.22 1.18	1.3 1.26	1.38 1.34	V V
EN/FBIN Minimum Input Voltage High Hysteresis				44		mV
EN/FBIN Input Voltage Low	Shutdown Mode	●			0.3	V
EN/FBIN Pin Bias Current	$V_{EN/FBIN}$ = 3V $V_{EN/FBIN}$ = 1.7V $V_{EN/FBIN}$ = 1.6V $V_{EN/FBIN}$ = 0V		 14 13	44 19.5 17.5 0	60 25 22.5 0.1	µA µA µA µA
SS Charge Current	V_{SS} = 50mV, Current Flowing Out of SS Pin	●	7	10.1	13.8	µA
SS Low Detection Voltage	Part Exiting Undervoltage Lockout	●	18	50	82	mV
SS Hi Detection Voltage	SS Rising SS Falling		1.5 1.3	1.8 1.7	2.1 2.05	V V
SS Hi Detection Hysteresis				100		mV
Low Dropout Regulators, $INTV_{CC}$ and $INTV_{EE}$						
$INTV_{CC}$ Voltage	I_{INTVCC} = 10mA	●	6.2	6.3	6.4	V
$INTV_{CC}$ Undervoltage Lockout	$INTV_{CC}$ Rising $INTV_{CC}$ Falling	● ●	3.88 3.5	4 3.73	4.12 3.95	V V
$INTV_{CC}$ Undervoltage Lockout Hysteresis				270		mV
$INTV_{CC}$ Dropout Voltage, $V_{GND} - INTV_{CC}$	$V_{GND} - V_{-VIN}$ = 6V, $V_{BIAS} - V_{-VIN}$ = 0V, I_{INTVCC} = 10mA $V_{GND} - V_{-VIN}$ = 0V, $V_{BIAS} - V_{-VIN}$ = 6V, I_{INTVCC} = 10mA			255 280		mV mV
$INTV_{CC}$ Load Regulation	$V_{GND} - V_{-VIN}$ = 0V, I_{INTVCC} = 0mA to 80mA $V_{BIAS} - V_{-VIN}$ = 0V, I_{INTVCC} = 0mA to 40mA			–0.44 –0.34	–2 –2	% %
$INTV_{CC}$ Line Regulation	10V ≤ $V_{GND} - V_{-VIN}$ ≤ 80V, $V_{BIAS} - V_{-VIN}$ = 0V, I_{INTVCC} = 10mA 10V ≤ $V_{BIAS} - V_{-VIN}$ ≤ 80V, $V_{GND} - V_{-VIN}$ = 0V, I_{INTVCC} = 10mA			–0.003 –0.006	–0.03 –0.03	%/V %/V
$INTV_{CC}$ Maximum External Load Current					5	mA
$INTV_{EE}$ Voltage, $V_{BIAS} - V_{INTVEE}$	I_{INTVEE} = 10mA	●	6.03	6.18	6.33	V
$INTV_{EE}$ Undervoltage Lockout, $V_{BIAS} - V_{INTVEE}$	$V_{BIAS} - V_{INTVEE}$ Rising $V_{BIAS} - V_{INTVEE}$ Falling	● ●	3.24 2.94	3.42 3.22	3.6 3.48	V V
$INTV_{EE}$ Undervoltage Lockout Hysteresis, $V_{BIAS} - V_{INTVEE}$				200		mV
$INTV_{EE}$ Dropout Voltage, $V_{INTVEE} - V_{-VIN}$	$V_{BIAS} - V_{-VIN}$ = 6V, I_{INTVEE} = 10mA			0.75		V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications for each channel are at T_A = 25°C. $V_{GND} – V_{–VIN}$ = 12V, $V_{EN/FBIN} – V_{–VIN}$ = 12V, $V_{BIAS} – V_{–VIN}$ = 12V, unless otherwise noted. Pin voltages have the following relations: FBY is relative to the GND pin, TG and $INTV_{EE}$ to the BIAS pin, and all other pins to the $–V_{IN}$ pin, unless otherwise stated. Pin currents have the following relations: positive current is denoted as current flowing into the pin; negative current is denoted as current flowing out of the pin, unless otherwise stated. (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Control Loops (Refer to Block Diagram to Locate Amplifiers)						
Current Limit Voltage, $V_{CSP} – V_{CSN}$	I_{FBY} = –67.9µA, Minimum Duty Cycle I_{FBY} = –67.9µA, Maximum Duty Cycle	● ●	46 23	50 31	54 38	mV mV
	I_{FBY} = –108µA, MODE = 0V, Minimum Duty Cycle I_{FBY} = –108µA, MODE = 0V, Maximum Duty Cycle	● ●	–41 –65	–32 –51	–23 –38	mV mV
FBY Voltage for Negative Output Voltage Regulation	Q1 Conducting Current, Current Flowing Out of FBY Pin	●	–1.28	–1.234	–1.18	V
FBY Voltage for Positive Output Voltage Regulation	M1 Conducting Current, Current Flowing into FBY Pin	●	–60	–15.8	25	mV
Negative FBY Pin Bias Current	Current Flowing Out of FBY Pin	●	81.4	83.5	85.7	µA
Positive FBY Pin Bias Current	Current Flowing Into FBY Pin	●	80.1	83.9	87.5	µA
FBY Voltage-to-Current Amp Transconductance, $\Delta I_{FBY}/\Delta V_{FBY}$	Current Flowing Out of FBY Pin, ΔI_{FBY} = 10µA Current Flowing into FBY Pin, ΔI_{FBY} = 10µA			1.8 1.05		mS mS
FBY Error Amp Transresistance $\Delta V_{VC}/\Delta I_{FBY}$	Current Flowing Out of FBY Pin, ΔV_{VC} = 200mV Current Flowing into FBY Pin, ΔV_{VC} = 200mV			508 516		kΩ kΩ
FBY Error Amp Current Gain $\Delta I_{VC}/\Delta I_{FBY}$	ΔI_{VC} = 2µA			1.5		A/A
FBY Line Regulation	4.5V ≤ $V_{GND} – V_{–VIN}$ ≤ 80V, $V_{BIAS} – V_{–VIN}$ = 0V		–0.02	0.003	0.02	%/V
Output Current Sense Regulation Voltage, $V_{ISP} – V_{ISN}$	V_{ISN} = 80V, I_{FBY} = –53µA V_{ISN} = 12V, I_{FBY} = –53µA V_{ISN} = 0V, I_{FBY} = –53µA V_{ISN} = 12V, I_{FBY} = –53µA, $INTV_{EE}$ in UVLO and SS > 1.8V	● ● ● ●	43 43 40 17	50 50 50 25	57 57 60 34	mV mV mV mV
IMON Regulation Voltage, EA2	I_{FBY} = –53µA I_{FBY} = –53µA, $INTV_{EE}$ in UVLO and SS > 1.8V	● ●	1.184 0.885	1.213 0.916	1.24 0.947	V V
Output Current Sense Amp Transconductance, A7	ΔI_{IMON} = 10µA			1000		µS
Output Current Sense Amp Voltage Gain, A7				11.9		V/V
Output Current Sense Amp Input Dynamic Range, A7	Negative Input Range Positive Input Range		500	–51.8		mV mV
IMON Amp Transconductance, EA2	ΔI_{VC} = 2µA, I_{FBY} = –53µA			165		µS
IMON Amp Voltage Gain, EA2	V_{ISN} = 12V, I_{FBY} = –53µA			65		V/V
EN/FBIN Input Regulation Voltage, EA3	I_{FBY} = –53µA	●	1.55	1.607	1.662	V
EN/FBIN Amp Transconductance, EA3	ΔI_{VC} = 2µA, I_{FBY} = –53µA			140		µS
EN/FBIN Amp Voltage Gain, EA3	I_{FBY} = –53µA			55		V/V
MODE Forced CCM Threshold	To Exit Forced CCM Mode, MODE Rising To Enter Forced CCM Mode, MODE Falling	● ●	1.19 1.125	1.224 1.175	1.258 1.23	V V
MODE Forced CCM Threshold Hysteresis				49		mV
DCM Comparator Threshold in Pulse-Skipping Mode, MODE = 2V	V_{ISN} = 80V, To Enter DCM Mode, $V_{ISP} – V_{ISN}$ Falling V_{ISN} = 12V, To Enter DCM Mode, $V_{ISP} – V_{ISN}$ Falling V_{ISN} = 0V, To Enter DCM Mode, $V_{ISP} – V_{ISN}$ Falling	● ● ●	–4.5 –4.5 –7.5	2.8 2.8 2.8	10 10 13	mV mV mV
DCM Comparator Threshold in Forced CCM, MODE = 0V	V_{ISN} = 80V, To Enter DCM Mode, $V_{ISP} – V_{ISN}$ Falling V_{ISN} = 12V, To Enter DCM Mode, $V_{ISP} – V_{ISN}$ Falling V_{ISN} = 0V, To Enter DCM Mode, $V_{ISP} – V_{ISN}$ Falling	● ● ●	–380 –380 –380	–300 –300 –300	–220 –220 –220	mV mV mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications for each channel are at T_A = 25°C. $V_{GND} – V_{–VIN}$ = 12V, $V_{EN/FBIN} – V_{–VIN}$ = 12V, $V_{BIAS} – V_{–VIN}$ = 12V, unless otherwise noted. Pin voltages have the following relations: FBY is relative to the GND pin, TG and $INTV_{EE}$ to the BIAS pin, and all other pins to the $–V_{IN}$ pin, unless otherwise stated. Pin currents have the following relations: positive current is denoted as current flowing into the pin; negative current is denoted as current flowing out of the pin, unless otherwise stated. (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Oscillator						
Switching Frequency, f_{OSC}	R_T = 46.4k R_T = 357k	● ●	640 85	750 100	860 115	kHz kHz
Switching Frequency in Foldback	Compared to Normal f_{OSC}			1/5		ratio
Switching Frequency Range	Free-Running or Synchronizing	●	100		750	kHz
SYNC High Level for Sync		●	1.5			V
SYNC Low Level for Sync		●			0.4	V
SYNC Clock Pulse Duty Cycle	V_{SYNC} = 0V to 3V		20		80	%
Recommended Min SYNC Ratio	f_{SYNC}/f_{OSC}			3/4		
Gate Drivers, BG and TG						
BG Rise Time	C_{BG} = 3300pF (Note 3)			24		ns
BG Fall Time	C_{BG} = 3300pF (Note 3)			21		ns
TG Rise Time	C_{TG} = 3300pF (Note 3)			15		ns
TG Fall Time	C_{TG} = 3300pF (Note 3)			16		ns
BG and TG Non-Overlap Time	TG Rising to BG Rising, $C_{BG} = C_{TG}$ = 3300pF (Note 3) BG Falling to TG Falling, $C_{BG} = C_{TG}$ = 3300pF (Note 3)		80 45	140 90	220 150	ns ns
BG Minimum On-Time	$C_{BG} = C_{TG}$ = 3300pF		150		420	ns
BG Minimum Off-Time	$C_{BG} = C_{TG}$ = 3300pF		100		480	ns
TG Minimum On-Time	$C_{BG} = C_{TG}$ = 3300pF		0		150	ns
TG Minimum Off-Time	$C_{BG} = C_{TG}$ = 3300pF		290		770	ns
Power Good Indicators, PG						
PG Power Good Threshold for Negative FBY Voltage	Current Out of FBY Pin Rising Current Out of FBY Pin Falling	● ●	71 63.5	74.9 67.5	79 71.5	µA µA
PG Power Good Threshold for Positive FBY Voltage	Current into FBY Pin Rising Current into FBY Pin Falling	● ●	71.5 63.5	75.4 67.5	79.5 71.5	µA µA
PG Power Good Hysteresis for Negative FBY Voltage				7.4		µA
PG Power Good Hysteresis for Positive FBY Voltage				7.9		µA
PG Anti-Glitch Delay	Delay from PG Threshold Trip to PG Toggle			100		µs
PG Output Voltage Low	100µA into PG Pin, $\lvert I_{FBY}\rvert$ < PG Threshold	●		9	50	mV
PG Leakage Current	V_{PG} = 7V, $\lvert I_{FBY}\rvert$ > PG Threshold			0.01	1	µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LT8709E is guaranteed to meet performance specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating temperature range are assured by design, characterization and correlation with statistical process controls. The LT8709I is guaranteed over the full –40°C to 125°C operating junction temperature range.

Note 3: Rise and fall times are measured using 10% and 90% levels. Delay times are measured using 50% levels.

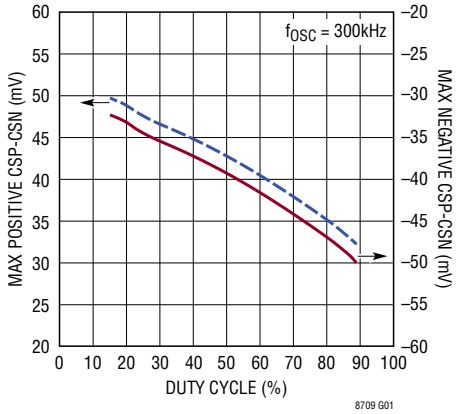
Note 4: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation over the specified maximum operating junction temperature may impair device reliability.

Note 5: Do not apply a positive or negative voltage or current source to the BG, TG, and $INTV_{EE}$ pins, otherwise permanent damage may occur, except $INTV_{EE}$ may be connected to $–V_{IN}$ if BIAS is connected to $INTV_{CC}$.

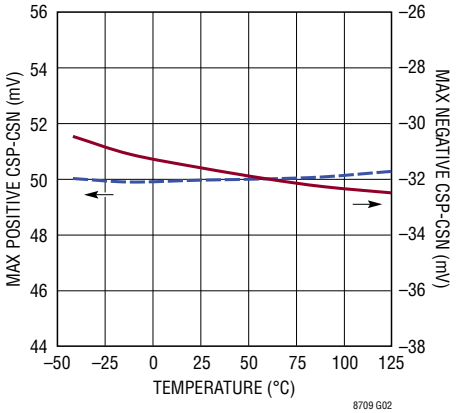
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, all voltages relative to $-V_{IN}$ unless otherwise noted.

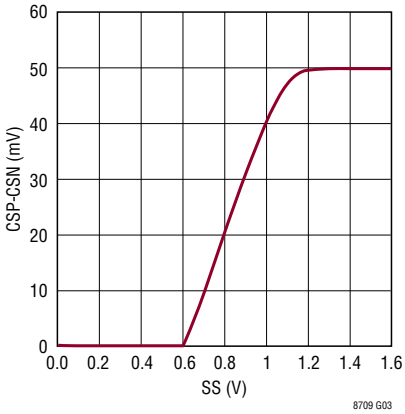
Max Current Limit vs Duty Cycle (CSP - CSN)



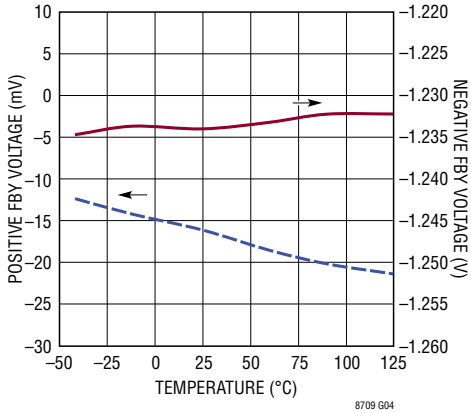
Max Current Limit vs Temperature (CSP - CSN)



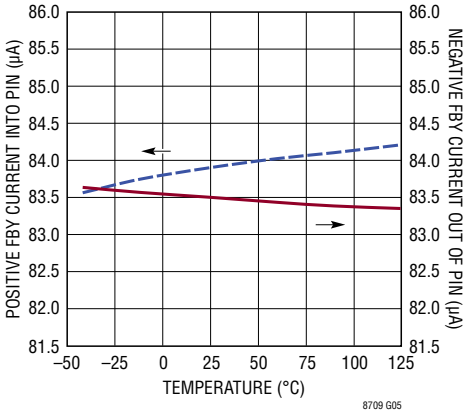
Max Current Limit vs SS (CSP - CSN)



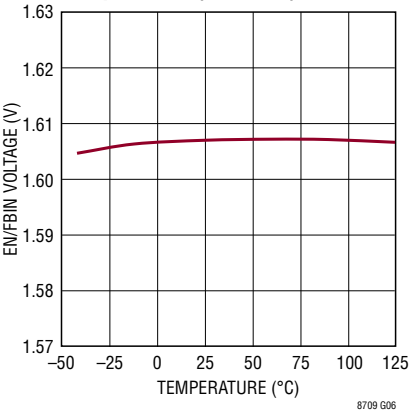
Positive and Negative Feedback Voltage vs Temperature



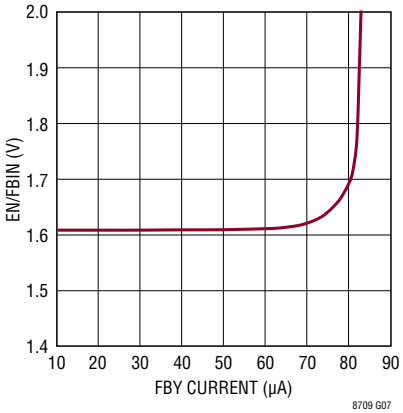
Positive and Negative FBY Currents vs Temperature



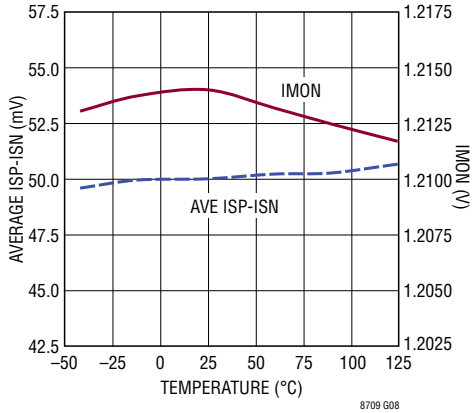
Input Regulation Voltage vs Temperature (EN/FBIN)



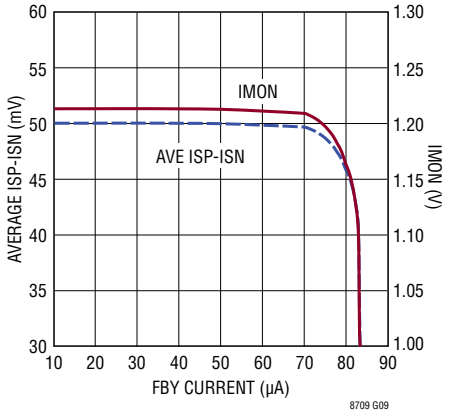
Input Regulation Voltage vs FBY (EN/FBIN)



Current Sense Voltage vs Temperature (ISP-ISN and IMON)



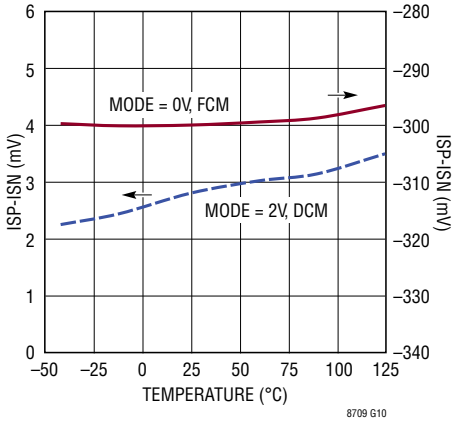
Current Sense Voltage vs FBY (ISP-ISN and IMON)



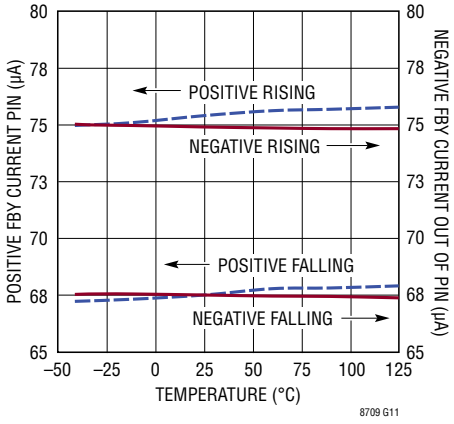
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, all voltages relative to $-V_{IN}$ unless otherwise noted.

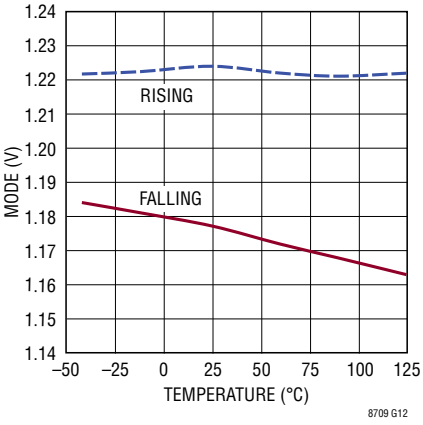
DCM Comparator Threshold vs Temperature



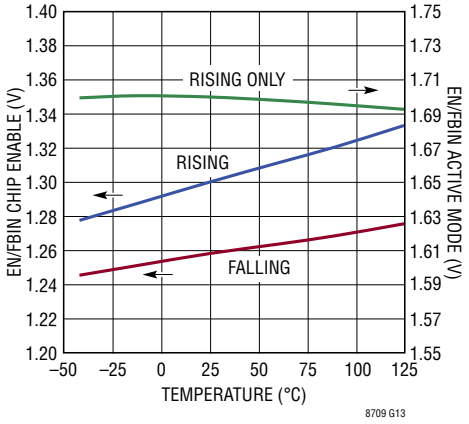
PG Threshold vs Temperature (Rising and Falling)



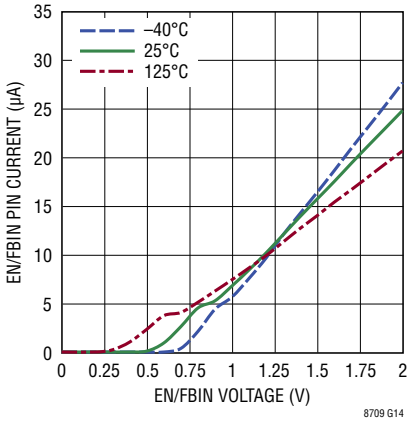
MODE Pin Threshold vs Temperature (Rising and Falling)



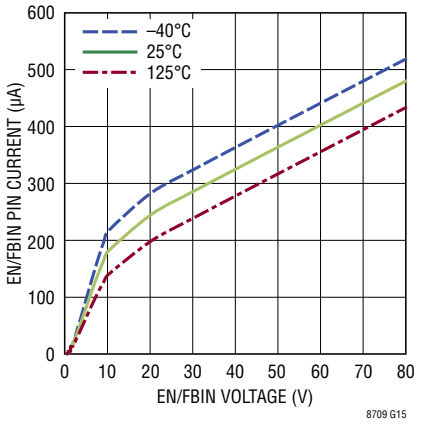
EN/FBIN Thresholds vs Temperature (1.7V and 1.3V)



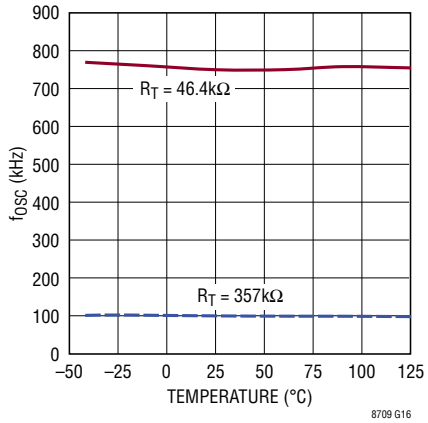
EN/FBIN Pin Current (0V to 2V) vs Temperature



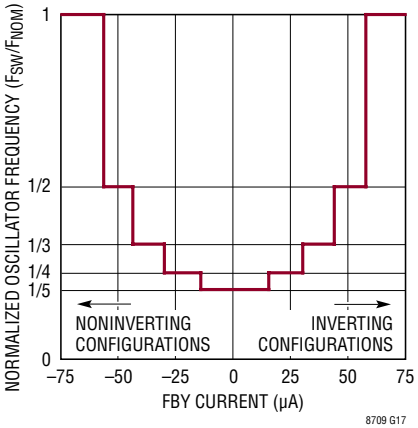
EN/FBIN Pin Current (0V to 80V) vs Temperature



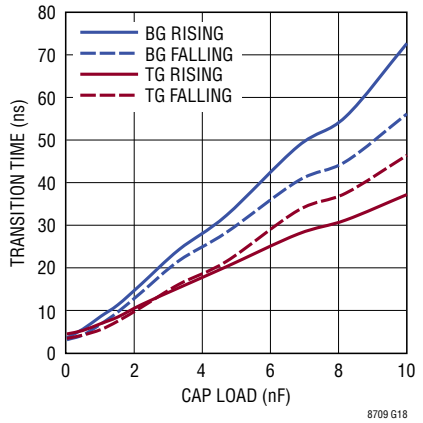
Oscillator Frequency vs Temperature (100kHz and 750kHz)



Oscillator Frequency During Soft-Start



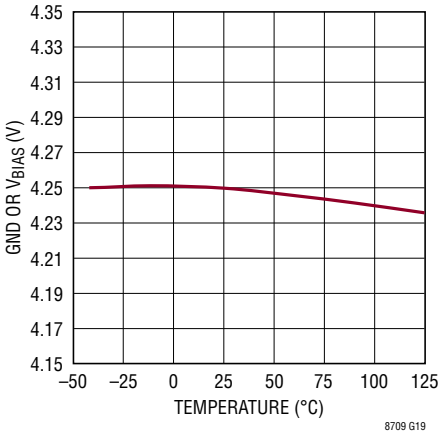
BG and TG Transition Time vs Cap Load



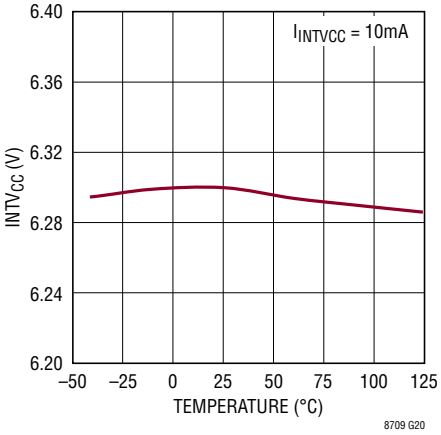
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, all voltages relative to $-V_{IN}$ unless otherwise noted.

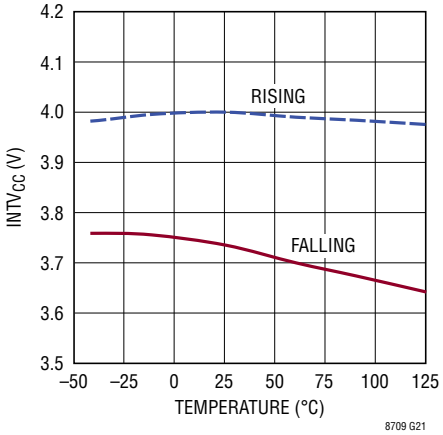
Minimum Operating Input Voltage



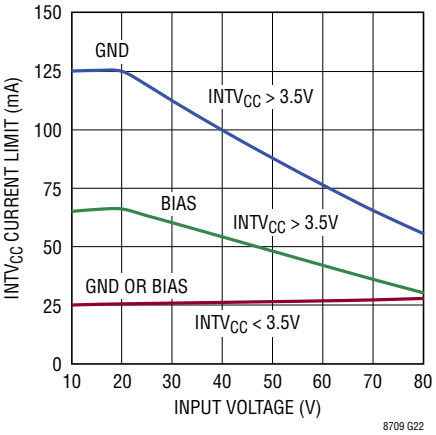
$INTV_{CC}$ vs Temperature



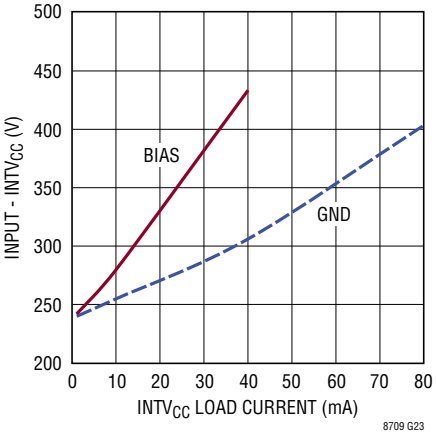
$INTV_{CC}$ UVLO vs Temperature (Rising and Falling)



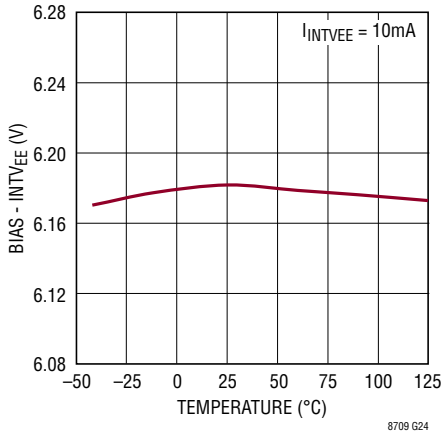
$INTV_{CC}$ Current Limit vs GND or BIAS



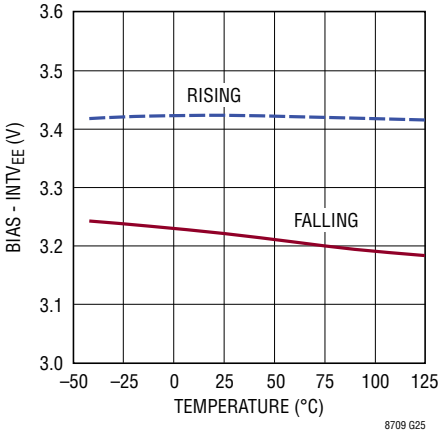
$INTV_{CC}$ Dropout from GND or BIAS



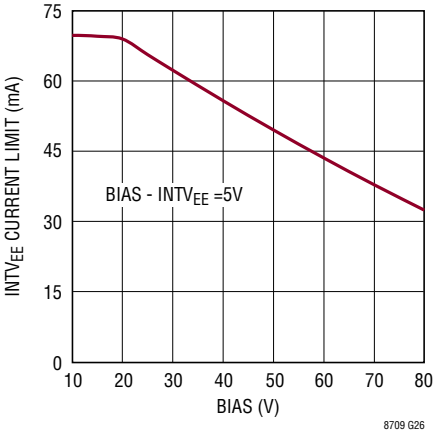
$INTV_{EE}$ vs Temperature



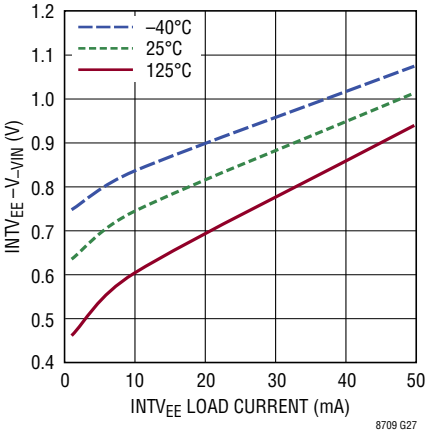
$INTV_{EE}$ UVLO vs Temperature (Rising and Falling)



$INTV_{EE}$ Current Limit vs BIAS



$INTV_{EE}$ Dropout (BIAS = 6V)



PIN FUNCTIONS

FBY (Pin 1): Feedback Pin. Its voltage is referred to the GND pin. For a boost, buck-boost, or inverting converter, tie a resistor from the FBY pin to V_{OUT} according to the following equations:

$$R_{FBY} = \frac{|V_{OUT}| - 1.234V}{83.5\mu A} \quad \text{Negative Output Voltage}$$

$$R_{FBY} = \frac{V_{OUT} + 15.8mV}{83.9\mu A} \quad \text{Positive Output Voltage}$$

See the Applications section for more information.

V_C (Pin 2): Error Amplifier Output Pin. Its voltage is referred to the $-V_{IN}$ pin. Connect an external compensation network between this pin and the $-V_{IN}$ pin.

SS (Pin 3): Soft-Start Pin. Its voltage is referred to the $-V_{IN}$ pin. Place a soft-start capacitor here that is about 5× greater than the IMON capacitor. Upon start-up, the SS pin will be charged by a nominal 260k resistor to ~2.7V. During a current overload as seen by ISP-ISN, overtemperature, or UVLO condition, the SS pin will be quickly discharged to reset the part. Once these conditions have cleared, the part will attempt to restart.

PG (Pin 4): Power Good Indication Pin. Its voltage is referred to the $-V_{IN}$ pin. The PG pin functions as an active high power good pin. Power is good when the FBY pin current is –74.9µA or 75.4µA (~90% of the regulation current), which corresponds to ~90% of the regulation voltage on V_{OUT}. For power good indication, there is a 100µs anti-glitch delay. A pull-up resistor or some other form of pull-up network is required on this pin to use the feature. See the Block Diagram and Applications section for more information.

IMON (Pin 5): Output Current Sense Monitor Pin. Its voltage is referred to the $-V_{IN}$ pin. Outputs a voltage that is proportional to the voltage between the ISP and ISN pins, as given below.

$$V_{IMON} = 11.9 \bullet (V_{ISP-ISN} + 51.8mV)$$

Since the voltage across the ISP and ISN pins is AC, a filtering capacitor is needed between the IMON and $-V_{IN}$ pins to average out the ISP and ISN voltage. Recommended capacitor values are from 10nF – 100nF. A 51.8mV offset is added to the amplifier such that an average voltage of 0V on ISP-ISN corresponds to a IMON voltage of 616mV. When the average voltage across the ISP and ISN pins is 50mV, the IMON pin will output ~1.213V. Do not resistively load down this pin.

ISN, ISP (Pins 6, 7): Output Current Sense Negative and Positive Input Pins Respectively. Kelvin connect the ISN and ISP pins to a sense resistor to limit the output current. The commanded NFET current will limit the voltage difference across the sense resistor to 50mV.

BIAS (Pin 8): Additional Input Supply and TG Gate Driver High Voltage Rail. BIAS is a second positive input supply pin in addition to GND and must be locally bypassed to $-V_{IN}$. The BIAS pin sets the top rail for the TG gate driver. BIAS must be connected to the converter's V_{OUT} for a negative inverting converter, or $INTV_{CC}$ for a negative boost converter, or GND for a negative buck or negative buck-boost converter.

$INTV_{EE}$ (Pin 9): 6.18V-Below-BIAS Regulator Pin. Must be locally bypassed to BIAS with a minimum capacitance of 2.2µF. This pin sets the bottom rail for the TG gate driver. The TG gate driver can begin switching when BIAS – $INTV_{EE}$ exceeds 3.42V (typical). Connect this pin to $-V_{IN}$ for a negative boost converter.

TG (Pin 10): PFET Gate Drive Pin. Low and high levels are BIAS – $INTV_{EE}$ and BIAS respectively.

BG (Pin 11): NFET Gate Drive Pin. Low and high levels are $-V_{IN}$ and $INTV_{CC}$ respectively.

$INTV_{CC}$ (Pin 12): 6.3V Dual Input LDO Regulator Pin. Its voltage is referred to the $-V_{IN}$ pin. Must be locally bypassed to $-V_{IN}$ with a minimum capacitance of 2.2µF. Logic will choose to run $INTV_{CC}$ from the GND or BIAS pins. A maximum 5mA external load can connect to the $INTV_{CC}$ pin. The BG gate driver can begin switching when $INTV_{CC}$ exceeds the 4V (typical) $INTV_{CC}$ undervoltage lockout.

GND (Pin 13): Positive Input Supply Pin. Must be locally bypassed to $-V_{IN}$. Can run down to V_{-VIN} as long as BIAS $-V_{-VIN} > 4.5V$.

PIN FUNCTIONS

CSN, CSP (Pins 14, 15): NFET Current Sense Negative and Positive Input Pins Respectively. Kelvin connect these pins to a sense resistor to control the NFET switch current. The maximum sense voltage at low duty cycle is 50mV (typical).

EN/FBIN (Pin 16): Enable and Input Voltage Regulation Pin. Its voltage is referred to the $-V_{IN}$ pin. In conjunction with the $INTV_{CC}$ and $INTV_{EE}$ UVLO (undervoltage lockout) circuits, overtemperature protection and output overcurrent protection; this pin is used to enable/disable the chip and restart the soft-start sequence. The EN/FBIN pin is also used to limit the NFET current to avoid collapsing the input supply. Drive the pin below 0.3V to disable the chip with very low quiescent current. Drive the pin above 1.7V (typical) to activate the chip and restart the soft-start sequence. The commanded NFET current will be controlled by the EN/FBIN amplifier when the voltage drops between 1.55V and 1.662V. See the Block Diagram and Applications section for more information. Do not float this pin.

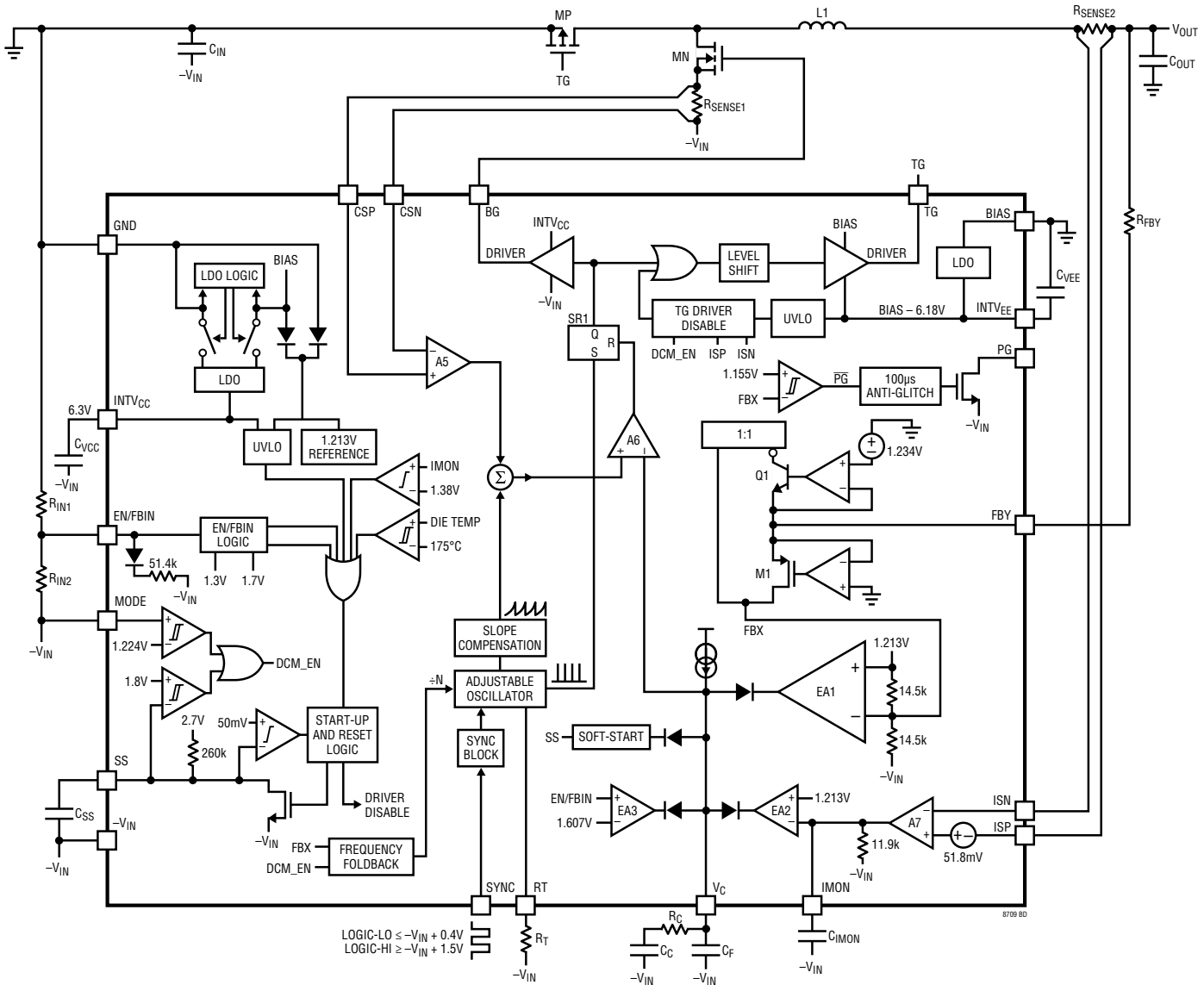
MODE (Pin 17): DCM/CCM Mode Pin. Its voltage is referred to the $-V_{IN}$ pin. Drive the pin below 1.175V (typical) to operate in forced CCM. Drive the pin above 1.224V (typical) to operate in DCM and/or pulse-skipping mode at light loads. If SS < 1.8V (typical) or $INTV_{EE}$ is in UVLO, the part will operate in DCM at light load.

RT (Pin 18): Timing Resistor Pin. Adjusts the LT8709's switching frequency. Place a resistor from this pin to $-V_{IN}$ to set the frequency to a fixed free running level. Do not float this pin.

SYNC (Pin 19): External Clock Input Pin. Its voltage is referred to the $-V_{IN}$ pin. To synchronize the switching frequency to an outside clock, simply drive this pin with a clock to override the internal clock. The logic-high voltage level of the SYNC clock must exceed 1.5V, and the logic-low level must be less than 0.4V. Drive this pin to less than 0.4V to revert to the internal free running clock. See the Applications Information section for more information.

$-V_{IN}$ (Pin 20, Exposed Pad Pin 21): Negative Voltage Input Pin. Since $-V_{IN}$ also serves as the chip ground, it must be soldered onto a local $-V_{IN}$ plane on the PCB.

BLOCK DIAGRAM



NOTE: ALL THE VOLTAGES INSIDE THE CHIP ARE REFERRED TO THE $-V_{IN}$ PIN.

Figure 1. Block Diagram

STATE DIAGRAM

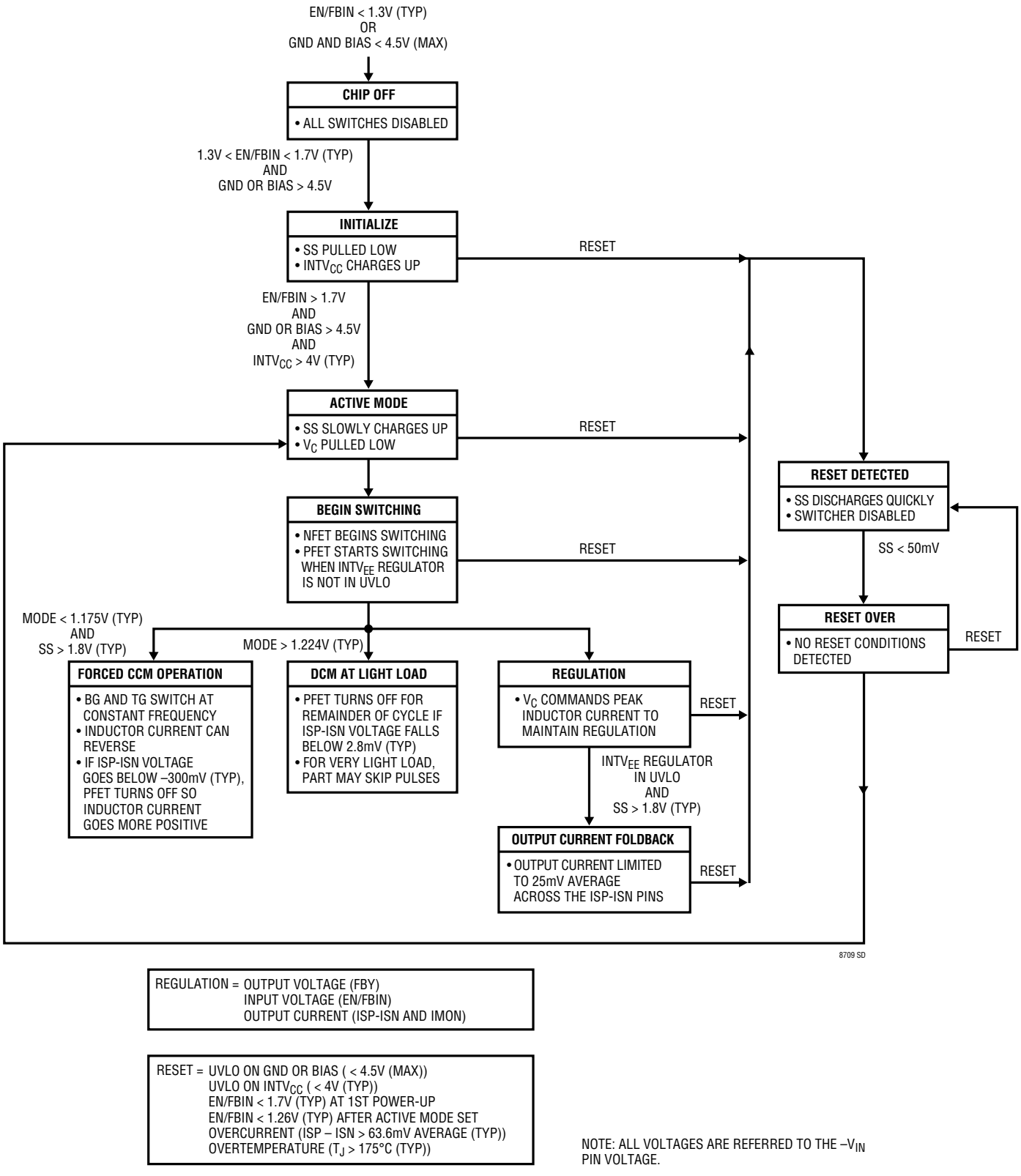


Figure 2. State Diagram

OPERATION

OPERATION – OVERVIEW

Throughout the whole context of this data sheet, keep in mind the following voltage relations: 1) FBY is relative to the GND pin; FBY positive or negative current refers to current flowing into or out of the FBY pin 2) TG and $INTV_{EE}$ are relative to the BIAS pin; and 3) all other pins, including the BIAS pin, are relative to the $-V_{IN}$ pin.

The LT8709 uses a constant frequency, current mode control to provide excellent line and load regulation. The part's undervoltage lockout (UVLO) function, together with soft-start and frequency foldback, offers a controlled means of start-up. Output voltage, output current, and input voltage have control over the commanded peak current, which allows for a wide range of applications to be built using the LT8709. Synchronous switching makes high efficiency and high output current applications possible. When operating at light currents with the MODE pin > 1.224V (typical), the LT8709 will disable synchronous operation for part of the cycle to prevent negative switch currents. Refer to the Block Diagram (Figure 1) and the State Diagram (Figure 2) for the following description of the part's operation.

OPERATION – START-UP

Several functions are provided to enable a very clean start-up of the LT8709.

Precise Turn-On Voltages

The EN/FBIN pin has two voltage levels for activating the part: the 1st one enables the part and allows internal rails to operate; and the 2nd voltage threshold activates a soft-start cycle and thus allows switching to begin. To enable the part, take the EN/FBIN pin above 1.3V (typical). This comparator has 44mV of hysteresis to protect against glitches and slow ramping. To activate a soft-start cycle and allow switching, take the EN/FBIN above 1.7V (typical). When EN/FBIN exceeds 1.7V (typical), the logic state is latched so that if EN/FBIN drops between 1.3V to 1.7V (typical), the SS pin is not pulled low by the EN/FBIN pin. The EN/FBIN pin is also used for input voltage regulation which is at 1.607V (typical). Input voltage regulation is explained in more detail in the Operation – Regulation section. Taking the EN/FBIN pin below 0.3V shuts down the chip, resulting in extremely low quiescent current. See Figure 3 for the different EN/FBIN voltage thresholds.

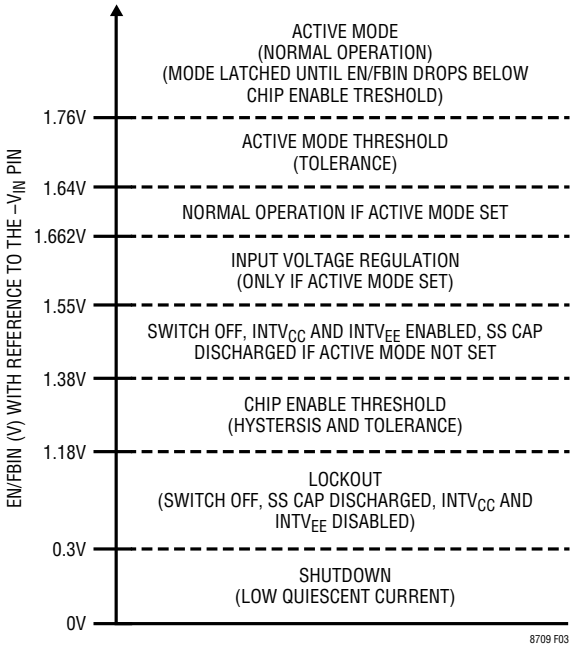


Figure 3. EN/FBIN Modes of Operation

Undervoltage Lockout (UVLO)

The LT8709 has internal UVLO circuitry that disables the chip when the greater of GND or BIAS < 4.5V (maximum) or $INTV_{CC}$ < 4V (typical). The EN/FBIN pin can also be used to create a configurable UVLO. See the Applications section for more information.

Soft-Start of Switch Current

The soft-start circuitry provides for a gradual rise of the switch current (refer to *Max Current Limit vs SS(CSP–CSN)* in Typical Performance Characteristics). When the part is brought out of shutdown, the external SS capacitor is first discharged, which resets the states of the logic circuits in the chip. Once $INTV_{CC}$ is out of UVLO (> 4V typical) and the chip is in active mode, an integrated 260k resistor pulls the SS pin to ~2.7V at a ramp rate set by the external capacitor connected to the pin. Typical values for the soft-start capacitor range from 100nF to 1µF. The soft-start capacitor should also be about 5× greater than the external capacitor connected to the IMON pin to avoid start-up issues.

OPERATION

Frequency Foldback

The frequency foldback circuitry reduces the switching frequency when the FBY pin current < 56.9µA (typical). This feature lowers the minimum duty cycle that the part can achieve, thus allowing better control of the inductor current at start-up. When the FBY current exceeds this value, the switching frequency returns to normal. If the part is configured to be in forced continuous conduction mode (MODE pin is driven below 1.175V), then the frequency foldback circuitry is disabled as long as $INTV_{EE}$ is not in UVLO and the SS pin is higher than the SS Hi threshold.

Note that the peak inductor current at start-up is a function of many variables including load profile, output capacitance, target V_{OUT}, V_{IN}, switching frequency, etc.

OPERATION – REGULATION

Use the Block Diagram when stepping through the following description of the LT8709 operating in regulation. Also, assume the converter's load current is high enough such that the part is operating in synchronous switching. The LT8709 has three modes of regulation:

1. Output Voltage (via FBY pin)
2. Input Voltage (via EN/FBIN pin)
3. Output Current (via ISP, ISN, and IMON pins)

All three of these regulation loops control the peak commanded current through the external NFET, MN. This operation is the same regardless of the regulation mode, so that will be described first.

At the start of each oscillator cycle, the SR latch (SR1) is set, which first turns off the external PFET, MP, and then turns on the external NFET, MN. The NFET's source current flows through an external current sense resistor (R_{SENSE1}) generating a voltage proportional to the NFET switch current. This voltage is then amplified by A5 and added to a stabilizing ramp. The resulting sum is fed into the positive terminal of the PWM comparator A6. When the voltage on the positive input of A6 exceeds the voltage on the negative input (V_C pin), the SR latch is reset, turning off the NFET and then turning on the PFET. The voltage on the V_C pin is controlled by one of the regulation loops, or a combination of regulation loops. For simplicity, each mode of regulation will be described independently so that only one of the regulation loops is in command of the LT8709.

Output Voltage Regulation

In most cases, a single external resistor is used to set the target output voltage. See the Pin Functions section for selecting the feedback resistor for a desired output voltage. The V_C pin voltage (negative input of A6) is set by EA1, which is an amplified difference between the FBX voltage, (the product of the FBY current and 7.25kΩ plus 0.6065V) and the reference voltage (1.213V). In this manner, the FBY error amplifier sets the correct peak current level to maintain output voltage regulation.

Input Voltage Regulation

There are two ways to set the input voltage regulation: a resistor divider to EN/FBIN between GND and $–V_{IN}$ or, a single resistor between GND and EN/FBIN pins. It is recommended to use a resistor divider for improved accuracy as described in the Setting the Input Voltage Regulation or Undervoltage Lockout section. The EN/FBIN pin voltage connects to the positive input of amplifier EA3. The V_C pin voltage is set by EA3, which is simply an amplified difference between the EN/FBIN pin voltage and a 1.607V reference voltage. In this manner, the EN/FBIN error amplifier sets the correct peak current level to maintain input voltage regulation.

Output Current Regulation

An external sense resistor connected between the ISP and ISN pins (R_{SENSE2}) sets the maximum output current of the converter and is placed in series either with the source of the PFET, MP, or in series with the converter output, depending on the type of converter. A built-in 51.8mV offset is added to the voltage seen across R_{SENSE2}. The sensed voltage along with the 51.8mV offset is then amplified and output to the IMON pin. An external capacitor must be placed from IMON to $–V_{IN}$ to filter the amplified chopped voltage that's sensed across R_{SENSE2}. The voltage at the IMON pin is fed to the negative input of the IMON error amplifier, EA2. The V_C pin voltage is set by EA2, which is simply an amplified difference between the IMON pin voltage and the 1.213V reference voltage. In this manner,

OPERATION

the IMON error amplifier sets the correct peak current level to maintain output current regulation.

Note that if the $INTV_{EE}$ LDO is in UVLO and SS > 1.8V (typical), then the voltage reference at the positive input of EA2 is 916mV (typical), resulting in limiting the output current to about half of the desired limit.

OPERATION – RESET CONDITIONS

The LT8709 has three reset cases. When the part is in reset, the SS pin is pulled low and both power switches, MN and MP, are forced off. Once all of the reset conditions are gone, the part is allowed to begin a soft-start sequence and switching can commence. Each of the following events can cause the LT8709 to be in reset:

1. UVLO
   a. The greater of GND and BIAS is < 4.5V (maximum)
   b. $INTV_{CC}$ < 4V (typical)
   c. EN/FBIN < 1.7V (typical) at the first power-up
2. Overcurrent sensed by IMON > 1.38V (typical)
3. Die Temperature > 175°C

OPERATION – POWER SWITCH CONTROL

The primary power switch is the external NFET (MN in Block Diagram) and the synchronous secondary power switch is the external PFET (MP in Block Diagram). The two switches are never on at the same time, and there is a non-overlap time of ~140ns and ~90ns from MP off to MN on and from MN off to MP on, respectively (see Electrical Characteristics) to prevent cross conduction. Figure 4 below shows the relative timing of the BG and TG (BIAS–TG) signals:

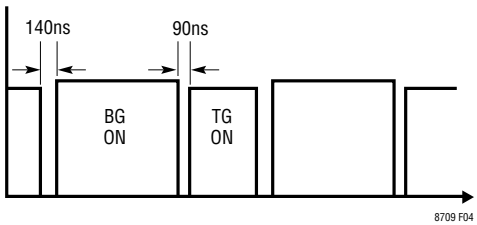


Figure 4. Synchronous Switching

Light Load Current (MODE Pin)

The MODE pin can be used to tell the LT8709 to operate in forced CCM regardless of load current, or operate in DCM at light loads.

- MODE < 1.175V (typical) = Forced CCM or FCM
- MODE > 1.224V (typical) = DCM

The forced continuous mode (FCM) allows the inductor current to reverse directions without any switches being forced off. At very light load currents, the inductor current will swing positive and negative as the appropriate average current is delivered to the output. There are some exceptions that negate the MODE pin and force the part to operate in DCM at light loads:

1. The $INTV_{EE}$ LDO is in UVLO (BIAS – $INTV_{EE}$ < 3.42V typical).
2. SS < 1.8V (typical).
3. The part is in a reset condition.

When the LT8709 is in discontinuous mode (DCM), synchronous switch MP is held off whenever MP's current falls near 0 current (less than 2.8mV (typical) across R_{SENSE2}). This is to prevent current draw from the output and/or feeding current to the input supply. Under very light loads, the current comparator A6, may also remain tripped for several cycles (i.e. skipping pulses). Since MP is held off during the skipped pulses, the inductor current will not reverse.

OPERATION – POWER GOOD (PG PIN)

The PG pin is an open-drain pin that functions as an active high power good pin. The PG pin has 100µs (typical) delay in order to reject glitches or transient events.

Power is good when FBY pin current is –74.9µA or 75.4µA (~90% of the regulation current), which corresponds to ~90% of the regulation voltage on V_{OUT}. The PG comparators have 7.65µA of hysteresis to reject glitches.

OPERATION

OPERATION – LDO REGULATORS ($INTV_{CC}$ AND $INTV_{EE}$)

The $INTV_{CC}$ LDO regulates to 6.3V (typical) and is used as the top rail for the BG gate driver. The $INTV_{CC}$ LDO can run from GND or BIAS and will minimize power losses by intelligently selecting the lower voltage as long as both are at a high enough voltage above $–V_{IN}$. The $INTV_{CC}$ regulator also has safety features to limit the power dissipation in the internal pass device and also to prevent it from damage if the pin is shorted to ground. The UVLO threshold on $INTV_{CC}$ is 4V (typical), and the LT8709 will be in reset until the LDO comes out of UVLO.

The $INTV_{EE}$ regulator regulates to 6.18V (typical) below the BIAS pin voltage. The BIAS and $INTV_{EE}$ voltages are used for the top and bottom rails of the TG gate driver respectively. Just like the $INTV_{CC}$ regulator, the $INTV_{EE}$ regulator has a safety feature to limit the power dissipation in the internal pass device. The TG pin can begin switching after the $INTV_{EE}$ regulator comes out of UVLO (3.42V typical across the BIAS and $INTV_{EE}$ pins) and the part is not in a reset condition.

APPLICATIONS INFORMATION

NEGATIVE BUCK CONVERTER COMPONENT SELECTION

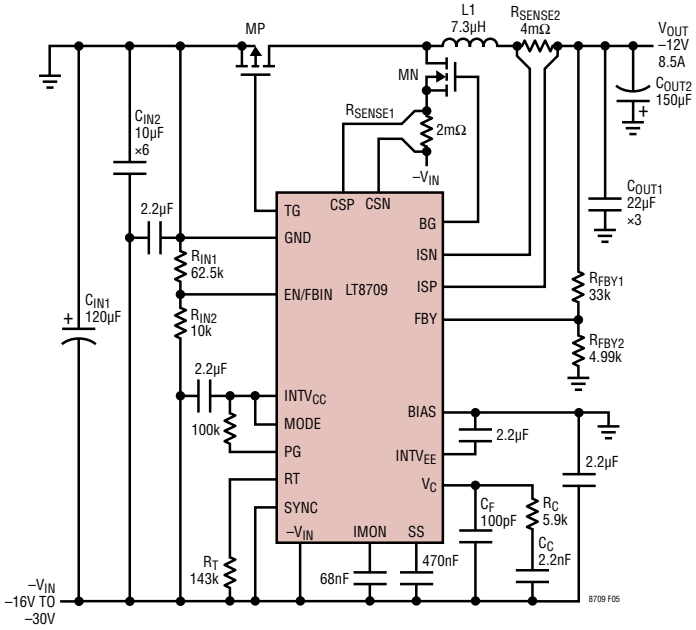


Figure 5. Negative Buck Converter – The Component Values Given are Typical for a 250kHz, –16V to –30V Input to –12V/8.5A Output Buck.

The LT8709 can be configured as a negative to less negative buck converter as in Figure 5. This topology generates a negative output voltage from a more negative input voltage. Resistors R_{FBY1} and R_{FBY2} set the output voltage by regulating FBY to –1.234V, referred to GND.

For a desired output load current at the negative output voltage over a given negative input voltage range, Table 1 is a step-by-step set of equations to calculate component values for the LT8709 when operating as a negative buck converter. Refer to this section and the Appendix for further information on the design equations presented in Table 1.

Variable Definitions:

$V_{IN(MIN)}$ = Minimum Input Voltage
$V_{IN(MAX)}$ = Maximum Input Voltage
V_{OUT} = Output Voltage
I_{OUT} = Output Load Current of Converter
f = Switching Frequency
DC_{MIN} = Power Switch Duty Cycle at $V_{IN(MAX)}$
DC_{MAX} = Power Switch Duty Cycle at $V_{IN(MIN)}$
V_{CSPN} = Current Limit Voltage at DC_{MAX}

Table 1. Negative Buck Design Equations

	Parameters/Equations
Step 1: Inputs	Pick V_{IN}, V_{OUT}, I_{OUT}, and f to calculate equations below.
Step 2: DC_{MAX} DC_{MIN}	$DC_{MAX} \cong \frac{V_{OUT}}{V_{IN(MIN)}}$; $DC_{MIN} \cong \frac{V_{OUT}}{V_{IN(MAX)}}$
Step 3: V_{CSPN}	See Max Current Limit vs Duty Cycle plot in Typical Performance Characteristics to find V_{CSPN} at DC_{MAX}.
Step 4: R_{SENSE1}	$R_{SENSE1} = 0.58 \bullet \frac{V_{CSPN}}{I_{OUT}}$
Step 5: R_{SENSE2}	$R_{SENSE2} = \frac{0.05}{1.6 \bullet I_{OUT}}$
Step 6: L	$L_{TYP} = \frac{R_{SENSE1} \bullet (\lvert V_{IN(MIN)} \rvert - \lvert V_{OUT} \rvert) \bullet DC_{MAX}}{12.5mV \bullet f}$ (1) $L_{MIN} \geq \frac{R_{SENSE1} \bullet \lvert V_{IN(MIN)} \rvert}{f \bullet 40mV \bullet DC_{MAX}} \bullet (2DC_{MAX} - 1)$ (2) $L_{MAX} \leq \frac{R_{SENSE1} \bullet (\lvert V_{IN(MIN)} \rvert - \lvert V_{OUT} \rvert) \bullet DC_{MAX}}{3mV \bullet f}$ (3) • Solve equations 1 to 3 for a range of L values. • The minimum value of the L range is the higher of L_{TYP} and L_{MIN}. The maximum of the L value range is L_{MAX}.
Step 7: C_{OUT}	$C_{OUT} \geq \frac{1 - DC_{MIN}}{8 \bullet L \bullet f^2 \bullet 0.005}$
Step 8: C_{IN}	$C_{IN} \geq \frac{I_{OUT} \bullet DC_{MAX} \bullet (1 - DC_{MAX})}{f \bullet 0.005 \bullet \lvert V_{IN(MIN)} \rvert}$
Step 9: C_{IMON}	$C_{IMON} \geq \frac{100\mu A \bullet DC_{MAX}}{0.005 \bullet f}$
Step 10: R_{FBY1}, R_{FBY2}	$R_{FBY2} = 4.99k\Omega$; $R_{FBY1} = \frac{\lvert V_{OUT} \rvert - 1.234V}{83.5\mu A + \frac{1.234V}{R_{FBY2}}}$
Step 11: R_T	$R_T = \frac{35,880}{f} - 1$; f in kHz and R_T in kΩ

NOTE: The final values for C_{OUT} and C_{IN} may deviate from the above equations in order to obtain desired load transient performance for a particular application. The C_{OUT} and C_{IN} equations assume zero ESR, so increase the capacitance accordingly based on the effective ESR.

APPLICATIONS INFORMATION

NEGATIVE INVERTING CONVERTER COMPONENT SELECTION

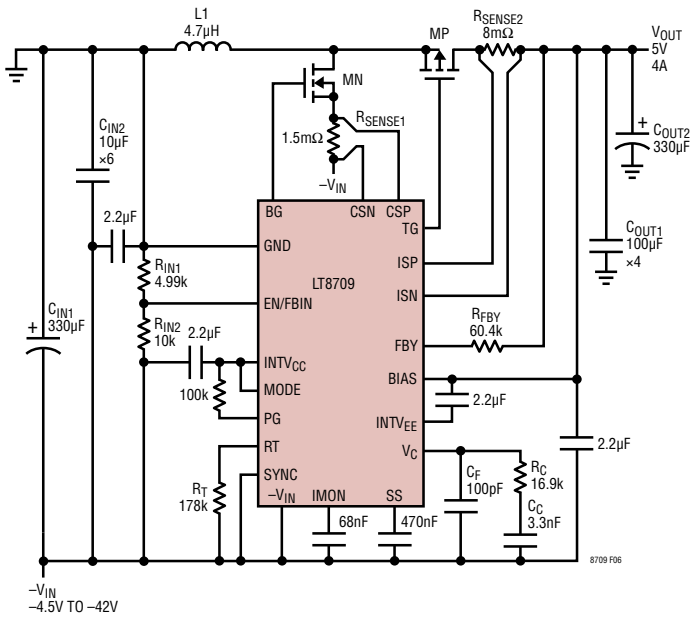


Figure 6. Negative Inverting Converter – The Component Values Given Are Typical for a 200kHz, –4.5V to –42V Input to 5V/4A Output.

The LT8709 can be configured as a negative to positive inverting converter as in Figure 6. This topology generates a positive output voltage from a negative input voltage with larger, equal or smaller magnitude. A single feedback resistor sets the output voltage by regulating FBY to –15.8mV with reference to the GND pin voltage.

For a desired output load current at the positive output voltage over a given negative input voltage range, Table 2 is a step-by-step set of equations to calculate component values for LT8709 when operating as a negative inverting converter. Refer to this section and the Appendix for further information on the design equations presented in Table 2.

Variable Definitions:

$V_{IN(MIN)}$ = Minimum Input Voltage
$V_{IN(MAX)}$ = Maximum Input Voltage
V_{OUT} = Output Voltage
I_{OUT} = Output Load Current of Converter
f = Switching Frequency
DC_{MIN} = Power Switch Duty Cycle at $V_{IN(MAX)}$
DC_{MAX} = Power Switch Duty Cycle at $V_{IN(MIN)}$
V_{CSPN} = Current Limit Voltage at DC_{MAX}

Table 2. Negative Inverting Converter Design Equations

	Parameters/Equations
Step 1: Inputs	Pick V_{IN}, V_{OUT}, I_{OUT}, and f to calculate equations below.
Step 2: DC_{MAX} DC_{MIN}	$DC_{MAX} \cong \frac{V_{OUT}}{V_{OUT}+\lvert V_{IN(MIN)}\rvert}$; $DC_{MIN} \cong \frac{V_{OUT}}{V_{OUT}+\lvert V_{IN(MAX)}\rvert}$
Step 3: V_{CSPN}	See Max Current Limit vs Duty Cycle plot in Typical Performance Characteristics to find V_{CSPN} at DC_{MAX}.
Step 4: R_{SENSE1}	$R_{SENSE1} = 0.58 \bullet \frac{V_{CSPN}}{I_{OUT}} \bullet (1-DC_{MAX})$
Step 5: R_{SENSE2}	$R_{SENSE2} = \frac{0.05}{1.6 \bullet I_{OUT}}$
Step 6: L	$L_{TYP} = \frac{R_{SENSE1} \bullet \lvert V_{IN(MIN)}\rvert \bullet DC_{MAX}}{12.5mV \bullet f}$ (1) $L_{MIN} \geq \frac{R_{SENSE1} \bullet \lvert V_{IN(MIN)}\rvert}{f \bullet 40mV \bullet DC_{MAX}} \bullet \left(\frac{2DC_{MAX}-1}{1-DC_{MAX}}\right)$ (2) $L_{MAX} \leq \frac{R_{SENSE1} \bullet \lvert V_{IN(MIN)}\rvert \bullet DC_{MAX}}{3mV \bullet f}$ (3) • Solve equations 1 to 3 for a range of L values. • The minimum value of the L range is the higher of L_{TYP} and L_{MIN}. The maximum of the L value range is L_{MAX}.
Step 7: C_{OUT}	$C_{OUT} \geq \frac{I_{OUT} \bullet DC_{MAX}}{f \bullet 0.005 \bullet V_{OUT}}$
Step 8: C_{IN}	$C_{IN} \geq \frac{I_{OUT} \bullet DC_{MAX}}{f \bullet 0.005 \bullet V_{IN(MIN)}}$
Step 9: C_{IMON}	$C_{IMON} \geq \frac{100\mu A \bullet DC_{MAX}}{0.005 \bullet f}$
Step 10: R_{FBY}	$R_{FBY} = \frac{\lvert V_{OUT}\rvert + 15.8mV}{83.9\mu A}$
Step 11: R_T	$R_T = \frac{35,880}{f} - 1$; f in kHz and R_T in kΩ

NOTE: The final values for C_{OUT} and C_{IN} may deviate from the above equations in order to obtain desired load transient performance for a particular application. The C_{OUT} and C_{IN} equations assume zero ESR, so increase the capacitance accordingly based on the effective ESR.

APPLICATIONS INFORMATION

NEGATIVE BUCK-BOOST CONVERTER COMPONENT SELECTION – COUPLED OR UNCOUPLED INDUCTORS

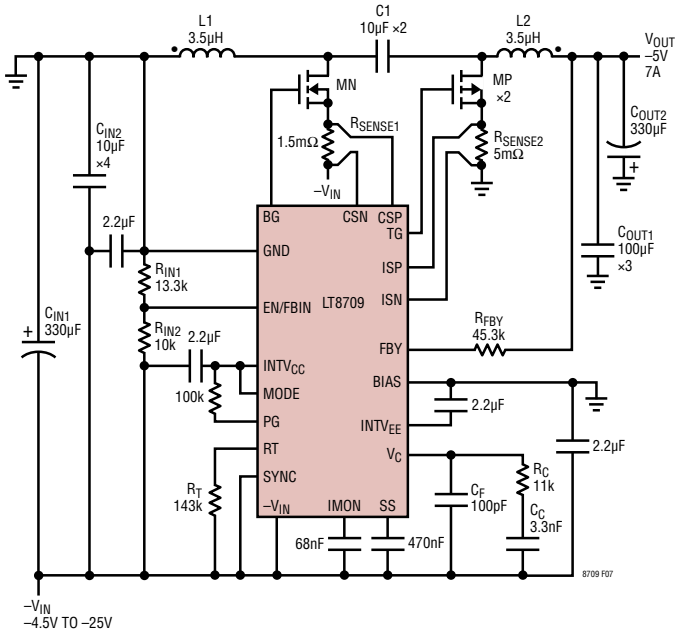


Figure 7. Negative Buck-Boost Converter – The Component Values Given Are Typical for a 250kHz, –4.5V to –25V Input to –5V/7A Buck-Boost Topology Using Coupled Inductors.

The LT8709 can be configured as a negative buck-boost as in Figure 7. This topology generates a negative output voltage from a more, equal or less negative input voltage with very low output voltage ripple due to inductor L2 in series with the output. Output disconnect is built into the topology through C1, meaning no DC path exists between the input and output. GND-referred FBY is regulated to –1.234V through a single resistor between V_{OUT} and FBY.

For a desired output load current at the negative output voltage over a given negative input voltage range, Table 3 is a step-by-step set of equations to calculate component values for LT8709 when operating as a negative buck-boost converter. Refer to more detail in this section and the Appendix for the design equations.

Variable Definitions:

$V_{IN(MIN)}$ = Minimum Input Voltage
V_{OUT} = Output Voltage
I_{OUT} = Output Load Current of Converter
f = Switching Frequency
$V_{IN(MAX)}$ = Maximum Input Voltage
DC_{MIN} = Power Switch Duty Cycle at $V_{IN(MAX)}$
DC_{MAX} = Power Switch Duty Cycle at $V_{IN(MIN)}$
V_{CSPN} = Current Limit Voltage at DC_{MAX}

Table 3. Negative Buck-Boost Design Equations

	Parameters/Equations
Step 1: Inputs	Pick V_{IN}, V_{OUT}, I_{OUT}, and f to calculate equations below.
Step 2: DC_{MAX} DC_{MIN}	$DC_{MAX} \cong \frac{V_{OUT}}{V_{OUT}+V_{IN(MIN)}}$; $DC_{MIN} \cong \frac{V_{OUT}}{V_{OUT}+V_{IN(MAX)}}$
Step 3: V_{CSPN}	See Current Limit vs Duty Cycle plot in Typical Performance Characteristics to find V_{CSPN} at DC_{MAX}.
Step 4: R_{SENSE1}	$R_{SENSE1} = 0.58 \bullet \frac{V_{CSPN}}{I_{OUT}} \bullet (1-DC_{MAX})$
Step 5: R_{SENSE2}	$R_{SENSE2} = \frac{0.05}{1.6 \bullet I_{OUT}}$
Step 6: L	$L_{TYP} = \frac{R_{SENSE1} \bullet \lvert V_{IN(MIN)} \rvert \bullet DC_{MAX}}{12.5mV \bullet f}$ (1) $L_{MIN} \geq \frac{R_{SENSE1} \bullet \lvert V_{IN(MIN)} \rvert}{f \bullet 40mV \bullet DC_{MAX}} \bullet \left(\frac{2DC_{MAX}-1}{1-DC_{MAX}}\right)$ (2) $L_{MAX} \leq \frac{R_{SENSE1} \bullet \lvert V_{IN(MIN)} \rvert \bullet DC_{MAX}}{3mV \bullet f}$ (3) • Solve equations 1 to 3 for a range of L values. • The minimum value of the L range is the higher of L_{TYP} and L_{MIN}. The maximum of the L value range is L_{MAX}. • $L = L_1 = L_2$ for coupled inductors. • $L = L_1 \parallel L_2$ for uncoupled inductors.
Step 7: C1	$C_1 \geq 10\mu F$ (TYPICAL; $V_{RATING} > \lvert V_{OUT} \rvert$)
Step 8: C_{OUT}	$C_{OUT} \geq \frac{1-DC_{MIN}}{8 \bullet L \bullet f^2 \bullet 0.005}$
Step 9: C_{IN}	$C_{IN} \geq \frac{I_{OUT} \bullet DC_{MAX}}{f \bullet 0.005 \bullet \lvert V_{IN(MIN)} \rvert}$
Step 10: C_{IMON}	$C_{IMON} \geq \frac{100\mu A \bullet DC_{MAX}}{0.005 \bullet f}$
Step 11: R_{FBY}	$R_{FBY} = \frac{\lvert V_{OUT} \rvert - 1.234V}{83.5\mu A}$
Step 12: R_T	$R_T = \frac{35,880}{f} - 1$; f in kHz and R_T in kΩ

NOTE: The final values for C_{OUT} and C_{IN} may deviate from the above equations in order to obtain desired load transient performance for a particular application. The C_{OUT} and C_{IN} equations assume zero ESR, so increase the capacitance accordingly based on the effective ESR.

APPLICATIONS INFORMATION

NEGATIVE BOOST COMPONENT SELECTION – COUPLED OR UNCOUPLED INDUCTORS

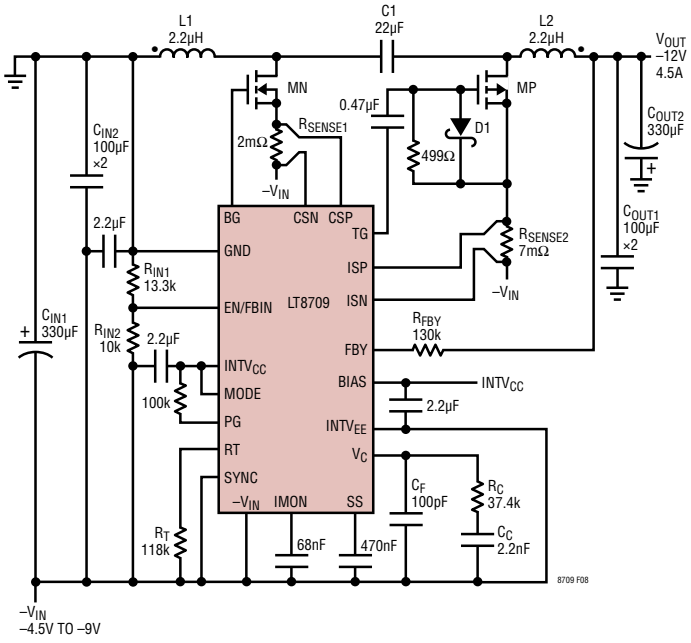


Figure 8. Negative Boost Converter – The Component Values Given Are Typical for a 300kHz, –4.5V to –9V Input to –12V/4.5A Output Boost Topology Using Coupled Inductors.

The LT8709 can work in a negative boost configuration as in Figure 8. Changing the connection from GND to $-V_{IN}$ for the source of the PFET in the negative buck-boost topology (Figure 7) results in generating a more negative output voltage. This solution gives rise to very low output voltage ripple due to inductor L2 in series with the output. FBY is regulated to –1.234V with reference to the GND pin voltage.

For a desired output current and output voltage over a given input voltage range, Table 4 is a step-by-step set of equations to calculate component values for the LT8709 when operating as a negative boost converter. Refer to this section and the Appendix for further information on the design equations presented in Table 4.

Variable Definitions:

$V_{IN(MIN)}$ = Minimum Input Voltage
$V_{IN(MAX)}$ = Maximum Input Voltage
V_{OUT} = Output Voltage
I_{OUT} = Output Current of Converter
f = Switching Frequency
DC_{MIN} = Power Switch Duty Cycle at $V_{IN(MAX)}$
DC_{MAX} = Power Switch Duty Cycle at $V_{IN(MIN)}$
V_{CSPN} = Current Limit Voltage at DC_{MAX}

Table 4. Negative Boost Design Equations

	Parameters/Equations
Step 1: Inputs	Pick V_{IN}, V_{OUT}, I_{OUT}, and f to calculate equations below.
Step 2: DC_{MAX}; DC_{MIN}	$DC_{MAX} \cong 1-\frac{V_{IN(MIN)}}{V_{OUT}}$; $DC_{MIN} \cong 1-\frac{V_{IN(MAX)}}{V_{OUT}}$
Step 3: V_{CSPN}	See Current Limit vs Duty Cycle plot in Typical Performance Characteristics to find V_{CSPN} at DC_{MAX}.
Step 4: R_{SENSE1}	$R_{SENSE1} = 0.58 \bullet \frac{V_{CSPN}}{I_{OUT}} \bullet (1-DC_{MAX})$
Step 5: R_{SENSE2}	$R_{SENSE2} = \frac{0.05}{1.6 \bullet I_{OUT}}$
Step 6: L	$L_{TYP} = \frac{R_{SENSE1} \bullet \lvert V_{IN(MIN)} \rvert \bullet DC_{MAX}}{12.5mV \bullet f}$ (1) $L_{MIN} \geq \frac{R_{SENSE1} \bullet \lvert V_{IN(MIN)} \rvert \bullet (2DC_{MAX}-1)/(1-DC_{MAX})}{f \bullet 40mV \bullet DC_{MAX}}$ (2) $L_{MAX} \leq \frac{R_{SENSE1} \bullet \lvert V_{IN(MIN)} \rvert \bullet DC_{MAX}}{3mV \bullet f}$ (3) • Solve equations 1 to 3 for a range of L values. • The minimum value of the L range is the higher of L_{TYP} and L_{MIN}. The maximum of the L value range is L_{MAX}. • $L = L_1 = L_2$ for coupled inductors. • $L = L_1 \parallel L_2$ for uncoupled inductors.
Step 7: C1	$C_1 \geq 10\mu F$ (TYPICAL; $V_{RATING} > \lvert V_{OUT} \rvert$)
Step 8: C_{OUT}	$C_{OUT} \geq \frac{1-DC_{MIN}}{8 \bullet L \bullet f^2 \bullet 0.005}$
Step 9: C_{IN}	$C_{IN} \geq \frac{DC_{MAX}}{8 \bullet L \bullet f^2 \bullet 0.005}$
Step 10: C_{IMON}	$C_{IMON} \geq \frac{100\mu A \bullet DC_{MAX}}{0.005 \bullet f}$
Step 11: R_{FBY}	$R_{FBY} = \frac{\lvert V_{OUT} \rvert - 1.234V}{83.5\mu A}$
Step 12: R_T	$R_T = \frac{35,880}{f} - 1$; f in kHz and R_T in kΩ

NOTE: The final values for C_{OUT} and C_{IN} may deviate from the above equations in order to obtain desired load transient performance for a particular application. The C_{OUT} and C_{IN} equations assume zero ESR, so increase the capacitance accordingly based on the combined ESR.

APPLICATIONS INFORMATION

SETTING THE OUTPUT VOLTAGE REGULATION

In most cases the LT8709 output voltage is set by connecting an external resistor (R_{FBY}) from the converter's output, V_{OUT}, to the FBY pin. The equations below determine R_{FBY}:

$$R_{FBY} = \frac{|V_{OUT}| - 1.234V}{83.5\mu A} \text{ NEGATIVE OUTPUT VOLTAGE}$$

$$R_{FBY} = \frac{V_{OUT} + 15.8mV}{83.9\mu A} \text{ POSITIVE OUTPUT VOLTAGE}$$

See the Electrical Characteristics for tolerances on the FBY regulation voltage and current.

SETTING THE INPUT VOLTAGE REGULATION OR UNDERVOLTAGE LOCKOUT

A resistor divider between $-V_{IN}$ and GND, connected to the EN/FBIN pin, provides a means to regulate the input voltage or to create an undervoltage lockout function. Referring to error amplifier EA3 in the block diagram, when EN/FBIN is lower than the 1.607V reference, V_C is pulled low. For example, if the negative input voltage is provided by a relatively high impedance source (e.g. a solar panel) and the current draw pulls the magnitude of the input voltage below a preset limit, V_C will be reduced, thus reducing current draw from the input supply and limiting the input voltage drop. Note that using this function in forced continuous mode (MODE pin low) can result in current being drawn from the output and forced into the input. If this behavior is not desired then set the MODE pin high to prevent reverse current flow.

To set the minimum or regulated input voltage use:

$$|V_{IN(MIN-REG)}| = 1.607V \bullet \left(1 + \frac{R_{IN1}}{R_{IN2}}\right) + 17.6\mu A \bullet R_{IN1}$$

$$R_{IN1} = \frac{|V_{IN(MIN-REG)}| - 1.607V}{\left(\frac{1.607V}{R_{IN2}}\right) + 17.6\mu A}$$

where R_{IN1} and R_{IN2} are shown in Figure 9. For increased accuracy, set $R_{IN2} \leq 10k$. The resistor R_{IN2} is optional, but is recommended to be used to increase the accuracy of the input voltage regulation by making the R_{IN1} current much higher than the EN/FBIN pin current.

This same technique can be used to create an undervoltage lockout if the LT8709 is NOT in forced continuous mode.

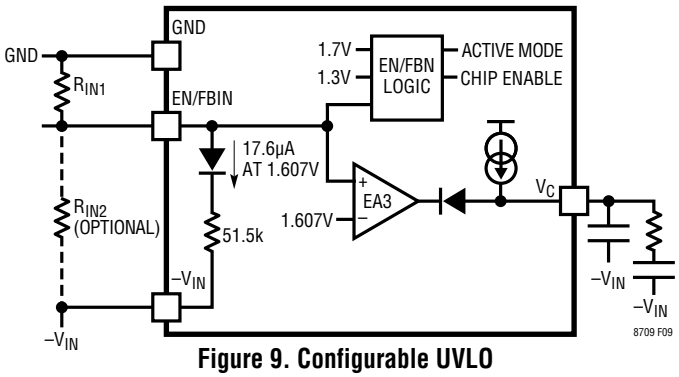


Figure 9. Configurable UVLO

When in discontinuous mode, forcing V_C low will stop all switching activity. Note that this does not reset the soft start, therefore resumption of switching activity will not be accompanied by a soft-start.

Note that at start-up, the minimum voltage on EN/FBIN must exceed 1.7V (typical) to begin a soft-start cycle. Afterwards, the EN/FBIN voltage can drop below 1.7V and the input can be regulated such that the EN/FBIN voltage is at ~1.607V. So the equation below gives the start-up input voltage for a desired input regulation voltage:

$$|V_{IN(START-UP)}| = \frac{1.7V}{1.607V} \bullet |V_{IN(MIN-REG)}| + 0.78\mu A \bullet R_{IN1}$$

OUTPUT CURRENT MONITORING AND LIMITING (R_{SENSE2} AND ISP-ISN AND IMON PINS)

The LT8709 has an output current monitor circuit that can be used to monitor and/or limit the output current. The current monitor circuit works as shown in Figure 10. If it is not desirable to monitor and limit the output current, simply connect the IMON pin to the chip ground i.e., $-V_{IN}$. Note that the current sense resistor connected to the ISP and ISN pins must still be used, and the value should follow the guidelines in the next couple sections.

APPLICATIONS INFORMATION

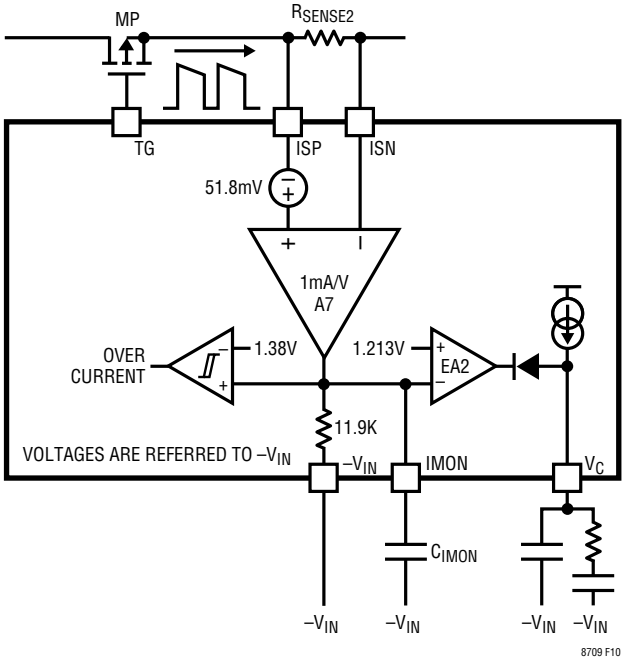


Figure 10. Output Current Monitor and Control

The current through R_{SENSE2} is the sensed current through MP which turns on and off every clock cycle. Since the current through R_{SENSE2} is chopped, a filtering capacitor between the IMON and $–V_{IN}$ pins is needed to filter the voltage at the IMON pin before heading to EA2. Given below is the equation to calculate the required IMON pin capacitance:

$$C_{IMON} \geq \frac{100\mu A \bullet DC_{MAX}}{5mV \bullet f}$$

where DC_{MAX} is the maximum duty cycle of the converter's application (with minimum input magnitude) and f is the switching frequency.

To prevent start-up issues, the IMON capacitor should charge up faster than the SS capacitor. It is recommended to size the SS capacitor about 5x greater than the IMON capacitor.

Output Current Monitoring

The voltage at the IMON pin is a gained up version of the voltage seen across the ISP and ISN pins. Given below are the equations relating the R_{SENSE2} current to the IMON pin voltage. Assume that the current through R_{SENSE2} is of steady state and that its time average is approximately equal to the converter's load current:

$$V_{IMON} = 11.9 \bullet \left(I_{RSENSE2(AVE)} \bullet R_{SENSE2} + 51.8mV\right)$$

$$I_{OUT} \approx I_{SENSE2(AVE)} = \frac{\left(\frac{V_{IMON}}{11.9} - 51.8mV\right)}{R_{SENSE2}}$$

Output Current Limiting

As shown in Figure 10, IMON voltages exceeding 1.213V (typical) cause the V_C voltage to reduce, thus limiting the inductor current. This voltage on IMON corresponds to an average voltage of 50mV across R_{SENSE2}. The equation below is used to select the R_{SENSE2} resistor for limiting the output current at steady state:

$$R_{SENSE2} = \frac{50mV}{I_{OUT(LIMIT)}}$$

If it is not desirable to limit the output current, size R_{SENSE2} by setting $I_{OUT(LIMIT)}$ 60% higher than the maximum output current of the converter. This current sense resistor is needed if using the synchronous PFET in the converter. When the PFET is replaced with a Schottky power diode, then R_{SENSE2} is not needed if output current limiting or monitoring isn't required.

Note that if the $INTV_{EE}$ LDO is in UVLO and SS > 1.8V (typical), then the reference voltage at EA2 reduces to 916mV, and the output current is limited to about half its set value.

Output Overcurrent

As shown in Figure 10, a comparator monitors the voltage at the IMON pin and triggers a reset condition if the IMON pin voltage exceeds 1.38V (typical). This corresponds to an average voltage of 63.6mV (typical) across the ISP and ISN pins:

$$I_{OUT(OVERCURRENT)} = \frac{63.6mV}{R_{SENSE2}}$$

$$I_{OUT(OVERCURRENT)} = 1.27 \bullet I_{OUT(LIMIT)}$$

APPLICATIONS INFORMATION

Capacitor Charging

When the application is to charge a bank of capacitors such as SuperCaps, the charging current is set by R_{SENSE2}.

SWITCH CURRENT LIMIT (R_{SENSE1} AND CSP-CSN PINS)

The external current sense resistor (R_{SENSE1}) sets the maximum peak current though the external NFET switch (MN). The maximum voltage across R_{SENSE1} is 50mV (typical) at very low switch duty cycles, and then slope compensation decreases the current limit as the duty cycle increases (see the *Max Current Limit vs Duty Cycle (CSP-CSN)* plot in the Typical Performance Characteristics). The equation below gives the switch current limit for a given duty cycle and current sense resistor (find V_{CSPN} at the operating duty cycle in the plot mentioned).

$$I_{SW(LIMIT)} = \frac{V_{CSPN}}{R_{SENSE1}}$$

To provide a desired load current for any given application, R_{SENSE1} must be sized appropriately. The switch current will be at its highest when the input voltage magnitude is at the lowest of its range. The equation below calculates R_{SENSE1} for a desired output current:

$$R_{SENSE1} \leq 0.74 \bullet \eta \bullet \frac{V_{CSPN}}{I_{OUT}} \bullet (1 - DC_{MAX}) \bullet \left(1 - \frac{i_{RIPPLE}}{2}\right)$$

where

η = Conversion efficiency (assume ~90%)

V_{CSPN} = Max current limit voltage (see *Max Current Limit vs Duty Cycle (CSP-CSN)* plot in the Typical Performance Characteristics)

I_{OUT} = Converter load current

DC_{MAX} = Switching duty cycle at minimum magnitude V_{IN} (see Power Switch Duty Cycle in Appendix)

i_{RIPPLE} = Peak-to-peak inductor ripple current percentage at minimum magnitude V_{IN} (recommended to use 25%)

REVERSE CURRENT APPLICATIONS (MODE PIN LOW)

When the forced continuous mode is selected (MODE pin low), inductor current is allowed to reverse directions and flow from the output side to the input side. This can lead to current sinking from the output and being forced into the input. The reverse current is at a maximum magnitude when V_C is lowest. The graph of *Maximum Current Limit vs Duty Cycle (CSP – CSN)* in the Typical Performance Characteristics section can help to determine the maximum reverse current capability.

The IMON pin voltage will indicate negative inductor currents. Note that the IMON voltage is only accurate if the dynamic input of the output current sense amp stays within –51.8mV to 500mV.

If the inductor current goes more negative than –300mV as sensed by R_{SENSE2}, the external PFET will turn off, and the inductor current will start going more positive.

Input Overvoltage Protection

Whenever the MODE pin is low to allow current to flow from output to input, it is strongly recommended to add a couple external components to protect the input from overvoltage as shown in Figure 11 below. With either approach, as $–V_{IN}$ approaches the OVP point, the MODE pin approaches the MODE FCM threshold (1.224V typical) and the LT8709 won't allow reverse current flow, preventing $–V_{IN}$ from going below the OVP point.

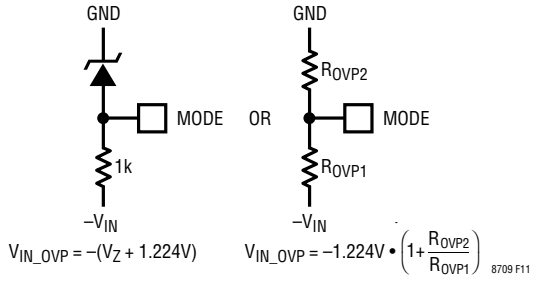


Figure 11. Input Overvoltage Protection

APPLICATIONS INFORMATION

CURRENT SENSE FILTERING

Certain applications may require filtering of the inductor current sense signals due to excessive switching noise that can appear across R_{SENSE1} and/or R_{SENSE2}. Higher operating voltages, higher values of R_{SENSE}, and more capacitive MOSFETs will all contribute additional noise across R_{SENSE} when MOSFETs transition. The CSP/CSN and/or the ISP/ISN sense signals can be filtered by adding one of the RC networks shown in Figure 12. The filter shown in Figure 12a filters out differential noise, whereas the filter in Figure 12b filters out differential and common mode noise at the expense of an additional capacitor and approximately twice the capacitance value. It is recommended to Kelvin connect the $-V_{IN}$ sides of the filter caps directly to the paddle of the LT8709 if using the filter in Figure 12b. The filter network should be placed as close as possible to the LT8709. Resistors greater than 10Ω should be avoided as this can increase the offset voltages at the CSP/CSN and ISP/ISN pins. The RC product should be kept less than 30ns, which is simply the total series R (5.1Ω+5.1Ω in this case) times the equivalent capacitance seen across the sense pins (2.2nF for Figure 12a and 2.35nF for Figure 12b).

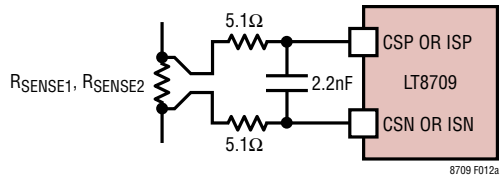


Figure 12a. Differential RC Filter on CSP/CSN and/or ISP/ISN Pins

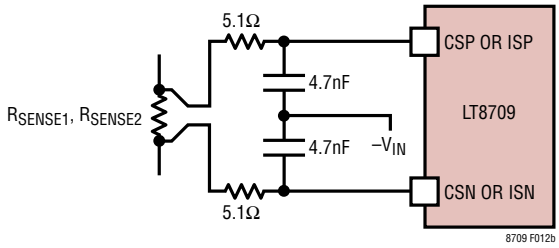


Figure 12b. Differential and Common Mode RC Filter on CSP/CSN and/or ISP/ISN Pins

SWITCHING FREQUENCY

The LT8709 runs with a constant frequency between 100kHz and 750kHz. The frequency can be set using the internal oscillator or can be synchronized to an external clock source. Selection of the switching frequency is a trade-off between efficiency and component size. Low frequency operation increases efficiency by reducing MOSFET switching losses, but requires larger inductance and/or capacitance to maintain low output ripple voltage. For high power applications, consider operating at lower frequencies to minimize MOSFET heating from switching losses. To use the on-chip oscillator, the switching frequency can be set by placing an appropriate resistor from the RT pin to $-V_{IN}$, the chip ground and tying the SYNC pin to $-V_{IN}$, the logic low. The frequency can also be synchronized to an external clock source driven into the SYNC pin, as long as the logic levels appearing at the SYNC pin are relative to the chip ground (i.e., $-V_{IN}$). The following sections provide more details.

Oscillator Timing Resistor (R_T)

The operating frequency of the LT8709 can be set by the internal free-running oscillator. When the SYNC pin is driven low (< 0.4V), the frequency of operation is set by a resistor from the RT pin to $-V_{IN}$. The oscillator frequency is calculated using the following formula:

$$f_{OSC} = \frac{35,880}{(R_T + 1)}$$

where f_{OSC} is in kHz and R_T is in kΩ. Conversely, R_T (in kΩ) can be calculated from the desired frequency (in kHz) using:

$$R_T = \frac{35,880}{f_{OSC}} - 1$$

Clock Synchronization

With proper logic levels, an external source can set the operating frequency for LT8709 by providing a digital clock signal into the SYNC pin (R_T resistor still required). That way, the LT8709 will operate with this overriding SYNC clock frequency. The LT8709 will revert to its internal free-running oscillator clock when the SYNC pin is driven to logic low, i.e., below 0.4V for a few free-running clock periods.

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Driving SYNC high, i.e., ≥1.5V for an extended period of time effectively stops the operating clock and prevents latch SR1 from becoming set (see Block Diagram). As a result, the switching operation of the LT8709 will stop.

The duty cycle of the SYNC signal must be between 20% and 80% for proper operation. Also, the frequency of the SYNC signal must meet the following two criteria:

1. SYNC may not toggle outside the frequency range of 100kHz to 750kHz.
2. The SYNC frequency can always be higher than the free-running oscillator frequency (as set by the R_T resistor), f_{OSC}, but should not be less than 75% of f_{OSC}.

After SYNC begins toggling, it is recommended that switching activity is stopped before the SYNC pin stops toggling. Excess negative inductor current can result when SYNC stops toggling as the LT8709 transitions from the external SYNC clock source to the internal free-running oscillator clock. Switching activity can be stopped by driving the EN/FBIN pin low.

LEVEL SHIFTER CIRCUITS

It is often the case that the user has a GND referenced signal and would like to be able to externally control the part. This could include using a signal to enable the part, read the logic state of power good (PG), or to sync the part to a clock. The following circuits below level shift the input signal with respect to $–V_{IN}$ to achieve these functions.

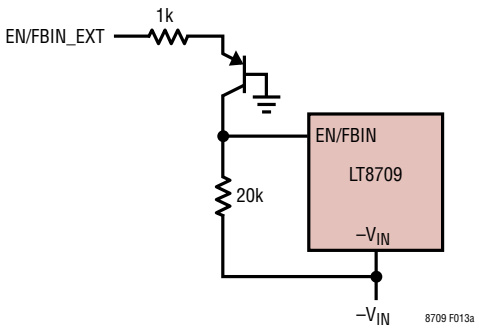

Figure 13a. Level Shifter Circuit for EN/FBIN

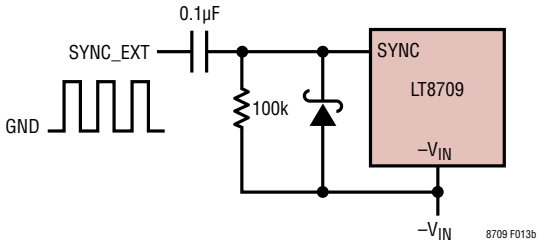

Figure 13b. Level Shifter Circuit for SYNC

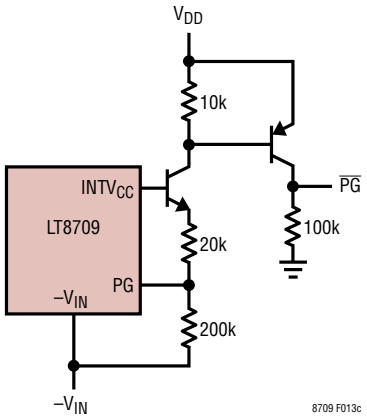

Figure 13c. Level Shifter Circuit for PG

LDO REGULATORS

The LT8709 has two linear regulators to run the BG and TG gate drivers. The $INTV_{CC}$ LDO regulates to 6.3V (typical) above the $–V_{IN}$ pin, and the $INTV_{EE}$ regulator regulates 6.18V (typical) below the BIAS pin.

$INTV_{CC}$ LDO Regulator

The $INTV_{CC}$ LDO is used as the top rail for the BG gate driver of the primary switch, which is an N-type power MOSFET with its source connected to the chip ground (i.e., $–V_{IN}$) in any applications of the LT8709. The $INTV_{CC}$ LDO is also used as the top rail for the TG gate driver for applications in which BIAS and $INTV_{EE}$ are tied to $INTV_{CC}$ and $–V_{IN}$, respectively. An external capacitor of 2.2µF or greater must be placed from the $INTV_{CC}$ pin to $–V_{IN}$. The UVLO threshold on $INTV_{CC}$ is 4V (typical), and the LT8709 will be in reset until the LDO comes out of UVLO.

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The $INTV_{CC}$ LDO can run from GND or BIAS and will minimize power losses by intelligently selecting the lower voltage one as long as both are at a high enough voltage above $–V_{IN}$. For example, the following is a plot that shows an inverting application where V_{OUT}/BIAS is regulated to 5V while $–V_{IN}$ starts at –10V and ramps to –5V; and indicates that $INTV_{CC}$ is regulated from GND or BIAS. It should be noted that all voltages in the plot are relative to $–V_{IN}$.

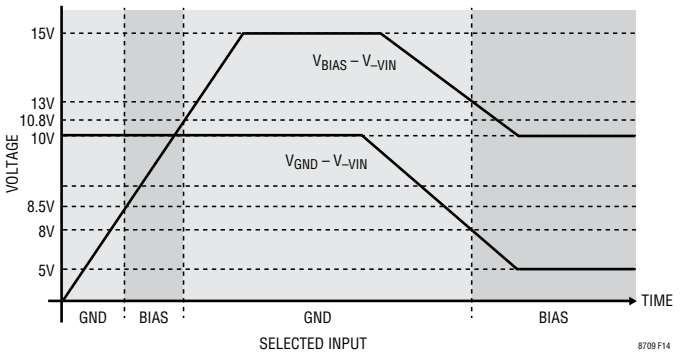

Figure 14. $INTV_{CC}$ Input Voltage Selection

Overcurrent protection circuitry typically limits the maximum current draw from the LDO to 125mA and 65mA when running from GND and BIAS respectively. When $INTV_{CC}$ is below ~3.5V during start-up or an overload condition, the typical current limit is reduced to 25mA when running from either GND or BIAS. If the selected input voltage is greater than 20V (typical), then the current limit of the LDO reduces linearly with input voltage to limit the maximum power in the $INTV_{CC}$ pass device. See the *$INTV_{CC}$ Current Limit vs GND or BIAS* plot in the Typical Performance Characteristics. If the die temperature exceeds 175°C (typical), the current limit of the LDO drops to 0.

Power dissipated in the $INTV_{CC}$ LDO should be minimized to improve efficiency and prevent overheating of the LT8709. The current limit reduction with input voltage circuit helps prevent the part from overheating, but these guidelines should be followed. The maximum current drawn through the $INTV_{CC}$ LDO occurs under the following conditions:

1. Large (capacitive) MOSFETs being driven at high frequencies.
2. The converter's switching-node voltage ($|V_{IN}|$ for negative buck, $|V_{IN}| + V_{OUT}$ for negative inverter, or $|V_{IN}| + |V_{OUT}|$ for negative boost or buck-boost) is high, thus requiring more charge to turn the MOSFET gates on and off.

In general, use appropriately sized MOSFETs and lower the switching frequency for higher voltage applications to keep the $INTV_{CC}$ current at a minimum.

$INTV_{EE}$ LDO Regulator

The BIAS and $INTV_{EE}$ voltages are used for the top and bottom rails of the TG gate driver respectively. An external capacitor of 2.2µF or greater must be placed between the BIAS and $INTV_{EE}$ pins. The UVLO threshold on the regulator (BIAS-$INTV_{EE}$) is 3.42V (typical) as long as the BIAS voltage is greater than ~3.36V. The TG pin can begin switching after the $INTV_{EE}$ regulator comes out of UVLO. For positive output converters, BIAS must be tied to the converter's output voltage. For a negative buck or negative buck-boost converter, BIAS must connect to GND. For a negative boost converter, BIAS must tie to $INTV_{CC}$, and $INTV_{EE}$ ties to $–V_{IN}$. In the third case, the voltage of the $INTV_{EE}$ regulator is driven to the $INTV_{CC}$ voltage of 6.3V and hence the TG gate driver will have $–V_{IN}$ referred levels of 0V and 6.3V.

Overcurrent protection circuitry typically limits the maximum current draw from the regulator to 65mA. If the BIAS voltage is greater than 20V (typical), then the current limit of the regulator reduces linearly with input voltage to limit the maximum power in the $INTV_{EE}$ pass device. See the *$INTV_{EE}$ Current Limit vs BIAS* plot in the Typical Performance Characteristics. If the die temperature exceeds 175°C (typical), the current limit of the LDO drops to zero.

The thermal guidelines from the $INTV_{CC}$ LDO Regulator section apply to the $INTV_{EE}$ regulator as well.

NON-SYNCHRONOUS CONVERTER

It may be desirable in some applications to replace the external PFET with a Schottky diode to make a non-synchronous converter. One example would be a high

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output voltage application because the voltage drop across the rectifier has a small effect on the efficiency of the converter. In fact, replacing the PFET with a Schottky may result in higher efficiency because the LT8709 doesn't have to supply gate drive to the PFET. Figure 15 shows the recommended connections for using the LT8709 as a non-synchronous negative buck-boost converter, however the same concept can be used for any other converter.

Note that the MODE pin must be tied high if using the LT8709 as a non-synchronous converter or else the output might not be regulated at light load. Also, the TG pin must be left floating or permanent damage could occur to the TG gate driver. If it is not desirable to monitor and/or control the output current, R_{SENSE2} is not needed and simply tie the ISP and ISN pins to GND. The IMON pin can be left floating or connected to $-V_{IN}$. The BIAS and $INTV_{EE}$ pins can tie to $-V_{IN}$ if the dual input feature of the $INTV_{CC}$ LDO is not needed and the input voltage magnitude stays above 4.5V.

LAYOUT GUIDELINES FOR APPLICATIONS

General Layout Guidelines

- To optimize thermal performance, solder the exposed pad of the LT8709 to the chip ground plane (i.e., $-V_{IN}$) with multiple vias around the pad connecting to additional $-V_{IN}$ planes.
- High speed switching path (see specific topology below for more information) must be kept as short as possible.
- The FBY, V_C, IMON, and RT components should be placed as close to the LT8709 as possible, while being far away as practically possible from switching nodes. The $-V_{IN}$ node/plane for these components should be separated from the switch current path.
- Place bypass capacitors for the GND and BIAS pins (C_{GND} and C_{BIAS}) as close as possible to the LT8709.
- Place bypass capacitors for the $INTV_{CC}$ and $INTV_{EE}$ pins (C_{VCC} and C_{VEE}) as close as possible to the LT8709.
- The load should connect directly to the positive and negative terminals of the output capacitor for best load regulation.

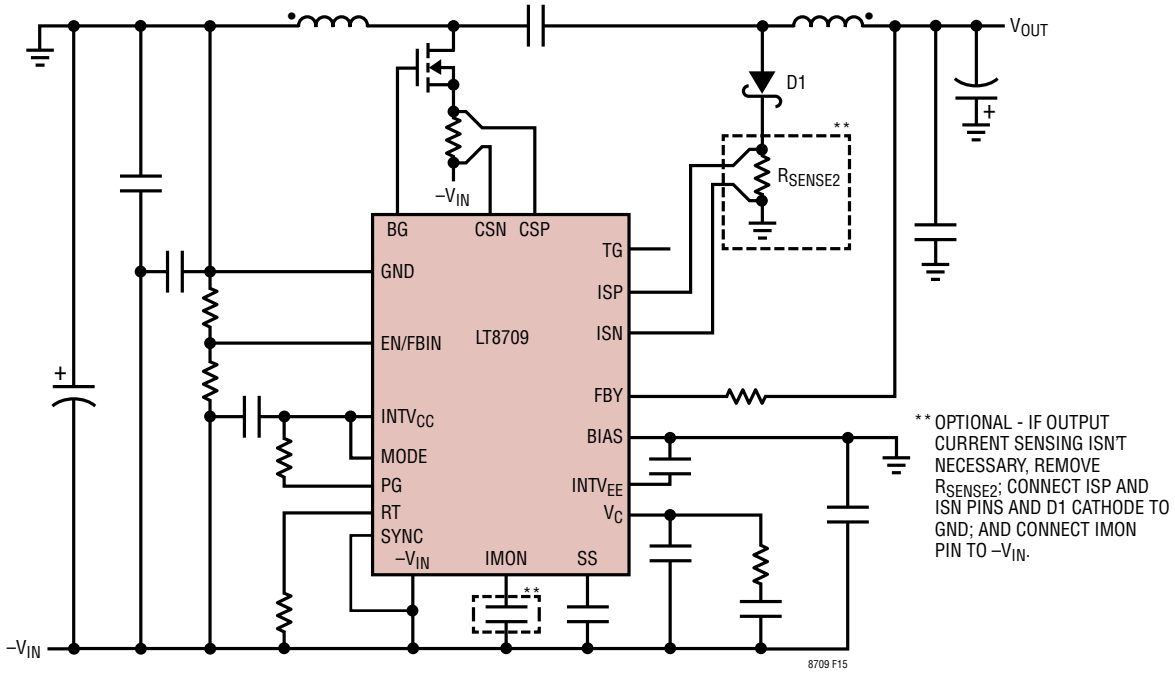

Figure 15. Nonsynchronous Negative Buck-Boost

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Negative Inverting Topology Specific Layout Guidelines

- Keep length of loop (high speed switching path) governing C_{IN2}, R_{SENSE1}, MN, MP, R_{SENSE2}, C_{OUT1}, and return through ground as short as possible to minimize parasitic inductive spikes at the switch node during switching.

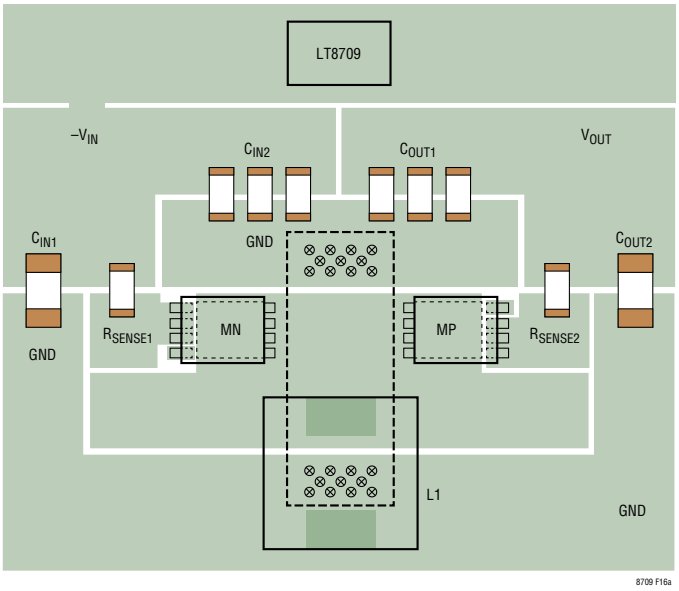

Figure 16a. Inverting Converter PCB Layout

Negative Buck Topology Specific Layout Guidelines

- Keep length of loop (high speed switching path) governing R_{SENSE1}, MN, MP, C_{IN} and return through $–V_{IN}$ as short as possible to minimize parasitic inductive spikes at the switch node during switching.

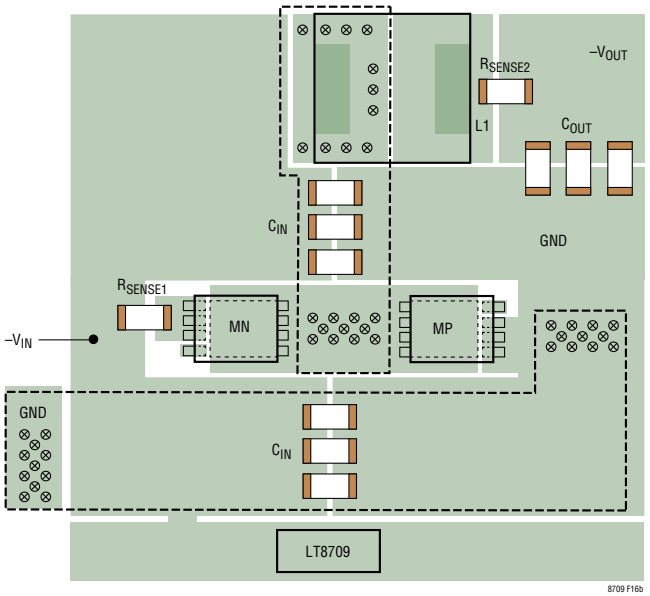

Figure 16b. Negative Buck Converter PCB Layout

Negative Buck-Boost Topology Specific Layout Guidelines

- Keep length of loop (high speed switching path) governing C_{IN}, R_{SENSE1}, MN, C1, MP, R_{SENSE2}, and return through ground as short as possible to minimize parasitic inductive spikes at the switch node during switching.

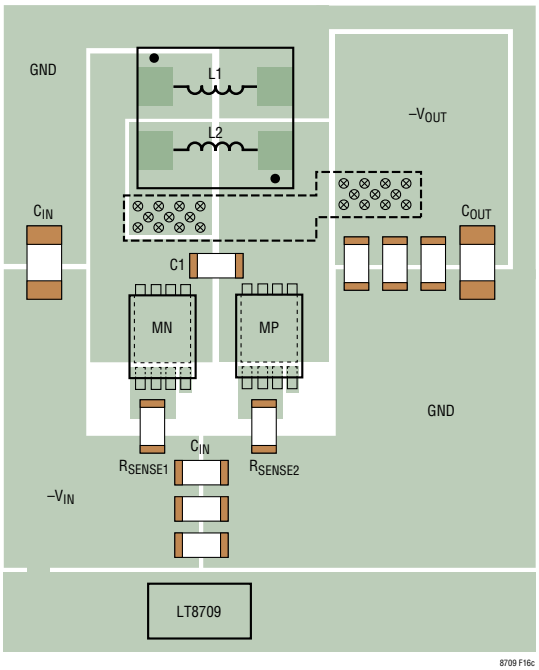

Figure 16c. Negative Buck-Boost PCB Layout

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Negative Boost Topology Specific Layout Guidelines

- Keep length of loop (high speed switching path) governing R_{SENSE1}, MN, C1, MP, R_{SENSE2}, and return through $-V_{IN}$ as short as possible to minimize parasitic inductive spikes at the switch node during switching.

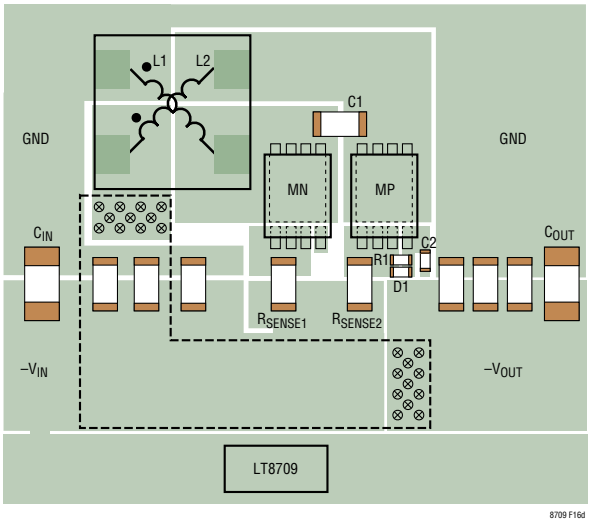

Figure 16d. Negative Boost PCB Layout

Current Sense Resistor Layout Guidelines

- Route the CSP/CSN and ISP/ISN lines differentially (close together) from the chip to the current sense resistors as shown in Figure 17.
- Place the vias that connect to CSP/CSN and ISP/ISN lines directly at the inner current sense pads of the current sense resistors as shown in Figure 17.

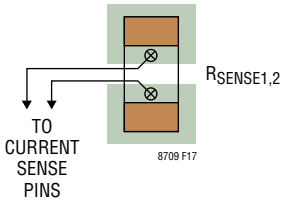

Figure 17. Suggested Routing and Connections of CSP/CSN and ISP/ISN Lines

THERMAL CONSIDERATIONS

Overview

The components on the board that dissipate the most heat are the power switches, (i.e., MN and MP), the power inductor, and the LT8709 IC. It is imperative that a good thermal path be provided for these components to dissipate the heat generated within the packages. This can be accomplished by taking advantage of the thermal pads on the underside of the packages. It is recommended that multiple vias in the printed circuit board be used to conduct heat away from each of these components and into a copper plane with as much area as possible. For the case of the power switches, the copper area of the drain connections shouldn't be too big as to create a large EMI surface that can radiate noise around the board.

Power MOSFET Loss and Thermal Calculations

The LT8709 requires two external power MOSFETs, an NFET switch for the BG gate driver and a PFET switch for the TG gate driver. Important parameters for estimating the power dissipation in the MOSFETs are:

1. On-resistance (R_{DSON})
2. Gate-to-drain charge (Q_{GD})
3. PFET body diode forward voltage (V_{BD})
4. V_{DS} of the FETs during their Off-Time
5. Switch current (I_{SW})
6. Switching frequency (f)

The power loss in each power switch has a DC and AC term. The DC term is when the power switch is fully on, and the AC term is when the power switch is transitioning from on-off or off-on.

The following applies for both the NFET and PFET power switches. For a negative buck converter, the average current through the MOSFET (I_{SW}) during its on-time is the same as the average output current; and the magnitude of the drain-to-source voltage, V_{DS}, during its off-time is $|V_{IN}|$. For a negative buck-boost or inverting or boost application, the average current through each MOSFET (I_{SW}) during its on-time, is the sum of the average input current and the output current. The $|V_{DS}|$ voltage during the off-time is approximately $|V_{IN}| + |V_{OUT}|$. During the

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non-overlap time of the gate drivers, the peak and valley inductor current is flowing through the body diode of the PFET. Given below are the equations for the power loss in MN and MP.

$$P_{MOSFET} = P_{I^2R} + P_{SWITCHING}$$

$$P_{MN} = I_N^2 \bullet R_{DSON} + V_{DS} \bullet I_N \bullet f \bullet t_{RF} + P_{RR-N}$$

$$P_{MP} = I_P^2 \bullet R_{DSON} + V_{BD} \bullet \left(I_{PK} + \frac{I_{VY}}{1.6}\right) \bullet f \bullet 140ns + P_{RR-P}$$

$$I_{SW} = \frac{I_{OUT}}{(1-DC)};\quad I_{PK} = I_{SW} + \frac{i_{RIPPLE}}{2};\quad I_{VY} = I_{SW} - \frac{i_{RIPPLE}}{2}$$

$$I_N = \sqrt{DC \bullet \left(I_{SW}^2 + \frac{i_{RIPPLE}^2}{12}\right)}$$

$$I_P = \sqrt{(1-DC) \bullet \left(I_{SW}^2 + \frac{i_{RIPPLE}^2}{12}\right)}$$

$$P_{RR-N} \approx \frac{V_{DS} \bullet I_{RR} \bullet t_{RR} \bullet f}{2}$$

$$P_{RR-P} \approx \frac{V_{DS} \bullet I_{RR} \bullet t_{RR} \bullet f}{2}$$

where:

- f = Switching Frequency
- I_N = NFET RMS Current
- I_P = PFET RMS Current
- t_{RF} = Average of the rise and fall times of the NFET's drain voltage
- I_{SW} = Average switch current during its on-time
- I_{PK} = Peak inductor current
- I_{VY} = Valley inductor current
- i_{RIPPLE} = Inductor ripple current
- DC = Switch duty cycle (see Power Switch Duty Cycle section in Appendix)
- V_{BD} = PFET body diode forward voltage at I_{SW}
- P_{RR-N} = NFET I^2R loss term from the PFET body diode reverse recovery
- P_{RR-P} = PFET body diode reverse recovery power loss
- I_{RR} = Current needed to remove the PFET body diode charge
- t_{RR} = Reverse recovery time of PFET body diode

Typical values for t_{RF} are 10ns to 40ns depending on the MOSFET capacitance and drain voltage. In general, the lower the Q_{GD} of the MOSFET, the faster the rise and fall times of its drain voltage. For best calculations, measure the rise and fall times in the application.

PFET body diode reverse recovery power loss is dependent on many factors and can be difficult to quantify in an application. In general, this power loss increases with higher V_{DS} and/or higher switching frequency.

Chip Power and Thermal Calculations

Power dissipation in the LT8709 chip comes from three primary sources: the $INTV_{CC}$ LDO, $INTV_{EE}$ LDO, and input quiescent current. The average current through each LDO is determined by the gate charge of the power switches, MN and MP, and the switching frequency. Given below are the equations for calculating the chip power loss followed by examples.

Negative Buck, Buck-Boost and Inverting Converters: The $INTV_{CC}$ LDO primarily supplies voltage for the BG gate driver. The BIAS and $INTV_{EE}$ voltages supply the top and bottom rails of the TG gate driver respectively. The chip Q current comes from the higher of GND and BIAS, referred to $-V_{IN}$. Given below are the chip power equations for a negative buck, buck-boost or inverting converter:

$$P_{VCC} = 1.04 \bullet Q_{MN} \bullet f \bullet V_{SELECT}$$
$$P_{VEE1} = Q_{MP} \bullet f \bullet V_{BIAS}$$
$$P_{VEE2} = 3.1mA \bullet (1 - DC) \bullet V_{BIAS}$$
$$P_Q = 4mA \bullet V_{MAX}$$

where:

- f = Switching frequency
- DC = Switch duty cycle (see Power Switch Duty Cycle section in Appendix)
- Q_{MN} = Total gate charge of NFET power switch (MN) at $6.3V_{GS}$
- Q_{MP} = Total gate charge of PFET power switch (MP) at $6.18V_{SG}$
- V_{SELECT} = $INTV_{CC}$ LDO selected input voltage, GND or BIAS (see LDO REGULATORS section)
- V_{MAX} = Higher of GND and BIAS.

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Negative Boost Converter: Since BIAS connects to $INTV_{CC}$ and $INTV_{EE}$ connects to $-V_{IN}$ (see Typical Applications), all the chip power comes from the GND pin. The $INTV_{CC}$ LDO primarily supplies voltage for both the BG and TG gate drivers. The chip Q current comes from GND. For consistency, the power that's needed to run the TG gate driver is still labeled as P_{VEE} even though the power is coming from $INTV_{CC}$. Given below are the chip power equations for a negative boost converter:

$$P_{VCC} = 1.04 \bullet Q_{MN} \bullet f \bullet V_{IN}$$
$$P_{VEE1} = Q_{MP} \bullet f \bullet V_{IN}$$
$$P_{VEE2} = 3.15mA \bullet (1 - DC) \bullet V_{IN}$$
$$P_Q = 5.5mA \bullet V_{IN}$$

where:

f = Switching frequency

V_{IN} = The voltage difference between GND and $-V_{IN}$ pins

DC = Switch duty cycle (see Power Switch Duty Cycle section in Appendix)

Q_{MN} = Total gate charge of NFET power switch (MN) at $6.3V_{GS}$

Q_{MP} = Total gate charge of PFET power switch (MP) at $6.3V_{SG}$

Chip Power Calculations Example

Table 5 calculates the power dissipation of the LT8709 for a 250kHz, –16V to –30V input to –12V/8.5A buck application when V_{IN} is –24V. From P_{CHIP} in Table 5, the die junction temperature can be calculated using the appropriate thermal resistance and worst-case ambient temperature:

$$T_J = T_A + \theta_{JA} \bullet P_{CHIP}$$

where T_J = die junction temperature, T_A = ambient temperature and θ_{JA} is the thermal resistance from the silicon junction to the ambient air.

The published θ_{JA} value is 38°C/W for the TSSOP exposed pad package. In practice, lower θ_{JA} values are realizable if board layout is performed with appropriate grounding (accounting for heat sinking properties of the board) and other considerations listed in the Layout Guidelines section. For instance, a θ_{JA} value of ~22°C/W was consistently achieved when board layout was optimized as per the suggestions in the Layout Guidelines section.

Thermal Lockout

If the die temperature reaches ~175°C, the part will go into reset, so the power switches turn off, the soft-start capacitor will be discharged and the current limit of the $INTV_{CC}$ and $INTV_{EE}$ regulators drop to 0. The LT8709 will come out of reset when the die temperature drops by ~5°C (typical).

Table 5. Power Calculations Example for a 250kHz, $-16V_{IN}$ to $-30V_{IN}$ to $-12V_{OUT}$/8.5A Buck ($-V_{IN}$ = –24V, MN = BSC026N04LS and MP = FDD4141)

DEFINITION OF VARIABLES	EQUATION	DESIGN EXAMPLE	VALUE
DC = Switch Duty Cycle	$DC \cong \frac{V_{OUT}}{V_{IN}}$	$DC \cong \frac{-12V}{-24V}$	DC ≅ 50%
P_{VCC} = $INTV_{CC}$ LDO Power Driving the BG Gate Driver Q_{MN} = NFET Total Gate Charge at V_{GS} = 6.3V f = Switching Frequency V_{SELECT} = LDO Chooses GND	$P_{VCC} = 1.04 \bullet Q_{MN} \bullet f \bullet V_{SELECT}$	$P_{VCC} = 1.04 \bullet 20nC \bullet 250kHz \bullet 24V$	P_{VCC} = 125mW
P_{VEE1} = $INTV_{EE}$ LDO Power Driving the TG Gate Driver Q_{MP} = PFET Total Gate Charge at V_{SG} = 6.18V	$P_{VEE1} = Q_{MP} \bullet f \bullet V_{BIAS}$	$P_{VEE1} = 24nC \bullet 250kHz \bullet 24V$	P_{VEE1} = 144mW
P_{VEE2} = Additional TG Gate Driver Power Loss	$P_{VEE2} = 3.1mA \bullet (1 - DC) \bullet V_{BIAS}$	$P_{VEE2} = 3.1mA \bullet (1 - 0.5) \bullet 24V$	P_{VEE2} = 37.2mW
P_Q = Chip Bias Loss V_{MAX} = Higher Voltage of ($V_{GND} - V_{-VIN}$) and ($V_{BIAS} - V_{-VIN}$)	$P_Q = 4mA \bullet V_{MAX}$	$P_Q = 4mA \bullet 24V$	P_Q = 96mW
			P_{CHIP} = 0.4021W

APPENDIX

POWER SWITCH DUTY CYCLE

In order to maintain loop stability and deliver adequate current to the load, the external power NFET (MN in the Block Diagram) cannot remain on for 100% of each clock cycle. The maximum allowable duty cycle is given by:

$$DC_{MAX} = \frac{(T_P - MinOffTime)}{T_P} \bullet 100\%$$

where T_P is the clock period and MinOffTime (found in the Electrical Characteristics) is a maximum of 480ns.

Conversely, the external power NFET (MN in the Block Diagram) cannot remain off for 100% of each clock cycle, and will turn on for a minimum on time (MinOnTime) when in regulation. This MinOnTime governs the minimum allowable duty cycle given by:

$$DC_{MIN} = \frac{(MinOnTime)}{T_P} \bullet 100\%$$

where T_P is the clock period and MinOnTime (found in the Electrical Characteristics) is a maximum of 420ns.

The application should be designed such that the operating duty cycle is between DC_{MIN} and DC_{MAX}.

Duty cycle equations for several common topologies are given below where V_{MP_ON} is the voltage drop across the external power PFET (MP) when it is on, and V_{MN_ON} is the voltage drop across the external power NFET (MN) when it is on.

For the negative buck topology (see Figure 5):

$$DC_{-BUCK} \cong \frac{|V_{OUT}| + V_{MP\_ON}}{|V_{IN}| + V_{MP\_ON} - V_{MN\_ON}}$$

For the negative inverting topology (see Figure 6):

$$DC_{-INVERTER} \cong \frac{V_{OUT} + V_{MP\_ON}}{|V_{IN}| + V_{OUT} + V_{MP\_ON} - V_{MN\_ON}}$$

For the negative buck-boost topology (see Figure 7):

$$DC_{-BUCK-BOOST} \cong \frac{|V_{OUT}| + V_{MP\_ON}}{|V_{IN}| + |V_{OUT}| + V_{MP\_ON} - V_{MN\_ON}}$$

For the negative boost topology (see Figure 8):

$$DC_{-BOOST} \cong \frac{|V_{OUT}| - |V_{IN}| + V_{MP\_ON}}{|V_{OUT}| + V_{MP\_ON} - V_{MN\_ON}}$$

The LT8709 can be used in configurations where the duty cycle is higher than DC_{MAX}, but it must be operated in the discontinuous conduction mode (MODE pin must be high) so that the effective duty cycle is reduced.

INDUCTOR SELECTION

For high efficiency, choose inductors with high frequency core material, such as ferrite, to reduce core losses. Also to improve efficiency, choose inductors with more volume for a given inductance. The inductor should have low DCR (copper-wire resistance) to reduce I^2R losses, and must be able to handle the peak inductor current without saturating. Note that in some applications, the current handling requirements of the inductor can be lower, such as in the negative buck-boost topology where each inductor carries a fraction of the total switch current. Molded chokes or chip inductors do not have enough core area to support peak inductor currents in the 5A to 15A range. To minimize radiated noise, use a toroidal or shielded inductor. See Table 6 for a list of inductor manufacturers.

Table 6. Inductor Manufacturers

Coilcraft	MSS1278, XAL1010, and MSD1278 Series	www.coilcraft.com
Cooper Bussmann	DR127, DRQ127, and HCM1104 Series	www.cooperbussmann.com
Vishay	IHLP Series	www.vishay.com
Würth	WE-HCI and WE-CFWI Series	www.we-online.com

Minimum or Maximum Inductance

Although there can be a tradeoff with efficiency, it is often desirable to minimize board space by choosing smaller inductors. When choosing an inductor, there are three conditions that limit the minimum or maximum inductance; (1) providing adequate load current, and (2) avoiding subharmonic oscillation, and (3) supplying a minimum ripple current to avoid false tripping of the current comparator.

APPENDIX

Adequate Load Current

Small value inductors result in increased ripple currents and thus, due to the limited peak switch current, decrease the average current that can be provided to the load. In order to provide adequate load current, L should be at least:

$$L_{-BUCK} \geq \frac{(|V_{IN}| - |V_{OUT}|) \bullet DC}{2 \bullet f \bullet \left(\frac{V_{CSPN}}{R_{SENSE1}} - I_{OUT} \right)}$$

$$L_{-INVERTER} \geq \frac{|V_{IN}| \bullet DC}{2 \bullet f \bullet \left(\frac{V_{CSPN}}{R_{SENSE1}} - \frac{|V_{OUT}| \bullet I_{OUT}}{|V_{IN}| \bullet \eta} - I_{OUT} \right)}$$

$$L_{-BUCK\_BOOST} \geq \frac{|V_{IN}| \bullet DC}{2 \bullet f \bullet \left(\frac{V_{CSPN}}{R_{SENSE1}} - \frac{|V_{OUT}| \bullet I_{OUT}}{|V_{IN}| \bullet \eta} - I_{OUT} \right)}$$

$$L_{-BOOST} \geq \frac{|V_{IN}| \bullet DC}{2 \bullet f \bullet \left(\frac{V_{CSPN}}{R_{SENSE1}} - \frac{|V_{OUT}| \bullet I_{OUT}}{|V_{IN}| \bullet \eta} - I_{OUT} \right)}$$

where…

L_{-BUCK} or $L_{-INVERTER}$ = L_1 for the negative buck or inverting topologies (see Figures 5 and 6)

$L_{-BUCK-BOOST}$ or L_{-BOOST} = L_1 = L_2 for coupled dual inductor topologies (see Figures 7 and 8)

$L_{-BUCK-BOOST}$ or L_{-BOOST} = L_1 || L_2 for uncoupled dual inductor topologies (see Figures 7 and 8)

DC = Switch duty cycle (see previous section)

V_{CSPN} = Current limit voltage at the operating switch duty cycle (see *Max Current Limit vs Duty Cycle (CSP – CSN)* plot in the Typical Performance Characteristics)

R_{SENSE1} = Current sense resistor connected across the CSP-CSN pins (see Block Diagram)

η = Power conversion efficiency (assume ~90%)

f = Switching frequency

I_{OUT} = Maximum output current

Negative values of inductance from above equations' indicate that the output load current, I_{OUT}, exceeds the switch current limit capability of the converter. Decrease R_{SENSE1} to increase the switch current limit.

Avoiding Sub-Harmonic Oscillations

The LT8709's internal slope compensation circuit will prevent sub-harmonic oscillations that can occur when the duty cycle is greater than 50%, provided that the inductance exceeds a minimum value. In applications that operate with duty cycles greater than 50%, the inductance must be at least:

$$L_{MIN} \geq \frac{|V_{IN}| \bullet R_{SENSE1} \bullet (2 \bullet DC - 1)}{40m \bullet DC \bullet f \bullet (1 - DC)}$$

FOR NEGATIVE BOOST, BUCK-BOOST AND INVERTING CONVERTERS

$$L_{MIN} \geq \frac{R_{SENSE1} \bullet |V_{IN}| \bullet (2 \bullet DC - 1)}{f \bullet 40mV \bullet DC}$$

FOR NEGATIVE BUCK CONVERTERS

where…

L_{MIN} = L_1 for single inductor topologies (see Figures 5 and 6). Note: for the negative buck, $|V_{IN}| - |V_{OUT}|$ replaces $|V_{IN}|$.

L_{MIN} = L_1 = L_2 for coupled dual inductor topologies (see Figures 7 and 8)

L_{MIN} = L_1 || L_2 for uncoupled dual inductor topologies (see Figures 7 and 8)

Maximum Inductance

Excessive inductance can reduce ripple current to levels that are difficult for the current comparator (A6 in the Block Diagram) to cleanly discriminate, thus causing duty cycle jitter and/or poor regulation. The maximum inductance can be calculated by:

$$L_{MAX} \leq \frac{|V_{IN}| \bullet R_{SENSE1} \bullet DC}{3mV \bullet f}$$

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where…

L_{MAX} = L_1 for single inductor topologies (see Figures 5 and 6). Note: for the negative buck, $|V_{IN}| - |V_{OUT}|$ replaces $|V_{IN}|$.

L_{MAX} = L_1 = L_2 for coupled dual inductor topologies (see Figures 7 and 8)

L_{MAX} = L_1 || L_2 for uncoupled dual inductor topologies (see Figures 7 and 8)

Inductor Current Rating

The inductor(s) must have a rating greater than its (their) peak operating current to prevent inductor saturation, which would result in efficiency losses. The maximum inductor current (considering start-up and steady-state conditions) is given by:

$$I_{L\_PEAK} = \frac{54mV - 16mV \bullet DC^2}{R_{SENSE1}} + \frac{V_{IN} \bullet T_{MIN\_PROP}}{L}$$

where

I_{L_PEAK} = Peak inductor current in L_1 for a single inductor topologies or the sum of the peak inductor currents for dual inductor topologies.

T_{MIN_PROP} = 100ns (propagation delay through the current feedback loop).

Note that these equations offer conservative results for the required inductor current ratings. The current ratings could be lower for applications with light loads, and if the SS capacitor is sized appropriately to limit inductor currents at start-up.

For wide input voltage range applications, as the input voltage increases, the max peak inductor current also increases due to the duty cycle decreasing. It is recommended to utilize the output current limiting feature to reduce the max peak inductor current given by the following equation:

$$I_{L\_PEAK} = \frac{V_{ISPN}}{R_{SENSE2} \bullet (1 - DC)} + \frac{V_L \bullet DC}{2 \bullet f \bullet L}$$

where...

V_{ISPN} = 57mV max for negative buck, inverting and buck-boost converters and 60mV max for the negative boost converter. Note that V_L represents the voltage across the inductor and is equal to $|V_{IN}| - |V_{OUT}|$ for a negative buck converter and $|V_{IN}|$ for a negative boost, buck-boost, or inverting converter.

RC Damping Network for Dual Inductor Topologies with Single Inductors

Two discrete inductors shown in Figure 18 can be used when the LT8709 is configured for the negative buck-boost or negative boost topologies with a few requirements.

1. Size the flying capacitor C1 ≥ 4.7µF
2. Calculate the value of the damping resistor and ensure that $R_{DAMP} \leq 3\Omega$ to limit power dissipation
3. Calcuate C_{DAMP}

It should be noted that the value of C1 may need to be adjusted if R_{DAMP} cannot be made below or close to 3Ω.

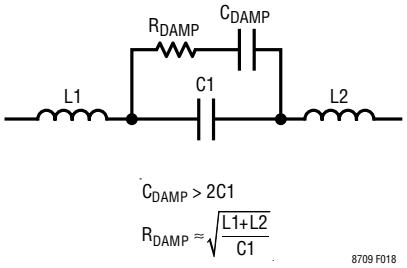

Figure 18. RC Damp Network for Single Inductors

POWER MOSFET SELECTION

The LT8709 requires two external power MOSFETs, an NFET switch for the BG gate driver and a PFET switch for the TG gate driver. It is important to select MOSFETs for optimizing efficiency. For choosing an NFET and PFET, the important device parameters are:

1. Breakdown voltage (BV_{DSS})
2. Gate threshold voltage (V_{GSTH})
3. On-resistance (r_{DSON})
4. Total gate charge (Q_G)
5. Turn-off delay time ($t_{D(OFF)}$)
6. Package has exposed paddle as heat sink

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The drain-to-source breakdown voltage of the NFET and PFET power MOSFETs must exceed:

- $BV_{DSS} > |V_{IN}|$ for negative buck converters
- $BV_{DSS} > |V_{IN}| + |V_{OUT}|$ for negative boost, buck-boost, or inverting converters

If operating close to the BV_{DSS} rating of the MOSFET, check the leakage specifications on the MOSFET because leakage can decrease the efficiency of the converter.

The NFET and PFET gate-to-source drive is approximately 6.3V and 6.18V respectively, so logic level MOSFETs are required. The BG gate driver can begin switching when the $INTV_{CC}$ voltage exceeds ~4V, so ensure the selected NFET is in the triode region of operation with 4V of gate-to-source drive to prevent possible damage to the NFET.

The TG gate driver can begin switching when the BIAS-$INTV_{EE}$ voltage exceeds ~3.42V, so it is optimal that the PFET be in the triode region of operation with 3.42V of gate-to-source drive. However, the PFET is less likely to be damaged if it's not operating in the triode region since the drain-to-source voltage is clamped by its body diode during the NFET's off-time. Having said that, try to choose a PFET with a low body diode reverse recovery time to minimize stored charge in the PFET. The stored charge in the PFET body diode is removed when the NFET switch turns on and can lead to a reduction in efficiency especially in applications where the V_{DS} of the PFET (during off-time) is high. For these applications, it may be beneficial to put a Schottky diode across the PFET to reduce the amount of charge in the PFET body diode. In applications where the output voltage is high in magnitude, it is recommended to replace the PFET with a Schottky diode since the converter may be more efficient.

Power MOSFET on-resistance and total gate charge go hand-in-hand and are typically inversely proportional to each other; the lower the on-resistance, the higher total gate charge. Choose MOSFETs with an on-resistance to give a voltage drop to be less than 300mV at the peak current. At the same time, choose MOSFETs with a lower total gate charge to reduce LT8709 power dissipation and MOSFET switching losses.

The turn-off delay time ($t_{D(OFF)}$) of available NFETs is generally smaller than the LT8709's non-overlap time. However, the turn-off time of the available PFETs should be checked before deciding on a PFET for a given application. The turn-off time must be less than the non-overlap time of the LT8709 or else the NFET and PFET could be on at the same time and damage to external components may occur. If the PFET turn-off delay time as specified in the data sheet is less than the LT8709 non-overlap time, then the PFET is good to use. If the turn-off delay time is longer than the non-overlap time, it doesn't necessarily mean it can't be used. It may be unclear how the PFET manufacturer measures the turn-off delay time, so it is best to measure the PFET turn-off delay time with respect to the PFET gate voltage.

Finally, both the NFET and PFET power MOSFETs should be in a package with an exposed paddle for the drain connection to be able to dissipate heat. The on-resistance of MOSFETs is proportional to temperature, so it's more efficient if the MOSFETs are running cool with the help of the exposed paddle. See Table 7 for a list of power MOSFET manufacturers.

Table 7. Power MOSFET (NFET and PFET) Manufacturers

Fairchild Semiconductor	www.fairchildsemi.com
On-Semiconductor	www.onsemi.com
Vishay	www.vishay.com
Diodes Inc.	www.diodes.com

Table 8. Recommended PFETs

20V	Si7635DP, Si7633DP	www.vishay.com
30V	Si7101DN, Si7143DP	www.vishay.com
40V	FDD4141, Si7463ADP, SiS443DN, Si7611DN,	www.fairchildsemi.com, www.vishay.com
60V	Si7465DP, SUD19P06-60, SUD50P06-15	www.vishay.com
100V	FDMC86139P, Si7113DN	www.fairchildsemi.com, www.vishay.com

INPUT AND OUTPUT CAPACITOR SELECTION

Input and output capacitance is necessary to suppress voltage ripple caused by discontinuous current moving in and out of the regulator. A parallel combination of capacitors is typically used to achieve high capacitance and low ESR (equivalent series resistance). Tantalum, special polymer, aluminum electrolytic and ceramic capacitors are all available in surface mount packages. Capacitors with

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low ESR and high ripple current ratings, such as OS-CON, SUN-CON and POSCAP are also available.

Ceramic capacitors should be placed near the regulator input and output to suppress high frequency switching noise. A minimum 2.2µF ceramic capacitor should also be placed from GND to $-V_{IN}$ and from BIAS to $-V_{IN}$ as close to the LT8709 pins as possible. Due to their excellent low ESR characteristics, ceramic capacitors can significantly reduce ripple voltage and help reduce power loss in the higher ESR bulk capacitors. X5R or X7R dielectrics are preferred, as these materials retain their capacitance over wide voltage and temperature ranges. Many ceramic capacitors, particularly 0805 or 0603 case sizes, have greatly reduced capacitance at the desired operating voltage.

Input Capacitor, C_{IN}

Given below are the equations for calculating the capacitance of C_{IN} for 0.5% input voltage ripple:

$$C_{IN} \geq \frac{I_{OUT} \bullet DC \bullet (1-DC)}{f \bullet 0.005 \bullet |V_{IN}|}$$ Negative Buck Converter

$$C_{IN} \geq \frac{DC}{8 \bullet L \bullet f^2 \bullet 0.005}$$ Negative Boost Converter

$$C_{IN} \geq \frac{I_{OUT} \bullet DC}{f \bullet 0.005 \bullet V_{OUT}}$$ Negative Inverting Converter

$$C_{IN} \geq \frac{I_{OUT} \bullet DC}{f \bullet 0.005 \bullet V_{IN}}$$ Negative Buck-Boost Converter

where:

DC = Switch duty cycle (see Power Switch Duty Cycle section)

L = Inductance for adequate load current (see Inductor Selection section)

f = Switching frequency

Keep in mind that the voltage rating of the input capacitor needs to be greater than the maximum input voltage. The equations calculate the capacitance value during steady-state operation and may need to be adjusted for desired transient response. Also, this assumes no ESR, so the input capacitance may need to be larger depending on the equivalent ESR of the input capacitor(s).

Output Capacitor, C_{OUT}

The output capacitor, C_{OUT}, in a negative inverting topology has chopped current flowing through it, whereas the output capacitor in a negative buck, boost or buck-boost topology sees the inductor ripple current continuously ramping up and down. Given below is the equation for calculating the capacitance of C_{OUT} for 0.5% output voltage ripple:

$$C_{OUT} > \frac{I_{OUT} \bullet DC}{f \bullet 0.005 \bullet V_{OUT}}$$ Negative Inverting Converters

or

$$C_{OUT} > \frac{1-DC}{8 \bullet L \bullet f^2 \bullet 0.005}$$ Negative Buck, Boost, Buck-Boost Converters

where:

I_{OUT} = Maximum output current of converter

DC = Switch duty cycle (see Power Switch Duty Cycle section)

L = Inductance for adequate load current (see Inductor Selection section)

f = Switching frequency

The equations calculate the capacitance value during steady-state operation and may need to be adjusted for desired transient response. Also, this assumes no ESR, so the output capacitance may need to be larger depending on the equivalent ESR of the output capacitor(s). See Table 9 for a list of ceramic capacitor manufacturers.

Table 9. Ceramic Capacitor Manufacturers

TDK	www.tdk.com
Murata	www.murata.com
Taiyo Yuden	www.t-yuden.com

COMPENSATION – ADJUSTMENT

To compensate the feedback loop of the LT8709, a series resistor capacitor network in parallel with an optional single capacitor should be connected from the V_C pin to

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$-V_{IN}$. For most applications, choose a series capacitor in the range of 1nF to 10nF with 4.7nF being a good starting value. The optional parallel capacitor should range in value from 47pF to 220pF with 100pF being a good starting value. The compensation resistor, R_C, is usually in the range of 5k to 50k. A good technique to compensate a new application is to use a 100k potentiometer in place of the series resistor R_C. With the series and parallel capacitors at 2.2nF and 100pF respectively, adjust the potentiometer while observing the transient response and the optimum value for R_C can be found. Figures 19a to 19c illustrate this process for the circuit of Figure 22 with a load current stepped between 3A and 8A. Figure 19a shows the transient response with R_C equal to 208Ω. The phase margin is poor as evidenced by the excessive ringing in the output voltage and inductor current. In Figure 19b, the value of R_C is increased to 1.5k, which results in a more damped response. Figure 19c shows the results when R_C is increased further to 5.9k. The transient response is nicely damped and the compensation procedure is complete.

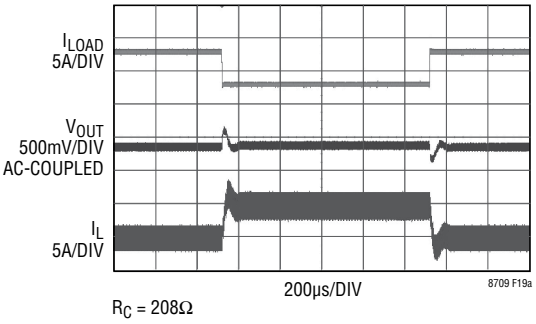

Figure 19a. Transient Response Shows Excessive Ringing

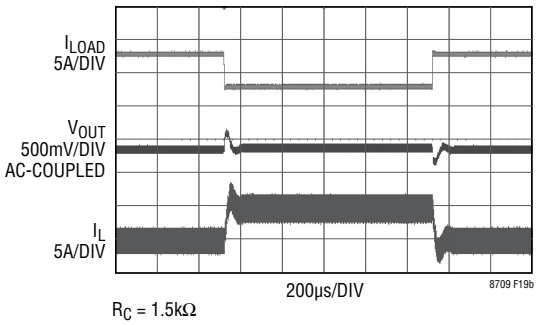

Figure 19b. Transient Response is Better

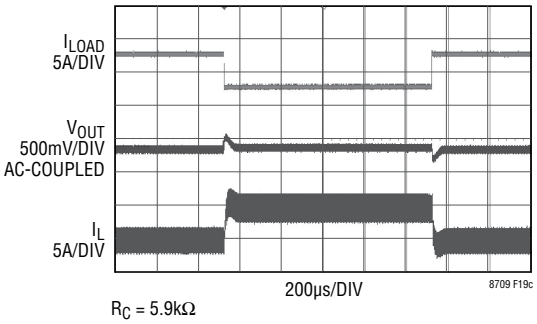

Figure 19c. Transient Response is Well Damped

COMPENSATION – THEORY

Like all other current mode switching regulators, the LT8709 needs to be compensated for stable and efficient operation. Two feedback loops are used in the LT8709: a fast current loop which does not require compensation, and a slower voltage loop which does. Standard bode plot analysis can be used to understand and adjust the voltage feedback loop.

As with any feedback loop, identifying the gain and phase contribution of the various elements in the loop is critical. Figure 20 shows the key equivalent elements of a negative buck converter where $-V_{IN}$ is treated as the signal ground. Because of the fast current control loop, the power stage of the IC, inductor and diode have been replaced by a combination of the equivalent transconductance amplifier g_{mp} and a current controlled current source G_{mp} acts as a current source where the peak input current, I_{OUT}, is proportional to the V_C voltage and current sense resistor, R_{SENSE1}.

Note that the maximum output currents of g_{mp} and g_{ma} are finite. The external current sense resistor, R_{SENSE1}, sets the value of:

$$g_{mp} \approx \frac{1}{6 \bullet R_{SENSE1}}$$

The error amplifier, g_{ma}, is nominally about 200µmhos with a source and sink current of about 12µA and 19µA respectively.

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From Figure 20, the DC gain, poles and zeros can be calculated as follows:

DC GAIN:

$$A_{DC} = g_{ma} \bullet R_O \bullet g_{mp} \bullet R_L \bullet \frac{\left(R_{FBY2} \| \frac{1}{g_{m,Q1}}\right)}{R_{FBY1} + \left(R_{FBY2} \| \frac{1}{g_{m,Q1}}\right)} \bullet g_{m,Q1} \bullet R2/2$$

$$\text{Output Pole: } P1 = \frac{1}{2 \bullet \pi \bullet R_L \bullet C_{OUT}}$$

$$\text{Error Amp Pole: } P2 = \frac{1}{2 \bullet \pi \bullet (R_O + R_C) \bullet C_C}$$

$$\text{Error Amp Zero: } Z1 = \frac{1}{2 \bullet \pi \bullet R_C \bullet C_C}$$

$$\text{ESR Zero: } Z2 = \frac{1}{2 \bullet \pi \bullet R_{ESR} \bullet C_{OUT}}$$

$$\text{Phase Lead Zero: } Z3 = \frac{1}{2 \bullet \pi \bullet R_{FBY1} \bullet C_{PL}}$$

$$\text{Phase Lead Pole: } P4 = \frac{1}{2 \bullet \pi \bullet R_{FBY2} \| \frac{1}{g_{m(Q1)}} \bullet C_{PL}}$$

$$\text{Error Amp Filter Pole: } P5 = \frac{1}{2 \bullet \pi \bullet \frac{R_C \bullet R_O}{R_C + R_O} \bullet C_F}, C_F < \frac{C_C}{10}$$

$$\text{RHP Zero: } Z4 = \frac{V_{IN}^2 \bullet R_L}{2 \bullet \pi \bullet V_{OUT}^2 \bullet L}$$

The current mode zero (Z3) which exists for the inverting and dual inductor topologies only, is a right half plane zero which can be an issue in feedback control design, but is manageable with proper external component selection.

Using the circuit in Figure 22 as an example, Table 10 shows the parameters used to generate the bode plot shown in Figure 21.

Table 10: Bode Plot Parameters

PARAMETER	VALUE	UNITS	COMMENT
R_L	1.41	Ω	Application Specific
C_{OUT}	66	µF	Application Specific
R_{ESR}	2	mΩ	Application Specific
R_O	350	kΩ	Not Adjustable
C_C	2200	pF	Adjustable
C_F	100	pF	Optional/Adjustable
C_{PL}	0	pF	Optional/Adjustable
R_C	5.9	kΩ	Adjustable
R_{FBY1}	33	kΩ	Adjustable
R_{FBY2}	4.99	kΩ	Adjustable
R2	14.5	kΩ	Not Adjustable
V_{OUT}	–12	V	Application Specific
V_{IN}	–24	V	Application Specific
g_{ma}	200	µmho	Not Adjustable
g_{mp}	83.3	mho	Application Specific
$g_{m,Q1}$	1.8	mmho	Not Adjustable
$g_{m,M1}$	1.05	mmho	Not Adjustable
L	7.3	µH	Application Specific
f_{OSC}	250	kHz	Adjustable

From Figure 21, the phase is –120° when the gain reaches 0dB giving a phase margin of 60°. The crossover frequency is 50kHz.

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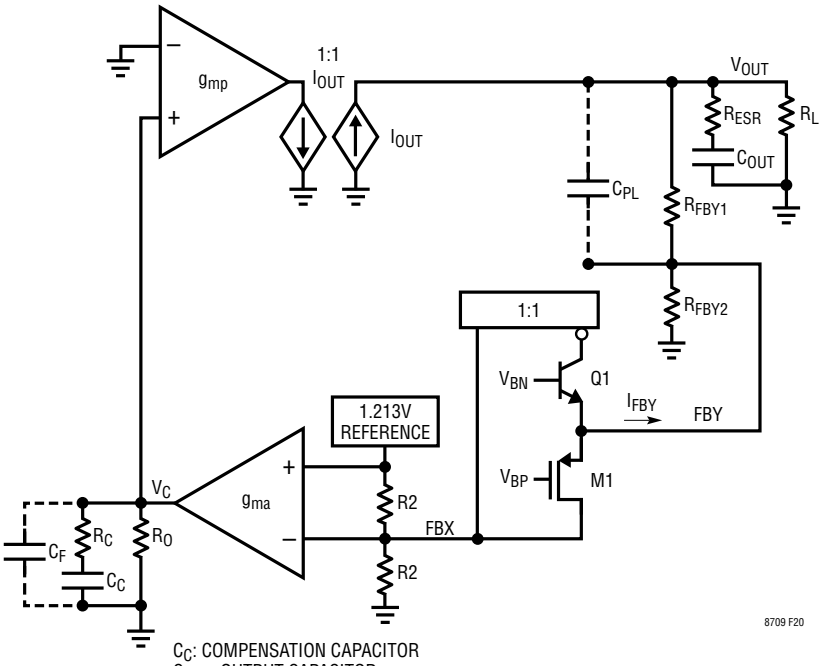

C_C: COMPENSATION CAPACITOR
C_{OUT}: OUTPUT CAPACITOR
C_{PL}: PHASE LEAD CAPACITOR
C_F: HIGH FREQUENCY FILTER CAPACITOR
g_{ma}: TRANSCONDUCTANCE AMPLIFIER INSIDE IC
g_{mp}: POWER STAGE TRANSCONDUCTANCE AMPLIFIER
$g_{m,Q1}$: TRANSCONDUCTANCE OF Q1 WHEN CONDUCTING FOR $-V_{OUT}$
$g_{m,M1}$: TRANSCONDUCTANCE OF M1 WHEN CONDUCTING FOR $+V_{OUT}$
R_C: COMPENSATION RESISTOR
R_L: OUTPUT RESISTANCE DEFINED AS $V_{OUT}/I_{LOAD(MAX)}$
R_O: OUTPUT RESISTANCE OF g_{ma}
R_{FBY1}, R_{FBY2}: FEEDBACK RESISTOR DIVIDER NETWORK
R_{ESR}: OUTPUT CAPACITOR ESR
η: CONVERTER EFFICIENCY (~90% AT HIGHER CURRENTS)

Figure 20. Negative Buck Converter Equivalent Model

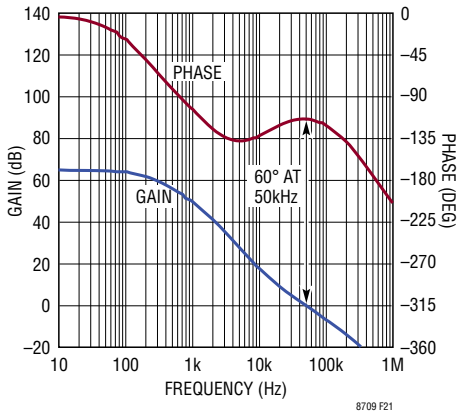

Figure 21. Bode Plot for Example Negative Buck Converter

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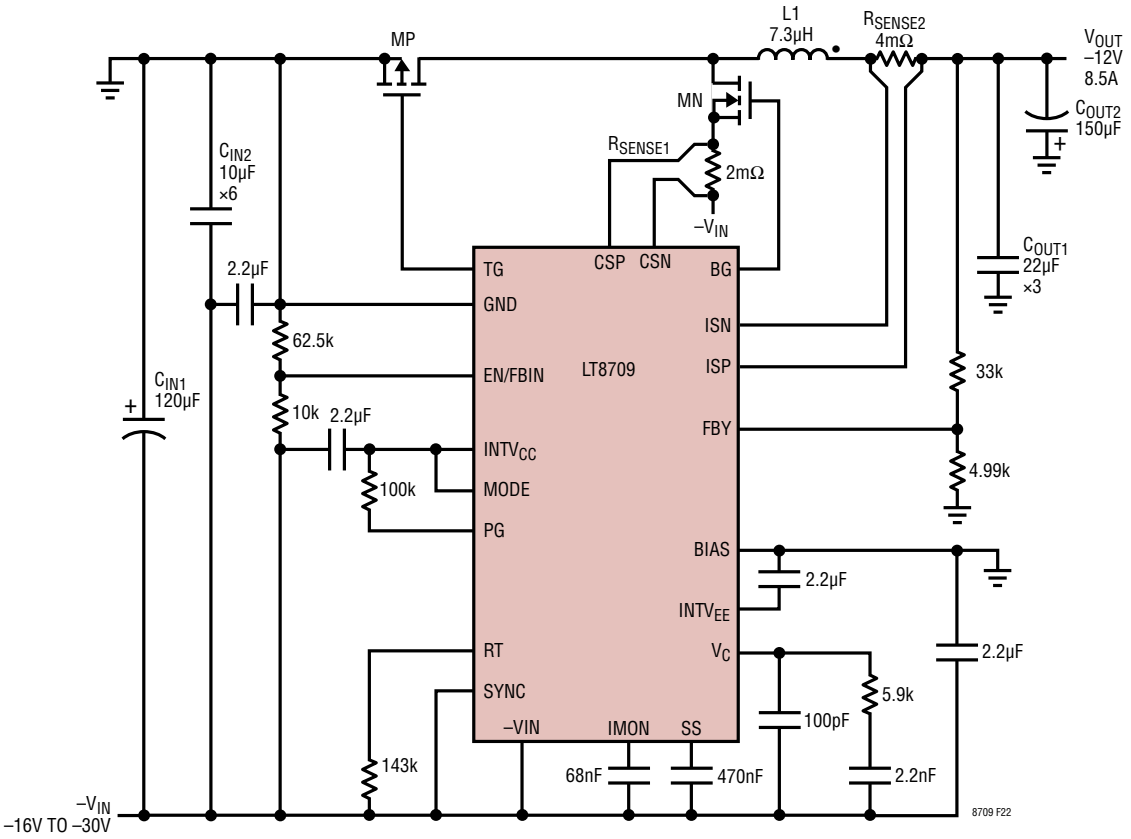
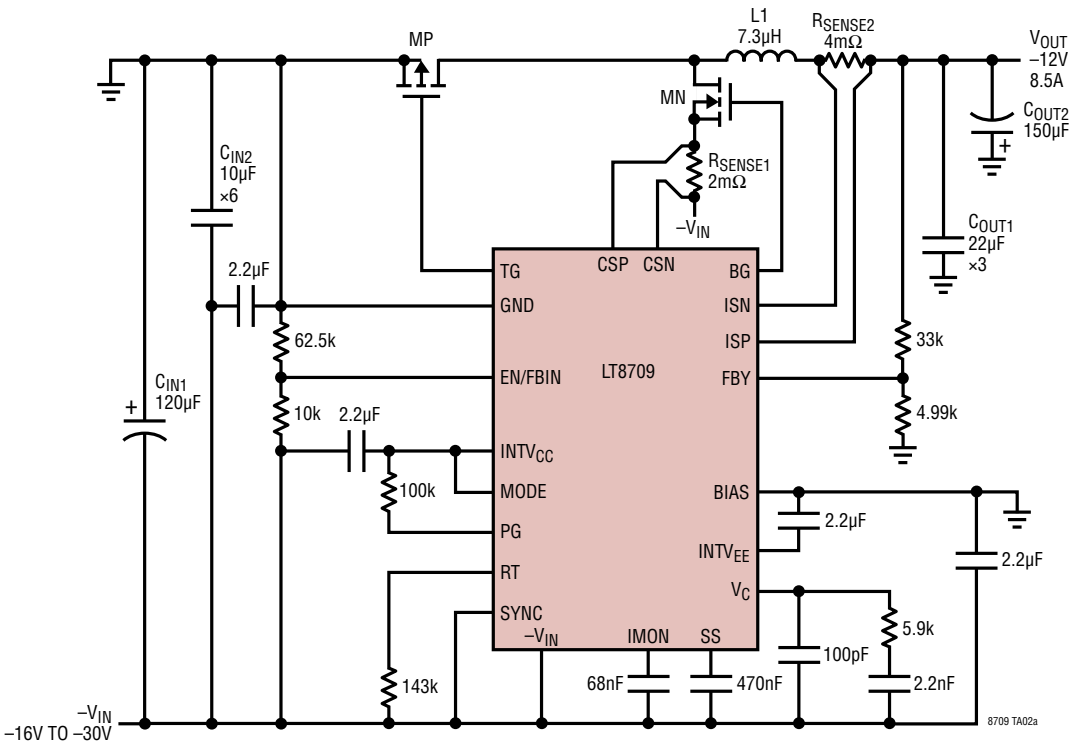


Figure 22. Negative Buck Converter

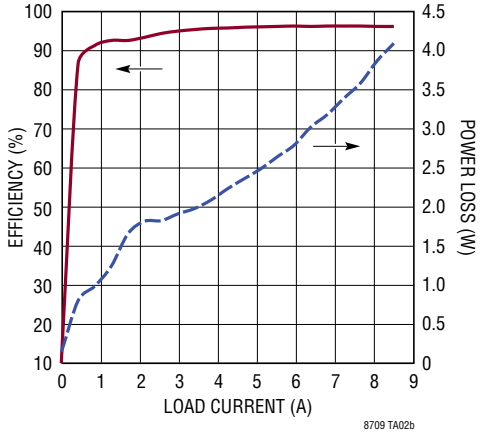
TYPICAL APPLICATION

250kHz, –16V to –30V Input to –12V Output, Negative Buck Converter Delivers Up to 8.5A Output Current

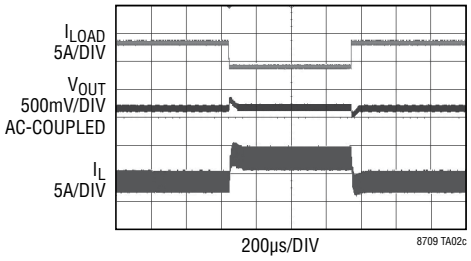


L1: WÜRTH-HCI, 7.3µH, 7443551730
MP: FAIRCHILD, FDD4141
MN: INFINEON, BSC026N04LS
R_{SENSE1}: 2mΩ, 2512
R_{SENSE2}: 4mΩ, 2512
C_{IN1}: OSCON, 35V, 120µF, 35SVPF120M
C_{IN2}: 50V, 10µF, X7S, 1210
C_{OUT1}: 25V, 22µF, X7R, 1812
C_{OUT2}: OSCON, 16V, 150µF, 16SEQP150M

Efficiency and Power Loss vs Load Current ($–V_{IN}$ = –24V)

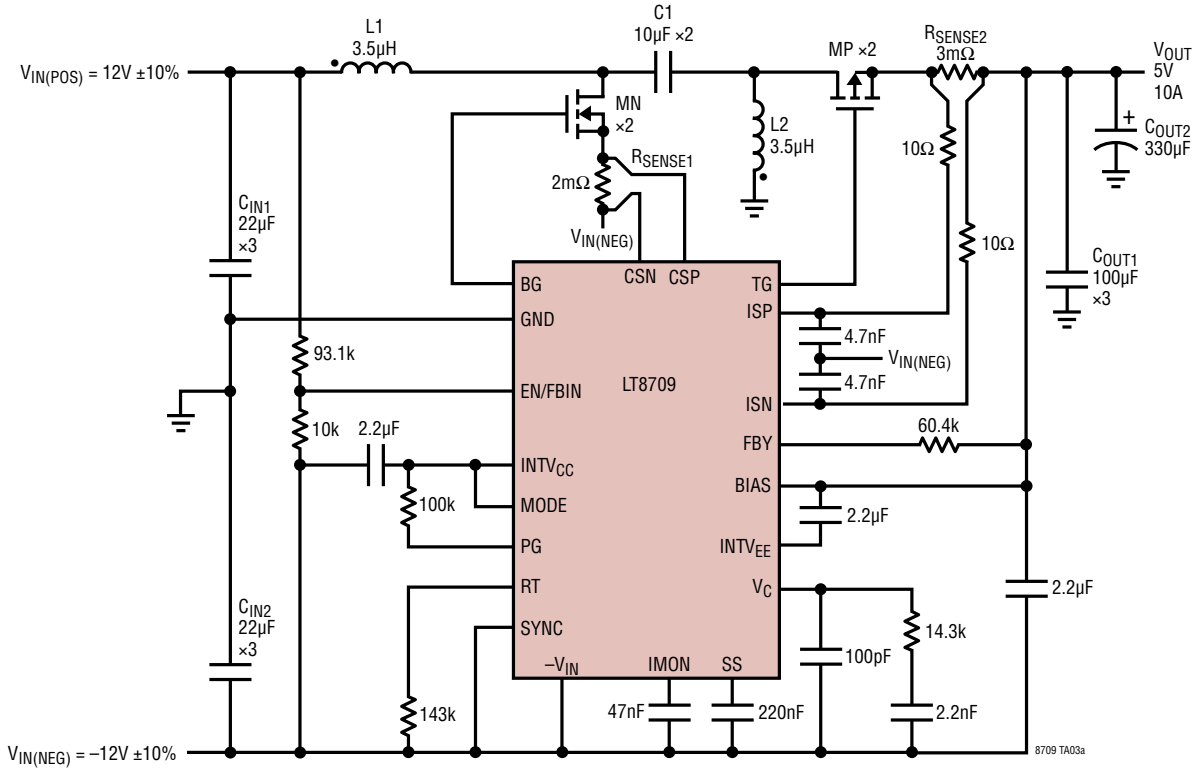


Transient Response with 3A to 8A to 3A Output Load Step ($–V_{IN}$ = –24V)



TYPICAL APPLICATION

Split Supply Input Generates 5V with Up to 10A Output Current

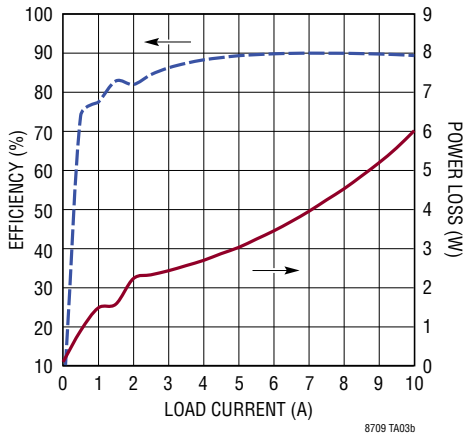


$$DC = \frac{V_{OUT}}{V_{IN(POS)} + |V_{IN(NEG)}| + V_{OUT}} \quad FET\ BV_{DSS} > V_{IN(POS)} + |V_{IN(NEG)}| + V_{OUT} \quad C1_{VRATING} > V_{IN(POS)}$$

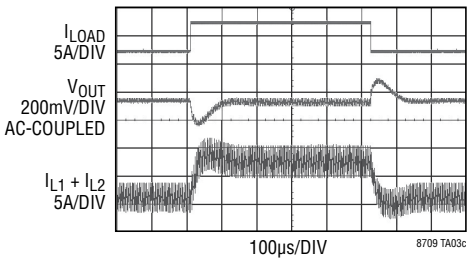
L1, L2: WÜRTH-CFWI, 3.5µH, 74485540350
MN: INFINEON, BSC059N04LSG
MP: FAIRCHILD, FDD4141
R_{SENSE1}: 2mΩ, 2512
R_{SENSE2}: 3mΩ, 2512

C_{IN1}: 22µF, 25V, 1812, X7R
C_{IN2}: 22µF, 25V, 1812, X7R
C1: 10µF, 25V, 1210, X7R
C_{OUT1}: 100µF, 16V, 1210, X5R
C_{OUT2}: OSCON, 16V, 330µF, 16SEQP330M

Efficiency and Power Loss vs Load Current (V_{IN} = ±12V)

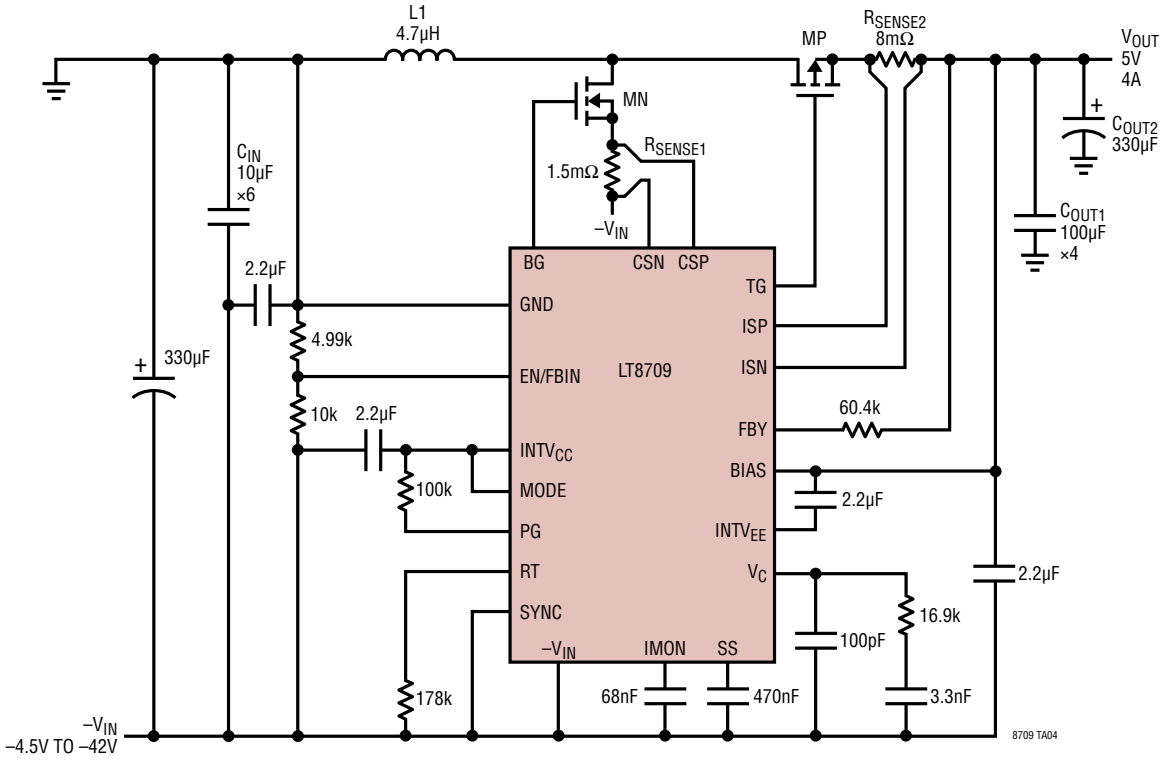


Transient Response with 3A to 8A to 3A Output Load Step (V_{IN} = ±12V)



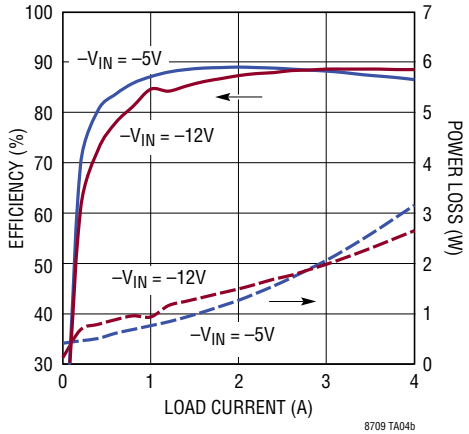
TYPICAL APPLICATION

200kHz, –4.5V to –42V Input to 5V/4A Output Negative Inverting Converter

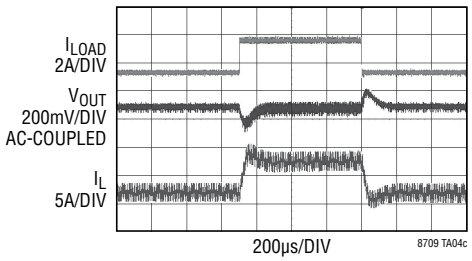


L1: WÜRTH-HCI, 4.7µH, 7443551470
MP: VISHAY, SUD50P06
MN: FAIRCHILD, FDMS86500L
R_{SENSE1}: 1.5mΩ, 2512
R_{SENSE2}: 8mΩ, 2512
C_{IN1}: 10µF, 50V, 1206, X5R
C_{OUT1}: 100µF, 6.3V, 1812, X5R
C_{OUT2}: OSCON, 16V, 330µF, 16SEQP330M

Efficiency and Power Loss vs Load Current

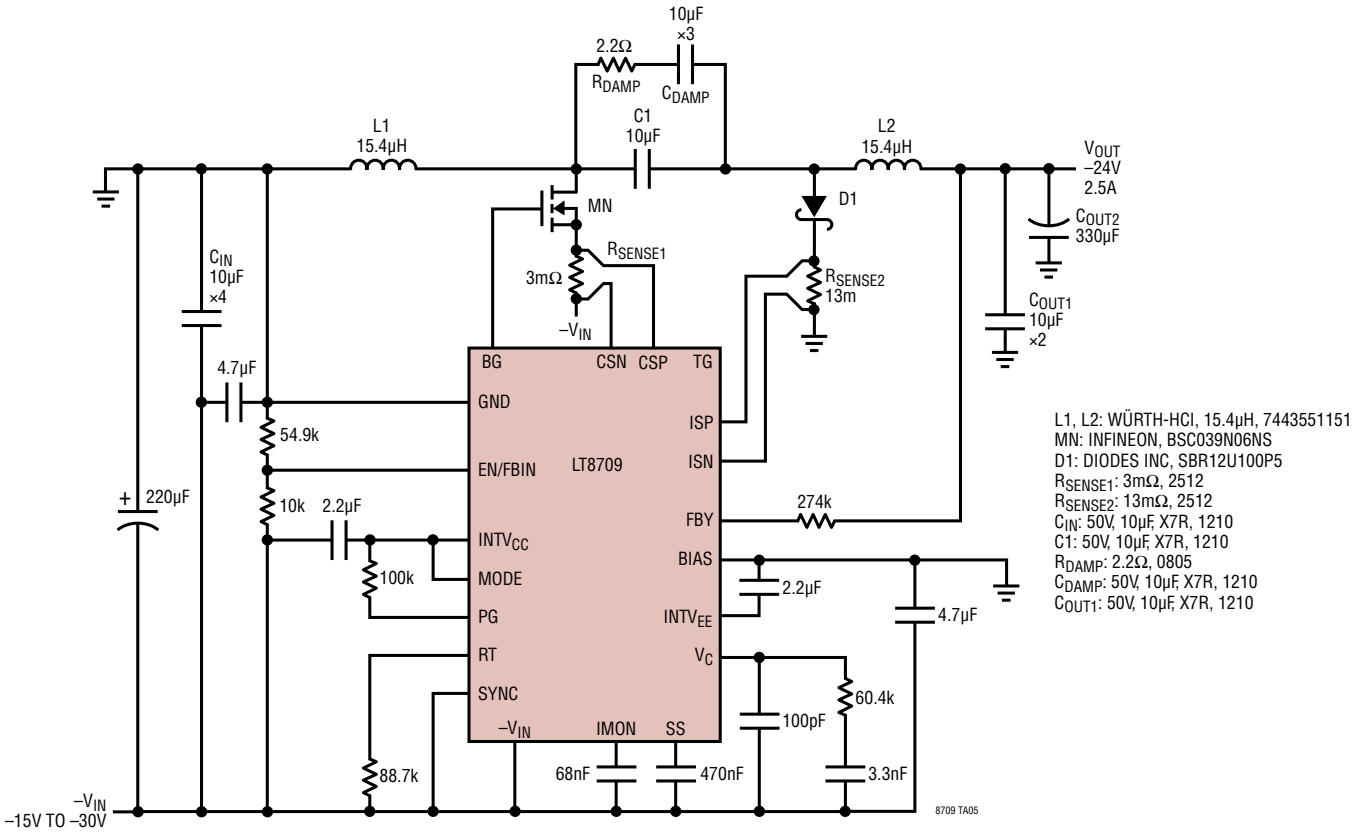


Transient Response with 1.5A to 4A to 1.5A Output Load Step ($–V_{IN}$ = –5V)

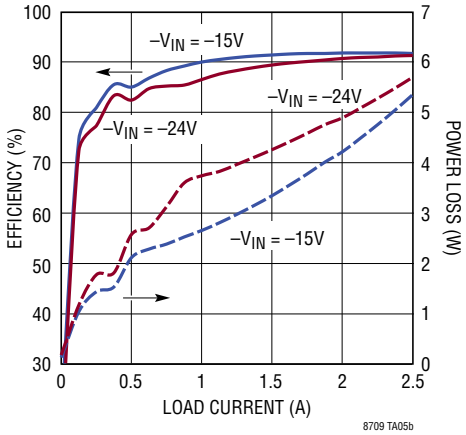


TYPICAL APPLICATION

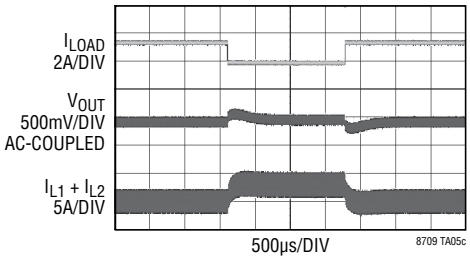
400kHz, Negative Buck-Boost Converter Generates a –24V/2.5A Output from a –15V to –30V Input



Efficiency and Power Loss vs Load Current

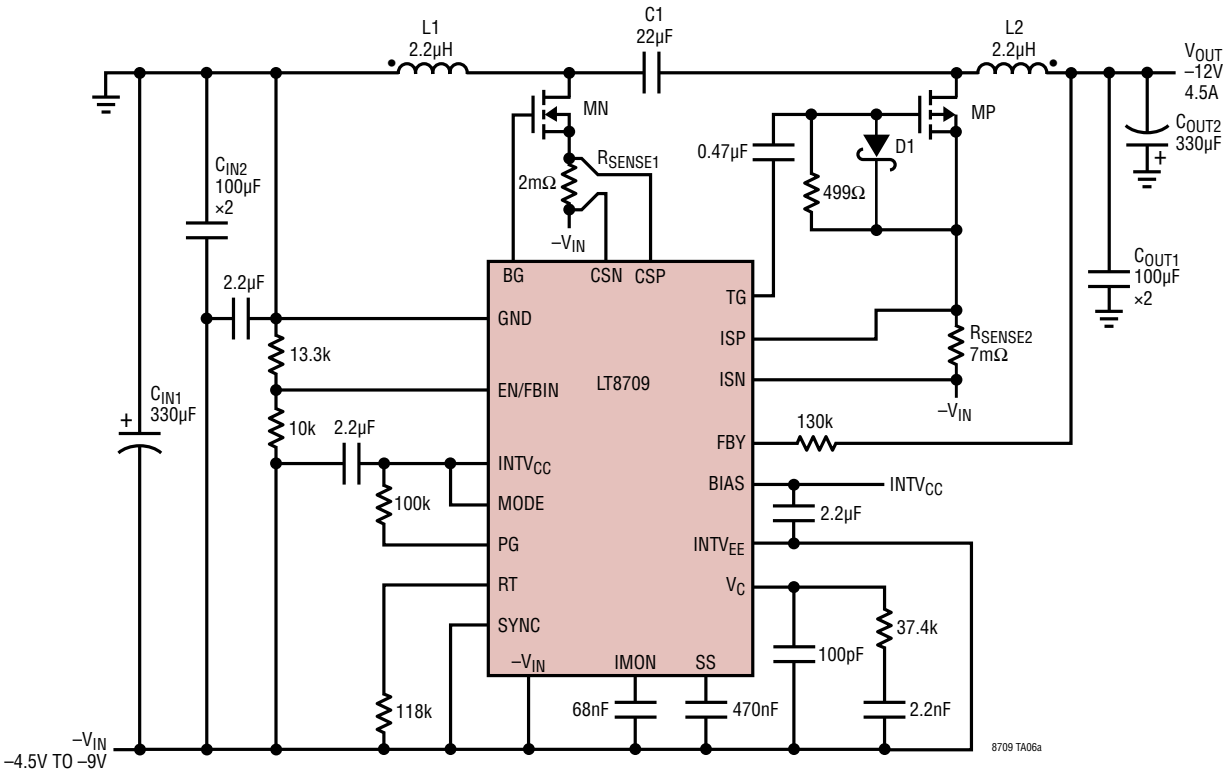


Transient Response with 1A to 2.5A to 1A Output Load Step (–V_{IN} = –24V)



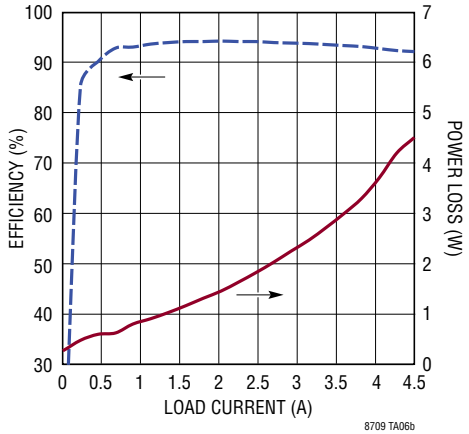
TYPICAL APPLICATION

High Power 300kHz, Negative Boost Converter Generates a –12V/4.5A Output from a –4.5V to –9V Input

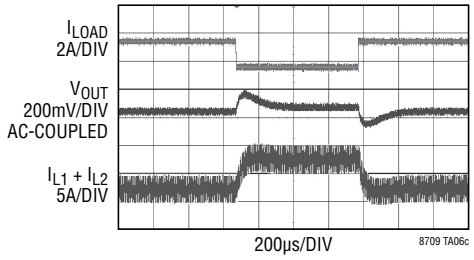


L1, L2: WÜRTH-CFWI, 2.2µH, 74485540220
MN: INFINEON, BSC0901NSI
MP: VISHAY, Si7143DP
R_{SENSE1}: 2mΩ, 2512
R_{SENSE2}: 7mΩ, 2512
D1: ON-SEMI, MBRM110
C_{IN1}: OSCON, 16V, 330µF, 16SEQP330M
C_{IN2}: 100µF, 16V, X5R, 1210
C1: 25V, 22µF, X7R, 1812
C_{OUT1}: 100µF, 16V, X5R, 1210
C_{OUT2}: OSCON, 16V, 330µF, 16SEQP330M

Efficiency and Power Loss vs Load Current ($–V_{IN}$ = –5V)



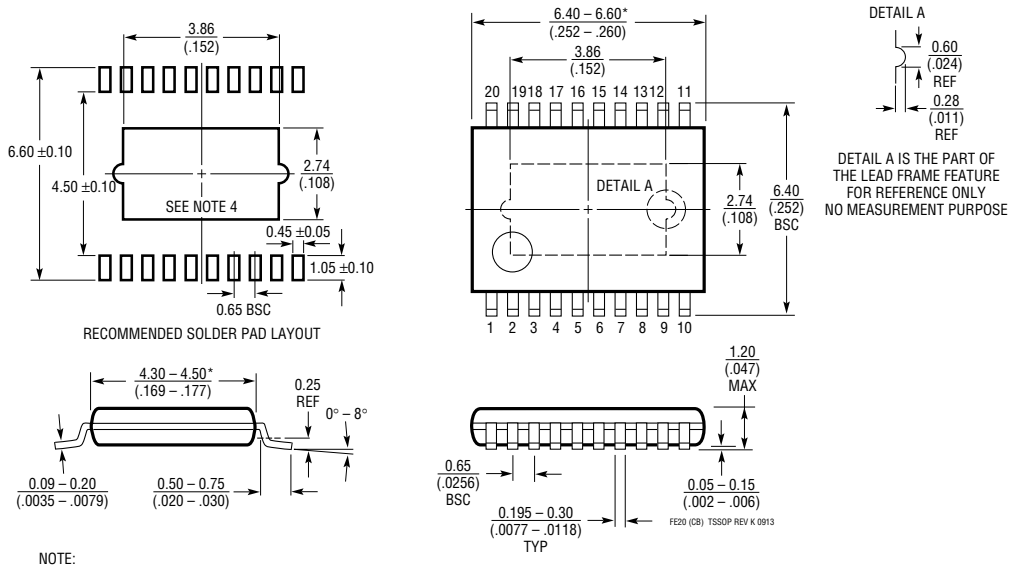
Transient Response with 2A to 4A to 2A Output Load Step ($–V_{IN}$ = –5V)



PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LT8709#packaging for the most recent package drawings.

FE Package
20-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1663 Rev K)
Exposed Pad Variation CB



NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN MILLIMETERS (INCHES)
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT

*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	03/16	Corrected Figure 6	18
		Corrected Figure 9	21
		Modified Figure 15	27
		Modified Schematic	42