12-Bit, 300ksps Sampling A/D Converters with Reference

FEATURES

- Single Supply 5V or ±5V Operation
- 300ksps Sample Rate
- 75mW (Typ) Power Dissipation
- On-Chip 25ppm/°C Reference
- Internal Synchronized Clock; No Clock Required
- High Impedance Analog Input
- 70dB S/(N + D) and 77dB THD at Nyquist
- ±1/2LSB INL and ±3/4LSB DNL Max (A Grade)
- ESD Protected On All Pins
- 24-Pin Narrow PDIP and SW Packages
- Variety of Input Ranges:
  0V to 5V (LTC1273)
  ±2.5V (LTC1275)
  ±5V (LTC1276)

APPLICATIONS

- High Speed Data Acquisition
- Digital Signal Processing
- Multiplexed Data Acquisition Systems
- Audio and Telecom Processing
- Spectrum Analysis

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DESCRIPTION

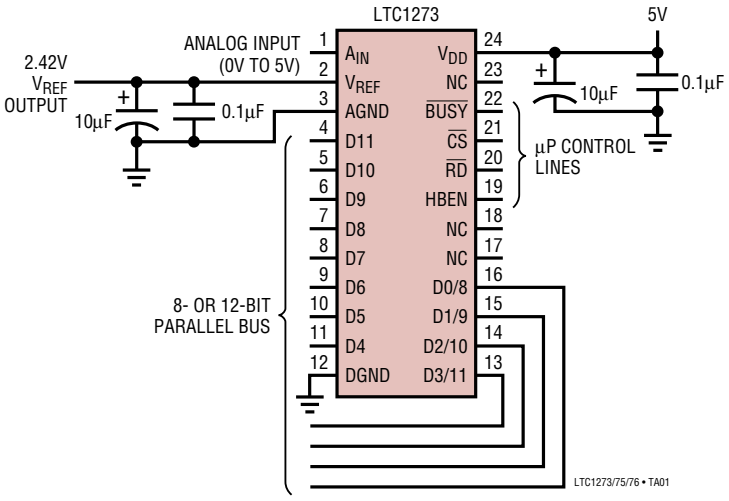
The LTC®1273/LTC1275/LTC1276 are 300ksps, sampling 12-bit A/D converters that draw only 75mW from single 5V or ±5V supplies. These easy-to-use devices come complete with 600ns sample-and-holds, precision references and internally trimmed clocks. Unipolar and bipolar conversion modes provide flexibility for various applications. They are built with LTBiCMOS™ switched capacitor technology.

These devices have 25ppm/°C (max) internal references. The LTC1273 converts 0V to 5V unipolar inputs from a single 5V supply. The LTC1275/LTC1276 convert ±2.5V and ±5V respectively from ±5V supplies. Maximum DC specifications include ±1/2LSB INL, ±3/4LSB DNL and 25ppm/°C full scale drift over temperature. Outstanding AC performance includes 70dB S/(N + D) and 77dB THD at the Nyquist input frequency of 150kHz.

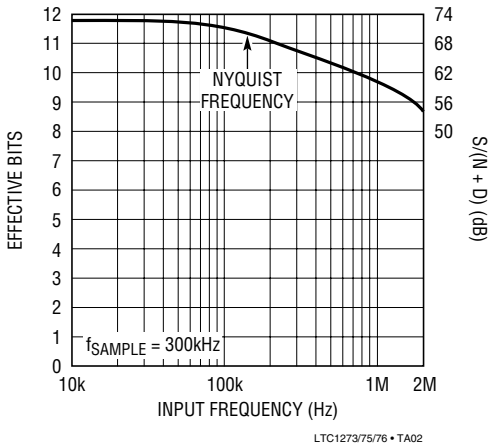
The internal clock is trimmed for 2.7µs maximum conversion time. The clock automatically synchronizes to each sample command eliminating problems with asynchronous clock noise found in competitive devices. A high speed parallel interface eases connections to FIFOs, DSPs and microprocessors.

TYPICAL APPLICATION

Single 5V Supply, 300ksps, 12-Bit Sampling A/D Converter



Effective Bits and Signal to (Noise + Distortion) vs Input Frequency

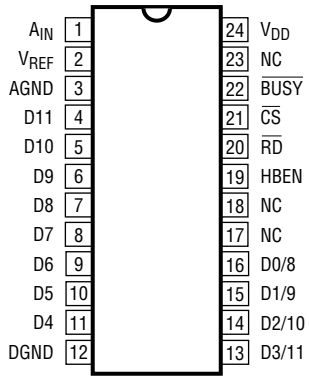


ABSOLUTE MAXIMUM RATINGS (Notes 1 and 2)

Supply Voltage (V_{DD}) 12V
Negative Supply Voltage (V_{SS})
  LTC1275/LTC1276 ..... –6V to GND
Total Supply Voltage (V_{DD} to V_{SS})
  LTC1275/LTC1276 ..... 12V
Analog Input Voltage (Note 3)
  LTC1273 ..... –0.3V to V_{DD} + 0.3V
  LTC1275/LTC1276 ..... V_{SS} – 0.3V to V_{DD} + 0.3V
Digital Input Voltage (Note 4)
  LTC1273 ..... –0.3V to 12V
  LTC1275/LTC1276 ..... V_{SS} – 0.3V to 12V
Digital Output Voltage (Note 3)
  LTC1273 ..... –0.3V to V_{DD} + 0.3V
  LTC1275/LTC1276 ..... V_{SS} – 0.3V to V_{DD} + 0.3V
Power Dissipation 500mW
Operating Temperature Range
  LTC1273AC, LTC1273BC, LTC1275AC
  LTC1275BC, LTC1276AC, LTC1276BC .... 0°C to 70°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION

TOP VIEW



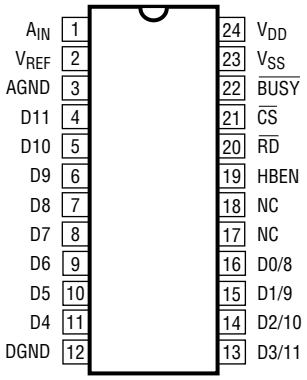
N PACKAGE
24-LEAD PDIP

SW PACKAGE
24-LEAD PLASTIC SO WIDE

T_{JMAX} = 110°C, θ_{JA} = 100°C/W (N)
T_{JMAX} = 110°C, θ_{JA} = 130°C/W (SW)

ORDER PART NUMBER
LTC1273ACN
LTC1273BCN
LTC1273ACSW
LTC1273BCSW

TOP VIEW



N PACKAGE
24-LEAD PDIP

SW PACKAGE
24-LEAD PLASTIC SO WIDE

T_{JMAX} = 110°C, θ_{JA} = 100°C/W (N)
T_{JMAX} = 110°C, θ_{JA} = 130°C/W (SW)

ORDER PART NUMBER
LTC1275ACN
LTC1275BCN
LTC1275ACSW
LTC1275BCSW
LTC1276ACN
LTC1276BCN
LTC1276ACSW
LTC1276BCSW

Order Options Tape and Reel: Add #TR Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: http://www.linear.com/leadfree/

Consult LTC Marketing for parts specified with wider operating temperature ranges.

CONVERTER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specfications are at T_A = 25°C. With Internal Reference (Notes 5 and 6)

PARAMETER	CONDITIONS		LTC1273A/LTC1275A/LTC1276A MIN	TYP	MAX	LTC1273B/LTC1275B/LTC1276B MIN	TYP	MAX	UNITS
Resolution (No Missing Codes)		●	12			12			Bits
Integral Linearity Error	(Note 7)				±1/2			±1	LSB
	Commercial	●			±1/2			±1	LSB
	Military	●			±3/4			±1	LSB
Differential Linearity Error	Commercial	●			±3/4			±1	LSB
	Military	●			±1			±1	LSB
Offset Error	(Note 8)				±3			±4	LSB
		●			±4			±6	LSB
Gain Error					±10			±15	LSB
Gain Error Tempco	$I_{OUT(REFERENCE)}$ = 0	●		±5	±35		±10	±45	ppm/°C

DYNAMIC ACCURACY (Note 5)

SYMBOL	PARAMETER	CONDITIONS	LTC1273A/LTC1275A/LTC1276A LTC1273B/LTC1275B/LTC1276B MIN	TYP	MAX	UNITS
S/(N + D)	Signal-to-Noise Plus Distortion Ratio	50kHz/150kHz Input Signal		72/70		dB
THD	Total Harmonic Distortion Up to 5th Harmonic	50kHz/150kHz Input Signal		–83/–74		dB
	Peak Harmonic or Spurious Noise	50kHz/150kHz Input Signal		–85/–76		dB
IMD	Intermodulation Distortion	f_{IN1} = 29.37kHz, f_{IN2} = 32.446kHz		–80		dB
	Full Power Bandwidth			4.5		MHz
	Full Linear Bandwidth (S/(N + D) ≥ 68dB)			200		kHz

ANALOG INPUT

The ● denotes the specifications which apply over the full operating temperature range, otherwise specfications are at T_A = 25°C. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		LTC1273A/LTC1275A/LTC1276A LTC1273B/LTC1275B/LTC1276B MIN	TYP	MAX	UNITS
V_{IN}	Analog Input Range (Note 9)	4.95V ≤ V_{DD} ≤ 5.25V (LTC1273)	●		0 to 5		V
		4.75V ≤ V_{DD} ≤ 5.25V, –5.25V ≤ V_{SS} ≤ –2.45V (LTC1275)	●		±2.5		V
		4.95V ≤ V_{DD} ≤ 5.25V, –5.25V ≤ V_{SS} ≤ –4.95V (LTC1276)	●		±5		V
I_{IN}	Analog Input Leakage Current	$\overline{CS}$ = High	●			±1	µA
C_{IN}	Analog Input Capacitance	Between Conversions (Sample Mode)			50		pF
		During Conversions (Hold Mode)			5		pF
t_{ACQ}	Sample-and-Hold Acquisition Time	Commercial	●			600	ns
		Military	●			1000	ns

INTERNAL REFERENCE CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specfications are at T_A = 25°C. (Note 5)

PARAMETER	CONDITIONS		LTC1273A/LTC1275A/LTC1276A MIN	TYP	MAX	LTC1273B/LTC1275B/LTC1276B MIN	TYP	MAX	UNITS
V_{REF} Output Voltage	I_{OUT} = 0		2.400	2.420	2.440	2.400	2.420	2.440	V
V_{REF} Output Tempco	I_{OUT} = 0	●		±5	±25		±10	±45	ppm/°C
V_{REF} Line Regulation	4.95V ≤ V_{DD} ≤ 5.25V			0.01			0.01		LSB/V
	–5.25V ≤ V_{SS} ≤ –4.95V			0.01			0.01		LSB/V
V_{REF} Load Regulation	0V ≤ $\lvert I_{OUT} \rvert$ ≤ 1mA			2			2		LSB/mA

DIGITAL INPUTS AND DIGITAL OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specfications are at T_A = 25°C. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		LTC1273A/LTC1275A/LTC1276A LTC1273B/LTC1275B/LTC1276B MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	V_{DD} = 5.25V	●	2.4			V
V_{IL}	Low Level Input Voltage	V_{DD} = 4.95V	●			0.8	V
I_{IN}	Digital Input Current	V_{IN} = 0V to V_{DD}	●			±10	µA
C_{IN}	Digital Input Capacitance				5		pF
V_{OH}	High Level Output Voltage	V_{DD} = 4.95V					
		I_O = –10µA			4.7		V
		I_O = –200µA	●	4.0			V
V_{OL}	Low Level Output Voltage	V_{DD} = 4.95V					
		I_O = 160µA			0.05		V
		I_O = 1.6mA	●		0.10	0.4	V
I_{OZ}	High Z Output Leakage D11-D0/8	V_{OUT} = 0V to V_{DD}, $\overline{CS}$ High	●			±10	µA
C_{OZ}	High Z Output Capacitance D11-D0/8	$\overline{CS}$ High (Note 9)	●			15	pF
I_{SOURCE}	Output Source Current	V_{OUT} = 0V			–10		mA
I_{SINK}	Output Sink Current	V_{OUT} = V_{DD}			10		mA

POWER REQUIREMENTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specfications are at T_A = 25°C. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		LTC1273A/LTC1275A/LTC1276A LTC1273B/LTC1275B/LTC1276B MIN	TYP	MAX	UNITS
V_{DD}	Positive Supply Voltage	LTC1273/LTC1276 (Notes 10, 11)		4.95		5.25	V
		LTC1275 (Note 10)		4.75		5.25	V
V_{SS}	Negative Supply Voltage	LTC1275 (Note 10)		–2.45		–5.25	V
		LTC1276 (Notes 10, 11)		–4.95		–5.25	V
I_{DD}	Positive Supply Current		●		15	25	mA
I_{SS}	Negative Supply Current	LTC1275/LTC1276	●		0.065	0.200	mA
P_D	Power Dissipation				75		mW

TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specfications are at T_A = 25°C. See Timing Characteristics Figures (Note 5)

SYMBOL	PARAMETER	CONDITIONS		LTC1273A/LTC1275A/LTC1276A LTC1273B/LTC1275B/LTC1276B MIN	TYP	MAX	UNITS
$f_{SAMPLE(MAX)}$	Maximum Sampling Frequency	(Note 10)					
		Commercial	●	300			kHz
		Military	●	250			kHz
t_{CONV}	Conversion Time	Commercial	●			2.7	µs
		Military	●			3.0	µs
t_1	$\overline{CS}$ to $\overline{RD}$ Setup Time		●	0			ns
t_2	$\overline{RD}$ to $\overline{BUSY}$ Delay	C_L = 50pF			80	190	ns
		Commercial	●			230	ns
		Military	●			270	ns

TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specfications are at T_A = 25°C. See Timing Characteristics Figures (Note 5)

SYMBOL	PARAMETER	CONDITIONS		LTC1273A/LTC1275A/LTC1276A LTC1273B/LTC1275B/LTC1276B MIN	TYP	MAX	UNITS
t_3	Data Access Time After $\overline{RD}\downarrow$	C_L = 20pF			40	90	ns
		Commercial	●			110	ns
		Military	●			120	ns
		C_L = 100pF			50	125	ns
		Commercial	●			150	ns
		Military	●			170	ns
t_4	$\overline{RD}$ Pulse Width		●	t_3			ns
t_5	$\overline{CS}$ to $\overline{RD}$ Hold Time		●	0			ns
t_6	Data Setup Time After $\overline{BUSY}\uparrow$				40	70	ns
		Commercial	●			90	ns
		Military	●			100	ns
t_7	Bus Relinquish Time			20	30	75	ns
		Commercial	●	20		85	ns
		Military	●	20		90	ns
t_8	HBEN to $\overline{RD}$ Setup Time		●	0			ns
t_9	HBEN to $\overline{RD}$ Hold Time		●	0			ns
t_{10}	Delay Between $\overline{RD}$ Operations		●	40			ns
t_{11}	Delay Between Conversions	(Note 10)		500			ns
		Commercial	●	600			ns
		Military	●	1000			ns
t_{12}	Aperture Delay of Sample-and-Hold				25		ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltage values are with respect to ground with DGND and AGND wired together (unless otherwise noted).

Note 3: When these pin voltages are taken below V_{SS} (ground for LTC1273) or above V_{DD}, they will be clamped by internal diodes. This product can handle input currents greater than 60mA below V_{SS} (ground for LTC1273) or above V_{DD} without latch-up.

Note 4: When these pin voltages are taken below V_{SS} (ground for LTC1273) they will be clamped by internal diodes. This product can handle input currents greater than 60mA below V_{SS} (ground for LTC1273) without latch-up. These pins are not clamped to V_{DD}.

Note 5: V_{DD} = 5V (V_{SS} = –5V for LTC1275/LTC1276), 300kHz at 70°C and 250kHz at 125°C, $t_r = t_f$ = 5ns unless otherwise specified.

Note 6: Linearity, offset and full scale specifications apply for unipolar and bipolar modes.

Note 7: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 8: Bipolar offset (LTC1275/LTC1276) is the different voltage measured from –0.5LSB when the LTC1275/LTC1276 output code flickers between 0000 0000 0000 and 1111 1111 1111.

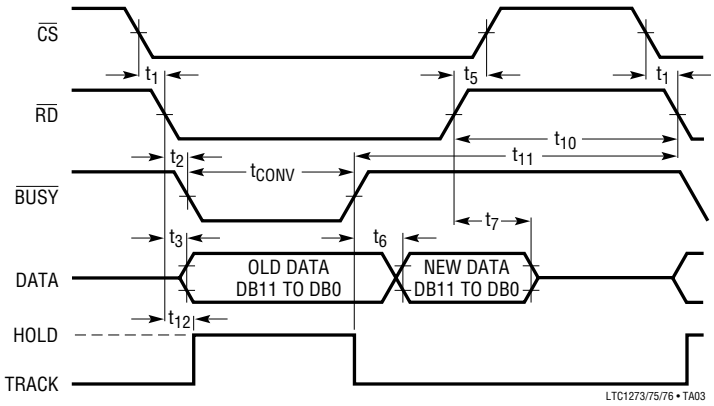
Note 9: Guaranteed by design, not subject to test.

Note 10: Recommended operating conditions.

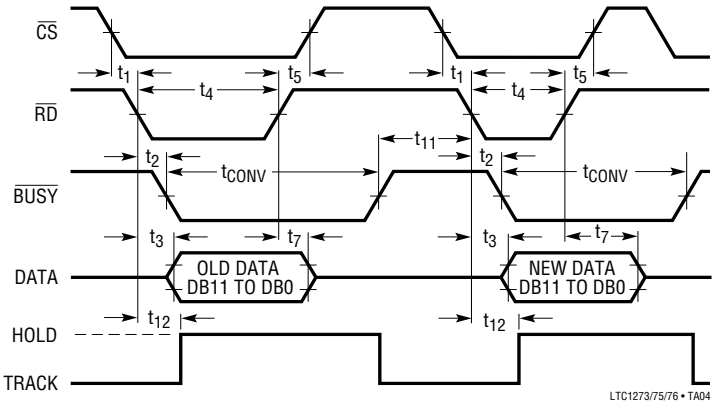
Note11: A_{IN} must not exceed V_{DD} or fall below V_{SS} by more than 50mV for specified accuracy. Therefore the minimum supply voltage for the LTC1273 is +4.95V. The minimum supplies for the LTC1275 are +4.75V and –2.45V and the minimum supplies for the LTC1276 are ±4.95V.

TIMING CHARACTERISTICS (Note 5)

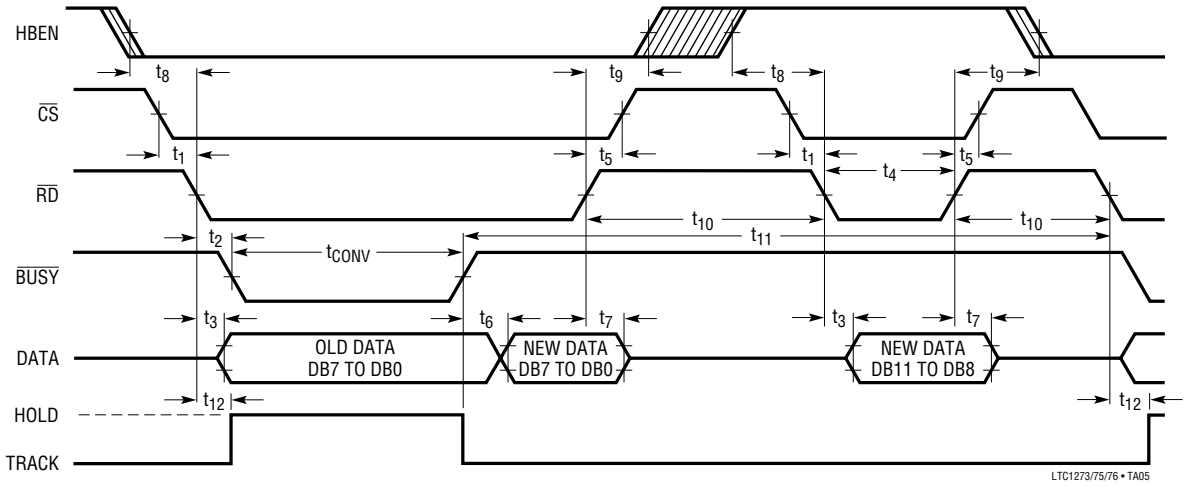
Slow Memory Mode, Parallel Read Timing Diagram



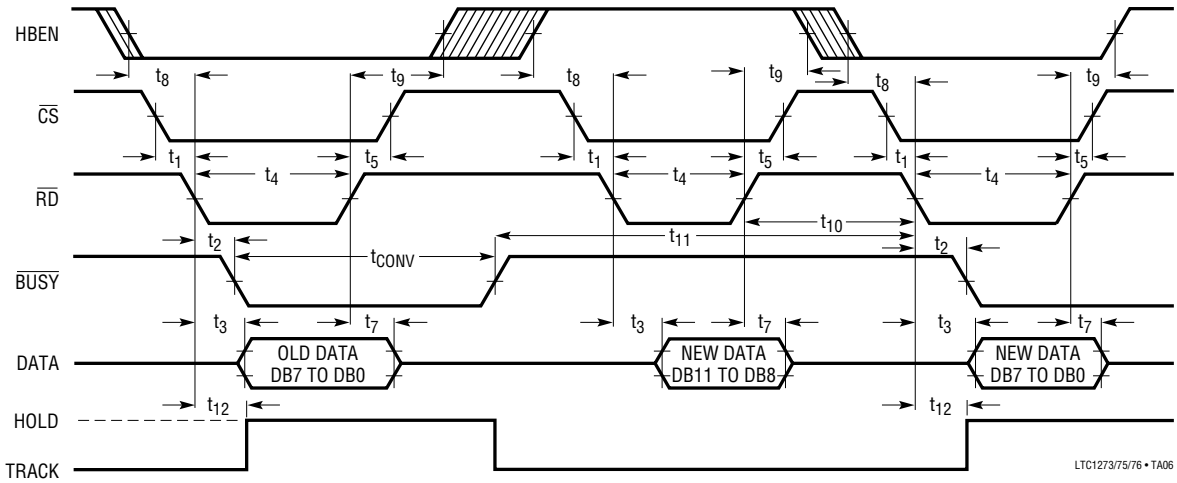
ROM Mode, Parallel Read Timing Diagram



Slow Memory Mode, Two Byte Read Timing Diagram

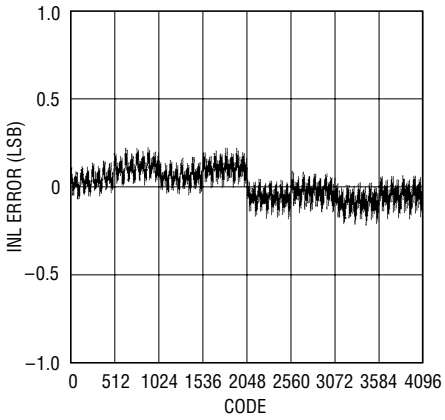


ROM Mode, Two Byte Read Timing Diagram



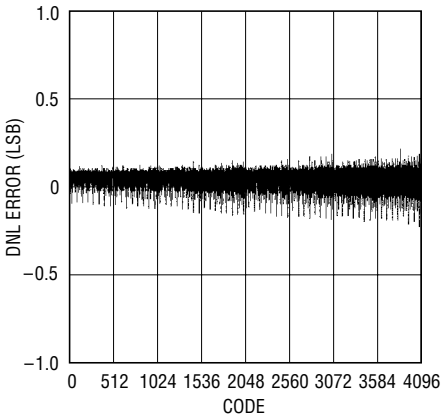
TYPICAL PERFORMANCE CHARACTERISTICS

Integral Nonlinearity



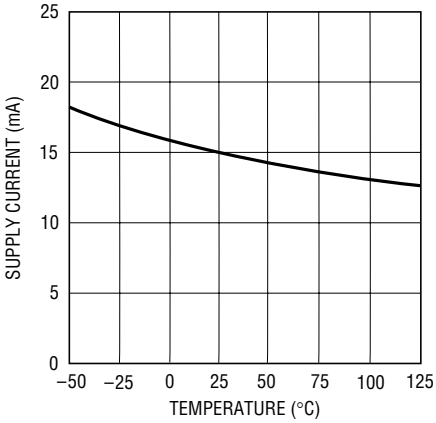
LTC1273/75/76 • TPC01

Differential Nonlinearity



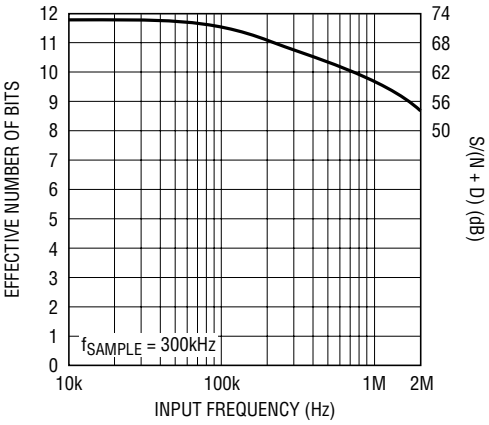
LTC1273/75/76 • TPC02

Supply Current vs Temperature



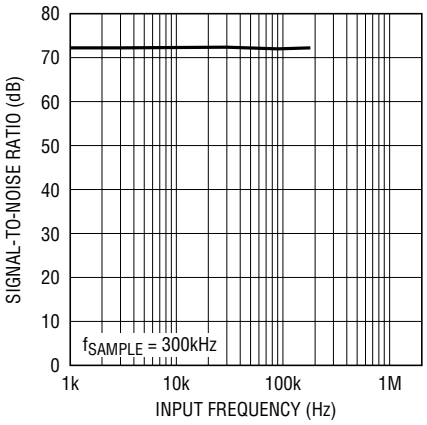
LTC1273/75/76 • TPC03

ENOBs and S/(N + D) vs Input Frequency



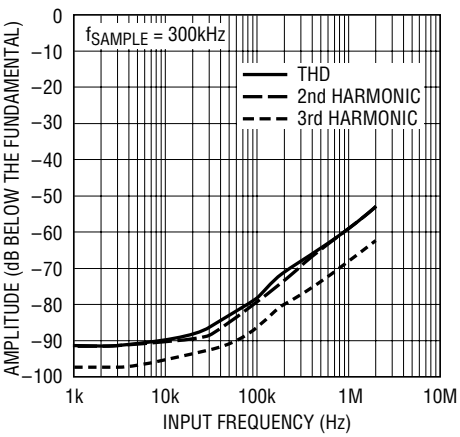
LTC1273/75/76 • TPC04

Signal-to-Noise Ratio (Without Harmonics) vs Input Frequency



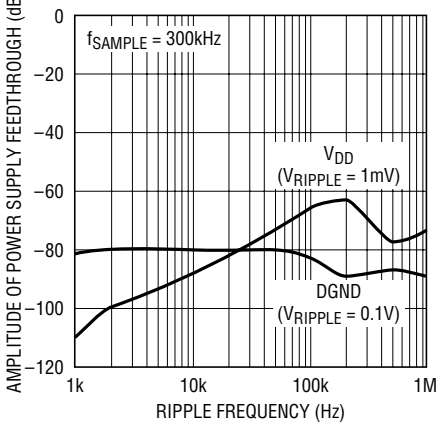
LTC1273/75/76 • TPC05

Distortion vs Input Frequency



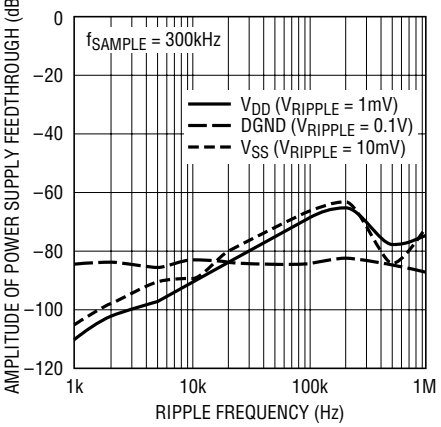
LTC1273/75/76 • TPC06

Power Supply Feedthrough vs Ripple Frequency (LTC1273)



LTC1273/75/76 • TPC07

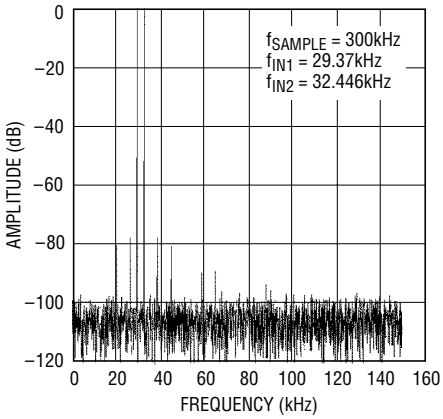
Power Supply Feedthrough vs Ripple Frequency (LTC1275/76)



LTC1273/75/76 • TPC08

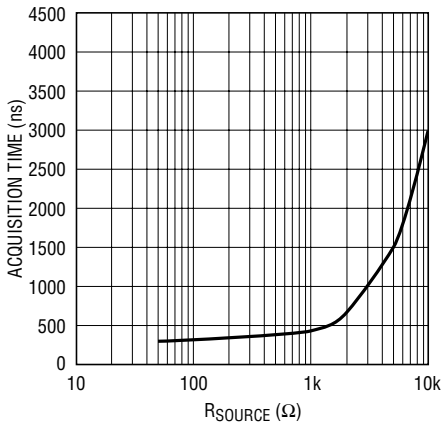
TYPICAL PERFORMANCE CHARACTERISTICS

Intermodulation Distortion Plot



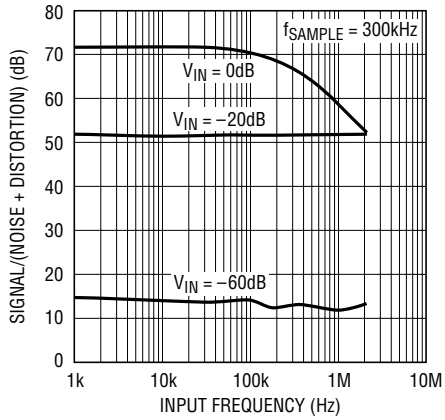
LTC1273/75/76 • F05

Acquisition Time vs Source Impedance



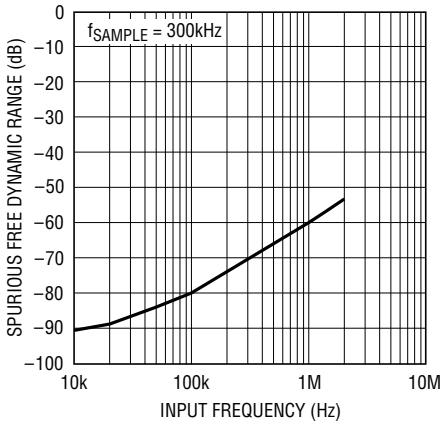
LTC1273/75/76 • TPC10

S/(N + D) vs Input Frequency and Amplitude



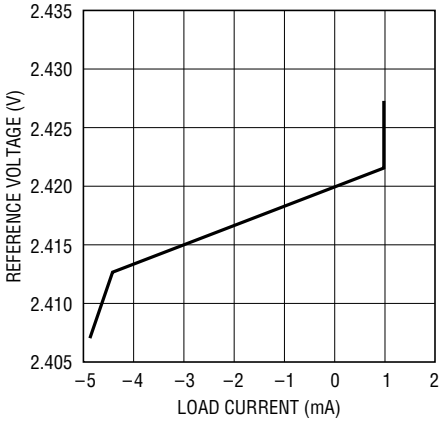
LTC1273/75/76 • TPC11

Spurious Free Dynamic Range vs Input Frequency



LTC1273/75/76 • TPC12

Reference Voltage vs Load Current



LTC1273/75/76 • TPC13

PIN FUNCTIONS

A_{IN} (Pin 1): Analog Input. 0V to 5V (LTC1273), ±2.5V (LTC1275) or ±5V (LTC1276).

V_{REF} (Pin 2): +2.42V Reference Output. Bypass to AGND (10µF tantalum in parallel with 0.1µF ceramic).

AGND (Pin 3): Analog Ground.

D11-D4 (Pins 4 to 11): Three-State Data Outputs.

DGND (Pin 12): Digital Ground.

D3/11-D0/8 (Pins 13 to 16): Three-State Data Outputs.

NC (Pins 17 and 18): No Connection.

HBEN (Pin 19): High Byte Enable Input. This pin is used to multiplex the internal 12-bit conversion result into the lower bit outputs (D7-D0/8). See Table 1. HBEN also disables conversion start when HIGH.

$\overline{RD}$ (Pin 20): READ Input. This active low signal starts a conversion when $\overline{CS}$ and HBEN are low. $\overline{RD}$ also enables the output drivers when $\overline{CS}$ is low.

$\overline{CS}$ (Pin 21): The CHIP SELECT Input must be low for the ADC to recognize $\overline{RD}$ and HBEN inputs.

$\overline{BUSY}$ (Pin 22): The $\overline{BUSY}$ Output shows the converter status. It is low when a conversion is in progress.

PIN FUNCTIONS

V_{SS} (Pin 23): Negative Supply. –5V for LTC1275/LTC1276. Bypass to AGND with 0.1µF ceramic.

V_{DD} (Pin 24): Positive Supply, 5V. Bypass to AGND (10µF tantalum in parallel with 0.1µF ceramic).

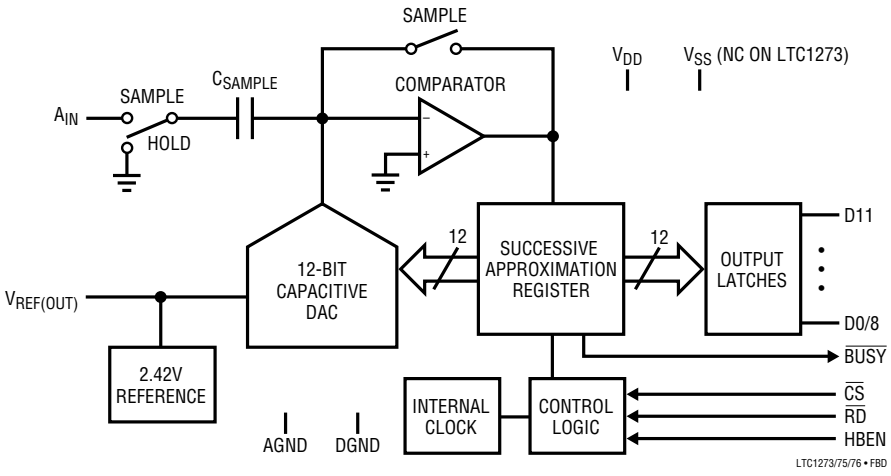
NC (Pin 23): No Connection for LTC1273.

Table 1. Data Bus Output, $\overline{CS}$ and $\overline{RD}$ = LOW

	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8	Pin 9	Pin 10	Pin 11	Pin 13	Pin 14	Pin 15	Pin 16
MNEMONIC*	D11	D10	D9	D8	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
HBEN = LOW	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
HBEN = HIGH	DB11	DB10	DB9	DB8	LOW	LOW	LOW	LOW	DB11	DB10	DB9	DB8

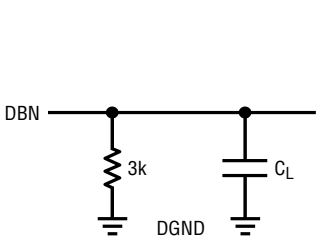
* D11...D0/8 are the ADC data output pins.
DB11...DB0 are the 12-bit conversion results, DB11 is the MSB.

FUNTIONAL BLOCK DIAGRAM

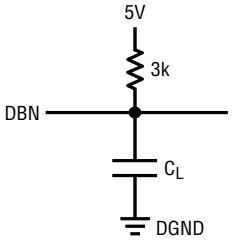


TEST CIRCUITS

Load Circuits for Access Time



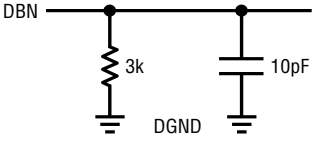
A) HIGH-Z TO V_{OH} (t_3) AND V_{OL} TO V_{OH} (t_6)



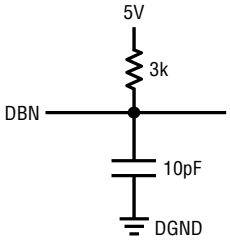
B) HIGH-Z TO V_{OL} (t_3) AND V_{OH} TO V_{OL} (t_6)

1273/75/76 • TA07

Load Circuits for Output Float Delay



A) V_{OH} TO HIGH-Z



B) V_{OL} TO HIGH-Z

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APPLICATIONS INFORMATION

CONVERSION DETAILS

The LTC1273/LTC1275/LTC1276 use a successive approximation algorithm and an internal sample-and-hold circuit to convert an analog signal to a 12-bit parallel or 2-byte output. The ADCs are complete with a precision reference and an internal clock. The control logic provides easy interface to microprocessors and DSPs. (Please refer to the Digital Interface section for the data format.)

Conversion start is controlled by the $\overline{CS}$, $\overline{RD}$ and HBEN inputs. At the start of conversion the successive approximation register (SAR) is reset and the three-state data outputs are enabled. Once a conversion cycle has begun it cannot be restarted.

During conversion, the internal 12-bit capacitive DAC output is sequenced by the SAR from the most significant bit (MSB) to the least significant bit (LSB). Referring to Figure 1, the A_{IN} input connects to the sample-and-hold capacitor during the acquire phase, and the comparator offset is nulled by the feedback switch. In this acquire phase, a minimum delay of 600ns will provide enough time for the sample-and-hold capacitor to acquire the analog signal. During the convert phase, the comparator feedback switch opens, putting the comparator into the compare mode. The input switch switches C_{SAMPLE} to ground, injecting the analog input charge onto the summing junction. This input charge is successively compared with the binary-weighted charges supplied by the capacitive DAC. Bit decisions are made by the high speed comparator. At the end of a conversion, the DAC output balances the A_{IN} input charge. The SAR contents (a 12-bit data word) which represent the A_{IN} are loaded into the 12-bit output latches.

DYNAMIC PERFORMANCE

The LTC1273/LTC1275/LTC1276 have an exceptionally high speed sampling capability. FFT (Fast Fourier Transform) test techniques are used to characterize the ADC's frequency response, distortion and noise at the rated throughput. By applying a low distortion sine wave and analyzing the digital output using an FFT algorithm, the ADC's spectral content can be examined for frequencies outside the fundamental. Figure 2 shows a typical LTC1275 FFT plot.

Signal-to-Noise Ratio

The Signal-to-Noise plus Distortion Ratio [S/(N + D)] is the ratio between the RMS amplitude of the fundamental input frequency to the RMS amplitude of all other frequency components at the A/D output. The output is band limited to frequencies from above DC and below half the sampling frequency. Figure 2 shows a typical spectral content with a 300kHz sampling rate and a 29kHz input. The dynamic performance is excellent for input frequencies up to the Nyquist limit of 150kHz.

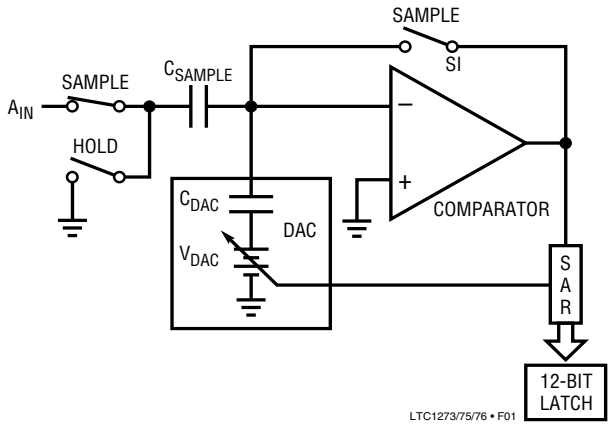

Figure 1. A_{IN} Input

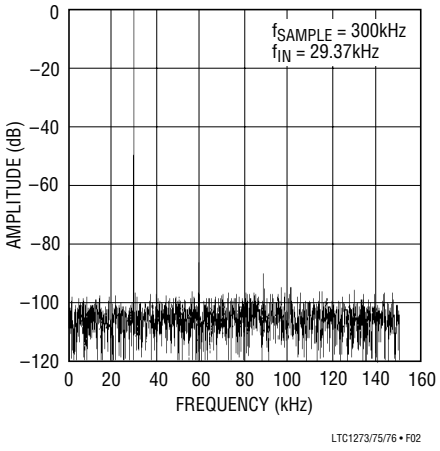

Figure 2. LTC1275 Nonaveraged, 1024 Point FFT Plot

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Effective Number of Bits

The Effective Number of Bits (ENOBs) is a measurement of the resolution of an ADC and is directly related to the S/(N + D) by the equation:

$$N = [S/(N + D) – 1.76]/6.02$$

where N is the Effective Number of Bits of resolution and S/(N + D) is expressed in dB. At the maximum sampling rate of 300kHz the LTC1273/LTC1275/LTC1276 maintain very good ENOBs up to the Nyquist input frequency of 150kHz. Refer to Figure 3.

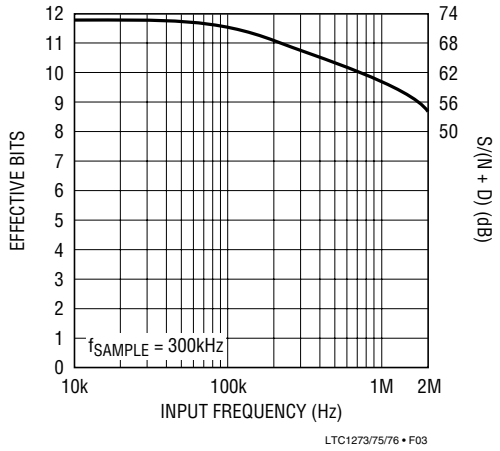

Figure 3. Effective Bits and Signal to (Noise + Distortion) vs Input Frequency

Total Harmonic Distortion

Total Harmonic Distortion (THD) is the ratio of the RMS sum of all harmonics of the input signal to the fundamental itself. The out-of-band harmonics alias into the frequency band between DC and half the sampling frequency. THD is expressed as:

$$THD = 20\log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 \ldots + V_N^2}}{V_1}$$

where V_1 is the RMS amplitude of the fundamental frequency and V_2 through V_N are the amplitudes of the second through Nth harmonics. THD versus input frequency is shown in Figure 4. The LTC1273/LTC1275/LTC1276 have good distortion performance up to Nyquist and beyond.

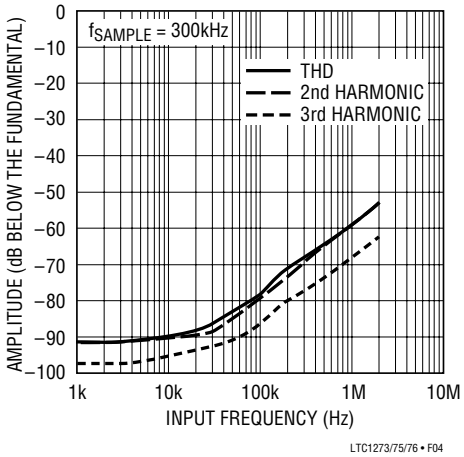

Figure 4. Distortion vs Input Frequency

Intermodulation Distortion

If the ADC input signal consists of more than one spectral component, the ADC transfer function nonlinearity can produce intermodulation distortion (IMD) in addition to THD. IMD is the change in one sinusoidal input caused by the presence of another sinusoidal input at a different frequency.

If two pure sine waves of frequencies fa and fb are applied to the ADC input, nonlinearities in the ADC transfer function can create distortion products at sum and difference frequencies of mfa ± nfb, where m and n = 0, 1, 2, 3, etc. For example, the 2nd order IMD terms include (fa + fb) and (fa – fb) while the 3rd order IMD terms include (2fa + fb), (2fa – fb), (fa + 2fb), and (fa – 2fb). If the two input sine waves are equal in magnitude, the value (in decibels) of the 2nd order IMD products can be expressed by the following formula:

$$IMD\ (fa \pm fb) = 20\log \frac{\text{Amplitude at } (fa \pm fb)}{\text{Amplitude at fa}}$$

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Figure 5 shows the IMD performance at a 30kHz input.

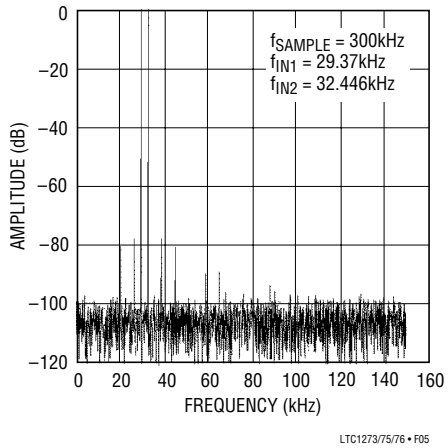

Figure 5. Intermodulation Distortion Plot

Peak Harmonic or Spurious Noise

The peak harmonic or spurious noise is the largest spectral component excluding the input signal and DC. This value is expressed in decibels relative to the RMS value of a full scale input signal.

Full Power and Full Linear Bandwidth

The full power bandwidth is that input frequency at which the amplitude of the reconstructed fundamental is reduced by 3dB for a full scale input signal.

The full linear bandwidth is the input frequency at which the S/(N + D) has dropped to 68dB (11 effective bits). The LTC1273/LTC1275/LTC1276 have been designed to optimize input bandwidth, allowing ADCs to undersample input signals with frequencies above the converters' Nyquist Frequency. The noise floor stays very low at high frequencies; S/(N + D) becomes dominated by distortion at frequencies far beyond Nyquist.

Driving the Analog Input

The analog inputs of the LTC1273/LTC1275/LTC1276 are easy to drive. They draw only one small current spike while charging the sample-and-hold capacitor at the end of conversion. During conversion the analog input draws no current. The only requirement is that the amplifier driving the analog input must settle after the small current spike before the next conversion starts. Any op amp that settles in 600ns to small current transients will allow maximum speed operation. If slower op amps are used, more settling time can be provided by increasing the time between conversions. Suitable devices capable of driving the ADCs' A_{IN} input include the LT1190/LT1191, LT1007, LT1220, LT1223 and LT1224 op amps.

The analog input tolerates source resistance very well. Here again, the only requirement is that the analog input must settle before the next conversion starts. For larger source resistance, full DC accuracy can be obtained if more time is allowed between conversions. For more information, see the Acquisition Time vs Source Resistance curve in the Typical Performance Characteristics section. For optimum frequency domain performance [e.g., S/(N + D)], keep the source resistance below 100Ω.

Internal Reference

The LTC1273/LTC1275/LTC1276 have an on-chip, temperature compensated, curvature corrected, bandgap reference which is factory trimmed to 2.42V. It is internally connected to the DAC and is available at pin 2 to provide up to 1mA current to an external load.

For minimum code transition noise the reference output should be decoupled with a capacitor to filter wideband noise from the reference (10µF tantalum in parallel with a 0.1µF ceramic).

In the LTC1275, the V_{REF} pin can be driven above its normal value with a DAC or other means to provide input span adjustment or to improve the reference temperature drift. Figure 6 shows an LT1006 op amp driving the

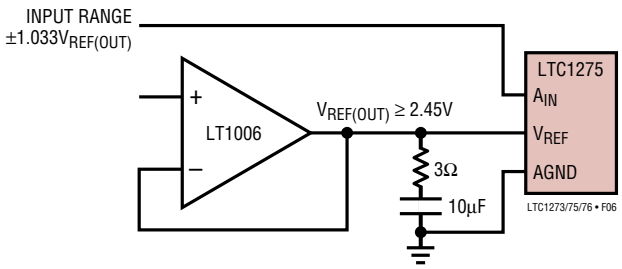

Figure 6. Driving the V_{REF} with the LT1006 Op Amp

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reference pin. The V_{REF} pin must be driven to at least 2.45V to prevent conflict with the internal reference. The reference should be driven to no more than 4.8V to keep the input span within the ±5V supplies. In the LTC1273/LT1276, the input spans are 0V to 5V and ±5V respectively with the internal reference. Driving the reference is not recommended on the LTC1273/LTC1276 since the input spans will exceed the supplies and codes will be lost at full scale.

Figure 7 shows a typical reference, the LT1019A-2.5 connected to the LTC1275. This will provide an improved drift (equal to the maximum 5ppm/°C of the LT1019A-2.5) and a ±2.582V full scale.

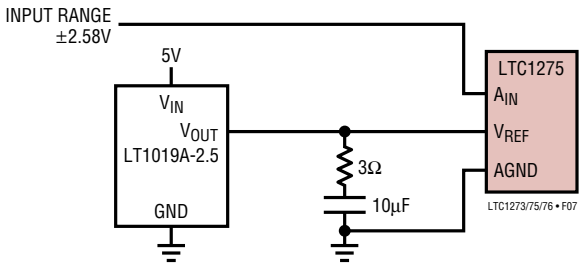

Figure 7. Supplying a 2.5V Reference Voltage to the LTC1275 with the LT1019A-2.5

UNIPOLAR/BIPOLAR OPERATION AND ADJUSTMENT

Figure 8 shows the ideal input/output characteristics for the LTC1273. The code transitions occur midway between successive integer LSB values (i.e., 1/2LSB, 1 1/2LSBs, 2 1/2LSBs, ... FS – 1 1/2LSBs). The output code is natural binary with 1LSB = FS/4096 = 5V/4096 = 1.22mV. Figure 9 shows the input/output transfer characteristics for the LTC1275/LTC1276 in 2's complement format. As stated in the figure, 1LSB for LTC1275/LTC1276 are 1.22mV and 2.44mV respectively.

Unipolar Offset and Full Scale Adjustment (LTC1273)

In applications where absolute accuracy is important, offset and full scale errors can be adjusted to zero. Figure 10a shows the extra components required for full scale error adjustment. If both offset and full scale adjustments are needed, the circuit in Figure 10b can be used. Offset

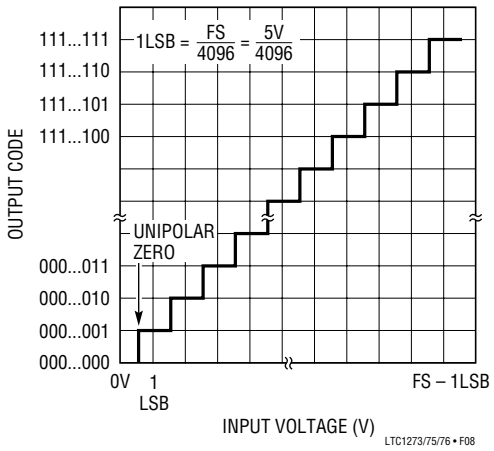

Figure 8. LTC1273 Unipolar Transfer Characteristic

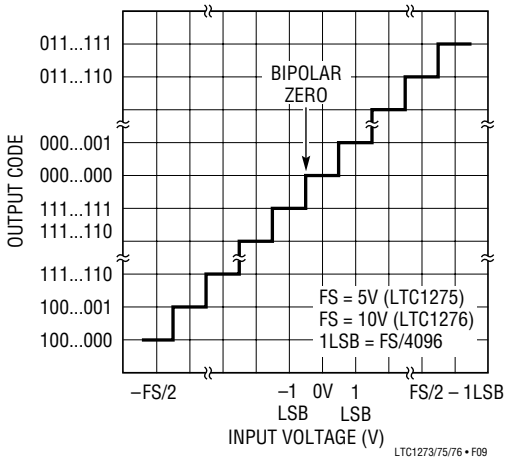

Figure 9. LTC1275/LTC1276 Bipolar Transfer Characteristic

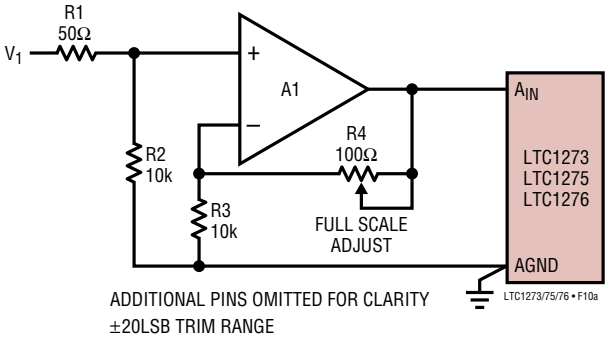

Figure 10a. Full Scale Adjust Circuit

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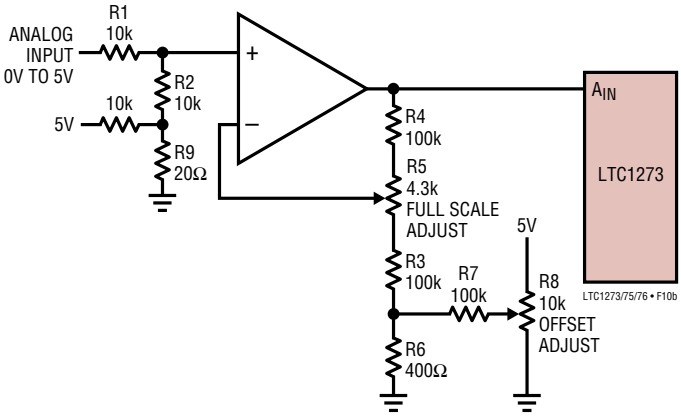

Figure 10b. LTC1273 Offset and Full Scale Adjust Circuit

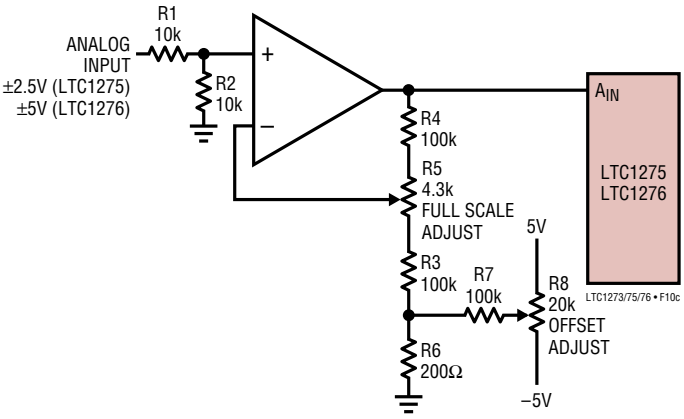

Figure 10c. LTC1275/LTC1276 Offset and Full Scale Adjust Circuit

should be adjusted before full scale. To adjust offset, apply 0.61mV (i.e., 1/2LSB) at the input and adjust the offset trim until the LTC1273 output code flickers between 0000 0000 0000 and 0000 0000 0001. To adjust full scale, apply an analog input of 4.99817V (i.e., FS – 1 1/2LSBs or last code transition) at the input and adjust the full scale trim until the LTC1273 output code flickers between 1111 1111 1110 and 1111 1111 1111. It should be noted that if negative ADC offsets need to be adjusted or if an output swing to ground is required, the op amp in Figure 10b requires a negative power supply.

Bipolar Offset and Full Scale Adjustment (LTC1275/LTC1276)

Bipolar offset and full scale errors are adjusted in a similar fashion to the unipolar case. Figure 10a shows the extra components required for full scale error adjustment. If both offset and full scale adjustments are needed, the circuit in Figure 10c can be used. Again, bipolar offset must be adjusted before full scale error. Bipolar offset adjustment is achieved by trimming the offset adjustment of Figure 10c while the input voltage is 1/2LSB below ground. This is done by applying an input voltage of –0.61mV or –1.22mV (–0.5LSB for LTC1275 or LTC1276) to the input in Figure 10c and adjusting R8 until the ADC output code flickers between 0000 0000 0000 and 1111 1111 1111. For full scale adjustment, an input voltage of 2.49817V or 4.99636V (FS – 1 1/2LSBs for LTC1275 or LTC1276) is applied to the input and R5 is adjusted until the output code flickers between 0111 1111 1110 and 0111 1111 1111.

BOARD LAYOUT AND BYPASSING

The LTC1273/LTC1275/LTC1276 are easy to use. To obtain the best performance from the devices a printed circuit board is required. Layout for the printed circuit board should ensure that digital and analog signal lines are separated as much as possible. In particular, care should be taken not to run any digital track alongside an analog signal track. The analog input should be screened by AGND.

High quality tantalum and ceramic bypass capacitors should be used at the V_{DD} and V_{REF} pins as shown in Figure 11. For the LTC1275/LTC1276 a 0.1µF ceramic provides adequate bypassing for the V_{SS} pin. The capacitors must be located as close to the pins as possible. The traces connecting the pins and the bypass capacitors must be kept short and should be made as wide as possible.

Noise: Input signal leads to A_{IN} and signal return leads from AGND (Pin 3) should be kept as short as possible to minimize input noise coupling. In applications where this is not possible, a shielded cable between source and ADC is recommended. Also, since any potential difference in grounds between the signal source and ADC appears as an

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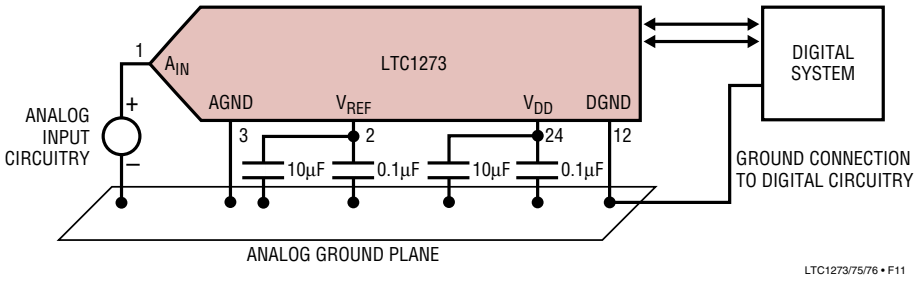

Figure 11. Power Supply Grounding Practice

error voltage in series with the input signal, attention should be paid to reducing the ground circuit impedances as much as possible.

A single point analog ground plane separate from the logic system ground should be established at Pin 3 (AGND) or as close as possible to the ADC, as shown in Figure 11. Pin 12 (DGND) and all other analog grounds should be connected to this single analog ground point. No other digital grounds should be connected to this analog ground point. Low impedance analog and digital power supply common returns are essential to low noise operation of the ADC and the width for these traces should be as wide as possible.

In applications where the ADC data outputs and control signals are connected to a continuously active microprocessor bus, it is possible to get errors in conversion results. These errors are due to feedthrough from the microprocessor to the ADC. The problem can be eliminated by forcing the microprocessor into a WAIT state during conversion or by using three-state buffers to isolate the ADC data bus.

DIGITAL INTERFACE

The ADCs are designed to interface with microprocessors as a memory mapped device. The $\overline{CS}$ and $\overline{RD}$ control inputs are common to all peripheral memory interfacing. The HBEN input serves as a data byte select for 8-bit processors and is normally either connected to the microprocessor address bus or grounded.

Internal Clock

These ADCs have an internal clock that eliminates the need for synchronization between an external clock and the $\overline{CS}$ and $\overline{RD}$ signals found in other ADCs. The internal clock is factory trimmed to achieve a typical conversion time of 2.45µs, and a maximum conversion time over the full operating temperature range of 2.7µs. No external adjustments are required and, with the guaranteed maximum acquisition time of 600ns, throughput performance of 300ksps is assured.

Timing and Control

Conversion start and data read operations are controlled by three digital inputs: HBEN, $\overline{CS}$ and $\overline{RD}$. Figure 12 shows the logic structure associated with these inputs. The three signals are internally gated so that a logic “0” is required

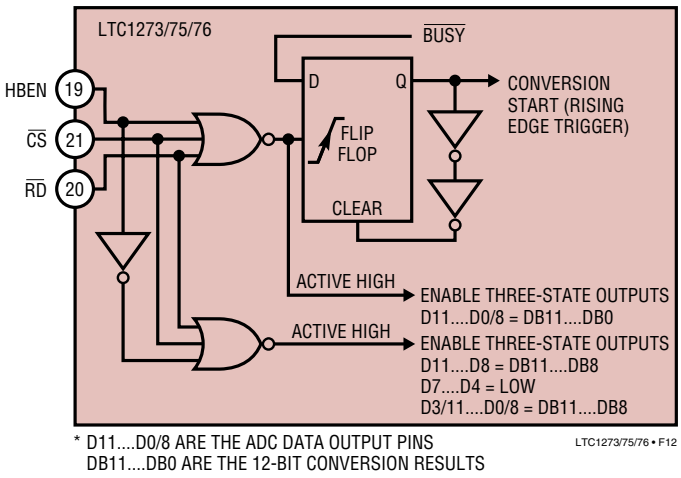

Figure 12. Internal Logic for Control Inputs $\overline{CS}$, $\overline{RD}$ and HBEN

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on all three inputs to initiate a conversion. Once initiated it cannot be restarted until the conversion is complete. Converter status is indicated by the $\overline{BUSY}$ output, and this is low while conversion is in progress.

There are two modes of operation as outlined by the timing diagrams of Figures 13 to 16. Slow Memory Mode is designed for microprocessors which can be driven into a WAIT state. A READ operation brings $\overline{CS}$ and $\overline{RD}$ low which initiates a conversion and data is read when conversion is complete. The second is the ROM Mode which does not require microprocessor WAIT states. A READ operation brings $\overline{CS}$ and $\overline{RD}$ low which initiates a conversion and reads the previous conversion result.

Data Format

The output format can be either a complete parallel load for 16-bit microprocessors or a two byte load for 8-bit microprocessors. Data is always right justified (i.e., LSB is the most right-hand bit in a 16-bit word). For a two byte read, only data outputs D7...D0/8 are used. Byte selection is governed by the HBEN input which controls an internal digital multiplexer. This multiplexes the 12-bits of conversion data onto the lower D7...D0/8 outputs (4MSBs or 8MSBs) where it can be read in two read cycles. The 4MSBs always appear on D11...D8 whenever the three-state output drivers are turned on.

Slow Memory Mode, Parallel Read (HBEN = LOW)

Figure 13 and Table 2 show the timing diagram and data bus status for Slow Memory Mode, Parallel Read. $\overline{CS}$ and $\overline{RD}$ going low trigger a conversion and the ADC acknowledges by taking $\overline{BUSY}$ low. Data from the previous conversion appears on the three-state data outputs. $\overline{BUSY}$ returns high at the end of conversion when the output latches have been updated and the conversion result is placed on data outputs D11...D0/8.

Slow Memory Mode, Two Byte Read

For a two byte read, only 8 data outputs D7...D0/8 are used. Conversion start procedure and data output status for the first read operation are identical to Slow Memory Mode, Parallel Read. See Figure 14 timing diagram and Table 3 data bus status. At the end of the conversion, the low data byte (D7...D0/8) is read from the ADC. A second READ operation, with the HBEN high, places the high byte on data outputs D3/11...D0/8 and disables conversion start. Note

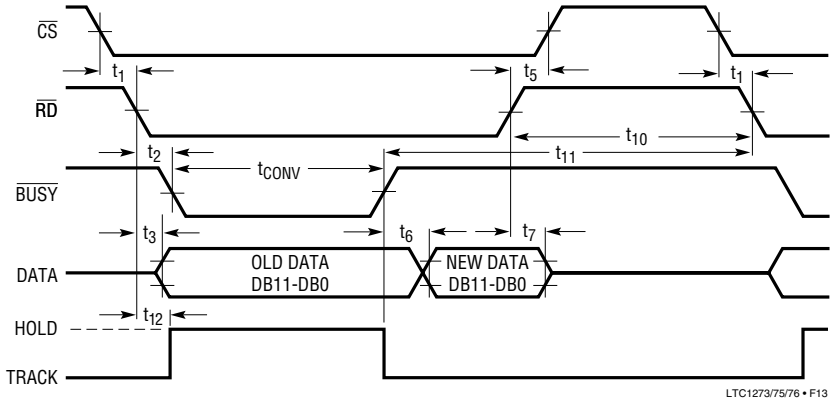


Figure 13. Slow Memory Mode, Parallel Read Timing Diagram

Table 2. Slow Memory Mode, Parallel Read Data Bus Status

Data Outputs	D11	D10	D9	D8	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
Read	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

APPLICATIONS INFORMATION

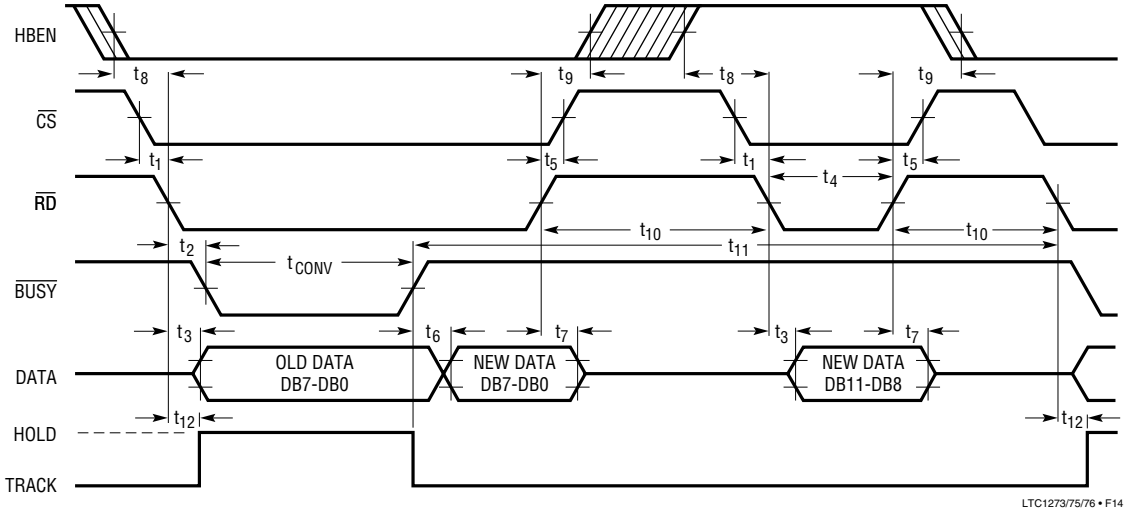


Figure 14. Slow Memory Mode, Two Byte Read Timing Diagram

Table 3. Slow Memory Mode, Two Byte Read Data Bus Status

Data Outputs	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
First Read	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Second Read	Low	Low	Low	Low	DB11	DB10	DB9	DB8

that the 4MSBs appear on data output D11...D8 during both READ operations.

ROM Mode, Parallel Read (HBEN = LOW)

The ROM Mode avoids placing a microprocessor into a WAIT state. A conversion is started with a READ operation, and the 12 bits of data from the previous conversion are available on data outputs D11...D0/8 (see Figure 15 and Table 4). This data may be disregarded if not required. A second READ operation reads the new data (DB11...DB0) and starts another conversion. A delay at least as long as the ADC's conversion time plus the 600ns minimum delay between conversions must be allowed between READ operations.

ROM Mode, Two Byte Read

As previously mentioned for a two byte read, only data outputs D7...D0/8 are used. Conversion is started in the normal way with a READ operation and the data output status is the same as the ROM mode, Parallel Read (see Figure 16 timing diagram and Table 5 data bus status). Two more READ operations are required to access the new conversion result. A delay equal at the ADCs' conversion time must be allowed between conversion start and the third data READ operation. The second READ operation with HBEN high disables conversion start and places the high byte (4MSBs) on data outputs D3/11...D0/8. A third read operation accesses the low data byte (DB7...DB0) and starts another conversion. The 4MSBs appear on data outputs D11...D8 during all three read operations.

MICROPROCESSOR INTERFACING

The LTC1273/LTC1275/LTC1276 allow easy interfacing to digital signal processors as well as modern high speed, 8-bit or 16-bit microprocessors. Here are several examples.

APPLICATIONS INFORMATION

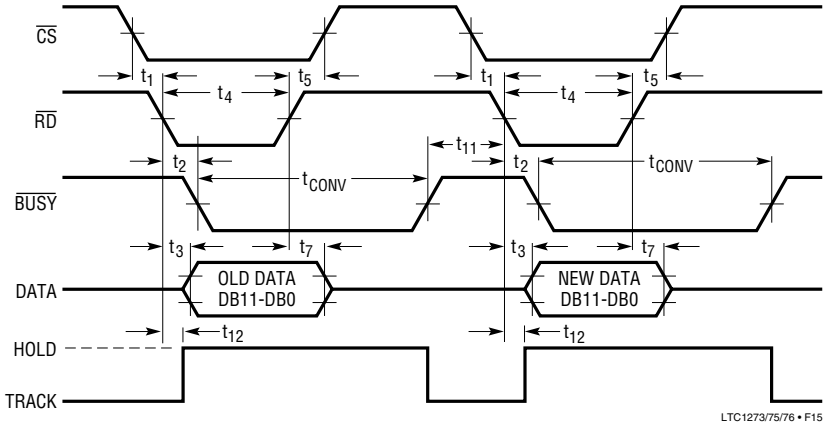


Figure 15. ROM Mode, Parallel Read Timing Diagram (HBEN = LOW)

Table 4. ROM Mode, Parallel Read Data Bus Status

Data Outputs	D11	D10	D9	D8	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
First Read (Old Data)	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Second Read	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

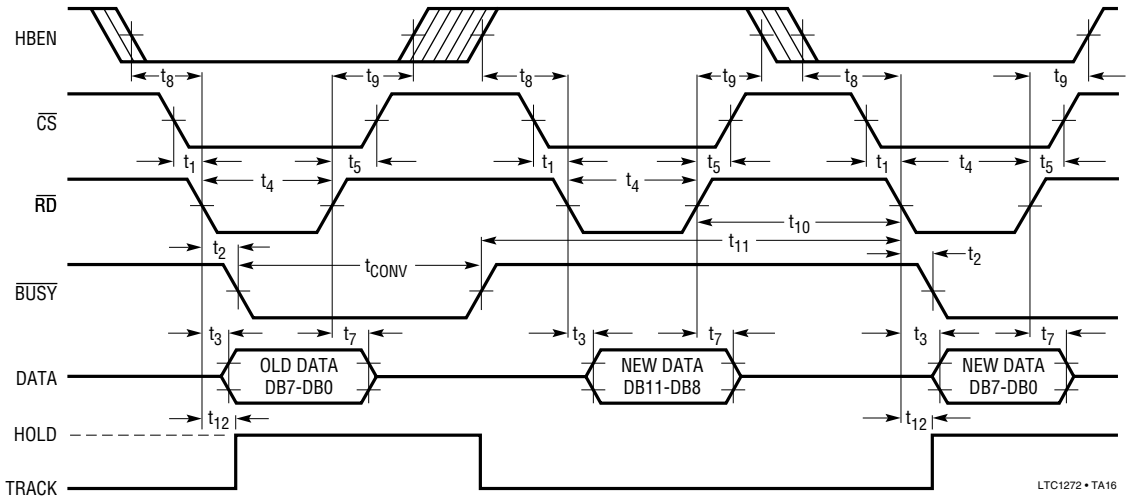


Figure 16. ROM Mode Two Byte Read Timing Diagram

Table 5. ROM Mode, Two Byte Read Data Bus Status

Data Outputs	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
First Read (Old Data)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Second Read (New Data)	Low	Low	Low	Low	DB11	DB10	DB9	DB8
Third Read (New Data)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

APPLICATIONS INFORMATION

TMS320C25

Figure 17 shows an interface between the LTC1273 and the TMS320C25.

The W/$\overline{R}$ signal of the DSP initiates a conversion and conversion results are read from the LTC1273 using the following instruction:

IN D, PA

where D is Data Memory Address and PA is the PORT ADDRESS.

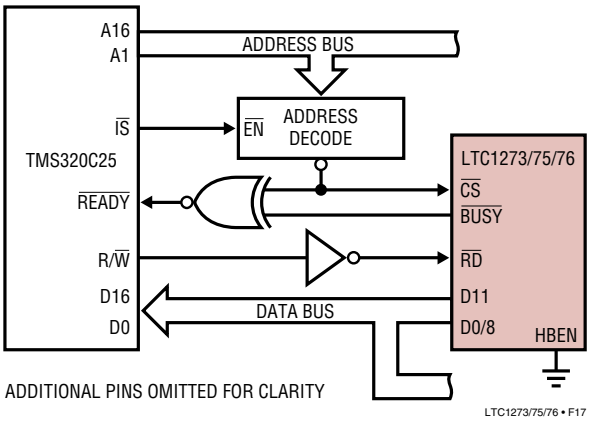


Figure 17. TMS320C25 Interface

MC68000 Microprocessor

Figure 18 shows a typical interface for the MC68000. The LTC1273 is operating in the Slow Memory Mode. Assuming the LTC1273 is located at address C000, then the following single 16-bit MOVE instruction both starts a conversion and reads the conversion result:

Move.W $C000,D0

At the beginning of the instruction cycle when the ADC address is selected, $\overline{BUSY}$ and $\overline{CS}$ assert $\overline{DTACK}$ so that the MC68000 is forced into a WAIT state. At the end of conversion, $\overline{BUSY}$ returns high and the conversion result is placed in the D0 register of the microprocessor.

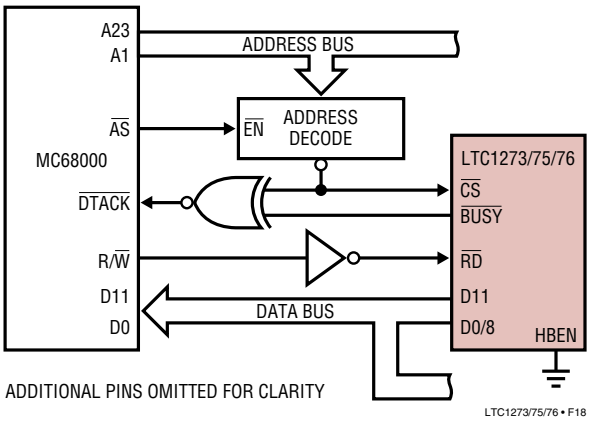


Figure 18. MC68000 Interface

8085A/Z80 Microprocessor

Figure 19 shows an LTC1273 interface for the Z80/8085A. The LTC1273 is operating in the Slow Memory Mode and a two byte read is required. Not shown in the figure is the 8-bit latch required to demultiplex the 8085A common address/data bus. A0 is used to assert HBEN so that an even address (HBEN = LOW) to the LTC1273 will start a conversion and read the low data byte. An odd address (HBEN = HIGH) will read the high data byte. This is accomplished with the single 16-bit LOAD instruction below.

For the 8085A	LHLD (B000)
For the Z80	LDHL, (B000)

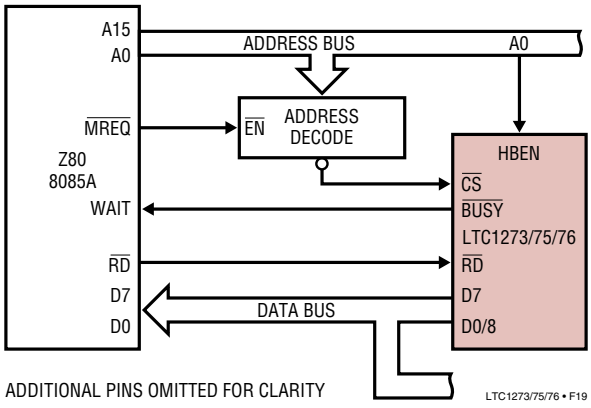


Figure 19. 8085A and Z80 Interface

APPLICATIONS INFORMATION

This is a two byte read instruction which loads the ADC data (address B000) into the HL register pair. During the first read operation, $\overline{BUSY}$ forces the microprocessor to WAIT for the LTC1273 conversion. No WAIT states are inserted during the second read operation when the microprocessor is reading the high data byte.

TMS32010 Microcomputer

Figure 20 shows an LTC1273/TMS32010 interface. The LTC1273 is operating in the ROM Mode.

The LTC1273 is mapped at a port address. The following I/O instruction starts a conversion and reads the previous conversion result into data memory.

IN A,PA (PA = PORT ADDRESS)

When conversion is complete, a second I/O instruction reads the up-to-date data into memory and starts another conversion. A delay at least as long as the ADC conversion time must be allowed between I/O instructions.

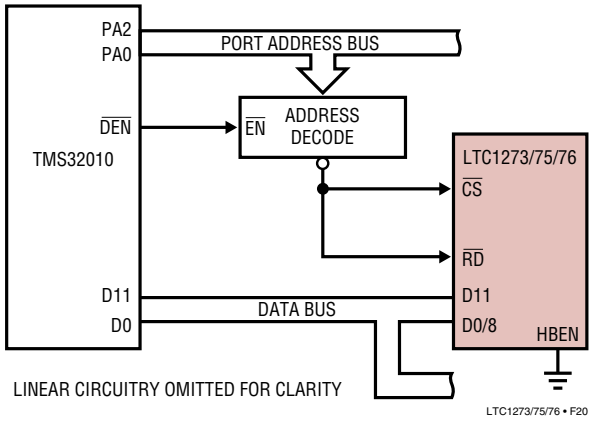


Figure 20. TMS32010 Interface

MUXing with CD4051

The high input impedance of the LTC1273/LTC1275/LTC1276 provides an easy, cheap, fast, and accurate way to multiplex many channels of data through one converter. Figure 21 shows a low cost CD4051 connected to the LTC1275. The LTC1275's input draws no DC input current so it can be accurately driven by the unbuffered MUX. The CD4520 counter increments the MUX channel after each sample is taken. Figure 22 shows the acquisition time of LTC1275 vs the source resistance. For a 500Ω maximum "on" resistance of the CD4051, the acquisition time of the ADC is not greatly affected. For larger source resistances, modest increases in acquisition time must be allowed.

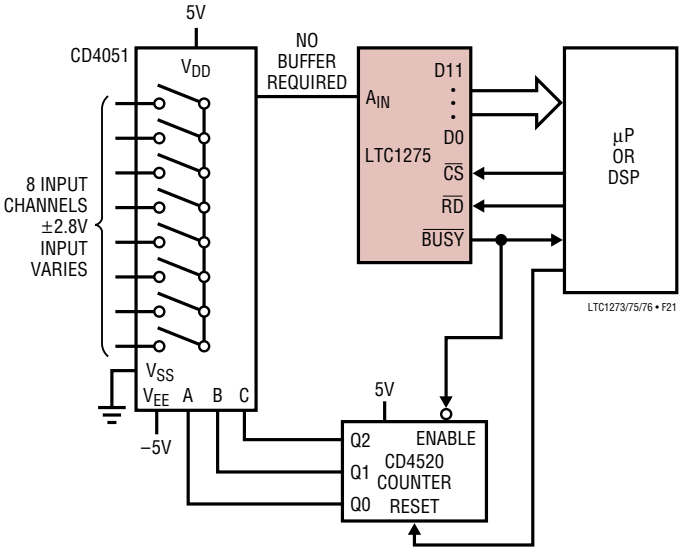


Figure 21. MUXing the LTC1275 with CD4051

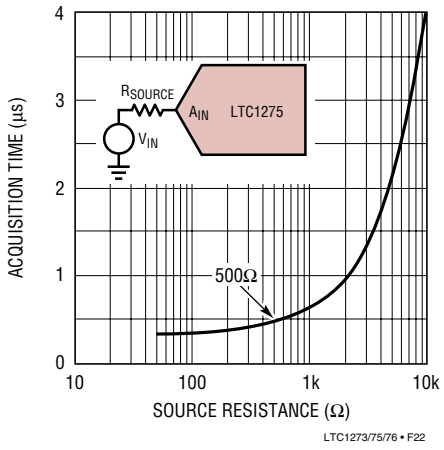


Figure 22. Acqusition Time of LTC1275 vs Source Resistance

APPLICATIONS INFORMATION

Demodulating a Signal by Undersampling with LTC1275

Figure 23 shows a 455kHz amplitude modulated input undersampled by the LTC1275. With a 227.5kHz sample rate, the converter provides a 100dB noise floor and 68dB distortion when digitizing the 455kHz AM input.

Figure 24 shows an FFT of the AM signal digitized at 212.5kHz.

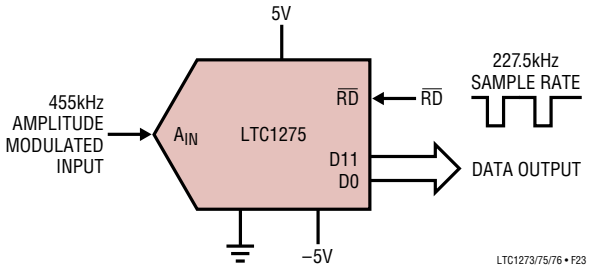


Figure 23. A 455kHz Amplitude Modulated Input Undersampled by the LTC1275

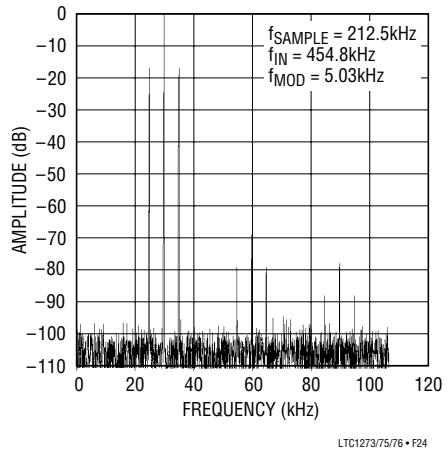


Figure 24. 455kHz Input Voltage Modulated by a 5kHz Signal

A time domain view of the demodulation is shown in Figure 25. The top trace shows the 455kHz waveform modulated by a –6dB, 5kHz signal. The bottom trace shows the demodulated signal produced by the LTC1275 reconstructed through a 12-bit DAC. The resultant frequency is 5kHz with a sample rate of 227.5kHz. There are roughly 45 points per cycle.

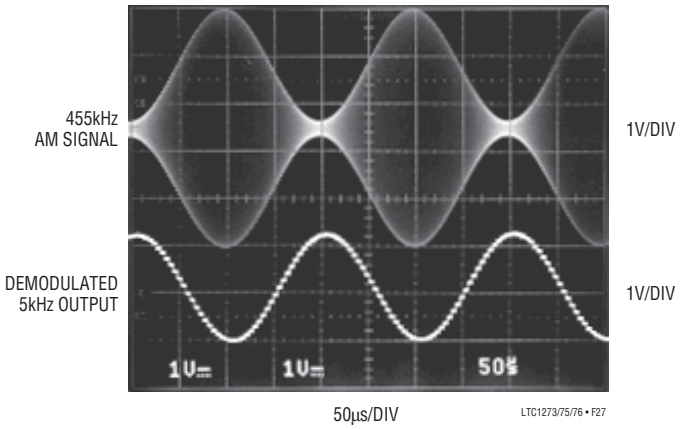


Figure 25. 455kHz AM Signal Demodulated to 10.5 ENOBs

100ps Resolution ΔTime Measurement with LTC1273

Figure 26 shows a circuit that precisely measures the difference in time between two events. It has a 400ns full scale and 100ps resolution. The start signal releases the ramp generator made up of the PNP current source and the 250pF capacitor. The circuit ramps until the stop signal shuts off the current source. The final value of the ramp represents the time between the start and stop events. The LTC1273 digitizes this final value and outputs the digital data.

APPLICATIONS INFORMATION

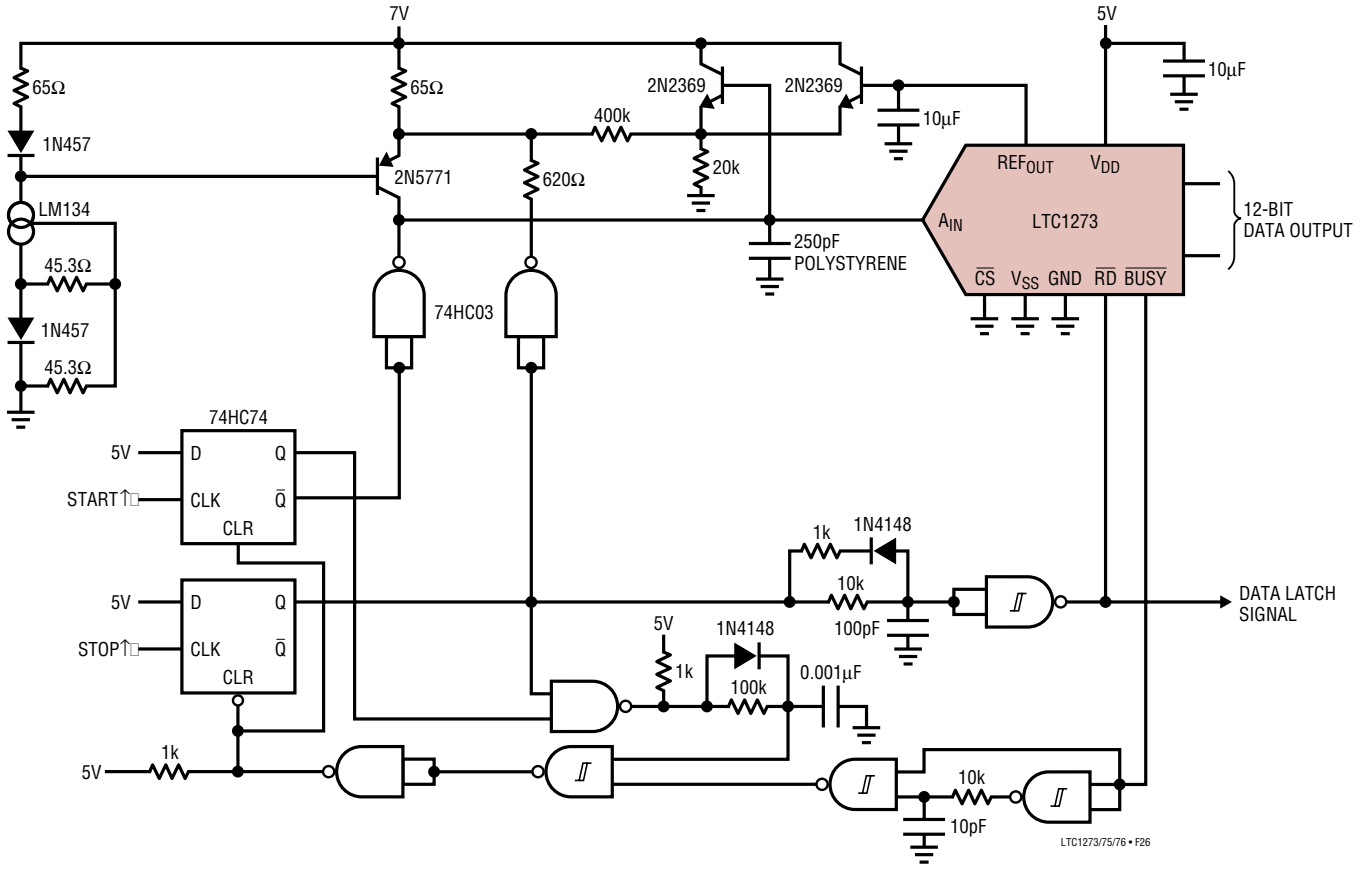
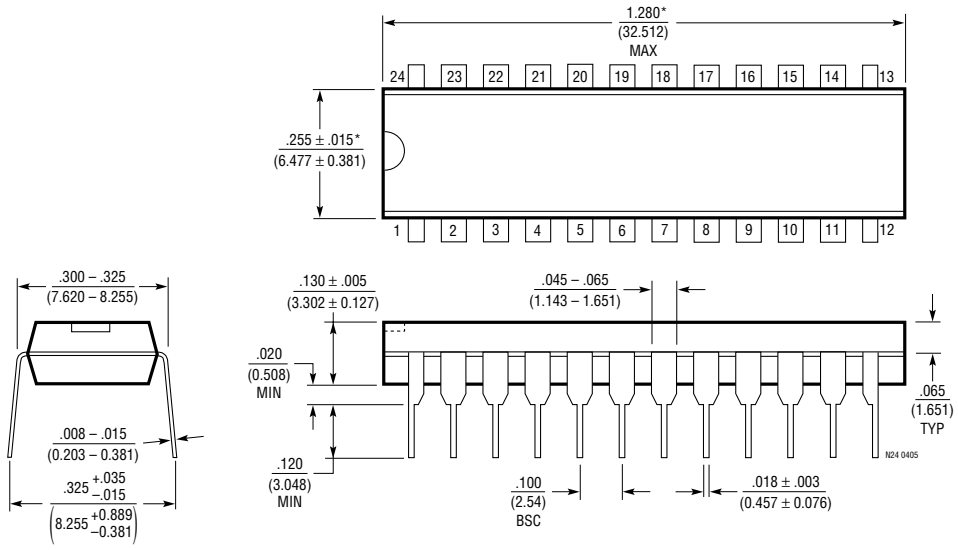


Figure 26. ΔTime Measurement with the LTC1273

PACKAGE DESCRIPTION

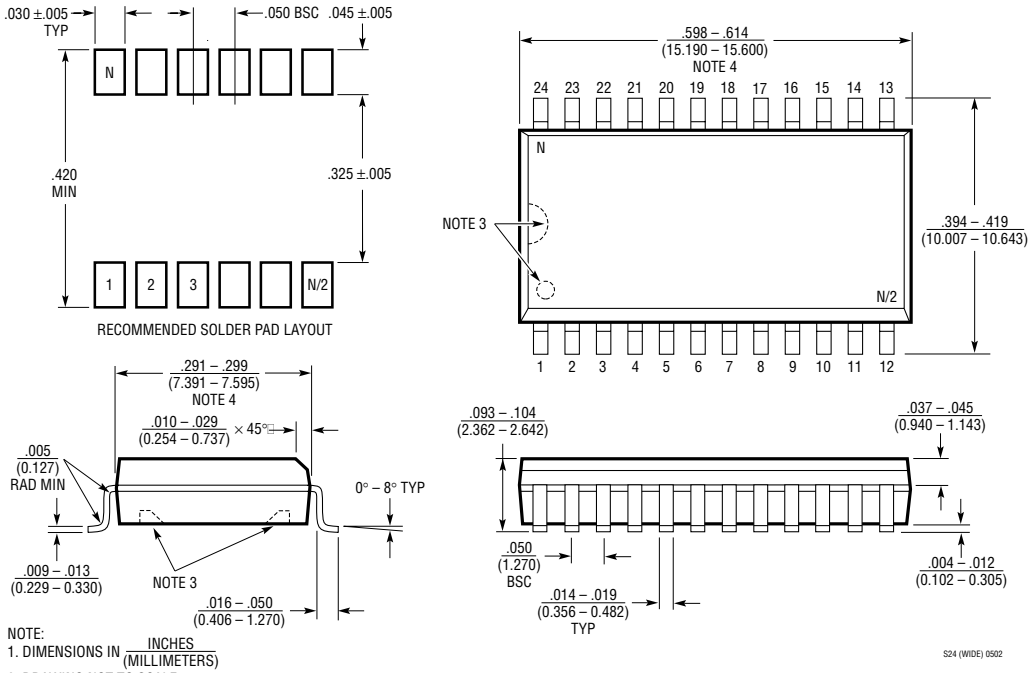
N Package
24-Lead PDIP (Narrow .300 Inch)
(Reference LTC DWG # 05-08-1510)



NOTE:
1. DIMENSIONS ARE INCHES / MILLIMETERS

*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.254mm)

SW Package
24-Lead Plastic Small Outline (Wide .300 Inch)
(Reference LTC DWG # 05-08-1620)



NOTE:
1. DIMENSIONS IN INCHES / (MILLIMETERS)
2. DRAWING NOT TO SCALE
3. PIN 1 IDENT, NOTCH ON TOP AND CAVITIES ON THE BOTTOM OF PACKAGES ARE THE MANUFACTURING OPTIONS.
THE PART MAY BE SUPPLIED WITH OR WITHOUT ANY OF THE OPTIONS
4. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

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