Software-Selectable Multiprotocol Transceiver

FEATURES

- **Software-Selectable Transceiver Supports: RS232, RS449, EIA-530, EIA-530-A, V.35, V.36, X.21**
- **NET1 and NET2 Compliant**
- Software-Selectable Cable Termination Using the LTC1344
- 4-Driver/4-Receiver Configuration Provides a Complete 2-Chip DTE or DCE Port
- Operates from Single 5V Supply
- Internal Echoed Clock and Loop-Back Logic

APPLICATIONS

- Data Networking
- CSU and DSU
- Data Routers

DESCRIPTION

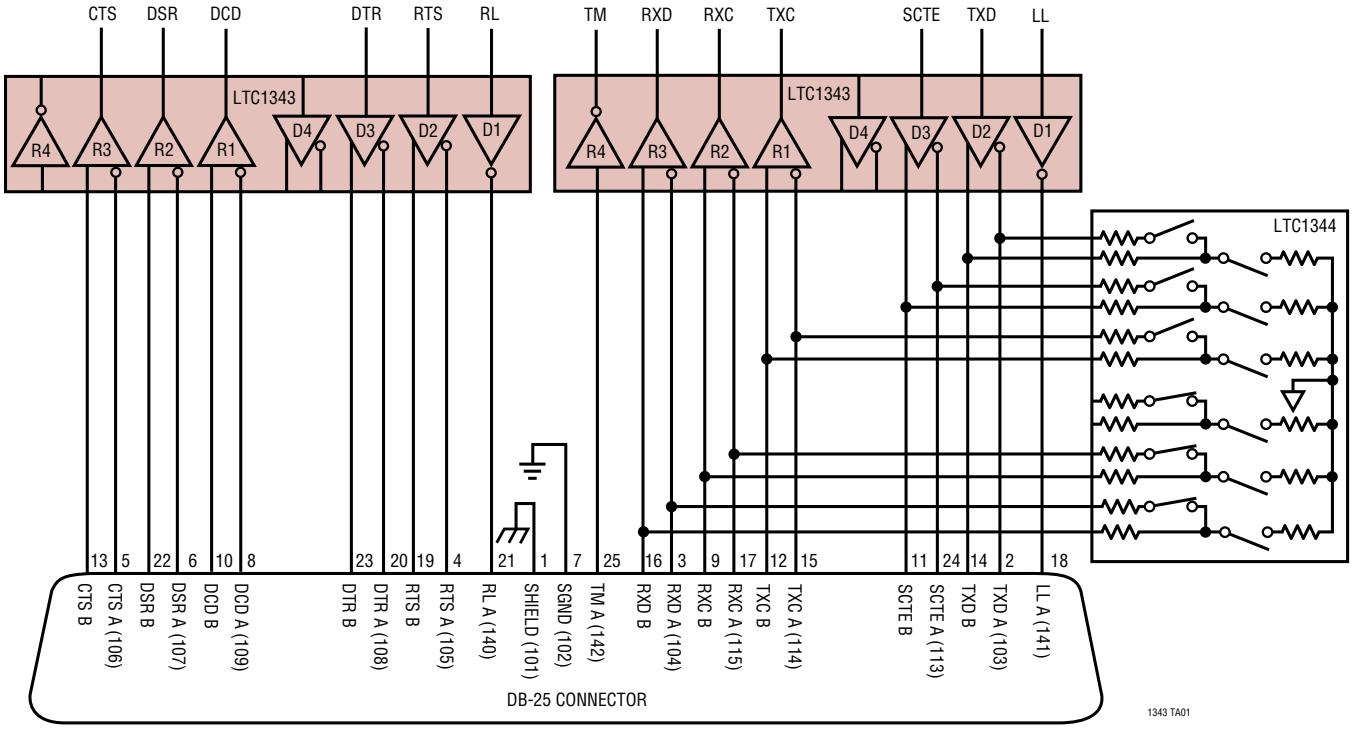
The LTC®1343 is a 4-driver/4-receiver multiprotocol transceiver that operates from a single 5V supply. Two LTC1343s form the core of a complete software-selectable DTE or DCE interface port that supports the RS232, RS449, EIA-530, EIA-530-A, V.35, V.36 or X.21 protocols. Cable termination may be implemented using the LTC1344 software-selectable cable termination chip or by using existing discrete designs.

The LTC1343 runs from a single 5V supply using an internal charge pump that requires only five space saving surface mount capacitors. The mode pins are latched internally to allow sharing of the select lines between multiple interface ports.

Software-selectable echoed clock and loop-back modes help eliminate the need for external glue logic between the serial controller and line transceiver. The part features a flow-through architecture to simplify EMI shielding and is available in the 44-lead SSOP surface mount package.

TYPICAL APPLICATION

DTE Multiprotocol Serial Interface with DB-25 Connector



ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage 6.5V

Input Voltage

- Transmitters ..... −0.3V to (V_{CC} + 0.3V)
- Receivers ..... −18V to 18V
- Logic Pins ..... −0.3V to (V_{CC} + 0.3V)

Output Voltage

- Transmitters ..... (V_{EE} − 0.3V) to (V_{DD} + 0.3V)
- Receivers ..... −0.3V to (V_{CC} + 0.3V)
- Logic Pins ..... −0.3V to (V_{CC} + 0.3V)
- V_{EE} ..... −10V to 0.3V
- V_{DD} ..... −0.3V to 10V

Short-Circuit Duration

- Transmitter Output ..... Indefinite
- Receiver Output ..... Indefinite
- V_{EE} ..... 30 sec

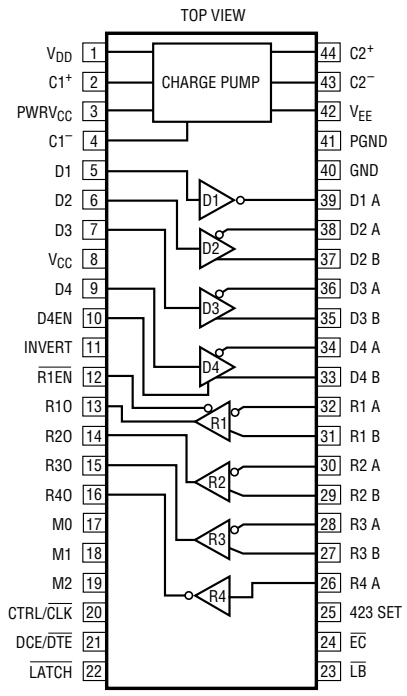
Operating Temperature Range

- LTC1343C ..... 0°C to 70°C
- LTC1343I ..... −40°C to 85°C

Storage Temperature Range ..... −65°C to 150°C

Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



GW PACKAGE
44-LEAD PLASTIC SSOP

T_{JMAX} = 150°C, θ_{JA} = 65°C/W

ORDER PART NUMBER
LTC1343CGW LTC1343IGW

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 5V (Notes 2, 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supplies							
I_{CC}	V_{CC} Supply Current (DCE Mode, All Digital Pins = GND or V_{CC})	V.10 Mode, No Load			12		mA
		V.10 Mode, Full Load	●		80	150	mA
		RS530, RS530-A, X.21 Modes, No Load			80		mA
		RS530, RS530-A, X.21 Modes, Full Load	●		160	200	mA
		V.35 Mode, No Load			20		mA
		V.35 Mode, Full Load	●		115	160	mA
		V.28 Mode, No Load			20		mA
		V.28 Mode, Full Load	●		30	90	mA
		No-Cable Mode	●		0.05	1	mA
P_D	Internal Power Dissipation (DCE Mode, All Digital Pins = GND or V_{CC})	V.10 Mode, Full Load			400		mW
		RS530, RS530-A, X.21 Modes, Full Load			680		mW
		V.35 Mode, Full Load			500		mW
		V.28 Mode, Full Load			150		mW
V^+	Positive Charge Pump Output Voltage	Any Mode, No Load	●	8.5	9.1		V
		V.28 Mode, with Load	●	8.0	7.0		V
V^-	Negative Charge Pump Output Voltage	V.28 Mode, Full Load	●	−7.8	−8.4		V
		V.35 Mode, Full Load	●	−5.8	−6.7		V
		−40°C ≤ T_A ≤ 85°C	●	−5.5			V
		V.10, RS530, RS530A, X.21 Modes, Full Load	●	−5.0	−6.1		V
		−40°C ≤ T_A ≤ 85°C	●	−4.8			V

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 5V (Notes 2, 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_r	Supply Rise Time	No-Cable Mode or Power-Up to Turn On			2		ms
Logic Inputs and Outputs							
V_{IH}	Logic Input High Voltage		●	2			V
V_{IL}	Logic Input Low Voltage		●			0.8	V
I_{IN}	Logic Input Current		●			±10	µA
V_{OH}	Output High Voltage	I_O = –4mA	●	3	4.5		V
V_{OL}	Output Low Voltage	I_O = 4mA	●		0.3	0.8	V
I_{OSR}	Output Short-Circuit Current	0V ≤ V_O ≤ V_{CC}, 0°C ≤ T_A ≤ 70°C 0V ≤ V_O ≤ V_{CC}, –40°C ≤ T_A ≤ 85°C	● ●	–60 –70		60 70	mA mA
I_{OZR}	Three-State Output Current	M0 = M1 = M2 = V_{CC}, 0V ≤ V_O ≤ V_{CC}			±1		µA
V.11 Driver							
V_{OD}	Differential Output Voltage	Open Circuit, R_L = 1.95k R_L = 50Ω (Figure 1), V_{OD} at 50Ω > 1/2 V_{OD} at R_L = 1.95k	● ●	 ±2		±6	V V
ΔV_{OD}	Change in Magnitude of Differential Output Voltage	R_L = 50Ω (Figure 1)	●			0.2	V
V_{OC}	Common Mode Output Voltage	R_L = 50Ω (Figure 1)	●			3.0	V
ΔV_{OC}	Change in Magnitude of Common Mode Output Voltage	R_L = 50Ω (Figure 1)	●			0.2	V
I_{SS}	Short-Circuit Current	–0.25V ≤ V_O ≤ 0.25V, Power Off or No-Cable Mode or Driver Disabled				±150	mA
I_{OZ}	Output Leakage Current	–0.25V ≤ V_O ≤ 0.25V, Power Off or No-Cable Mode or Driver Disabled	●		±0.01	±100	µA
t_r, t_f	Rise or Fall Time	(Figures 2, 6)	●	4	13	25	ns
t_{PLH}	Input to Output	(Figures 2, 6), 0°C ≤ T_A ≤ 70°C (Figures 2, 6), –40°C ≤ T_A ≤ 85°C	● ●	25 25	55 55	80 90	ns ns
t_{PHL}	Input to Output	(Figures 2, 6), 0°C ≤ T_A ≤ 70°C (Figures 2, 6), –40°C ≤ T_A ≤ 85°C	● ●	25 25	55 55	80 90	ns ns
Δt	Input to Output Difference, $\lvert t_{PLH} - t_{PHL} \rvert$	(Figures 2, 6), 0°C ≤ T_A ≤ 70°C (Figures 2, 6), –40°C ≤ T_A ≤ 85°C	● ●	0 0	3 3	17 25	ns ns
t_{SKEW}	Output to Output Skew	(Figures 2, 6)			3		ns
V.11 Receiver							
V_{TH}	Input Threshold Voltage	–7V ≤ V_{CM} ≤ 7V, 0°C ≤ T_A ≤ 70°C –7V ≤ V_{CM} ≤ 7V, –40°C ≤ T_A ≤ 85°C	● ●	–0.2 –0.3		0.2 0.3	V V
ΔV_{TH}	Input Hysteresis	–7V ≤ V_{CM} ≤ 7V, 0°C ≤ T_A ≤ 70°C –7V ≤ V_{CM} ≤ 7V, –40°C ≤ T_A ≤ 85°C	● ●		15	40 60	mV mV
I_{IN}	Input Current (A, B)	–10V ≤ $V_{A, B}$ ≤ 10V	●			±0.50	mA
R_{IN}	Input Impedance	–10V ≤ $V_{A, B}$ ≤ 10V	●	20	32		kΩ
t_r, t_f	Rise or Fall Time	(Figures 2, 7)			15		ns
t_{PLH}	Input to Output	(Figures 2, 7), CTRL = GND, 0°C ≤ T_A ≤ 70°C CTRL = V_{CC}, 0°C ≤ T_A ≤ 70°C	●	35	80 400	115	ns ns
		(Figures 2, 7), CTRL = GND, –40°C ≤ T_A ≤ 85°C CTRL = V_{CC}, –40°C ≤ T_A ≤ 85°C	●	25	80 400	130	ns ns

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 5V (Notes 2, 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{PHL}	Input to Output	(Figures 2, 7), CTRL = GND, 0°C ≤ T_A ≤ 70°C CTRL = V_{CC}, 0°C ≤ T_A ≤ 70°C	● 	35	80 400	115	ns ns
		(Figures 2, 7), CTRL = GND, –40°C ≤ T_A ≤ 85°C CTRL = V_{CC}, –40°C ≤ T_A ≤ 85°C	● 	25	80 400	130	ns ns
Δt	Input to Output Difference, $\lvert t_{PLH} - t_{PHL} \rvert$	(Figures 2, 7), 0°C ≤ T_A ≤ 70°C (Figures 2, 7), –40°C ≤ T_A ≤ 85°C	● ●	0 0	5 5	17 25	ns ns
V.35 Driver							
V_{OD}	Differential Output Voltage	Open Circuit With Load, –4.0V ≤ V_{CM} = 4.0V (Figure 3)	 ●	 ±0.44	 ±0.55	6.0 ±0.66	V V
I_{OH}	Transmitter Output High Current	$V_{A, B}$ = 0V	●	–12.6	–11	–9.4	mA
I_{OL}	Transmitter Output Low Current	$V_{A, B}$ = 0V	●	9.4	11	12.6	mA
I_{OZ}	Transmitter Output Leakage Current	–0.25V ≤ $V_{A, B}$ ≤ 0.25V	●		±0.01	±100	µA
t_r, t_f	Rise or Fall Time	(Figures 3, 6)			5		ns
t_{PLH}	Input to Output	(Figures 3, 6), 0°C ≤ T_A ≤ 70°C (Figures 3, 6), –40°C ≤ T_A ≤ 85°C	● ●	25 25	45 45	75 90	ns ns
t_{PHL}	Input to Output	(Figures 3, 6), 0°C ≤ T_A ≤ 70°C (Figures 3, 6), –40°C ≤ T_A ≤ 85°C	● ●	25 25	45 45	75 90	ns ns
Δt	Input to Output Difference, $\lvert t_{PLH} - t_{PHL} \rvert$	(Figures 3, 6), 0°C ≤ T_A ≤ 70°C (Figures 3, 6), –40°C ≤ T_A ≤ 85°C	● ●	0 0	5 5	17 25	ns ns
t_{SKEW}	Output to Output Skew	(Figures 3, 6)			4		ns
V.35 Receiver							
V_{TH}	Differential Receiver Input Threshold Voltage	–2V ≤ (V_A + V_B)/2 ≤ 2V (Figure 3)	●	–0.2		0.2	V
ΔV_{TH}	Receiver Input Hysteresis	–2V ≤ (V_A + V_B)/2 ≤ 2V (Figure 3)	●		11	40	mV
I_{IN}	Receiver Input Current (A, B)	–10V ≤ $V_{A, B}$ ≤ 10V	●			±0.50	mA
R_{IN}	Receiver Input Impedance	–10V ≤ $V_{A, B}$ ≤ 10V	●	20	32		kΩ
t_r, t_f	Rise or Fall Time	(Figures 3, 7)			15		ns
t_{PLH}	Input to Output	(Figures 3, 7), 0°C ≤ T_A ≤ 70°C (Figures 3, 7), –40°C ≤ T_A ≤ 85°C	● ●		80 80	115 130	ns ns
t_{PHL}	Input to Output	(Figures 3, 7), 0°C ≤ T_A ≤ 70°C (Figures 3, 7), –40°C ≤ T_A ≤ 85°C	● ●		100 100	115 130	ns ns
Δt	Input to Output Difference, $\lvert t_{PLH} - t_{PHL} \rvert$	(Figures 3, 7), 0°C ≤ T_A ≤ 70°C (Figures 3, 7), –40°C ≤ T_A ≤ 85°C	● ●		4 4	17 25	ns ns
V.10 Driver							
V_O	Output Voltage	Open Circuit, R_L = 3.9k R_L = 450Ω (Figure 4) V_O at 450Ω > 0.9 V_O at R_L = 3.9k Driver 1 Only		±4.0 ±3.6		±6.0	V V
I_{SS}	Short-Circuit Current	V_O = GND; EIA-530, X.21, EIA-530-A Modes				±150	mA
I_{OZ}	Output Leakage Current	–0.25V ≤ V_O ≤ 0.25V, Power Off or No-Cable Mode or Driver Disabled	●		±0.1	±100	µA
t_r, t_f	Rise or Fall Time	(Figures 4, 8), R_L = 450Ω, C_L = 100pF R_{423SET} = 100k			4		µs
t_{PLH}	Input to Output	(Figures 4, 8), R_L = 450Ω, C_L = 100pF R_{423SET} = 100k			8		µs
t_{PHL}	Input to Output	(Figures 4, 8), R_L = 450Ω, C_L = 100pF R_{423SET} = 100k			8		µs

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 5V (Notes 2, 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V.10 Receiver							
V_{TH}	Receiver Input Threshold Voltage	0°C ≤ T_A ≤ 70°C –7V ≤ V_{CM} ≤ 7V, –40°C ≤ T_A ≤ 85°C	● ●	–0.2 –0.3		0.2 0.3	V V
ΔV_{TH}	Receiver Input Hysteresis		●		11	50	mV
I_{IN}	Receiver Input Current	–10V ≤ V_A ≤ 10V	●			±0.50	mA
R_{IN}	Receiver Input Impedance	–10V ≤ V_A ≤ 10V	●	20	30		kΩ
t_r, t_f	Rise or Fall Time	(Figures 5, 9)			15		ns
t_{PLH}	Input to Output	(Figures 5, 9)			350		ns
t_{PHL}	Input to Output	(Figures 5, 9)			350		ns
V.28 Driver							
V_O	Output Voltage	Open Circuit R_L = 3k (Figure 4)	 ●	 ±5	 7.6	±10	V V
I_{SS}	Short-Circuit Current	V_O = GND	●			±150	mA
I_{OZ}	Output Leakage Current	–0.25V ≤ V_O ≤ 0.25V, Power Off or No-Cable Mode or Driver Disabled	●		±0.01	±100	µA
SR	Slew Rate	(Figures 4, 8), R_L = 3k, C_L = 2500pF	●	4.0		30.0	V/µs
t_{PLH}	Input to Output	(Figures 4, 8), R_L = 3k, C_L = 2500pF	●		1.6	2.5	µs
t_{PHL}	Input to Output	(Figures 4, 8), R_L = 3k, C_L = 2500pF	●		1.6	2.5	µs
V.28 Receiver							
V_{THL}	Input Low Threshold Voltage		●		1.4	0.8	V
V_{TLH}	Input High Threshold Voltage		●	2.0	1.4		V
ΔV_{TH}	Receiver Input Hysteresis		●	0.1	0.4	1.0	V
R_{IN}	Receiver Input Impedance	–15V ≤ V_A ≤ 15V	●	3	5	7	kΩ
t_r, t_f	Rise or Fall Time	(Figures 5, 9)			15		ns
t_{PLH}	Input to Output	(Figures 5, 9), CTRL = 0V CTRL = V_{CC}	 ●		110 330	 800	ns ns
t_{PHL}	Input to Output	(Figures 5, 9), CTRL = 0V CTRL = V_{CC}	 ●		170 480	 800	ns ns

Note 1: Absolute Maximum Ratings are those beyond which the safety of a device may be impaired.

Note 2: All currents into device pins are positive; all currents out of device are negative. All voltages are referenced to device ground unless otherwise specified.

Note 3: All typicals are given for V_{CC} = 5V, C1 = C2 = C_{VCC} = C_{VDD} = 1µF, C_{VEE} = 3.3µF tantalum capacitors and T_A = 25°C.

PIN FUNCTIONS

V_{DD} (Pin 1): Generated Positive Supply Voltage for RS232. Connect a 1µF capacitor to ground.

C1⁺ (Pin 2): Capacitor C1 Positive Terminal. Connect a 1µF capacitor between C1⁺ and C1⁻.

$PWRV_{CC}$ (Pin 3): Positive Supply for the Charge Pump. 4.75V ≤ $PWRV_{CC}$ ≤ 5.25V. Tie to V_{CC} (Pin 8) and bypass with a 1µF capacitor to ground.

C1⁻ (Pin 4): Capacitor C1 Negative Terminal.

D1 (Pin 5): TTL Level Driver 1 Input.

D2 (Pin 6): TTL Level Driver 2 Input.

D3 (Pin 7): TTL Level Driver 3 Input. Becomes a CMOS level output when the chip is in the echoed clock mode ($\overline{EC}$ = 0V).

PIN FUNCTIONS

V_{CC} (Pin 8): Positive Supply for the Transceivers. 4.75V ≤ V_{CC} ≤ 5.25V. Tie to $PWRV_{CC}$ (Pin 3).

D4 (Pin 9): TTL Level Driver 4 Input.

D4EN (Pin 10): TTL Level Enable Input for Driver 4. When high, driver 4 outputs are enabled. When low, driver 4 outputs are forced into a high impedance state. D4EN is not affected by the $\overline{LATCH}$ pin.

INVERT (Pin 11): TTL Level Signal Invert Input. When high, an extra inverter will be added to the driver 4 and receiver 1 signal path. The data stream will change polarity, i.e., a 1 becomes 0 and a 0 becomes a 1. When the pin is low the data flows through with no polarity change. INVERT is not affected by the $\overline{LATCH}$ pin.

$\overline{R1EN}$ (Pin 12): Logic Level Enable Input for Receiver 1. When low, receiver 1 output is enabled. When high, receiver 1 output is forced into a high impedance state.

R1O (Pin 13): CMOS Level Receiver 1 Output.

R2O (Pin 14): CMOS Level Receiver 2 Output.

R3O (Pin 15): CMOS Level Receiver 3 Output.

R4O (Pin 16): CMOS Level Receiver 4 Output.

M0 (Pin 17): TTL Level Mode Select Input 0. The data on M0 is latched when $\overline{LATCH}$ is high.

M1 (Pin 18): TTL Level Mode Select Input 1. The data on M1 is latched when $\overline{LATCH}$ is high.

M2 (Pin 19): TTL Level Mode Select Input 2. The data on M2 is latched when $\overline{LATCH}$ is high.

CTRL/$\overline{CLK}$ (Pin 20): TTL Level Mode Select Input. When the pin is low the chip will be configured for clock and data signals. When the pin is high the chip will be configured for control signals. The data on CTRL/$\overline{CLK}$ is latched when $\overline{LATCH}$ is high.

DCE/$\overline{DTE}$ (Pin 21): TTL Level Mode Select Input. When high, the DCE mode is selected. When low the DTE mode is selected. The data on DCE/$\overline{DTE}$ is latched when $\overline{LATCH}$ is high.

$\overline{LATCH}$ (Pin 22): TTL Level Logic Signal Latch Input. When low the input buffers on M0, M1, M2, CTRL/$\overline{CLK}$, DCE/$\overline{DTE}$, $\overline{LB}$ and $\overline{EC}$ are transparent. When $\overline{LATCH}$ is pulled high the data on the logic pins is latched into their respective input buffers. The data latch allows the logic lines to be shared between multiple I/O ports.

$\overline{LB}$ (Pin 23): TTL Level Loop-Back Select Input. When low the chip enters the loop-back configuration and is configured for normal operation when $\overline{LB}$ is high. The data on $\overline{LB}$ is latched when $\overline{LATCH}$ is high.

$\overline{EC}$ (Pin 24): TTL Level Echoed Clock Select Input. When low the part enters the echoed clock configuration and is configured for normal operation when $\overline{EC}$ is high. The data on $\overline{EC}$ is latched when $\overline{LATCH}$ is high.

423 SET (Pin 25): Analog Input Pin for the RS423 Driver Output Rise and Fall Time Set Resistor. Connect the resistor from the pin to ground.

R4 A (Pin 26): Receiver 4 Inverting Input.

R3 B (Pin 27): Receiver 3 Noninverting Input.

R3 A (Pin 28): Receiver 3 Inverting Input.

R2 B (Pin 29): Receiver 2 Noninverting Input.

R2 A (Pin 30): Receiver 2 Inverting Input.

R1 B (Pin 31): Receiver 1 Noninverting Input.

R1 A (Pin 32): Receiver 1 Inverting Input.

D4 B (Pin 33): Driver 4 Noninverting Output.

D4 A (Pin 34): Driver 4 Inverting Output.

D3 B (Pin 35): Driver 3 Noninverting Output.

D3 A (Pin 36): Driver 3 Inverting Output.

D2 B (Pin 37): Driver 2 Noninverting Output.

D2 A (Pin 38): Driver 2 Inverting Output.

D1 A (Pin 39): Driver 1 Inverting Output.

GND (Pin 40): Signal Ground. Connect to PGND (Pin 41).

PGND (Pin 41): Charge Pump Power Ground. Connect to the GND (Pin 40).

V_{EE} (Pin 42): Generated Negative Supply Voltage. Connect a 3.3µF capacitor to ground.

$C2^-$ (Pin 43): Capacitor C2 Negative Terminal. Connect a 1µF capacitor between $C2^+$ and $C2^-$.

$C2^+$ (Pin 44): Capacitor C2 Positive Terminal. Connect a 1µF capacitor between $C2^+$ and $C2^-$.

TEST CIRCUITS

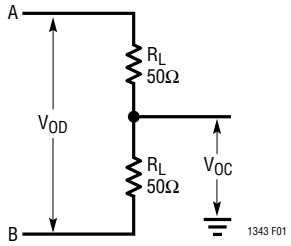


Figure 1. RS422 Driver Test Circuit

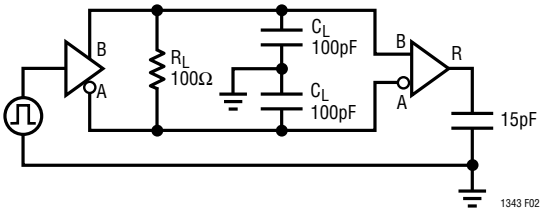


Figure 2. RS422 Driver/Receiver AC Test Circuit

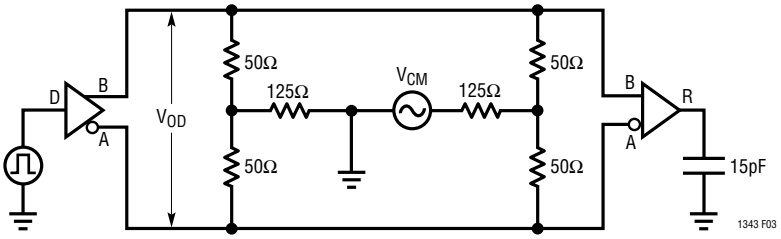


Figure 3. V.35 Driver/Receiver Test Circuit

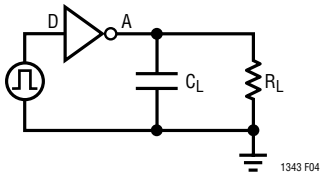


Figure 4. V.10/V.28 Driver Test Circuit

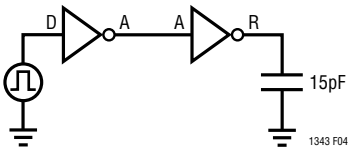


Figure 5. V.10/V.28 Receiver Test Circuit

MODE SELECTION

LTC1343 MODE NAME	M2	M1	M0	CTRL/CLK	D1	D2	D3	D4	R1	R2	R3	R4
V.10, RS423	0	0	0	X	V.10	V.10	V.10	V.10	V.10	V.10	V.10	V.10
EIA-530-A Clock and Data	0	0	1	0	V.10	V.11	V.11	V.11	V.11	V.11	V.11	V.10
EIA-530-A Control	0	0	1	1	V.10	V.11	V.10	V.11	V.11	V.10	V.11	V.10
Reserved	0	1	0	X	V.10	V.11	V.11	V.11	V.11	V.11	V.11	V.10
X.21	0	1	1	X	V.10	V.11	V.11	V.11	V.11	V.11	V.11	V.10
V.35 Clock and Data	1	0	0	0	V.28	V.35	V.35	V.35	V.35	V.35	V.35	V.28
V.35 Control	1	0	0	1	V.28	V.28	V.28	V.28	V.28	V.28	V.28	V.28
EIA-530, RS449, V.36	1	0	1	X	V.10	V.11	V.11	V.11	V.11	V.11	V.11	V.10
V.28, RS232	1	1	0	X	V.28	V.28	V.28	V.28	V.28	V.28	V.28	V.28
No Cable	1	1	1	X	Z	Z	Z	Z	Z	Z	Z	Z

SWITCHING TIME WAVEFORMS

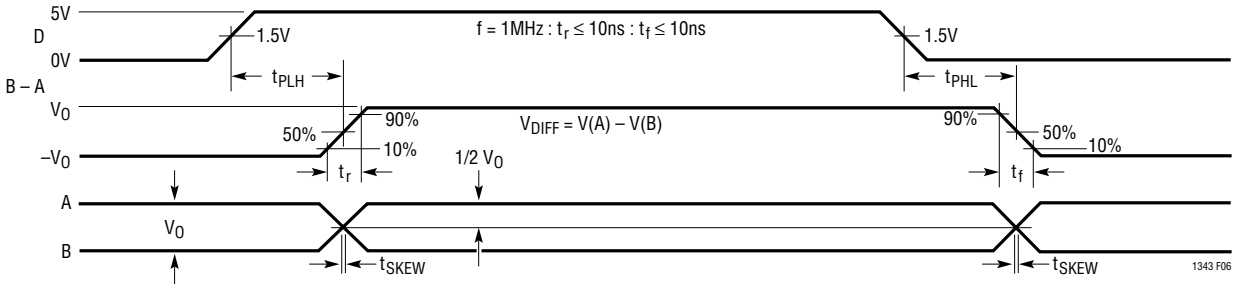


Figure 6. V.11, V.35 Driver Propagation Delays

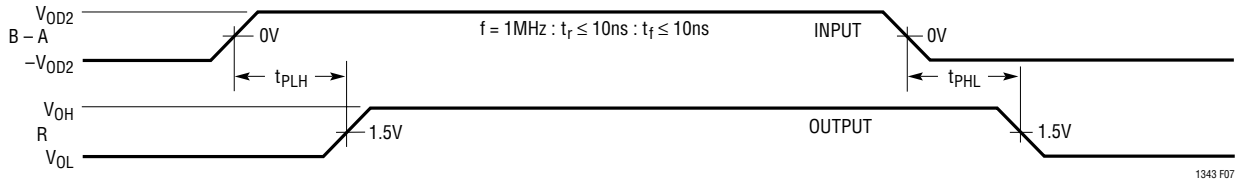


Figure 7. V.11, V.35 Receiver Propagation Delays

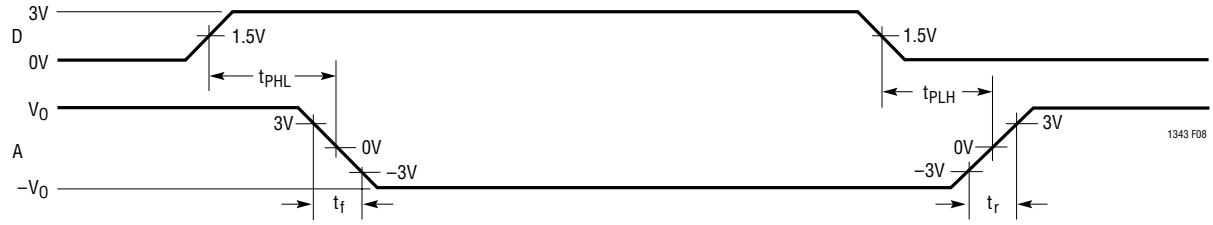


Figure 8. V.10, V.28 Driver Propagation Delays

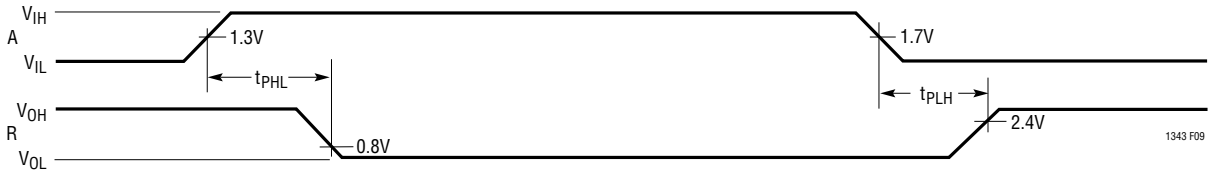


Figure 9. V.10, V.28 Receiver Propagation Delays

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Overview

The LTC1343 is a 4-driver/4-receiver multiprotocol transceiver that operates from a single 5V supply. Two LTC1343s form the core of a complete software-selectable DTE or DCE interface port that supports the RS232, RS449, EIA-530, EIA-530-A, V.35, V.36 or X.21 protocols. Cable termination may be implemented using the LTC1344 software-selectable cable termination chip or by using existing discrete designs.

A complete DCE-to-DTE interface operating in EIA-530 mode is shown in Figure 10. The first LTC1343 of each port is used to generate the clock and data signals along with LL (Local Loop-back) and TM (Test Mode). The second LTC1343 is used to generate the control signals along with

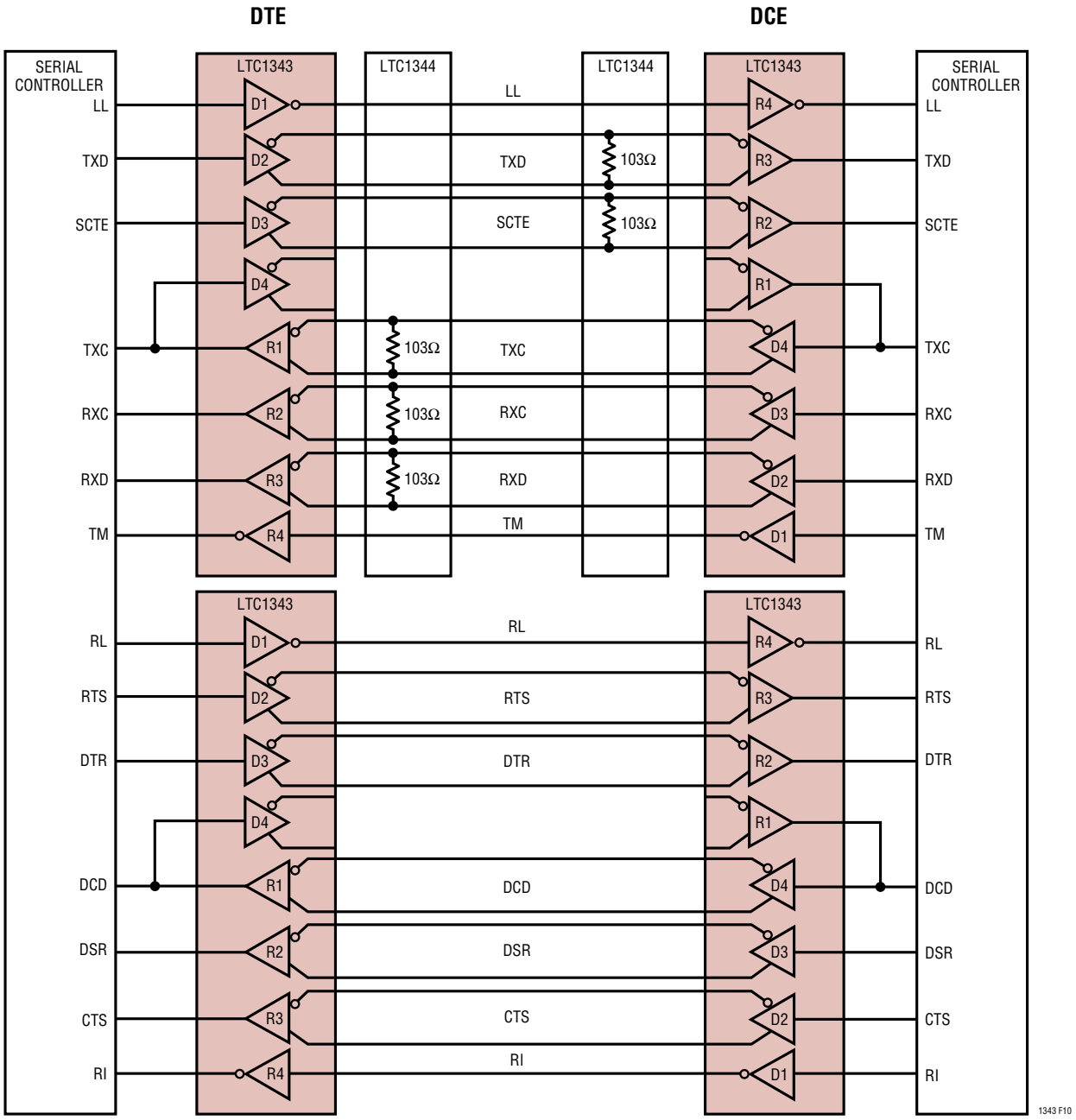

Figure 10. Complete Multiprotocol Interface in EIA-530 Mode

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RL (Remote Loop-back) and RI (Ring Indicate). The LTC1344 cable termination chip is used only for the clock and data signals because they must support V.35 cable termination. The control signals do not need any external resistors.

Mode Selection

The interface protocol is selected using the mode select pins M0, M1, M2 and CTRL/$\overline{CLK}$ (see the Mode Selection table). The CTRL/$\overline{CLK}$ pin should be pulled high if the LTC1343 is being used to generate control signals and pulled low if used to generate clock and data signals.

For example, if the port is configured as a V.35 interface, the mode selection pins should be M2 = 1, M1 = 0, M0 = 0. For the control signals, CTRL/$\overline{CLK}$ = 1 and the drivers and receivers will operate in RS232 (V.28) electrical mode. For the clock and data signals, CTRL/$\overline{CLK}$ = 0 and the drivers and receivers will operate in V.35 electrical mode, except for the single-ended driver and receiver which will operate in the RS232 (V.28) electrical mode. The DCE/$\overline{DTE}$ pin will configure the port for DCE mode when high, and DTE when low.

The interface protocol may be selected simply by plugging the appropriate interface cable into the connector. The mode pins are routed to the connector and are left unconnected (1) or wired to ground (0) in the cable as shown in Figure 11.

The pull-up resistors R1 through R4 will ensure a binary 1 when a pin is left unconnected and that the two LTC1343s and the LTC1344 enter the no-cable mode when the cable is removed. In the no-cable mode the LTC1343 supply current drops to less than 200µA and all LTC1343 driver outputs and LTC1344 resistive terminations are forced into a high impedance state. Note that the data latch pin, $\overline{LATCH}$, is shorted to ground for all chips.

The interface protocol may also be selected by the serial controller or host microprocessor as shown in Figure 12.

The mode selection pins M0, M1, M2 and DCE/$\overline{DTE}$ can be shared between multiple interface ports, while each port

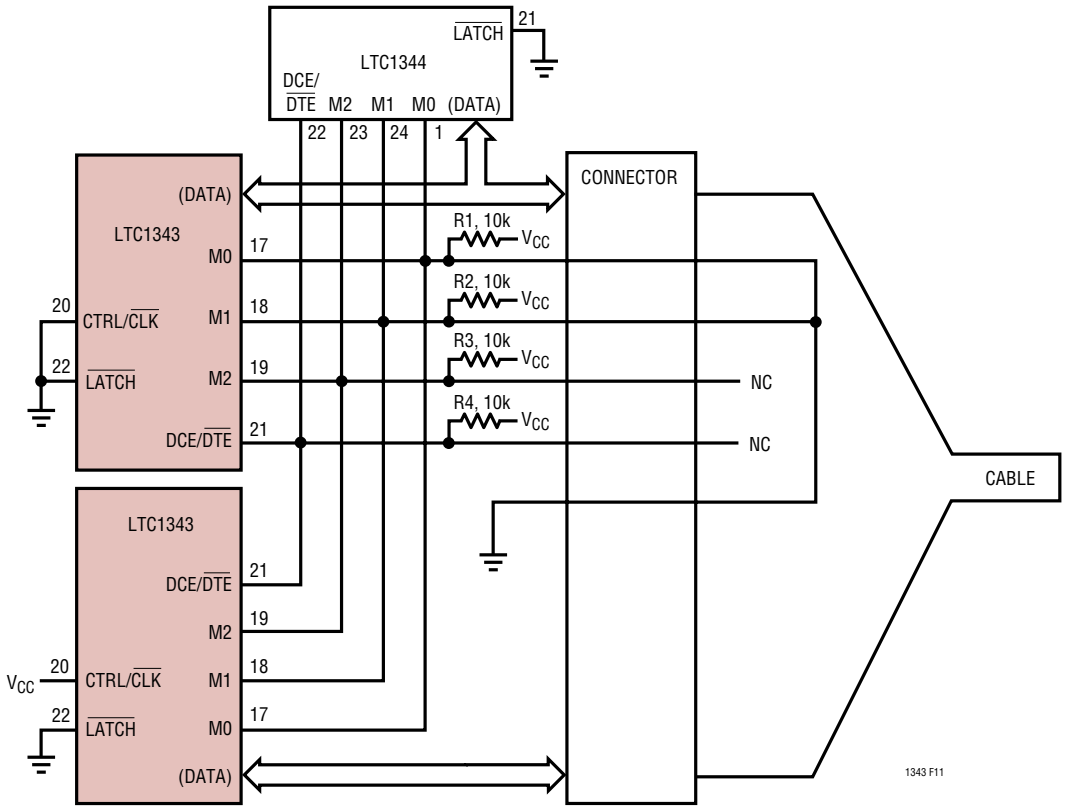

Figure 11: Single Port DCE/V.35 Mode Selection in the Cable

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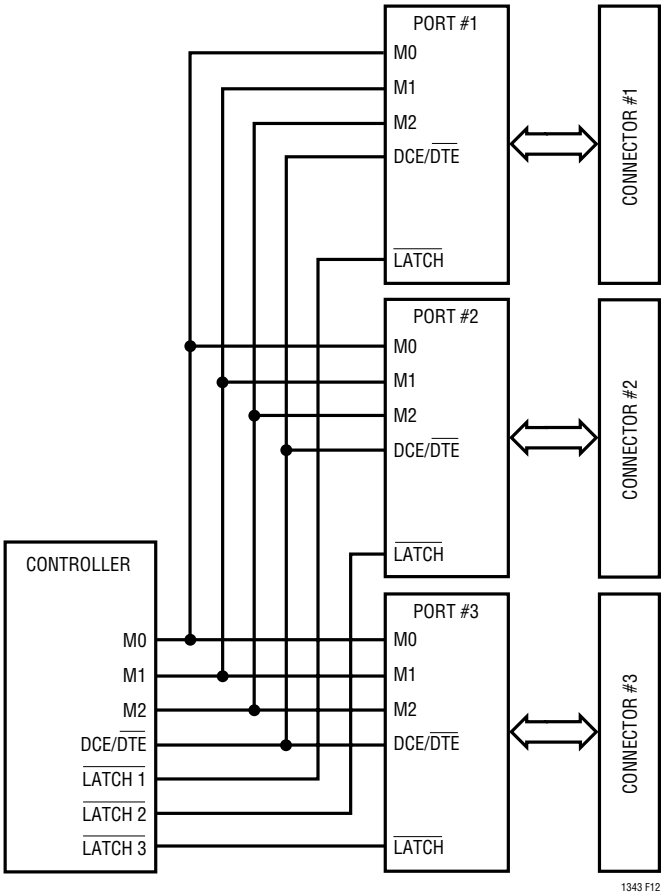

Figure 12: Mode Selection by the Controller

has a unique data latch signal which acts as a write enable. When the $\overline{\text{LATCH}}$ pin is low the buffers on the M0, M1, M2, CTRL/$\overline{\text{CLK}}$, DCE/$\overline{\text{DTE}}$, $\overline{\text{LB}}$ and $\overline{\text{EC}}$ pins are transparent. When the $\overline{\text{LATCH}}$ pin is pulled high the buffers latch the data and changes on the input pins will no longer affect the chip.

The mode selection may also be accomplished by using jumpers to connect the mode pins to ground or V_{CC}.

Cable Termination

Traditional implementations have included switching resistors with expensive relays, or requiring the user to change termination modules every time the interface standard has changed. Custom cables have been used with the termination in the cable head, or separate terminations are built on the board and a custom cable routes the signals to the appropriate termination. Switching the terminations with FETs is difficult because the FETs must remain off even though the signal voltage is beyond the supply voltage for the FET drivers or the power is off.

Using the LTC1344 along with the LTC1343 solves the cable termination switching problem. Via software control, the LTC1344 provides termination for the V.10 (RS423), V.11 (RS422), V.28 (RS232) and V.35 electrical protocols.

V.10 (RS423) Interface

A typical V.10 unbalanced interface is shown in Figure 13. A V.10 single-ended generator output A with ground C is connected to a differential receiver with inputs A' connected to A, and input B' connected to the signal return ground C. The receiver's ground C' is separate from the signal return. Usually, no cable termination is required for V.10 interfaces, but the receiver inputs must be compliant with the impedance curve shown in Figure 14.

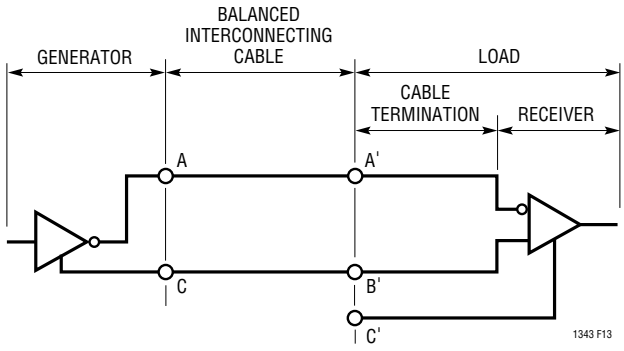

Figure 13. Typical V.10 Interface

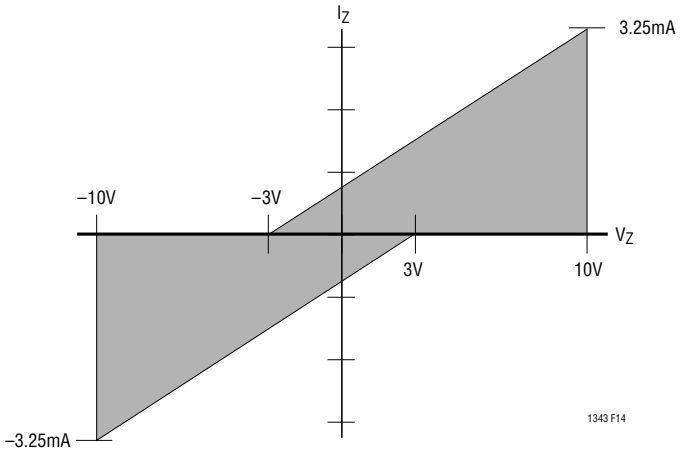

Figure 14. V.10 Receiver Input Impedance

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The V.10 receiver configuration in the LTC1343 and LTC1344 is shown in Figure 15. In V.10 mode switches S1 and S2 inside the LTC1344 and S3 inside the LTC1343 are turned off. Switch S4 inside the LTC1343 shorts the noninverting receiver input to ground so the B input at the connector can be left floating. The cable termination is then the 30k input impedance to ground of the LTC1343 V.10 receiver.

V.11 (RS422) Interface

A typical V.11 balanced interface is shown in Figure 16. A V.11 differential generator with outputs A and B with ground C is connected to a differential receiver with ground C', inputs A' connected to A, B' connected to B. The V.11 interface has a differential termination at the receiver end that has a minimum value of 100Ω. The termination resistor is optional in the V.11 specification, but for the high speed clock and data lines, the termination is required to prevent reflections from corrupting the data. The receiver inputs must also be compliant with the impedance curve shown in Figure 14.

In V.11 mode, all switches are off except S1 inside the LTC1344 which connects a 103Ω differential termination impedance to the cable as shown in Figure 17.

V.28 (RS232) Interface

A typical V.28 unbalanced interface is shown in Figure 18. A. V.28 single-ended generator output A with ground C is connected to a single-ended receiver with inputs A' connected to A, ground C' connected via the signal return ground C.

In V.28 mode all switches are off except S3 inside the LTC1343 which connects a 6k (R8) impedance to ground in parallel with 20k (R5) plus 10k (R6) for a combined impedance of 5k as shown in Figure 19. The noninverting input is disconnected inside the LTC1343 receiver and connected to a TTL level reference voltage for a 1.4V receiver trip point.

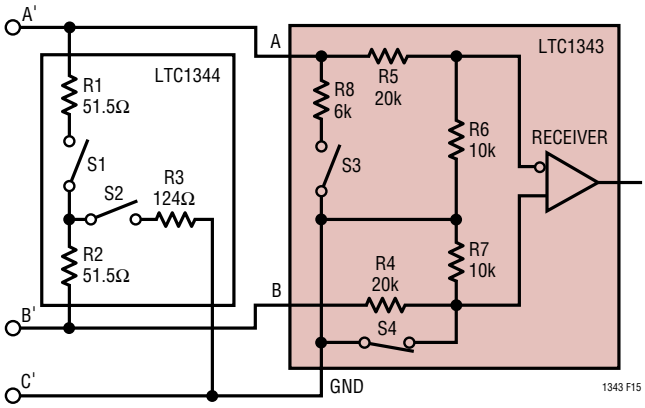

Figure 15. V.10 Receiver Configuration

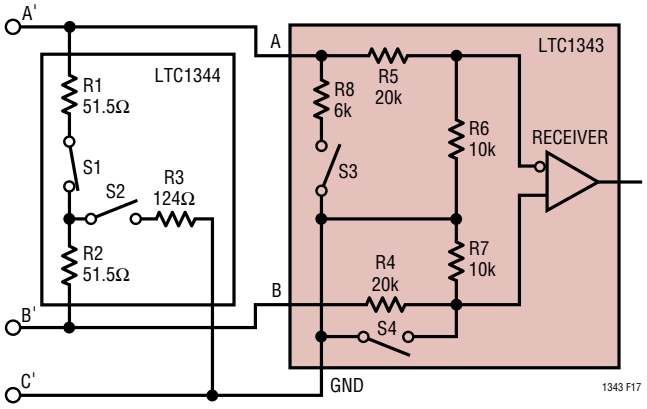

Figure 17. V.11 Receiver Configuration

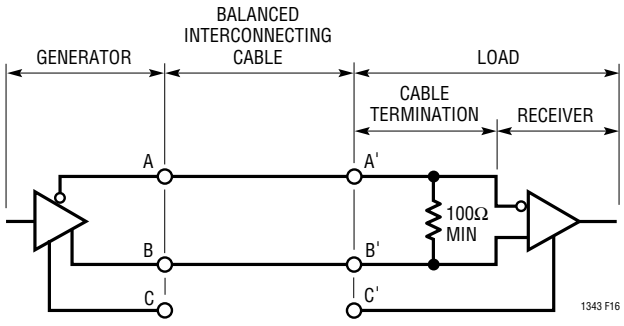

Figure 16. Typical V.11 Interface

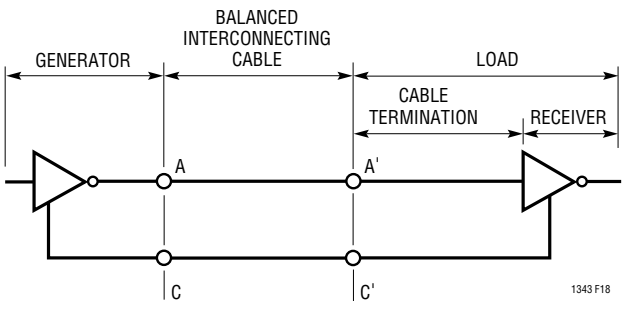

Figure 18. Typical V.28 Interface

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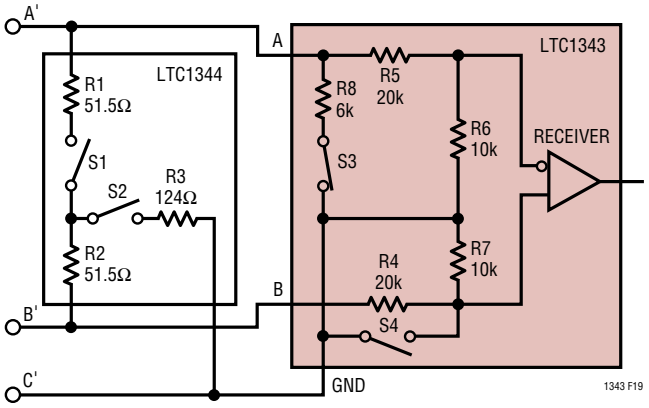

Figure 19. V.28 Receiver Configuration

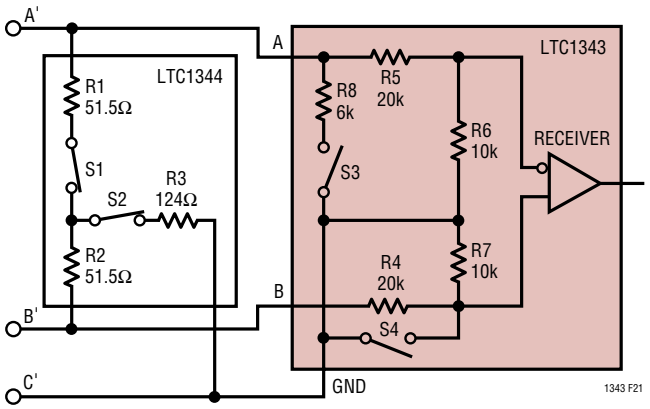

Figure 21. V.35 Receiver Configuration

V.35 Interface

A typical V.35 balanced interface is shown in Figure 20. A V.35 differential generator with outputs A and B with ground C is connected to a differential receiver with ground C', inputs A' connected to A, B' connected to B. The V.35 interface requires a T or delta network termination at the receiver end and the generator end. The receiver differential impedance measured at the connector must be 100Ω ±10Ω, and the impedance between shorted terminals (A' and B) and ground C' must be 150Ω ±15Ω.

In V.35 mode, both switches S1 and S2 inside the LTC1344 are on, connecting the T network impedance as shown in Figure 21. Both switches in the LTC1343 are off. The 30k input impedance of the receiver is placed in parallel with the T network termination, but does not affect the overall input impedance significantly.

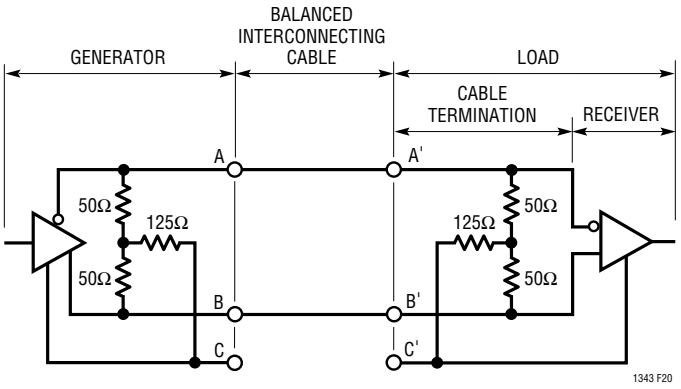

Figure 20. Typical V.35 Interface

The generator differential impedance must be 50Ω to 150Ω and the impedance between shorted terminals (A and B) and ground C must be 150Ω ±15Ω. For the generator termination, switches S1 and S2 are both on and the top side of the center resistor is brought out to a pin so it can be bypassed with an external capacitor to reduce common mode noise as shown in Figure 22.

Any mismatch in the driver rise and fall times or skew in the driver propagation delays will force current through the center termination resistor to ground, causing a high frequency common mode spike on the A and B terminals. The common mode spike can cause EMI problems that are reduced by capacitor C1 which shunts much of the common mode energy to ground rather than down the cable.

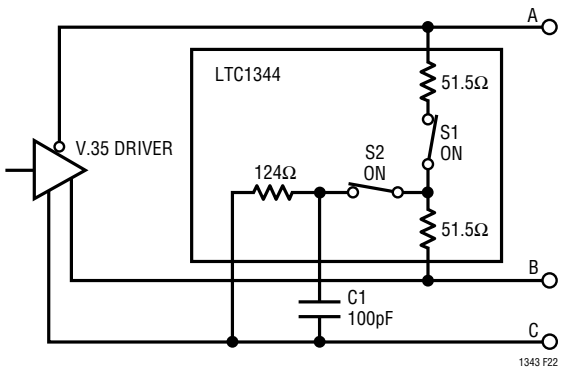

Figure 22. V.35 Driver Using the LTC1344

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Echoed Clock Mode

The LTC1343 contains the logic to generate the echoed clock when using a serial controller with only two clock pins. Figure 23 shows the chip in both the DTE and DCE echoed clock in EIA-530 mode. The control signals are not shown. The echoed clock configuration is selected by pulling the $\overline{EC}$ pin low. On the DTE side the transmit clock TXC receiver output is connected to the echoed clock, SCTE, driver input. The TXC pin on the serial controller is configured as an input. On the DCE side, the transmit clock from the serial controller is used to generate both TXC and RXC. A phase inverter is placed in the TXC signal path on both the DTE and DCE side to help correct phase problems with long cables. If the Invert pin is high, the phase of the data is inverted.

Loop-Back

The LTC1343 contains logic for placing the interface into a loop-back configuration for testing. Both DTE and DCE loop-back configurations are supported. Figure 24 shows a complete DTE interface in the loop-back configuration with the $\overline{EC}$ pin pulled high. The loop-back configuration is selected by pulling the $\overline{LB}$ pin low. Both the line side and logic side signals are looped back. The DCE loop-back configuration is shown in Figure 25.

If the echoed clock mode is selected by pulling $\overline{EC}$ low, D3 becomes an output and is connected to receiver 2's output R3 in DTE mode as shown in Figure 26. In the echoed clock DCE loop-back mode, driver 4 is connected to driver 3's input D3 as shown in Figure 27.

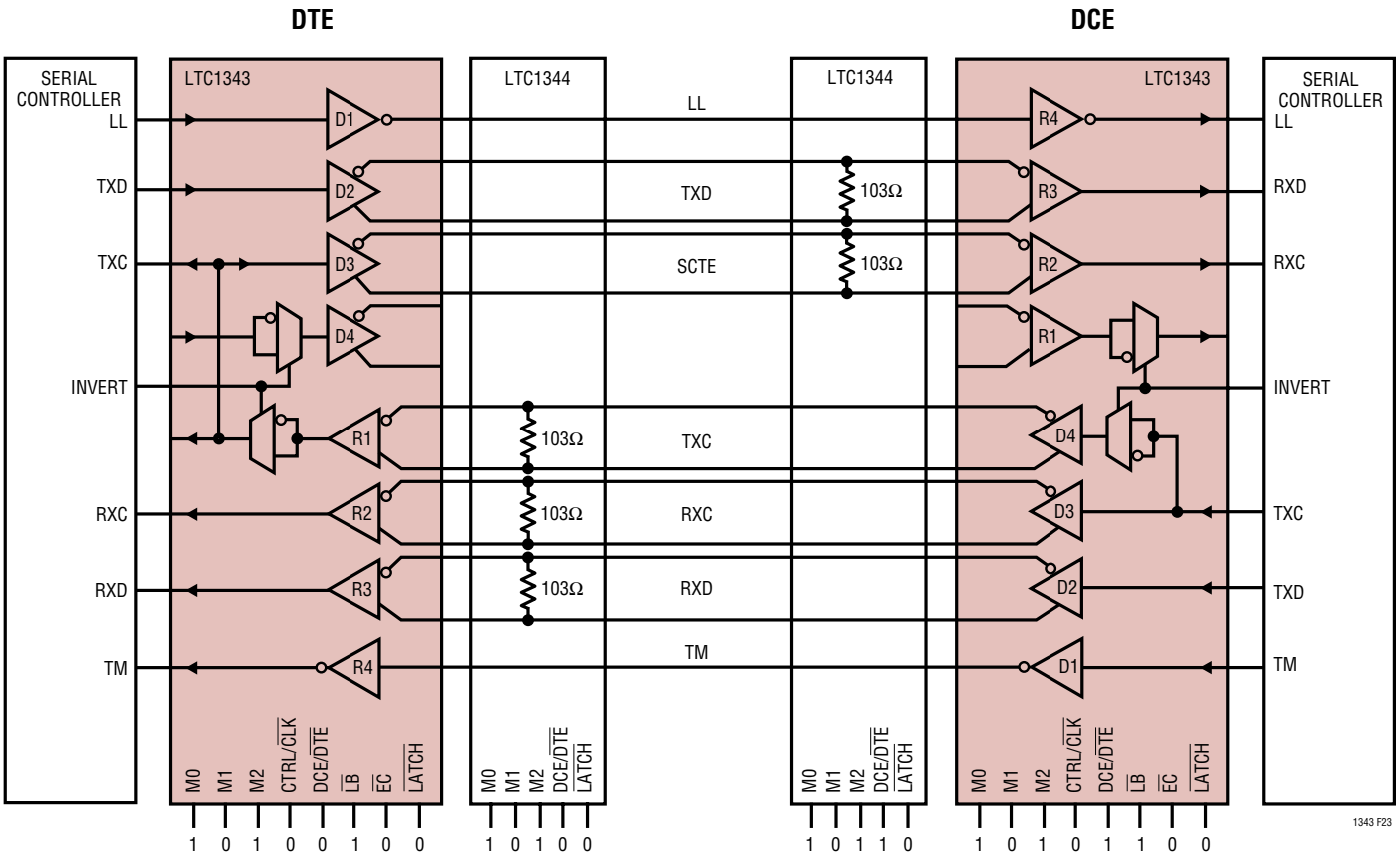

Figure 23. EIA-530 Echoed Clock Configuration

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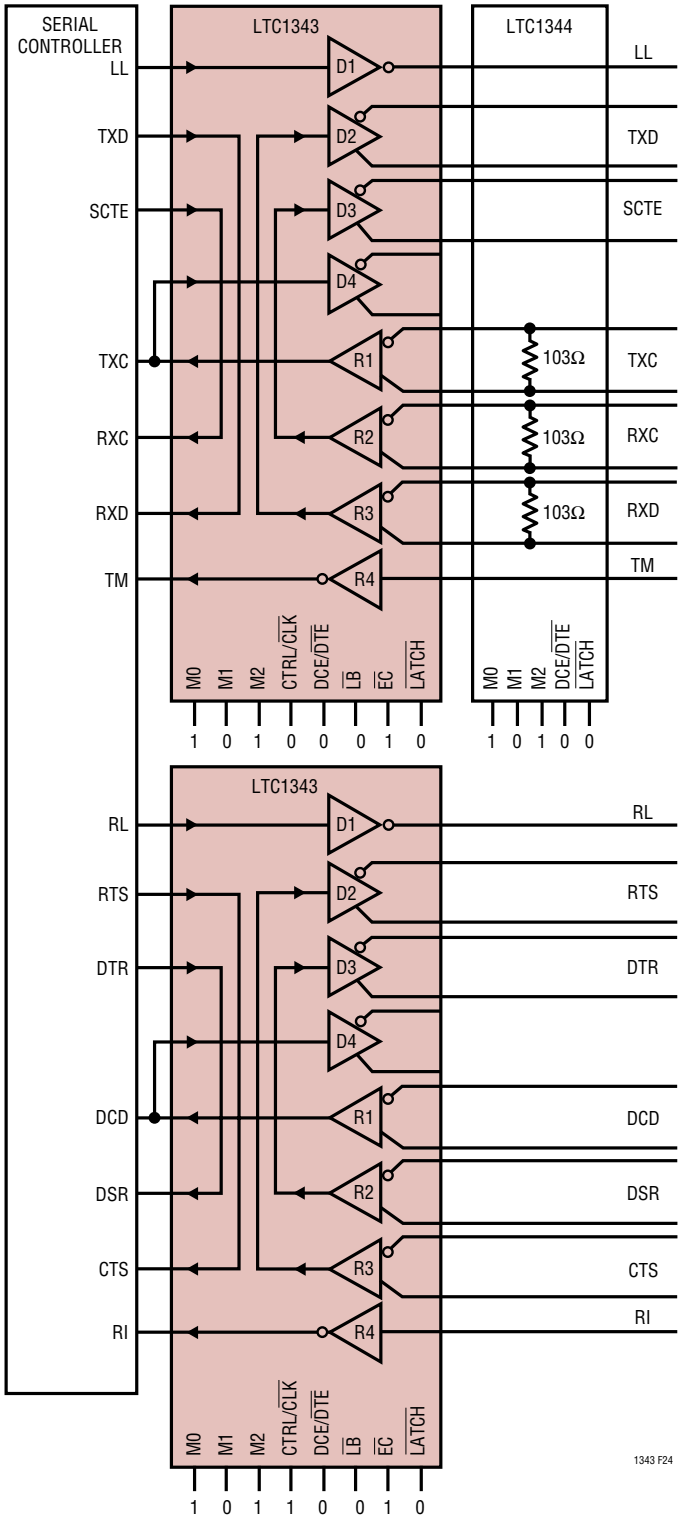

Figure 24. Normal DTE Loop-Back

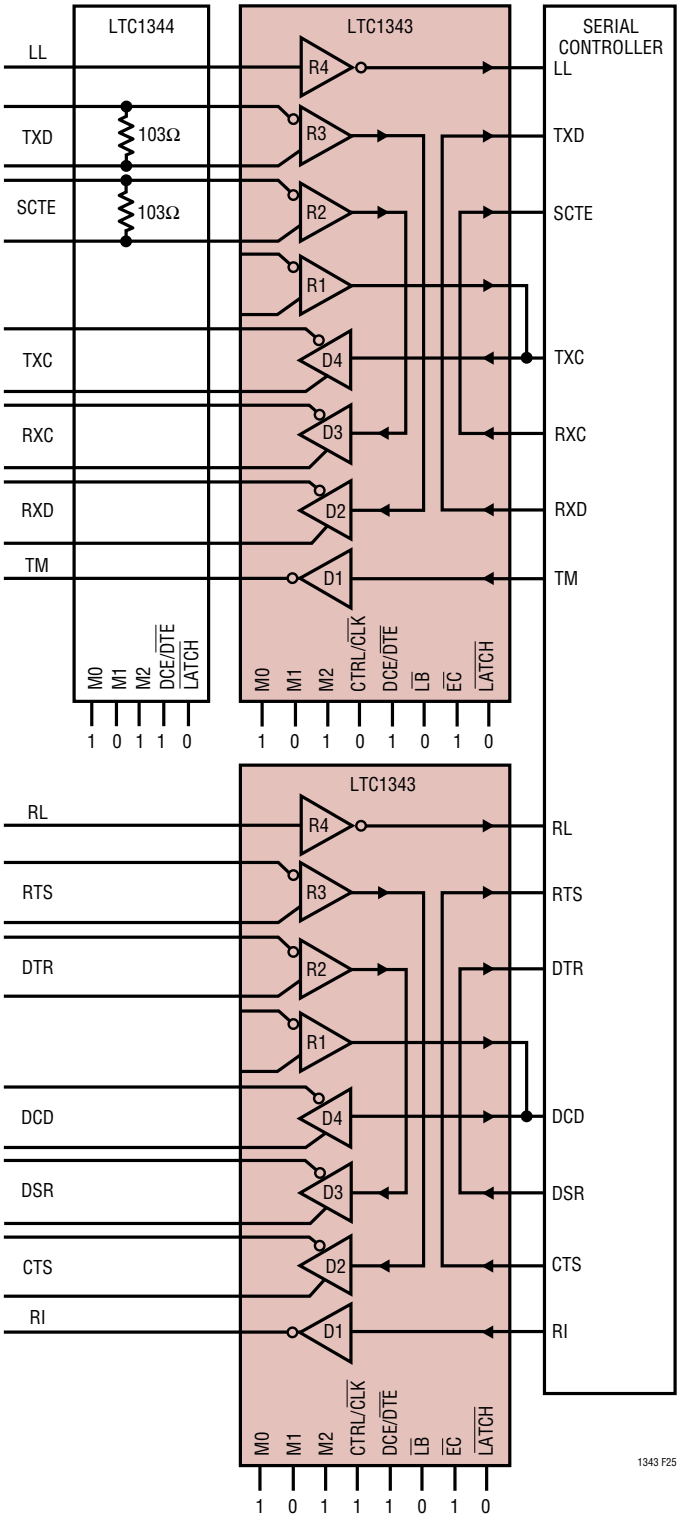

Figure 25. Normal DCE Loop-Back

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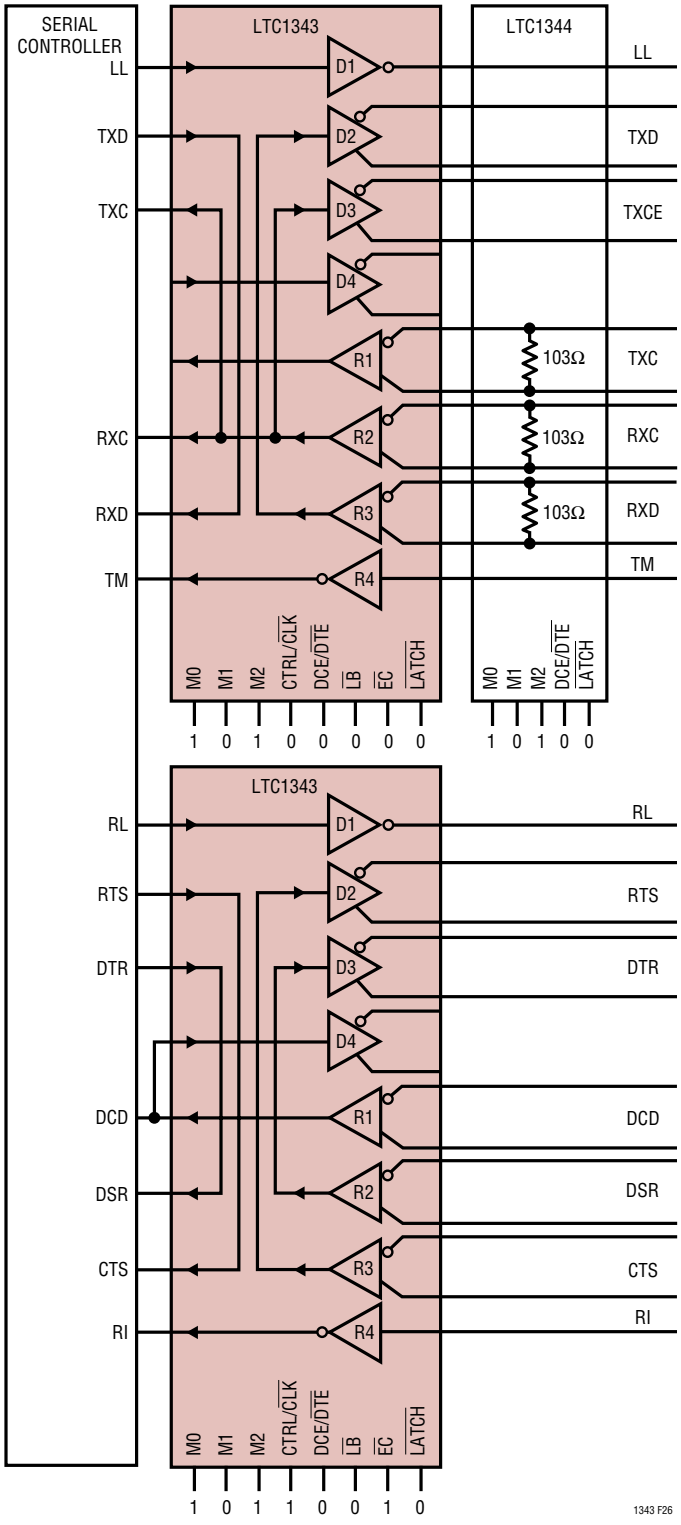

Figure 26. Echoed Clock, DTE Loop-Back

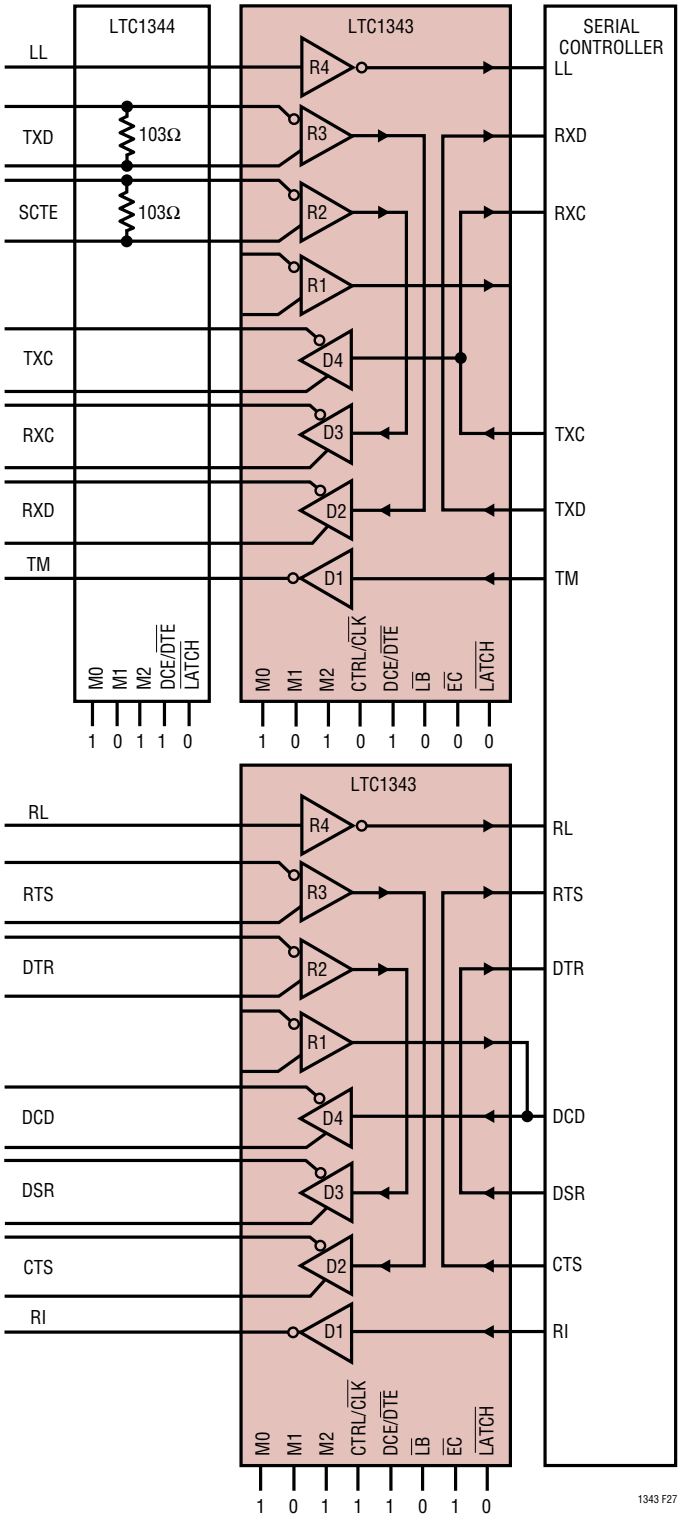

Figure 27. Echoed Clock, DCE Loop-Back

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No-Cable Mode

The no-cable mode (M0 = M1 = M2 = 1) is intended for the case when the cable is disconnected from the connector. The charge pump, bias circuitry, drivers and receivers are turned off, the driver outputs are forced into a high impedance state, and the supply current drops to less than 200μA. It can also be used to share I/O lines with other drivers and receivers without loading down the signals.

Charge Pump

The LTC1343 uses an internal capacitive charge pump to generate V_{DD} and V_{EE} as shown in Figure 28. A voltage doubler generates about 8V on V_{DD} and a voltage inverter generates about –7.5V for V_{EE}. Four 1μF surface mounted tantalum or ceramic capacitors are required for C1, C2, C3 and C4. The V_{EE} capacitor C5 should be a minimum of 3.3μF. All capacitors are 16V.

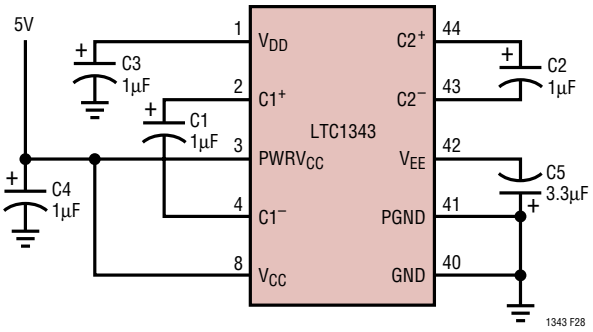

Figure 28. Charge Pump

Receiver Fail-Safe and Glitch Filter

All LTC1343 receivers feature fail-safe operation in all modes except no-cable mode. If the receiver inputs are left floating or shorted together by a termination resistor, the receiver output will always be forced to a logic high. External pull-up resistors are required on receiver outputs if fail-safe operation in the no-cable mode is desired.

When the chip is configured for control signals by pulling the CTRL/$\overline{CLK}$ pin high, a glitch filter is connected to all receiver inputs. The filter will reject any glitches at the receiver inputs less than 300ns.

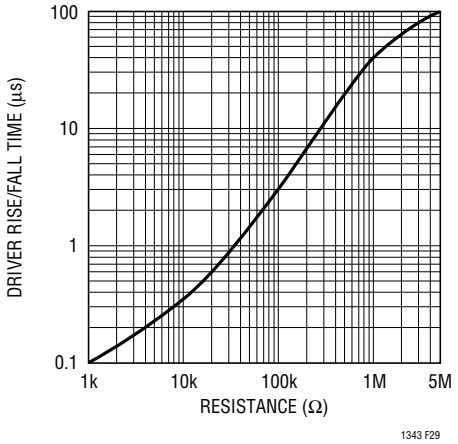

Figure 29. V.10 Driver Rise and Fall Time vs Resistor Value

V.10 Driver Rise and Fall Times

The rise and fall times of the V.10 drivers is programmed by placing a 1/8W, 5% resistor between the 423 SET (Pin 25) and ground. The graph of Driver Rise and Fall Times vs Resistor Value is shown in Figure 29.

Enabling the Single-Ended Driver and Receiver

When the LTC1343 is being used to generate the control signals (CTRL/$\overline{CLK}$ = high) and the $\overline{EC}$ pin is pulled low, the DCE/$\overline{DTE}$ pin becomes an enable for driver 1 and receiver 4 so their inputs and outputs can be tied together as shown in Figure 30.

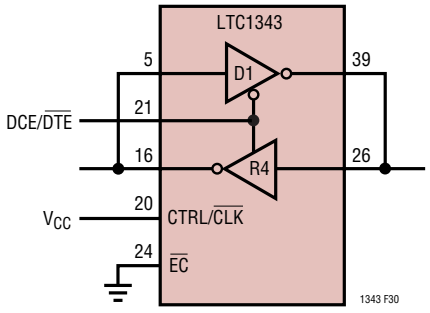

Figure 30. Single-Ended Driver and Receiver Enable

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The $\overline{EC}$ pin has no affect on the configuration when CTRL/$\overline{CLK}$ is high except to allow the DCE/$\overline{DTE}$ pin to become an enable. When DCE/$\overline{DTE}$ is low, the driver 1 output is enabled. The receiver 4 output goes into three-state and the input presents a 30kΩ load to ground.

When DCE/$\overline{DTE}$ is high, the driver 1 output goes into three-state and the receiver 4 output is enabled. The receiver 4 input presents a 30kΩ load to ground in all modes except when configured for RS232 operation when the input impedance is 5kΩ to ground.

DTE vs DCE Operation

The DCE/$\overline{DTE}$ pin does not allow a given LTC1343 pin to be reconfigured as a driver or receiver. The DCE/$\overline{DTE}$ pin only selects the loop-back topology and acts as an enable for the single-ended driver and receiver for control signals.

However, the LTC1343 can be configured for either DTE or DCE operation in one of three ways: a dedicated DTE or DCE port with a connector of appropriate gender, a port with one connector that can be configured for DTE or DCE operation by rerouting the signals to the LTC1343 using a dedicated DTE cable or dedicated DCE cable, or a port with one connector and one cable using four LTC1343s.

A dedicated DTE port using a DB-25 male connector is shown in Figure 31. The interface mode is selected by logic outputs from the controller or from jumpers to either V_{CC} or GND on the mode select pins. A dedicated DCE port using a DB-25 female connector is shown in Figure 32.

A port with one DB-25 connector that can be configured for either DTE or DCE operation is shown in Figure 33. The configuration requires separate cables for proper signal routing in DTE or DCE operation. For example, in DTE mode, the TXD signal is routed to connector Pins 2 and 14 via driver 2 in the LTC1343. In DCE mode, driver 2 now routes the RXD signal to Pins 2 and 14.

A combination DTE/DCE port that doesn't require separate DCE/DTE cables is shown in Figure 34. In DTE mode, the top and bottom LTC1343s are enabled and the middle two are placed in the no-cable mode, which forces all of the drivers and receivers into a high impedance state. In the DCE mode, the middle two LTC1343s are enabled and the top and bottom LTC1343s disabled. With this scheme, any connector pin can be configured for sending or receiving signals. Note that only one LTC1344 is required.

Multiprotocol Interface with Ring-Indicate and a DB-25 Connector

If the RI signal in RS232 mode is implemented, driver 4 and receiver 1 in the control chip can be tied to connector Pin 22 in order to implement the RI signal in RS232 mode and DSR B signal for the other modes. Figure 35 shows the DTE configuration and Figure 36 the DCE configuration. In DCE mode, the DCE/$\overline{DTE}$ pin should be driven with a logic signal from the controller that goes low only when the interface is in the RS232 mode. Since the receiver 4 input impedance is greater than 30kΩ in all modes except RS232, it can be enabled at all other times and not load down the line. When driver 1 is disabled, it remains in a high impedance state and does not load the line.

Cable-Selectable Multiprotocol Interface

A cable-selectable multiprotocol DTE/DCE interface is shown in Figure 37. The control signals LL, RL and TM are not implemented. The select lines M0, M1 and DCE/$\overline{DTE}$ are brought out to the connector. The mode is selected through the cable by wiring M0 (connector Pin 18), M1 (connector Pin 21) and DCE/$\overline{DTE}$ (connector Pin 25) to ground (connector Pin 7) or letting them float. If M0, M1 or DCE/$\overline{DTE}$ are floating, pull-up resistors R3, R4 and R5 will pull the signals to V_{CC}. The select bit M1 is hard wired to V_{CC}. When the cable is pulled out, the interface will go into the no-cable mode.

Multiprotocol Interface with a μDB-26 Connector

The controller-selectable multiprotocol DTE/DCE interface with a standard μDB-26 connector is shown in Figure 38. The RL, LL and TM signals are implemented and RI is mapped to Pin 26 on the connector. A cable-selectable version is shown in Figure 39. The TM and RL signals have been dropped, but LL is still implemented.

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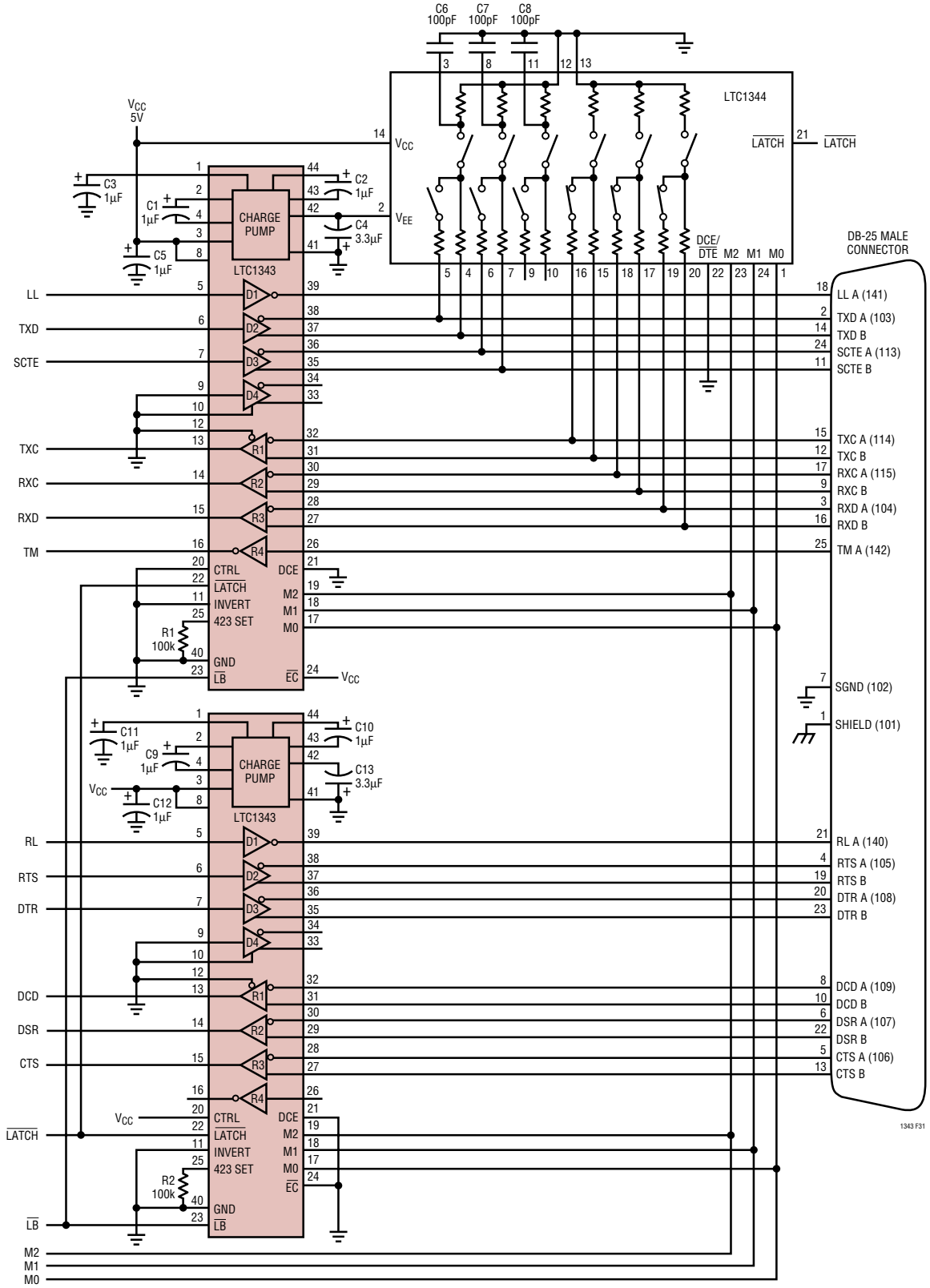

Figure 31: Controller-Selectable Multiprotocol DTE Port with DB-25 Connector

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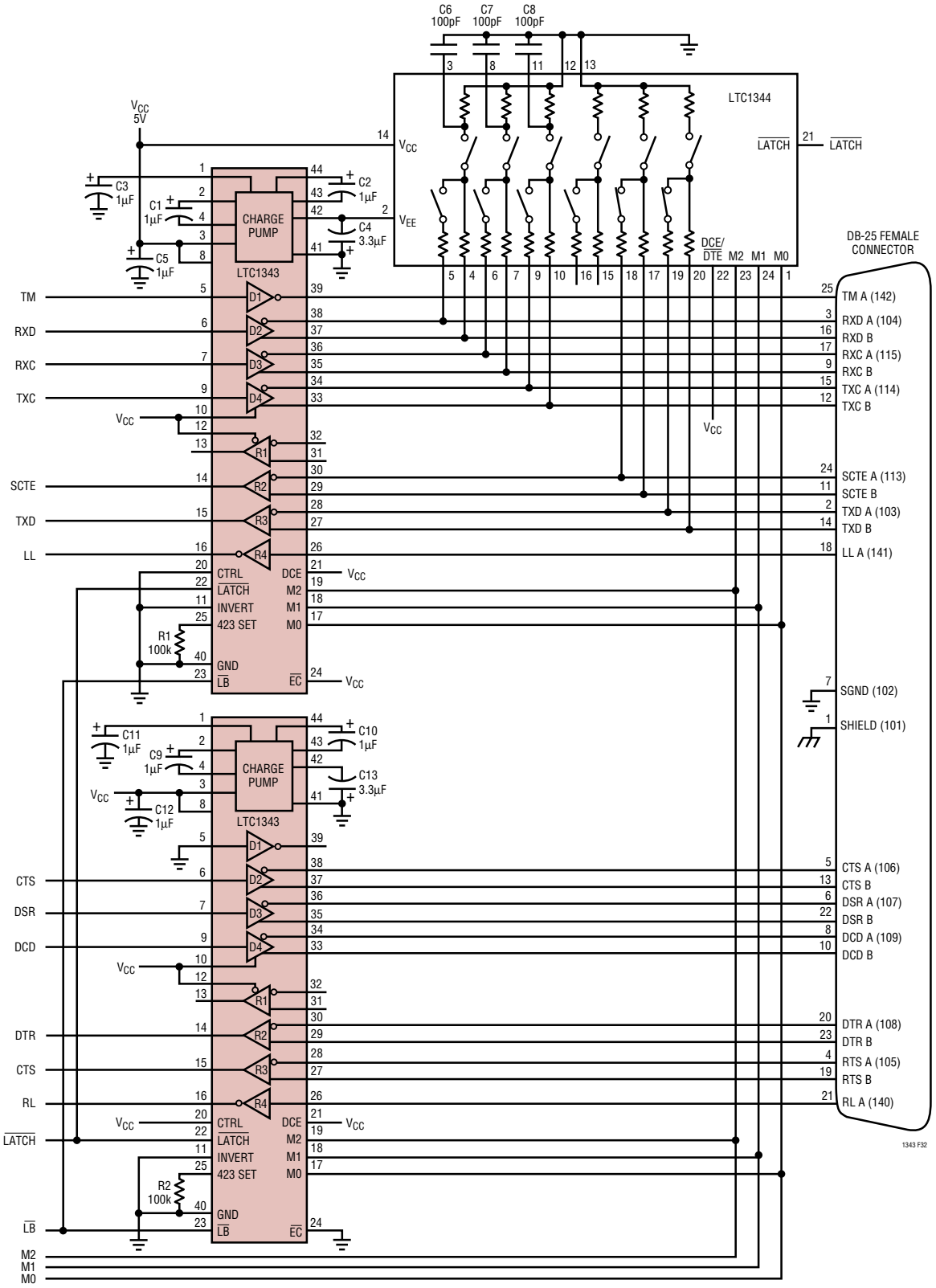

Figure 32: Controller-Selectable Multiprotocol DCE Port with DB-25 Connector

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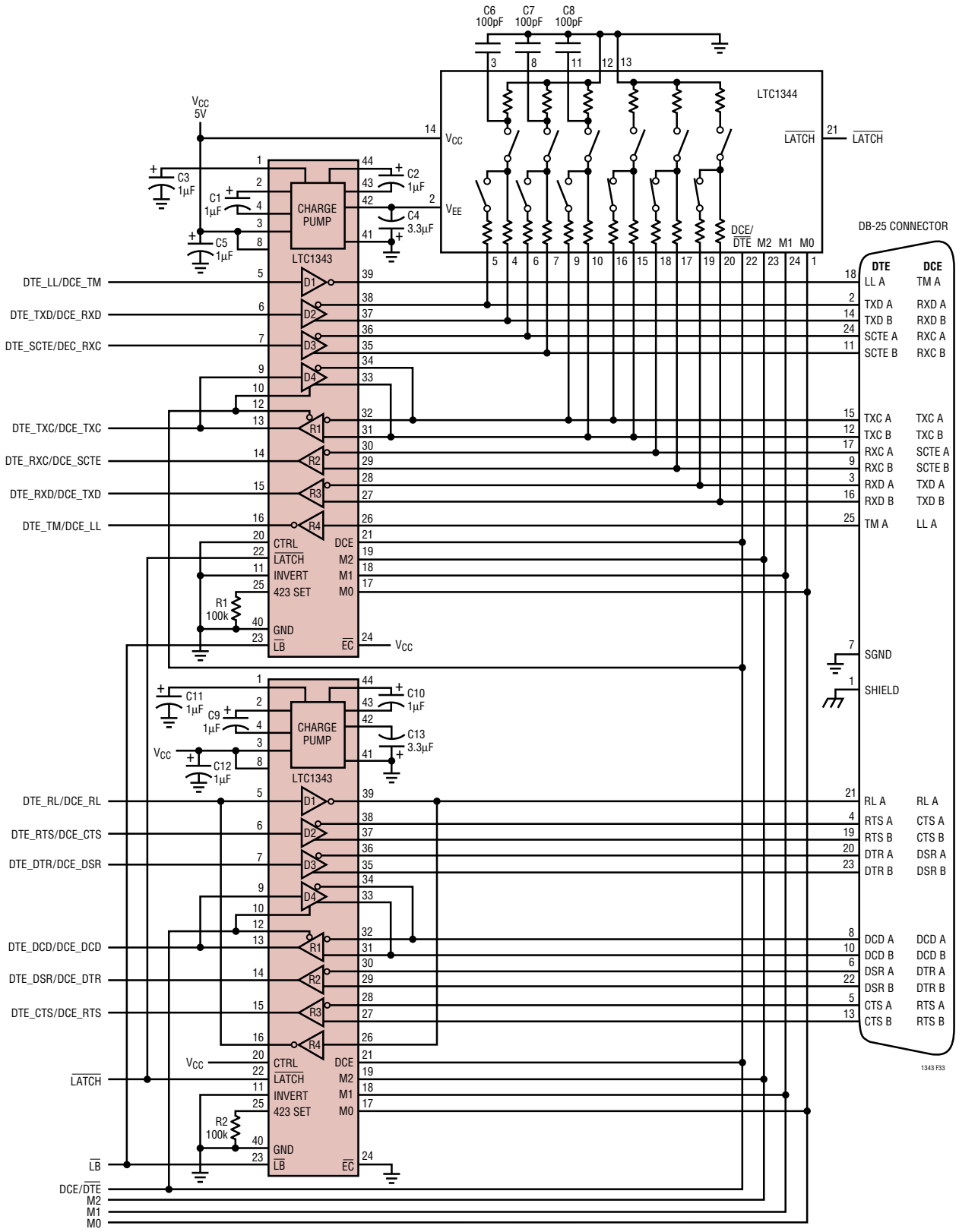


Figure 33. Controller-Selectable Multiprotocol DTE/DCE Port with DB-25 Connector

APPLICATIONS INFORMATION

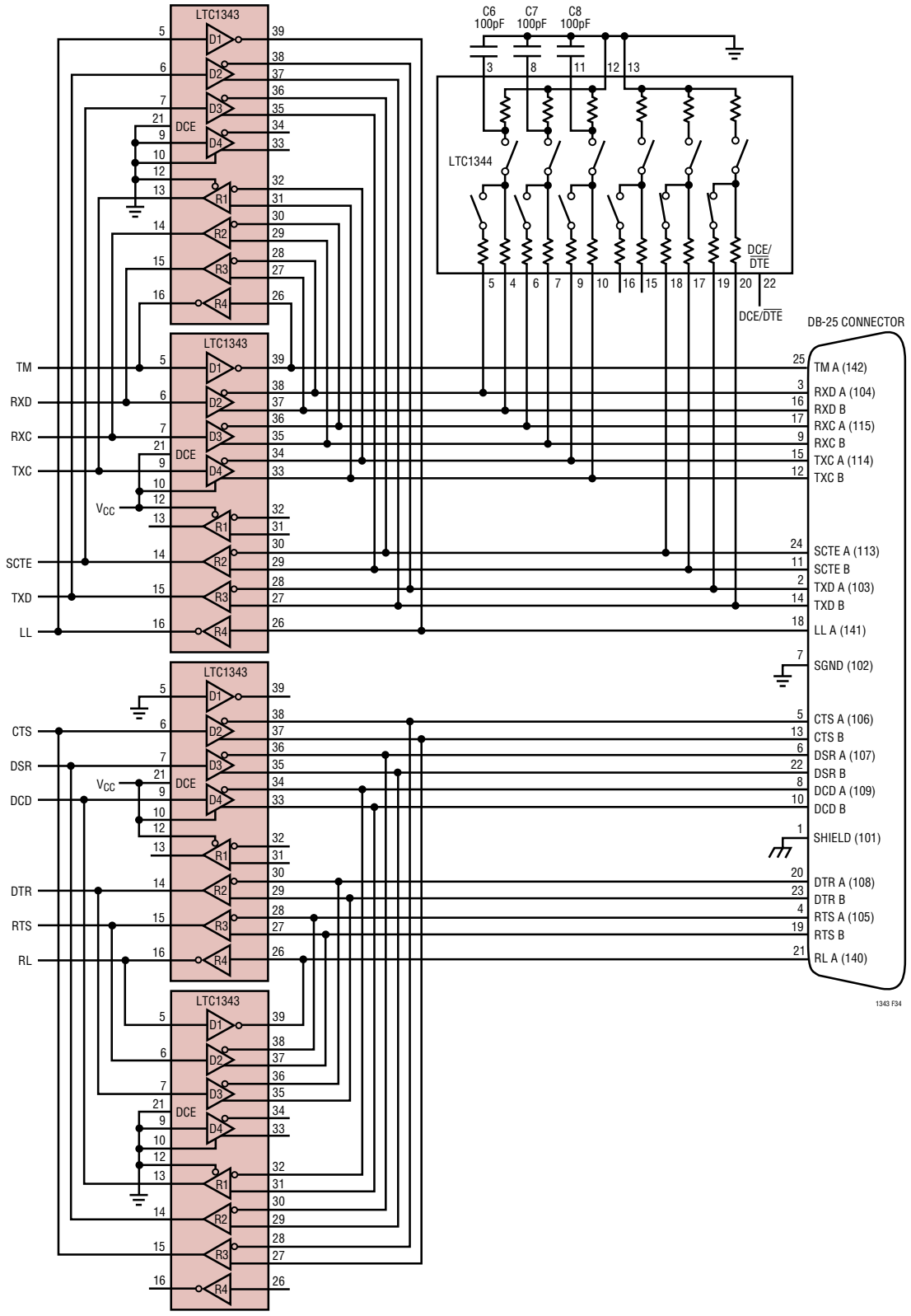


Figure 34. Controller-Selectable Multiprotocol DTE/DCE Port with DB-25

APPLICATIONS INFORMATION

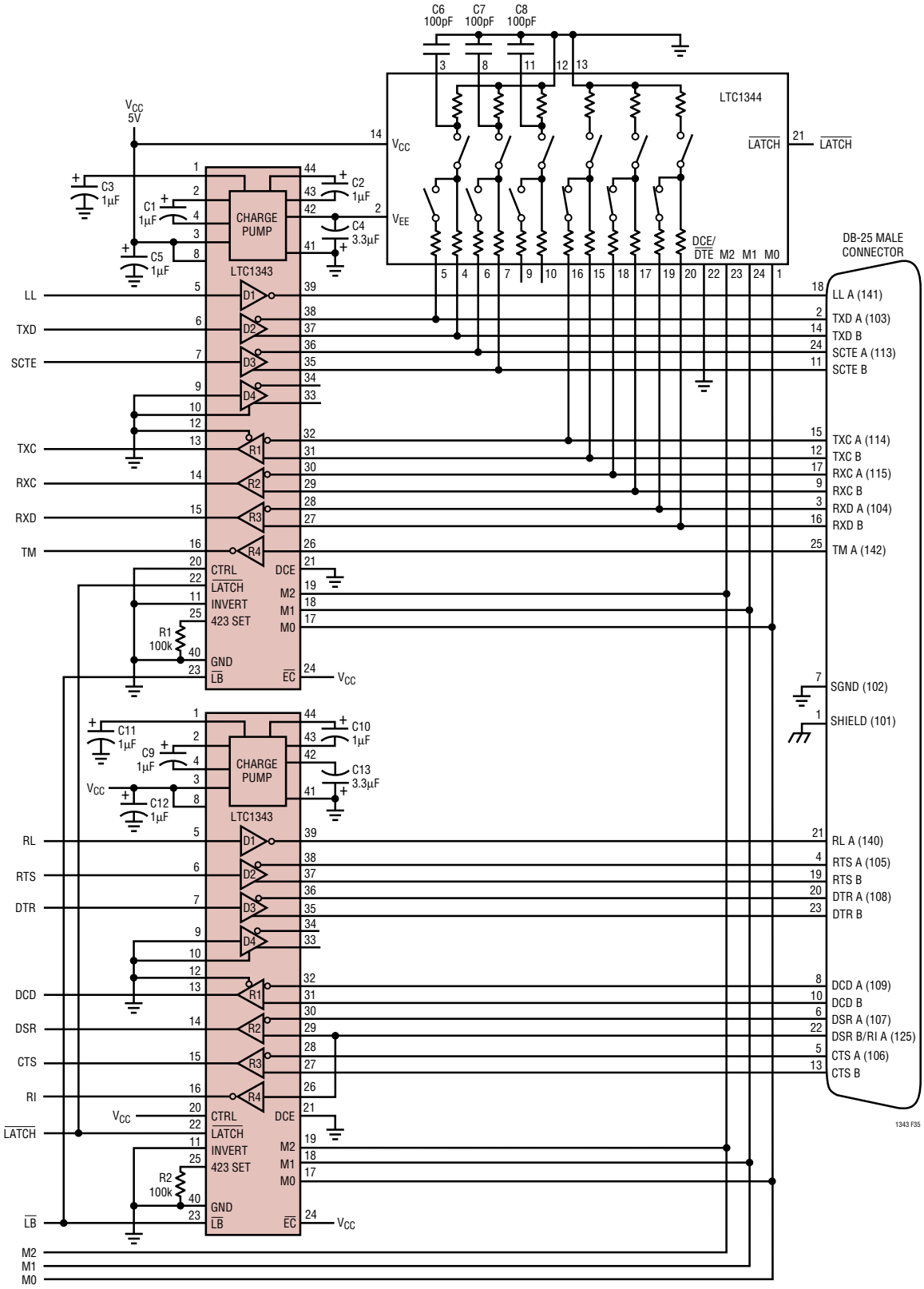


Figure 35. Controller-Selectable Multiprotocol DTE Port with RI and DB-25 Connector

APPLICATIONS INFORMATION

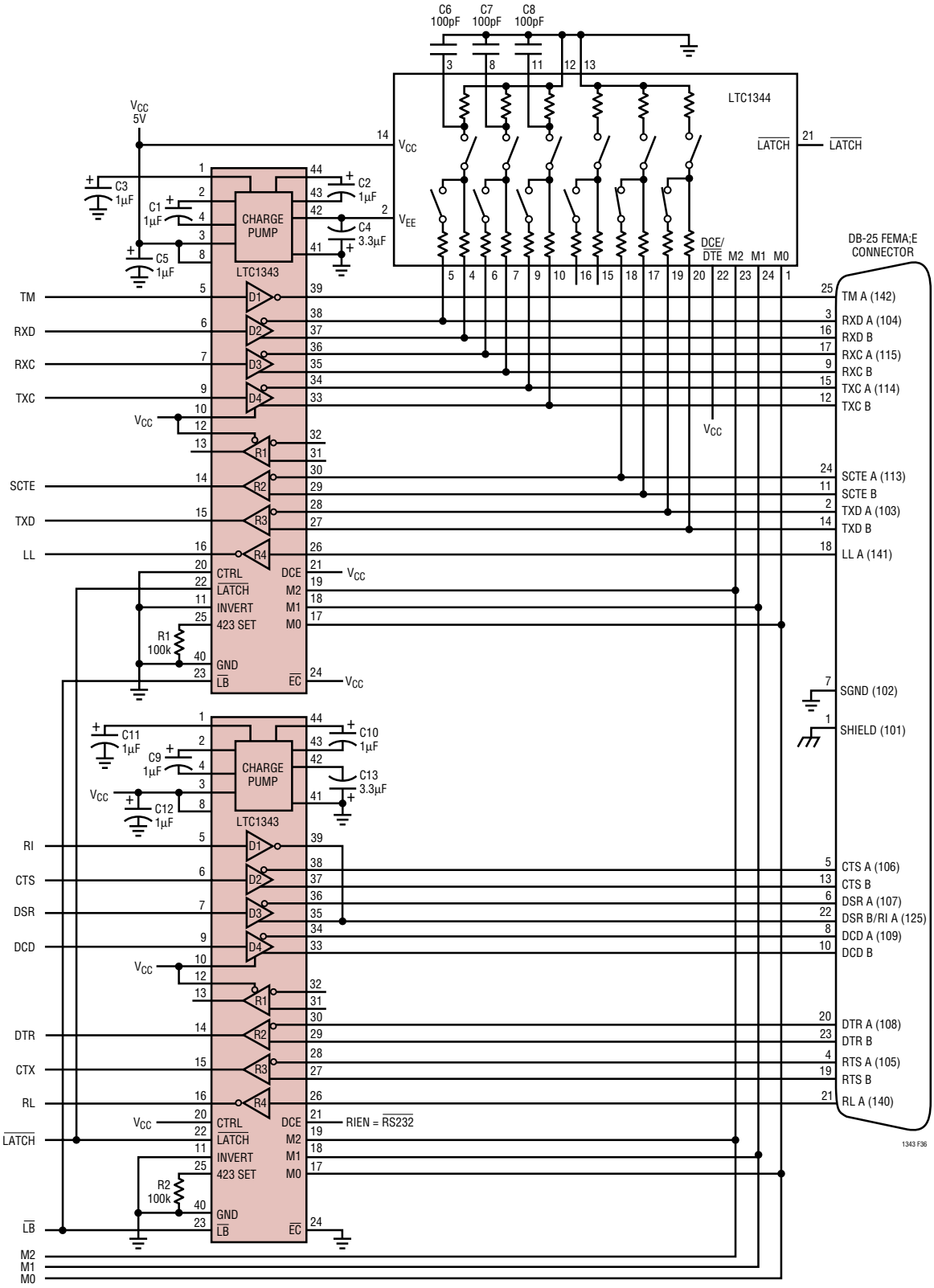
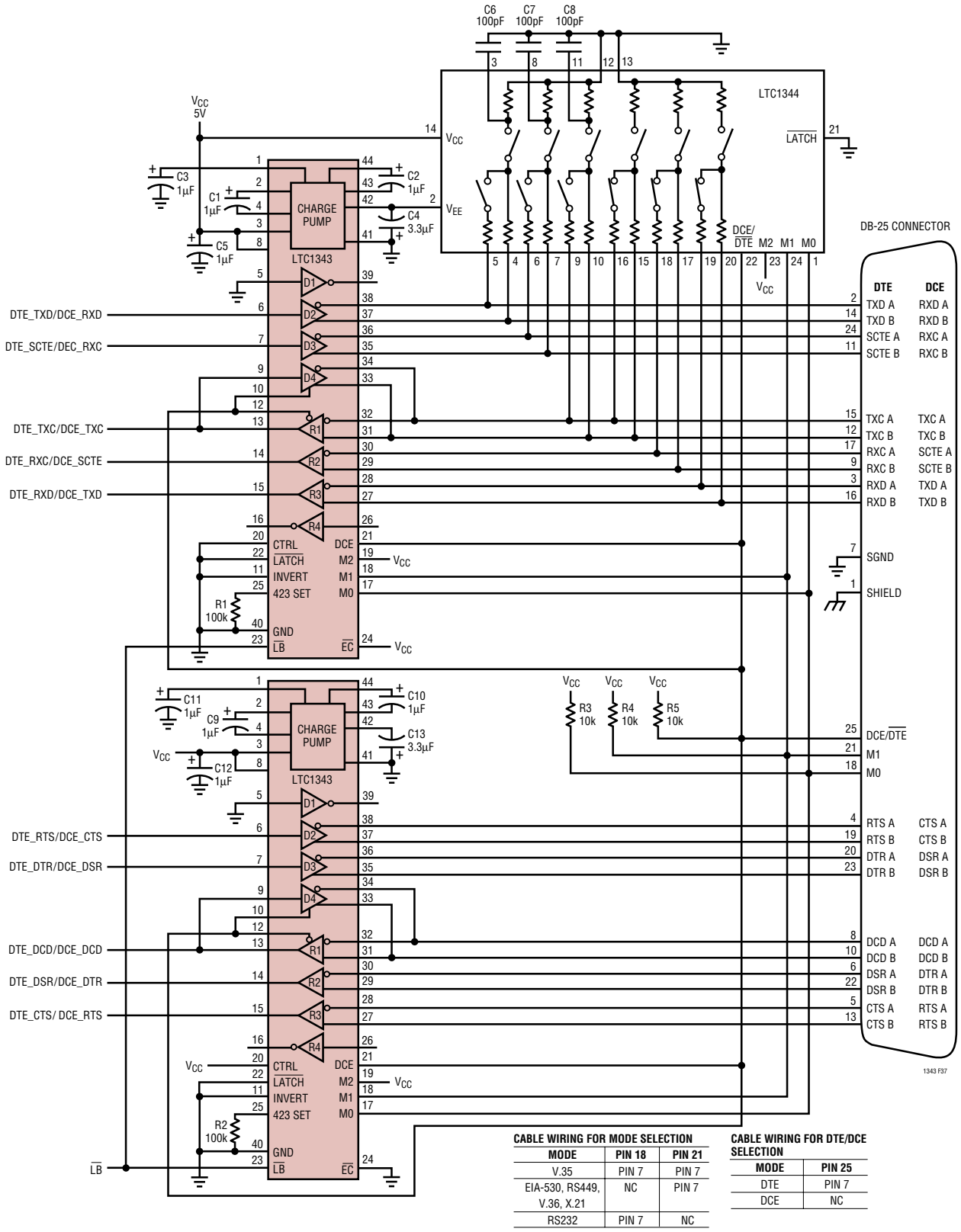


Figure 36. Controller-Selectable Multiprotocol DCE Port with RI and DB-25 Connector

APPLICATIONS INFORMATION



CABLE WIRING FOR MODE SELECTION

MODE	PIN 18	PIN 21
V.35	PIN 7	PIN 7
EIA-530, RS449, V.36, X.21	NC	PIN 7
RS232	PIN 7	NC

CABLE WIRING FOR DTE/DCE SELECTION

MODE	PIN 25
DTE	PIN 7
DCE	NC

Figure 37. Cable-Selectable Multiprotocol DTE/DCE Port with DB-25 Connector

APPLICATIONS INFORMATION

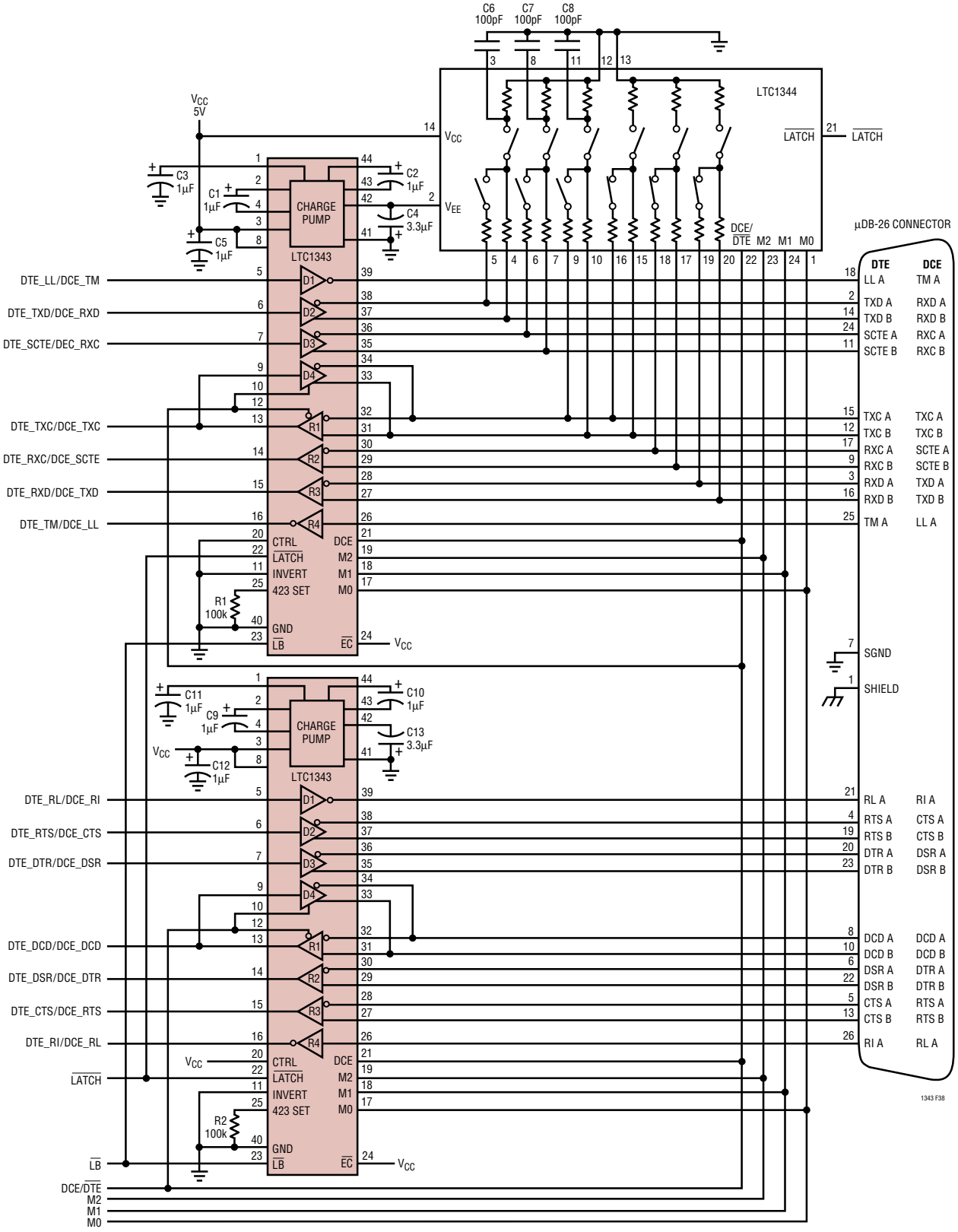
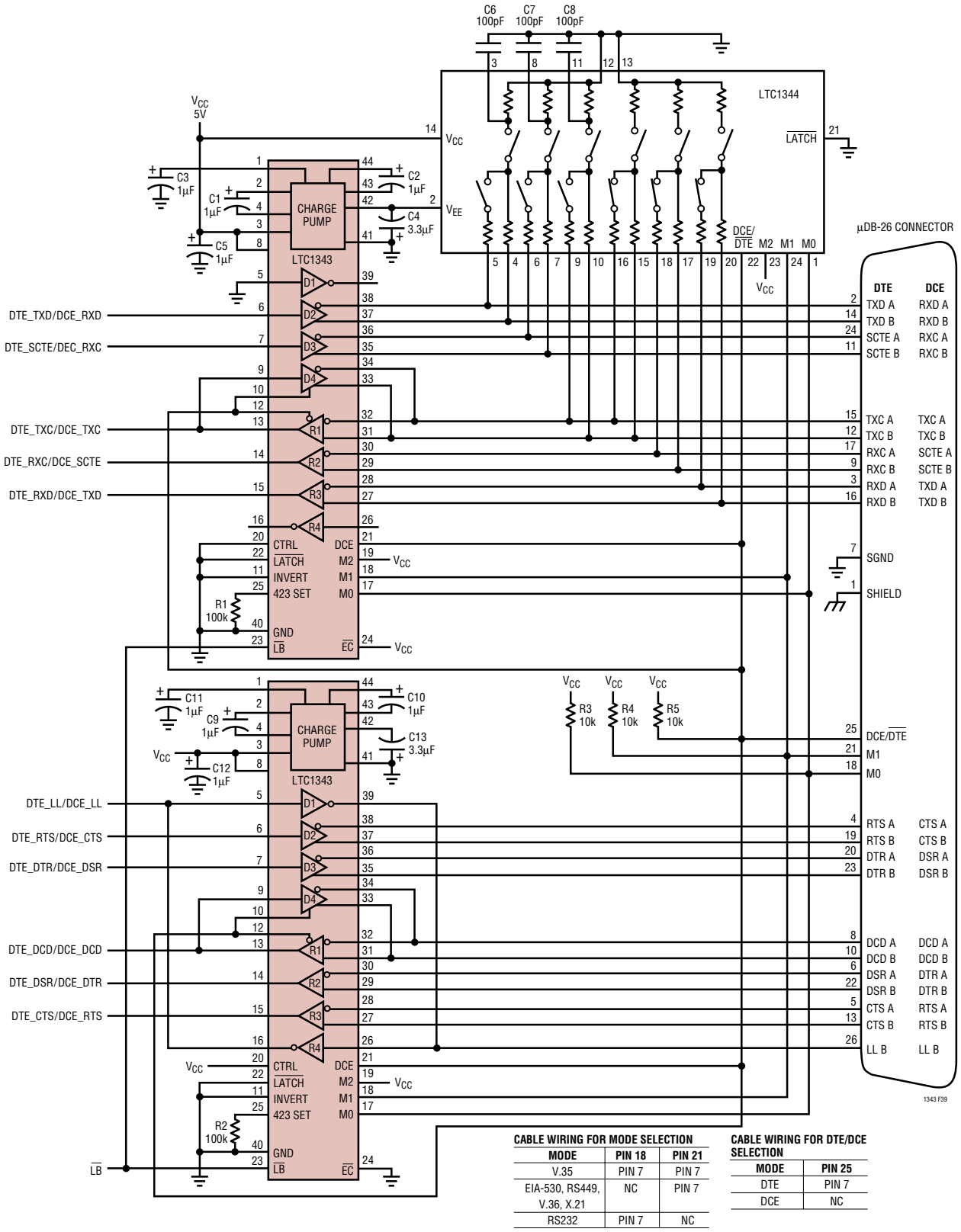


Figure 38. Controller-Selectable Multiprotocol DTE/DCE Port with DB-26 Connector

APPLICATIONS INFORMATION



CABLE WIRING FOR MODE SELECTION

MODE	PIN 18	PIN 21
V.35	PIN 7	PIN 7
EIA-530, RS449, V.36, X.21	NC	PIN 7
RS232	PIN 7	NC

CABLE WIRING FOR DTE/DCE SELECTION

MODE	PIN 25
DTE	PIN 7
DCE	NC

Figure 39. Cable-Selectable Multiprotocol DTE Port with DB-26 Connector