Single Supply V.35 Transceiver

FEATURES

- **Single Chip Provides All V.35 Differential Clock and Data Signals**
- **Operates From Single 5V Supply**
- **Software Selectable DTE or DCE Configuration**
- **Transmitters and Receivers Will Withstand Repeated ±10kV ESD Pulses**
- Shutdown Mode Reduces I_{CC} to 1µA Typ
- 10MBaud Transmission Rate
- Transmitter Maintains High Impedance When Disabled, Shut Down, or with Power Off
- Meets CCITT V.35 Specification
- Transmitters are Short-Circuit Protected

APPLICATIONS

- Modems
- Telecommunications
- Data Routers

DESCRIPTION

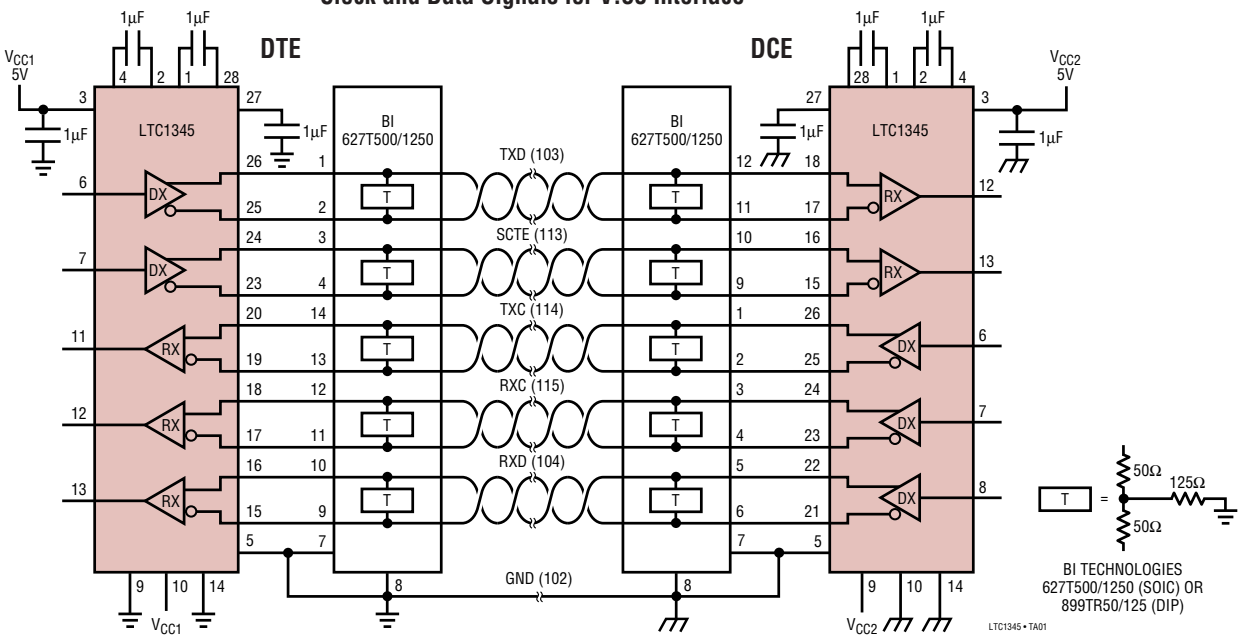
The LTC®1345 is a single chip transceiver that provides the differential clock and data signals for a V.35 interface from a single 5V supply. Combined with an external resistor termination network and an LT®1134A RS232 transceiver for the control signals, the LTC1345 forms a complete low power DTE or DCE V.35 interface port operating from a single 5V supply.

The LTC1345 features three current output differential transmitters, three differential receivers, and a charge pump. The transceiver can be configured for DTE or DCE operation or shut down using two Select pins. In the Shutdown mode, the supply current is reduced to 1µA.

The transceiver operates up to 10Mbaud. All transmitters feature short-circuit protection and a Receiver Output Enable pin allows the receiver outputs to be forced into a high impedance state. Both transmitter outputs and receiver inputs feature ±10kV ESD protection. The charge pump features a regulated V_{EE} output using three external 1µF capacitors.

TYPICAL APPLICATION

Clock and Data Signals for V.35 Interface



ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage, V_{CC} 6V

Input Voltage

Transmitters ..... −0.3V to (V_{CC} + 0.3V)

Receivers ..... −18V to 18V

S1, S2, OE ..... −0.3V to (V_{CC} + 0.3V)

Output Voltage

Transmitters ..... −18V to 18V

Receivers ..... −0.3V to (V_{CC} + 0.3V)

V_{EE} ..... −10V to 0.3V

Short-Circuit Duration

Transmitter Output ..... Indefinite

Receiver Output ..... Indefinite

V_{EE} ..... 30 sec

Operating Temperature Range

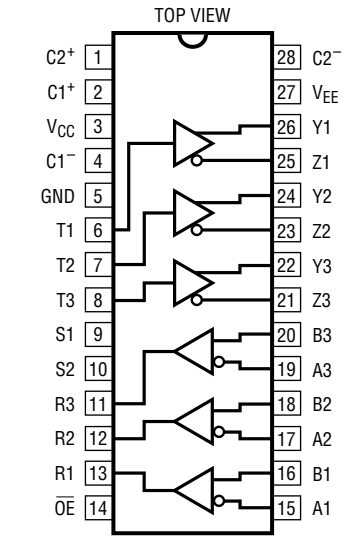
Commercial ..... 0°C to 70°C

Industrial ..... −40°C to 85°C

Storage Temperature Range ..... −65°C to 150°C

Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



NW PACKAGE
28-LEAD PDIP

SW PACKAGE
28-LEAD PLASTIC SO

THREE V.35 TRANSMITTERS AND THREE RECEIVERS

T_{JMAX} = 125°C, θ_{JA} = 56°C/W (NW)
T_{JMAX} = 125°C, θ_{JA} = 65°C/W (SW)

ORDER PART NUMBER
LTC1345CNW
LTC1345CSW
LTC1345INW
LTC1345ISW

Consult factory for Military grade parts.

DC ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 5V ±5% (Notes 2, 3), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OD}	Transmitter Differential Output Voltage	Figure 1, −4V ≤ V_{OS} ≤ 4V	●	0.44	0.55	0.66	V
V_{OC}	Transmitter Common-Mode Output Voltage	Figure 1, V_{OS} = 0V	●	−0.6	0	0.6	V
I_{OH}	Transmitter Output High Current	$V_{Y, Z}$ = 0V	●	−12.6	−11	−9.4	mA
I_{OL}	Transmitter Output Low Current	$V_{Y, Z}$ = 0V	●	9.4	11	12.6	mA
I_{OZ}	Transmitter Output Leakage Current	S1 = S2 = 0V, −5V ≤ $V_{Y, Z}$ ≤ 5V	●		±1	±100	µA
R_O	Transmitter Output Impedance	−2V ≤ $V_{Y, Z}$ ≤ 2V			100		kΩ
V_{TH}	Differential Receiver Input Threshold Voltage	−7V ≤ (V_A + V_B)/2 ≤ 7V	●		25	200	mV
ΔV_{TH}	Receiver Input Hysterisis	−7V ≤ (V_A + V_B)/2 ≤ 7V			50		mV
I_{IN}	Receiver Input Current (A, B)	−7V ≤ $V_{A, B}$ ≤ 7V	●			0.4	mA
R_{IN}	Receiver Input Impedance	−7V ≤ $V_{A, B}$ ≤ 7V	●	17.5	30		kΩ
V_{OH}	Receiver Output High Voltage	I_O = 4mA, $V_{B, A}$ = 0.2V	●	3	4.5		V
V_{OL}	Receiver Output Low Voltage	I_O = 4mA, $V_{B, A}$ = −0.2V	●		0.2	0.4	V
I_{OSR}	Receiver Output Short-Circuit Current	0V ≤ V_O ≤ V_{CC}	●	7		85	mA
I_{OZR}	Receiver Three-State Output Current	S1 = S2 = 0V, 0V ≤ V_O ≤ V_{CC}	●			±10	µA
V_{IH}	Logic Input High Voltage	T, S1, S2, $\overline{OE}$	●	2			V
V_{IL}	Logic Input Low Voltage	T, S1, S2, $\overline{OE}$	●			0.8	V
I_{IN}	Logic Input Current	T, S1, S2, $\overline{OE}$	●			±10	µA
I_{CC}	V_{CC} Supply Current	Figure 1, V_{OS} = 0, S1 = S2 = HIGH No Load, S1 = S2 = HIGH Shutdown, S1 = S2 = 0V	● ● ●		118 19 1	170 30 100	mA mA µA
V_{EE}	V_{EE} Voltage	No Load, S1 = S2 = HIGH			−5.5		V

AC ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 5V ±5% (Notes 2, 3), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_R, t_F	Transmitter Rise or Fall Time	Figures 1 and 3, V_{OS} = 0V	●		7	40	ns
t_{PLH}	Transmitter Input to Output ↑	Figures 1 and 3, V_{OS} = 0V	●		25	70	ns
t_{PHL}	Transmitter Input to Output ↓	Figures 1 and 3, V_{OS} = 0V	●		25	70	ns
t_{SKEW}	Transmitter Output to Output	Figures 1 and 3, V_{OS} = 0V			0		ns
t_{PLH}	Receiver Input to Output ↑	Figures 1 and 4, V_{OS} = 0V	●		49	100	ns
t_{PHL}	Receiver Input to Output ↓	Figures 1 and 4, V_{OS} = 0V	●		52	100	ns
t_{SKEW}	Differential Receiver Skew, $t_{PLH} - t_{PHL}$	Figures 1 and 4, V_{OS} = 0V			3		ns
t_{ZL}	Receiver Enable to Output LOW	Figures 2 and 5, C_L = 15pF, S1 Closed	●		40	70	ns
t_{ZH}	Receiver Enable to Output HIGH	Figures 2 and 5, C_L = 15pF, S2 Closed	●		35	70	ns
t_{LZ}	Receiver Disable From LOW	Figures 2 and 5, C_L = 15pF, S1 Closed	●		30	70	ns
t_{HZ}	Receiver Disable From HIGH	Figures 2 and 5, C_L = 15pF, S2 Closed	●		35	70	ns
f_{OSC}	Charge Pump Oscillator Frequency				200		kHz
BR_{MAX}	Maximum Data Rate (Note 4)		●	10	15		Mbaud

Note 1: The absolute maximum ratings are those values beyond which the safety of the device cannot be guaranteed.

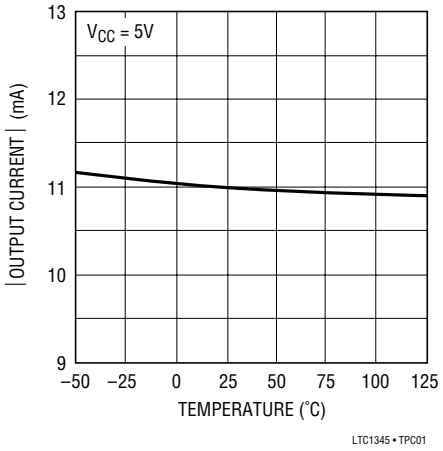
Note 2: All currents into device pins are termed positive; all currents out of device pins are termed negative. All voltages are referenced to device ground unless otherwise specified.

Note 3: All typicals are given for V_{CC} = 5V, C1 = C2 = C3 = 1µF ceramic capacitors and T_A = 25°C.

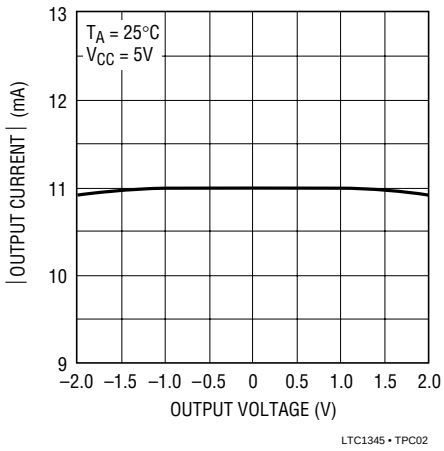
Note 4: Maximum data rate is specified for NRZ data encoding scheme. The maximum data rate may be different for other data encoding schemes. Data rate is guaranteed by correlation and is not tested.

TYPICAL PERFORMANCE CHARACTERISTICS

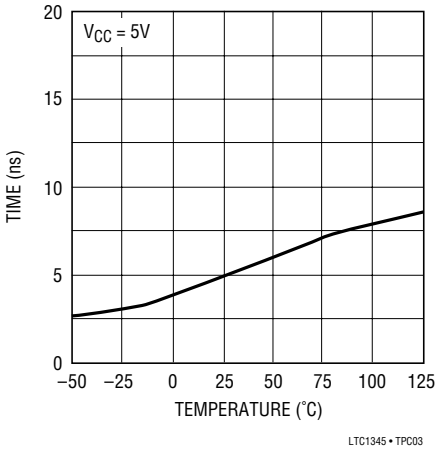
Transmitter Output Current vs Temperature



Transmitter Output Current vs Output Voltage

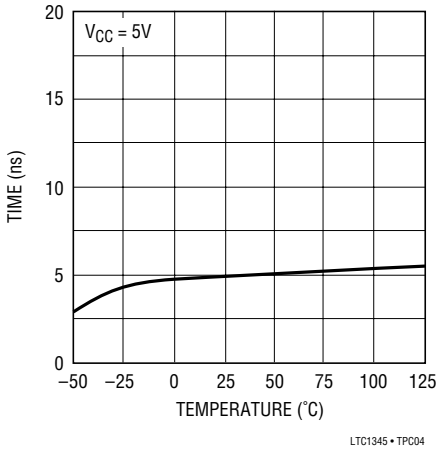


Transmitter Output Skew vs Temperature



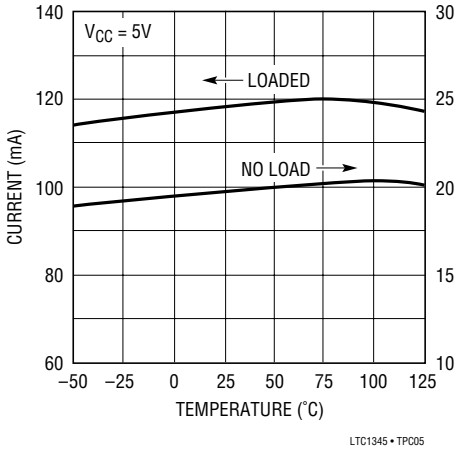
TYPICAL PERFORMANCE CHARACTERISTICS

Receiver $|t_{PLH} - t_{PHL}|$ vs Temperature



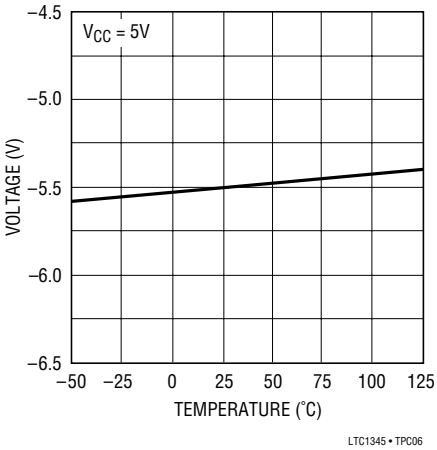
LTC1345 • TPC04

Supply Current vs Temperature



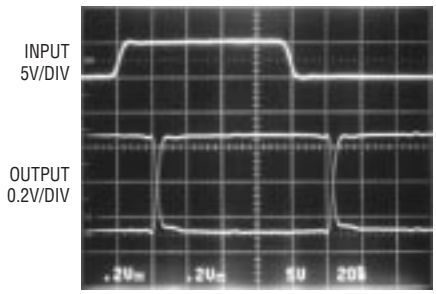
LTC1345 • TPC05

V_{EE} Voltage vs Temperature



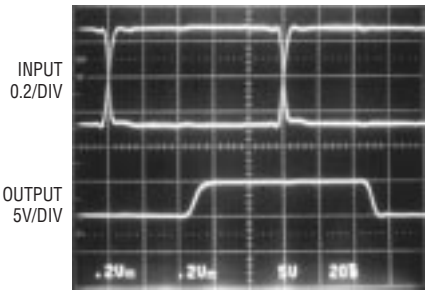
LTC1345 • TPC06

Transmitter Output Waveforms



LTC1345 • TPC07

Receiver Output Waveforms



LTC1345 • TPC08

PIN FUNCTIONS

$C2^+$ (Pin 1): Capacitor C2 Positive Terminal.

$C1^+$ (Pin 2): Capacitor C1 Positive Terminal.

V_{CC} (Pin 3): Positive Supply, $4.75 \leq V_{CC} \leq 5.25V$.

$C1^-$ (Pin 4): Capacitor C1 Negative Terminal.

GND (Pin 5): Ground. The positive terminal of C3 is connected to ground.

T1 (Pin 6): Transmitter 1 Input.

T2 (Pin 7): Transmitter 2 Input.

T3 (Pin 8): Transmitter 3 Input.

S1 (Pin 9): Select Input 1.

S2 (Pin 10): Select Input 2.

R3 (Pin 11): Receiver 3 Output.

R2 (Pin 12): Receiver 2 Output.

R1 (Pin 13): Receiver 1 Output.

$\overline{OE}$ (Pin 14): Receiver Output Enable.

A1 (Pin 15): Receiver 1 Inverting Input.

B1 (Pin 16): Receiver 1 Noninverting Input.

A2 (Pin 17): Receiver 2 Inverting Input.

B2 (Pin 18): Receiver 2 Noninverting Input.

A3 (Pin 19): Receiver 3 Inverting Input.

B3 (Pin 20): Receiver 3 Noninverting Input.

Z3 (Pin 21): Transmitter 3 Inverting Output.

PIN FUNCTIONS

Y3 (Pin 22): Transmitter 3 Noninverting Output.

Z2 (Pin 23): Transmitter 2 Inverting Output.

Y2 (Pin 24): Transmitter 2 Noninverting Output

Z1 (Pin 25): Transmitter 1 Inverting Output.

Y1 (Pin 26): Transmitter 1 Noninverting Output.

V_{EE} (Pin 27): Charge Pump Output. Connected to negative terminal of capacitor C3.

$C2^-$ (Pin 28): Capacitor C2 Negative Terminal.

FUNCTION TABLES

Transmitter and Receiver Configuration

S1	S2	TX#	RX#	REMARKS
0	0	—	—	Shutdown
1	0	1, 2, 3	1, 2	DCE Mode, RX3 Shut Down
0	1	1, 2	1, 2, 3	DTE Mode, TX3 Shut Down
1	1	1, 2, 3	1, 2, 3	All Active

Transmitter

	INPUTS			OUTPUTS			
CONFIGURATION	S1	S2	T	Y1 AND Y2	Z1 AND Z2	Y3	Z3
DTE	0	1	0	0	1	Z	Z
DTE	0	1	1	1	0	Z	Z
DCE or All ON	1	X	0	0	1	0	1
DCE or All ON	1	X	1	1	0	1	0
Shutdown	0	0	X	Z	Z	Z	Z

Receiver

	INPUTS				OUTPUTS	
CONFIGURATION	S1	S2	$\overline{OE}$	B – A	R1 AND R2	R3
DTE or All ON	X	1	0	≥0.2V	1	1
DTE or All ON	X	1	0	≤–0.2V	0	0
DCE	1	0	0	≥0.2V	1	Z
DCE	1	0	0	≤–0.2V	0	Z
Disabled	X	X	1	X	Z	Z
Shutdown	0	0	X	X	Z	Z

TEST CIRCUITS

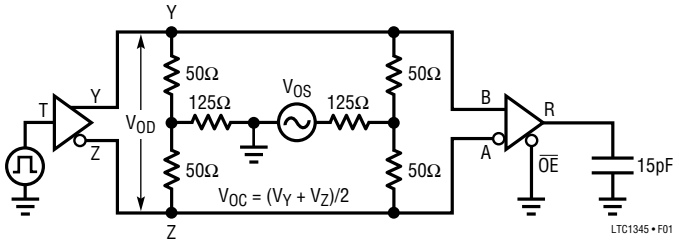


Figure 1. V.35 Transmitter/Receiver Test Circuit

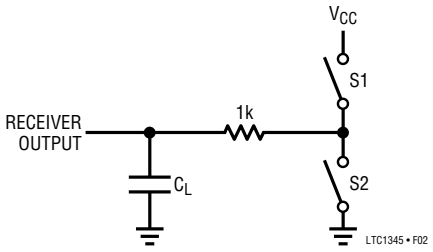


Figure 2. Receiver Output Enable/Disable Timing Test Load

SWITCHING TIME WAVEFORMS

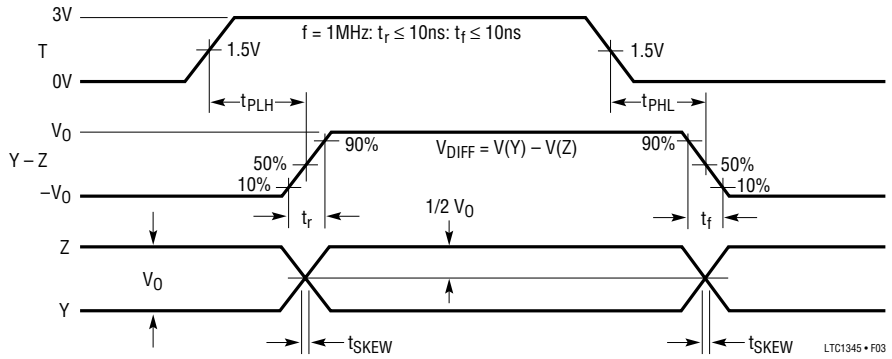


Figure 3. V.35 Transmitter Propagation Delays

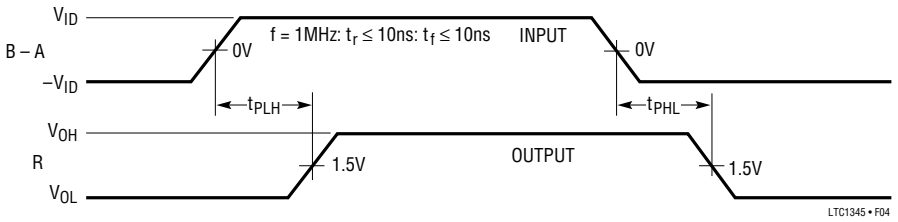


Figure 4. V.35 Receiver Propagation Delays

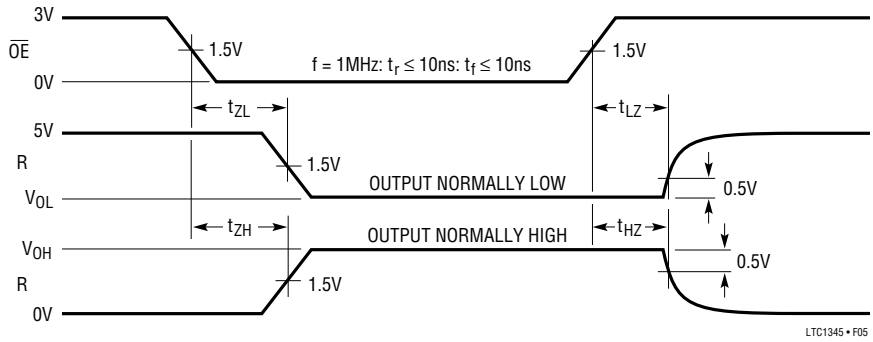


Figure 5. Receiver Enable and Disable Times

APPLICATIONS INFORMATION

Review of CCITT Recommendation V.35 Electrical Specifications

V.35 is a CCITT recommendation for synchronous data transmission via modems. Appendix 2 of the recommendation describes the electrical specifications which are summarized below:

1. The interface cable is balanced twisted-pair with 80Ω to 120Ω impedance.

2. The transmitter's source impedance is between 50Ω and 150Ω.

3. The transmitter's resistance between shorted terminals and ground is 150Ω ±15Ω.

4. When terminated by a 100Ω resistive load, the terminal-to-terminal voltage should be 0.55V ±20%.

5. The transmitter's rise time should be less than 1% of the signal pulse or 40ns, whichever is greater.

6. The common-mode voltage at the transmitter output should not exceed 0.6V.

7. The receiver impedance is 100Ω ±10Ω.

8. The receiver impedance to ground is 150Ω ±15Ω.

9. The transmitter or receiver should not be damaged by connection to earth ground, short-circuiting, or cross connection to other lines.

10. No data errors should occur with ±2V common-mode change at either the transmitter or receiver, or ±4V ground potential difference between transmitter and receiver.

Cable Termination

Each end of the cable connected to an LTC1345 must be terminated by either one of two electrically equivalent external Y or Δ resistor networks for proper operation. The Y-termination has two series connected 50Ω resistors and a 125Ω resistor connected between ground and the center tap of the two 50Ω resistors as shown in Figure 6A.

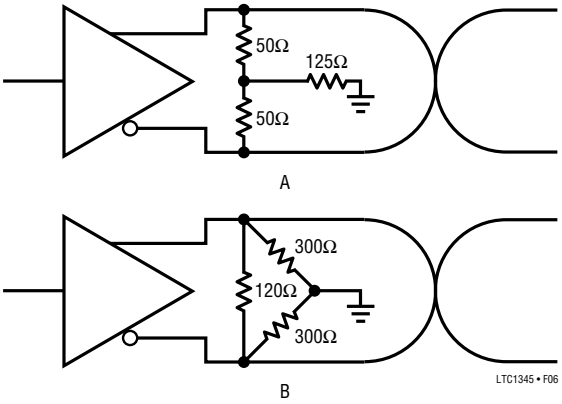


Figure 6. Y and Δ Termination Networks

The alternative Δ-termination has a 120Ω resistor across the twisted wires and two 300Ω resistors between each wire and ground as shown in Figure 6B. Standard 1/8W, 5% surface mount resistors can be used for the termination network. To maintain the proper differential output swing, the resistor tolerance must be 5% or less. A termination network that combines all the resistors into an SO-14 package is available from:

BI Technologies (Formerly Beckman Industrial)
Resistor Networks
4200 Bonita Place
Fullerton, CA 92635
Phone: (714) 447-2357
FAX: (714) 447-2500
Part #: BI Technologies 627T500/1250 (SOIC)
899TR50/125 (DIP)

APPLICATIONS INFORMATION

Theory of Operation

The transmitter output consists of complementary switched-current sources as shown in Figure 7.

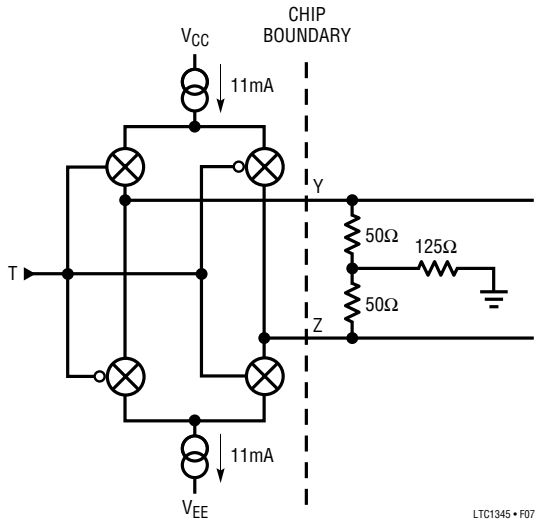


Figure 7. Simplified Transmitter Schematic

With a logic zero at the transmitter input, the inverting output Z sources 11mA and the noninverting output Y sinks 11mA. The differential transmitter output voltage is then set by the termination resistors. With two differential 50Ω resistors at each end of the cable, the voltage is set to (50Ω × 11mA) = 0.55V. With a logic 1 at the transmitter input, output Z sinks 11mA and Y sources 11mA. The common-mode voltage of Y and Z is 0V when both current sources are matched and there is no ground potential difference between the cable terminations. The transmitter current sources have a common-mode range of ±2V, which allows for a ground difference between cable terminations of ±4V.

Each receiver input has a 30k resistance to ground and requires external termination to meet the V.35 input impedance specification. The receivers have an input hysteresis of 50mV to improve noise immunity. The receiver output may be forced into a high impedance state by pulling the output enable ($\overline{OE}$) pin high. For normal operation $\overline{OE}$ should be pulled low.

A charge pump generates the regulated negative supply voltage (V_{EE}) with three 1μF capacitors. Commutating capacitors C1 and C2 form a voltage doubler and inverter while C3 acts as a reservoir capacitor. To insure proper operation, the capacitors must have an ESR less than 1Ω. Monolithic ceramic or solid tantalum capacitors are good choices. Under light loads, regulation at about –5.2V is provided by a pulse-skipping scheme. Under heavy loads the charge pump is on continuously. A small ripple of about 500mV will be present on V_{EE}.

Two Select pins, S1 and S2, configure the chip for DTE, DCE, all transmitters and receivers on, or Shutdown. In Shutdown mode, I_{CC} drops to 1μA. The outputs of the transmitters and receivers are in high impedance states, the charge pump stops and V_{EE} is clamped to ground.

ESD Protection

LTC1345 transmitter outputs and receiver inputs have on-chip protection from multiple ±10kV ESD transients. ESD testing is done using the Human Body ESD Model. ESD testing must be done with an AC ground on the V_{CC} and V_{EE} supply pins. The low ESR supply decoupling and V_{EE} reservoir capacitors provide this AC ground during normal operation.

Complete V.35 Port

Figure 8 shows the schematic of a complete surface mounted, single 5V DTE and DCE V.35 port using only three ICs and eight capacitors per port. The LTC1345 is used to transmit the clock and data signals, and the LT1134A to transmit the control signals. If test signals 140, 141, and 142 are not used, the transmitter inputs should be tied to V_{CC}.

APPLICATIONS INFORMATION

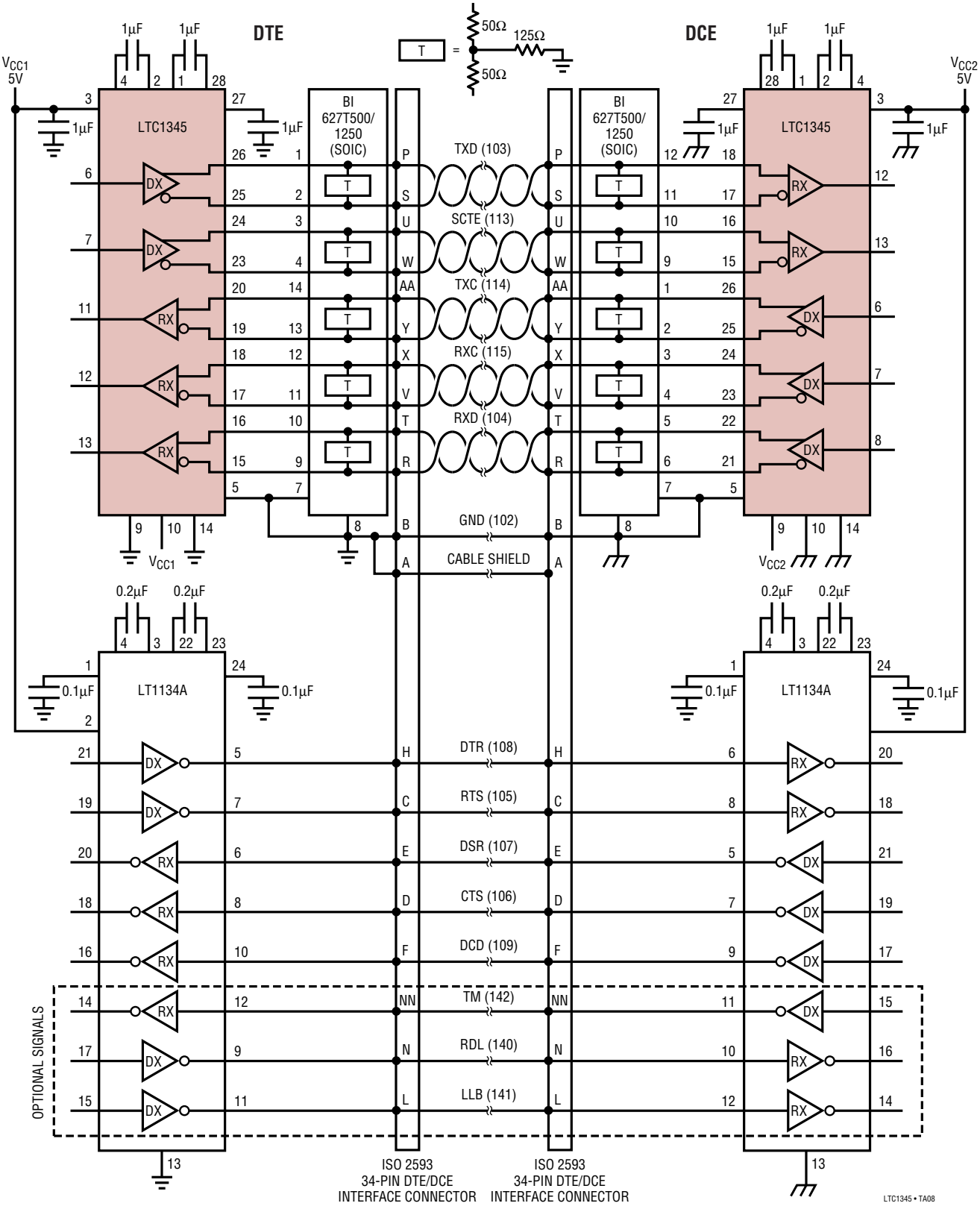


Figure 8. Complete Single 5V V.35 Interface

APPLICATIONS INFORMATION

RS422/RS485 Applications

The receivers on the LTC1345 are ideal for RS422 and RS485 applications. Using the test circuit in Figure 9, the LTC1345 receivers are able to successfully reconstruct the data stream with the common-mode voltage meeting RS422 and RS485 requirements (12V to –7V).

Figures 10 and 11 show that the LTC1345 receivers are very capable of reconstructing data at rates up to 10Mbaud.

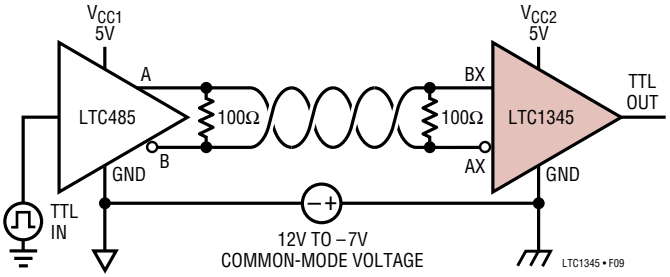


Figure 9 RS422/RS485 Receiver Interface

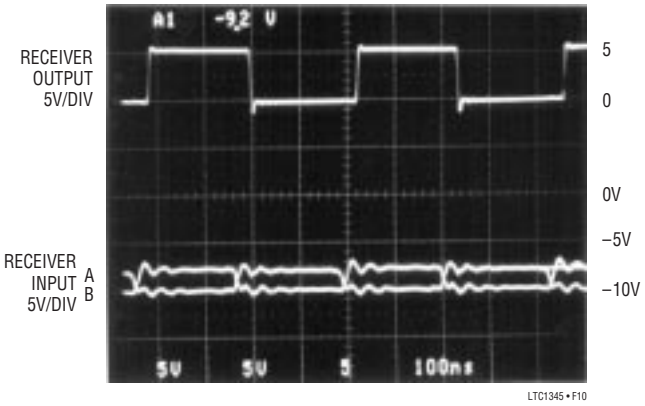


Figure 10. –7V Common Mode

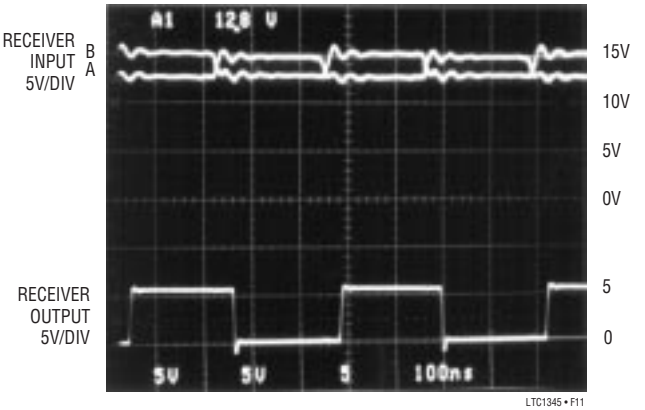
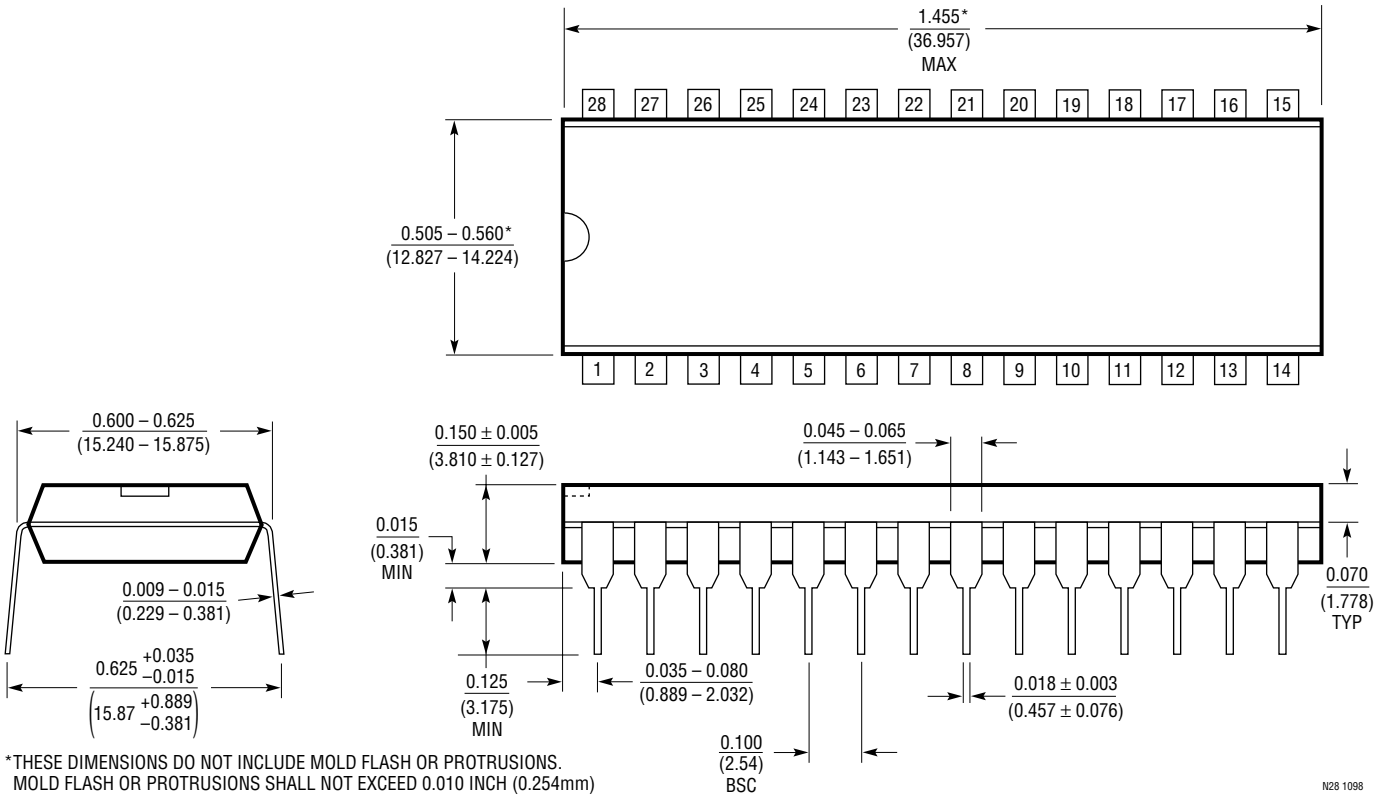


Figure 11. 12V Common Mode

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

NW Package
28-Lead PDIP (Wide 0.600)
(LTC DWG # 05-08-1520)



*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

N28 1098