# Dual PowerPath™ Switch Driver

## FEATURES

- **Power Path Management for Systems with Multiple DC Sources**
- **All N-Channel Switching to Reduce Power Losses and System Cost**
- Switches and Isolates Sources Up to 30V
- Adaptive High Voltage Step-Up Regulator for N-Channel Gate Drive
- Capacitor Inrush and Short-Circuit Current Limited
- User-Programmable Timer to Limit Switch Dissipation
- Small Footprint: 16-Pin Narrow SSOP

## APPLICATIONS

- Notebook Computers
- Portable Instruments
- Handi-Terminals
- Portable Medical Equipment
- Portable Industrial Control Equipment

## DESCRIPTION

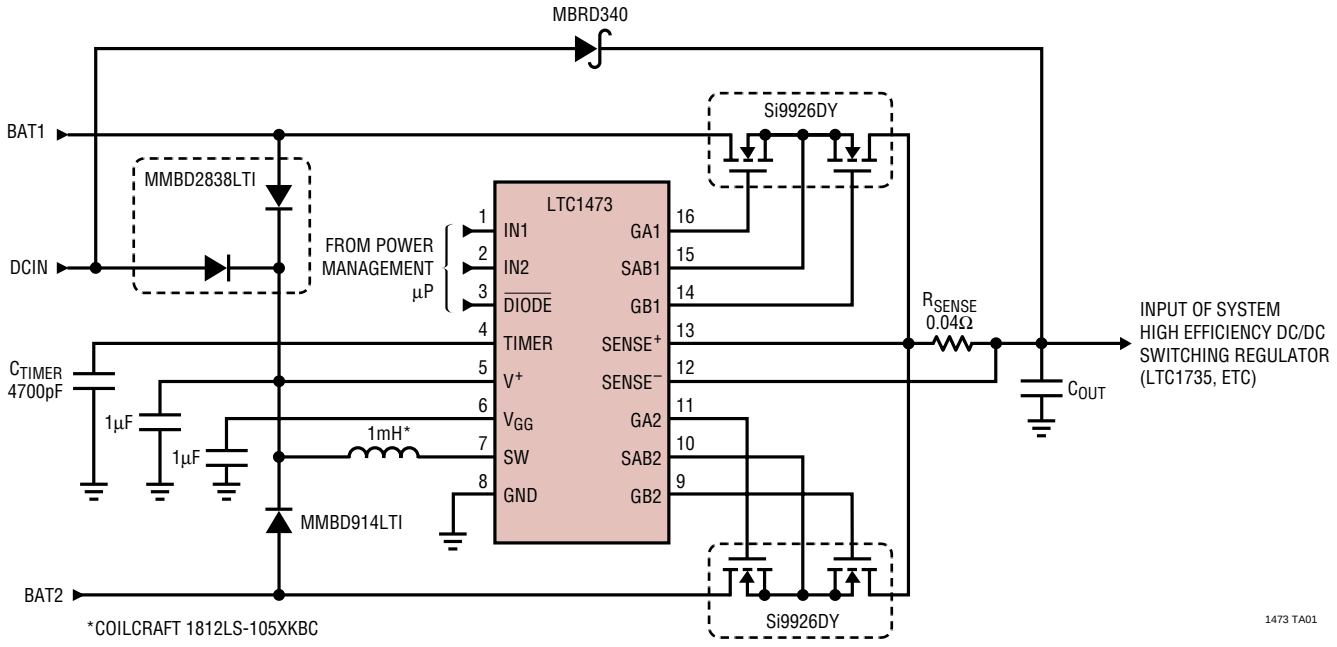
The LTC®1473 provides a power management solution for single and dual battery notebook computers and other portable equipment. The LTC1473 drives two sets of back-to-back N-channel MOSFET switches to route power to the input of the main system switching regulator. An internal boost regulator provides the voltage to fully enhance the logic level N-channel MOSFET switches.

The LTC1473 senses current to limit surge currents both into and out of the batteries and the system supply capacitor during switch-over transitions or during fault conditions. A user-programmable timer monitors the time the MOSFET switches are in current limit and latches them off when the programmed time is exceeded.

A unique “2-diode mode” logic ensures system start-up regardless of which input receives power first.



## TYPICAL APPLICATION

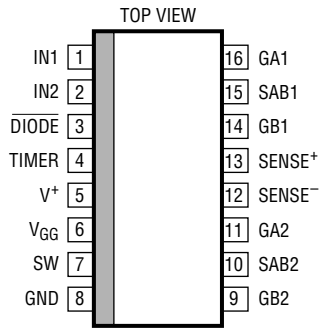


## ABSOLUTE MAXIMUM RATINGS

**(Note 1)**

DCIN, BAT1, BAT2 Supply Voltage ..... –0.3 to 32V
SENSE⁺, SENSE⁻, V⁺ ..... –0.3 to 32V
GA1, GB1, GA2, GB2 ..... –0.3 to 42V
SAB1, SAB2 ..... –0.3 to 32V
SW, $V_{GG}$ ..... –0.3 to 42V
IN1, IN2, $\overline{DIODE}$ ..... –0.3V to 7.5V
Junction Temperature (Note 2) ..... 125°C
Operating Temperature Range
  Commercial ..... 0°C to 70°C
  Industrial ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

## PACKAGE/ORDER INFORMATION




GN PACKAGE
16-LEAD NARROW PLASTIC SSOP
$T_{JMAX}$ = 125°C, $\theta_{JA}$ = 150°C/W

| ORDER PART NUMBER |
|---|
| LTC1473CGN<br>LTC1473IGN |
| **GN PART MARKING** |
| 1473<br>1473I |

Consult factory for Military grade parts.

## ELECTRICAL CHARACTERISTICS

**The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are $T_A$ = 25°C. Test circuit, V⁺ = 20V, unless otherwise specified.**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $V^+$ | Supply Operating Range | | | 4.75 | | 30 | V |
| $I_S$ | Supply Current | $V_{IN1} = V_{\overline{DIODE}} = 5V$, $V_{IN2} = 0V$, $V_{SENSE^+} = V_{SENSE^-} = 20V$ | ● | | 100 | 200 | µA |
| $V_{GS}$ | $V_{GS}$ Gate Supply Voltage | $V_{GS} = V_{GG} – V^+$ | ● | 7.5 | 8.5 | 9.5 | V |
| $V^+_{UVLO}$ | V⁺ Undervoltage Lockout Threshold | V⁺ Ramping Down | | 2.7 | 3.1 | 3.5 | V |
| $V^+_{UVLOHYS}$ | V⁺ Undervoltage Lockout Hysteresis | | | 0.75 | 1 | 1.25 | V |
| $V_{HIDIGIN}$ | Digital Input Logic High | | ● | 2 | 1.6 | | V |
| $V_{LODIGIN}$ | Digital Input Logic Low | | ● | | 1.5 | 0.8 | V |
| $I_{IN}$ | Input Current | $V_{IN1} = V_{IN2} = V_{\overline{DIODE}} = 5V$ | | | | ±1 | µA |
| $V_{GS(ON)}$ | Gate-to-Source ON Voltage | $I_{GA1} = I_{GA2} = I_{GB1} = I_{GB2} = –1µA$, $V_{SAB1} = V_{SAB2} = 20V$ | ● | 5.0 | 5.7 | 7.0 | V |
| $V_{GS(OFF)}$ | Gate-to-Source OFF Voltage | $I_{GA1} = I_{GA2} = I_{GB1} = I_{GB2} = 100µA$, $V_{SAB1} = V_{SAB2} = 20V$ | ● | | 0 | 0.4 | V |
| $I_{BSENSE^+}$ | SENSE⁺ Input Bias Current | $V_{SENSE^+} = V_{SENSE^-} = 20V$<br>$V_{SENSE^+} = V_{SENSE^-} = 0V$ (Note 3) | ●<br>● | 2<br>–300 | 4.5<br>–160 | 6.5<br>–100 | µA<br>µA |
| $I_{BSENSE^-}$ | SENSE⁻ Input Bias Current | $V_{SENSE^+} = V_{SENSE^-} = 20V$<br>$V_{SENSE^+} = V_{SENSE^-} = 0V$ (Note 3) | ●<br>● | 2<br>–300 | 4.5<br>–160 | 6.5<br>–100 | µA<br>µA |
| $V_{SENSE}$ | Inrush Current Limit Sense Voltage | $V_{SENSE^-} = 20V$ ($V_{SENSE^+} – V_{SENSE^-}$)<br>$V_{SENSE^-} = 0V$ ($V_{SENSE^+} – V_{SENSE^-}$) | ● | 0.15<br>0.10 | 0.20<br>0.20 | 0.25<br>0.30 | V<br>V |
| $I_{PDSAB}$ | SAB1, SAB2 Pull-Down Current | $V_{IN1} = V_{IN2} = V_{\overline{DIODE}} = 0.8V$<br>$V_{IN1} = V_{IN2} = 0.8V$, $V_{\overline{DIODE}} = 2V$ | | 5<br>30 | 20<br>200 | 35<br>350 | µA<br>µA |
| $I_{TIMER}$ | Timer Source Current | $V_{IN1} = 0.8V$, $V_{IN2} = V_{\overline{DIODE}} = 2V$, $V_{TIMER} = 0V$,<br>$V_{SENSE^+} – V_{SENSE^-} = 300mV$ | ● | 3 | 5.5 | 9 | µA |
| $V_{TIMER}$ | Timer Latch Threshold Voltage | $V_{IN1} = 0.8V$, $V_{IN2} = V_{\overline{DIODE}} = 2V$ | ● | 1.1 | 1.2 | 1.3 | V |
| $t_{ON}$ | Gate Drive Rise Time | $C_{GS}$ = 1000pF, $V_{SAB1} = V_{SAB2} = 0V$ (Note 4) | | | 33 | | µs |
| $t_{OFF}$ | Gate Drive Fall Time | $C_{GS}$ = 1000pF, $V_{SAB1} = V_{SAB2} = 20V$ (Note 4) | | | 2 | | µs |
| $t_{D1}$ | Gate Drive Turn-On Delay | $C_{GS}$ = 1000pF, $V_{SAB1} = V_{SAB2} = 0V$ (Note 4) | | | 22 | | µs |
| $t_{D2}$ | Gate Drive Turn-Off Delay | $C_{GS}$ = 1000pF, $V_{SAB1} = V_{SAB2} = 20V$ (Note 4) | | | 1 | | µs |
| $f_{OVGG}$ | $V_{GG}$ Regulator Operating Frequency | | | | 30 | | kHz |

## ELECTRICAL CHARACTERISTICS

**Note 1:** Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

**Note 2:** $T_J$ is calculated from the ambient temperature $T_A$ and power dissipation $P_D$ according to the following formula:

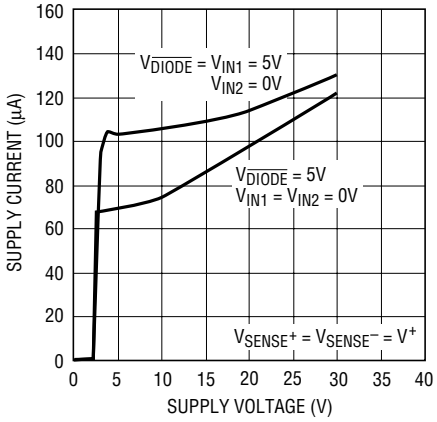
$T_J = T_A + (P_D)(150°C/W)$

**Note 3:** $I_S$ increases by the same amount as $I_{BSENSE}^+ + I_{BSENSE}^-$ when their common mode falls below 5V.

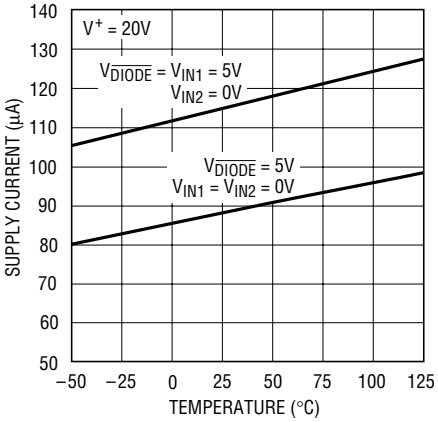
**Note 4:** Gate turn-on and turn-off times are measured with no inrush current limiting, i.e., $V_{SENSE}$ = 0V. Gate rise times are measured from 1V to 4.5V and fall times are measured from 4.5V to 1V. Delay times are measured from the input transition to when the gate voltage has risen or fallen to 3V.

## TYPICAL PERFORMANCE CHARACTERISTICS

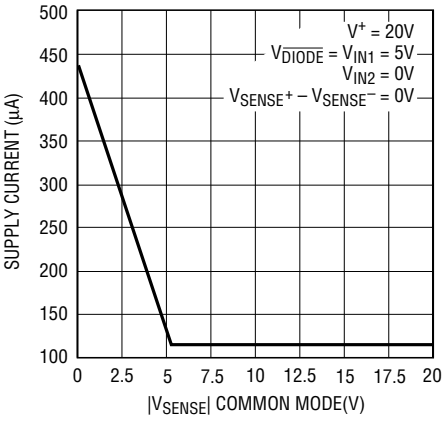
**DC Supply Current vs Supply Voltage**



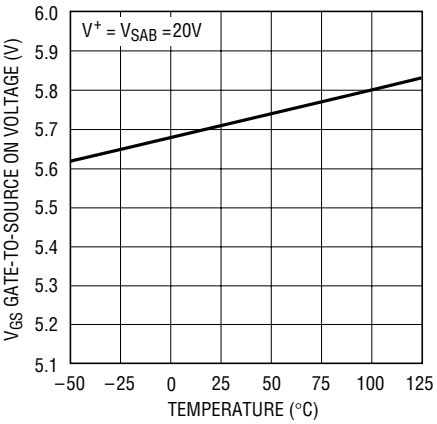

**DC Supply Current vs Temperature**



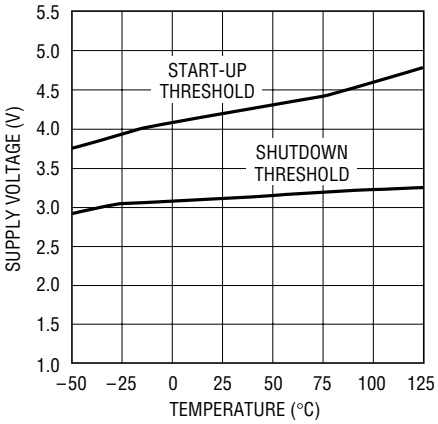

**DC Supply Current vs $V_{SENSE}$**



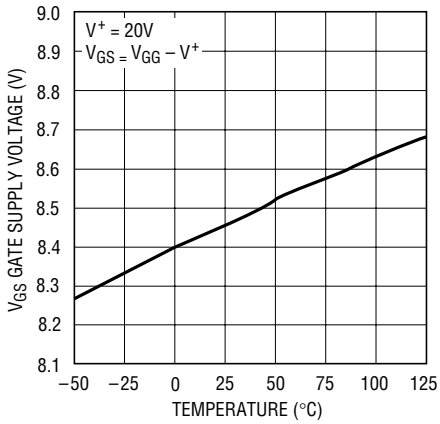

**$V_{GS}$ Gate-to-Source ON Voltage vs Temperature**




**Undervoltage Lockout Threshold ($V^+$) vs Temperature**

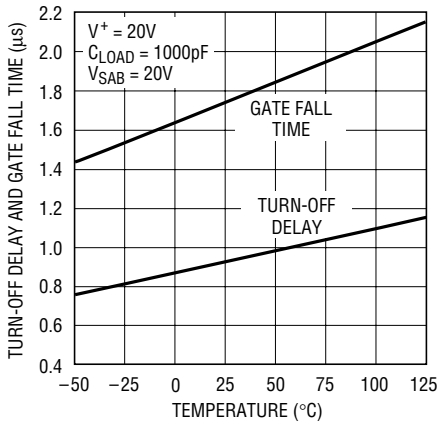



**$V_{GS}$ Gate Supply Voltage vs Temperature**



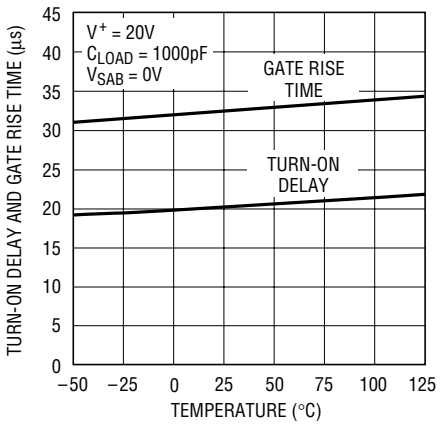
## TYPICAL PERFORMANCE CHARACTERISTICS

### Turn-Off Delay and Gate Fall Time vs Temperature



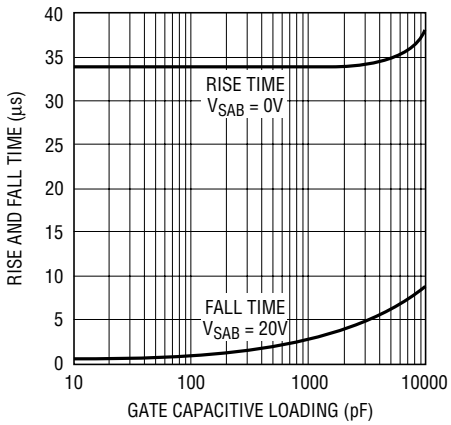

1473 G07

### Turn-On Delay and Gate Rise Time vs Temperature



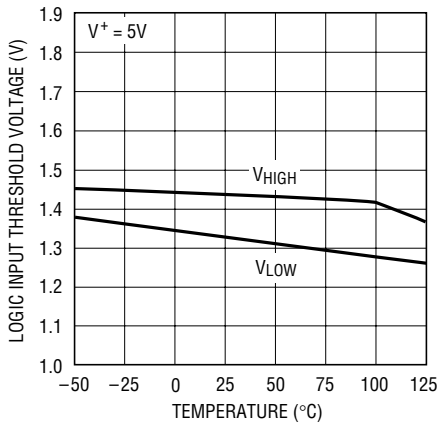

1473 G06

### Rise and Fall Time vs Gate Capacitive Loading



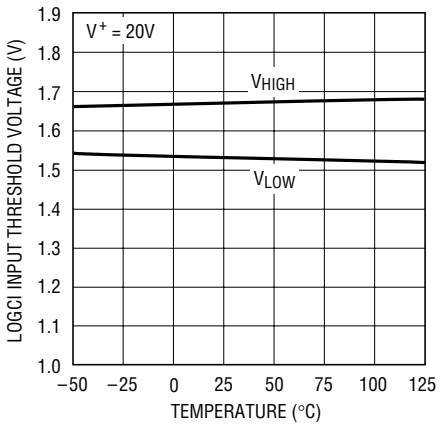

1473 G08

### Logic Input Threshold Voltage vs Temperature



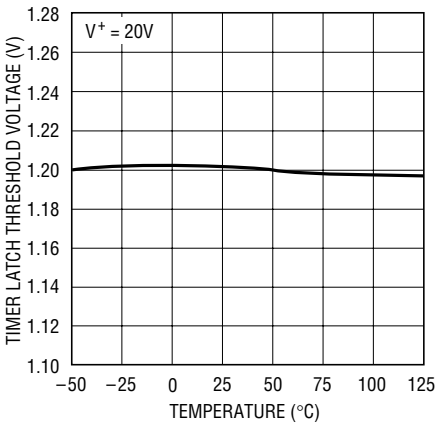

1473 G10

### Logic Input Threshold Voltage vs Temperature



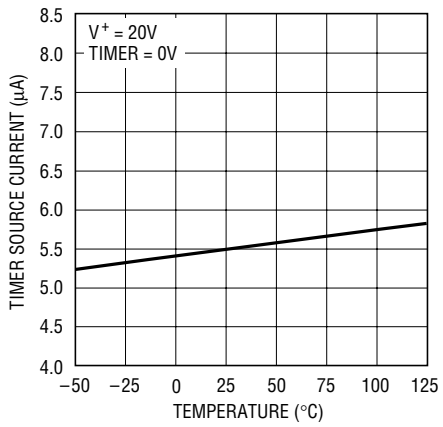

1473 G11

### Timer Latch Threshold Voltage vs Temperature



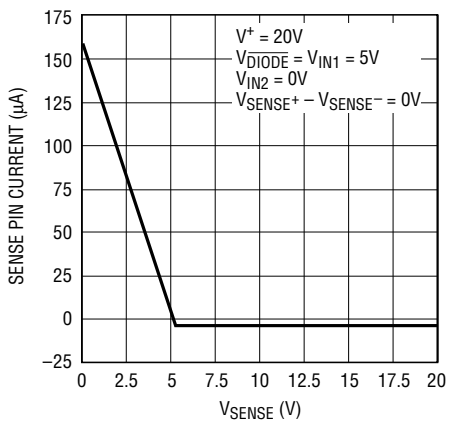

1473 G12

### Timer Source Current vs Temperature




1473 G13

### Sense Pin Source Current $I_{BSENSE}$ vs $V_{SENSE}$




1473 • TPC14

## PIN FUNCTIONS

**IN1 (Pin 1):** Logic Input of Gate Drivers GA1 and GB1. IN1 is disabled when IN2 is high or $\overline{DIODE}$ is low.

**IN2 (Pin 2):** Logic Input of Gate Drivers GA2 and GB2. IN2 is disabled when IN1 is high or $\overline{DIODE}$ is low.

**$\overline{DIODE}$ (Pin 3):** "2-Diode Mode" Logic Input. $\overline{DIODE}$ overrides IN1 and IN2 by forcing the two back-to-back external N-channel MOSFET switches to mimic two diodes.

**TIMER (Pin 4):** Fault Timer. A capacitor connected from this pin to GND programs the time the MOSFET switches are allowed to be in current limit. To disable this function, Pin 4 can be grounded.

**$V^+$ (Pin 5):** Input Supply. Bypass this pin with at least a 1µF capacitor.

**$V_{GG}$ (Pin 6):** Gate Driver Supply. This high voltage supply is intended only for driving the internal micropower gate drive circuitry. *Do not load this pin with any external circuitry*. Bypass this pin with at least 1µF.

**SW (Pin 7):** Open Drain of an internal N-Channel MOSFET Switch. This pin drives the bottom of the $V_{GG}$ switching regulator inductor which is connected between this pin and the $V^+$ pin.

**GND (Pin 8):** Ground.

**GA2, GB2 (Pins 11, 9):** Switch Gate Drivers. GA2 and GB2 drive the gates of the second back-to-back external N-channel switches.

**SAB2 (Pin 10):** Source Return. The SAB2 pin is connected to the sources of SW A2 and SW B2. A small pull-down current source returns this node to 0V when the switches are turned off.

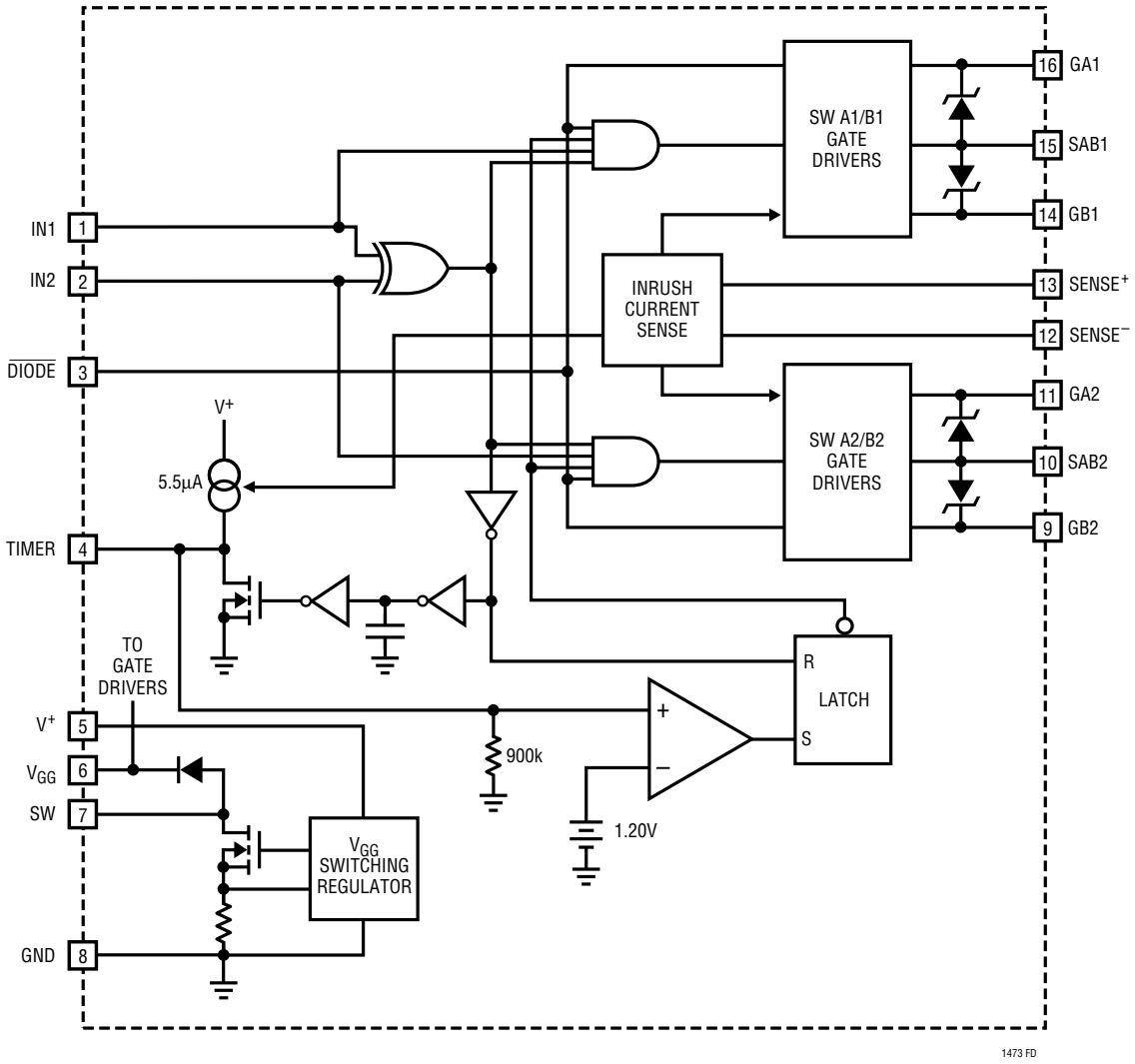
**$SENSE^-$ (Pin 12):** Inrush Current Input. This pin should be connected directly to the bottom (output side) of the low value current sense resistor in series with the two input power selector switch pairs, SW A1/B1 and SW A2/B2, for detecting and controlling the inrush current into and out of the power supply sources and the output capacitor.

**$SENSE^+$ (Pin 13):** Inrush Current Input. This pin should be connected directly to the top (switch side) of the low value current sense resistor in series with the two input power selector switch pairs, SW A1/B1 and SW A2/B2, for detecting and controlling the inrush current into and out of the power supply sources and the output capacitor. Current limit is invoked when ($V_{SENSE}^+ - V_{SENSE}^-$) exceeds ±0.2V.

**GA1, GB1 (Pins 16, 14):** Switch Gate Drivers. GA1 and GB1 drive the gates of the first back-to-back external N-channel switches.

**SAB1 (Pin 15):** Source Return. The SAB1 pin is connected to the sources of SW A1 and SW B1. A small pull-down current source returns this node to 0V when the switches are turned off.

## FUNCTIONAL DIAGRAM



## OPERATION

The LTC1473 is responsible for low-loss switching and isolation at the "front end" of the power management system, where up to two battery packs can be connected and disconnected seamlessly. Smooth switching between input power sources is accomplished with the help of lowloss N-channel switches. They are driven by special gate drive circuitry which limits the inrush current in and out of the battery packs and the system power supply capacitors.

### All N-Channel Switching

The LTC1473 drives external back-to-back N-channel MOSFET switches to direct power from two sources: the primary battery and the secondary battery or a battery and a wall unit. (N-channel MOSFET switches are more cost effective and provide lower voltage drops than their P-channel counterparts.)

### Gate Drive ($V_{GG}$) Power Supply

The gate drive for the low-loss N-channel switches is supplied by an internal micropower boost regulator which is regulated at approximately 8.5V above $V^+$, up to 37V maximum. In two battery systems, the LTC1473 $V^+$ pin is diode ORed through three external diodes connected to the three main power sources, DCIN, BAT1 and BAT2. Thus, $V_{GG}$ is regulated at 8.5V above the highest power source and will provide the overdrive required to fully enhance the MOSFET switches.

For maximum efficiency the top of the boost regulator inductor is connected to $V^+$ as shown in Figure 1. C1 provides filtering at the top of the 1mH switched inductor, L1, which is housed in a small surface mount package. An internal diode directs the current from the 1mH inductor to the $V_{GG}$ output capacitor C2.

### Inrush and Short-Circuit Current Limiting

The LTC1473 uses an adaptive inrush current limiting scheme to reduce current flowing in and out of the two main power sources and the following system's input capacitor during switch-over transitions. The voltage across a single small valued resistor, $R_{SENSE}$, is measured to ascertain the instantaneous current flowing through the two switch pairs, SW A1/B1 and SW A2/B2, during the transitions.

Figure 2 shows a block diagram of a switch driver pair, SW A1/B1. A bidirectional current sensing and limiting circuit determines when the voltage drop across $R_{SENSE}$ reaches ±200mV. The gate-to-source voltage, $V_{GS}$, of the appropriate switch is limited during the transition period until the inrush current subsides, generally within a few milliseconds, depending upon the value of the following system's input capacitor.

This scheme allows capacitors and MOSFET switches of differing sizes and current ratings to be used in the same system without circuit modifications.

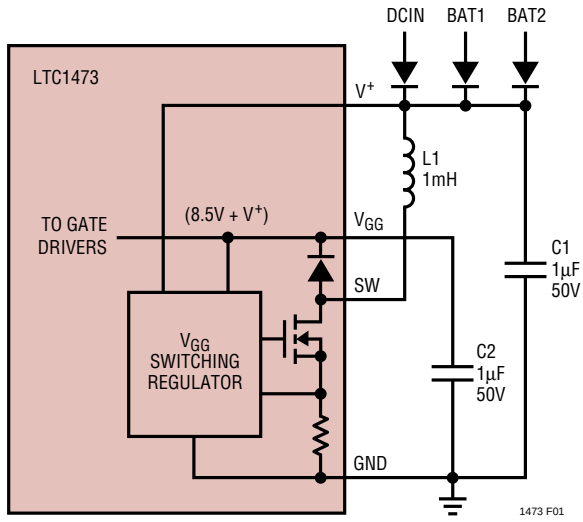



**Figure 1. $V_{GG}$ Switching Regulator**

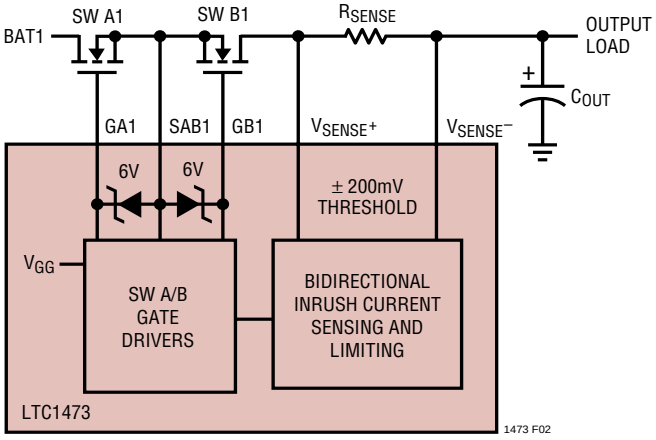



**Figure 2. SW A1/B1 Inrush Current Limiting**

## APPLICATIONS INFORMATION

After the transition period, the $V_{GS}$ of both MOSFETs in the selected switch pair rises to approximately 5.6V. The gate drive is set at 5.6V to provide ample overdrive for standard logic-level MOSFET switches without exceeding their maximum $V_{GS}$ rating.

In the event of a fault condition the current limit loop will limit the inrush current into the short. At the instant the MOSFET switch is in current limit, i.e., when the voltage drop across $R_{SENSE}$ is ±200mV, a fault timer will start timing. It will continue to time as long as the MOSFET switch is in current limit. Eventually the preset time will lapse and the MOSFET switch will latch off. The latch is reset by deselecting the gate drive input. Fault time-out is programmed by an external capacitor connected between the TIMER pin and ground.

### POWER PATH SWITCHING CONCEPTS

#### Power Source Selection

The LTC1473 drives low-loss switches to direct power in the main power path of a single or dual rechargeable battery system, the type found in many notebook computers and other portable equipment.

Figure 3 is a conceptual block diagram that illustrates the main features of an LTC1473 dual battery power management system starting with the three main power sources and ending at the output load (i.e.: system DC/DC regulator).

Switches SW A1/B1 and SW A2/B2 direct power from either batteries to the input of the DC/DC switching regulator. Each of the switches is controlled by a TTL/CMOS compatible input that can interface directly with a power management system µP.

#### Using Tantalum Capacitors

The inrush (and "outrush") current of the system DC/DC regulator input capacitor is limited by the LTC1473, i.e., the current flowing both in and out of the capacitor during transitions from one input power source to another is limited. In many applications, this inrush current limiting makes it feasible to use smaller tantalum surface mount capacitors in place of larger aluminum electrolytics.

*Note: The capacitor manufacturer should be consulted for specific inrush current specifications and limitations and some experimentation may be required to ensure compliance with these limitations under all possible operating conditions.*

#### Back-to-Back Switch Topology

The simple SPST switches shown in Figure 3 actually consist of two back-to-back N-channel switches. These low-loss N-channel switch pairs are housed in 8-pin SO and SSOP packaging and are available from a number of manufacturers. The back-to-back topology eliminates the problems associated with the inherent body diodes in power MOSFET switches and allows each switch pair to

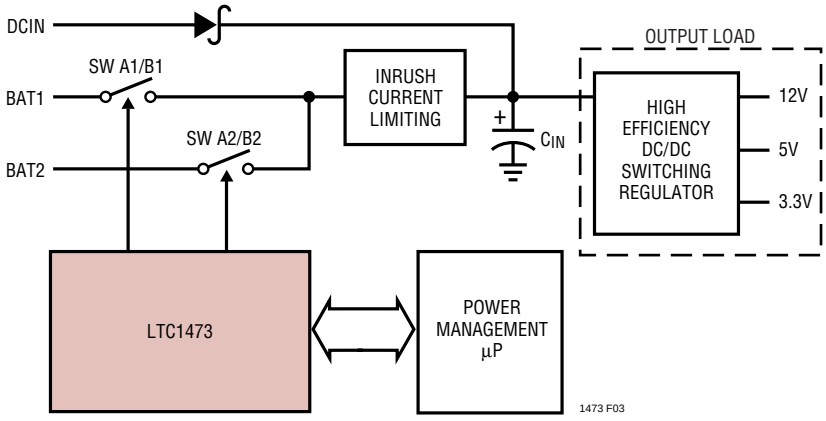



**Figure 3. LTC1473 PowerPath Conceptual Diagram**

## APPLICATIONS INFORMATION

block current flow in either direction when both switches are turned off.

The back-to-back topology also allows for independent control of each half of the switch pair which facilitates bidirectional inrush current limiting and the so-called "2-diode mode" described in the following section.

### The 2-Diode Mode

Under normal operating conditions, both halves of each switch pair are turned on and off simultaneously. For example, when the input power source is switched from BAT1 to BAT2 in Figure 4, both gates of switch pair SW A1/B1 are normally turned off and both gates of switch pair SW A2/B2 are turned on. The back-to-back body diodes in switch pair, SW A1/B1, block current flow in or out of the BAT1 input connector.

In the "2-diode mode," only the first half of each power path switch pair, i.e., SW A1 and SW A2, are turned on; and the second half, i.e., SW B1 and SW B2 are turned off. These two switch pairs now act simply as two diodes connected to the two main input power sources as illustrated in Figure 4. The power path diode with the highest input voltage passes current through to the output load (i.e. input of the DC/DC converter) to ensure that the power management μP is powered even under start-up or abnormal operating conditions. (An undervoltage lockout circuit defeats this mode when the $V^+$ pin drops below approximately 3.2V. The supply to $V^+$ comes from the main power sources, DCIN, BAT1 and BAT2 through three external diodes as shown in Figure 1.)

The 2-diode mode is asserted by applying an active low to the $\overline{DIODE}$ input.

## COMPONENT SELECTION

### N-Channel Switches

The LTC1473 adaptive inrush current limiting circuitry permits the use of a wide range of logic-level N-Channel MOSFET switches. A number of dual, low $R_{DS(ON)}$ N-channel switches in 8-lead surface mount packages are available that are well suited for LTC1473 applications.

The maximum allowable drain-source voltage, $V_{DS(MAX)}$, of the two switch pairs, SW A1/B1 and SW A2/B2 must be high enough to withstand the maximum DC supply voltage. If the DC supply is in the 20V to 28V range, use 30V MOSFET switches. If the DC supply is in the 10V to 18V range, and is well regulated, then 20V MOSFET switches will suffice.

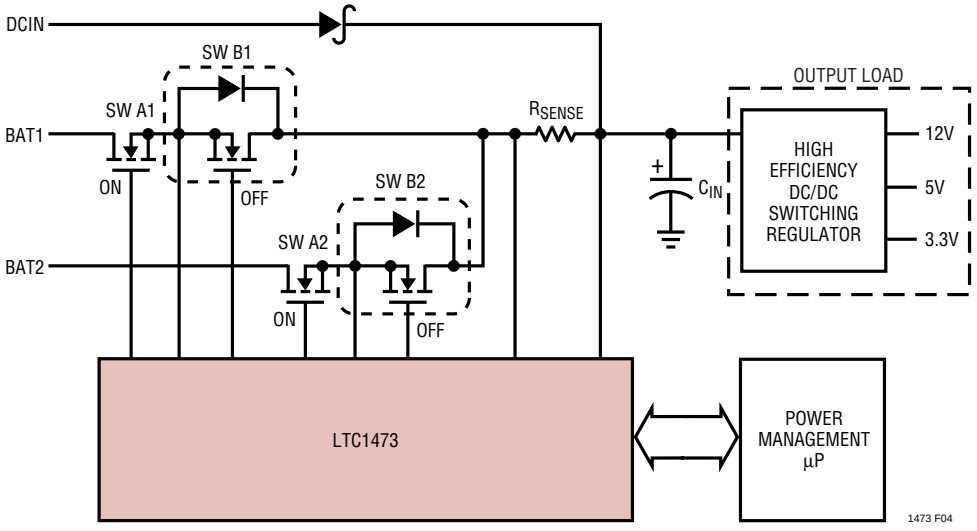



**Figure 4. LTC1473 PowerPath Switches in 2-Diode Mode**

## APPLICATIONS INFORMATION

As a general rule, select the switch with the lowest $R_{DS(ON)}$ and able to withstand the maximum allowable $V_{DS}$. This will minimize the heat dissipated in the switches while increasing the overall system efficiency. Higher switch resistances can be tolerated in some systems with lower current requirements, but care should be taken to ensure that the power dissipated in the switches is never allowed to rise above the manufacturers' recommended level.

### Inrush Current Sense Resistor, $R_{SENSE}$

A small valued sense resistor (current shunt) is used by the two switch pair drivers to measure and limit the inrush or short-circuit current flowing through the conducting switch pair.

The inrush current limit should be set at approximately 2× or 3× the maximum required output current. For example, if the maximum current required by the DC/DC converter is 2A, an inrush current limit of 6A is set by selecting a 0.033Ω sense resistor, $R_{SENSE}$, using the following formula:

$$R_{SENSE} = (200mV)/I_{INRUSH}$$

Note that the voltage drop across the resistor in this example is only 66mV under normal operating conditions. Therefore, the power dissipated in the resistor is extremely small (132mW), and a small 1/4W surface mount resistor can be used in this application (the resistor will tolerate the higher power dissipation during current limit for the duration of the fault time-out). A number of small valued surface mount resistors are available that have been specifically designed for high efficiency current sensing applications.

### Programmable Fault Timer Capacitor, $C_{TIMER}$

A fault timer capacitor, $C_{TIMER}$, is used to program the time duration the MOSFET switches are allowed to be in continuous current limit.

In the event of a fault condition, the MOSFET switch is driven into current limit by the inrush current limit loop. The MOSFET switch operating in current limit is in a high dissipation mode and can fail catastrophically if not promptly terminated.

The fault time delay is programmed with an external capacitor between the TIMER pin and GND. At the instant the MOSFET switch enters current limit, a 5.5μA current source starts charging $C_{TIMER}$ through the TIMER pin. When the voltage across $C_{TIMER}$ reaches 1.2V an internal latch is set and the MOSFET switch is turned off. To reset the latch, the logic input of the MOSFET gate driver is deselected.

The fault time delay should be programmed as large as possible, at least 3× to 5× the maximum switching transition period, to avoid prematurely tripping the protection circuit. Conversely, for the protection circuit to be effective, the fault time delay must be within the safe operating area of the MOSFET switches, as stated in the manufacturer's data sheet.

The maximum switching transition period happens during a cold start, when a fully charged battery is connected to an unpowered system. The inrush current charging the system supply capacitor to the battery voltage determines the switching transition period.

The following example illustrates the calculation of $C_{TIMER}$. Assume the maximum battery voltage is 20V, the system supply capacitor is 68μF, the inrush current limit is 6A and the maximum current required by the DC/DC converter is 2A. Then, the maximum switching transition period is calculated using the following formula:

$$t_{SW(MAX)} = \frac{(V_{BAT(MAX)})(C_{IN(DC/DC)})}{I_{INRUSH} - I_{LOAD}}$$

$$t_{SW(MAX)} = \frac{(20)(68\mu F)}{6A - 2A} = 340\mu s$$

Multiplying 3 by 340μs gives 1.02ms, the minimum fault delay time. Make sure this delay time does not fall outside of the safe operating area of the MOSFET switch dissipating 60W (6A • 20V/2). Using this delay time the $C_{TIMER}$ can be calculated using the following formula:

$$C_{TIMER} = 1.02ms\left(\frac{5.5\mu A}{1.20V}\right) = 4700pF$$

Therefore, $C_{TIMER}$ should be 4700pF.

## APPLICATIONS INFORMATION

### $V_{GG}$ Regulator Inductor and Capacitors

The $V_{GG}$ regulator provides a power supply voltage 8.5V higher than any of the three main power source voltages to allow the control of N-channel MOSFET switches. This micropower, step-up voltage regulator is powered by the highest potential available from the three main power sources for maximum regulator efficiency.

Three external components are required by the $V_{GG}$ regulator: L1, C1 and C2, as shown in Figure 5.

L1 is a small, low current, 1mH surface mount inductor. C1 provides filtering at the top of the 1mH switched inductor and should be at least 1µF to filter switching transients. The $V_{GG}$ output capacitor, C2, provides storage and filtering for the $V_{GG}$ output and should be at least 1µF and rated for 50V operation. C1 and C2 can be ceramic capacitors.

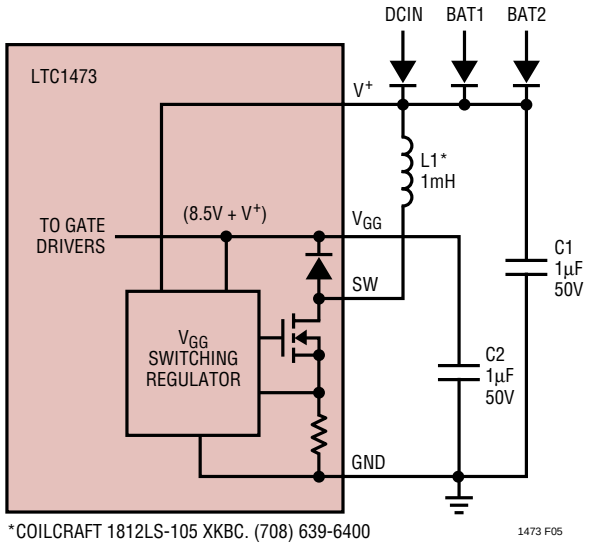
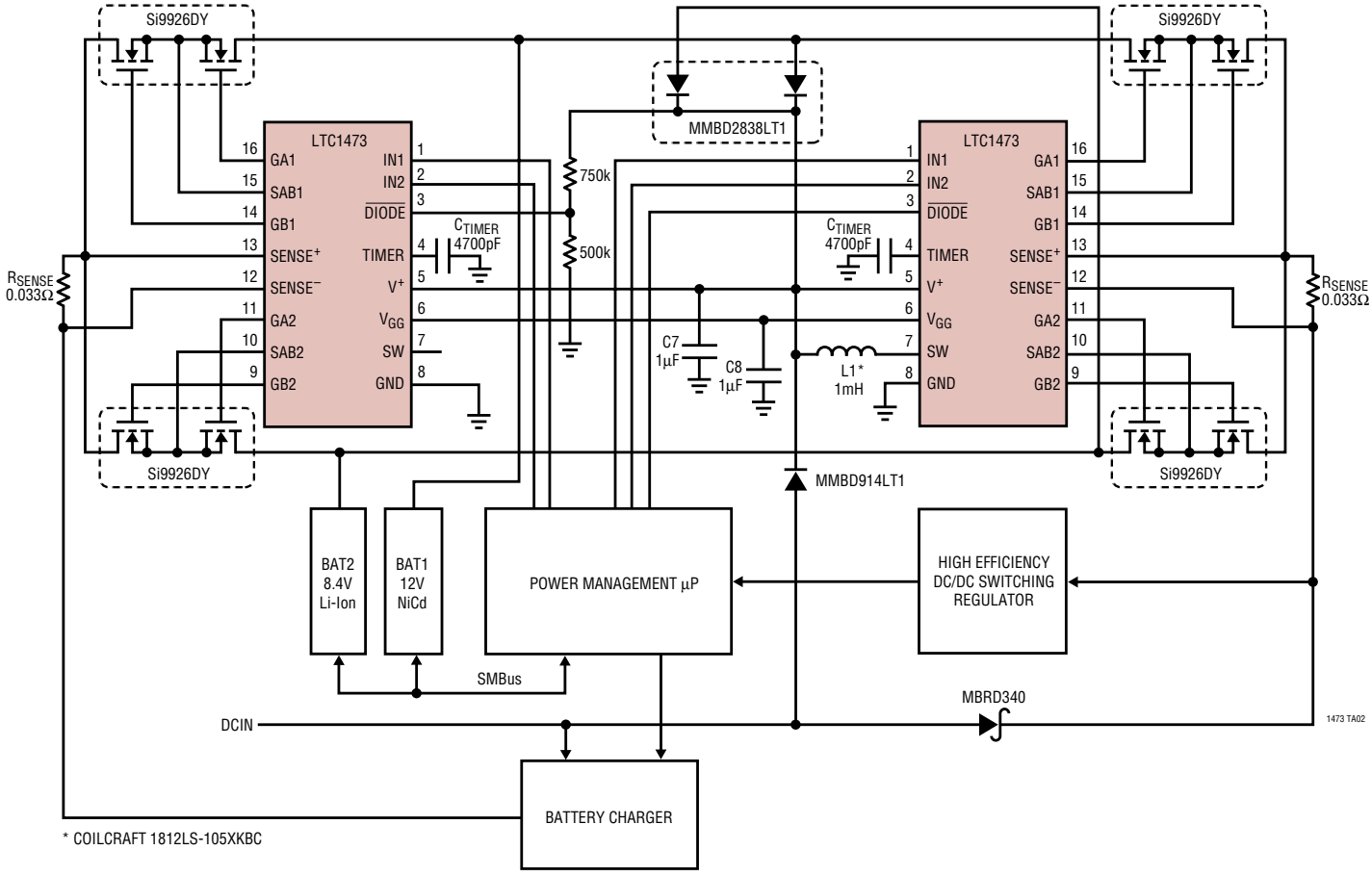



**Figure 5. $V_{GG}$ Step-Up Switching Regulator**

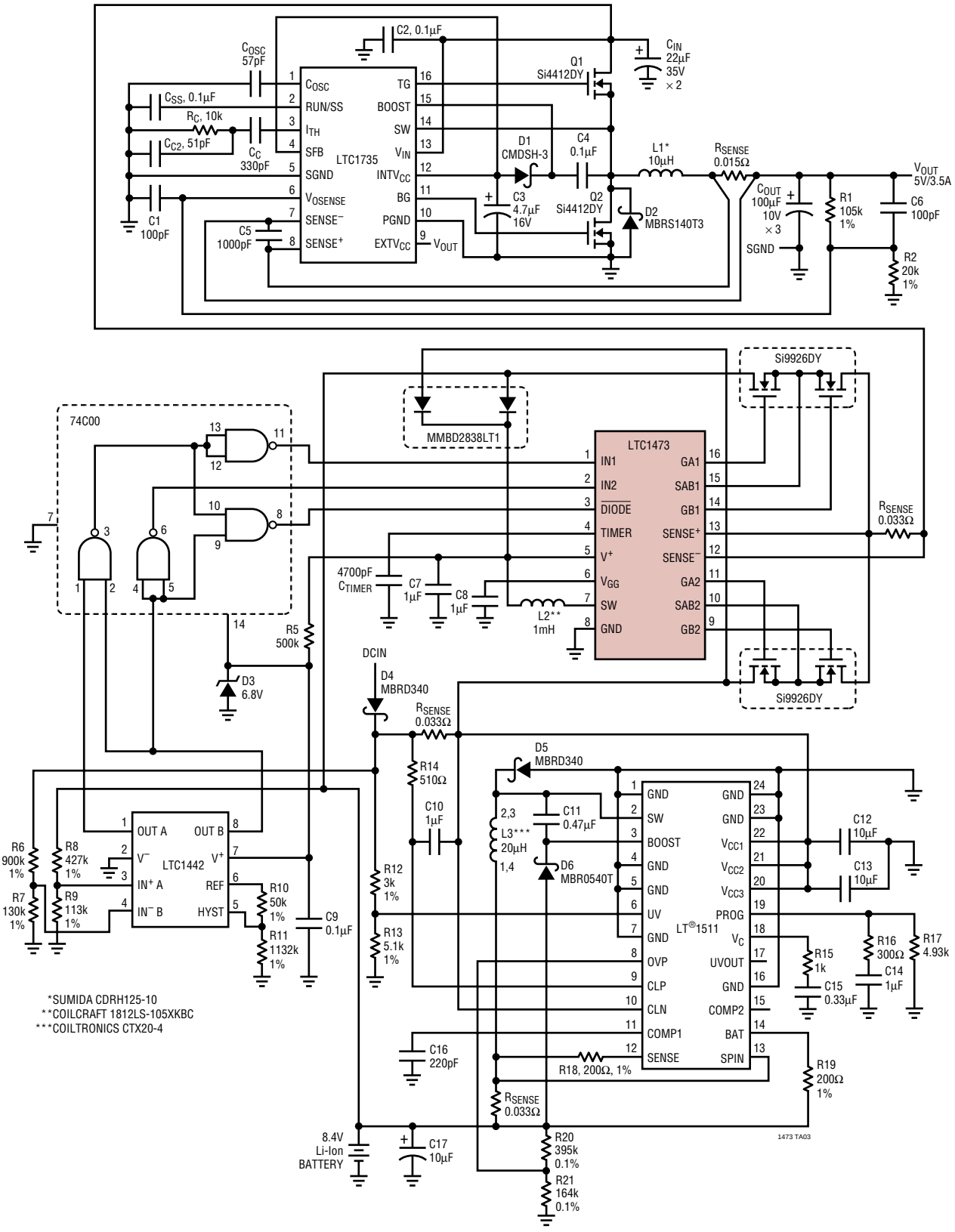
# TYPICAL APPLICATIONS

**Input Power Routing Circuit for Microprocessor Controlled Dual Battery Dual Chemistry System**



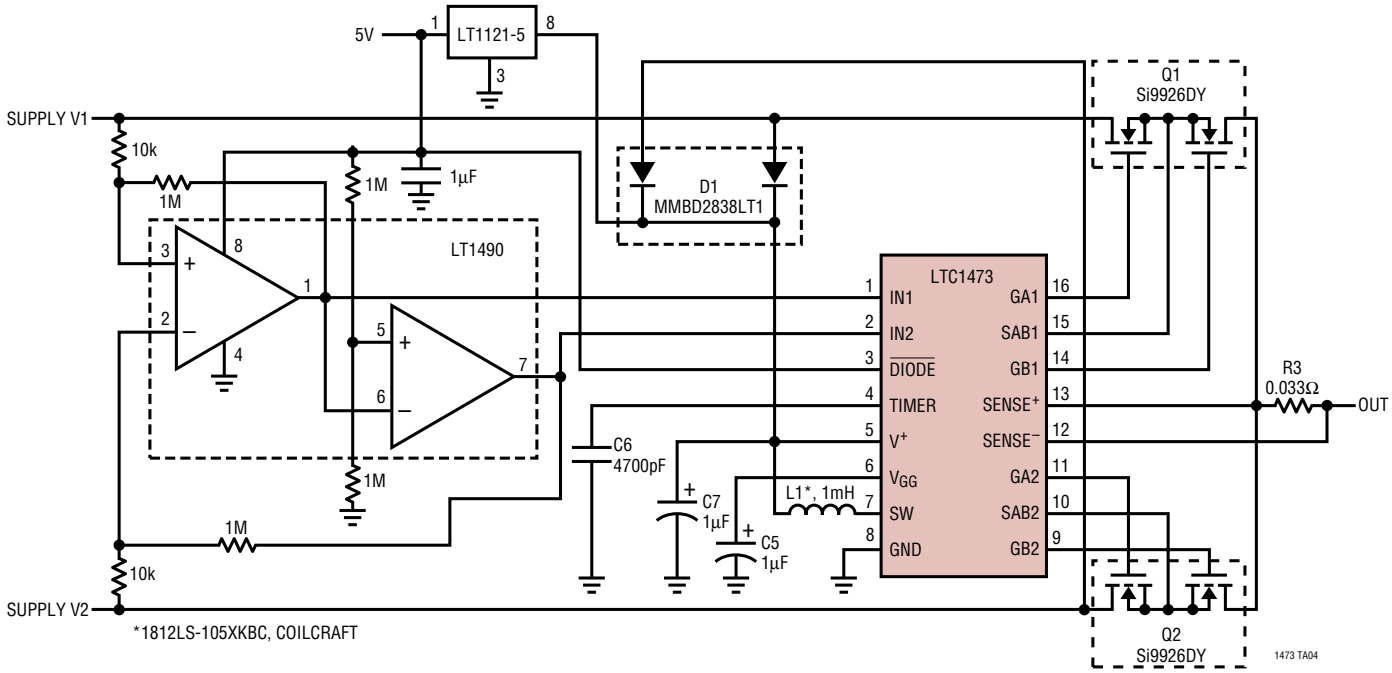
# TYPICAL APPLICATIONS

**Complete Front End Including Battery Charger and DC/DC Converter with Automatic Switchover Between Battery and DCIN**



## TYPICAL APPLICATION

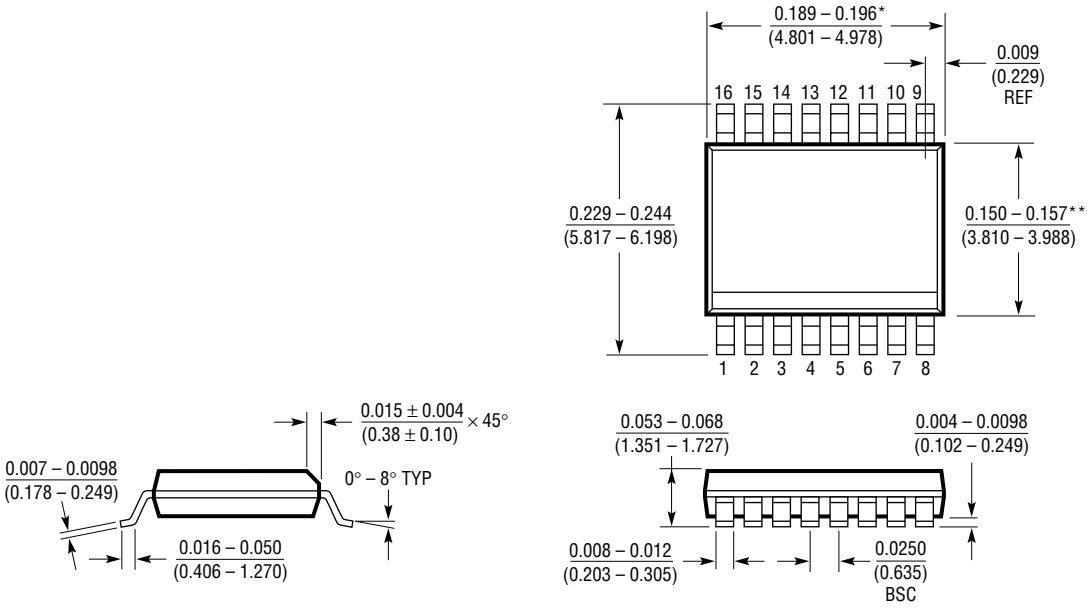
**Protected Automatic Switchover Between Two Supplies**



## PACKAGE DESCRIPTION

**Dimensions in inches (millimeters) unless otherwise noted.**

**GN Package**
**16-Lead Plastic SSOP (Narrow 0.150)**
(LTC DWG # 05-08-1641)




* DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

** DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

GN16 (SSOP) 1098