Dual Low Voltage PowerPath™ Switch Driver

FEATURES

- **Power Path Management for Systems with Multiple DC Sources**
- **Switches and Isolates Sources from 3.3V to 10V**
- **All N-Channel Switching to Reduce Power Losses and System Cost**
- Built-In Step-Up Regulator for N-Channel Gate Drive
- Capacitor Inrush and Short-Circuit Current Limited
- User-Programmable Timer Prevents Overdissipation During Current Limiting
- Undervoltage Lockout Prevents Operation with Low Inputs
- Small Footprint: 16-Pin Narrow SSOP

APPLICATIONS

- Portable Computers
- Portable Instruments
- Fault Tolerant Computers
- Battery-Backup Systems
- 3.3V/5V Power Management

DESCRIPTION

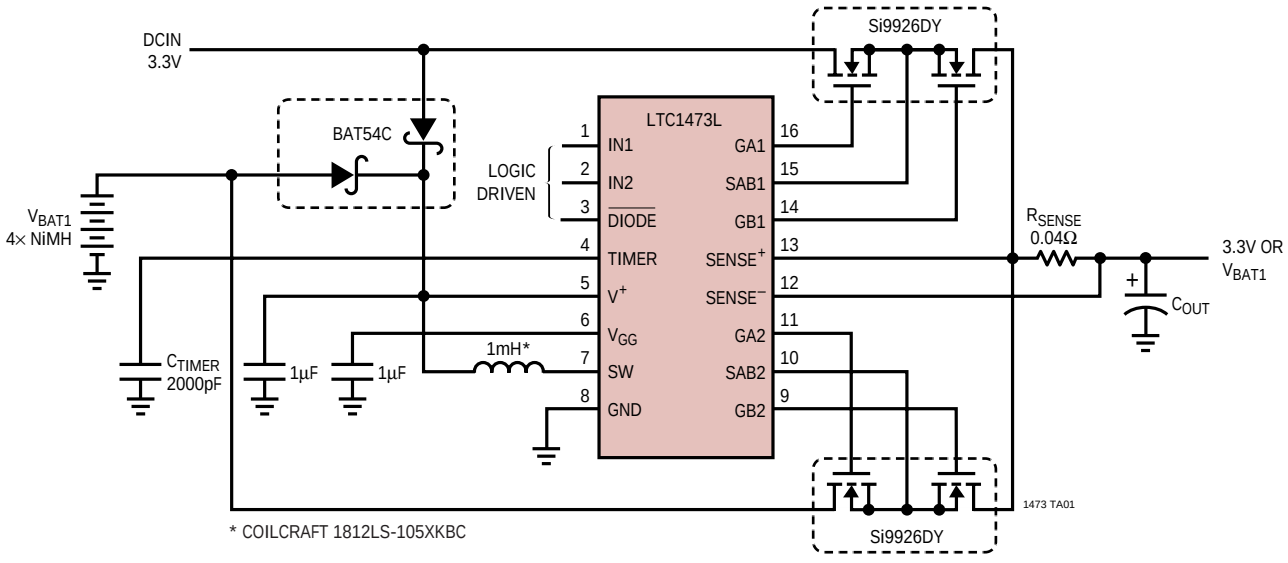
The LTC®1473L provides reliable and efficient switching between two DC power sources. This device drives two external sets of back-to-back N-channel MOSFET switches to route power to the input of a low voltage system. An internal boost regulator provides the voltage to fully enhance the logic-level N-channel MOSFET switches while an internal undervoltage lock-out circuit keeps the system alive down to 2.8V.

The LTC1473L senses current to limit inrush between the batteries and the system supply capacitor during switchover transitions or during fault conditions. A user-programmable timer monitors the time the MOSFET switches are in current limit and latches them off when the programmed time is exceeded.

A unique “2-diode” logic mode ensures system start-up regardless of which input receives power first.

TYPICAL APPLICATION

3.3V to 4-Cell NiMH Backup Switch

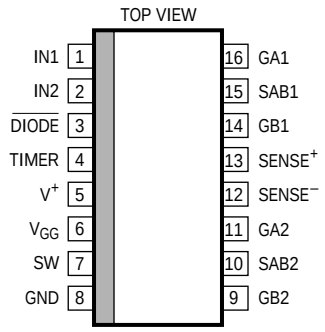


ABSOLUTE MAXIMUM RATINGS

(Note 1)

$SENSE^+$, $SENSE^-$, V^+ ..... –0.3 to 10V
GA1, GB1, GA2, GB2 ..... –0.3 to 20V
SAB1, SAB2 ..... –0.3 to 10V
SW, V_{GG} ..... –0.3 to 20V
IN1, IN2, DIODE ..... –0.3V to 7V
Junction Temperature (Note 2) ..... 125°C
Operating Temperature Range ..... 0°C to 70°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



GN PACKAGE
16-LEAD NARROW PLASTIC SSOP

T_{JMAX} = 125°C, θ_{JA} = 150°C/W

ORDER PART NUMBER
LTC1473LCGN
GN PART MARKING
1473L

Consult factory for Military and Industrial grade parts.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. Test circuit, V^+ = 5V, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V^+	Supply Operating Range			2.8		9	V
I_S	Supply Current	$V_{IN1} = V_{\overline{DIODE}} = 5V$, $V_{IN2} = 0V$, $V_{SENSE}^+ = V_{SENSE}^- = 5V$	●		100	200	µA
V_{GS}	V_{GS} Gate Supply Voltage	$V_{GS} = V_{GG} – V^+$, $2.8V \le V^+ \le 10V$ (Note 3)	●	7.5	8.5	9.5	V
V^+_{UVLO}	V^+ Undervoltage Lockout Threshold	V^+ Ramping Down	●	2.3	2.5	2.8	V
$V^+_{UVLOHYS}$	V^+ Undervoltage Lockout Hysteresis				70		mV
$V_{HIDIGIN}$	Digital Input Logic High	(Note 4)	●	2	0.9		V
$V_{LODIGIN}$	Digital Input Logic Low	(Note 4)	●		0.6	0.4	V
I_{IN}	Input Current	$V_{IN1} = V_{IN2} = V_{\overline{DIODE}} = 5V$				±1	µA
$V_{GS(ON)}$	Gate-to-Source ON Voltage	$I_{GA1} = I_{GA2} = I_{GB1} = I_{GB2} = –1µA$, $V_{SAB1} = V_{SAB2} = 5V$	●	4.5	5.6	7.0	V
$V_{GS(OFF)}$	Gate-to-Source OFF Voltage	$I_{GA1} = I_{GA2} = I_{GB1} = I_{GB2} = 100µA$, $V_{SAB1} = V_{SAB2} = 5V$	●		0	0.4	V
I_{BSENSE}^+	$SENSE^+$ Input Bias Current	$V_{SENSE}^+ = V_{SENSE}^- = 10V$ (Note 3) $V_{SENSE}^+ = V_{SENSE}^- = 0V$ (Note 5)	● ●	2 –300	4.5 –175	10 –75	µA µA
I_{BSENSE}^-	$SENSE^-$ Input Bias Current	$V_{SENSE}^+ = V_{SENSE}^- = 10V$ (Note 3) $V_{SENSE}^+ = V_{SENSE}^- = 0V$ (Note 5)	● ●	2 –300	4.5 –175	10 –75	µA µA
V_{SENSE}	Inrush Current Limit Sense Voltage	$V_{SENSE}^- = 10V$ ($V_{SENSE}^+ – V_{SENSE}^-$) (Note 3) $V_{SENSE}^- = 0V$ ($V_{SENSE}^+ – V_{SENSE}^-$)		0.15 0.10	0.20 0.20	0.25 0.30	V V
I_{PDSAB}	SAB1, SAB2 Pull-Down Current	$V_{IN1} = V_{IN2} = V_{\overline{DIODE}} = 0.4V$, $V^+ = 10V$ (Note 3) $V_{IN1} = V_{IN2} = 0.4V$, $V_{\overline{DIODE}} = 2V$		5 30	20 140	35 300	µA µA
I_{TIMER}	Timer Source Current	$V_{IN1} = 0.4V$, $V_{IN2} = V_{\overline{DIODE}} = 2V$, $V_{TIMER} = 0V$, $V_{SENSE}^+ – V_{SENSE}^- = 300mV$	●	3	6	9	µA
V_{TIMER}	Timer Latch Threshold Voltage	$V_{IN1} = 0.4V$, $V_{IN2} = V_{\overline{DIODE}} = 2V$	●	1.05	1.16	1.25	V
t_{ON}	Gate Drive Rise Time	$C_{GS} = 1000pF$, $V_{SAB1} = V_{SAB2} = 0V$ (Note 6)			33		µs
t_{OFF}	Gate Drive Fall Time	$C_{GS} = 1000pF$, $V_{SAB1} = V_{SAB2} = 5V$ (Note 6)			2		µs
t_{D1}	Gate Drive Turn-On Delay	$C_{GS} = 1000pF$, $V_{SAB1} = V_{SAB2} = 0V$ (Note 6)			22		µs
t_{D2}	Gate Drive Turn-Off Delay	$C_{GS} = 1000pF$, $V_{SAB1} = V_{SAB2} = 5V$ (Note 6)			1		µs
f_{OVGG}	V_{GS} Regulator Operating Frequency				30		kHz

ELECTRICAL CHARACTERISTICS

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula:

$T_J = T_A + (P_D)(150°C/W)$

Note 3: Some tests are performed under more stringent conditions to ensure reliable operation over the entire supply voltage range.

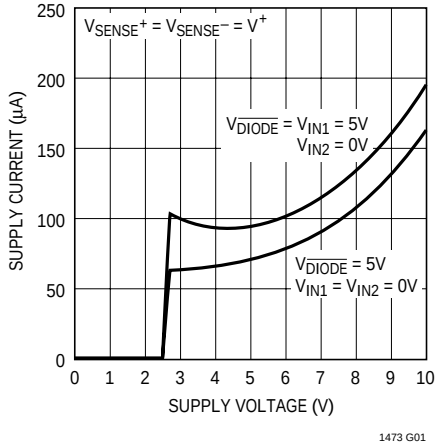
Note 4: Digital inputs include: IN1, IN2 and $\overline{DIODE}$.

Note 5: I_S increases by the same amount as $I_{BSENSE}^+ + I_{BSENSE}^-$ when their common mode falls below 5V.

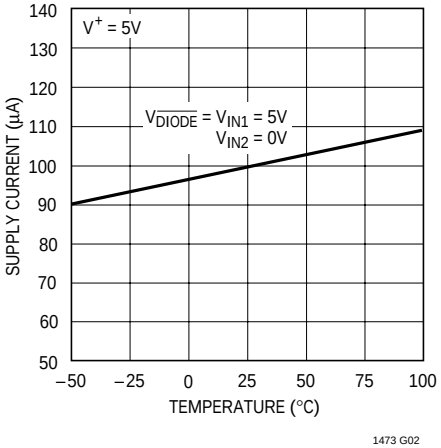
Note 6: Gate turn-on and turn-off times are measured with no inrush current limiting, i.e., V_{SENSE} = 0V. Gate rise times are measured from 1V to 4.5V and fall times are measured from 4.5V to 1V. Delay times are measured from the input transition to when the gate voltage has risen or fallen to 3V. Results are not tested, but guaranteed by design.

TYPICAL PERFORMANCE CHARACTERISTICS

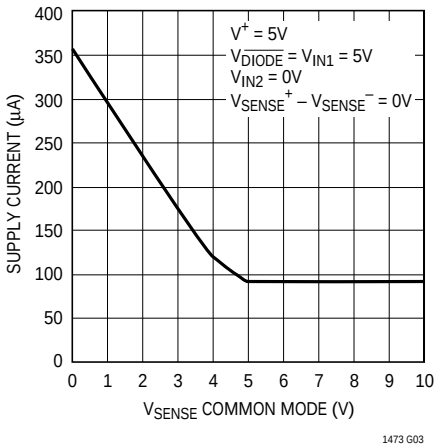
DC Supply Current vs Supply Voltage



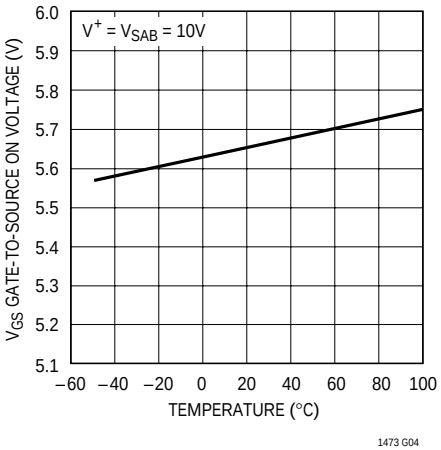
DC Supply Current vs Temperature



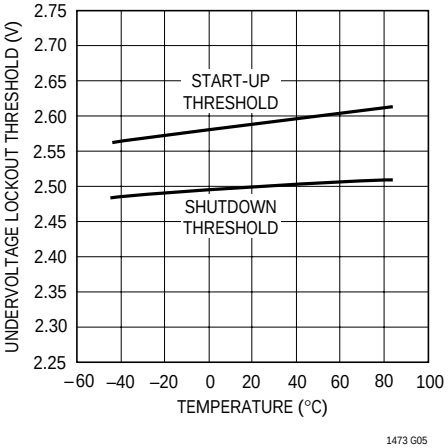
DC Supply Current vs V_{SENSE}



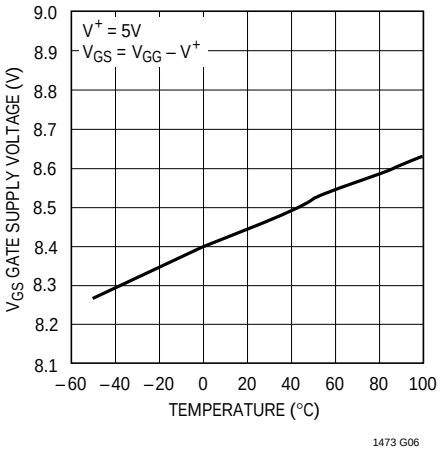
V_{GS} Gate-to-Source ON Voltage vs Temperature



Undervoltage Lockout Threshold (V^+) vs Temperature

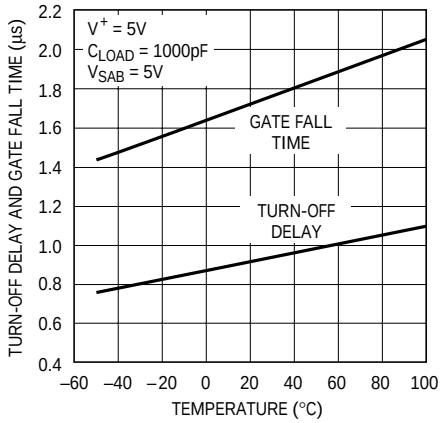


V_{GS} Gate Supply Voltage vs Temperature



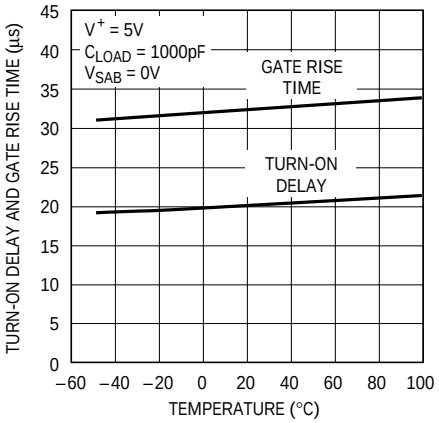
TYPICAL PERFORMANCE CHARACTERISTICS

Turn-Off Delay and Gate Fall Time vs Temperature



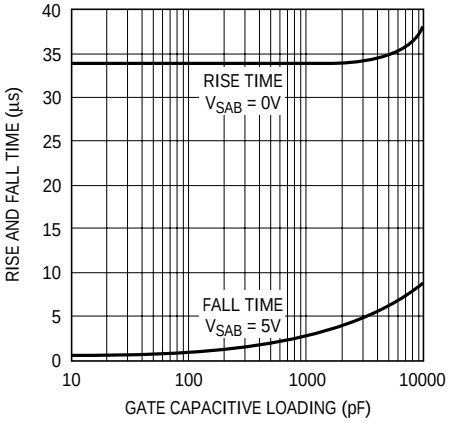
1473 G07

Turn-On Delay and Gate Rise Time vs Temperature



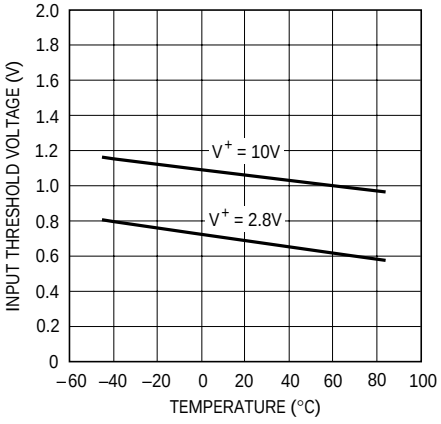
1473 G08

Rise and Fall Time vs Gate Capacitive Loading



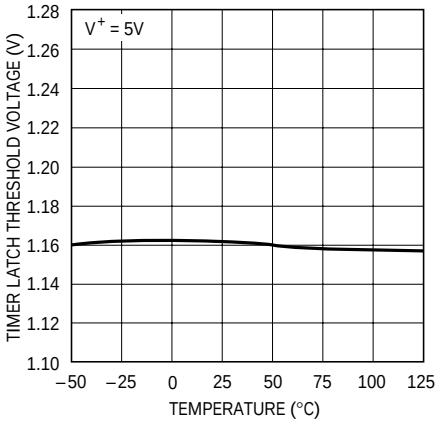
1473 G08

Logic Input Threshold Voltage vs Temperature



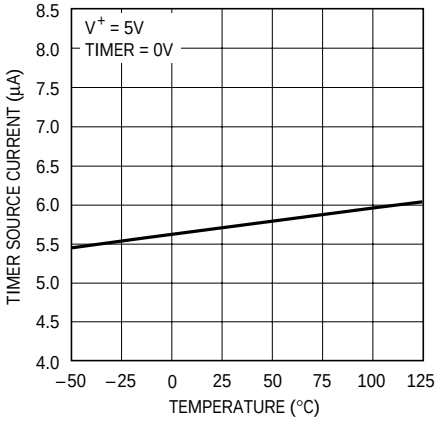
1473 G10

Timer Latch Threshold Voltage vs Temperature



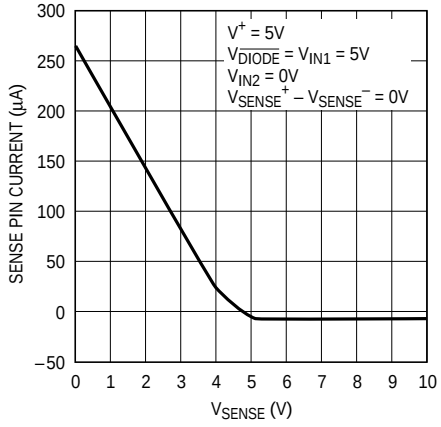
1473 G11

Timer Source Current vs Temperature



1473 G12

SENSE Pin Source Current (I_{BSENSE}) vs V_{SENSE}



1473 G13

PIN FUNCTIONS

IN1 (Pin 1): Logic Input of Gate Drivers GA1 and GB1. IN1 is disabled when IN2 is high or $\overline{DIODE}$ is low. During 2-diode mode, asserting IN1 disables the fault timer function.

IN2 (Pin 2): Logic Input of Gate Drivers GA2 and GB2. IN2 is disabled when IN1 is high or $\overline{DIODE}$ is low. During 2-diode mode, asserting IN2 disables the fault timer function.

$\overline{DIODE}$ (Pin 3): "2-Diode Mode" Logic Input. $\overline{Diode}$ overrides IN1 and IN2 by forcing the two back-to-back external N-channel MOSFET switches to mimic two diodes.

TIMER (Pin 4): Fault Timer. A capacitor connected from this pin to GND programs the time the MOSFET switches are allowed to be in current limit. To disable this function, Pin 4 can be grounded.

V^+ (Pin 5): Power Supply. Bypass this pin with at least a 1µF capacitor.

V_{GG} (Pin 6): Gate Driver Supply. This high voltage supply is intended only for driving the internal micropower gate drive circuitry. *Do not load this pin with any external circuitry*. Bypass this pin with at least 1µF.

SW (Pin 7): Open Drain of an Internal N-Channel MOSFET Switch. This pin drives the bottom of the V_{GG} switching regulator inductor which is connected between this pin and the V^+ pin.

GND (Pin 8): Ground.

GB2, GA2 (Pins 9, 11): Switch Gate Drivers. GA2 and GB2 drive the gates of the second back-to-back external N-channel switches.

SAB2 (Pin 10): Source Return. The SAB2 pin is connected to the sources of SW A2 and SW B2. A small pull-down current source returns this node to 0V when the switches are turned off.

$SENSE^-$ (Pin 12): Inrush Current Input. This pin should be connected directly to the bottom (output side) of the low valued resistor in series with the two input power selector switch pairs, SW A1/B1 and SW A2/B2, for detecting and controlling the inrush current into and out of the power supply sources and the output capacitor.

$SENSE^+$ (Pin 13): Inrush Current Input. This pin should be connected directly to the top (switch side) of the low valued resistor in series with the two input power selector switch pairs, SW A1/B1 and SW A2/B2, for detecting and controlling the inrush current into and out of the power supply sources and the output capacitor. Current limit is invoked when ($V_{SENSE}^+ - V_{SENSE}^-$) exceeds ±0.2V.

Pin Function Table

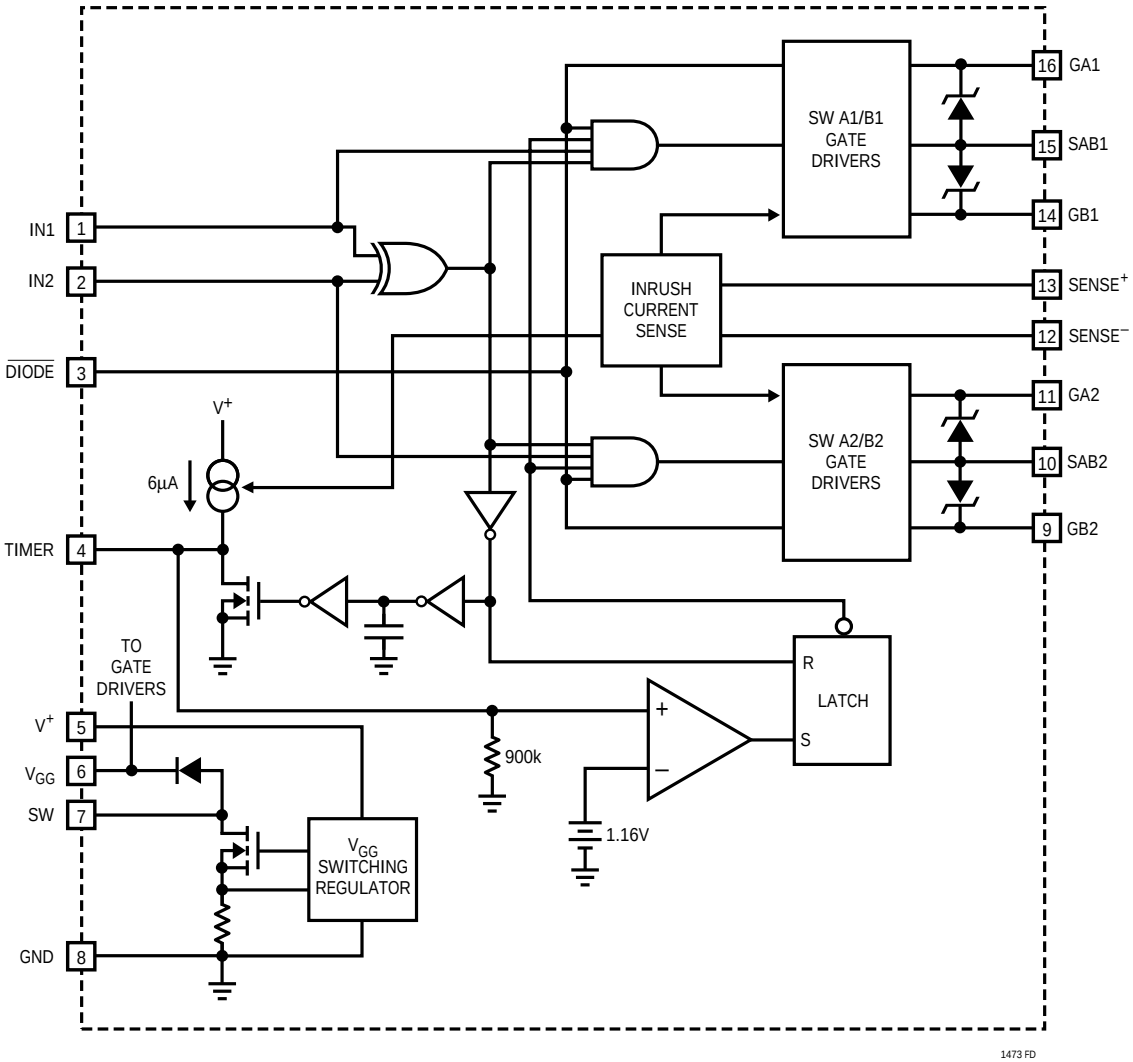
PIN	NAME	DESCRIPTION	NOMINAL (V) MIN	NOMINAL (V) TYP	NOMINAL (V) MAX	ABSOLUTE MAX (V) MIN	ABSOLUTE MAX (V) MAX
1	IN1	Logic Input of Gate Drivers GA1 and GB1	0.4	1	2	–0.3	7
2	IN2	Logic Input of Gate Drivers GA2 and GB2	0.4	1	2	–0.3	7
3	$\overline{DIODE}$	"2-Diode Mode" Logic Input	0.4	1	2	–0.3	7
4	TIMER	Fault Timer Programs Time in Current Limit		1.16		–0.3	5
5	V^+	Power Supply	2.8		9	–0.3	10
6	V_{GG}	Gate Driver Supply	10.2		20	–0.3	20
7	SW	Switch Node of Internal Boost Switching Regulator	0		20	–0.3	20
8	GND	Ground		0		0	0
9	GB2	Switch Gate Driver for Switch B2	0		17	–0.3	20
10	SAB2	Source Return of Switch 2	0		10	–0.3	10
11	GA2	Switch Gate Driver for Switch A2	0		17	–0.3	20
12	$SENSE^-$	Inrush Current Input, Low Side	0		10	–0.3	10
13	$SENSE^+$	Inrush Current Input, High Side	0		10	–0.3	10
14	GB1	Switch Gate Driver for Switch B1	0		17	–0.3	20
15	SAB1	Source Return of Switch 1	0		10	–0.3	10
16	GA1	Switch Gate Driver for Switch A1	0		17	–0.3	20

PIN FUNCTIONS

GB1, GA1 (Pins 14, 16): Switch Gate Drivers. GA1 and GB1 drive the gates of the first back-to-back external N-channel switches.

SAB1 (Pin 15): Source Return. The SAB1 pin is connected to the sources of SW A1 and SW B1. A small pull-down current source returns this node to 0V when the switches are turned off.

FUNCTIONAL DIAGRAM



OPERATION

The LTC1473L is responsible for low-loss switching and isolation for a dual supply system, where during a power backup situation, a battery pack can be connected or disconnected seamlessly. Smooth switching between input power sources is accomplished with the help of low-loss N-channel switches. They are driven by special gate drive circuitry which limits the inrush current in and out of the battery packs and the system power supply capacitors.

All N-Channel Switching

The LTC1473L drives external back-to-back N-channel MOSFET switches to direct power from two sources: the primary battery and the secondary battery, or a battery and a DC power supply. (N-channel MOSFET switches are more cost effective and provide lower voltage drops than their P-channel counterparts.)

Gate Drive (V_{GG}) Power Supply

The gate drive for the low-loss N-channel switches is supplied by an internal micropower boost regulator which is regulated at approximately 8.5V above V^+, up to 20V maximum. In a DC supply and backup battery system, the LTC1473L V^+ pin is diode ORed through two external Schottky diodes connected to the two main power sources, DCIN and BAT1. Thus, V_{GG} is regulated at 8.5V above the higher power source and will provide the overdrive required to fully enhance the MOSFET switches.

For maximum efficiency the input to the boost regulator inductor is connected to V^+ as shown in Figure 1. C1 provides filtering to the input of the 1mH switched inductor, L1, which is housed in a small surface mount package. An internal diode directs the current from the 1mH inductor to the V_{GG} output capacitor C2.

Inrush and Short-Circuit Current Limiting

The LTC1473L uses an adaptive inrush current limiting scheme to reduce current flowing in and out of the battery and the following system's input capacitor during switchover transitions. The voltage across a single small valued resistor, R_{SENSE}, is measured to ascertain the instantaneous current flowing through either of the two switch pairs, SW A1/B1 and SW A2/B2, during the transitions.

Figure 2 shows a block diagram of a switch driver pair, SW A1/B1. A bidirectional current sensing and limiting circuit determines when the voltage drop across R_{SENSE} reaches ±200mV. The gate-to-source voltage, V_{GS}, of the appropriate switch is limited during the transition period until the inrush current subsides.

This scheme allows capacitors and MOSFET switches of differing sizes and current ratings to be used in the same system without circuit modifications.

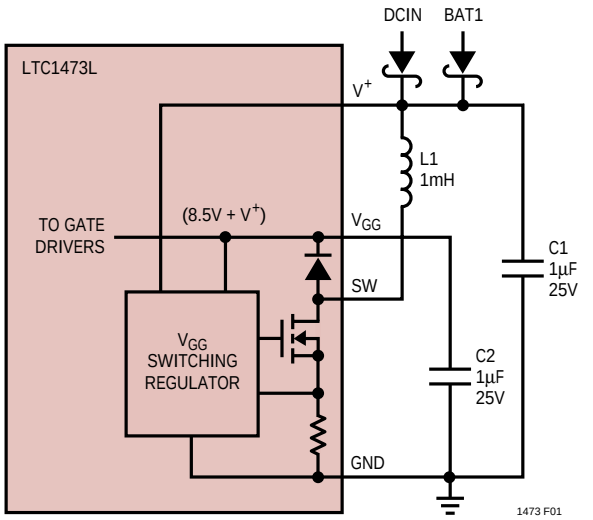


Figure 1. V_{GG} Switching Regulator

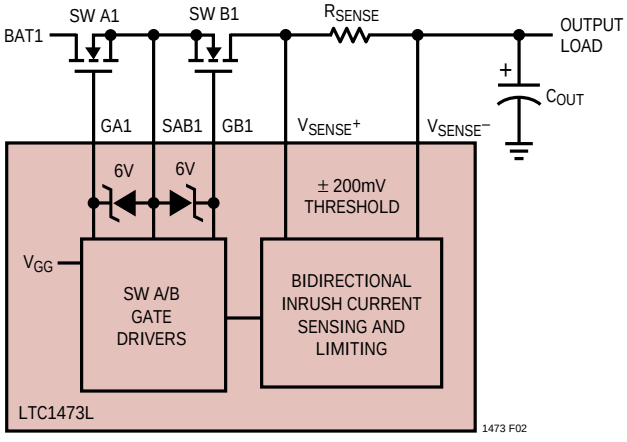


Figure 2. SW A1/B1 Inrush Current Limiting

APPLICATIONS INFORMATION

After the transition period, the V_{GS} of both MOSFETs in the selected switch pair rises to approximately 5.6V. The gate drive is set at 5.6V to provide ample overdrive for logic-level MOSFET switches without exceeding their maximum V_{GS} rating.

In the event of a fault condition, the current limit loop limits the inrush of current into the short. At the instant the MOSFET switch is in current limit, i.e., when the voltage drop across R_{SENSE} is ±200mV, a fault timer starts timing. It will continue to time as long as the MOSFET switch is in current limit. Eventually the preset time will lapse and the MOSFET switch will latch off. The latch is reset by deselecting the gate drive input. Fault time-out is programmed by an external capacitor connected between the TIMER pin and ground.

POWER PATH SWITCHING CONCEPTS

Power Source Selection

The LTC1473L drives low-loss switches to direct power from either the battery pack or the DC supply during power backup situations.

Figure 3 is a conceptual block diagram that illustrates the main features of an LTC1473L dual supply power management system starting with a 4 NiMH battery pack and a 5V/3.3V DC supply and ending with an uninterrupted output load. Switches SW A1/B1 and SW A2/B2 direct power from either the DC supply or the battery to the output load. Each of the switches is controlled by a logic compatible input that can interface directly with a digital pin.

Using Tantalum Capacitors

The inrush (and "outrush") current of the load capacitor is limited by the LTC1473L, i.e., the current flowing both in and out of the capacitor during transitions from one input power source to another is limited. In many applications, this inrush current limiting makes it feasible to use lower cost/size tantalum surface mount capacitors in place of more expensive/larger aluminum electrolytics.

Note: The capacitor manufacturer should be consulted for specific inrush current specifications and limitations and some experimentation may be required to ensure compliance with these limitations under all possible operating conditions.

Back-to-Back Switch Topology

The simple SPST switches shown in Figure 3 actually consist of two back-to-back N-channel switches. These low-loss N-channel switch pairs are housed in 8-pin SO or SSOP packaging and are available from a number of manufacturers. The back-to-back topology eliminates the problems associated with the inherent body diodes in power MOSFET switches and allows each switch pair to block current flow in either direction when the two switches are turned off.

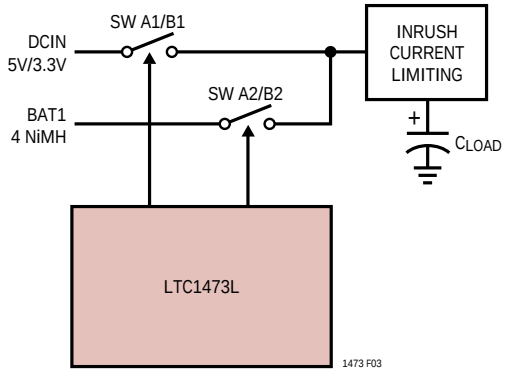


Figure 3. LTC1473L PowerPath Conceptual Diagram

APPLICATIONS INFORMATION

The back-to-back topology also allows for independent control of each half of the switch pair which facilitates bidirectional inrush current limiting and the so-called "2-diode mode" described in the following section.

The 2-Diode Mode

Under normal operating conditions, both halves of each switch pair are turned on and off simultaneously. For example, when the input power source is switched from BAT1 to DCIN in Figure 4, both gates of switch pair SW A1/B1 are normally turned off and both gates of switch pair SW A2/B2 are turned on. The back-to-back body diodes in switch pair, SW A1/B1, block current flow in or out of the BAT1 input connector.

In the "2-diode mode," only the first half of each power path switch pair, i.e., SW A1 and SW A2, is turned on; and the second half, i.e., SW B1 and SW B2, is turned off. These two switch pairs now act simply as two diodes connected to the two main input power sources as illustrated in Figure 4. The power path diode with the highest input voltage passes current through to the output load to ensure that the output is powered even under start-up or abnormal operating conditions. (An undervoltage lockout circuit defeats this mode when the V^+ pin drops below 2.5V. The supply to V^+ comes from the main power sources, DCIN and BAT1 through two common cathode Schottky diodes as shown in Figure 1.)

The 2-diode mode is asserted by applying an active low to the DIODE input.

COMPONENT SELECTION

N-Channel Switches

The LTC1473L adaptive inrush limiting circuitry permits the use of a wide range of logic-level N-Channel MOSFET switches. A number of dual low $R_{DS(ON)}$ N-channel switches in 8-lead surface mount packages are available that are well suited for LTC1473L applications.

The maximum allowable drain-source voltage, $V_{DS(MAX)}$, of the two switch pairs, SW A1/B1 and SW A2/B2 must be high enough to withstand the maximum input DC supply voltage. Since the DC supply is in the 3.3V to 10V range, 12V MOSFET switches will suffice.

As a general rule, select the switch with the lowest $R_{DS(ON)}$ at the maximum allowable V_{DS}. This will minimize the heat dissipated in the switches while increasing the overall system efficiency. Higher switch resistances can be tolerated in some systems with lower current requirements, but care should be taken to ensure that the

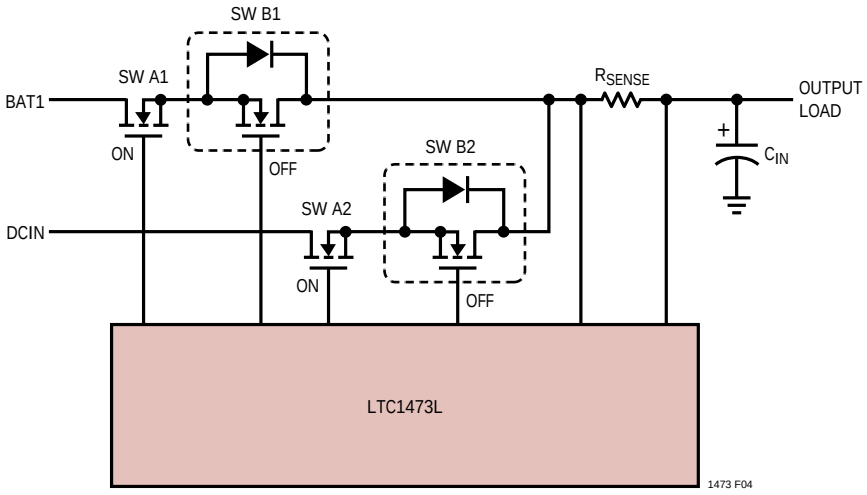


Figure 4. LTC1473L PowerPath Switches in 2-Diode Mode

APPLICATIONS INFORMATION

power dissipated in the switches is never allowed to rise above the manufacturers' recommended level.

Inrush Current Sense Resistor, R_{SENSE}

A small valued sense resistor (current shunt) is used by the two switch pair drivers to measure and limit the inrush or short-circuit current flowing through the conducting switch pair.

The inrush current limit should be set at approximately 2× or 3× the maximum required output current. For example, if the maximum current required by the DC/DC converter is 2A, an inrush current limit of 6A is set by selecting a 0.033Ω sense resistor, R_{SENSE}, using the following formula:

$$R_{SENSE} = (200mV)/I_{INRUSH}$$

Note that the voltage drop across the resistor in this example is only 66mV under normal operating conditions. Therefore, the power dissipated in the resistor is extremely small (132mW), and a small 1/4W surface mount resistor can be used in this application (the resistor will tolerate the higher power dissipation during current limit for the duration of the fault time-out). A number of small valued surface mount resistors are available that have been specifically designed for high efficiency current sensing applications.

Programmable Fault Timer Capacitor, C_{TIMER}

A fault timer capacitor, C_{TIMER}, is used to program the time duration the MOSFET switches are allowed to be in current limit continuously. This feature can be disabled by either grounding the TIMER pin or asserting $\overline{DIODE}$ low and asserting either IN1 or IN2 high.

In the event of a fault condition, the MOSFET switch is driven into current limit by the inrush current limit loop. The MOSFET switch operating in current limit is in a high dissipation mode and can fail catastrophically if not promptly terminated.

The fault time delay is programmed with an external capacitor connected between the TIMER pin and GND. At the instant the MOSFET switch enters current limit, a 6µA current source starts charging C_{TIMER} through the TIMER pin. When the voltage across C_{TIMER} reaches 1.16V an internal latch is set and the MOSFET switch is turned off. To reset the latch, the logic input of the MOSFET gate driver must be deselected.

The fault time delay should be programmed as large as possible, at least 3× to 5× the maximum switching transition period, to avoid prematurely tripping the protection circuit. Conversely, for the protection circuit to be effective, the fault time delay must be within the safe operating area of the MOSFET switches as stated in the manufacturer's data sheet.

The maximum switching transition period happens during a cold start, when a fully charged battery is connected to an unpowered system. The inrush current charging up the system supply capacitor to the battery voltage determines the switching transition period.

The following example illustrates the calculation of C_{TIMER}. Assume the maximum battery voltage is 10V, the system supply capacitor is 100µF, the inrush current limit is 6A and the maximum current required by the following system is 2A. Then, the maximum switching transition period is calculated using the following formula:

$$t_{SW(MAX)} = \frac{\left(V_{BAT(MAX)}\right)\left(C_{IN(SYSTEM)}\right)}{I_{INRUSH} - I_{LOAD}}$$

$$t_{SW(MAX)} = \frac{(10)(100\mu F)}{6A - 2A} = 250\mu s$$

Multiplying 3 by 250µs gives 0.75ms, the minimum fault delay time. Make sure this delay time does not fall outside of the safe operating area of the MOSFET switch dissipating 30W (6A • 10V/2). Using this delay time the C_{TIMER} can be calculated using the following formula:

$$C_{ITMER} = 0.75ms\left(\frac{6\mu A}{1.16V}\right) = 3879pF$$

Therefore, C_{TIMER} can be 3900pF.

APPLICATIONS INFORMATION

V_{GG} Regulator Inductor and Capacitors

The V_{GG} regulator provides a power supply voltage significantly higher than either of the two main power source voltages to allow the control of N-channel MOSFET switches. This micropower, step-up voltage regulator is powered by the higher potential available from the two main power sources for maximum regulator efficiency.

Three external components are required by the V_{GG} regulator: L1, C1 and C2, as shown in Figure 5.

L1 is a small, low current, 1mH surface mount inductor. C1 provides filtering to the input of the 1mH switched inductor and should be at least 1µF to filter switching transients. The V_{GG} output capacitor, C2, provides storage and filtering for the V_{GG} output and should be at least 1µF and rated for 25V operation. C1 and C2 can be ceramic capacitors.

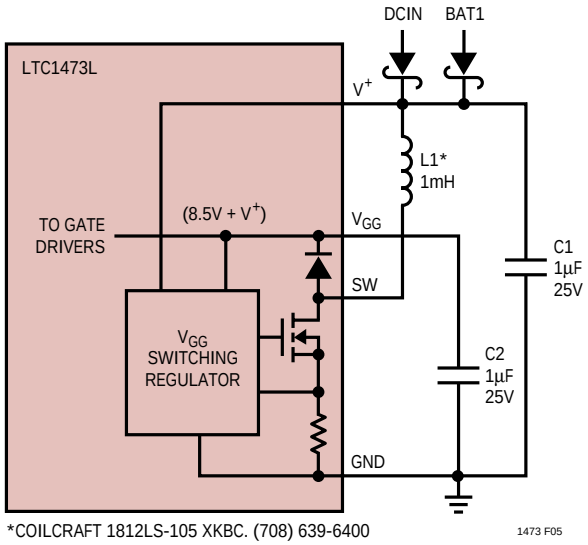
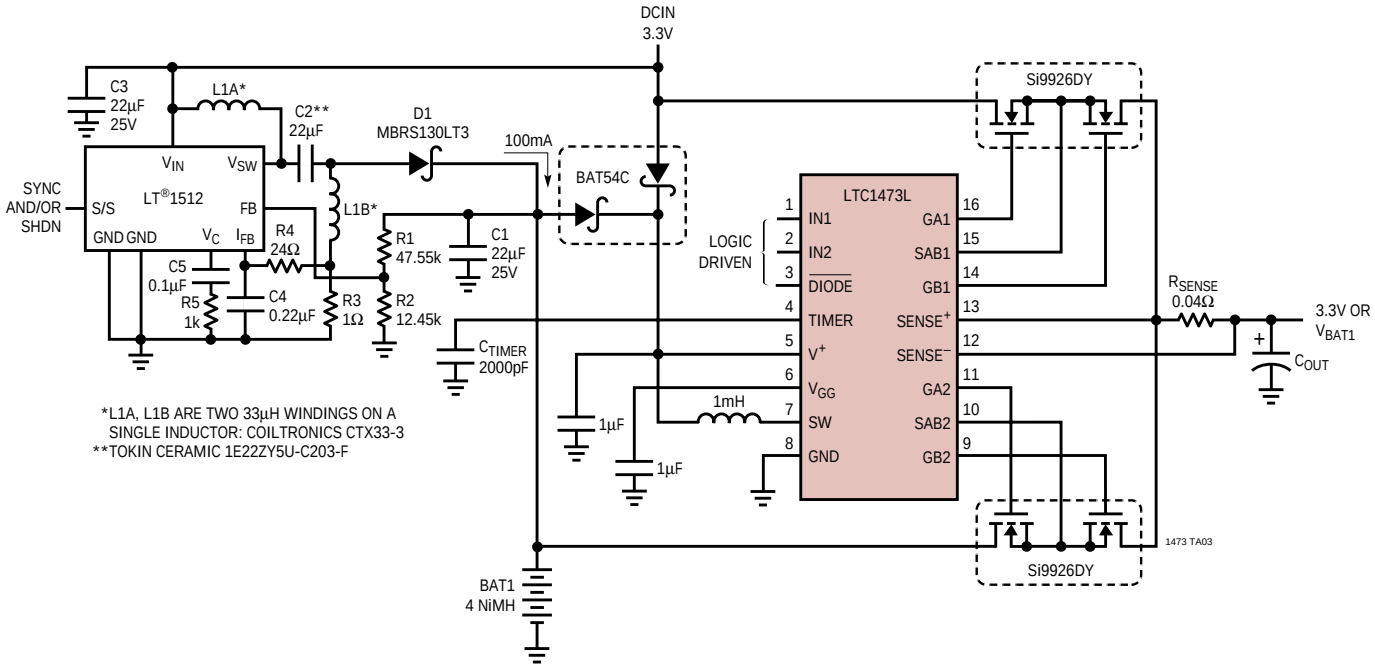


Figure 5. V_{GG} Step-Up Switching Regulator

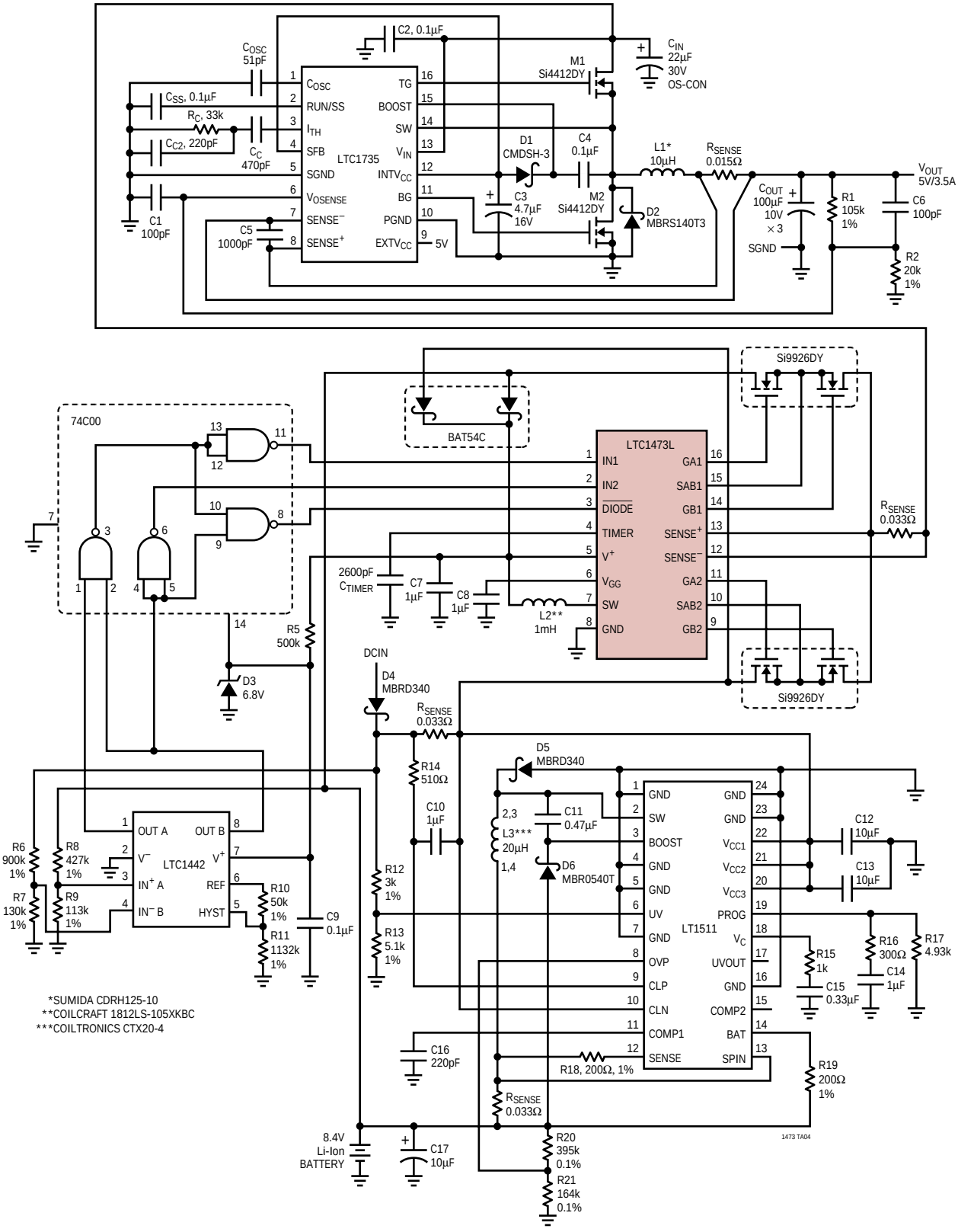
TYPICAL APPLICATIONS

LTC1473L with Battery Charger



TYPICAL APPLICATIONS

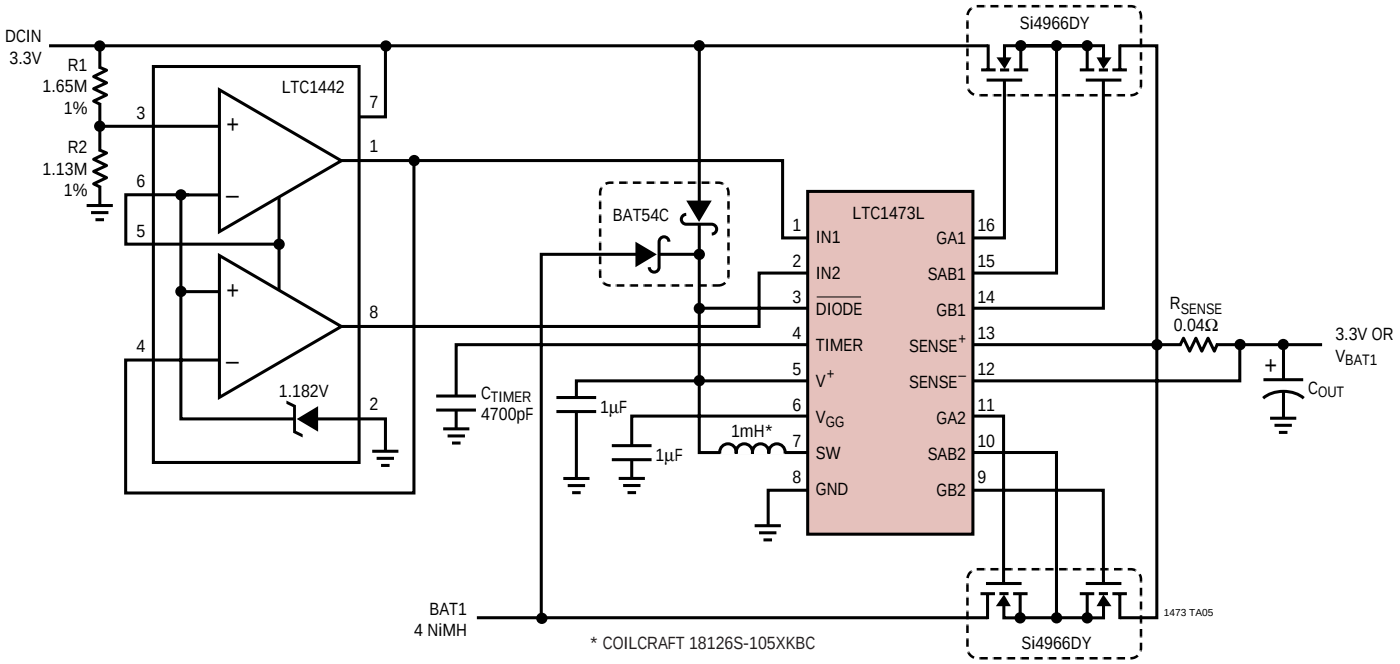
2-Cell Li-Ion to 5V/3.5A DC/DC Converter with Battery Charger and Automatic Switchover Between Battery and DCIN



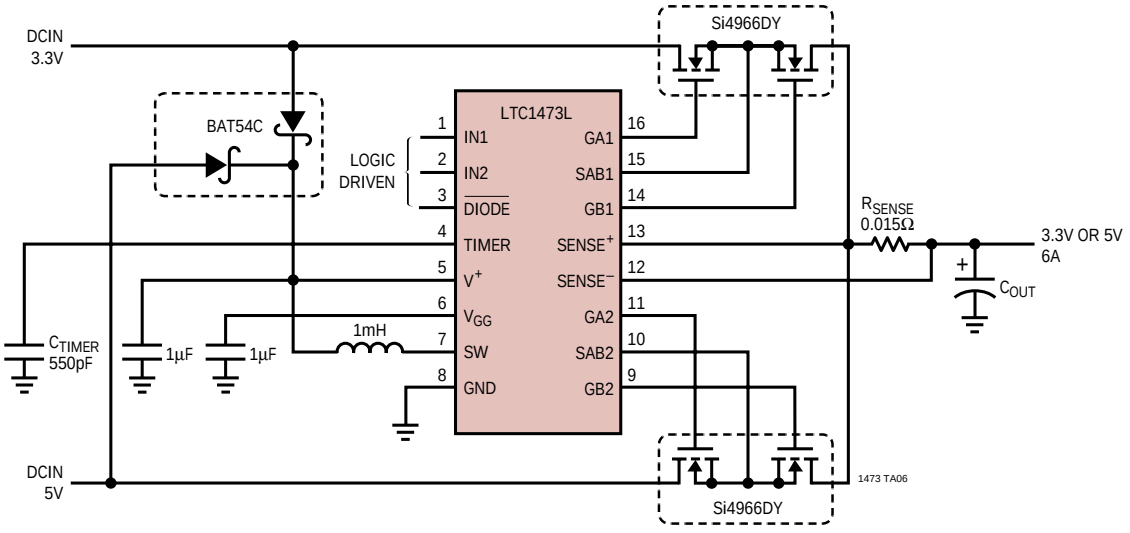
*SUMIDA CDRH125-10
**COILCRAFT 1812LS-105XKBC
***COILTRONICS CTX20-4

TYPICAL APPLICATIONS

Automatic PowerPath Switching for 3.3V Applications

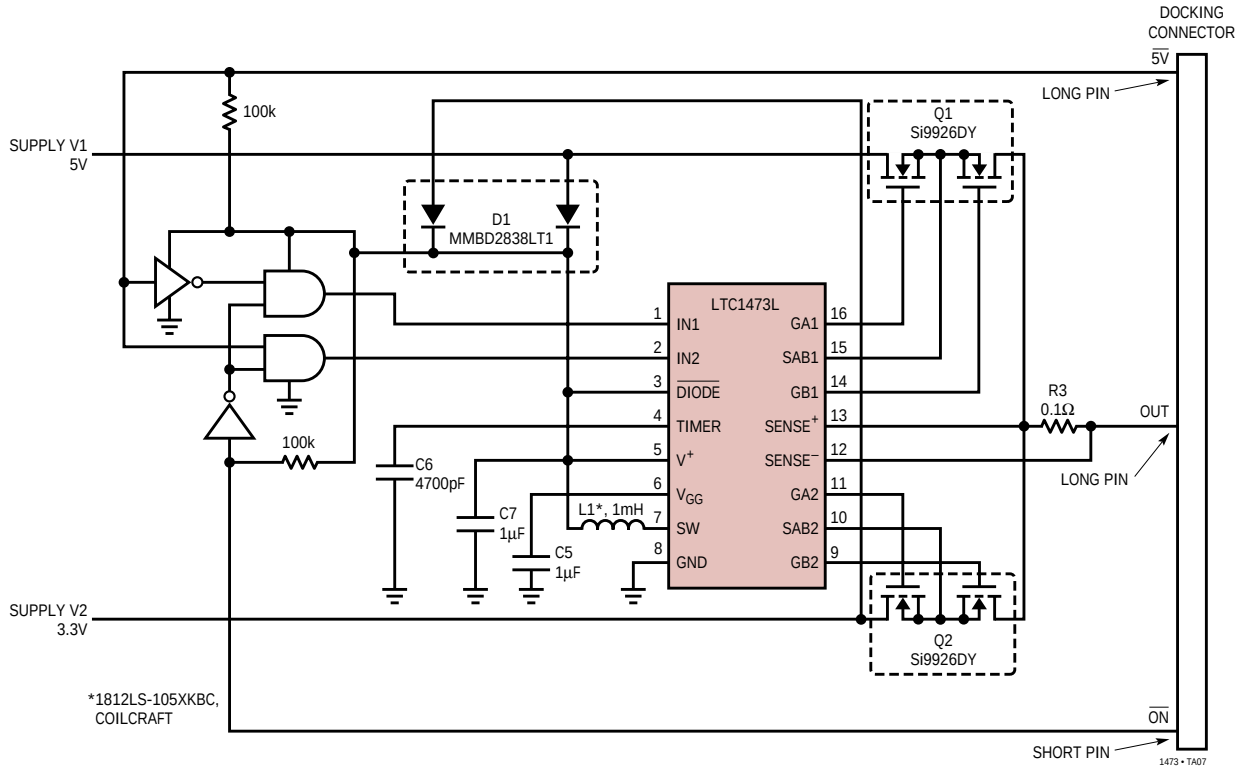


3.3V or 5V, 6A, PowerPath Switch



TYPICAL APPLICATIONS

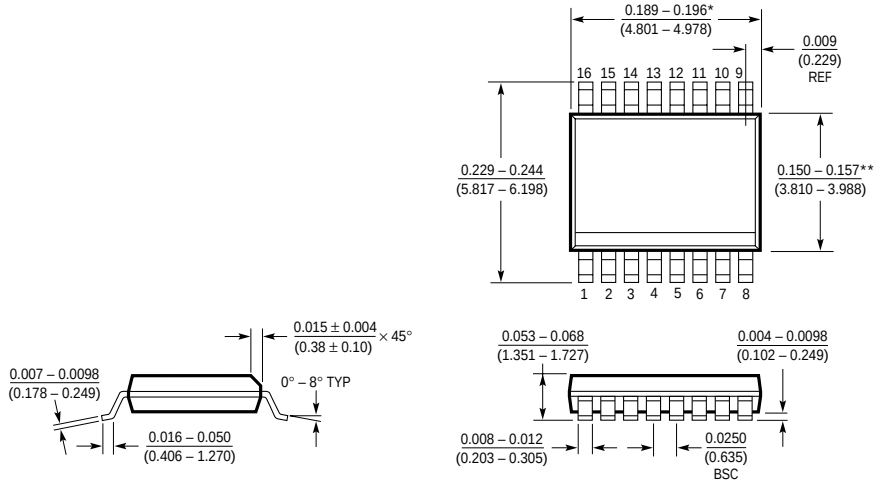
Protected Hot Swap™ Switchover Between Two Supplies for Portable PC



PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

GN Package
16-Lead Plastic SSOP (Narrow 0.150)
(LTC DWG # 05-08-1641)



* DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

** DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

Hot Swap is a trademark of Linear Technology Corporation