Software-Selectable Multiprotocol Transceiver

FEATURES

- **Software-Selectable Transceiver Supports: RS232, RS449, EIA530, EIA530-A, V.35, V.36, X.21**
- **TUV/Detecon Inc. Certified NET1 and NET2 Compliant (Test Report No. NET2/102201/97)**
- **TBR2 Compliant (Test Report No. CTR2/022701/98)**
- Software-Selectable Cable Termination Using the LTC1344A
- Complete DTE or DCE Port with LTC1544, LTC1344A
- Operates from Single 5V Supply

APPLICATIONS

- Data Networking
- CSU and DSU
- Data Routers

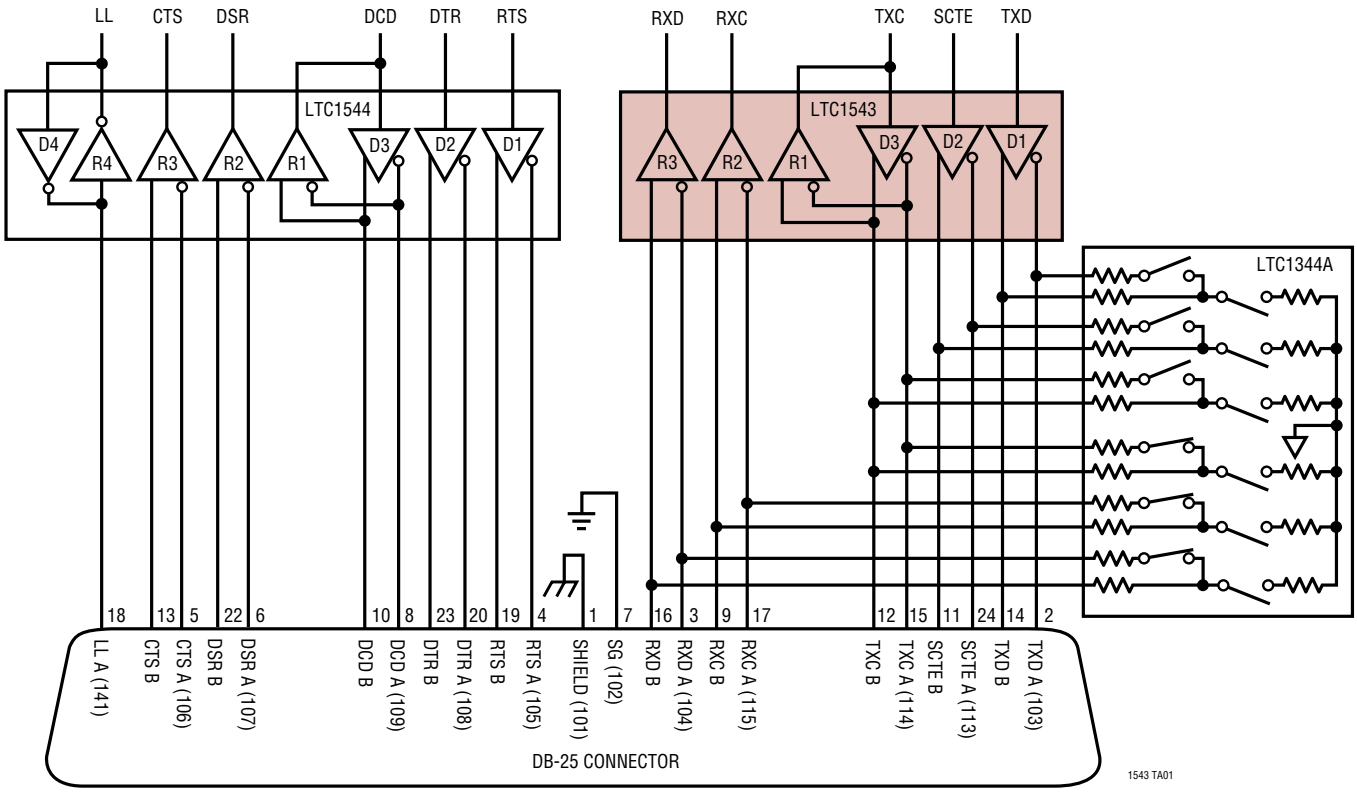
DESCRIPTION

The LTC®1543 is a 3-driver/3-receiver multiprotocol transceiver that operates from a single 5V supply. The LTC1543 and LTC1544 form the core of a complete software-selectable DTE or DCE interface port that supports the RS232, RS449, EIA530, EIA530-A, V.35, V.36 or X.21 protocols. Cable termination may be implemented using the LTC1344A software-selectable cable termination chip or by using existing discrete designs.

The LTC1543 runs from a single 5V supply using an internal charge pump that requires only five space-saving surface mounted capacitors. The part is available in a 28-lead SSOP surface mount package.

TYPICAL APPLICATION

DTE or DCE Multiprotocol Serial Interface with DB-25 Connector



ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage 6.5V

Input Voltage

- Transmitters ..... −0.3V to (V_{CC} + 0.3V)
- Receivers ..... −18V to 18V
- Logic Pins ..... −0.3V to (V_{CC} + 0.3V)

Output Voltage

- Transmitters ..... (V_{EE} − 0.3V) to (V_{DD} + 0.3V)
- Receivers ..... −0.3V to (V_{CC} + 0.3V)
- Logic Pins ..... −0.3V to (V_{CC} + 0.3V)
- V_{EE} ..... −10V to 0.3V
- V_{DD} ..... −0.3V to 10V

Short-Circuit Duration

- Transmitter Output ..... Indefinite
- Receiver Output ..... Indefinite
- V_{EE} ..... 30 sec

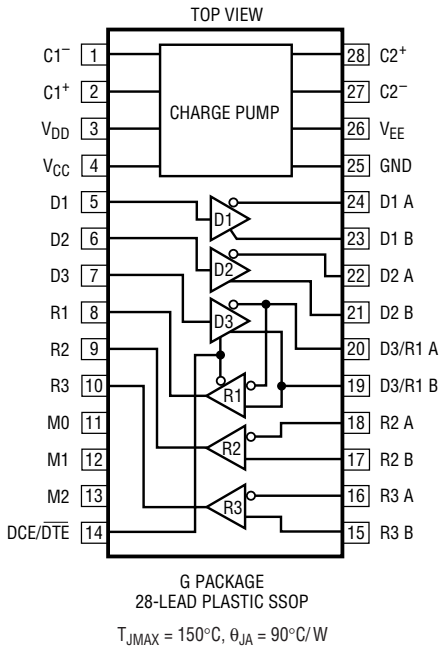
Operating Temperature Range

- LTC1543C ..... 0°C to 70°C
- LTC1543I ..... −40°C to 85°C

Storage Temperature Range ..... −65°C to 150°C

Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



G PACKAGE
28-LEAD PLASTIC SSOP

T_{JMAX} = 150°C, θ_{JA} = 90°C/W

ORDER PART NUMBER
LTC1543CG LTC1543IG

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range. V_{CC} = 5V (Notes 2, 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supplies							
I_{CC}	V_{CC} Supply Current (DCE Mode, All Digital Pins = GND or V_{CC})	RS530, RS530-A, X.21 Modes, No Load			13		mA
		RS530, RS530-A, X.21 Modes, Full Load	●		100	130	mA
		V.35 Mode, No Load			20		mA
		V.35 Mode, Full Load	●		126	170	mA
		V.28 Mode, No Load			20		mA
		V.28 Mode, Full Load	●		40	75	mA
		No-Cable Mode	●		120	500	µA
P_D	Internal Power Dissipation (DCE Mode)	RS530, RS530-A, X.21 Modes, Full Load			230		mW
		V.35 Mode, Full Load			600		mW
		V.28 Mode, Full Load			140		mW
V^+	Positive Charge Pump Output Voltage	Any Mode, No Load	●	8.0	9.4		V
		V.28 Mode, with Load	●	8.0	8.7		V
		V.28 Mode, with Load, I_{DD} = 10mA			6.5		V
V^-	Negative Charge Pump Output Voltage	V.28, V.35 Modes, No Load			−9.6		V
		V.28 Mode, Full Load	●	−8.0	−8.5		V
		V.35 Mode, Full Load	●	−5.5	−6.7		V
		RS530, RS530-A, X.21 Modes, Full Load	●	−4.5	−5.7		V
f_{OSC}	Charge Pump Oscillator Frequency				150		kHz
t_r	Supply Rise Time	No-Cable Mode or Power-Up to Turn On			2		ms
Logic Inputs and Outputs							
V_{IH}	Logic Input High Voltage		●	2			V
V_{IL}	Logic Input Low Voltage		●			0.8	V

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range. V_{CC} = 5V (Notes 2, 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{IN}	Logic Input Current	D1, D2, D3	●			±10	µA
		M0, M1, M2, DCE = GND (LTC1543C)	●	–100	–50	–30	µA
		M0, M1, M2, DCE = GND (LTC1543I)	●	–120	–50	–30	µA
		M0, M1, M2, DCE = V_{CC}	●			±10	µA
V_{OH}	Output High Voltage	I_O = –4mA	●	3	4.5		V
V_{OL}	Output Low Voltage	I_O = 4mA	●		0.3	0.8	V
I_{OSR}	Output Short-Circuit Current	0V ≤ V_O ≤ V_{CC}	●	–50		50	mA
I_{OZR}	Three-State Output Current	M0 = M1 = M2 = V_{CC}, 0V ≤ V_O ≤ V_{CC}			±1		µA
V.11 Driver							
V_{ODO}	Open Circuit Differential Output Voltage	R_L = 1.95k (Figure 1)	●			±5	V
V_{ODL}	Loaded Differential Output Voltage	R_L = 50Ω (Figure 1)		0.5V_{ODO}		0.67V_{ODO}	V
		R_L = 50Ω (Figure 1)	●	±2			V
ΔV_{OD}	Change in Magnitude of Differential Output Voltage	R_L = 50Ω (Figure 1)	●			0.2	V
V_{OC}	Common Mode Output Voltage	R_L = 50Ω (Figure 1)	●			3	V
ΔV_{OC}	Change in Magnitude of Common Mode Output Voltage	R_L = 50Ω (Figure 1)	●			0.2	V
I_{SS}	Short-Circuit Current	V_{OUT} = GND				150	mA
I_{OZ}	Output Leakage Current	–0.25V ≤ V_O ≤ 0.25V, Power Off or No-Cable Mode or Driver Disabled	●		±1	±100	µA
t_r, t_f	Rise or Fall Time	(Figures 2, 6) (LTC1543C)	●	2	15	25	ns
		(Figures 2, 6) (LTC1543I)	●	2	15	35	ns
t_{PLH}	Input to Output	(Figures 2, 6) (LTC1543C)	●	20	40	65	ns
		(Figures 2, 6) (LTC1543I)	●	20	40	75	ns
t_{PHL}	Input to Output	(Figures 2, 6) (LTC1543C)	●	20	40	65	ns
		(Figures 2, 6) (LTC1543I)	●	20	40	75	ns
Δt	Input to Output Difference, $\lvert t_{PLH} - t_{PHL} \rvert$	(Figures 2, 6) (LTC1543C)	●	0	3	12	ns
		(Figures 2, 6) (LTC1543I)	●	0	3	17	ns
t_{SKEW}	Output to Output Skew	(Figures 2, 6)			3		ns
V.11 Receiver							
V_{TH}	Input Threshold Voltage	–7V ≤ V_{CM} ≤ 7V	●	–0.2		0.2	V
ΔV_{TH}	Input Hysteresis	–7V ≤ V_{CM} ≤ 7V	●		15	40	mV
I_{IN}	Input Current (A, B)	–10V ≤ $V_{A,B}$ ≤ 10V	●			±0.66	mA
R_{IN}	Input Impedance	–10V ≤ $V_{A,B}$ ≤ 10V	●	15	30		kΩ
t_r, t_f	Rise or Fall Time	(Figures 2, 7)			15		ns
t_{PLH}	Input to Output	(Figures 2, 7) (LTC1543C)	●		50	80	ns
		(Figures 2, 7) (LTC1543I)	●		50	90	ns
t_{PHL}	Input to Output	(Figures 2, 7) (LTC1543C)	●		50	80	ns
		(Figures 2, 7) (LTC1543I)	●		50	90	ns
Δt	Input to Output Difference, $\lvert t_{PLH} - t_{PHL} \rvert$	(Figures 2, 7) (LTC1543C)	●	0	4	16	ns
		(Figures 2, 7) (LTC1543I)	●	0	4	21	ns
V.35 Driver							
V_{OD}	Differential Output Voltage	Open Circuit	●			±10.00	V
		With Load, –4V ≤ V_{CM} ≤ 4V (Figure 3)	●	±0.44	±0.55	±0.66	V
I_{OH}	Transmitter Output High Current	$V_{A, B}$ = 0V	●	–13	–11	–9.0	mA
I_{OL}	Transmitter Output Low Current	$V_{A, B}$ = 0V	●	9.0	11	13	mA

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range. V_{CC} = 5V (Notes 2, 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{OZ}	Transmitter Output Leakage Current	$-0.25V \le V_{A,B} \le 0.25V$	●		±1	±100	µA
t_r, t_f	Rise or Fall Time	(Figures 3, 6)			5		ns
t_{PLH}	Input to Output	(Figures 3, 6) (LTC1543C) (Figures 3, 6) (LTC1543I)	● ●	20 20	35 35	65 75	ns ns
t_{PHL}	Input to Output	(Figures 3, 6) (LTC1543C) (Figures 3, 6) (LTC1543I)	● ●	20 20	35 35	65 75	ns ns
Δt	Input to Output Difference, $\lvert t_{PLH} - t_{PHL} \rvert$	(Figures 3, 6) (LTC1543C) (Figures 3, 6) (LTC1543I)	● ●	0 0	4 4	16 21	ns ns
t_{SKEW}	Output to Output Skew	(Figures 3, 6)			4		ns
V.35 Receiver							
V_{TH}	Differential Receiver Input Threshold Voltage	$-2V \le (V_A + V_B)/2 \le 2V$ (Figure 3)	●	–0.2		0.2	V
ΔV_{TH}	Receiver Input Hysteresis	$-2V \le (V_A + V_B)/2 \le 2V$ (Figure 3)	●		15	40	mV
I_{IN}	Receiver Input Current (A, B)	$-10V \le V_{A,B} \le 10V$	●			±0.66	mA
R_{IN}	Receiver Input Impedance	$-10V \le V_{A,B} \le 10V$	●	15	30		kΩ
t_r, t_f	Rise or Fall Time	(Figures 3, 7)			15		ns
t_{PLH}	Input to Output	(Figures 3, 7) (LTC1543C) (Figures 3, 7) (LTC1543I)	● ●		50 50	80 90	ns ns
t_{PHL}	Input to Output	(Figures 3, 7) (LTC1543C) (Figures 3, 7) (LTC1543I)	● ●		50 50	80 90	ns ns
Δt	Input to Output Difference, $\lvert t_{PLH} - t_{PHL} \rvert$	(Figures 3, 7) (LTC1543C) (Figures 3, 7) (LTC1543I)	● ●	0 0	4 4	16 21	ns ns
V.28 Driver							
V_O	Output Voltage	Open Circuit R_L = 3k (Figure 4)	● ●	 ±5	 ±8.5	±10 	V V
I_{SS}	Short-Circuit Current	V_{OUT} = GND	●			±150	mA
I_{OZ}	Output Leakage Current	$-0.25V \le V_O \le 0.25V$, Power Off or No-Cable Mode or Driver Disabled	●		±1	±100	µA
SR	Slew Rate	R_L = 3k, C_L = 2500pF (Figures 4, 8)	●	4		30	V/µs
t_{PLH}	Input to Output	R_L = 3k, C_L = 2500pF (Figures 4, 8)	●		1.5	2.5	µs
t_{PHL}	Input to Output	R_L = 3k, C_L = 2500pF (Figures 4, 8)	●		1.5	3	µs
V.28 Receiver							
V_{THL}	Input Low Threshold Voltage		●		1.2	0.8	V
V_{TLH}	Input High Threshold Voltage		●	2	1.2		V
ΔV_{TH}	Receiver Input Hysteresis		●	0	0.05	0.3	V
R_{IN}	Receiver Input Impedance	$-15V \le V_A \le 15V$	●	3	5	7	kΩ
t_r, t_f	Rise or Fall Time	(Figures 5, 9)			15		ns
t_{PLH}	Input to Output	(Figures 5, 9)	●		60	100	ns
t_{PHL}	Input to Output	(Figures 5, 9)	●		160	250	ns

Note 1: Absolute Maximum Ratings are those beyond which the safety of a device may be impaired.

Note 2: All currents into device pins are positive; all currents out of device are negative. All voltages are referenced to device ground unless otherwise specified.

Note 3: All typicals are given for V_{CC} = 5V, C1 = C2 = C_{VCC} = 1µF, C_{VDD} = C_{VEE} = 3.3µF tantalum capacitors and T_A = 25°C.

PIN FUNCTIONS

C1⁻ (Pin 1): Capacitor C1 Negative Terminal. Connect a 1µF capacitor between C1⁺ and C1⁻.

C1⁺ (Pin 2): Capacitor C1 Positive Terminal. Connect a 1µF capacitor between C1⁺ and C1⁻.

V_{DD} (Pin 3): Generated Positive Supply Voltage for V.28. Connect a 1µF capacitor to ground.

V_{CC} (Pin 4): Positive Supply Voltage Input. 4.75V ≤ V_{CC} ≤ 5.25V. Bypass with a 1µF capacitor to ground.

D1 (Pin 5): TTL Level Driver 1 Input.

D2 (Pin 6): TTL Level Driver 2 Input.

D3 (Pin 7): TTL Level Driver 3 Input.

R1 (Pin 8): CMOS Level Receiver 1 Output.

R2 (Pin 9): CMOS Level Receiver 2 Output.

R3 (Pin 10): CMOS Level Receiver 3 Output.

M0 (Pin 11): TTL Level Mode Select Input 0 with Pull-Up to V_{CC}.

M1 (Pin 12): TTL Level Mode Select Input 1 with Pull-Up to V_{CC}.

M2 (Pin 13): TTL Level Mode Select Input 2 with Pull-Up to V_{CC}.

DCE/$\overline{\text{DTE}}$ (Pin 14): TTL Level Mode Select Input with Pull-Up to V_{CC}.

R3 B (Pin 15): Receiver 3 Noninverting Input with Pull-Up to V_{CC}.

R3 A (Pin 16): Receiver 3 Inverting Input.

R2 B (Pin 17): Receiver 2 Noninverting Input.

R2 A (Pin 18): Receiver 2 Inverting Input.

D3/R1 B (Pin 19): Receiver 1 Noninverting Input and Driver 3 Noninverting Output.

D3/R1 A (Pin 20): Receiver 1 Inverting Input and Driver 3 Inverting Output.

D2 B (Pin 21): Driver 2 Noninverting Output.

D2 A (Pin 22): Driver 2 Inverting Output.

D1 B (Pin 23): Driver 1 Noninverting Output.

D1 A (Pin 24): Driver 1 Inverting Output.

GND (Pin 25): Ground.

V_{EE} (Pin 26): Negative Supply Voltage. Connect a 3.3µF capacitor to GND.

C2⁻ (Pin 27): Capacitor C2 Negative Terminal. Connect a 1µF capacitor between C2⁺ and C2⁻.

C2⁺ (Pin 28): Capacitor C2 Positive Terminal. Connect a 1µF capacitor between C2⁺ and C2⁻.

TEST CIRCUITS

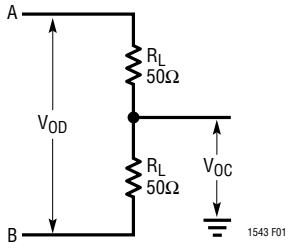


Figure 1. V.11 Driver Test Circuit

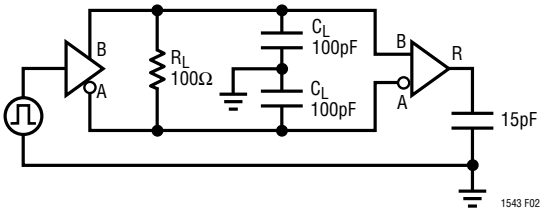


Figure 2. V.11 Driver/Receiver AC Test Circuit

TEST CIRCUITS

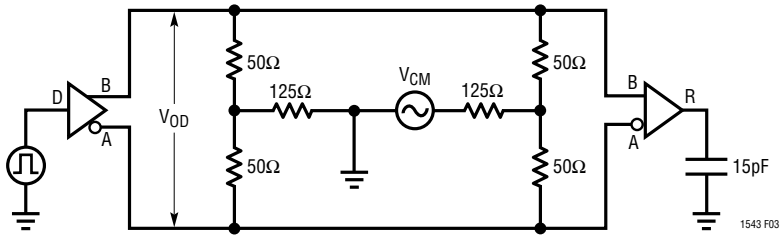


Figure 3. V.35 Driver/Receiver Test Circuit

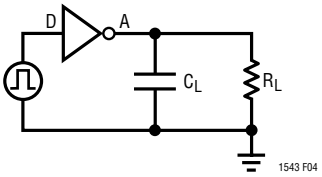


Figure 4. V.10/V.28 Driver Test Circuit

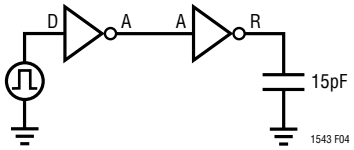


Figure 5. V.10/V.28 Receiver Test Circuit

MODE SELECTION

LTC1543 MODE NAME	M2	M1	M0	DCE/$\overline{\text{DTE}}$	D1	D2	D3	R1	R2	R3
Not Used (Default V.11)	0	0	0	0	V.11	V.11	Z	V.11	V.11	V.11
RS530A	0	0	1	0	V.11	V.11	Z	V.11	V.11	V.11
RS530	0	1	0	0	V.11	V.11	Z	V.11	V.11	V.11
X.21	0	1	1	0	V.11	V.11	Z	V.11	V.11	V.11
V.35	1	0	0	0	V.35	V.35	Z	V.35	V.35	V.35
RS449/V.36	1	0	1	0	V.11	V.11	Z	V.11	V.11	V.11
V.28/RS232	1	1	0	0	V.28	V.28	Z	V.28	V.28	V.28
No Cable	1	1	1	0	Z	Z	Z	Z	Z	Z
Not Used (Default V.11)	0	0	0	1	V.11	V.11	V.11	Z	V.11	V.11
RS530A	0	0	1	1	V.11	V.11	V.11	Z	V.11	V.11
RS530	0	1	0	1	V.11	V.11	V.11	Z	V.11	V.11
X.21	0	1	1	1	V.11	V.11	V.11	Z	V.11	V.11
V.35	1	0	0	1	V.35	V.35	V.35	Z	V.35	V.35
RS449/V.36	1	0	1	1	V.11	V.11	V.11	Z	V.11	V.11
V.28/RS232	1	1	0	1	V.28	V.28	V.28	Z	V.28	V.28
No Cable	1	1	1	1	Z	Z	Z	Z	Z	Z

SWITCHING TIME WAVEFORMS

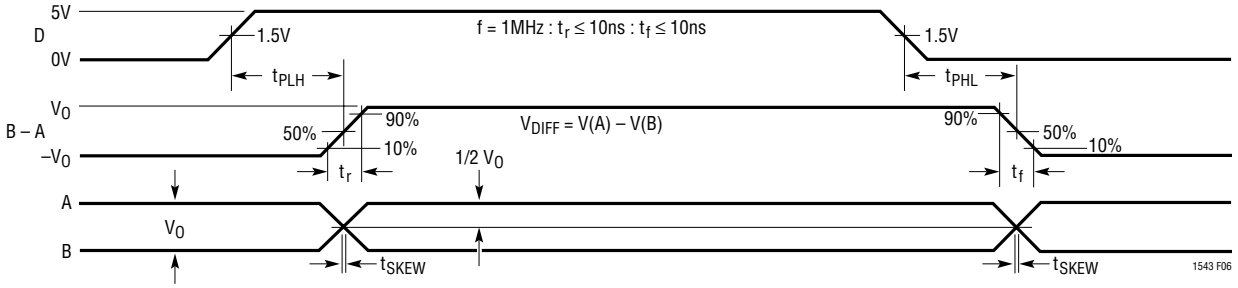


Figure 6. V.11, V.35 Driver Propagation Delays

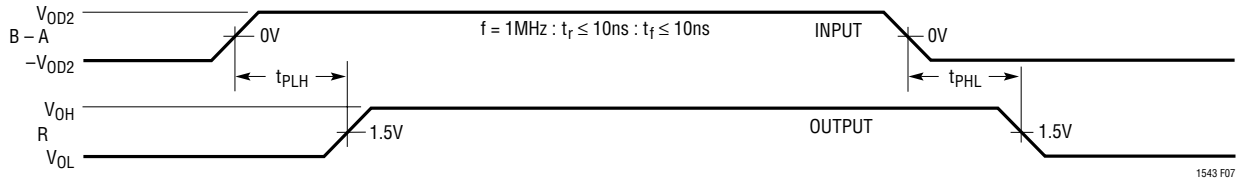


Figure 7. V.11, V.35 Receiver Propagation Delays

Figure 8. V.10, V.28 Driver Propagation Delays

Figure 9. V.10, V.28 Receiver Propagation Delays

APPLICATIONS INFORMATION

Overview

The LTC1543/LTC1544 form the core of a complete software-selectable DTE or DCE interface port that supports the RS232, RS449, EIA530, EIA530-A, V.35, V.36 or X.21 protocols. Cable termination may be implemented using the LTC1344A software-selectable cable termination chip or by using existing discrete designs.

A complete DCE-to-DTE interface operating in EIA530 mode is shown in Figure 10. The LTC1543 of each port is used to generate the clock and data signals. The LTC1544 is used to generate the control signals along with LL (Local Loopback).The LTC1344A cable termination chip is used only for the clock and data signals because they must support V.35 cable termination. The control signals do not need any external resistors.

Mode Selection

The interface protocol is selected using the mode select pins M0, M1 and M2 (see the Mode Selection table).

For example, if the port is configured as a V.35 interface, the mode selection pins should be M2 = 1, M1 = 0, M0 = 0. For the control signals, the drivers and receivers will operate in V.28 (RS232) electrical mode. For the clock and data signals, the drivers and receivers will operate in V.35 electrical mode. The DCE/$\overline{\text{DTE}}$ pin will configure the port for DCE mode when high, and DTE when low.

The interface protocol may be selected simply by plugging the appropriate interface cable into the connector. The mode pins are routed to the connector and are left unconnected (1) or wired to ground (0) in the cable as shown in Figure 11.

The internal pull-up current sources will ensure a binary 1 when a pin is left unconnected and that the LTC1543/LTC1544 and the LTC1344A enter the no-cable mode when the cable is removed. In the no-cable mode the LTC1543/LTC1544 supply current drops to less than 200µA and all LTC1543/LTC1544 driver outputs and LTC1344A resistive terminations are forced into a high impedance state.

The mode selection may also be accomplished by using jumpers to connect the mode pins to ground or V_{CC}.

Cable Termination

Traditional implementations have included switching resistors with expensive relays, or requiring the user to change termination modules every time the interface standard has changed. Custom cables have been used with the termination in the cable head or separate terminations are built on the board and a custom cable routes the signals to the appropriate termination. Switching the terminations with FETs is difficult because the FETs must remain off even though the signal voltage is beyond the supply voltage for the FET drivers or the power is off.

Using the LTC1344A along with the LTC1543/LTC1544 solves the cable termination switching problem. Via software control, the LTC1344A provides termination for the V.10 (RS423), V.11 (RS422), V.28 (RS232) and V.35 electrical protocols.

V.10 (RS423) Interface

A typical V.10 unbalanced interface is shown in Figure 12. A V.10 single-ended generator output A with ground C is connected to a differential receiver with inputs A' connected to A, and input C' connected to the signal return ground C. Usually, no cable termination is required for V.10 interfaces, but the receiver inputs must be compliant with the impedance curve shown in Figure 13.

The V.10 receiver configuration in the LTC1544 is shown in Figure 14. In V.10 mode switch S3 inside the LTC1544 is turned off.The noninverting input is disconnected inside the LTC1544 receiver and connected to ground. The cable termination is then the 30k input impedance to ground of the LTC1544 V.10 receiver.

APPLICATIONS INFORMATION

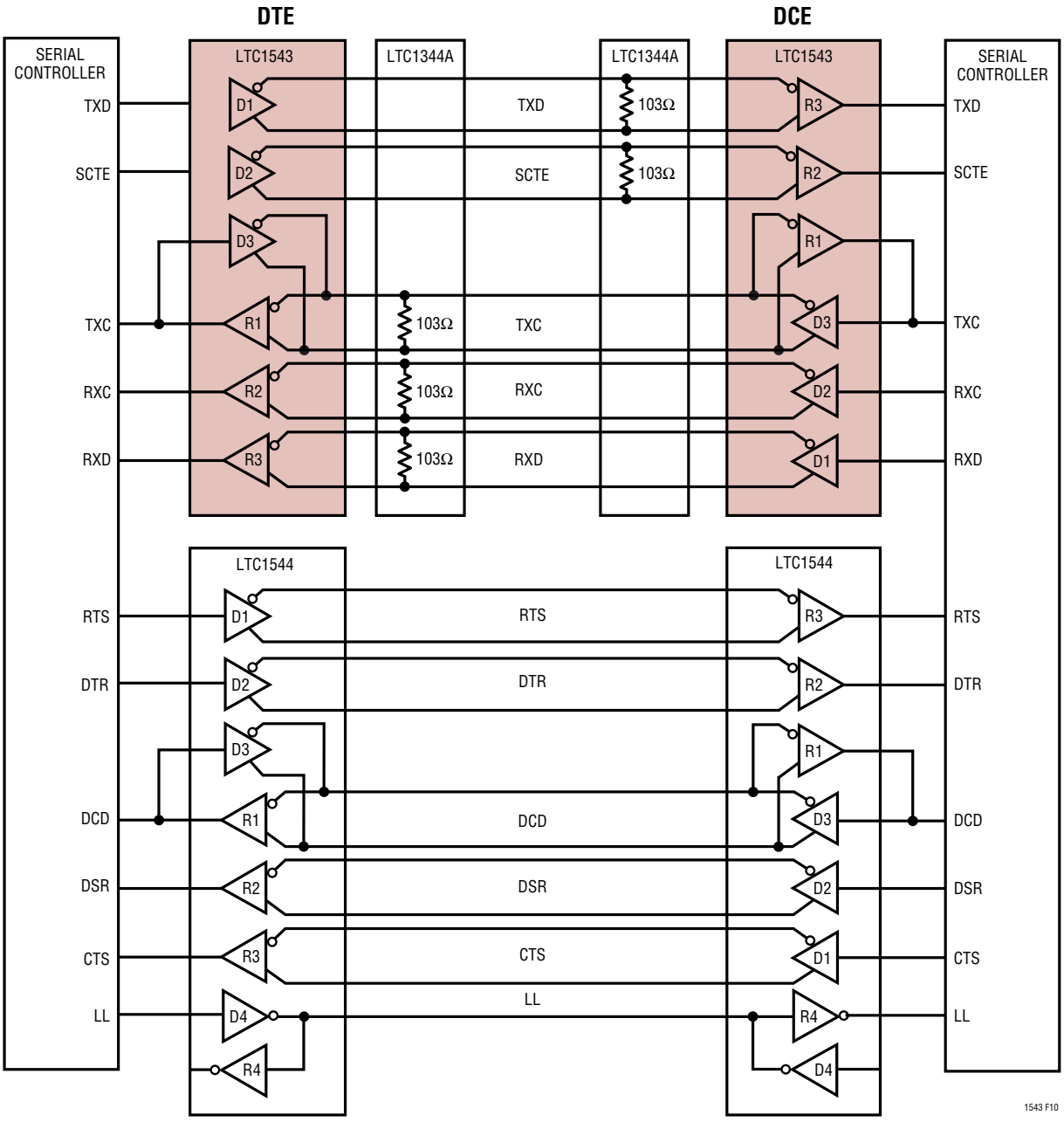


Figure 10. Complete Multiprotocol Interface in EIA530 Mode

APPLICATIONS INFORMATION

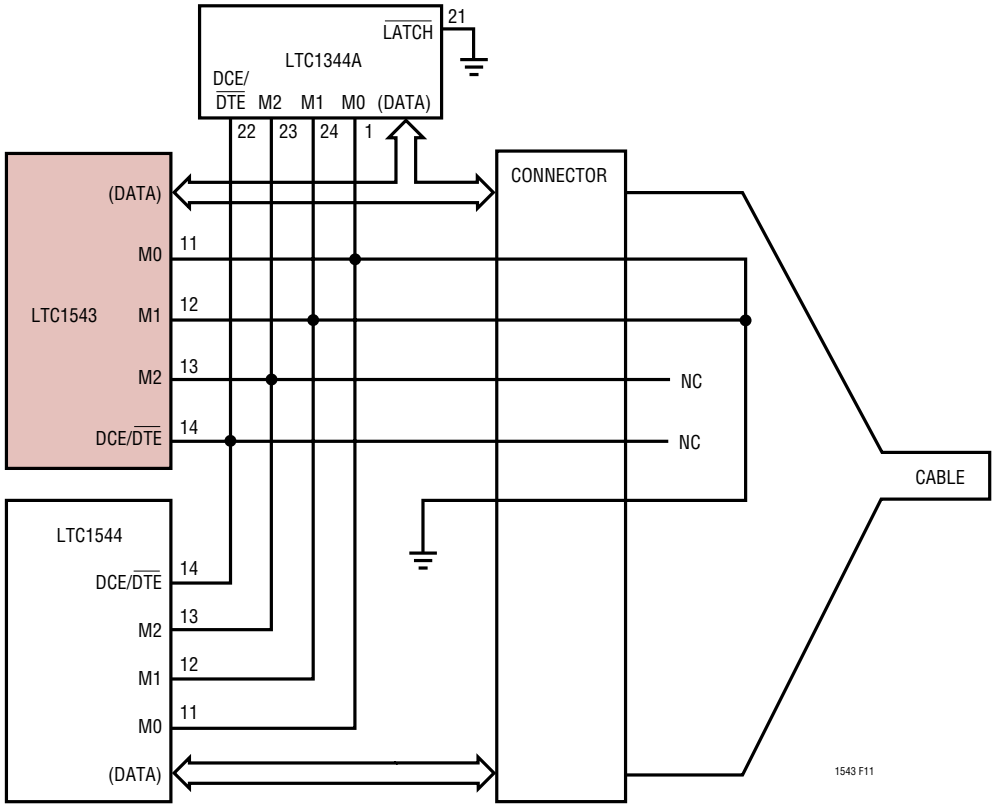


Figure 11. Single Port DCE V.35 Mode Selection in the Cable

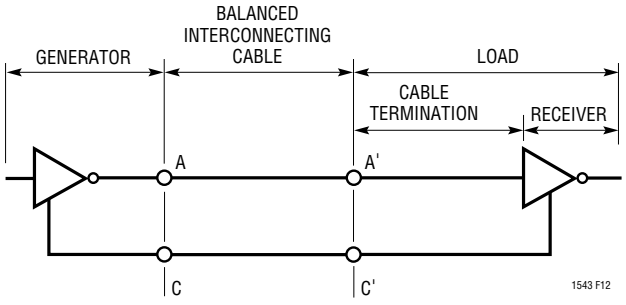


Figure 12. Typical V.10 Interface

APPLICATIONS INFORMATION

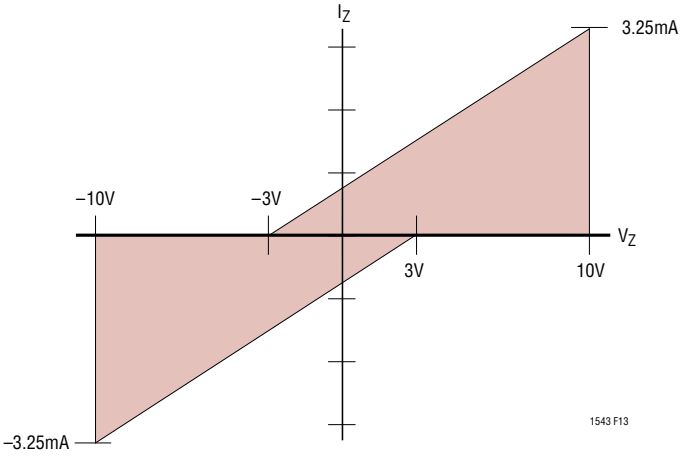


Figure 13. V.10 Receiver Input Impedance

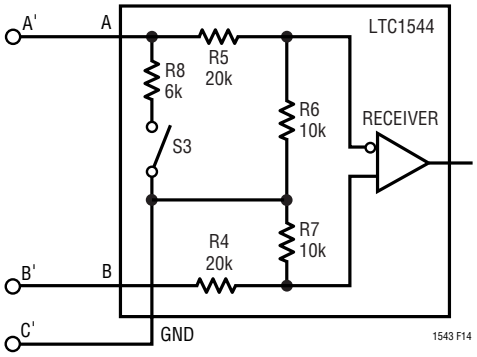


Figure 14. V.10 Receiver Configuration

V.11 (RS422) Interface

A typical V.11 balanced interface is shown in Figure 15. A V.11 differential generator with outputs A and B with ground C is connected to a differential receiver with ground C', inputs A' connected to A, B' connected to B. The V.11 interface has a differential termination at the receiver end that has a minimum value of 100Ω. The termination resistor is optional in the V.11 specification, but for the high speed clock and data lines, the termination is required to prevent reflections from corrupting the data. The receiver inputs must also be compliant with the impedance curve shown in Figure 13.

In V.11 mode, all switches are off except S1 inside the LTC1344A which connects a 103Ω differential termination impedance to the cable as shown in Figure 16.

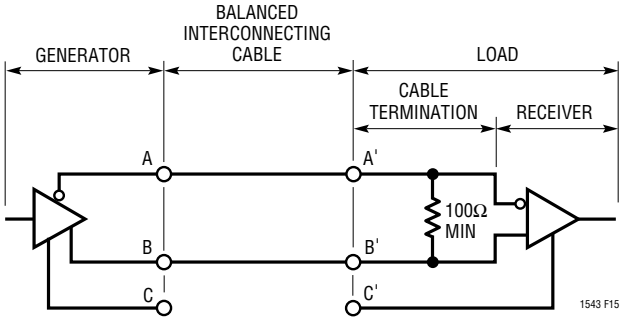


Figure 15. Typical V.11 Interface

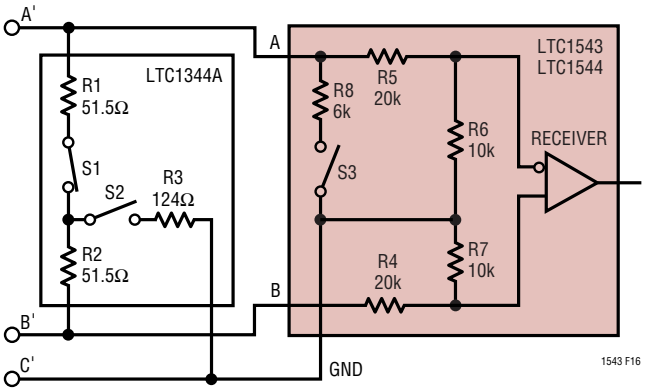


Figure 16. V.11 Receiver Configuration

APPLICATIONS INFORMATION

V.28 (RS232) Interface

A typical V.28 unbalanced interface is shown in Figure 17. A V.28 single-ended generator output A with ground C is connected to a single-ended receiver with input A' connected to A, ground C' connected via the signal return ground C.

In V.28 mode all switches are off except S3 inside the LTC1543/LTC1544 which connects a 6k (R8) impedance to ground in parallel with 20k (R5) plus 10k (R6) for a combined impedance of 5k as shown in Figure 18. The noninverting input is disconnected inside the LTC1543/LTC1544 receiver and connected to a TTL level reference voltage for a 1.4V receiver trip point.

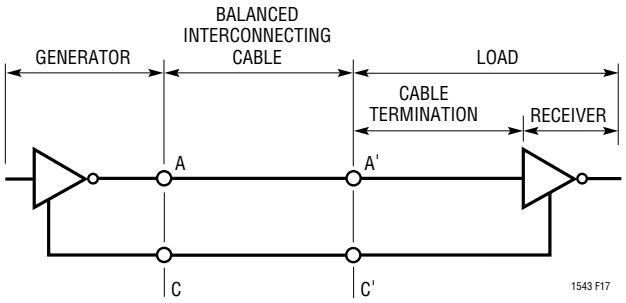


Figure 17. Typical V.28 Interface

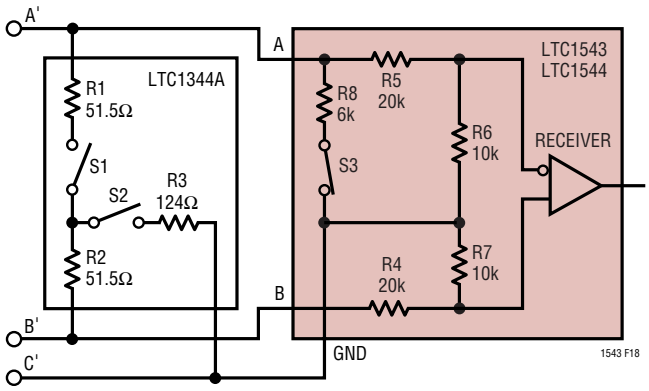


Figure 18. V.28 Receiver Configuration

V.35 Interface

A typical V.35 balanced interface is shown in Figure 19. A V.35 differential generator with outputs A and B with ground C is connected to a differential receiver with ground C', inputs A' connected to A, B' connected to B. The V.35 interface requires a T or delta network termination at the receiver end and the generator end. The receiver differential impedance measured at the connector must be 100Ω ±10Ω, and the impedance between shorted terminals (A' and B') and ground C' must be 150Ω ±15Ω.

In V.35 mode, both switches S1 and S2 inside the LTC1344A are on, connecting the T network impedance as shown in Figure 20. The switch in the LTC1543 is off. The 30k input

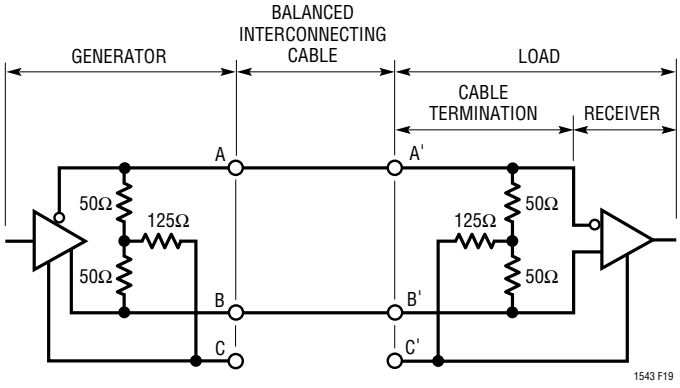


Figure 19. Typical V.35 Interface

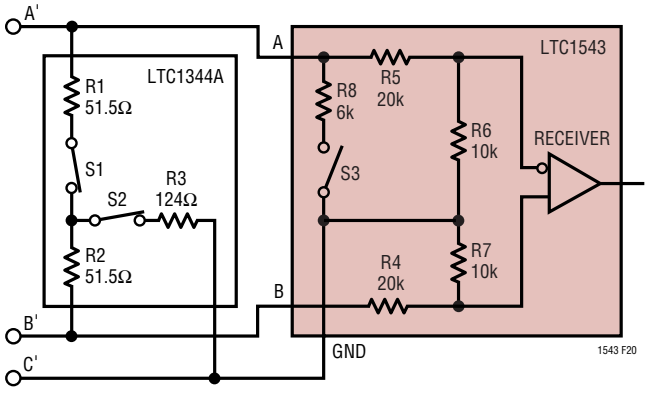


Figure 20. V.35 Receiver Configuration

APPLICATIONS INFORMATION

impedance of the receiver is placed in parallel with the T network termination, but does not affect the overall input impedance significantly.

The generator differential impedance must be 50Ω to 150Ω and the impedance between shorted terminals (A and B) and ground C must be 150Ω ±15Ω. For the generator termination, switches S1 and S2 are both on and the top side of the center resistor is brought out to a pin so it can be bypassed with an external capacitor to reduce common mode noise as shown in Figure 21.

Any mismatch in the driver rise and fall times or skew in the driver propagation delays will force current through the center termination resistor to ground, causing a high frequency common mode spike on the A and B terminals. The common mode spike can cause EMI problems that are reduced by capacitor C1 which shunts much of the common mode energy to ground rather than down the cable.

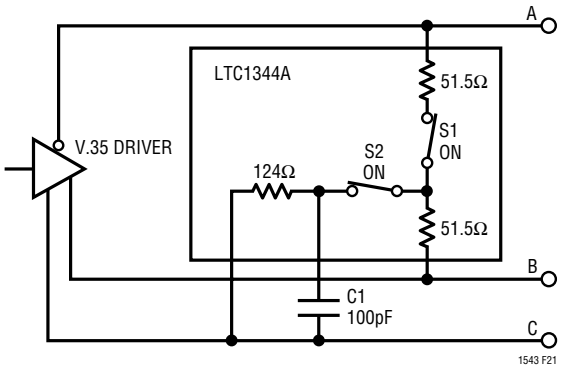


Figure 21. V.35 Driver Using the LTC1344A

No-Cable Mode

The no-cable mode (M0 = M1 = M2 = 1) is intended for the case when the cable is disconnected from the connector. The charge pump, bias circuitry, drivers and receivers are turned off, the driver outputs are forced into a high impedance state, and the supply current drops to less than 200µA.

Charge Pump

The LTC1543 uses an internal capacitive charge pump to generate V_{DD} and V_{EE} as shown in Figure 22. A voltage doubler generates about 8V on V_{DD} and a voltage inverter generates about –7.5V for V_{EE}. Four 1µF surface mounted tantalum or ceramic capacitors are required for C1, C2, C3 and C4. The V_{EE} capacitor C5 should be a minimum of 3.3µF. All capacitors are 16V and should be placed as close as possible to the LTC1543 to reduce EMI.

Receiver Fail-Safe

All LTC1543/LTC1544 receivers feature fail-safe operation in all modes. If the receiver inputs are left floating or shorted together by a termination resistor, the receiver output will always be forced to a logic high.

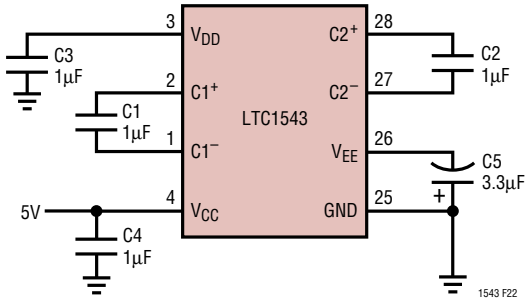


Figure 22. Charge Pump

APPLICATIONS INFORMATION

DTE vs DCE Operation

The DCE/$\overline{DTE}$ pin acts as an enable for Driver 3/Receiver 1 in the LTC1543, and Driver 3/Receiver 1 and Driver 4/Receiver 4 in the LTC1544. The INVERT pin in the LTC1544 allows the Driver 4/Receiver 4 enable to be high or low true polarity.

The LTC1543/LTC1544 can be configured for either DTE or DCE operation in one of two ways: a dedicated DTE or DCE port with a connector of appropriate gender or a port with one connector that can be configured for DTE or DCE operation by rerouting the signals to the LTC1543/LTC1544 using a dedicated DTE cable or dedicated DCE cable.

A dedicated DTE port using a DB-25 male connector is shown in Figure 23. The interface mode is selected by logic outputs from the controller or from jumpers to either V_{CC} or GND on the mode select pins. A dedicated DCE port using a DB-25 female connector is shown in Figure 24.

A port with one DB-25 connector, but can be configured for either DTE or DCE operation is shown in Figure 25. The configuration requires separate cables for proper signal routing in DTE or DCE operation. For example, in DTE mode, the TXD signal is routed to Pins 2 and 14 via Driver 1 in the LTC1543. In DCE mode, Driver 1 now routes the RXD signal to Pins 2 and 14.

Multiprotocol Interface with RL, LL, TM and a DB-25 Connector

If the RL, LL and TM signals are implemented, there are not enough drivers and receivers available in the LTC1543/LTC1544. In Figure 26, the required control signals are handled by the LTC1544 but the clock/data signals use the LTC1343. The LTC1343 has an additional single-ended driver/receiver pair that can handle two more optional control signals such as TM and LL.

Cable-Selectable Multiprotocol Interface

A cable-selectable multiprotocol DTE/DCE interface is shown in Figure 27. The select lines M0, M1 and DCE/$\overline{DTE}$ are brought out to the connector. The mode is selected by the cable by wiring M0 (connector Pin 18) and M1 (connector Pin 21) and DCE/$\overline{DTE}$ (connector Pin 25) to ground (connector Pin 7) or letting them float. If M0, M1 or DCE/$\overline{DTE}$ is floating, internal pull-up current sources will pull the signals to V_{CC}. The select bit M2 is hard wired to V_{CC}. When the cable is pulled out, the interface will go into the no-cable mode.

Compliance Testing

A European standard EN 45001 test report is available for the LTC1543/LTC1544/LTC1344A chipset. A copy of the test report is available from LTC or TUV Telecom Services Inc. (formerly Detecon Inc.)

The title of the report is:

Test Report No. NET2/102201/97.

The address of TUV Telecom Services Inc. is:

TUV Telecom Services Inc.
Type Approval Division
1775 Old Highway 8, Ste 107
St. Paul, MN 55112 USA
Tel. +1 (612) 639-0775
Fax. +1 (612) 639-0873

TYPICAL APPLICATIONS

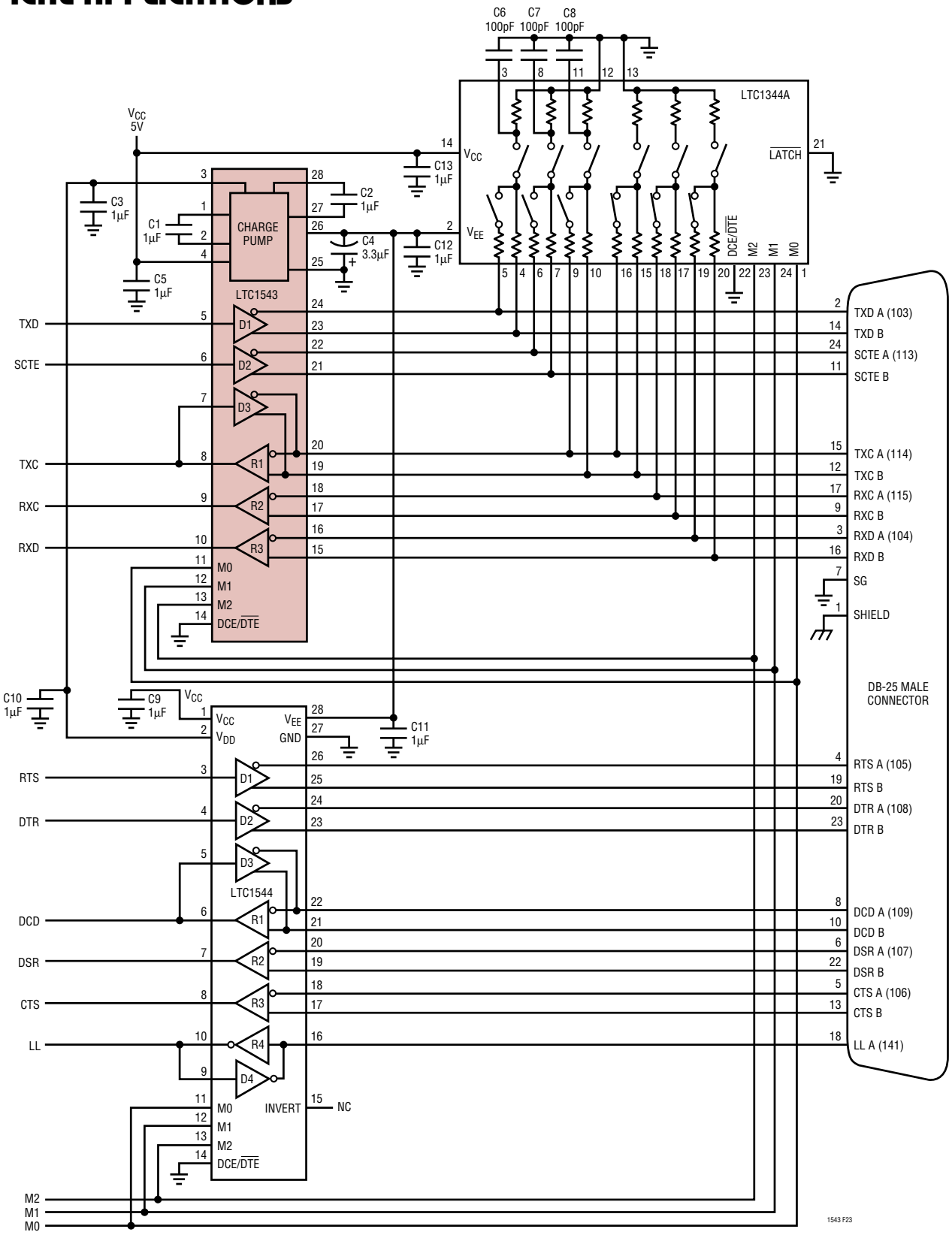


Figure 23. Controller-Selectable Multiprotocol DTE Port with DB-25 Connector

TYPICAL APPLICATIONS

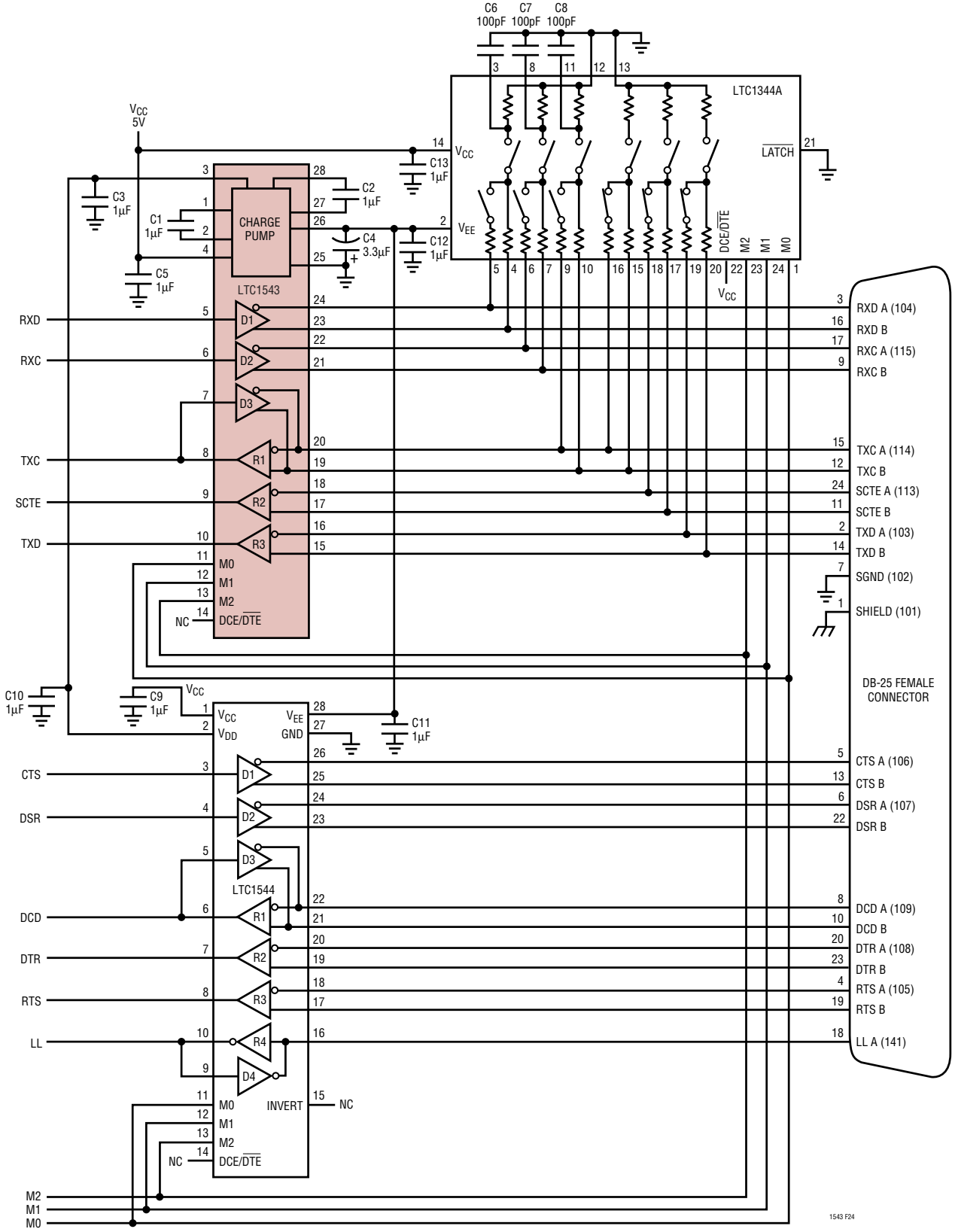


Figure 24. Controller-Selectable DCE Port with DB-25 Connector

TYPICAL APPLICATIONS

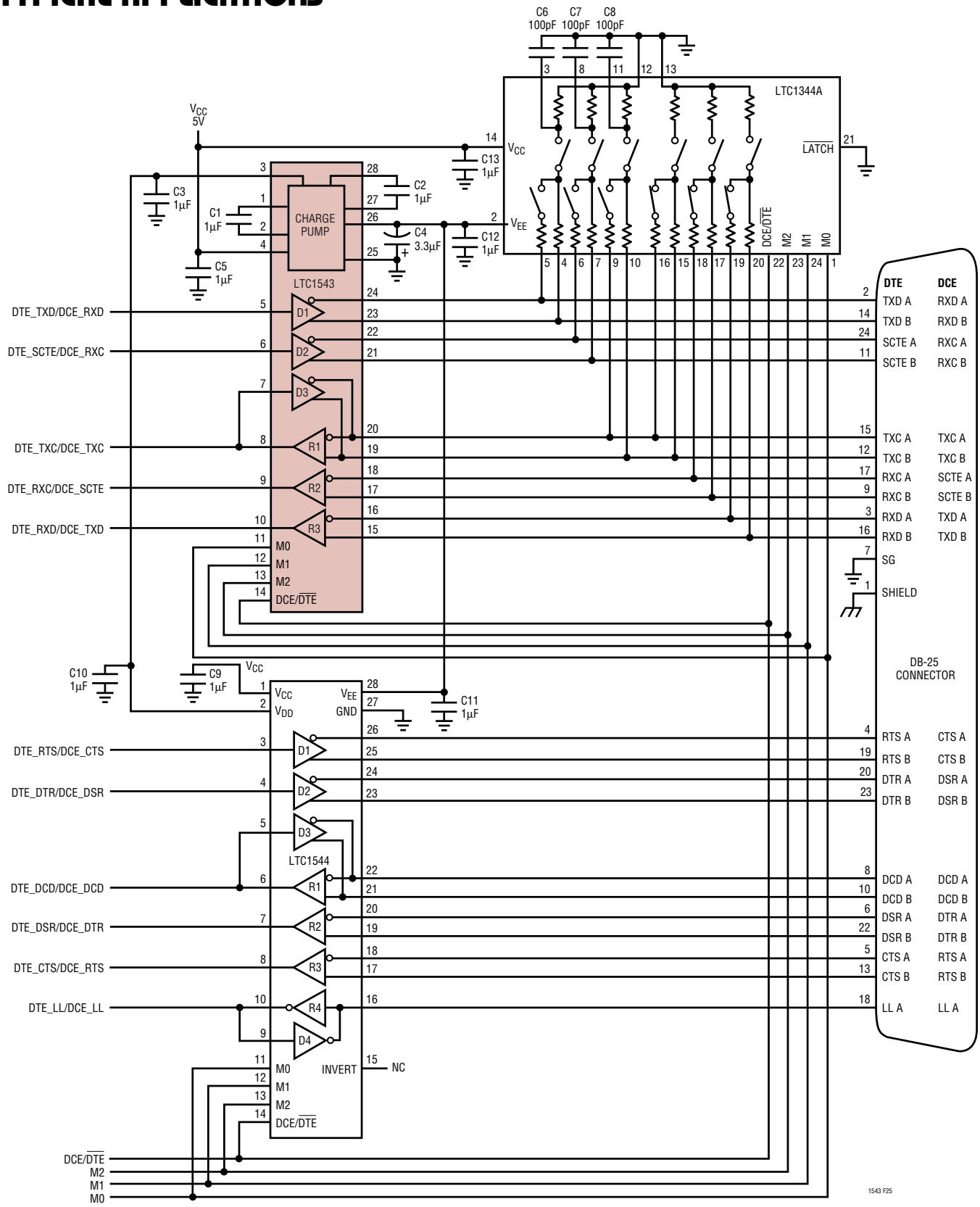


Figure 25. Controller-Selectable Multiprotocol DTE/DCE Port with DB-25 Connector

TYPICAL APPLICATIONS

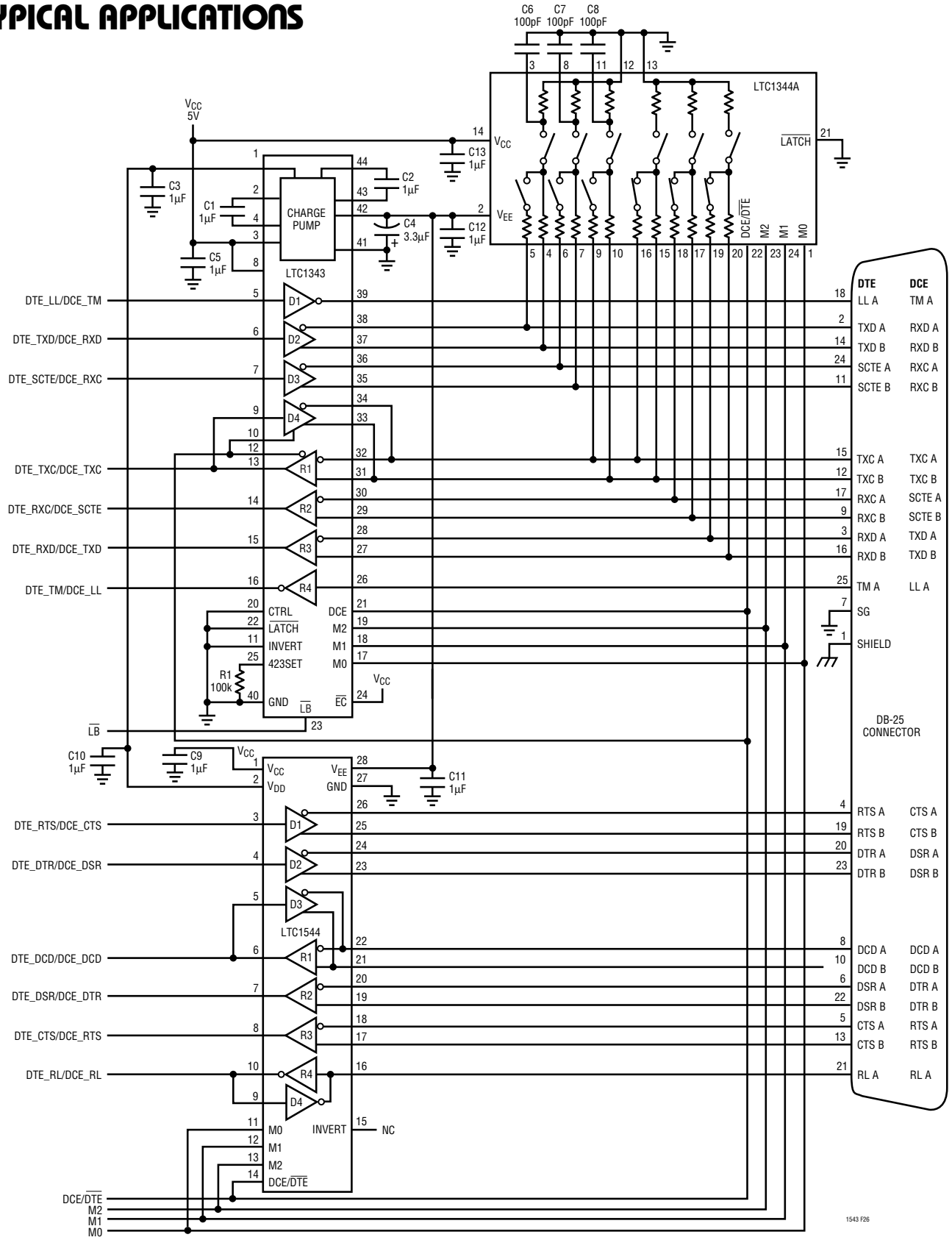
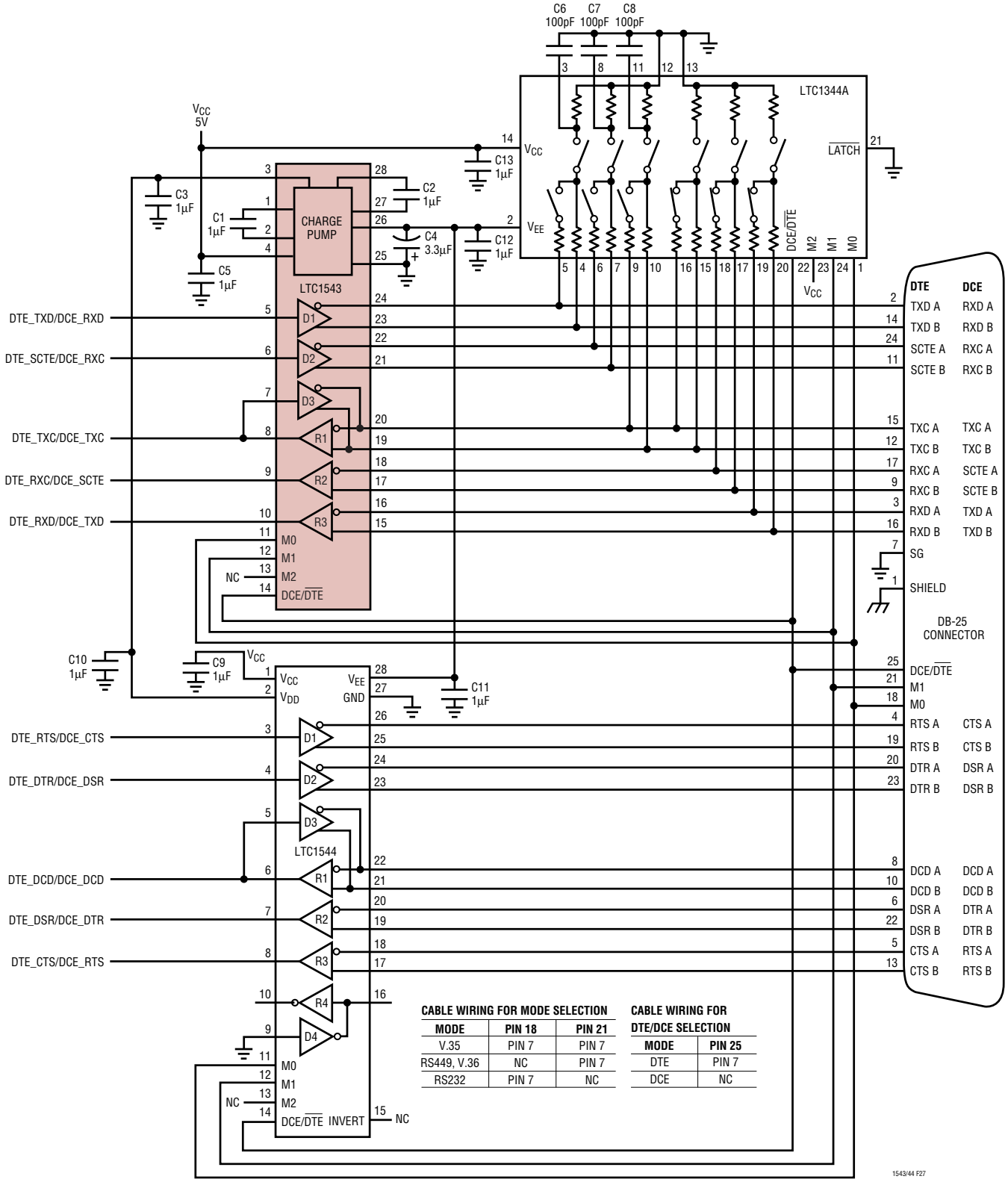


Figure 26. Controller-Selectable Multiprotocol DTE/DCE Port with RL, LL, TM and DB-25 Connector

TYPICAL APPLICATIONS



CABLE WIRING FOR MODE SELECTION

MODE	PIN 18	PIN 21
V.35	PIN 7	PIN 7
RS449, V.36	NC	PIN 7
RS232	PIN 7	NC

CABLE WIRING FOR DTE/DCE SELECTION

MODE	PIN 25
DTE	PIN 7
DCE	NC

Figure 27. Cable-Selectable Multiprotocol DTE/DCE Port with DB-25 Connector