Software-Selectable Multiprotocol Transceiver

FEATURES

- **Software-Selectable Transceiver Supports: RS232, RS449, EIA530, EIA530-A, V.35, V.36, X.21**
- **TUV/Detecon Inc. Certified NET1 and NET2 Compliant (Test Report No. NET2/071601/98)**
- **TBR2 Compliant (Test Report No. CTR2/071601/98)**
- Software-Selectable Cable Termination Using the LTC1344A
- Complete DTE or DCE Port with LTC1543, LTC1344A
- Operates from Single 5V Supply with LTC1543

APPLICATIONS

- Data Networking
- CSU and DSU
- Data Routers

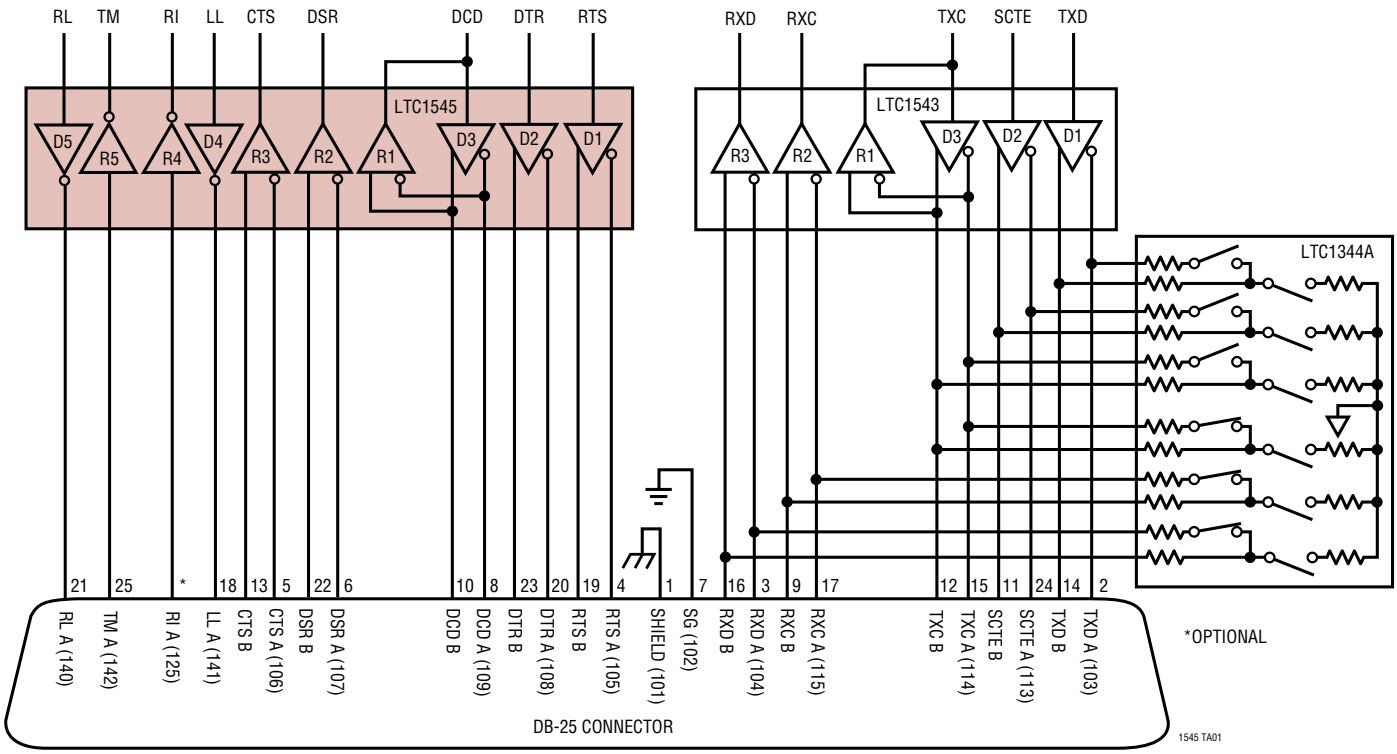
DESCRIPTION

The LTC®1545 is a 5-driver/5-receiver multiprotocol transceiver. The LTC1545 and LTC1543 form the core of a complete software-selectable DTE or DCE interface port that supports the RS232, RS449, EIA530, EIA530-A, V.35, V.36 or X.21 protocols. Cable termination may be implemented using the LTC1344A software-selectable cable termination chip or by using existing discrete designs.

The LTC1545 runs from a 5V supply and the charge pump on the LTC1543. The part is available in a 36-lead SSOP surface mount package.

TYPICAL APPLICATION

DTE or DCE Multiprotocol Serial Interface with DB-25 Connector



ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage
- V_{CC} 6.5V
- V_{EE} ..... –10V to 0.3V
- V_{DD} ..... –0.3V to 10V

Input Voltage
- Transmitters ..... –0.3V to (V_{CC} + 0.3V)
- Receivers ..... –18V to 18V
- Logic Pins ..... –0.3V to (V_{CC} + 0.3V)

Output Voltage
- Transmitters ..... (V_{EE} – 0.3V) to (V_{DD} + 0.3V)
- Receivers ..... –0.3V to (V_{CC} + 0.3V)

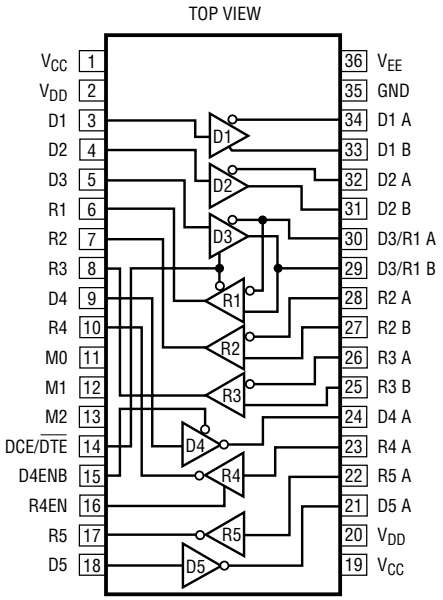
Short-Circuit Duration
- Transmitter Output ..... Indefinite
- Receiver Output ..... Indefinite
- V_{EE} ..... 30 sec

Operating Temperature Range
- LTC1545C ..... 0°C to 70°C
- LTC1545I ..... –40°C to 85°C

Storage Temperature Range ..... –65°C to 150°C

Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



G PACKAGE
36-LEAD PLASTIC SSOP

T_{JMAX} = 150°C, θ_{JA} = 65°C/ W

ORDER PART NUMBER
LTC1545CG LTC1545IG

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 5V, V_{DD} = 8V, V_{EE} = – 7V for V.28, –5.5V for V.10, V.11 (Notes 2, 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supplies							
I_{CC}	V_{CC} Supply Current (DCE Mode, All Digital Pins = GND or V_{CC})	RS530, RS530-A, X.21 Modes, No Load	●		2.7	5	mA
		RS530, RS530-A, X.21 Modes, Full Load	●		110	150	mA
		V.28 Mode, No Load	●		1	3	mA
		V.28 Mode, Full Load	●		1	3	mA
		No-Cable Mode, D4ENB = HIGH	●		10	500	µA
I_{EE}	V_{EE} Supply Current (DCE Mode, All Digital Pins = GND or V_{CC})	RS530, RS530-A, X.21 Modes, No Load	●		2.0	4.0	mA
		RS530, X.21 Modes, Full Load	●		23	35	mA
		RS530-A, Full Load	●		34	50	mA
		V.28 Mode, No Load	●		1	3	mA
		V.28 Mode, Full Load	●		12	18	mA
		No-Cable Mode, D4ENB = HIGH	●		10	500	µA
I_{DD}	V_{DD} Supply Current (DCE Mode, All Digital Pins = GND or V_{CC})	RS530, RS530-A, X.21 Modes, NoLoad	●		0.3	2	mA
		RS530, RS530-A, X.21 Modes, Full Load	●		0.3	2	mA
		V.28 Mode, No Load	●		1	3	mA
		V.28 Mode, Full Load	●		13.5	18	mA
		No-Cable Mode, D4ENB = HIGH	●		10	500	µA
P_D	Internal Power Dissipation (DCE Mode, (All Digital Pins = GND or V_{CC})	RS530, RS530-A, X.21 Modes, Full Load			340		mW
		V.28 Mode, Full Load			64		mW

ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Logic Inputs and Outputs							
V_{IH}	Logic Input High Voltage		●	2			V
V_{IL}	Logic Input Low Voltage		●			0.8	V
I_{IN}	Logic Input Current	D1, D2, D3, D4, D5	●			±10	µA
		M0, M1, M2, DCE, D4ENB, R4EN = GND (LTC1545C)	●	–100	–50	–30	µA
		M0, M1, M2, DCE, D4ENB, R4EN = GND (LTC1545I)	●	–120	–50	–30	µA
		M0, M1, M2, DCE, D4ENB, R4EN = V_{CC}	●			±10	µA
V_{OH}	Output High Voltage	I_O = –4mA	●	3	4.5		V
V_{OL}	Output Low Voltage	I_O = 4mA	●		0.3	0.8	V
I_{OSR}	Output Short-Circuit Current	0V ≤ V_O ≤ V_{CC}	●	–50	40	50	mA
I_{OZR}	Three-State Output Current	M0 = M1 = M2 = V_{CC}, 0V ≤ V_O ≤ V_{CC}			±1		µA
V.11 Driver							
V_{ODO}	Open Circuit Differential Output Voltage	R_L = 1.95k (Figure 1)	●			±5	V
V_{ODL}	Loaded Differential Output Voltage	R_L = 50Ω (Figure 1)		0.5V_{ODO}		0.67V_{ODO}	
		R_L = 50Ω (Figure 1)	●	±2			V
ΔV_{OD}	Change in Magnitude of Differential Output Voltage	R_L = 50Ω (Figure 1)	●			0.2	V
V_{OC}	Common Mode Output Voltage	R_L = 50Ω (Figure 1)	●			3	V
ΔV_{OC}	Change in Magnitude of Common Mode Output Voltage	R_L = 50Ω (Figure 1)	●			0.2	V
I_{SS}	Short-Circuit Current	V_{OUT} = GND				±150	mA
I_{OZ}	Output Leakage Current	–0.25V ≤ V_O ≤ 0.25V, Power Off or No-Cable Mode or Driver Disabled	●		±1	±100	µA
t_r, t_f	Rise or Fall Time	LTC1545C (Figures 2, 5)	●	2	15	25	ns
		LTC1545I (Figures 2, 5)	●	2	15	35	ns
t_{PLH}	Input to Output	LTC1545C (Figures 2, 5)	●	20	40	65	ns
		LTC1545I (Figures 2, 5)	●	20	40	75	ns
t_{PHL}	Input to Output	LTC1545C (Figures 2, 5)	●	20	40	65	ns
		LTC1545I (Figures 2, 5)	●	20	40	75	ns
Δt	Input to Output Difference, $\lvert t_{PLH} - t_{PHL} \rvert$	LTC1545C (Figures 2, 5)	●	0	3	12	ns
		LTC1545I (Figures 2, 5)	●	0	3	17	ns
t_{SKEW}	Output to Output Skew	(Figures 2, 5)			3		ns
V.11 Receiver							
V_{TH}	Input Threshold Voltage	–7V ≤ V_{CM} ≤ 7V	●	–0.2		0.2	V
ΔV_{TH}	Input Hysteresis	–7V ≤ V_{CM} ≤ 7V	●		15	40	mV
I_{IN}	Input Current (A, B)	–10V ≤ $V_{A,B}$ ≤ 10V	●			±0.66	mA
R_{IN}	Input Impedance	–10V ≤ $V_{A,B}$ ≤ 10V	●	15	30		kΩ
t_r, t_f	Rise or Fall Time	(Figures 2, 6)			15		ns
t_{PLH}	Input to Output	LTC1545C (Figures 2, 6)	●		50	80	ns
		LTC1545I (Figures 2, 6)	●		50	90	ns
t_{PHL}	Input to Output	LTC1545C (Figures 2, 6)	●		50	80	ns
		LTC1545I (Figures 2, 6)	●		50	90	ns
Δt	Input to Output Difference, $\lvert t_{PLH} - t_{PHL} \rvert$	LTC1545C (Figures 2, 6)	●	0	4	16	ns
		LTC1545I (Figures 2, 6)	●	0	4	21	ns

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 5V, V_{DD} = 8V, V_{EE} = –7V for V.28, –5.5V for V.10, V.11 (Notes 2, 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V.10 Driver							
V_O	Output Voltage	Open Circuit, R_L = 3.9k	●	±4		±6	V
V_T	Output Voltage	R_L = 450Ω (Figure 3) R_L = 450Ω (Figure 3)	● ●	±3.6 0.9V_O			V
I_{SS}	Short-Circuit Current	V_O = GND				±150	mA
I_{OZ}	Output Leakage Current	–0.25V ≤ V_O ≤ 0.25V, Power Off or No-Cable Mode or Driver Disabled	●		±0.1	±100	µA
t_r, t_f	Rise or Fall Time	R_L = 450Ω, C_L = 100pF (Figures 3, 7)			2		µs
t_{PLH}	Input to Output	R_L = 450Ω, C_L = 100pF (Figures 3, 7)			1		µs
t_{PHL}	Input to Output	R_L = 450Ω, C_L = 100pF (Figures 3, 7)			1		µs
V.10 Receiver							
V_{TH}	Receiver Input Threshold Voltage		●	–0.25		0.25	V
ΔV_{TH}	Receiver Input Hysteresis		●		25	50	mV
I_{IN}	Receiver Input Current	–10V ≤ V_A ≤ 10V	●			±0.66	mA
R_{IN}	Receiver Input Impedance	–10V ≤ V_A ≤ 10V	●	15	30		kΩ
t_r, t_f	Rise or Fall Time	(Figures 4, 8)			15		ns
t_{PLH}	Input to Output	(Figures 4, 8)			55		ns
t_{PHL}	Input to Output	(Figures 4, 8)			109		ns
Δt	Input to Output Difference, $\lvert t_{PLH} - t_{PHL} \rvert$	(Figures 4, 8)			60		ns
V.28 Driver							
V_O	Output Voltage	Open Circuit R_L = 3k (Figure 3)	● ●	 ±5	 ±8.5	±10	V V
I_{SS}	Short-Circuit Current	V_O = GND	●			±150	mA
I_{OZ}	Output Leakage Current	–0.25V ≤ V_O ≤ 0.25V, Power Off or No-Cable Mode or Driver Disabled	●		±1	±100	µA
SR	Slew Rate	R_L = 3k, C_L = 2500pF (Figures 3, 7)	●	4		30	V/µs
t_{PLH}	Input to Output	R_L = 3k, C_L = 2500pF (Figures 3, 7)	●		1.3	2.5	µs
t_{PHL}	Input to Output	R_L = 3k, C_L = 2500pF (Figures 3, 7)	●		1.3	2.5	µs
V.28 Receiver							
V_{THL}	Input Low Threshold Voltage		●		1.5	0.8	V
V_{TLH}	Input High Threshold Voltage		●	2	1.6		V
ΔV_{TH}	Receiver Input Hysterisis		●		0.1	0.3	V
R_{IN}	Receiver Input Impedance	–15V ≤ V_A ≤ 15V	●	3	5	7	kΩ
t_r, t_f	Rise or Fall Time	(Figures 4, 8)			15		ns
t_{PLH}	Input to Output	(Figures 4, 8)	●		60	100	ns
t_{PHL}	Input to Output	(Figures 4, 8)	●		150	450	ns

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: All currents into device pins are positive; all currents out of device are negative. All voltages are referenced to device ground unless otherwise specified.

Note 3: All typicals are given for V_{CC} = 5V, V_{DD} = 8V, V_{EE} = –7V for V.28, –5.5V for V.10, V.11 and T_A = 25°C.

PIN FUNCTIONS

V_{CC} (Pins 1, 19): Positive Supply for the Transceivers. 4.75V ≤ V_{CC} ≤ 5.25V. Connect a 1µF capacitor to ground.

V_{DD} (Pins 2, 20): Positive Supply Voltage for V.28. Connect to V_{DD} Pin 3 on LTC1543 or 8V supply. Connect a 1µF capacitor to ground.

D1 (Pin 3): TTL Level Driver 1 Input.

D2 (Pin 4): TTL Level Driver 2 Input.

D3 (Pin 5): TTL Level Driver 3 Input.

R1 (Pin 6): CMOS Level Receiver 1 Output.

R2 (Pin 7): CMOS Level Receiver 2 Output.

R3 (Pin 8): CMOS Level Receiver 3 Output.

D4 (Pin 9): TTL Level Driver 4 Input.

R4 (Pin 10): CMOS Level Receiver 4 Output.

M0 (Pin 11): TTL Level Mode Select Input 0 with Pull-Up to V_{CC}.

M1 (Pin 12): TTL Level Mode Select Input 1 with Pull-Up to V_{CC}.

M2 (Pin 13): TTL Level Mode Select Input 2 with Pull-Up to V_{CC}.

DCE/$\overline{\text{DTE}}$ (Pin 14): TTL Level Mode Select Input with Pull-Up to V_{CC}. Logic high enables Driver 3. Logic low enables Receiver 1.

D4ENB (Pin 15): TTL Level Enable Input with Pull-Up to V_{CC}. Logic low enables Driver 4.

R4EN (Pin 16): TTL Level Enable Input with Pull-Up to V_{CC}. Logic high enables Receiver 4.

R5 (Pin 17): CMOS Level Receiver 5 Output.

D5 (Pin 18): TTL Level Driver 5 Input.

D5 A (Pin 21): Driver 5 Output.

R5 A (Pin 22): Receiver 5 Input.

R4 A (Pin 23): Receiver 4 Input.

D4 A (Pin 24): Driver 4 Input.

R3 B (Pin 25): Receiver 3 Noninverting Input.

R3 A (Pin 26): Receiver 3 Inverting Input.

R2 B (Pin 27): Receiver 2 Noninverting Input.

R2 A (Pin 28): Receiver 2 Inverting Input.

D3/R1 B (Pin 29): Receiver 1 Noninverting Input and Driver 3 Noninverting Output.

D3/R1 A (Pin 30): Receiver 1 Inverting Input and Driver 3 Inverting Output.

D2 B (Pin 31): Driver 2 Noninverting Output.

D2 A (Pin 32): Driver 2 Inverting Output.

D1 B (Pin 33): Driver 1 Noninverting Output.

D1 A (Pin 34): Driver 1 Inverting Output.

GND (Pin 35): Ground.

V_{EE} (Pin 36): Negative Supply Voltage. Connect to V_{EE} Pin 26 on LTC1543. Connect a 1µF capacitor to ground.

TEST CIRCUITS

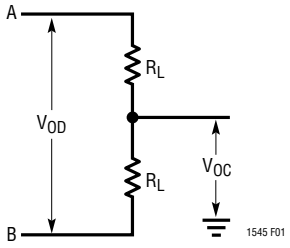

Figure 1. V.11 Driver Test Circuit

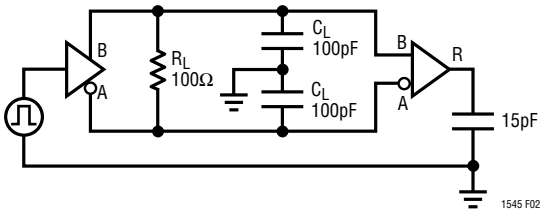

Figure 2. V.11 Driver/Receiver AC Test Circuit

TEST CIRCUITS

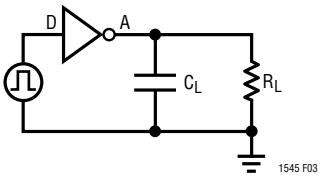

Figure 3. V.10/V.28 Driver Test Circuit

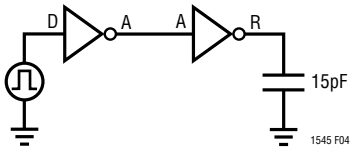

Figure 4. V.10/V.28 Receiver Test Circuit

MODE SELECTION

LTC1545 MODE NAME	M2	M1	M0	D1	D2	(Note 1) D3	(Note 2) D4	D5	(Note 1) R1	R2	R3	(Note 3) R4	R5
Not Used (Default V.11)	0	0	0	V.11	V.11	V.11	V.10	V.10	V.11	V.11	V.11	V.10	V.10
RS530A	0	0	1	V.11	V.10	V.11	V.10	V.10	V.11	V.10	V.11	V.10	V.10
RS530	0	1	0	V.11	V.11	V.11	V.10	V.10	V.11	V.11	V.11	V.10	V.10
X.21	0	1	1	V.11	V.11	V.11	V.10	V.10	V.11	V.11	V.11	V.10	V.10
V.35	1	0	0	V.28	V.28	V.28	V.28	V.28	V.28	V.28	V.28	V.28	V.28
RS449/V.36	1	0	1	V.11	V.11	V.11	V.10	V.10	V.11	V.11	V.11	V.10	V.10
V.28/RS232	1	1	0	V.28	V.28	V.28	V.28	V.28	V.28	V.28	V.28	V.28	V.28
D4ENB = 1, R4EN = 0 M0 = M1 = M2 = 1	1	1	1	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z

Note 1: Driver 3 and Receiver 1 are enabled (and disabled) by $\overline{DCE}/DTE$ (Pin 14). Logic high enables Driver 3. Logic low enables Receiver 1.

Note 2: Driver 4 is enabled by D4ENB = 0 (Pin 15).

Note 3: Receiver 4 is enabled by R4EN = 1 (Pin 16).

SWITCHING TIME WAVEFORMS

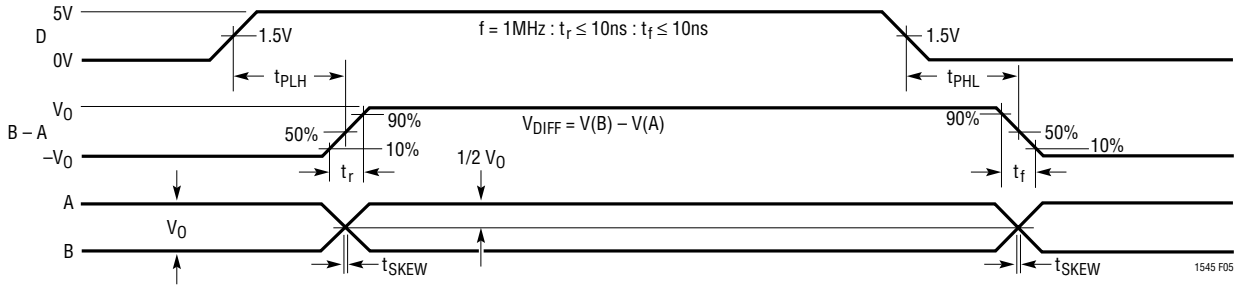

Figure 5. V.11 Driver Propagation Delays

SWITCHING TIME WAVEFORMS

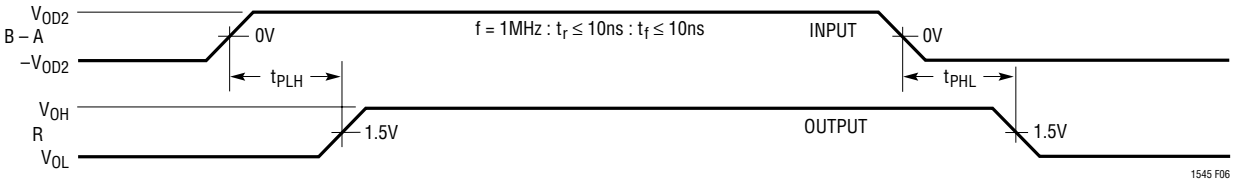

Figure 6. V.11 Receiver Propagation Delays

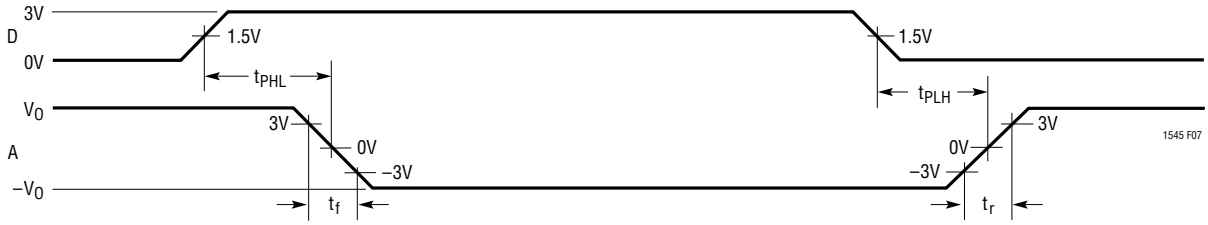

Figure 7. V.10, V.28 Driver Propagation Delays

Figure 8. V.10, V.28 Receiver Propagation Delays

APPLICATIONS INFORMATION

Overview

The LTC1543/LTC1545 form the core of a complete software-selectable DTE or DCE interface port that supports the RS232, RS449, EIA530, EIA530-A, V.35, V.36 or X.21 protocols. Cable termination may be implemented using the LTC1344A software-selectable cable termination chip or by using existing discrete designs.

A complete DCE-to-DTE interface operating in EIA530 mode is shown in Figure 9. The LTC1543 of each port is used to generate the clock and data signals. The LTC1545 is used to generate the control signals along with LL (Local Loop-Back), RL (Remote Loop-Back), TM (Test Mode) and RI (Ring Indicate). The LTC1344A cable termination chip is used only for the clock and data signals because they must support V.35 cable termination. The control signals do not need any external resistors.

Mode Selection

The interface protocol is selected using the mode select pins M0, M1 and M2 (see the Mode Selection table).

For example, if the port is configured as a V.35 interface, the mode selection pins should be M2 = 1, M1 = 0, M0 = 0. For the control signals, the drivers and receivers will operate in V.28 (RS232) electrical mode. For the clock and data signals, the drivers and receivers will operate in V.35 electrical mode. The DCE/$\overline{\text{DTE}}$ pin will configure the port for DCE mode when high, and DTE when low.

The interface protocol may be selected simply by plugging the appropriate interface cable into the connector. The mode pins are routed to the connector and are left unconnected (1) or wired to ground (0) in the cable as shown in Figure 10.

APPLICATIONS INFORMATION

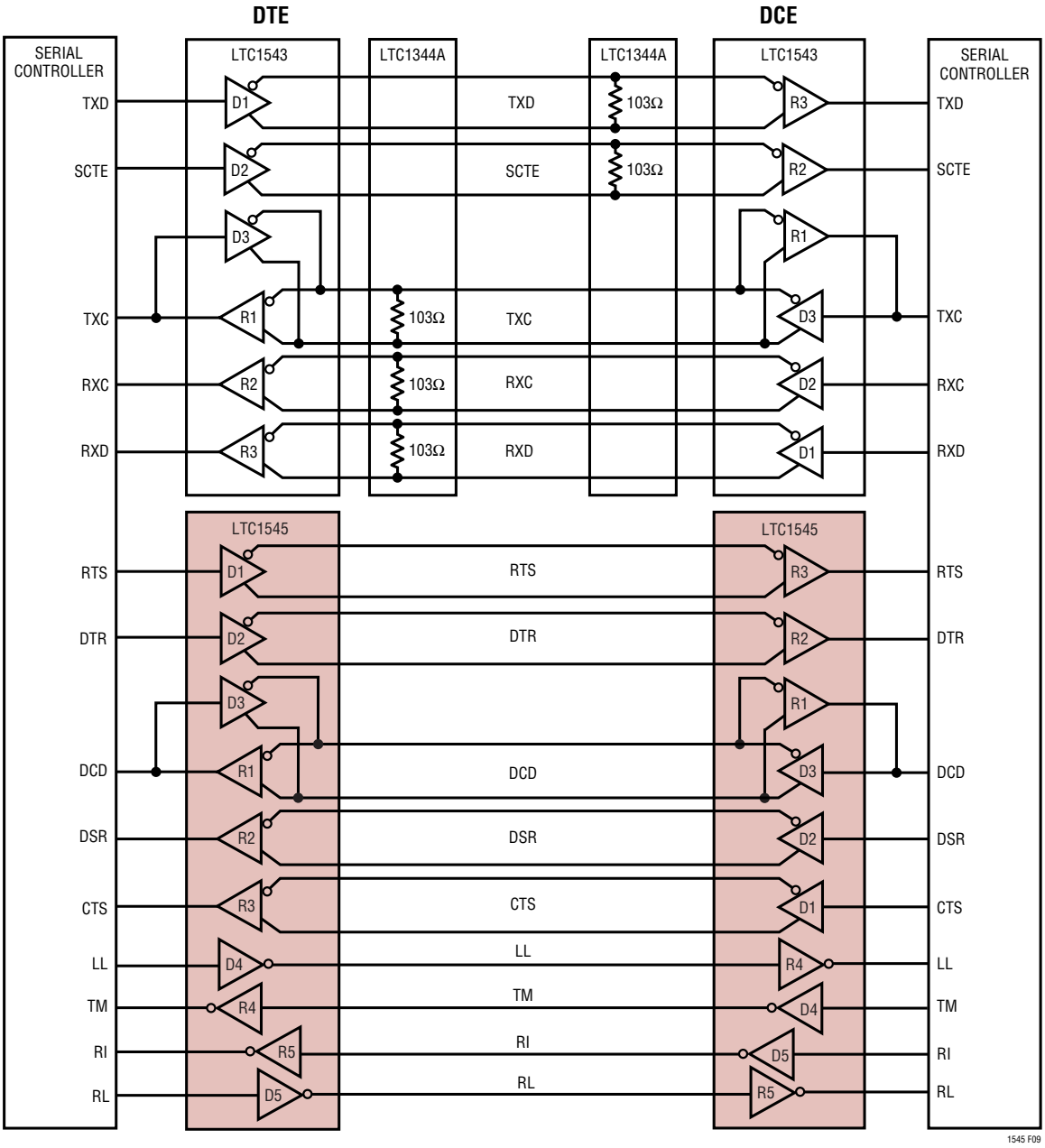

Figure 9. Complete Multiprotocol Interface in EIA530 Mode

The internal pull-up current sources will ensure a binary 1 when a pin is left unconnected and that the LTC1543/LTC1545 and the LTC1344A enter the no-cable mode when the cable is removed. In the no-cable mode the LTC1543/LTC1545 supply current drops to less than 200μA and all LTC1543/LTC1545 driver outputs and LTC1344A resistive terminations are forced into a high impedance state.

The mode selection may also be accomplished by using jumpers to connect the mode pins to ground or V_{CC}.

Cable Termination

Traditional implementations have included switching resistors with expensive relays, or required the user to change termination modules every time the interface standard has changed. Custom cables have been used

APPLICATIONS INFORMATION

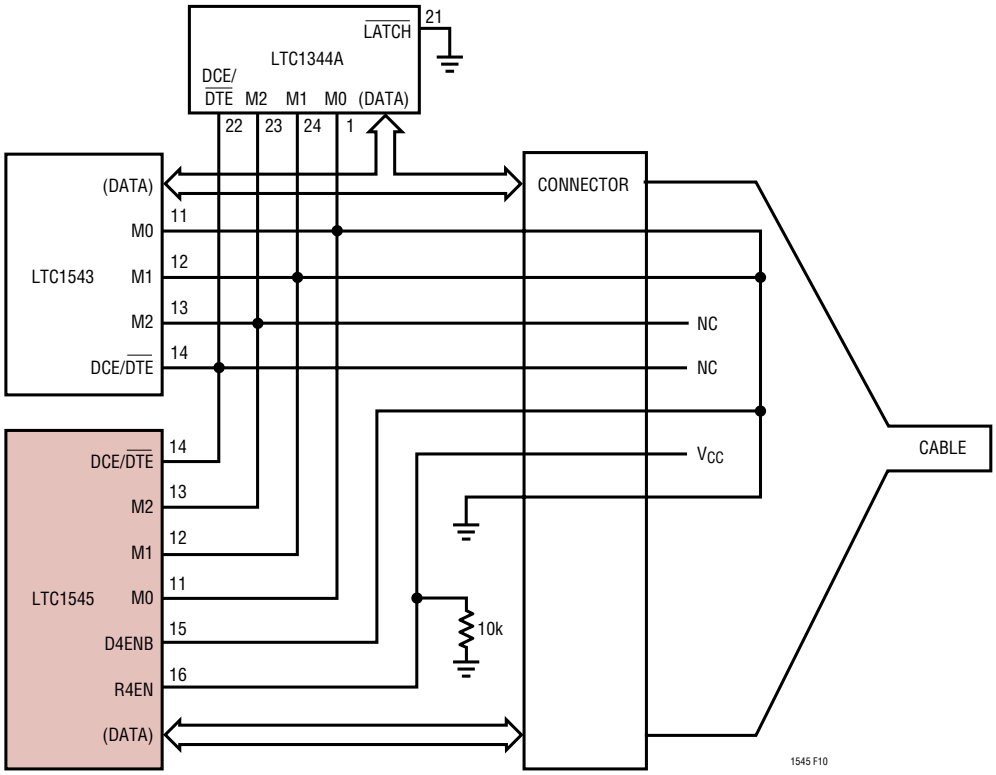

Figure 10: Single Port DCE V.35 Mode Selection in the Cable

with the termination in the cable head or separate terminations are built on the board and a custom cable routes the signals to the appropriate termination. Switching the terminations with FETs is difficult because the FETs must remain off even though the signal voltage is beyond the supply voltage for the FET drivers or the power is off.

Using the LTC1344A along with the LTC1543/LTC1545 solves the cable termination switching problem. Via software control, the LTC1344A provides termination for the V.10 (RS423), V.11 (RS422), V.28 (RS232) and V.35 electrical protocols.

V.10 (RS423) Interface

A typical V.10 unbalanced interface is shown in Figure 11. A V.10 single-ended generator output A with ground C is connected to a differential receiver with inputs A' connected to A, and input C' connected to the signal return ground C. Usually, no cable termination is required for V.10 interfaces, but the receiver inputs must be compliant with the impedance curve shown in Figure 12.

The V.10 receiver configuration in the LTC1545 is shown in Figure 13. In V.10 mode switch S3 inside the LTC1545 is turned off. The noninverting input is disconnected inside the LTC1545 receiver and connected to ground.The cable termination is then the 30k input impedance to ground of the LTC1545 V.10 receiver.

V.11 (RS422) Interface

A typical V.11 balanced interface is shown in Figure 14. A V.11 differential generator with outputs A and B with ground C is connected to a differential receiver with ground C', inputs A' connected to A, B' connected to B. The V.11 interface has a differential termination at the receiver end that has a minimum value of 100Ω. The termination resistor is optional in the V.11 specification, but for the high speed clock and data lines, the termination is required to prevent reflections from corrupting the data. The receiver inputs must also be compliant with the impedance curve shown in Figure 12.

APPLICATIONS INFORMATION

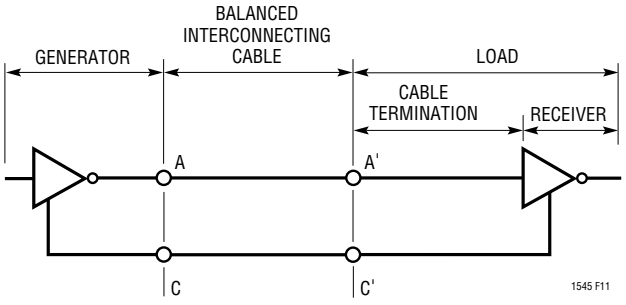

Figure 11. Typical V.10 Interface

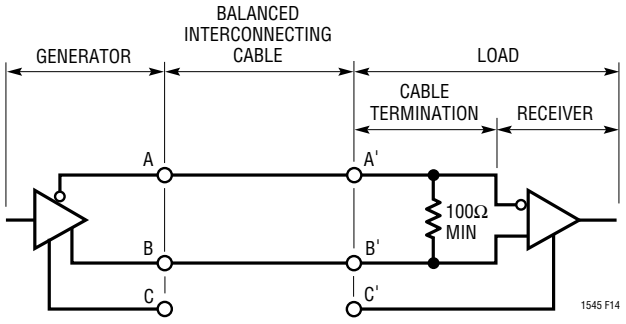

Figure 14. Typical V.11 Interface

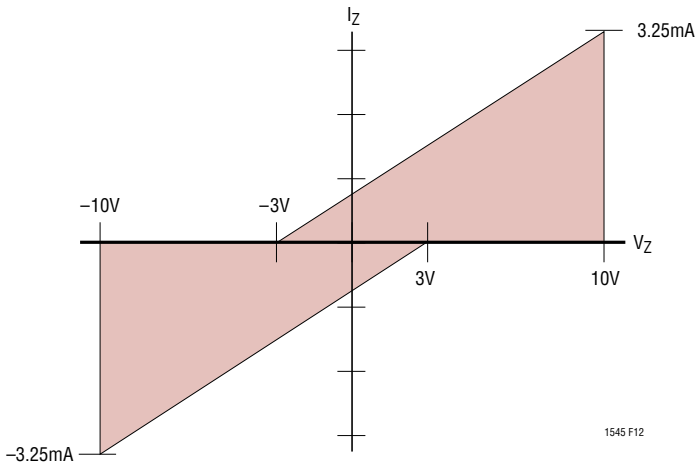

Figure 12. V.10 Receiver Input Impedance

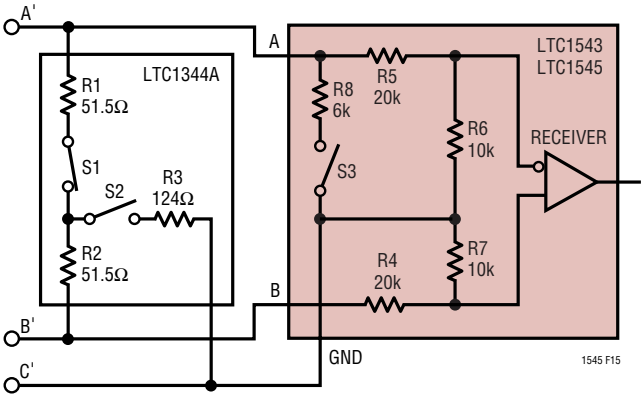

Figure 15. V.11 Receiver Configuration

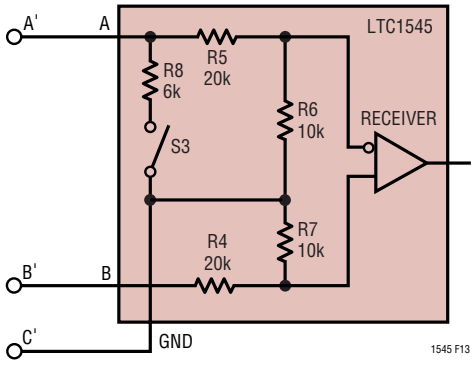

Figure 13. V.10 Receiver Configuration

In V.11 mode, all switches are off except S1 inside the LTC1344A which connects a 103Ω differential termination impedance to the cable as shown in Figure 15.

V.28 (RS232) Interface

A typical V.28 unbalanced interface is shown in Figure 16. A V.28 single-ended generator output A with ground C is connected to a single-ended receiver with input A' connected to A, ground C' connected via the signal return ground C.

In V.28 mode, all switches are off except S3 inside the LTC1543/LTC1545 which connects a 6k (R8) impedance to ground in parallel with 20k (R5) plus 10k (R6) for a combined impedance of 5k as shown in Figure 17. The noninverting input is disconnected inside the LTC1543/LTC1545 receiver and connected to a TTL level reference voltage for a 1.4V receiver trip point.

APPLICATIONS INFORMATION

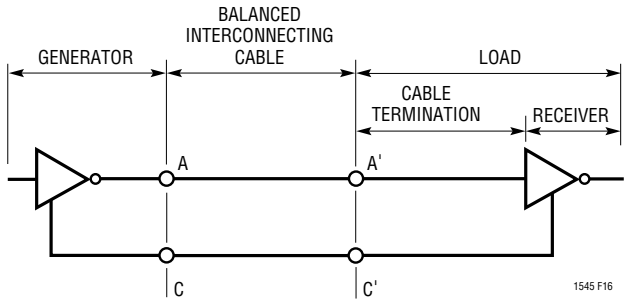

Figure 16. Typical V.28 Interface

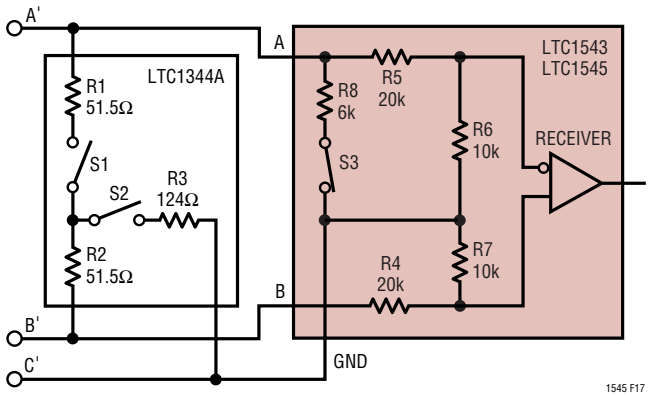

Figure 17. V.28 Receiver Configuration

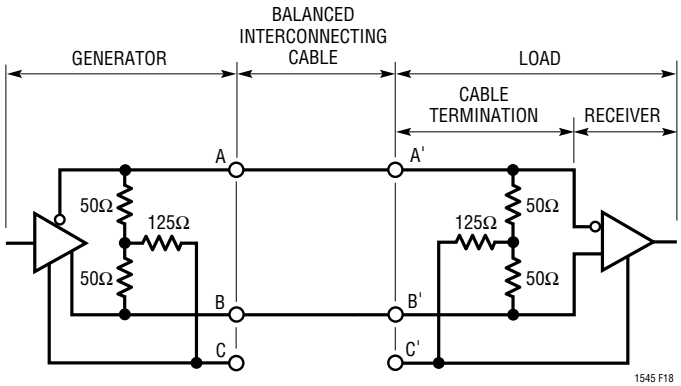

Figure 18. Typical V.35 Interface

V.35 Interface

A typical V.35 balanced interface is shown in Figure 18. A V.35 differential generator with outputs A and B with ground C is connected to a differential receiver with ground C', inputs A' connected to A, B' connected to B. The V.35 interface requires a T or delta network termination at the receiver end and the generator end. The receiver differential impedance measured at the connector must be 100Ω ±10Ω, and the impedance between shorted terminals (A' and B') and ground C' must be 150Ω ±15Ω.

In V.35 mode, both switches S1 and S2 inside the LTC1344A are on, connecting the T network impedance as shown in Figure 19. Both switches in the LTC1543 are off. The 30k input impedance of the receiver is placed in parallel with the T network termination, but does not affect the overall input impedance significantly.

The generator differential impedance must be 50Ω to 150Ω and the impedance between shorted terminals (A and B) and ground C must be 150Ω ±15Ω. For the generator termination, switches S1 and S2 are both on and the top side of the center resistor is brought out to a pin so it can be bypassed with an external capacitor to reduce common mode noise as shown in Figure 20.

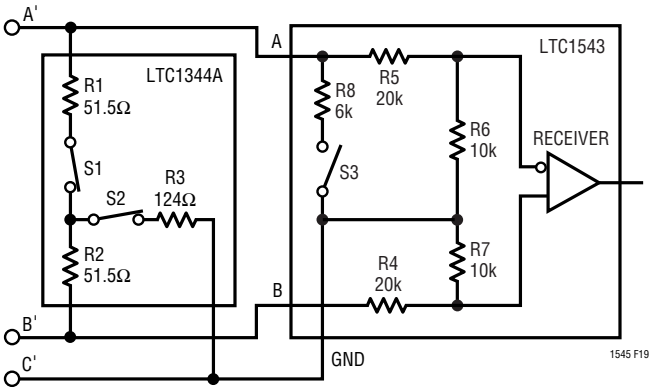

Figure 19. V.35 Receiver Configuration

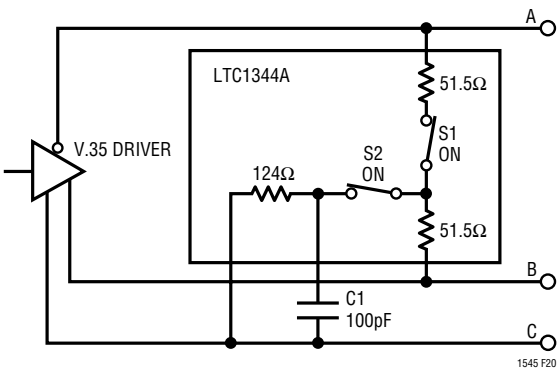

Figure 20. V.35 Driver Using the LTC1344A

APPLICATIONS INFORMATION

Any mismatch in the driver rise and fall times or skew in the driver propagation delays will force current through the center termination resistor to ground, causing a high frequency common mode spike on the A and B terminals. The common mode spike can cause EMI problems that are reduced by capacitor C1 which shunts much of the common mode energy to ground rather than down the cable.

No-Cable Mode

The no-cable mode (M0 = M1 = M2 = D4ENB = 1, R4EN = 0) is intended for the case when the cable is disconnected from the connector. The charge pump, bias circuitry, drivers and receivers are turned off, the driver outputs are forced into a high impedance state, and the supply current drops to less than 200µA.

Charge Pump

The LTC1543 uses an internal capacitive charge pump to generate V_{DD} and V_{EE} as shown in Figure 21. A voltage doubler generates about 8V on V_{DD} and a voltage inverter generates about –7.5V for V_{EE}. Four 1µF surface mounted tantalum or ceramic capacitors are required for C1, C2, C3 and C4. The V_{EE} capacitor C5 should be a minimum of 3.3µF. All capacitors are 16V and should be placed as close as possible to the LTC1543 to reduce EMI. The turn-on time for the charge pump is 60ms.

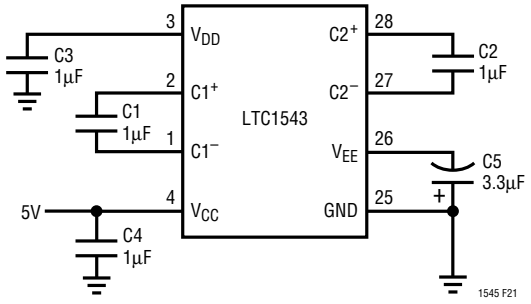

Figure 21. Charge Pump

Receiver Fail-Safe

All LTC1543/LTC1545 receivers feature fail-safe operation in all modes. If the receiver inputs are left floating or shorted together by a termination resistor, the receiver output will always be forced to a logic high.

DTE vs DCE Operation

The DCE/$\overline{\text{DTE}}$ pin acts as an enable for Driver 3/Receiver 1 in the LTC1543, and Driver 3/Receiver 1 in the LTC1545.

The LTC1543/LTC1545 can be configured for either DTE or DCE operation in one of two ways: a dedicated DTE or DCE port with a connector of appropriate gender, or a port with one connector that can be configured for DTE or DCE operation by rerouting the signals to the LTC1543/LTC1545 using a dedicated DTE cable or dedicated DCE cable.

A dedicated DTE port using a DB-25 male connector is shown in Figure 22. The interface mode is selected by logic outputs from the controller or from jumpers to either V_{CC} or GND on the mode select pins. A dedicated DCE port using a DB-25 female connector is shown in Figure 23.

A port with one DB-25 connector, can be configured for either DTE or DCE operation is shown in Figure 24. The configuration requires separate cables for proper signal routing in DTE or DCE operation. For example, in DTE mode, the TXD signal is routed to Pins 2 and 14 via Driver 1 in the LTC1543. In DCE mode, Driver 1 now routes the RXD signal to Pins 2 and 14.

Compliance Testing

A European standard EN 45001 test report is available for the LTC1343/LTC1545/LTC1344A chipset. A copy of the test report is available from LTC or TUV Telecom Services Inc. (formerly Detecon Inc.)

The title of the report is:

Test Report No. NET2/071601/98.

The address of TUV Telecom Services Inc. is:

TUV Telecom Services Inc.
Suite 107
1775 Old Highway 8
St. Paul, MN 55112 USA
Tel. +1 (612) 639-0775
Fax. +1 (612) 639-0873

TYPICAL APPLICATIONS

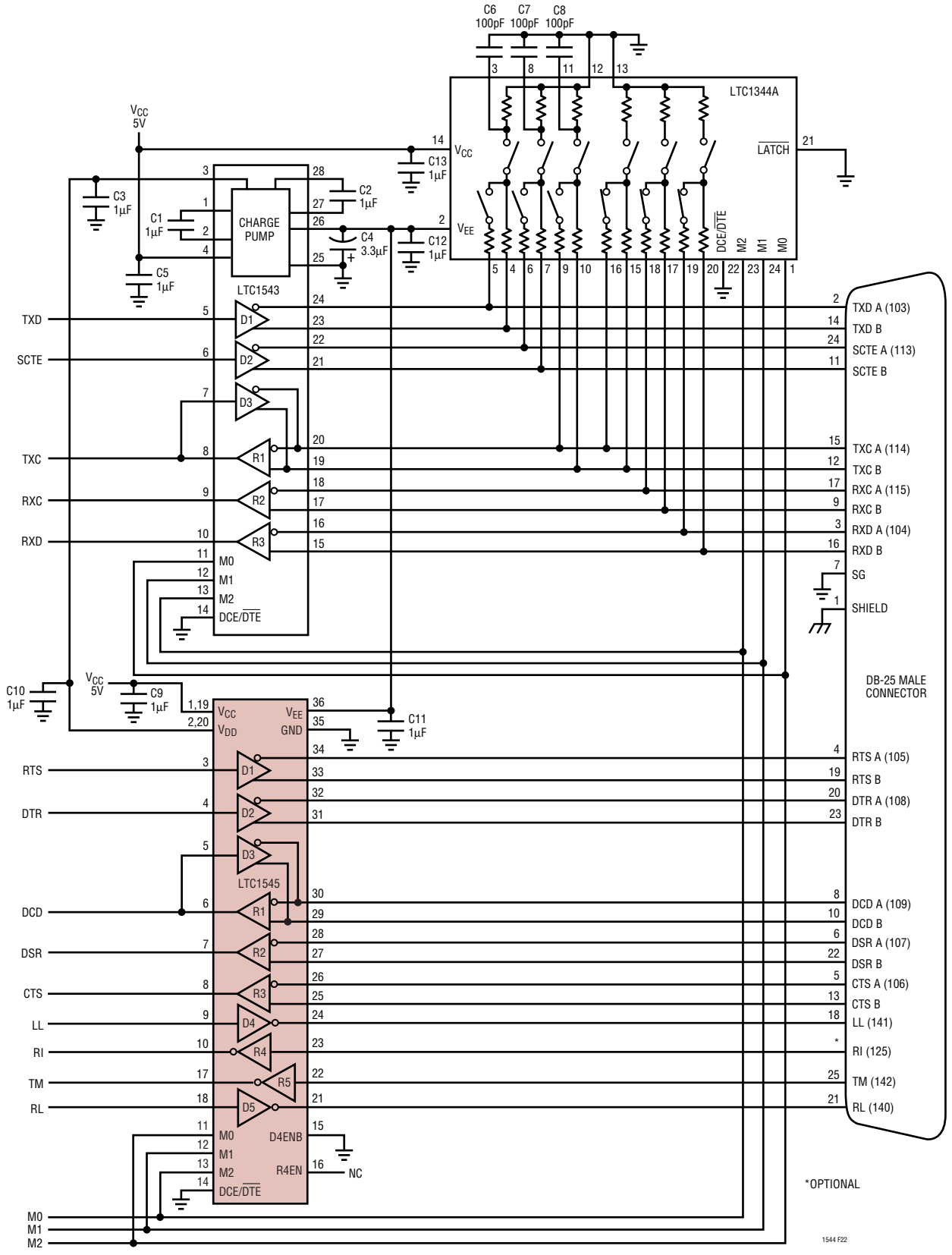

Figure 22. Controller-Selectable Multiprotocol DTE Port with DB-25 Connector

TYPICAL APPLICATIONS

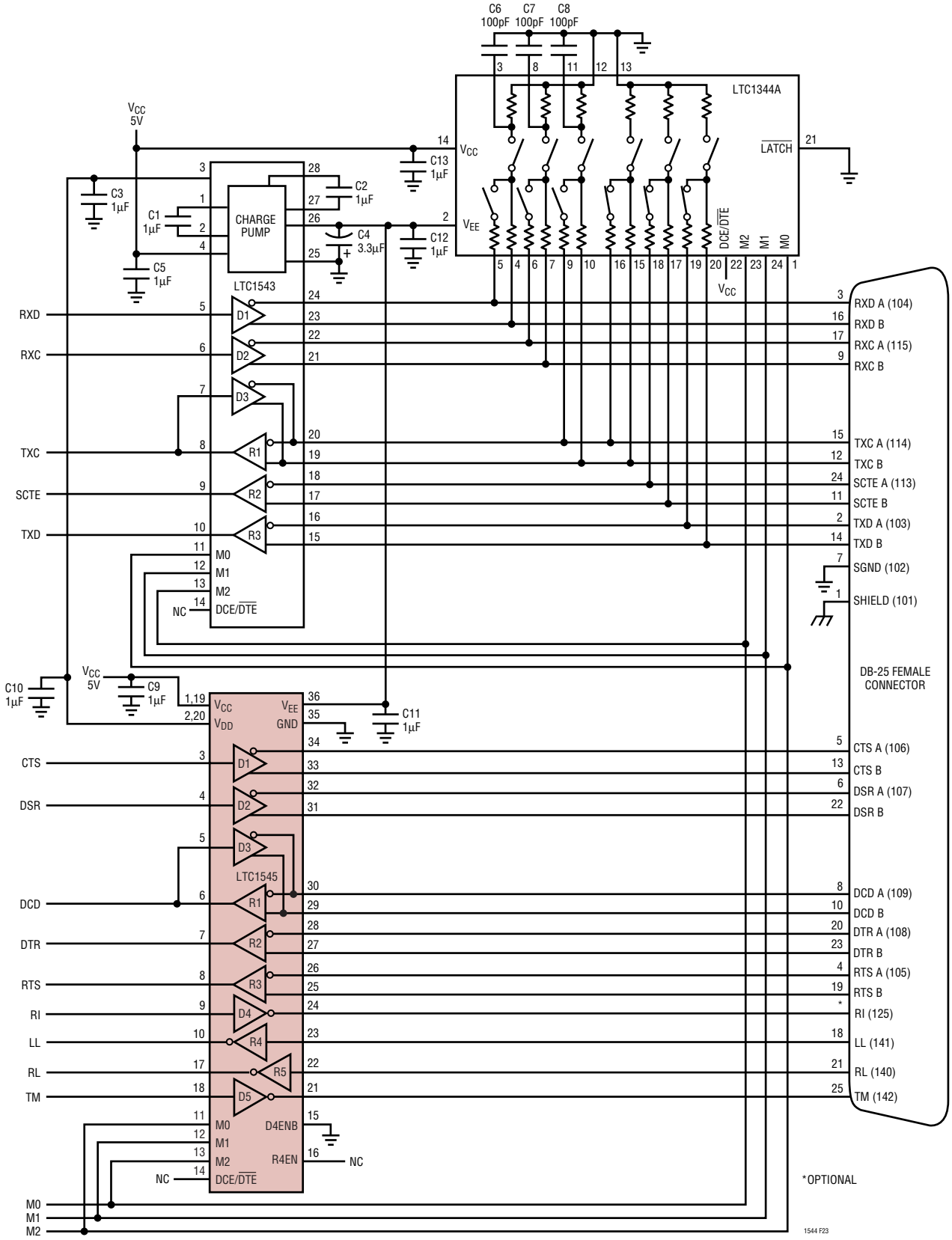

Figure 23. Controller-Selectable DCE Port with DB-25 Connector

TYPICAL APPLICATIONS

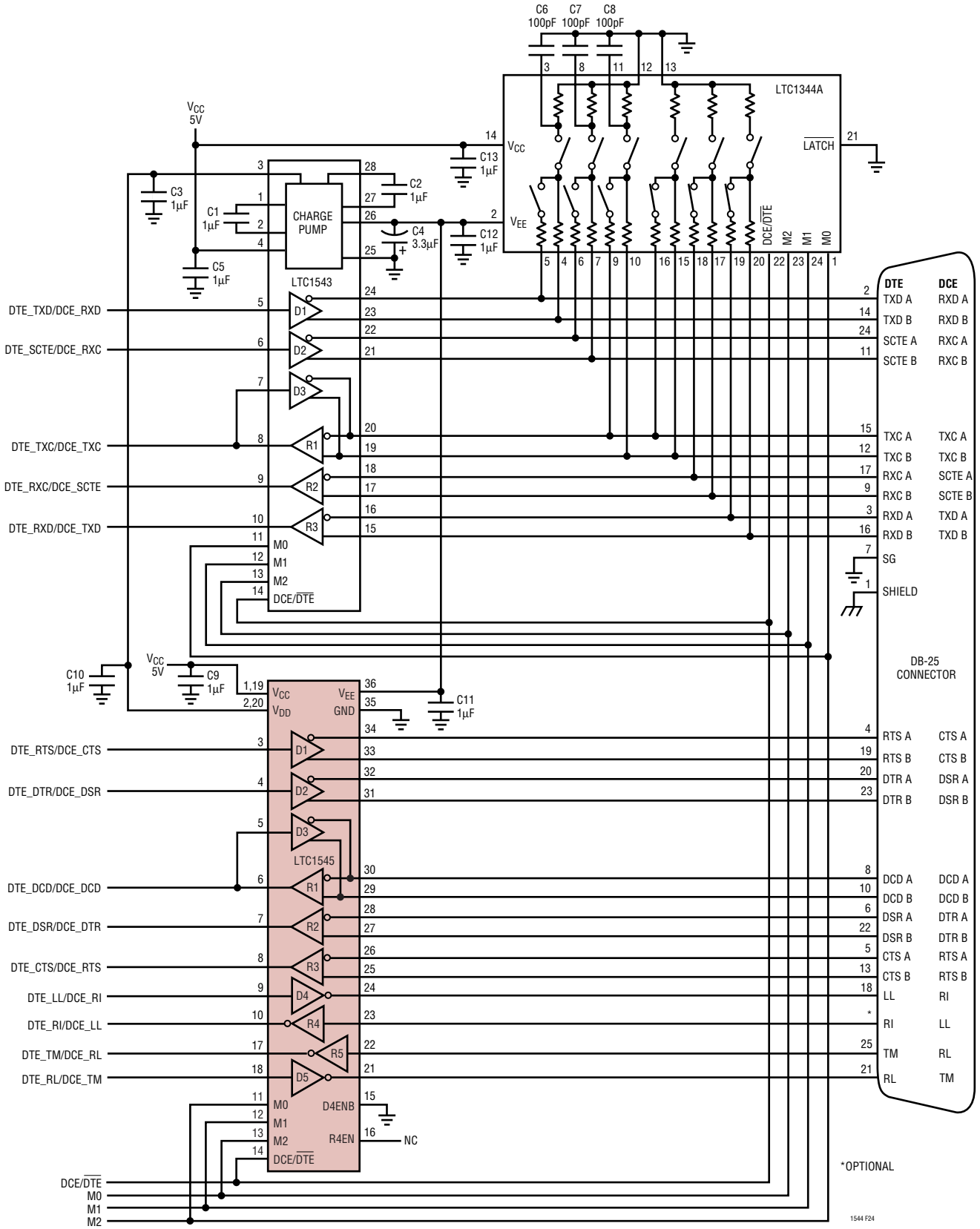

Figure 24. Controller-Selectable Multiprotocol DTE/DCE Port with DB-25 Connector